# Near East University 



# Computer Engineering <br> Department 

Special project<br>Com 400

## Practical Implementation Of <br> Memory Interfacing

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## INTRODUCTION

Memory is another image for the human memory, it does the same process from storing and deleting the information, with the advantage of that the processed information within the memory is kept in the storage until it has to be deleted intentionally, mean while the human memory is sometimes storing the information temporary without intention.

During the last decade, the information processing has been increasing very rapidly and the demand for memories with high capacity at information processing and storage has consequently increased. In this project I introduced the interfacing of memories to allow a microprocessor system to have more memory locations than the microprocessor is capable at addressing using some techniques.

## Chapter ONE

### 1.0 Microprocessors

### 1.1 A BRIEF HISTORY OF MICROPROCESSORS

The digital computer is controlled by a program, the program tells the digital computer how to process data $\ldots$ etc. It does this by using the digital computer calculation logic, memory circuit, and input/output device, which is called digital computer architecture. The microprocessor has architecture similar to the digital computer.

In 1950s, the first general-purpose digital computer appeared. They used vacuum tubes models were used to build basic circuit such as gates and flipflops. By assembling gate and flip-flops built the computers calculating logic and memory circuits. Nevertheless, the early computers introduced important idea of program storage. Later design provided computer with program storage.

Solid-state circuit technology also made great strides during 1950s. The knowledge of semiconductors increased. Naturally, the designers of digital computers jumped at the chance to replace vacuum tubes with transistor. In the early 1960 s, the art of building solid-state computers advanced. They were building huge solid-state computers that still required large air-condition
rooms. They could process large amount of data. Moving in a new direction were smaller companies they began building small computers, about the size of a disk.

By the early 1960 s, the semiconductor industry found away to put a number of transistors on one silicone wafer. The transistor are connected together with small metal traces, to perfume a function, such as a gate, flipflop, register, or adder the building blocks or circuit modules made this way are called an integrated circuit (IC).

By the mid-1960s, small-and medium-scale integration (SSI and MSI) produced major families of digital logic. The late 1960s and early 1970s saw large-scale integration ( LSI ). By the 1980s, very large scale integration (VLSI ) gave us ICs with over 100,000 transistors.

The development of electronic calculator shows the dramatic improvement in large scale integration. Development achieved great technology such that assembled to a microprocessor the microprocessor made possible the manufacture of powerful calculators and many other products.

Since the early 1970 s, the main effort has been to improve the microprocessor's architecture. Important evaluations of architecture design increases the microprocessor's speed and computing power. The early microprocessor processed digital data 4 bits ( 4 binary digits ) at a time. That is they used a 4-bit word. But new generations of microprocessors came fast.

The 4-bit microprocessor grew into 8 -bit, then into $\mathbf{1 6}$-bit, and then into $\mathbf{3 2}$ bit Microprocessors. During the early 1980s, complete 8-bit microprocessor system (microprocessor with memory and communication ability ) were developed.

### 1.2 THE MOTOROLA MC 6800 MPs

The MC6800 microprocessor was introduced by Motorola. it is an 8-bit microprocessor functionally having an 16-bits address bus. The programming model for the 6800 is shown in figure 1. Such as $68 \mathrm{HCl1}$, includes an 8 -bit microprocessor, a Timer, ROM, Ram, A/D Counter, and a Chip Oscillator. The functionality providing also programmable I/O lines and an EXROM.

The M6800 is an advanced 16-bit microprocessor. Other member of Motorola family are the 68 HC 000 ( CMOS ), 68008, 68010, 68020, and 68030. The 68000 microprocessor features are 32 -bit internal architecture, with a 16 -bit external data bus and it can address $16-\mathrm{MB}$ memory. The 68010 is an update 16 -bit external/32 internal virtual memory ( A programmer can write as if memory capacity is unlimited) MPU. The 68020 support 32 internal / external.

### 1.3 A Typical 6800 Microcomputer System



## MPU ( Microprocessor Unit )

Inside the MPU there three major functional blocks : ALU (the arithmeticlogic unit), Data Registers, and the control logic.

## Clock $\$ 1, \phi 2$

$\phi 1$ : Supply the required clock cycles to increment the internal register
\$2: Provides the necessary clock cycle to fetch and execute an Iinstructure.

ROM: Is a read only memory containing monitor suprotines
display routines tines and timer control subroutines.(see chapter 2).
RAM: Random Access memory $\mathrm{R} / \mathrm{W}$ where the program is execute (see chapter 2).

PIA (Peripheral Interface Adapter):
Has two I/O ports. Each ports is 8-bit Port A, Port B. Both Port A and Port B cab be programmed to interface I/O device (see chapter 3).

## System Description

The MC6800 required a +5 V power supply and an external two phase clock ( $\phi 1, \phi 2$ ). The restart input the MC6800 has H/W interrupt connects to the RESET PIN of the chip. This pin initialized the MPU for start operation. The MPU has 16 address line and 8 bi-directional data lines. The control lines added to the system is used to control the timing control how the information how the information transfer from RAM, ROM, and ALU. The interfacing between the MPU and the I/O devices is done with the PIA. The PIA provides two 8-bit data paths which can be used as input or output ports. The PIA also has 4 control lines between the PIA and the I/O devices.

The 6820/6821 PIA has internal register which makes it programmable and provide temporary storage to simplify the transfer of data. Thus the interrupt pluses can be send from the PA via the control bus to the MPU. In this way the PIA forms a two way communication link and a temporary storage device between the microprocessor and the peripheral device.

### 1.4 THE MC6800 PIN DIAGRAM AND FUNCTIONS



The Motorola 6800 is an 8 -bit microprocessor placed in 40 bin DIP (Duel In Line Package).

| PIN Name | Description | State Type |
| :---: | :---: | :---: |
| A0-A1O | Address Line | TriState, Output, Unidiriction |
| D0-D7 | Data Bus Lines | TriState, Bidirection |
| $\overline{\text { HALT }}$ | HALT | Input |
| TSC | Three State Control | Input |
| $\overline{\mathrm{R} / \mathrm{W}}$ | Read/Write Pin | TriState, Output |
| VMA | Valid Memory Add. | Output |
| DBE | Data Bus Available | Input |
| BA | Bus Available | Output |
| $\overline{\text { IRQ }}$ | Interrupt Request | Input |
| $\overline{\text { RESET }}$ | Reset Pin | Input |
| NMI | Non Maskable Int. | Input |
| ¢1, $\mathbf{\$ 2}^{2}$ | Two OverLooping |  |
|  | Clock Signal | Input |
| Vss,VCC | Power Input | Input |

### 1.5 MICROPROCESSOR INTERFACING

Most microprocessor in a stand alone fashion don't contain substantial memory. To increase the power of microprocessor, we have to interface I/O modules. The interfacing or leakage, of the port within the system called interfacing includes synchronization direction of transmission, and sometimes the adjustment of signal levels.

Interfacing deal with synchronization of data to and from the microprocessor unit, and there the $\mathrm{S} / \mathrm{W}$ as well the $\mathrm{H} / \mathrm{W}$ must be considered in great detail. Data transfers in and out of the microprocessor unit over the busses are :-

1- Memory Read
2- Memory write
3- I/O Read/Write
4- Interrupt or reset handling
Generally microprocessor is the focus of all operations. But in some case the MPU releases control of the address and data bus so that the peripheral device may access the main system memory directly going to the MPU, this is called DMA.

The MP itself uses MPU, ROM, and RAM externally, and it's of importance that the manufacturer produce peripheral interface adapters that are compatible with other MPUs. These are generally general purpose in that they can programmed to function as either input or output interface programmable communication device.

Manufactures produce specialized interface component IC's which are programmable DMA controllers, Programmable interrupt controllers, Diskette controllers, Synchrouns Data Link controller, and Keyboard display controller.

### 1.6 INTERFACING WITH ROM



FIG. 5

The data bus of MPU's is connected to the output of the ROM, and the address bus of the MPU is connected to the address inputs of the ROM.

The simple Red line $\overline{\mathbf{( R D}})$ output from the MPU is connected to the $\overline{\mathbf{O E}}$ of the ROM. $\overline{\mathrm{OE}}$ controls the data output from the ROM device. When activated the outputs of the ROM device is valid and when disabled the outputs of the ROM device is cut from the data bus. That is there is no response at the output of the ROM. For the MPU to access data from the ROM it has to set the address on the address bus frem A0-A11, set OE low using the read controt line, and set the CS line low sing the address decoder. In the MPU model of 6800 the decodes circuit was externally connected to the ROM. The ROM it self has a decoder mechanism so that, internally it could decode the selected address coming from the address bus. The CS line is used to select the line chip to be used. If CS line is hold low, that device is valid to be used.

The functionality of the decoder is great, such that it selects the memory range to be used. Since there are 4 address line connected to the decoder, there could be 16 device that could be interfaced to the MPU.

If each ROM device is 4 K , this makes a total of $16 \times 4 \mathrm{~K}=64 \mathrm{~K}$. But all of the ROM devices share the same address bus the data bus which is connected having the same characteristics of the address bus.

Simple configuration of interfacing the address bus and the data bus is the wired or connection of each parallel line. But this interfacing technique has the disadvantage that we can not access all the ROM devices at the same time. We could only use them by address interchange provided by the address decoder.

The advantage is that we could interface more memory units to the MPU by sampling changing the decoder mechanism.

### 1.7 INTERFACING WITH RAM



FIG. 5

The interfacing technique is similar to the ROM interface, except that $\mathbf{R} / \mathbf{W}$ control line is added to the circuit. The data bus could be programmed in two ways. The decoder mechanism works in the same way, such that may RAM modules could be interfaced to the MPU by the modules select line (MS).

If we want to write to the RAM device, we bring the $\overline{\mathbf{R D}}$ line and the $\mathbf{R} / \overline{\mathbf{W}}$ line low. The $\mathbf{I} / \mathbf{O}$ parts of the RAM are internally programmed as inputs.

Hence, the MPU selects the data to be written to the required memory location and places the address on the address bus. To activate the RAM device to be used it's selected by address line A12-A15. The decoder selected the appropriate device to be used at the decoder output. Similarly to read from the RAM, initially WR line is held HIGH so that the I/O ports of the RAM are programmed as outputs. Data to be acted on is fitched from the data bus of the RAM, which is selected from the address line inputs.

## Chapter TWO

### 2.0 MEMORY

### 2.1 INTRODUCTION

In the previous section, we discussed in detail about MP stem.. Each of these system has a memory. In some systems, the memory is quite small. This system may only have enough memory locations(or bytes of memory) to hold the program and to store a few bytes of variable data.

In this section, we will look at memory hard ware, and both read-write memory and read-only memory. We will also discuss both dynamic and static memories and we will give a short definition of three kind of read only memories.

Finally in this section we will show some memories I / O bin diagram, decoder and memory organization using two $2 \mathrm{~K} \times 8$ RAM.

### 2.2 RAM (Random-Access Read Write Memories)

In today microprocessor, it is found that there is only one type of addressable memory space, And this is known as the microprocessor main memory. More ever, it is a R/W memory.

However, there are two major semiconductors technologies to build integration circuit memories, used today to build memory system in computers, and these are the Bipolar and the Metal Oxide semiconductor technology.

Bipolar memories are seldom use with microprocessor system. the advantage of bipolar memories is their very fast access time. They do have a number of disadvantage when compared with MOS ( Metal Oxide Semiconductor) memories. They draw a great deal of power, and there fewer memory bits for the same size silicon chip. The bipolar semiconductor fabrication process is much more complicated than the MOS process. This makes bipolar memory much more expensive than MOS memories. For this reasons, bipolar memories are used only for applications which can introduce great speeds.

MOS memories is by far the most common microcomputer system. There are two different ways to construct MOS memories integrated circuits. MOS memory circuits are either static or dynamic. often, you will see the abbreviation SRAM ( Static RAM) and DRAM ( Dynamic RAM ) used for static RAM and dynamic Ram.

Static memory system are simples to build, especially for small memory system. There are much easier to service. Dynamic memory system use lowercost integrated circuits but required more support circuits. Also, dynamic memories must refreshed regularly.

They are usually used in large memory system.

Both static and dynamic semiconductor technologies are steadily improving. This means than large memories are being made on the same size silicon wafer. As a result, memory is becoming less expensive.

### 2.3 ROM ( Read Only Memory)

The read only memory is a memory device which once set with a given bit pattern, can not be changed. Every microprocessor system must have some ROM, since every system must have at least enough built-in program to be lead its RAM with a program from a mass storage device such as magnetic type or disk.

However, there are three different types of ROM. They are ROM, EPROM, EEROM. Each of the four types is used for a different application.

ROM is a device with a bit pattern permanently fixed by the semiconductor manufactures. ROMs are only used in high-volume applications, because costume mask designs are expensive. Of course, once a part is masked, it may never be changed.

EPROM (erasable programmable read-only memory) can be programmed, erased, and reprogrammed by the user.

Although these devices are somewhat more expensive than ROMs, EPROMs do let the user change the bit battern as needed. EPROM's are supplied with microprocessor system whose functions will be changed by the user, by experience, decide exactly what the system should do.

EEAROM (electrically erasable read only memory). The EAROM can programmed and altered electrically. Un like the EPROM, the EAROM does not need an outside device in order to erased.

### 2.4 RAM I/O Pin Diagram \& Function



In this section we will see the bin diagram of RAM memories the bin diagram (see fig.in appendix) and expling each bin and it's function.

## Pin Name

1- A0-A10

2- D0-D7

3- CS

4- $\overline{\mathrm{WE}}$

5- OE

6- VCC

7- GND

8- N/C

## Function

Address inputs

Data input/output

Chip Select
Write enable input

Output enable input
Positive Supply ( $+5 v$ )

Negative Supply ( ground)

No Connection

## Chapter THREE

### 3.0 PIA ( Peripheral Interface Adapter )

### 3.1 Introduction:

The PIA provides the universal means of interfacing peripheral component to the MPU. The PIA is capable of interfacing the MPU to peripheral to peripheral through two 8-bit bi-directional peripheral data bus and 4 control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during the system initialization. Each of the peripheral data lines can be programmed as input and output, and each of the 4 control interrupt lines may be programmed for one or several control modules. This allows a high flexibility in the overall operation of the PIA.

### 3.2 The 6821 PIA Block Diagram and Function Description.



## INTERNAL REGISTER

There are six location within the PIA accessible to the MPU data bus : two Peripheral Register, two Data Direction Register, And two Control Register. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in table 1.

| RS1 | RS0 | Control Register Bit |  | Location Selection |
| :---: | :---: | :---: | :---: | :---: |
|  |  | CRA2 | CRB2 |  |
| 0 | 0 | 1 | $x$ | Peripheral Register A |
| 0 | 0 | 0 | $\times$ | Data Direction Register A |
| 0 | 1 | $x$ | $\times$ | Control Register A |
| 1 | 0 | $\times$ | 1 | Peripheral Register B |
| 1 | 0 | $\times$ | 0 | Data Direction Register B |
| 1 | 1 | $\times$ | $x$ | Control Register B |

## Initialization The PIA

A "Low" reset line has the effect of zeroing all the PIA registers. This will set PA0..PA7, PB0..PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

## Data Direction Registers (DDRA and DDRB)

The two Data Direction Register allow the MPU to control the direction of data through each corresponding peripheral data lines. A Data Direction Register bit set a " 0 " configures the corresponding peripheral data line as input; a " 1 " results in an output.

## Control Register (CRA and CRB)

The two Control Register (CRA and CRB) allows the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1, CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bit 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bit 6 and 7 of the two register are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1, or CB2. The format of the control words is shown in table 2 .

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IRQA1 | IRQA2 | CA2 <br> Control | DRRA <br> Access | CA1 <br> Control  |  |  |  |


| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IRQB1 | IRQB2 | CB2 <br> Control | DRRB <br> Access | CB1 <br> Control |  |  |  |

Table 2

## Data Direction Access Control Bit (CRA2 and CRB2)

Bit 2 in each control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

## Interrupt Flags (CRA6, CRA7, CRB6, CRB7)

The four interrupt flag bits are set by active transitions of signals on the four interrupt and Peripheral Control Lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section. Control of CA1 and CB1 Interrupt Lines (CRA0, CRB0, CRA1, and CRB1).

The two lowest order bits of the control register are used to control the interrupt input lines CA1 and CB1. Bits CRA0 and CRB0 are used to enable the MPU interrupt signals IRQA and IRQB, respectively. Bits CRAI and CRB1 determine the active transition of the interrupt input signals CA1 and CB1. Control of CA2 and CB2 Peripheral Control Lines ( CRA3, CRA4, CRA5, CRB3, CRB4, and CRB5).

Bit 3,4 , and 5 of the two control register are used to control the CA2 and CB2 Peripheral Control Lines. This bits determine if the control lines will be an interrupt input or an output control signal. if bit CRA5 (CRB5) is "0", CA2 (CB2) is an interrupt input lines similar to CA1 (CB1). When CRA5 (CRB5) is " 1 ", CA2 (CB2) becomes an output signal that may be used to control peripheral data
transfers. When in the output mode, CA2 and CB2 have slightly different characteristics.

### 3.3 ARCHITECTURE OF THE PIA

## Pin-out of the PIA



The figure shows a pin-out of the PIA. the PIA has 40 pins, which connect to the various busses. First, we'll discuss four pins on the control bus that are inputs to the PIA. The PIA has pins that supply its power: +5 V and the GND. The R/W pin is connected to the MPU's R/W pin and is high when the MPU is reading from the PIA and low when the MPU is writing to the PIA. The PIA has some internal registers, which we'll descuss later. A low voltage on the PIA's RESET pin clears all of its registers. (when a register or memory location is cleared, each bit is cleared to zero).

Right now we'll focus our attention on the data pins. The PIA acts as "gobetween" for the 6800 and one more peripherals, so it has two kinds of data pins: one kind for exchanging data with the microprocessor, and other for exchanging data with peripherals.

The PIA has 8 data pins (D0-D7) for exchanging data with the microprocessor. There are connected to the $6800, \mathrm{~s}$ bi-directional data bus.

In additional, the PIA has 16 peripheral data pins (PA0 through PA7 and PB0 through PB7) for sending and receiving data to from the peripheral devices. The peripheral data pins are organized into two sets into two sets of 8, called set A and set B , corresponding to sides A and B of the PIA.

Each Peripheral data line can be either an input or an output of the PIA, but not both at once. Peripheral data lines are programmed individually to be an input or an output, depending on what we need. These lines can be all inputs, all outputs, or any combination.

### 3.4 Registers of the PIA



The fig shows the registers of the PIA, its data lines, and its registers.
Besides 8 peripheral data lines, each of the A and B sides has three registers. Although there are subtle differences between the two sides, we won't discuss those differences in this project. We just look one side, which is side A. For our purpose we assume that whatever we say about side A goes for side B.

On side A, peripheral data register A, is called Data Register A (DRA), is an 8-bin register in the PIA that holds the current data to be input or output from the A side of the PIA.

To determine whether each bit in DRA is used for input or output, we use Data Direction Register A (DDRA). If a bit in DDRA is a 1 , then the corresponding bit is DRA will be an output; if 0 , an input.

Control Register A (CRA) allows the MPU to control the operation of the 2 peripheral control lines CA1, CA2. In addition it allows the MPU to enable the interrupt lines and monitor the status of the interrupt flag.

### 3.5 Peripheral data lines and Data Register A (CRA)

a- Side A of the PIA Using Eight Switches as input


A block diagram showing the communication between side A's peripheral data lines and a set of 8 switches to be used for input. The MPU can read the data input on the switches after the data has first passed through the PIA.

Here, "switch up" causes 1 to be input, and "switch down" causes 0 to be input. Thus all of switches up would all the MPU to read 11111111 ( $\$ \mathrm{FF}$ ), and all switches drown would allow the MPU to read 00000000 (\$00). In the above figure illustrates a typical case. At (1) the user inputs the value (in this case, $\$ \mathrm{C} 2$ ) on the switches. At (2) the date, $\$ \mathrm{C} 2$, goes to data register A via side A's peripheral data lines. At (3) the data gets onto the data bus via the PIA's internal bus. Then the MPU can read the data. In this case side A is set up for all 8 lines to be inputs. Once we have wired side A for all inputs, it would naturally stay that way until its rewired.

Alternatively, we could wire side A so that all 8 were outputs. For an output device, we'll use a Light-Emitting Diode (LED), a small device that produces a red light when turned on. LED's are very commonly used in microcomputer displays. An LED can be wired so that a 1 means "light on" and a 0 mean "light off". Or it can be wired in opposite way: $1=$ "light off" and $0=$ "light on".

## b- Side a of the PIA Using Eight LED's as Outputs



The Figure show's side A of the PIA wired through interface circuitry so that all 8 peripheral data lines are outputs to 8 LED's. In this case the MPU can write data into LED's by first passing the data through the PIA. Here, a 1 output by the MPU to the PIA causes an outputs of light on, and 0 causes light off. So if the MPU writes $11111111(\$ F F)$ all the lights will be turned on. And the writes $00000000(\$ 00)$, all the lights will turned off. The figure showen above illustrates a particular example. At (1) the MPU places the data (\$A7, in this case) onto the data bus. At (2) the date placed into DRA via the PIAs internal bus. At (3) the data is output onto the LED's through the PIAs side A eripheral data lines, and the binary number 10101110 (\$A7) appears as the pattern on the light.

We've shown of side A of the PIA being used for inputs and all outputs. But we can use each line individually for either input or output. We could wire 4 peripheral data line to switches and 4 to LED's or 7 to switches and 1 to an LED's or 3 to switches and 4 to LED's, and so on.

### 3.6 Configuring the PIA

Setting the peripheral data lines of the PIA to be inputs or outputs. Configure side A of the PIA, we use Data Direction Register A (DDRA) and Control Register A (CRA).

The Content of DDRA determine whether a peripheral data line is an input or output: a 0 means input, and 1 means an output. To set the A side for all input as we done in fig(...), DDRA had to loaded with all 1s, or \$FF hexadecimal. Loading different words into the data direction register will cause possible combinations of inputs and outputs.

### 3.7 ADDRESSING THE PIA

Each register of the PIA has an address, and it accessed like a memory location. To load a register in the PIA, we write a number to the register's address. And to examine the content of the PIA registers, we read the content of that register's address.

There are six register all together, three on each side. But a PIA requires only four address: two for each side. The control register has own address. The data register and data direction register share a single address.

## a. Addressing the Control Register

In the previous section we load bit 2 with a 0 or a 1 to determine whether we're accessing DRA or DDRA. In this section we will see why DRA and DDRA both use the same address.

Figure...illustrates accessing the control register. Examing location $\$ 8005$ shows the contents of CRA, which can be change just by loading a different number into that location.

Some of the other bits in the control registers can be changed in the course of program execution. Thus we may find that locations $\$ 8005$ and $\$ 8007$ have had some of the contents altered since we loaded them with 00 . Typically, bit 2 will not be changed in this fashion. Now CRA is set so that we can get at DDRA through location $\$ 8004$

## b. Addressing The Data Direction Register

Once we've cleared CRA, we've assigned address $\$ 8004$ to DDRA. So that the content of $\$ 8004$ (the address of DDRA) determine which of the data lines will functions as which will function as output.
c. Addressing The Data Register

The data registers have to share address with the data direction registers. So far, by setting bit 2 of CRA to 0 , we've established that location $\$ 8004$ would access DDRA. But now, we are finished with DDRA and need to access DRA.

Thus, we go back to CRA and set bit 2 to 1 . Then the location $\$ 8004$ will address DRA.

### 3.8 PROGRAMMING WITH PIA

After we know how to address the registers of the PIA, we can begin writing programs that configure and use the PIA.

## a. Reading and Writing in the PIA

The cause the CPU to read the content of a location, we use LDA A or LDA B. To write into a location, we use STA A or STA B. Because the registers of the PIA are all represented by address, writing a program to read and write in them is easy

## Chapter FOUR

### 4.0 Discussing The Work Done

In the interfacing mechanism implemented in this project, I started by using four memories each one 1 KB .

First of all I construct the diagram shown on figure la (see appendix). This diagram illustrate the connections of the memories. After that I interfaced the memories with the MPU, then I selected the address busses (A0 to A9) connected to the memories, and by adjusting the address (A10 and A11) to the 2 to 4 decoder ( see Appendix I Fig. 1a) and leaving the address bus (A12, A13, A14, A15) unconnected. This has expand the memory size. 1st RAM is address from $(0000 \mathrm{H}-0377 \mathrm{H})$, the 2 nd RAM is address $(0400 \mathrm{H}-07 \mathrm{FFH})$, the 3rd RAM address $(0800 \mathrm{H}-0 \mathrm{BFFH})$, and the last one address ( $0 \mathrm{C} 00-0 \mathrm{FFF}$ ) (see Appendix I, Table 1a). Thus each RAM has 1 KB , and the total size for the four Ram's are 4 KB .

However, we change the MPU connection to (A11 and A12) and leaving (A10, A13, A14, A15) disconnected (see Appendix I, Fig. 1b), by doing we expanded the memory size. The 1st RAM now is contain address from ( $0000 \mathrm{H}-07 \mathrm{FFH})$, the 2 nd RAM $(0800 \mathrm{H}-07 \mathrm{FFH})$, the 3 rd RAM $(1000 \mathrm{H}-17 \mathrm{FFH})$, and the last one ( $1800 \mathrm{H}-1 \mathrm{FFFH}$ ) (see Appendix 1b, Table 1b). This time we increased the
size of the RAM for each one 2 KB and we got the total size can mapped for the 4 KB RAM's are 8 KB ( see appendix ).

More ever, we repeated the some process and changing the decoder poles to the address (A12 and A13) leaving address( A10, A11, A14, A15) disconnected (see Appendix I, Fig 1c). This process has increased the memory size for each one. The 1st RAM now is contain address ( $0000 \mathrm{H}-0 \mathrm{FFFH}$ ), the 2nd Ram address ( $1000 \mathrm{H}-1 \mathrm{FFFH}$ ), the 3 rd RAM ( $2000 \mathrm{H}-2 \mathrm{FFFH}$ ), and the last RAM ( $3000 \mathrm{H}-3 \mathrm{FFF}$ ) (see Appendix I, Table 1c). And has expand the memory capacity to 4 KB for each RAM, and the total capacity can access the 4 RAM's are 16 KB .

We carry on completing the decoder poles to the address bus and we found that each time the memory size increases every time until it reached it's maximum size 16 KB for each one. for more detail about the result (see appendix I)

Moreover, I used a 2 KB (see Appedix I, Fig. \& Table 2a, 2b, 2c, 2d) memories, 4 kB (see Appendix I, Fig. \& Table 3a, 3b, 3c, )) memories and 16KB (see Appendix I, Fig. \& Table, 4a) memories. And repeating the process I used in the beginning, this process has successful expand our memory capacity. The result of this project steps are shown in (appendix I).

By implementing this process practically in the lab, we found that our results are consistent to the theoretical figures. The practical connection of the MPU, 2K X 8 RAM as shown in (see Appendix I, Fig. 5a). And illustrated that our work was successfully accomplished.

## Conclusion

The last decays of 20th century the demand of storage system has increased, hence a demand for information storage system has consequently grown. The MPU system has been developed. In this project we interface the MPU to RAM/ROM to increase the size of memory, and this was done successfully by using the decoder mechanism. We interface all size of memory units to the MPU and by changing the connection of the MPU to the decoder we managed to increase the size of the memory successfully.

## APPENDIX I



INTERFACING WITH 1K X 8 RAM
Fig. 1 a

| ROM \# | A15 | Al4 | Al3 | A12 | Al1 | Al0 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | Al | A0 | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000 H |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 03 FFH |
| 2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0400 H |
|  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 07FF H |
| 3 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0800 H |
|  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | OBFF H |
| 4 | 0 | 0 | $0 \cdot$ | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 COO H |
|  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFFF H |

Table 1a

Note : Eeach RAM contain 1 K , and the total area is 4 KB


INTERFACING WITH 1K X 8 RAM
Fig. 1b

| ROM \# | A15 | A14 | A13 | Al2 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 |  | A2 | Al |  | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 1 \end{aligned}$ |  | $\begin{aligned} & 0000 \mathrm{H} \\ & 03 \mathrm{FFH} \end{aligned}$ |
|  | $\begin{aligned} & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & \hline \end{aligned}$ | $\begin{array}{r} 0 \\ 1 \\ \hline \end{array}$ | $\begin{aligned} & 0 \\ & 1 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & \hline \end{aligned}$ | $\begin{array}{r} 0 \\ 1 \\ \hline \end{array}$ | $\begin{aligned} & 0 \\ & 1 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 0 \\ & 1 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 0400 \mathrm{H} \\ & \mathbf{0 7 F F H} \\ & \hline \end{aligned}$ |
| 2 | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $0$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | 0800 H OBFF H |
|  | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ |  | 0 1 | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | 0 | 0 1 | 0 1 | 0 1 | 0 1 | 0 |  | 0CFFH OFFF H |
| 3 | 0 0 |  |  |  |  |  | 0 1 | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | $\begin{aligned} & 1000 \mathrm{H} \\ & 13 \mathrm{FFH} \end{aligned}$ |
|  | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | 0 1 | 0 |  | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | 0 |  | $\begin{aligned} & 1400 \mathrm{H} \\ & 17 \mathrm{FFH} \end{aligned}$ |
| 4 | 0 0 | 0 0 | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | 0 1 | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | $\begin{aligned} & 1800 \mathrm{H} \\ & \text { 1BFFH } \end{aligned}$ |
|  | ${ }^{0}$ | 0 0 | 0 0 | 1 1 | 1 | 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 | 0 1 |  | $1 \mathrm{C00H}$ <br> 1FFFH |

Table 1b
NOTE : Eeach RAM contain 2 K , and the total area is 8 KB


FIg. 1c
INTERFACING WITH 1K X 8 RAM


Table 1c
NOTE : Eeach RAM contain 4 K , and the total area is 16 KB


Flg. 1d
INTERFACING WITH 1K X 8 RAM


Table 1d
NOTE : Eeach RAM contain 8 K , and the total area is 32 KB
Contin...........

| ROM \# | A15 | A14 | Al3 | A12 | All | A10 | A9 | A8 | A7 | A6 | A5 | A4 |  | A3 | A2 A1 | Al |  | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 3 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 |  | 0 | 4000 H |
|  | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 43FFH |
|  | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 |  | 4400 H |
|  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 47FFH |
|  | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 |  | 4800H |
|  | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4BFFH |
|  | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ) | 0 | 0 | 0 |  | $4 \mathrm{C00H}$ |
|  | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 4FFFH |
|  | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 5000H |
|  | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 53 FFH |
|  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 5400 H |
|  | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 57FFH |
|  | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 |  |  |  | 5800H |
|  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 |  | 5BFFH |
|  | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | $5 \mathrm{C00H}$ |
|  | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 |  | 5FFFH |
| 4 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 |  | 6000 H |
|  | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 |  | 1 |  | 63 FFH |
|  | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  | 0 |  |  | 0 | 0 |  | 6800 H |
|  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  | 1 | 1 | 1 | 67 FFH |
|  | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 |  | $6800 \mathrm{H}$ |
|  | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 6BFFH |
|  | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  | ${ }^{6 \mathrm{COOH}}$ |
|  | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 6FFFH |
|  | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 |  | 7000 H |
|  | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 73FFH |
|  | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  | 7400 H |
|  | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 77FFH |
|  | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  | 7800H |
|  | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 78FFH |
|  | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $7 \mathrm{C00H}$ |
|  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7FFFH |



Flg. 1e
INTERFACING WITH 1K X 8 RAM

| ROM \# | A15 | A14 | A13 | A12 | Al1 | A10 | A9 | A8 | A7 | A6 | A5 | 5 A |  | A3 | A2 | Al | A0 | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  | 0 | 0 | 0 | 0 | 0000 H |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 03FFH |
|  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0400 H |
|  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 07FFH |
|  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  |  | 0 | 0 | 0 | 0 |  | 0800 H |
|  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  |  | 1 | 1 | 1 | 1 | 1 | 0BFFH |
|  | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 |  | $0 \mathrm{C00H}$ |
|  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 0FFFH |
|  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  | 0 | 0 | 0 |  | 1000 H |
|  | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 |  | 13FFH |
|  | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 |  | 1400 H |
|  | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 17FFH |
|  | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |  |  | 1800H |
|  | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 |  |  | 18FFH |
|  | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 |  | $1 \mathrm{C00H}$ |
|  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 1FFFH |
|  | 0 | 0 | 1 |  | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 |  | 2000H |
|  | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 |  | 23 FFH |
|  | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 |  | 2400H |
|  | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 |  | 27FFH |
|  |  | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 |  | 2800 H |
|  | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 |  | 2BFFH |
|  | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 |  |  |  | $2 \mathrm{C00H}$ |
|  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 2FFFH |
|  | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 |  | 3000 H |
|  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 33 FFH |
|  | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 |  |  |  | 3400 H |
|  | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 37FFH |
|  | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 |  | 0 | 0 | 3800H |
|  | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 3BFFH |
|  | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |  |  |  | 0 | 0 | 0 | 0 |  | $3 \mathrm{CO0H}$ |
|  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  | 1 | 1 |  |  | 3FFFH |

Table 1e
NOTE : Ecach RAM contain 16 K , and the total area is 64 KB
Continu.........

| ROM \# | Al5 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |  | A6 | AS | A4 |  | A3 | A2 | A1 | A0 | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 4000 H |
|  | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 43FFH |
|  | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 4400 H |
|  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 47FFH |
|  | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |  | 0 |  |  |  | 4800H |
|  | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |  |  | 1 | 1 | 1 | 1 | 4BFFH |
|  | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $4 \mathrm{C00H}$ |
|  | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 4FFFH |
|  | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  | 0 | 0 |  |  | 5000 H |
|  | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 53FFH |
|  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 |  |  | 5400 H |
|  | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 57FFH |
|  | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 5800 H |
|  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 5BFFH |
|  | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $5 \mathrm{C00H}$ |
|  | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 5FFFH |
|  | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 6000 H |
|  | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 63 FFH |
|  | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 |  |  |  | 6400 H |
|  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 67 FFH |
|  | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 6800H |
|  | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 6BFFH |
|  | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | $6 \mathrm{C00H}$ |
|  | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 6FFFH |
|  | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  | 7000 H |
|  | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 73 FFH |
|  | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7400 H |
|  | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 77 FFH |
|  | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 |  | 7800 H |
|  | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7BFFH |
|  | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $7 \mathrm{C00H}$ |
|  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7FFFH |





INTERFACING WITH 2K X 8 RAM
FIg. 2a

| ROM \# | A15 | Al4 | A13 | A12 | Al1 | A10 | A9 | A8 | A7 | A6 | A5 |  | A3 | A2 | Al |  | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000 H |
|  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 07FF H |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0800 H |
|  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | , | 1 | 1 | 0 fFF H |
| 3 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1000 H |
|  | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 17FF H |
| 4 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |  | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 1800 H |
|  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 FFF H |

## Table 2a

NOTE : Eeach RAM contain 2 K , and the total area is 8 KB


FIg. 2b
INTERFACING WITH 2K X 8 RAM

| ROM \# | A15 | Al4 | A13 | A12 | Al1 | A10 | A9 | A8 |  | A6 | A5 | A4 | A3 | A2 | Al | A0 | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $0$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | $\begin{aligned} & \mathbf{0 0 0 0 \mathrm { H }} \\ & \mathbf{0 7 F F H} \end{aligned}$ |
|  | 0 | 0 | 0 | 0 | 1 | 0 | 0 1 |  | 0 1 | 0 1 | 0 1 | 0 <br> 1 | 0 1 | 0 1 | 0 1 |  | $\begin{aligned} & 0800 \mathrm{H} \\ & \text { OfFFH } \\ & \hline \end{aligned}$ |
| 2 | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | $\begin{aligned} & 1000 \mathrm{H} \\ & \text { 17FF H } \end{aligned}$ |
|  | $\begin{gathered} 0 \\ 0 \end{gathered}$ | $\begin{aligned} & \mathbf{0} \\ & \mathbf{0} \end{aligned}$ | 0 | 1 1 | 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 1 |  | 0 1 | 0 1 | 0 |  | $\begin{gathered} \text { 1800H } \\ \text { 1FFFH } \end{gathered}$ |
| 3 | 0 |  |  |  |  |  | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  |  | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | $\begin{gathered} 2000 \mathrm{H} \\ 27 \mathrm{FFH} \end{gathered}$ |
|  | $\begin{aligned} & \mathbf{0} \\ & 0 \end{aligned}$ | $\begin{aligned} & \mathbf{0} \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $0$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & \mathbf{0} \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | $\begin{aligned} & 2800 \mathrm{H} \\ & 2 \mathrm{fFFH} \end{aligned}$ |
| 4 | 0 0 |  | 1 | 1 |  | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | 0 1 | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ |  | $\begin{aligned} & 3000 \mathrm{H} \\ & \mathbf{3 7 F F H} \end{aligned}$ |
|  |  | 0 0 | 0 | 1 1 | 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 | 0 1 | 0 | 0 1 | 0 1 |  | $\begin{gathered} 3800 \mathrm{H} \\ 3 \mathrm{FFFH} \end{gathered}$ |

Table 2 b
NOTE : Eeach RAM contain 4 K , and the total area is 16 KB


INTERFACING WITH 2K X 8 RAM
FIg. 2c


Table 2c
NOTE : Eeach RAM contain 8 K , and the total area is 32 KB


INTERFACING WITH 2K X 8 RAM
FIg. 2d


Table 2d
NOTE : Eeach RAM contain 4 KX 8 , and the total area is 64 KB
Conti..........



Flg. 3a
INTERFACING WITH 4K X 8 RAM

| ROM \# | A15 | Al4 | Al3 | Al2 | Al1 | A10 | A) | A8 | A7 | A6 | A5 |  |  | A2 | A1 |  | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000 H |
|  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFFF H |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1000 H |
|  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FFFH |
| 3 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2000 H |
|  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1. | 1 | 1 | 1 | 1 | 1 | 1 | 2FFF H |
| 4 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3000 H |
|  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | , | 1 | 1 | 1 | 1 | 1 | 1 | 3FFF H |

Table 3 a
NOTE : Eeach RAM contain 4 KX 8 , and the total area is 16 KB


INTERFACING WITH 4K X 8 RAM
FIg. 3b


Table 3b

NOTE : Eeach RAM contain 8 K , and the total area is 32 KB


INTERFACING WITH 4K X 8 RAM
FIg. 3c


Table 3c
NOTE : Eeach RAM contain 16 K , and the total area is 64 KB


INTERFACING WITH 16K X 8 RAM

FIg. 4a

| ROM \# | A15 | Al4 | A13 | Al2 | Al1 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | Al | A0 | ADDRESS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | $1)$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000 H |
|  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3FFF H |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4000 H |
|  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7FFF H |
| . 3 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8000 H |
|  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | BFFF H |
| 4 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\mathrm{C000} \mathrm{H}$ |
|  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFFF H |

Table 4a
NOTE : Eeach RAM contain 16 K , and the total area is 64 KB

## Practical Conection




Fig. 5b



## APPENDIX II

## General Description

These OR gates utilize advanced silicon-gate CMOS technology to achleve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high nolse immunity and the ability to drive 10 LS.TTL. loads. The $54 \mathrm{HC} / 74 \mathrm{HC}$ logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic \{amily. All inpuls are protected from damage due to static discharge by internal diode clamps to VCC and ground.

## Connection and Logic Diagrams

## Dual-In-LIne Package



TL/F/5132-1
Top VIew
Order Number MM54HC32' or MM74HC32
-Please look into Section 8, Appendix D for availability of various package types


Absolute Maximum Ratings (Notes 18 2) If Milliary/Aerospace specifled devlces are required, contact the Natlonal Semiconductor Sales Office/ Distributors for avallablity and specifications.
Supply Voltage (VCC)
-0.5 to +7.0 V
DC Input Voltage ( $\mathrm{V}_{\mathrm{N}}$ )
-1.5 to $V_{C C}+1.5 \mathrm{~V}$
DC Oulput Voltage (VOUT)
-0.5 to $V_{C C}+0.5 \mathrm{~V}$
$\pm 20 \mathrm{~mA}$
$\pm 25 \mathrm{~mA}$
$\pm 50 \mathrm{~mA}$
DC V $C C$ or GND Current, per pin (ICC)
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Power Dissipation (PD)
(Note 3)
600 mW
S.O. Package only 500 mW

Lead Temperature ( $T_{L}$ )
(Soldering 10 seconds)

## Operating Conditions

|  | Min | Max | Units |
| :--- | :---: | :---: | :---: |
| Supply Voltage $\left(V_{C C}\right)$ | 2 | 6 | $V$ |
| DC Input or Output Vollage | 0 | $V_{C C}$ | $V$ |
| (VIN VOUT) |  |  |  |
| Operating Temp. Range $\left(T_{A}\right)$ |  |  |  |
| MM74HC | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |
| MM54HC | -55 | +125 | ${ }^{\circ} \mathrm{C}$ |
| Input Rise or Fall Times |  |  |  |
| $\left(t_{r}, T_{1}\right) \quad V_{C C}=2.0 \mathrm{~V}$ |  | 1000 | ns |
| $V_{C C}=4.5 \mathrm{~V}$ |  | 500 | ns |
| $V_{C C}=6.0 \mathrm{~V}$ |  | 400 | ns |

DC Electrical Characteristics (Note 4)

| Syimbol | Parameter | Conditions | $V_{C C}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 74 \mathrm{HC} \\ T_{A}=-401085^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 54 \mathrm{HC} \\ T_{A}=-55 \text { to } 125^{\circ} \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typ | Guaranteed Limits |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High Level Input Voltage |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| VIL | Maximum Low Level Input Voltage" ${ }^{\circ}$ |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \\ & \hline \end{aligned}$ |  | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \\ \hline \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \\ \hline \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \\ \hline \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| V OH | Minimum High Level Output Voltage | $\begin{aligned} & V_{I N}=V_{I H} \text { or } V_{I L} \\ & \left\|I_{\text {OUT }}\right\| \leq 20 \mu A \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & V_{I N}=V_{I H} \text { or } V_{I L} \\ & \left\|l_{\text {out }}\right\| \leq 4.0 \mathrm{~mA} \\ & \left\|\left.\right\|_{\text {out }}\right\| \leq 5.2 \mathrm{~mA} \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.7 \\ & 5.2 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.98 \\ & 5.48 \\ & \hline \end{aligned}$ | $\begin{array}{r} 3.84 \\ 5.34 \\ \hline \end{array}$ | $\begin{aligned} & 3.7 \\ & 5.2 \\ & \hline \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| $\mathrm{V}_{\text {OL }}$ | Maximum Low Level Output Voltage | $\begin{aligned} & V_{\text {IN }}=V_{\text {IL }} \\ & \left\|I_{\text {OUT }}\right\| \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & V_{I N}=V_{I L} \\ & \left\|l_{\text {OUT }}\right\| \leq 4.0 \mathrm{~mA} \\ & \left\|\left.\right\|_{\text {OUT }}\right\| \leq 5.2 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 0.2 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.26 \\ & 0.26 \end{aligned}$ | $\begin{aligned} & 0.33 \\ & 0.33 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| $\mathrm{I}_{1 \times}$ | Maximum Input Current | $V_{I N}=V_{C C}$ or GND | 6.0 V |  | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| ${ }^{\text {ICC }}$ | Maximum Quiescent <br> Supply Current | $\begin{aligned} & V_{I N}=V_{C C} \text { or } G N D \\ & I_{\text {OUT }}=0 \mu \mathrm{~A} \end{aligned}$ | 6.0 V |  | 2.0 | 20 | 40 | $\mu \mathrm{A}$ |

Noto 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur
Note 2: Unless otherwise specified all voltages are ecterenced lo ground.
Hole 3: Pewer Dissipation temperalure derating - plastic "N"package: - $12 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ from $65^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$. ceramic "J" package - $12 \mathrm{mv} / \mathrm{F} /{ }^{\circ} \mathrm{C}$ from $100^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$
Note 4: for a power supply of $5 \mathrm{~V} \pm 10 \%$ the wers case output voltages ( V OH . and $\mathrm{V}_{\mathrm{OL}}$ ) occur lor HC at 4.5 V . Thus the 4.5 V viriues should be used when designing with this supply. Worsi case $V_{1 H}$ and $V_{1 L}$ decur al $V_{C C}=5.5 \mathrm{~V}$ and 45 V respectivoly (The $V_{1 \mathrm{H}} \mathrm{Valuo}$ al 55 V is 385 V .) The worsi case loakage current (IAN. 'Oc. and $\mathrm{I}_{\mathrm{Oz}}$ ) occur lor CMOS at the higher voltage and so the 6.0 V values should be used
" $V_{\text {IL }}$ limits are currently tested at $20 \%$ of $V_{C C}$. The above $V_{I L}$ spocification ( $30 \%$ of $V_{C C}$ ) will be implemented no later than O 1 . CY' 69 .

AC Electrical Characteristics $\mathrm{V}_{\mathrm{a}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} . \mathrm{I}_{\mathrm{f}}=\mathrm{t}_{\mathrm{I}}=6 \mathrm{~ns}$

| Symbol | Parameter | Conditions | Typ | Guaranteed <br> Limit | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IPHL, IpIH | Maximum Propagation <br> Delay |  | 10 | 18 | ns |

## AC Electrical Characteristics

| Symbol | Parameter | Conditions | Vcc | $T_{A}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 74 \mathrm{HC} \\ T_{A}=-40 \text { to } 85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 54 \mathrm{HC} \\ T_{A}=-55 \mathrm{to} 125^{\circ} \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typ | Guaranteed Limits |  |  |  |
| tphl. tple | Maximum Propagation Delay |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 30 \\ 12 \\ 9 \end{gathered}$ | $\begin{aligned} & 100 \\ & 20 \\ & 17 \end{aligned}$ | $\begin{aligned} & 125 \\ & 25 \\ & 21 \end{aligned}$ | $\begin{aligned} & 150 \\ & 30 \\ & 25 \end{aligned}$ | $\begin{aligned} & \text { ns } \\ & \text { ns } \\ & \text { ns } \end{aligned}$ |
| tteh, timl | Maximum Output Rise and Fall Time |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 30 \\ 8 \\ 7 \end{gathered}$ | $\begin{aligned} & 75 \\ & 15 \\ & 13 \end{aligned}$ | $\begin{aligned} & 95 \\ & 19 \\ & 16 \end{aligned}$ | $\begin{aligned} & 110 \\ & 22 \\ & 19 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| $\mathrm{C}_{P D}$ | Power Dissipation <br> Capacitance (Note 5) | (per gate) |  | 50 |  |  |  | pF |
| $\mathrm{ClN}_{\text {IN }}$ | Maximum Input Capacitance |  |  | 5 | 10 | 10 | 10 | pF |

Note 5: $C_{P D}$ determines the no load dynamic power consumption $P_{D}=C_{P D} V_{C O}{ }^{2}+I_{C C} \vee V_{C C}$. and the no load dynamic current consumption, $I_{S}=C_{P D} V_{C C} 1+l_{C C}$.

## General Description

These inverters utilize advanced silicon-gate CMOS lechnology to achieve operating speeds similar to LS-TTL gates with the low power consumption of siandard CMOS integrated circuits.
The MM54HC04/MM74HCO4 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The $54 \mathrm{HC} / 74 \mathrm{HC}$ logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{\mathrm{CC}}$ and ground.

## Features

- Typical propagation delay: 8 ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: $10 \mu \mathrm{~W}$ maximum at room temperature
- Low input current: $1 \mu \mathrm{~A}$ maximum

Connection and Logic Diagrams

## Dual-In-LIne Package



Order Number MM54 ${ }^{\circ} \mathrm{HC04}$ * or MM74HC04*

- Please look into Section B, Appendix $D$ lor availability ol various package lypes.

1 of 6 Inverters

A


Absolute Maximum Ratings (Notes 1\&2)
If Military/Aerospace specified devices are required, contact the National Semlconductor Sales Office/ Distributors for avaliablity and specifications.
Supply Voltage (VCC)
$-0.510+7.0 \mathrm{~V}$
DC Input Voltage ( $V_{I N}$ )
-1.5 to $V_{C C}+1.5 \mathrm{~V}$
DC Output Voltage ( $V_{\text {OUT }}$ )
Clamp Diode Current ( $1_{\mathrm{ik}}$. Iok)
-0.5 to $V_{C C}+0.5 \mathrm{~V}$
$\pm 20 \mathrm{~mA}$
$\pm 25 \mathrm{~mA}$
$\pm 50 \mathrm{~mA}$
DC $V_{C C}$ or GND Current, per pin (ICC)
Storage Temperalure Range (TSTG)
$-65^{\circ} \mathrm{C} 10+150^{\circ} \mathrm{C}$
Power Dissipation (PD)
(Note 3)
600 mW
S.O. Package only 500 mW

## Operating Conditions

|  | Min | Max | Units |
| :--- | :---: | :---: | :---: |
| Supply Voltage $\left(V_{C C}\right)$ | 2 | 6 | $V$ |
| DC input or Output Voltage | 0 | $V_{C C}$ | $V$ | (VIN. VOUT)

Operating Temp Range ( $T_{A}$ ) MM74HC $-40+85$ ${ }^{\circ} \mathrm{C}$ MM54HC $-55+125{ }^{\circ} \mathrm{C}$ Input Rise or Fall Times
$\left(t_{r}, t_{1}\right) \quad V_{C C}=2.0 \mathrm{~V} 1000 \quad \mathrm{~ns}$

| $V_{C C}=4.5 \mathrm{~V}$ | 500 | ns |
| :--- | :--- | :--- |
| $V_{C C}=6.0 \mathrm{~V}$ | 400 | $n s$ |

Lead Temperature ( $T_{L}$ )
(Soldering 10 seconds)

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{C C}$ | $T_{A}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 74 \mathrm{HC} \\ \mathrm{~T}_{\mathrm{A}}=-40 \text { to } 85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 54 \mathrm{HC} \\ T_{A}=-55 t 0125^{\circ} \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typ | Guaranteed Limits |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High Level input Voltage |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \\ \hline \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \\ \hline \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| $V_{\text {II }}$ | Maximum Low Level Inpul Voltage"* |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | Minimum High Level Output Vollage | $\begin{aligned} & V_{\text {IN }}=V_{\text {IL }} \\ & \mid \text { iouT } \mid \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & V_{I N}=V_{I L} \\ & \mid \text { lout } \mid \leq 4.0 \mathrm{~mA} \\ & \text { \|lout } \mid \leq 5.2 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 4.2 \\ & 5.7 \end{aligned}$ | $\begin{aligned} & 3.98 \\ & 5.48 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.84 \\ & 5.34 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.7 \\ & 5.2 \\ & \hline \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| $V_{\text {OL }}$ | Maximum Low Levei Output Voltage | $\begin{aligned} & V_{I N}=V_{I H} \\ & \left\|l_{\text {OuT }}\right\| \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & V_{1 N}=V_{1 H} \\ & \\|_{\text {OUT }} \mid \leq 4.0 \mathrm{~mA} \\ & \left.\right\|_{\text {OUT }} \mid \leq 5.2 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 0.2 \\ & \hline \end{aligned}$ | $\begin{array}{r} 0.26 \\ 0.26 \\ \hline \end{array}$ | $\begin{aligned} & 0.33 \\ & 0.33 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| 1 N | Maximum Input Current | $V_{\text {IN }}=V_{\text {CC }}$ or $G N D$ | 6.0 V |  | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| ${ }^{\text {cce }}$ | Maximum Quiescent Supply Current | $\begin{aligned} & V_{I N}=V_{C C} \text { or GND } \\ & \text { IOUT }=0 \mu \mathrm{~A} \end{aligned}$ | 6.0 V |  | 2.0 | 20 | 40 | $\mu \mathrm{A}$ |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2: Unless othenwise specilied all vollages are relerenced to ground.
Nole 3: Power Dissipation temperalure deraning - plastic " N " package: - $12 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ : $\mathrm{Hom} 65^{\circ} \mathrm{C} 1085^{\circ} \mathrm{C}$, ceramic "J" package $12 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ Irom $100^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$.
Note 4: For a power supply of $5 \mathrm{~V} \pm 10 \%$ the worst case oulput voltages ( $\mathrm{V}_{\mathrm{OH}}$, and $\mathrm{V}_{\mathrm{C}}$ ) occur for HC al 4.5 V . Thus the 4.5 V valtes should be used when designing with this supply. Worst case $V_{1 H}$ and $V_{I L}$ occur al $V_{C C}=5.5 \mathrm{~V}$ and 4.5 V respeclively. (The $V_{I H}$ value at 5.5 V is 3.85 V .) The wors; case leakage current (IIN. ICC. and IO2l occur for CMOS at the higher voltage and so the 6.0 V values should be used.
" $V_{\text {If }}$ limits are currently lested at $20 \%$ of $V_{C C}$. Tho above $V_{11}$ specification ( $30 \%$ of $V_{C C}$ ) will be implomonted no tater than 0 . CY'g9.

Absolute Maximum Ratings (Notes 1 \& 2)
If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Vollage (VCC)
DC input Vollage ( $\mathrm{V}_{\mathrm{iN}}$ )
DC Output Vollage (VOUT)
Clamp Diode Current (lık, lok)
DC Output Current, per pin (lout)
DC $\mathrm{V}_{\mathrm{CC}}$ or GND Current, per pin ( ICC )
$-0.510+7.0 \mathrm{~V}$

Storage Temperature Range ( $\mathrm{T}_{\mathrm{STG}}$ )
$-1.510 V_{C C}+1.5 \mathrm{~V}$
$-0.510 \mathrm{~V}_{\mathrm{CC}}+0.5 \mathrm{~V}$ $\pm 20 \mathrm{~mA}$ $\pm 25 \mathrm{~mA}$ $\pm 50 \mathrm{~mA}$ Power Dissipation ( $P_{D}$ )
$\begin{array}{ll}\text { (Note 3) } & 600 \mathrm{~mW} \\ \text { S.O. Package only } & 500 \mathrm{~mW}\end{array}$
(Soldering 10 seconds)
$260^{\circ} \mathrm{C}$

Operating Conditions

|  | Min | Max | Units |
| :--- | :---: | :---: | :---: |
| Supply Voltage $\left(V_{C C}\right)$ | 2 | 6 | $V$ |
| DC Input or Output Vollage | 0 | $V_{C C}$ | $V$ |
| $\left(V_{\mathbb{N}}, V_{\text {OUI }}\right)$ |  |  |  |
| Operating Temp. Range $\left(T_{A}\right)$ |  |  |  |
| MM74HC | -40 | 85 | ${ }^{\circ} \mathrm{C}$ |
| MM54HC | -55 | +125 | ${ }^{\circ} \mathrm{C}$ |
| Input Rise or Fall Times |  |  |  |
| $\left(I_{r}, t_{1}\right) \quad V_{C C}=2.0 \mathrm{~V}$ |  | 1000 | ns |
| $V_{C C}=4.5 \mathrm{~V}$ |  | 500 | ns |
| $V_{C C}=6.0 \mathrm{~V}$ |  | 400 | ns |

DC Electrical Characteristics (Note4)

| Symbol | Parameter | Conditions | VCC | $T_{A}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 74 \mathrm{HC} \\ \mathrm{~T}_{\mathrm{A}}=-40 \mathrm{to} 85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 54 \mathrm{HC} \\ T_{A}=-55 \text { to } 125^{\circ} \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typ | Guaranteed Limits |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High Level Input Voltage |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| $V_{\text {IL }}$ | Maximum Low Level Input Voltage ${ }^{\text {. }}$ |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 1.35 \\ & 1.8 \end{aligned}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| $\mathrm{VOH}^{\text {O }}$ | Minimum High Level Output Voliage | $\begin{aligned} & V_{\text {IN }}=V_{\text {III }} \\ & \mid \text { lout\| } \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & V_{\text {IN }}=V_{I L} \\ & \left.\right\|_{\text {OUT }} \leq 4.0 \mathrm{~mA} \\ & \left\|l_{\text {OUT }}\right\| \leq 5.2 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 4.2 \\ & 5.7 \end{aligned}$ | $\begin{aligned} & 3.98 \\ & 5.48 \end{aligned}$ | $\begin{aligned} & 3.84 \\ & 5.34 \end{aligned}$ | $\begin{aligned} & 3.7 \\ & 5.2 \\ & \hline \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| $\mathrm{V}_{\text {OL }}$ | Maximum Low Level Output Voltage | $\begin{aligned} & V_{I N}=V_{I H} \\ & \left\|I_{\text {OUT }}\right\| \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & v_{1 N}=v_{1 H} \\ & \\|_{\text {OUT }} \leq 4.0 \mathrm{~mA} \\ & \left.\right\|_{\text {lout }} \mid \leq 5.2 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & 0.26 \\ & 0.26 \end{aligned}$ | $\begin{aligned} & 0.33 \\ & 0.33 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| In | Maximum Input Current | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {CC }}$ or GND | 6.0 V |  | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| ${ }^{\text {ICC }}$ | Maximum Quiescent Supply Current | $\begin{aligned} & V_{I N}=V_{C C} \text { or } G N D \\ & \text { louT }=0 \mu \mathrm{~A} \end{aligned}$ | 6.0 V |  | 2.0 | 20 | 40 | $\mu \mathrm{A}$ |

Note 1: Absotute Maximum Ratings are those values boyond which darnage to the device may occur.
Note 2: Unless otherwise specified all vollaỵcs are relerenced to ground.
Nole 3: Power Oissipation temperature deralng - plastic "N" package:- $12 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ liom $65^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$; ceramic " 5 " package $\quad 12 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ from $100^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$. Nole 4: For a power supply of $5 \mathrm{~V} \pm 10 \%$ the worst case oulput vollages ( V OH. and $\mathrm{V}_{\text {On }}$ ) occur for HC al 4.5 V . Thus the 4.5 V vat, , should be used when designing wilh this supply. Worsi case $V_{1 H}$ and $V_{1 L}$ occur at $V_{C C}=5.5 \mathrm{~V}$ and 4.5 V respeclively, (The $V_{I H}$ value at 5.5 V is 3.85 V ) The wors: case leakage current (liN. ICC. and (O2) occur for CMOS at the higher vollage and so the 6.0 V values should be used.

- $V_{\text {IL }}$ limits are currently tested al $20 \%$ of $\mathrm{V}_{\mathrm{CC}}$. The above $\mathrm{V}_{\text {IL }}$ specification ( $30 \%$ of $\mathrm{V}_{\mathrm{CC}}$ ) will bo implemented no later than O . CY'e9

AC Electrical Characteristics $\mathrm{V}_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{t}}=6 \mathrm{~ns}$

| Symbol | Parameter | Conditions | Typ | Guaranteed <br> LImit | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IPHL. tPLH | Maximum Propagation <br> Delay |  | 8 | 15 | ns |

AC Electrical Chatacteristics $V_{C C}=2.0 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{l}}=6 \mathrm{~ns}$ (unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{c c}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 74 \mathrm{HC} \\ T_{A}=-40 \text { to } 85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 54 \mathrm{HC} \\ T_{A}=-55 \text { to } 125^{\circ} \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typ | Guaranteed Limits |  |  |  |
| tphl, tple | Maximum Propagation Delay |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{gathered} 55 \\ 11 \\ 9 \\ \hline \end{gathered}$ | 95 <br> 19 <br> 16 | $\begin{aligned} & 120 \\ & 24 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{aligned} & 145 \\ & 29 \\ & 24 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| ttih. ${ }^{\text {TheL }}$ | Maximum Output Rise and Fall Time |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 30 \\ 8 \\ 7 \end{gathered}$ | $\begin{aligned} & 75 \\ & 15 \\ & 13 \end{aligned}$ | $\begin{aligned} & 95 \\ & 19 \\ & 16 \\ & \hline \end{aligned}$ | $\begin{gathered} 110 \\ 22 \\ 19 \end{gathered}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| $\mathrm{C}_{P D}$ | Power Dissipation Capacitance (Note 5) | (per gate) |  | 20 |  |  |  | pF |
| $\mathrm{C}_{\text {IN }}$ | Maximum Input Capacitance |  |  | 5 | 10 | 10 | 10 | pF |

Note 5: $C_{P O}$ determines the no load dynamic power consumption. $P_{O}=C_{P O} V_{C C} 1+I_{C C} V_{C C}$, and the no load dynamic current consumption, $I_{S}=C_{P D} V_{C C} 1+l_{C C}$

National Semiconductor MM54HC138/MM74HC138 3-to-8 Line Decoder

## General Description

This decoder utilizes advanced silicon-gate CMOS technology, and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL. logic.
The MM54HC138/MM74HC138 has 3 binary select inputs ( $\mathrm{A}, \mathrm{B}$, and C ). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, G2A and $\overline{\mathrm{G} 2 \mathrm{~B}}$ ) are provided to ease the cascading of decoders.

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to $V_{C C}$ and ground.

## Features

- Typical propagation delay: 20 ns
- Wide power supply range: $2 \mathrm{~V}-6 \mathrm{~V}$
- Low quiescent current: $80 \mu \mathrm{~A}$ maximum ( 74 HC Series)
- Low input current: $1 \mu \mathrm{~A}$ maximum
- Fanout of 10 LS-TTL loads


## Connection and Logic Diagrams



Order Number MM54HC138* or MM74HC138*
-Please look into Section 8 , Appendix D for availabilly of various package types.


## Truth Table

| Inputs |  |  |  |  | Outputs |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Enable |  | Select |  |  |  |  |  |  |  |  |  |  |
| G1 | 言2* | c | B | A | Yo | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | $\times$ | X | X | H | H | H | H | H | H | H | H |
| L | X | X | $\times$ | x | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L. | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | 1 | H | H | L | H | H | H | H | H | H | , | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

[^0]Absolute Maximum Ratings (Notes 1 \& 2)
If Milltary/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for avallability and specifications.

Supply Voltage (VCC)
DC Input Voltage ( $V_{I N}$ )
DC Output Voltage (VOUT)
Clamp Diode Current (IK, IOK)
DC Output Current, per pin (lout)
DC $V_{C C}$ or GND Current, per pin (ICC)
-0.5 to +7.0 V
-1.5 to $\mathrm{V}_{C C}+1.5 \mathrm{~V}$
-0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$
$\pm 20 \mathrm{~mA}$
$\pm 25 \mathrm{~mA}$
$\pm 50 \mathrm{~mA}$
Storage Temperature Range (TSTG)
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Power Dissipation ( $\mathrm{P}_{\mathrm{D}}$ )
(Note 3)
600 mW
S.O. Package only

500 mW
Lead Temp. ( $T_{L}$ ) (Soldering 10 seconds)

Operating Conditions

|  | Min | Max | Units |
| :---: | :---: | :---: | :---: |
| Supply Voliage ( $\mathrm{V}_{\mathrm{CC}}$ ) | 2 | 6 | V |
| DC Input or Output Voltage ( $V_{\text {IN }}, V_{\text {OUT }}$ ) | 0 | $V_{C C}$ | V |
| Operating Temp. Range ( $\mathrm{T}_{\mathrm{A}}$ ) |  |  |  |
| MM74HC | -40 | $+85$ | ${ }^{\circ} \mathrm{C}$ |
| MM54HC | --55 | $+125$ | ${ }^{\circ} \mathrm{C}$ |
| Input Rise or Fall Times |  |  |  |
| $(t, 1) \quad V_{C C}=2.0 \mathrm{~V}$ |  | 1000 | ns |
| $V_{\text {cc }}=4.5 \mathrm{~V}$ |  | 500 | ns |
| $V_{C C}=6.0 \mathrm{~V}$ |  | 400 | ns |

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{\text {cc }}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 74 \mathrm{HC} \\ T_{A}=-40 \text { to } 85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 54 \mathrm{HC} \\ T_{A}=-55 \text { to } 125^{\circ} \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typ | Guaranteed Limits |  |  |  |
| $V_{\text {IH }}$ | Minimum High Level Input Voltage |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| $V_{\text {IL }}$ | Maximum Low Level Input Voltage** |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \\ \hline \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | Minimum High Level Output Voltage | $\begin{aligned} & V_{I N}=V_{I H} \text { or } V_{I L} \\ & \left\|l_{\text {OUT }}\right\| \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & V_{I N}=V_{I H} \text { or } V_{I L} \\ & \left\|\left.\right\|_{\text {OUT }}\right\| \leq 4.0 \mathrm{~mA} \\ & \left\|\left.\right\|_{\text {OUT }}\right\| \leq 5.2 \mathrm{~mA} \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.2 \\ & 5.7 \end{aligned}$ | $\begin{aligned} & 3.98 \\ & 5.48 \end{aligned}$ | $\begin{aligned} & 3.84 \\ & 5.34 \end{aligned}$ | $\begin{aligned} & 3.7 \\ & 5.2 \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| VOL | Maximum Low Level Output Voltage | $\begin{aligned} & V_{\text {IN }}=V_{\text {IH }} \text { or } V_{\text {IL }} \\ & \left\|\left.\right\|_{\text {OUT }}\right\| \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
|  |  | $\begin{aligned} & V_{1 N}=V_{1 H} \text { or } V_{11} \\ & \|l o u t\| \leq 4.0 \mathrm{~mA} \\ & \mid \text { lout } \mid \leq 5.2 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 0.2 \\ & \hline \end{aligned}$ | $\begin{array}{r} 0.26 \\ 0.26 \\ \hline \end{array}$ | $\begin{aligned} & 0.33 \\ & 0.33 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| IN | Maximum Input Current | $\mathrm{V}_{1 N}=\mathrm{V}_{\mathrm{CC}}$ or GND | 6.0 V |  | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| ${ }^{\text {I C C }}$ | Maximum Quiescent Supply Current | $\begin{aligned} & V_{I N}=V_{C C} \text { or } G N D \\ & I_{\text {OUT }}=0 \mu \mathrm{~A} \end{aligned}$ | 6.0 V |  | 8.0 | 80 | 160 | $\mu \mathrm{A}$ |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2: Unless otherwise specified all voltages are relerenced to ground.
Note 3: Power Dissipation temperature derating - plastic " N " package: $-12 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ trom $65^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$; ceramic "J"package: - $12 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ from $100^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$. Note 4: For a power supply of $5 \mathrm{~V} \pm 10 \%$ the worst case output voltages ( $\mathrm{VOH}_{\mathrm{OH}}$, and $\mathrm{V}_{\mathrm{OL}}$ ) occur for HC al 4.5 V . Thus the 4.5 V values should be used when designing with this supply. Worst case $V_{I H}$ and $V_{I L}$ occur at $V_{C C}=5.5 \mathrm{~V}$ and 4.5 V respectively. (The $\mathrm{V}_{I H}$ value al 5.5 V is 3.85 V .) The worst case leakage current (IIN. ICC, and loz) occur for CMOS at the higher voltage and so the 6.0 V values should be used.
$\because V_{\text {IL }}$ limits are currently tested at $20 \%$ of $\mathrm{V}_{\mathrm{CC}}$. The above $\mathrm{V}_{\text {IL }}$ specification ( $30 \%$ of $\mathrm{V}_{\mathrm{CC}}$ ) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $\mathrm{V}_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{t}}=6 \mathrm{~ns}$

| Symbol | Parameter | Conditlons | Typ | Guaranteed <br> Limit | Units |
| :--- | :--- | :---: | :---: | :---: | :---: |
| tPLH | Maximum Propagation <br> Delay, Binary Select to any Output |  | 18 | 25 | ns |
| TPHL | Maximum Propagation <br> Delay, Binary Select to any Output |  | 28 | 35 | ns |
| TPHL. TPLH | Maximum Propagation <br> Delay, G1 to any Output |  | 18 | 25 | ns |
| TPHL | Maximum Propagation <br> Delay G2A or G2B to <br> Output |  | 23 | 30 | ns |
| TPLH | Maximum Propagation <br> Delay G2A or G2B to <br> Output | 18 | 25 | ns |  |

AC Electrical Characteristics $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{l}}=6 \mathrm{~ns}$ (unless otherwise speciifed)

| Symbol | Parameter | Conditions | $V_{c c}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 74 \mathrm{HC} \\ T_{A}=-40 \text { to } 85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 54 \mathrm{HC} \\ \mathrm{~T}_{\mathrm{A}}=-55 \text { to } 125^{\circ} \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typ | Guaranteed Limits |  |  |  |
| $t_{\text {PLH }}$ | Maximum Propagation Delay Binary Select to any Output Low to High |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 75 \\ & 15 \\ & 13 \end{aligned}$ | $\begin{aligned} & 150 \\ & 30 \\ & 26 \end{aligned}$ | $\begin{aligned} & 189 \\ & 38 \\ & 32 \end{aligned}$ | $\begin{gathered} 224 \\ 45 \\ 38 \end{gathered}$ | $\begin{aligned} & \text { ns } \\ & \text { ns } \\ & \text { ns } \end{aligned}$ |
| $\mathrm{t}_{\text {PHL }}$ | Maximum Propagation Delay Binary Select to any Output High to Low |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 100 \\ & 20 \\ & 17 \end{aligned}$ | $\begin{gathered} 200 \\ 40 \\ 34 \end{gathered}$ | $\begin{gathered} 252 \\ 50 \\ 43 \end{gathered}$ | $\begin{aligned} & 298 \\ & 60 \\ & 51 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| ${ }^{\text {PPHL. }}$ tple | Maximum Propagation Delay G1 to any Output |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 75 \\ & 15 \\ & 13 \end{aligned}$ | $\begin{aligned} & 150 \\ & 30 \\ & 26 \end{aligned}$ | $\begin{aligned} & 189 \\ & 38 \\ & 32 \end{aligned}$ | $\begin{gathered} 224 \\ 45 \\ 38 \end{gathered}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| ${ }^{\text {tPHL }}$ | Maximum Propagation Delay $\overline{\mathrm{G} 2 \mathrm{~A}}$ or $\overline{\mathrm{G} 2 \mathrm{~B}}$ to Output |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 82 \\ & 28 \\ & 22 \end{aligned}$ | $\begin{gathered} 175 \\ 35 \\ 30 \\ \hline \end{gathered}$ | $\begin{aligned} & 221 \\ & 44 \\ & 37 \end{aligned}$ | $\begin{gathered} 261 \\ 52 \\ 44 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| $\mathrm{t}_{\text {PLH }}$ | Maximum Propagation Delay G2A or G2B to Output |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 75 \\ & 15 \\ & 13 \end{aligned}$ | $\begin{aligned} & 150 \\ & 30 \\ & 26 \\ & \hline \end{aligned}$ | $\begin{gathered} 189 \\ 38 \\ 32 \end{gathered}$ | $\begin{gathered} 224 \\ 45 \\ 38 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \\ & \hline \end{aligned}$ |
|  | Output Rise and Fall Time |  | $\begin{aligned} & 2.0 \mathrm{~V} \\ & 4.5 \mathrm{~V} \\ & 6.0 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 30 \\ 8 \\ 7 \\ \hline \end{gathered}$ | $\begin{aligned} & 75 \\ & 15 \\ & 13 \\ & \hline \end{aligned}$ | $\begin{aligned} & 95 \\ & 19 \\ & 16 \\ & \hline \end{aligned}$ | $\begin{aligned} & 110 \\ & 22 \\ & 19 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| $\mathrm{CIN}_{\text {IN }}$ | Maximum Input Capacitance |  |  | 3 | 10 | 10 | 10 | pF |
| CPD | Power Dissipation Capacitance | (Note 5) |  | 75 |  |  |  | pF |

Note 5: $C_{P D}$ determines the no load dynamic power consumption, $P_{D}=C_{P D} V_{C C}{ }^{2}+I_{C C} V_{C C}$, and the no load dynamic current consumption, $I_{S}=C_{P D} V_{C C} 1+I_{C C}$.

## References

> Prinoples

1. Microprocessor Preatrienke \& Application Program
2. Microcomputer \& Microprocessors

[^0]:    - $\mathrm{G} 2=\mathrm{G} 2 \mathrm{~A}+\mathrm{G} 2 \mathrm{~B}$
    $H=$ high level, $L=$ fow level, $X=$ don't care

