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EFFICIENCY ANALYSIS OF THE DIGITAL MODULATION TECHNIQUES & DESIGN OF THE NON-COHERENT PSK SYSTEM

A Master Thesis

Prepared by

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CHAPTERS Design of the Non-Coherent DPSK System

LIST OF ABBREVIATIONS & SYMBOLS

Abbreviations & SY!!!bols	Full Name
APK	Amplitude Phase Keying
ASK	Amplitude Shift Keying
AWGN	Additive White Gaussian Noise
b(t)	Baseband signal
B,BW	Bandwidth
BER	Bit Error Rate
BFSK	Binary Frequency Shift Keying
BPSK	Binary Phase Shift Keying
C	Channel capacity
c(t)	Carrier signal
d(t)	The data stream to be transmitted
DPSK	Digital Phase Shift Keying
Eb	Energy per bit
FSK	Frequency Shift Keying
h(t)	Actual impulse response (band-pass filter)
$\bar{h}(t)$	Complex impulse response
M	Operating points for different numbers of phase levels
MSK,MPSK	M-ary Phase Shift Keying
No	The sample voltage due to noise
NRZ	Non-Return Zero
Pc	The probability of correct reception
PE	The probability of symbol error
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
~	Bit rate
Re	Real number
Ref	Reference number
s(t)	Modulated signal
Tb	Bit duration

ABSTRACT

When it is required to transmit data over a band-pass channel, it is necessary to modulate the incoming data on to a carrier wave (usually sinusoidal) with fixed frequency limits imposed by the channel. The data may represent digital computer outputs or PCM waves generated by digitazing voice or video signals. The channel may be a telephone channel, microwave radio link, satellite channel or an optical fiber. In any event, the modulation process involves switching or keying the amplitude, frequency or phase of the carrier in accordance with the incoming data. Thus there are three basic modulation techniques for the transmission of digital data ; they are known as amplitude-shift keying (ASK) frequency-shift keying (FSK) and phase-shift keying (PSK).

This thesis is devoted to an analysis of PSK modulation techniques, its noise performance, spectral properties, merit and limit array, applications and other related topics.

We will see that each method offers *system trade-offs* of its own. The final choice will be way in which the available primary communication resources, *transmitted power* and *channel bandwidth,* are best exploited. In particular, the choice will made in favor of the scheme that attains as many of the following design goals as possible:

1. Maximum data rate.
2. Minimum probability of symbol error.
3. Minimum transmitted power.
4. Minimum channel bandwidth.
5. Maximum resistance to interfering signals.
6. Minimum circuit complexity.

Some of these goals pose conflicting requirements; for example, goals (1) and (2) are in conflict with goals (3) and (4). The best we can therefore do is to satisfy as many of these goals as possible.

The project consists of introduction, five chapters and conclusion.

In the first chapter we provide an overview and analysis of the ASK, FSK and PSK modulation techniques for transmission the digital information. Then we describe coherent and non-coherent reception of BPSK signals. For representation of the BPSK signal is used geometrical approach.

Chapter 2 studies M-ary PSK techniques. We begin with the design of QPSK modulation techniques. In this chapter we consider of the multilevel PSK modulation techniques their merit and limit array. The last section of chapter is developed to the design of the M-ary PSK transmission system.

Chapter 3 provides an error probability analysis of the PSK systems.

Chapter 4 is developed to the performance analysis of the digital modulation techniques. For this purpose different types of digital modulation techniques are analyzed in terms of power. Transmission, bandwidth efficiency, transmission rate and noise immunity.

Chapter 5 is devoted to the design of the non-coherent DPSK system. We show that non-coherent detection PSK signal can be realized by a simple method based on the variation of the output of the filter when the input signal phase is switched. The final section of this chapter presents the laboratory realization of the modulator and demodulator using integrated circuits.

CHAPTER 1 Basic of the Digital Modulation Techniques

1.1 BINARY MODULATION TECHNIQUES

Modulation is defined as *the process by which some characteristic of a carrier is varied in accordance with a modulating wave.* In digital communications, the modulating wave consists of *binary* data or an M-ary encoded version of it. For the carrier, it is customary to use a sinusoidal wave. With a sinusoidal carrier, the feature that is used by the modulator to distinguish one signal from another is a step change in the amplitude, frequency, or phase of the carrier. The result of this modulation process is *amplitude- shift keying* (ASK) , *frequency-shift keying (FSK)* or *phase-shift keying* (PSK) , respectively, as illustrated in Fig. 1.1 for the special case of a source of binary data.

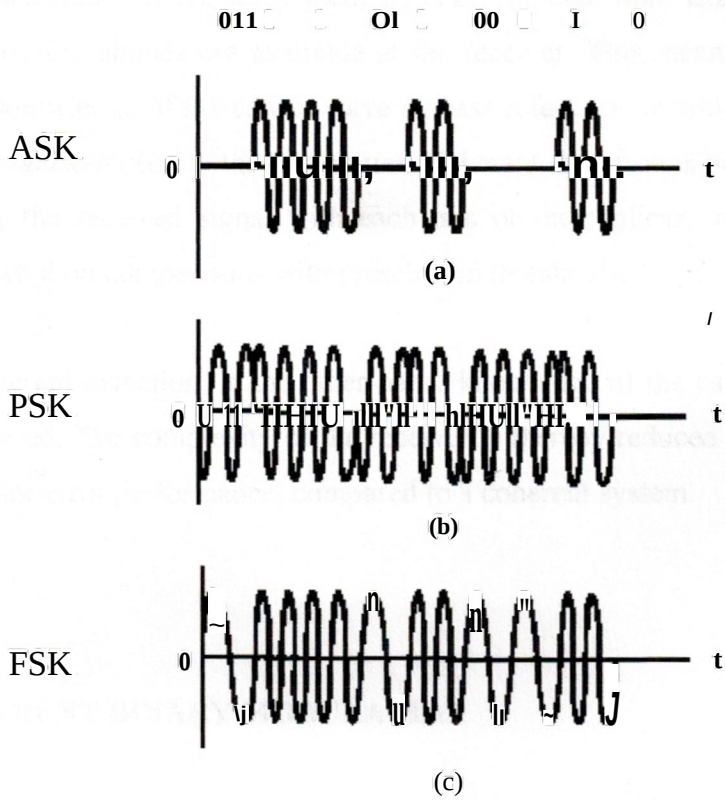


Figure 1.1 Wave forms for (a) amplitude-shift keying, (b) phase-shift keying, and (c) frequency-shift keying. [Ref 6, page 274]

Ideally, PSK and FSK signals have a constant envelope, as shown in Fig 1.1. This feature makes them impervious to amplitude non-linearities, as encountered in microwave radio links and satellite channels.

Accordingly, we find that, in practice, PSK and FSK signals are much more widely used than ASK signals. In the more general case of M-ary signalling, the modulator produces one of an available set of $M = 2^m$ distinct signals in response to *m* bits of source data at a time. Clearly, binary modulation is a special case of M-ary modulation with M = 2. In the waveforms shown in Fig. 1.1 , a single feature of the carrier (i.e., amplitude, phase, or frequency) undergoes modulation. Sometimes, a *hybrid* form of modulation is used. For example, changes in both amplitude and phase of the carrier are combined to produce *amplitude-phase keying* (APK). The use of hybrid techniques opens up yet another format for digital modulation.

To perform demodulation at the receiver, we have the choice of *coherent* or *non-coherent detection.* In the ideal form of coherent detection, exact replicas of the possible arriving signals are available at the receiver. This means that the receiver has exact knowledge of the carrier wave's phase reference, in which case we say the receiver is *phase-locked* to the transmitter. Coherent detection is performed by cross-correlating the received signal with each one of the replicas, and then making a decision based on comparisons with preselected thresholds.

In non-coherent detection, in the other hand, knowledge of the carrier wave's phase is not required. The complexity of the receiver is thereby reduced but at the expense of an inferior error performance, compared to a coherent system.

1.2 COHERENT BINARY MODULATION

As mentioned previously, binary modulation has three basic forms: amplitude-shift keying (ASK), phase-shift keying (PSK), and frequency-shift keying (FSK).In this

section, we present the noise analysis for the coherent detection of ASK, FSK and PSK signals, assuming an *Additive White Gaussian Noise (AWGN) model.*

1.2.1 COHERENT BINARY PSK

In binary phase-shift keying (BPSK) the transmitted signal is a sinusoid of fixed amplitude. It has one fixed phase when the data is at the other level the *phase* is different by 180°. If the sinusoid is of amplitude A, it has a power Ps= 1/2 A_2 so that $A = .JiP.$ Thus the transmitted signal is either

$$S_1(t) = \sim\overline{2\,Ps}\ \cos(\{i)_o f)$$

$$S_2(t) = jiP;\ \cos(\{i)_o/+7r) \quad (1.1)$$

$$=-\sim\overline{2P_5}\ \cos(\{i)_{o/)} \quad (1.2)$$

where $r0_0$ is a corner frequency of the carrier $r0_o$= 21tfo. In BPSK the data b(t) is a stream of binary digits with voltage levels which, as a matter of convenience, we take to be at+ 1 V and -1V. When b(t) = 1 V we say it is at logic level 1 and when b(t) = -1 V we say it is at logic level 0. Hence V8rsK(t) can be written, with no loss of generality, as

$$S(t) = b(t)/iP:\ \cos\{i)_o t \quad (1.3)$$

1.2.2 TRANSMITTER OF BPSK SYSTEM

In practice, BPSK signal is generated by applying the waveform cos $r0_o t$, as a carrier, to a balanced modulator and applying the baseband signal b(t) as the (Figl .2)

modulating waveform. In this sense BPSK can be thought of as an AM signal.

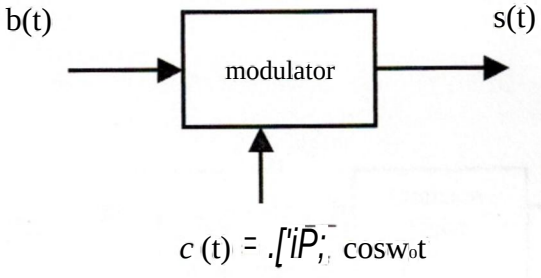


Figure 1.2 Modulating of the BPSK signal.

Timing diagrams of the modulator are shown in Fig 1.3

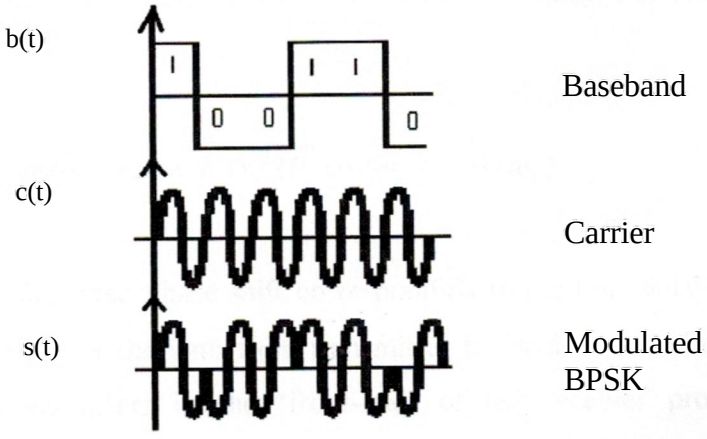


Fig. 1.3 Timing diagrams of the BPSK modulator

1.2.3 RECEIVER OF BPSK SYSTEM

To detect the original binary sequence of 1's and O's, we apply the noisy PSK wave b(t) (at the channel output) to a correlator, which is also supplied with a locally

generated coherent reference signal $c_1(t)$, as shown in Fig. 1.4. The correlator output, b_1, is compared with a threshold of zero volts. If $b_1 > 0$, the receiver decides in favor of symbol 1. On the other hand, if $b_1 < 0$, it decides in favor of symbol 0.

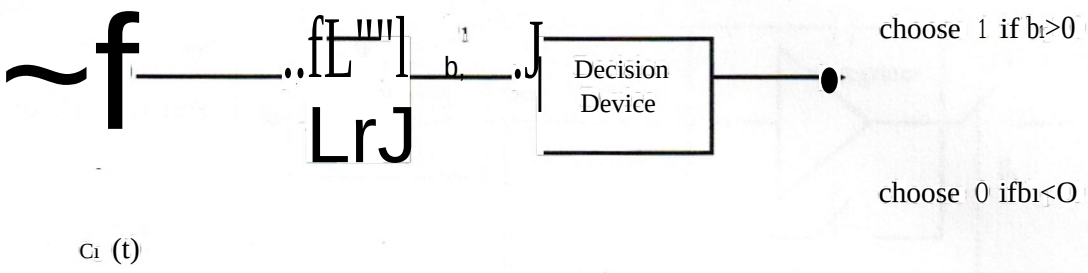


Figure 1.4 [Ref 6, page 278]

Now consider principle of generation carrier $c_1(t)$ and correlator. The received signal has the form

$$v_{BPSK} = b(t)\sqrt{\frac{2}{T_b}}\cos(\omega_{ot} + B) = b(t)\sqrt{\frac{2}{T_b}}\cos\omega_o(t + \theta/\omega_o) \quad (1.4)$$

Here 8 is a nominally fixed phase shift corresponding to the time delay $8/\omega_o$ which depends on the length of the path from transmitter to receiver and the phase shift produced by the amplifiers in the 'front-end' of the receiver proceeding the modulator. The original data b(t) is recovered in the demodulator. The demodulation technique usually employed is called synchronous demodulation and requires that there be available at the demodulator the waveform cos(root+8). A scheme for generating the carrier at the demodulator and for recovering the baseband signal is shown in Fig.1.5

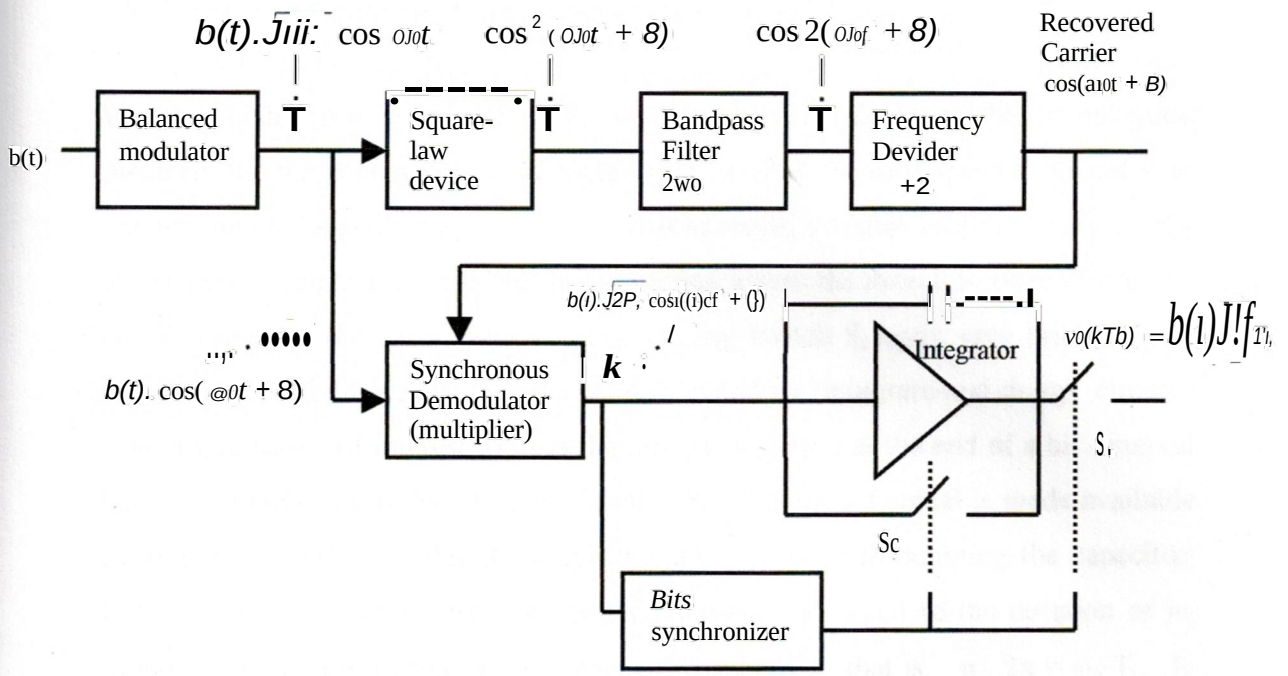


Figure 1.5 [Ref 17, page 251]

The received signal is squared to generate the signal

$$\text{Cos2(root+8)} = V_l + 1/_l \cos 2(\text{root}+8) \qquad (1.5)$$

The de component is removed by the bandpass filter whose passband is centred around 2fo and we then have the signal whose waveform is that of cos 2(root+8).A frequency divider is used to regenerate the waveform cos (root+8). Only the waveforms of the signals at the outputs of the squarer, filter and divider are relevant to our discussion and not their amplitudes. Accordingly Fig.1.5 we have arbitrarily taken each amplitude to be unity. In practice, the amplitudes will be determined by features of these devices which are of no present concern. In any event, the carrier having been recovered, it is multiplied with the received signal to generate

$$b(t)j_1P;.\cos 2(wo'+B) = b(t).J_IP:.[\sim + \sim \cos 2(w_0t+B)] \qquad (1.6)$$

which is then applied to an integrator as shown in Fig. 1.5.

We have included in the system a bit synchroniser. This device is able to recognise precisely the moment which corresponds to the end of the time interval allocated to one bit and the beginning of the next. At that moment, it closes switch Sc very briefly to discharge (dump) the integrator capacitor and leaves the switch Sc open during the entire course of the ensuing bit interval, closing switch Sc again very briefly at the end of the next bit time, etc. (This circuit is called an 'integrate-and-dump' circuit.) The output signal of interest to us is the integrator output at the end of a bit interval but immediately before the closing of switch Sc. This output signal is made available by switch S, which samples the output voltage just prior to dumping the capacitor. Let us assume for simplicity that the bit interval Tb is equal to the duration of an integral number n of cycles of the carrier of frequency/0, that is, $n \cdot 2n = r00\ Tb$. In this case the output voltage $v_0(kTb)$ at the end of a bit interval extending from time (k-1) Tb to k'I', is using following equation

$$v_0(kJ'ı) = b(kl'tı)Jıii:. \int_{(k-l)Th}^{kTb} \frac{1}{2}dt + b(kl'ı)Jıii:. \int_{(k-l)Tb}^{kTb} \frac{1}{2}\cos 2(w_0t + O)dt$$

$$= b(kTb).1\{2 \cdot .Tb \qquad (1.7)$$

since the integral of a sinusoid over a whole number of cycles has the value zero. Thus we see that our system reproduces at the demodulator output the transmitted bit stream b(t). The operation of the bit synchroniser allow us to sense each bit independently of every other bit. The brief closing of both switches, after each bit has been determined, wipes clean all influence of a proceeding bit and allows the receiver to deal exclusively with the present bit.

ÜUf rtl has been rather naive since it has ignored the effects of thermal noise, frequency jitter in the and random fluctuations in propagation delay. When

these perturbing influences need to be taken into account a phase-locked synchronisation system.

1.3 GEOMETRICAL REPRESENTATION OF BPSK SIGNALS

A BPSK signal can be represented, in terms of one orthonormal signal

$u_1(t) = \sqrt{\frac{2}{T_b}} \cos \omega_0 t$ as

$$v_{BPSK}(t) = \left[\sqrt{P_s T_b}\, b(t)\right]\sqrt{\frac{2}{T_b}} \cos \omega_0 t = \left[\sqrt{P_s T_b}\, b(t)\right] u_1(t) \quad (1.8)$$

The binary PSK signal can then be drawn as in Fig.1.6. The distance d between signals is $d = 2\sqrt{P_s T_b} = 2\sqrt{E_b}$ where Eb = P_s Tb is the energy contained in a bit duration.

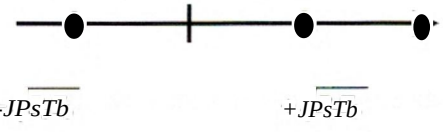


Figure 1.6 Geometrical representation of BPSK signals. [Ref 17, page 255]

The distance d is inversely proportional to the probability that we make an error when, in the presence of noise, we try to determine which of the levels of b(t) is being received.

1.4 BINARY FREQUENCY SHIFT -KEYING

In binary frequency-shift keying (BFSK) the binary data waveform d(t) generates a binary signal

$$v_{BFSK(t)} = \pm\sqrt{2P_s}\cos[\omega_0 t + d(t)\Delta\omega t] \quad (1.9)$$

Here d (t) = +1 or -1 corresponding to the logic levels 1 and 0 of the data waveform. The transmitted signal is of amplitude $\sqrt{2P_s}$ and is either

$$v_{BFSK}(t) = s_H(t) = \pm\sqrt{2P_s}\cos(\omega_0 + \Delta\omega)t \quad (1.10)$$

$$v_{BFSK(c)=s_L}(t) = \pm\sqrt{2P_s}\cos(\omega_0 - \Delta\omega)t \quad (1.11)$$

/ and thus has an angular frequency $\omega_0+\omega$ or $\omega_0-\Delta\omega$ with na constant offset from the nominal carrier frequency ω_0.

1.4.1 TRANSMITTER OF THE BFSK SIGNALS FSK MODULATOR

To generate a binary FSK signal, we may use the scheme shown in Fig.1.7. The input binary sequence is represented in its on-off form, with symbol 1 represented by a constant amplitude of $\sqrt{2P_s}$ volts and symbol 0 represented by zero volts. By using an inverter in the lower channel in Fig.1.7, we in effect make sure that when we have symbol 1 at the input, the oscillator with frequency ω_1 in the upper channel is switched on while the oscillator with frequency ω_2 in the lower channel is switched off. With the result that frequency w_1 is transmitted. Conversely, when we have symbol 0 at the input, the oscillator in the upper channel is switched off, and the oscillator in the lower channel is switched on, with the result that frequency ω_2 is

transmitted. The two frequencies f_{01} and f_{02} are chosen to equal integer multiples of the bit rate $1/T_b$.

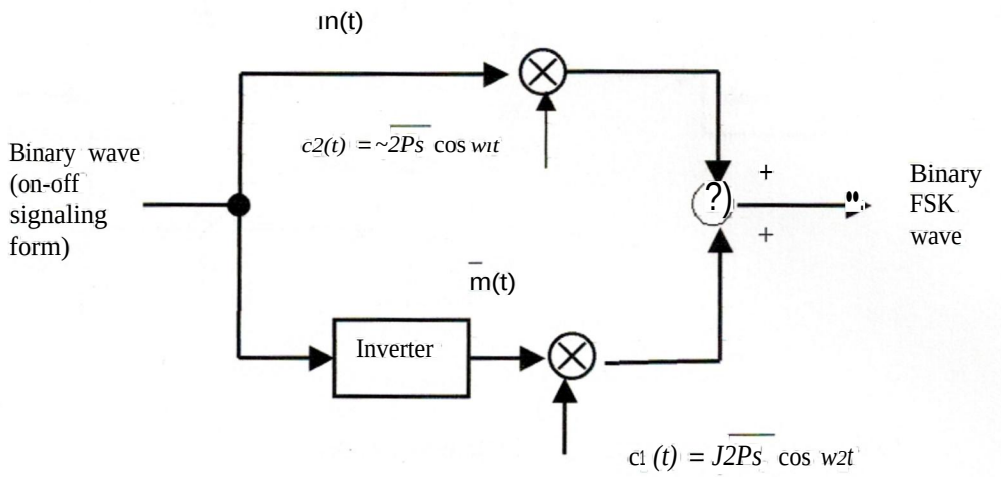


Figure 1.7 Binary FSK transmitter [Ref 6, page 283]

In the transmitter of Fig.1.7, we assume that the two oscillators are synchronized. Alternatively, we may use a single keyed (voltage-controlled) oscillator. In either case, the frequency of the modulated wave is shifted with a continuous phase, in accordance with the input binary wave. That is to say, phase continuity is always maintained, including the inter-bit switching times. We refer the this form of digital modulation as *Continuous - Phase Frequency - Shift Keying* (CPFSK).

1.4.2 COHERENT FSK RECEIVER

In order to detect the original binary sequence given the noisy received wave b(t), we may use the receiver shown in Fig.1.8. It consist of two correlators with a common input, which are supplied with locally generated coherent reference signals c_1 (t) and c_2(t). The correlator outputs are then subtracted, one from the other, and the resulting difference , *l*, is compared with a threshold of zero volts. If $l > 0$, the receiver decides in favor of 1. On the other hand, if $l < 0$, it decides in favor of 0.

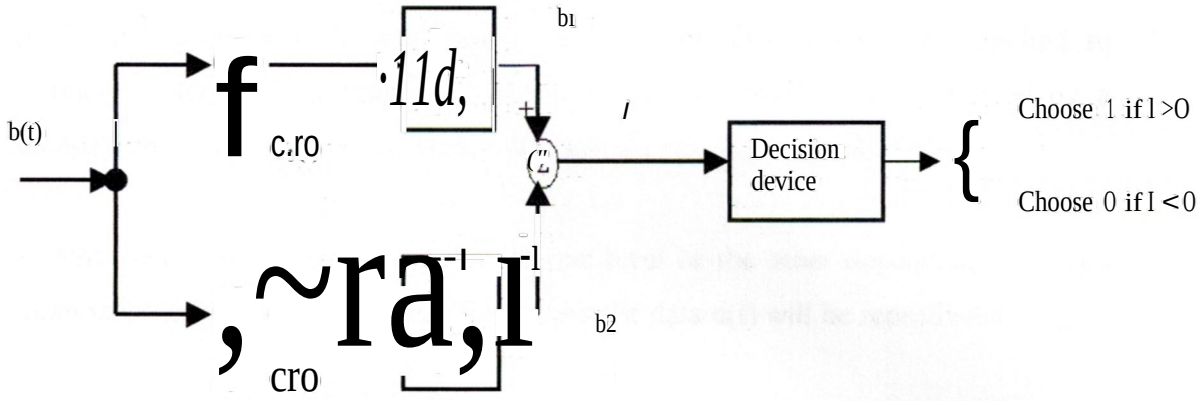


Figure 1.8 Coherent binary FSK receiver [Ref 6, page 283]

1.4.3 NON-COHERENT FSK RECEIVER

A BFSK signal can be demodulated by a receiver system as in Fig.1.9. The signal is applied to two band-pass filters one with centre frequency at f_1 the other at f_2. Here we have assumed, as above, that $f_1 - f_2 = 2(Q/21t) = 2f_b$. The filter frequency ranges selected do not overlap and each filter has a pass-band wide enough to encompass a main lobe in the spectrum of Fig. 1.9.

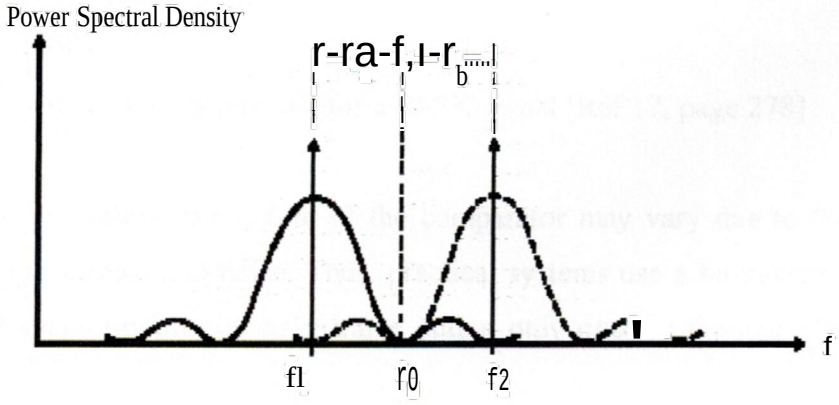


Figure 1.9 The power spectral densities [Ref 17, page 278]

Hence one filter will pass nearly all the energy in the transmission at f_1 the other will perform similarly for the transmission at f_2 . The filter outputs are applied to envelope detectors and finally the envelope detector outputs are compared by a comparator. A comparator is a circuit that accepts two input signals.

It generates a binary output which is at one level or the other depending on which input is larger. Thus at the comparator output the data d(t) will be reproduced.

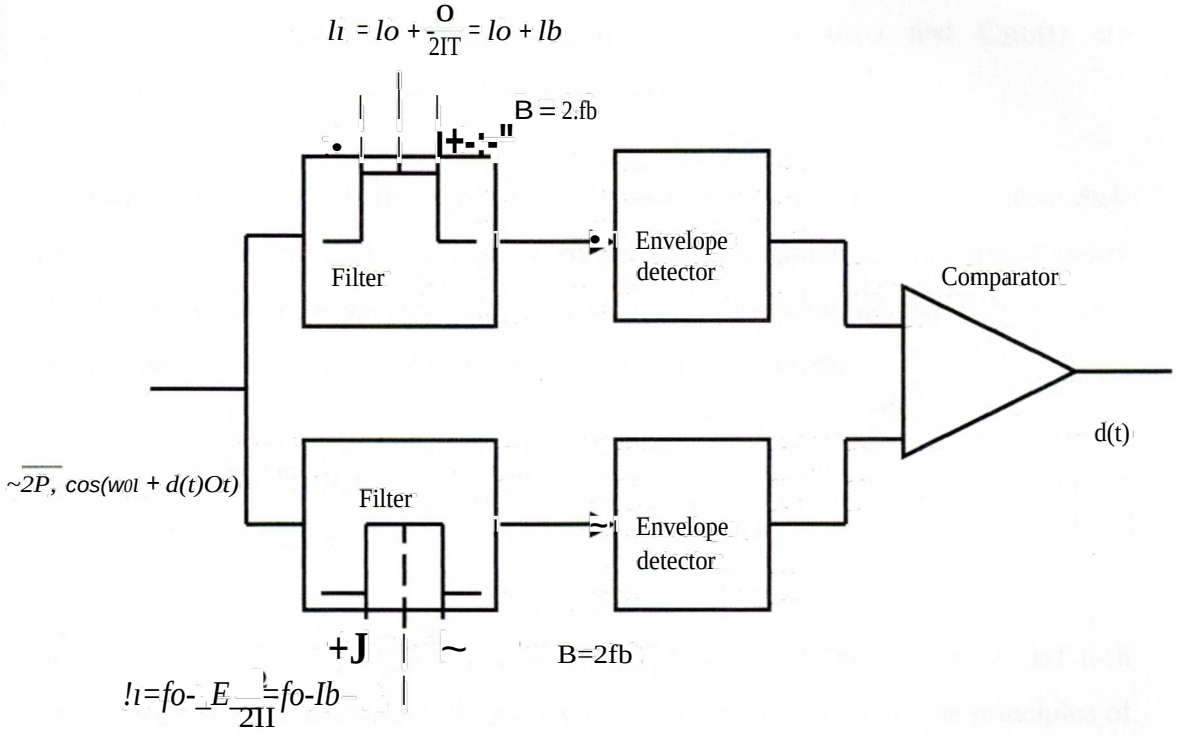


Figure 1.10 A receiver for a BFSK signal [Ref 17, page 278]

When noise is present, the output of the comparator may vary due to the systems response to the signal and noise. Thus, practical systems use a bit synchroniser and an integrator and sample the comparator output only once at the end of each time interval Tb.

1.4.4 GEOMETRICAL REPRESENTATION OF ORTHOGONAL BFSK

We noted, in M-ary phase-shift keying and in quadrature-amplitude shift keying, that any signal could be represented as $C_{1}u_{1}(t) + C_{2}u_{2}(t)$. There $u_{1}(t)$ and $u_{2}(t)$ are the orthonormal vectors in signal space, that is, $u_{1}(t) = \sim\sqrt{2/T_b}\cos mj$ and $u_{2}(t) = \sim\sqrt{2/\sim}\sin(\iota)J$. The functions u_{1} and u_{2} are orthonormal over the symbol interval Ts and, if the symbol is a single bit, Ts= Tb. The coefficients C_{1} and C_{2} are constants. The normalised energies associated with $C_{1}u_{1}(t)$ and $C_{2}u_{2}(t)$ are respectively c_{1}^{2} and c_{2}^{2} and the total signal energy is $c_{1}^{2} + c_{2}^{2}$

In M-ary PSK and QASK the orthogonality of the vectors u_{1} and u_{2} results from their phase quadrature. In the present case of BFSK it is appropriate that the orthogonality should result from a special selection of the frequencies of the unit vectors. Accordingly, with m and n integers, let us establish unit vectors

$$u_{1}(t) = \sim\sqrt{2/T_b}\cos 2\pi m f_1 t \qquad (1.12)$$

$$u_{2}(t) = \sim\sqrt{2/T_b}\cos 2\pi n f_1 t \qquad (1.13)$$

in which, as usual, $f_b = 1/T_b$. The vectors $u_{1}(t)$ and $u_{2}(t)$ are the m-th and n-th harmonics of the (fundamental) frequency f_b. As we are aware, from the principles of Fourier analysis, different harmonics $(m \pm n)$ are orthogonal over the interval of the fundamental period $T_b = 1/f_1$. If now the frequencies f_h and f_L in a BFSK system are selected to be (assuming m>n)

$$f_h = mf_1 \qquad (1.14)$$

$$f_L = nf_1 \qquad (1.15)$$

then the corresponding signal vectors are

$$S_H(t) = \sqrt{E_b}\,u_{1}(t) \qquad (1.16)$$

(1.17)

SL(t) =-*[if;uı(t)*

The signal space representation of these signals is shown in Fig.1.11. The signals, like the unit vectors are orthogonal. The distance between signal end points is therefore d= *J2Eb*

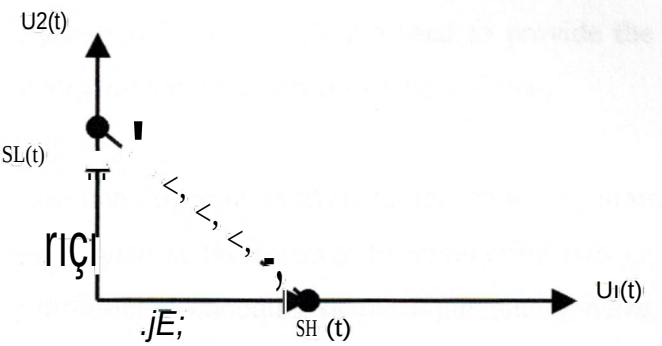


Fig. I.11 [Ref 17, page 280]

In a binary PSK system the distance between the two message points is equal to 2*Ji;,* whereas in a binary FSK system the corresponding distance is *J2Eb* .This shows that, in an AWGN channel, the detection performance of equal energy binary signals depends only on the 'distance' between the two pertinent message points in the signal space. In particular, the larger we make this distance, the smaller will the average probability of error be. This is intuitively appealing, since the larger the distance between the message points, the less will be the probability of mistaking one signal for the other.

1.5 DIFFERENTIAL PHASE-SHIFT KEYING

We observed in Fig.1.5 that, in BPSK, to regenerate the carrier we start by squaring *b(t)Jui:* cos *(J)i.* Accordingly, if the received signal were instead -

$b(t).[i\bar{P};$ cos $OJ/,$ the recovered carrier would remain as before. Therefore we shall not be able to determine whether the received baseband signal is the transmitted signal b(t) or its negative -b(t).

Differential phase-shift keying (DPSK) is modifications of BPSK which have the merit that they eliminate the ambiguity about whether the demodulated data is or is not inverted. In addition DPSK avoids the need to provide the synchronous carrier required at the demodulator for detecting a BPSK signal.

The DPSK as the non-coherent version of the PSK. It eliminates the need for a coherent reference signal at the receiver by combining two basic operations at the transmitter: (I) differential encoding of the input binary wave, and (2) phase-shift keying-hence, the name, DPSK. In effect, to send symbol 0 we phase advance the current signal waveform by 180°, and to send symbol 1 we leave the phase of the current signal waveform unchanged (Figure I. 12). The receiver is equipped with a storage capability, so that it can measure the *relative phase difference* between the waveforms received during two successive bit intervals. Provided that the unknown phase θ contained in the received wave varies slowly (that is, slow enough for it to be considered essentially constant over two bits intervals), the phase difference between waveforms received in two successive bit intervals will be independent of θ.

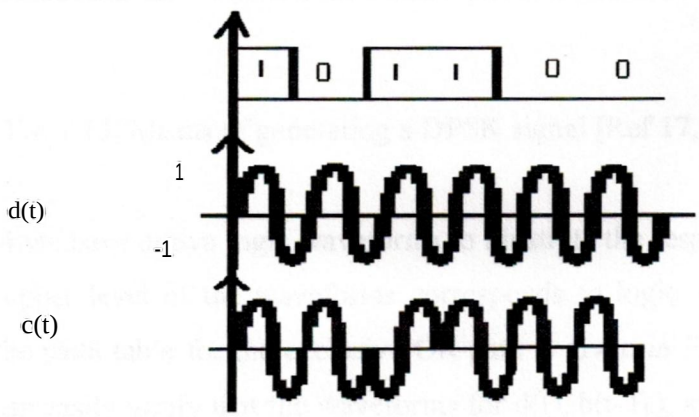
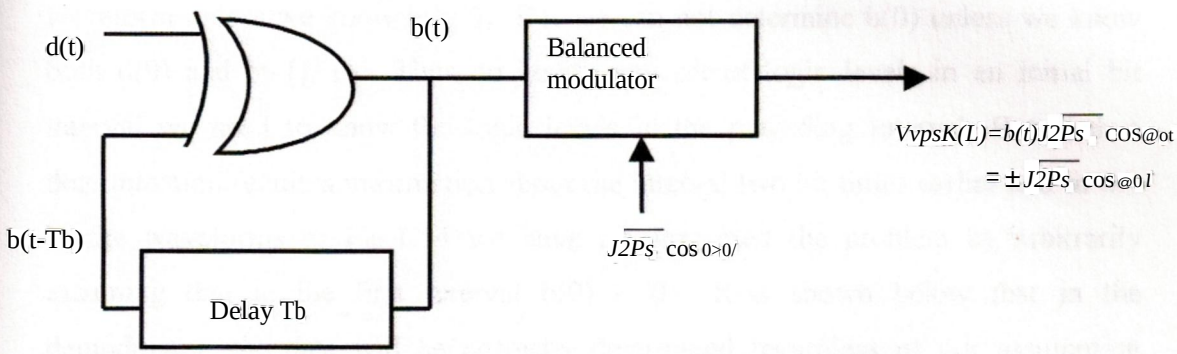


Figure 1.12

1.5.1 DPSK TRANSMITTER

A means for generating a DPSK signal is shown in Fig.1.13. The data stream to be transmitted d(t), is applied to one input of an exclusive-OR logic gate. To the other gate input is applied the output of the exclusive-OR gate b(t) delayed by the time Tb allocated to one bit. This second input is then b(t-Tb).



d(t)		b(t-Tb)		b (t)	
logic level	voltage	logic level	voltage	logic level	voltage
0	-1	0	-1	0	-1
0	-1	▮	▮	▮	▮
▮	1	0	-1	1	-1
1	1	▮	1	0	1

Fig. 1.13. Means of generating a DPSK signal [Ref 17, page 255]

In Fig. 1. 14 we have drawn logic waveforms to illustrate the response b(t) to an input d(t). The upper level of the waveforms corresponds to logic 1, the lower level to logic 0. The truth table for the exclusive-OR gate is given in Fig.1.13 and with this table we can easily verify that the waveforms for d(t), b(t-Ts), and b(t) are consistent with one another. We observe that, as required, b(t-Th) is indeed b(t) delayed by one

bit time and that in any bit interval the bit b(t) is given by b(t) = d(t) ⊕ b(t-Tb). In the ensuing discussion we shall use the symbolism d(k) and b(k) to represent the logic levels of d(t) and b(t) during the k-th interval.

Because of the feedback involved in the system of Fig.1.14 there is a difficulty in determining the logic levels in the interval in which we start the draw the intervals (interval 1 in Fig.1.14). We can not determine b(t) in this first interval of our waveform unless we know b(k=O). But we can not determine b(O) unless we know both d(O) and b(-1), etc. Thus, to justify any set of logic levels in an initial bit interval we need to know the logic levels in the preceding interval. But such a determination requires information about the interval two bit times earlier and so on. In the waveforms of Fig.1.14 we have circumvented the problem by arbitrarily assuming that in the first interval b(O) = 0 . It is shown below that in the demodulator, the data will be correctly determined regardless of our assumption concerning b(O).

The response of b(t) to d(t) is that b(t) changes level at the beginning of each interval in which d(t) = 1 and b(t) does not change level when d(t) = 0. Thus during interval 3, d(3) =1, and correspondingly b(3) changes at the beginning at that interval. During intervals 6 and 7

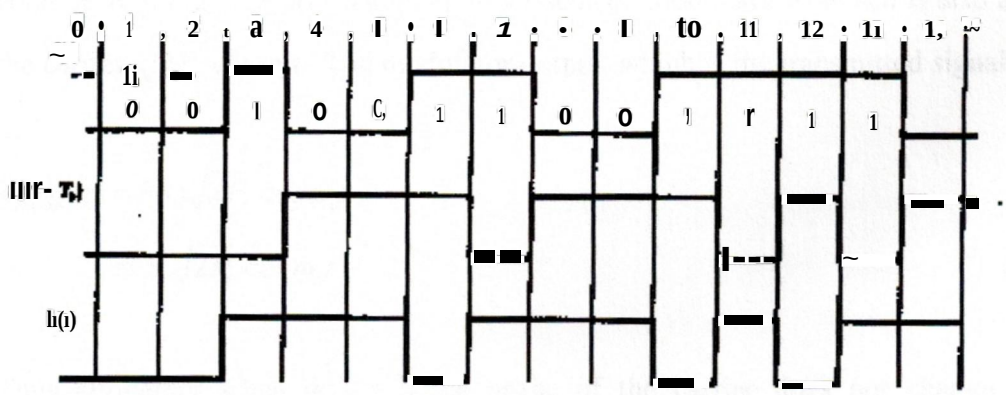


Figure 1.14 Logic waveforms to illustrate the response b(t) to an input d(t)

[Ref 17, page 256]

d(6) = d(7) = 1 and there are changes in b(t) at the beginnings of both intervals. During bits 10, 11, 12 and 13 d(t) = 1 and there are changes in b(t) at the beginnings of each of these intervals. This behaviour is to be anticipated from the truth table of the exclusive-OR gate. When d(t) = 0, b(t) = b(t-Tb) so that, whatever the initial value of b(t-Tb), it reproduces itself. On the other hand when d(t) = 1 then b(t) = b(t-Tb). Thus, in each successive bit interval b(t) changes from its value in the previous interval. Note that in some intervals where d(t) = 0 we have b(t) = 0 and in other intervals when d(t) =Owe have b(t) = 1. Similarly, when d(t) = 1 sometimes b(t) = 1 and sometimes b(t) = 0. Thus there is no correspondence between the levels of d(t) and b(t), and the only invariant feature of the system is that a change (sometimes up and sometimes down) in b(t) occurs whenever d(t) = 1, and that no change in b(t) will occur whenever d(t) = 0.

Finally, the waveforms of Fig.1.14 are drawn on the assumption that, in interval 1, b(O) = 0. As is easily verified, if not intuitively apparent, if we had assumed b(O) = 1, the invariant feature by which we have characterised the system would continue to apply. Since b(O) must be either b(O) = 0 or b(O) = 1, there being no other possibilities, our result is valid quite generally. If, however, we had started with b(O) = 1, the levels b(l) and b(O) would have been inverted.

As is seen in Fig 1.13 b(t) is applied to a balanced modulator to which is also applied the carrier $\sqrt{\frac{2P}{T_b}}\cos \omega_c t$. The modulator output, which is the transmitted signal is

$$\begin{aligned} v_{DPSK}(t) &= b(t)\sqrt{\frac{2P}{T_b}}\cos \omega_c t \\ &= \pm \sqrt{\frac{2P}{T_b}}\cos \omega_c t \end{aligned} \qquad (1.18)$$

Thus altogether when d(t) = 0 the phase of the carrier does not change at the beginning of the bit interval, while when d(t) = 1 there is a phase change of magnitude n.

1.4.1 DPSK RECEIVER

A method of demodulating the DPSK signal is shown in Fig.1.15. At the receiver input, the received DPSK signal plus noise (n(t)) is passed through a bandpass filter centered at the carrier frequency ω_0 so as to limit the noise power. The filter output and a delayed version of it, with the delay equal to the bit duration Tb, are applied to a correlator, as depicted in Fig. 1.15. Correlator consist of the multiplier and integrator.

The multiplier output is

$$b(t)b(t-T_b)(2P_s)\cos(\omega_0 t + \theta)\cos[\omega_0(t-T_b)+\theta]$$

$$= b(t)b(t-T_b)P_s\{\cos\omega_0 T_b + \cos[\omega_0(2t-T_b)+2\theta]\} \quad (1.19)$$

The first term on the right hand-side of this equation is, aside from a multiplicative constant, the waveform b(t)(t-Tb) which, as we shall see is precisely the signal we require. As noted previously in connection with BPSK, and so here, the output integrator will suppress the double frequency term. We should select $\omega_0 T_b$ so that $\omega_0 T_b = 2n\pi$ with n an integer. For, in this case we shall have $\cos \omega_0 T_b = +1$ and the signal output will be as large as possible.

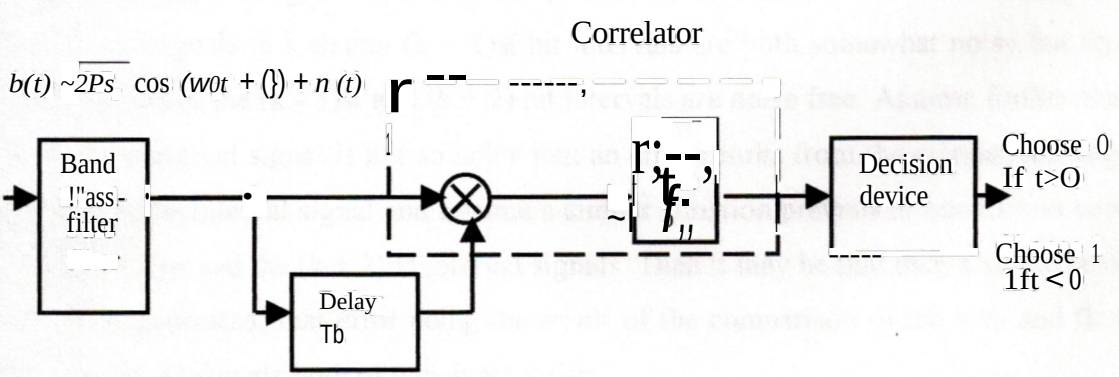


Figure 1.15 DPSK demodulator [Ref 6, page 308]

Further, with this selection, the bit duration encompasses an integral number of clock cycles and the integral of the double-frequency term is exactly zero.

The correlator output is finally compared with a threshold of zero volts, and a decision is thereby made in favor of symbols 'l' or 'O'. If the correlator output is positive, there was no phase change, b(t) = bit-Ts). both being +IV or -IV, and the receiver decides its favor of symbol zero. If correlator output negative, there was a phase change and either b(t) = + IV, with b(t-Tb) = -IV or vice versa, and the receiver decides in favor of symbol 1.

The differentially coherent system, DPSK, which we have been describing has a clear advantage ov:er the coherent BPSK system in that the former avoids the need for complicated circuitry used to generate a local carrier at the receiver. To see the relative disadvantage of DPSK in comparison with PSK, consider in a PSK system an error would be made in the determination of whether the transmitted bit was a 1 or a 0. In DPSK a bit determination is made on the basis of the signal received in two successive bit intervals. Hence noise in one bit interval may cause errors to two bit determinations.

The error rate in DPSK is therefore grater than in PSK, and, as a matter of fact, there is a tendency for bit errors to occur in pairs. It is not inevitable however that errors occur in pairs. Single errors are still possible. For consider a case in which the received signals in k-th and (k + l)st bit intervals are both somewhat noisy but that the signals in the (k - 1)st and (k + 2) nd intervals are noise free. Assume further that the k-th interval signal is not so noisy that an error results from the comparison with the (k - 1)st interval signal and assume a similar situation prevails in connection with the (k + 1)st and the (k + 2)nd interval signals. Then it may be that only a single error will be generated, that error being the result of the comparison of the k-th and (k + l)st interval signals both of which are noisy.

1.6 DIFFERENTIALLY-ENCODED PSK (DEPSK)

The DPSK demodulator requires a device which operates at the carrier frequency and provides a delay of Tb. Differentially-encoded PSK eliminates the need for such a piece of hardware. In this system, synchronous demodulation recovers the signal b(t), and the decoding ofb(t) to generate d(t) is done at baseband.

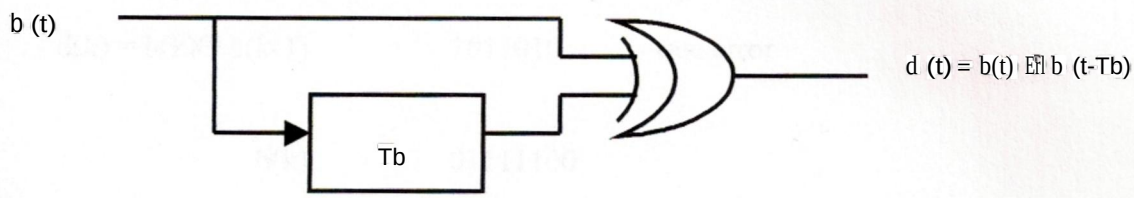


Figure 1.16 Baseband decoder to obtain d(t) from b(t) [Ref 17, page 258]

The transmitter of the DEPSK system is identical to the transmitter of the DPSK system shown in Fig.1.13. The signal b(t) is recovered in exactly the manner shown in Fig. I. 5 for a BPSK system. The recovered signal is then applied directly to one input of an exclusive-OR logic gate and to the other input is applied b(t - Tb) (see Fig.1.16). The gate output will be at one or the other of its levels depending on whether b(t)=b(t-Tb) orb(t)=$\overline{b(t-Tb)}$. In the first case b(t) did not change level and therefore the transmitted bit is d(t) = 0. In the second case d(t) = 1.

We have seen that in DPSK there is a tendency for bit errors to occur in pairs but that single bit errors are possible. In DEPSK errors always occur in pairs. The reason for the difference is that in DPSK we do not make a hard decision, in each bit interval about the phase of the received signal. We simply allow the received signal in one interval to compare itself with the signal in an adjoining interval and, as we have seen, a single error is not precluded. In DEPSK, a firm definite hard decision is made in each interval about the value of b(t). If we make a mistake, then errors must result

from a comparison with the preceding and succeeding bit. This result is illustrated in Fig. I. 17.

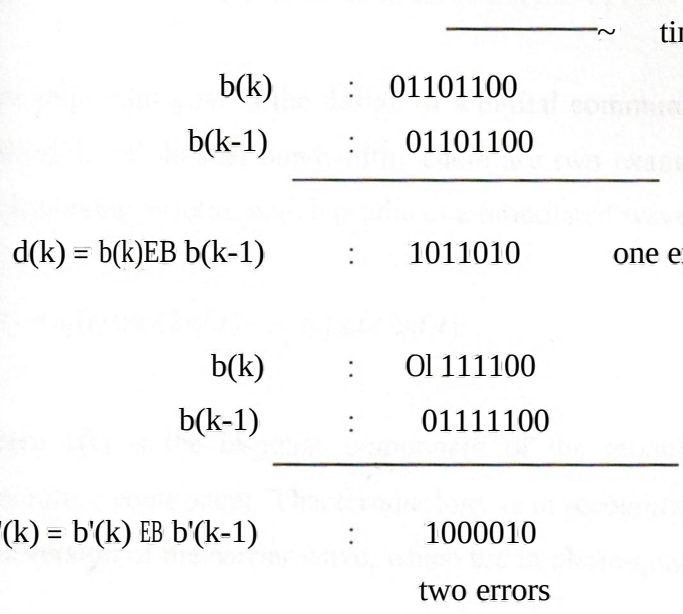


Figure 1.17 Errors in differentially encoded PSK occur in pairs [Ref 17, page 259]

In Fig. 1.17.a is shown the error free signals b(k), b(k - 1) and d(k) = b(k) EB b(k-1). In Fig.1.17.b we have assumed that b'(k) has a single error. Then b'(k-I) must also have a single error. We note that the reconstructed waveform d'(k) now has two errors.

CHAPTER2 M-ARY MODULATION TECHNIQUES

2.1 COHERENT QUADRATURE-MODULATION TECHNIQUES

One important goal in the design of a digital communication system is the efficient utilisation of channel bandwidth. There are two examples of the quadrature-carrier multiplexing system, which produces a modulated wave described as follows:

$$s(t) = s_I(t)\cos(2efJ) - s_Q(t)\sin(2efJ) \quad (2.1)$$

where $s_I(t)$ is the in-phase component of the modulated wave, and $S_Q(t)$ is the quadrature component. This terminology is in recognition of the associated cosine or sine version of the carrier wave, which are in phase-quadrature with each other.

We first study a quadrature-carrier signalling technique known as quadriphase-shift keying, which is an extension of binary PSK. Next we consider minimum shift keying, which is a special form of continuous-phase frequency-shift keying (CPFSK).

As with binary PSK, this modulation scheme is characterised by the fact that the information carried by th.e. transmitted wave is contained in the phase. In particular, in quadriphase-shift keying (QPSK), the phase of the carrier takes on one of four equally spaced values, such as *n/4,3n/4,5n/4,* and *7n/4* as shown by

$$S_i(t) = \sqrt{\frac{2E}{T}}\cos\left[\omega_i t + (2i-1)\frac{\pi}{4}\right] \quad (2.2)$$

where 1=1,2,3,4. Each possible value of the phase corresponds to a unique pair of bits called a *di bit.* Thus, for example, we may choose the foregoing set of phase values to represent the Gray encoded set of dibits: 10, 00, 01, and 11.

Using a well-known trigonometric identity, we may rewrite Eq.2.2 in the equivalent form:

$$S_i(t) = \sqrt{\frac{E}{2}}\cos(2i-1)\frac{\pi}{4}\cos w_0 t - \sqrt{\frac{E}{2}}\sin(2i-1)\frac{\pi}{4}\sin w_0 t \qquad (2.3)$$

This signal can be represented in terms of the two orthonormal signals

$$c_1(t) = \sqrt{\frac{2}{T}}\cos w_0 t$$

and

$$c_2(t) = \sqrt{\frac{2}{T}}\sin w_0 t \qquad (2.4)$$

There are four message points, and the associated signal vectors are defined by

$$S_i(t) = \left[\sqrt{\frac{E}{2}}\cos(2i-1)\frac{\pi}{4}, -\sqrt{\frac{E}{2}}\sin(2i-1)\frac{\pi}{4}\right] \quad i = 1,2,3,4 \qquad (2.5)$$

The elements of the signal vectors, namely, s_{i1} and s_{i2}, have their values summarised in Table 2.1. The first two columns of this table give the associated dibits and phase of the QPSK signal.

Input dibit	Phase of QPSK signal(radians)	Coordinates of Message points s_{i1}	s_{i2}
10	IT/4	$+\sqrt{\frac{E}{2}}$	$-\sqrt{\frac{E}{2}}$
00	3IT/4	$-\sqrt{\frac{E}{2}}$	$-\sqrt{\frac{E}{2}}$
01	5IT/4	$-\sqrt{\frac{E}{2}}$	$+\sqrt{\frac{E}{2}}$
11	7I1/4	$+\sqrt{\frac{E}{2}}$	$+\sqrt{\frac{E}{2}}$

Table 2.1 Signal-Space Characterisation of QPSK [Ref 6, page 285]

Accordingly, a QPSK signal is characterised by having a two-dimensional signal constellation (i.e. N = 2) and four message points (i.e. M = 4), as illustrated in Fig.2.1.

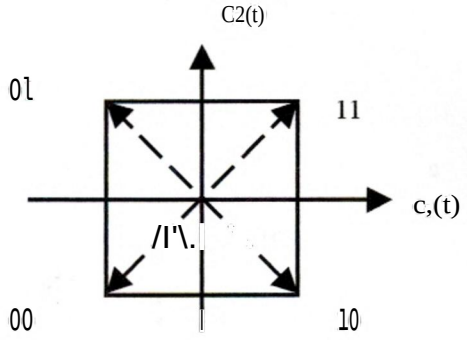


Figure 2.1 Signal-Space diagram of QPSK system [Ref 6, page 286]

Figure 2.2 illustrates the sequence and waveforms involved in the generation of a QPSK signal. The input binary sequence 01101000 is shown in Fig.2.2.a. This sequence is divided into two other sequences, consisting of odd-and even-numbered bits of the input sequence. These two sequences are shown in the top lines of Figs 2.2.b and 2.2.c.

The waveforms representing in the in-phase and quadrature components of the QPSK signal are also shown in Figs 2.2.b and 2.2.c, respectively. These two waveforms may individua11y be viewed as examples of a binary PSK signal. Adding them, we get the QPSK waveform shown in Fig.2.2.d.

To realise the decision rule for the detection of the transmitted data sequence, we partition the signal space into four regions. as described here:

1. The set of points closest to the message point associated with signal vector s_1,
2. The set of points closest to the message point associated with signal vector s_2.
3. The set of points closest to the message point associated with signal vector s_3.

This is accomplished by constructing the perpendicular bisectors of the square formed by joining the four message points, and then marking off the appropriate regions.

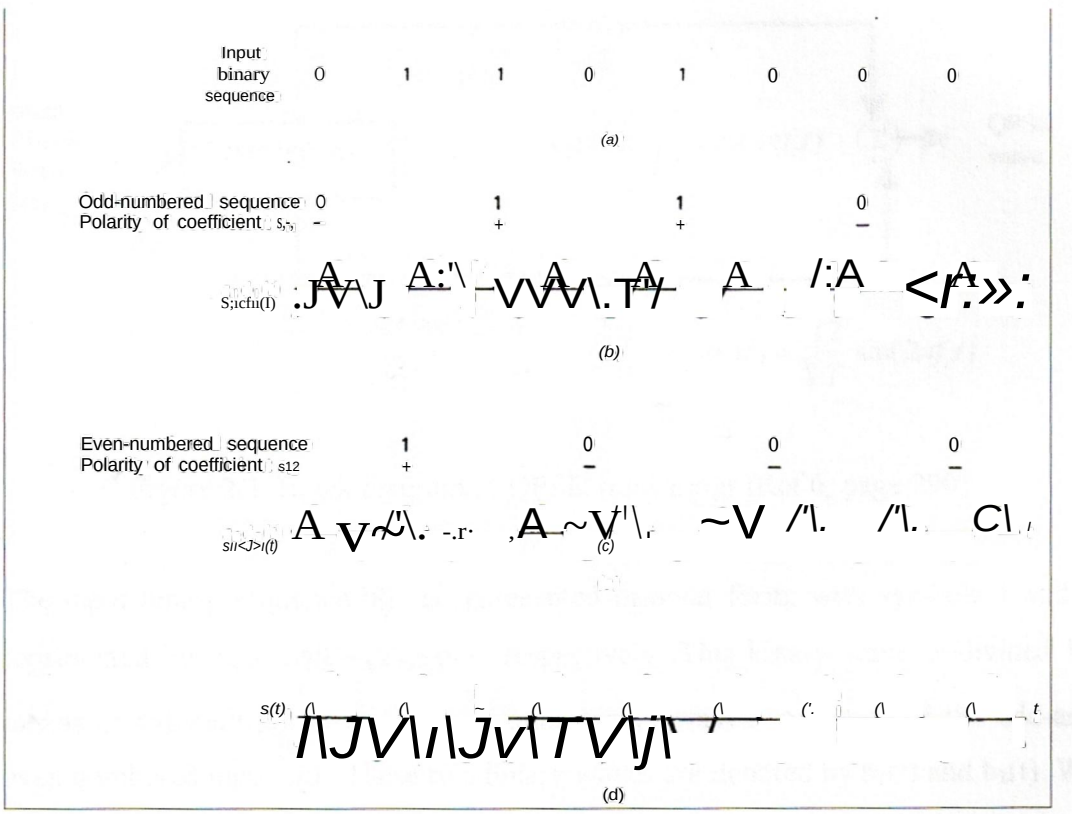


Figure 2.2 (a) Input binary sequence. (b) Odd-numbered bits of input sequence and associated binary PSK wave. (c) Even-numbered bits of input sequence and associated binary PSK wave. (d) QPSK waveform. [Ref 6, page 286]

We thus find that the decision regions are quadrants whose vertices coincide with the origin.

2.1.1 QPSK TRANSMITTER

Consider the generation and demodulation of QPSK. Fig.2.3 shows the block diagram of a typical QPSK transmitter.

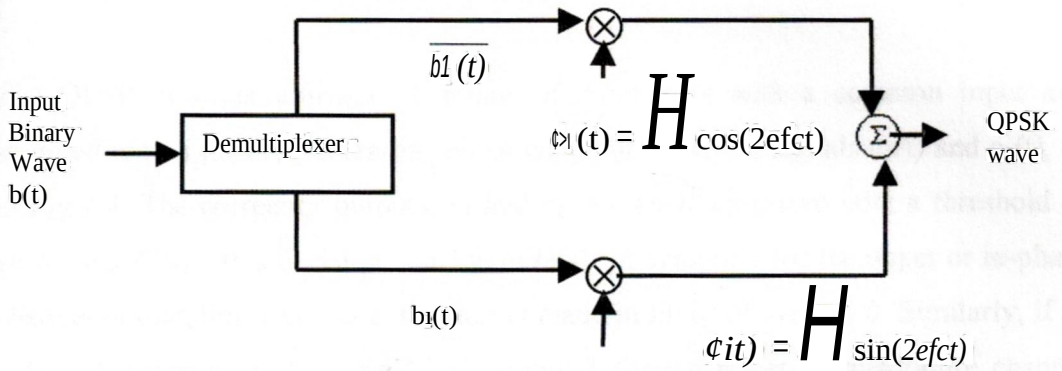


Figure 2.3 Block diagram ofQPSK transmitter [Ref 6, page 290]

The input binary sequence b(t) is represented in polar form, with symbols 1 and 0 represented by $+\sqrt{E_b}$ and $-\sqrt{E_b}$ volts, respectively. This binary wave is divided by means of a demultiplexer into two separate binary waves consisting of the odd-and even numbered input bits. These two binary waves are denoted by $b_1(t)$ and $b_2(t)$. We note that in any signalling interval, the amplitudes of $b_1(t)$ and $b_2(t)$ equals s_{i1} and s_{i2}, respectively, depending on the particular dibit that is being transmitted. The two binary waves $b_1(t)$ and $b_2(t)$ are used to modulate a pair of quadrature carriers or orthonormal basis functions: $c_1(t)$ equal to $\sqrt{\frac{2}{T_b}}\cos(w_{o1})$ and $c_2(t)$ equal to $\sqrt{\frac{2}{T_b}}\sin(@_{of})$. The result is a pair of binary PSK waves, which may be detected independently due to the orthogonality of $c_1(t)$ and $e_1(t)$. Finally, the two binary PSK waves are added to produce the desired QPSK wave. Note that the symbol duration, T, of a QPSK wave is twice as long as the bit duration, Tb, of the input binary wave. That is, for a given bit rate I/Tb, a QPSK wave requires half the transmission bandwidth of the corresponding binary PSK wave. Equivalently, for a given transmission bandwidth, a

QPSK wave carries twice as many bits of information as the corresponding binary PSK wave.

2.1.2 QPSK RECEIVER

The QPSK receiver consists of a pair of correlators with a common input and supplied with a locally generated pair of coherent reference signals $c_1(t)$ and $C2(t)$, as in Fig.2.4. The correlator outputs, x_1 and x_2, are each compared with a threshold of zero volts. If $x_1 > 0$, a decision is made in favor of symbol 1 for the upper or in-phase channel output, but if $x_1 < 0$ a decision is made in favor of symbol 0. Similarly, if $x_2 > 0$, a decision is made in favor of symbol 1 for the lower or quadrature channel output, but if $x_2 < 0$, a decision is made in favor of symbol 0.

Finally, these two binary sequences at the in-phase and quadrature channel outputs are combined in a multiplexer to reproduce the original binary sequence at the transmitter input with the minimum probability of symbol error.

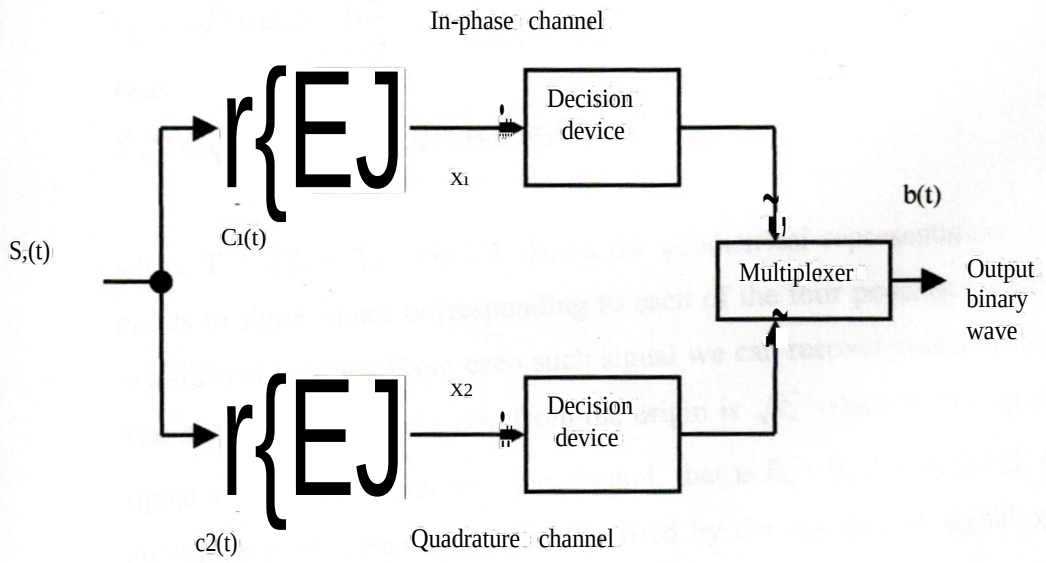


Figure 2.4 Block diagram of QPSK receiver [Ref 6, page 290]

2.1.3 SIGNAL SPACE REPRESENTATION

In section 2.1 we investigated four quadrature signals. Equation 2.2, repeated here, is

$$S_i(t) = \sqrt{\frac{2E_s}{T}} \cos[\omega_0 t + (2i-1)\pi/4] \qquad i=1, 2, 3, 4$$

These signals were then represented in terms of the two orthonormal signals $u_1(t) = \sqrt{\frac{2}{T}} \cos\omega_i t$ and $u_2(t) = \sqrt{\frac{2}{T}} \sin\omega_i t$

Energy Es in term of $p_s = \frac{E_s}{T}$;

$$S_i(t) = \sqrt{E_s} \cos(2i-1)\frac{\pi}{4} \sqrt{\frac{2}{T}} \cos\omega_0 t - \sqrt{E_s} \sin(2i-1)\frac{\pi}{4} \sqrt{\frac{2}{T}} \sin\omega_0 t \qquad (2.6)$$

$$S_{i1} = \sqrt{E_s} \cos(2i-1)\frac{\pi}{4} \qquad \text{and} \qquad (2.7a)$$

$$S_{i2} = -\sqrt{E_s} \sin(2i-1)\frac{\pi}{4} \qquad (2.7b)$$

Thus

$$S_i(t) = \sqrt{E_s} b_0(t) u_1(t) - \sqrt{E_s} b_0(t) u_1(t) \qquad (2.8)$$

where T = 2Tb = Ts . Fig.2.5 shows the geometrical representation of QPSK. The points in signal space corresponding to each of the four possible transmitted signals is indicared by dots. From each such signal we can recover two bits rather than one. The distance of a signal point from the origin is $\sqrt{E_s}$ which is the square root of the signal energy associated with the symbol that is Es= PsTs = P, (2Tb). Our ability to determine a bit without error is measured by the distance in signal space between points corresponding to the different values of the bit.

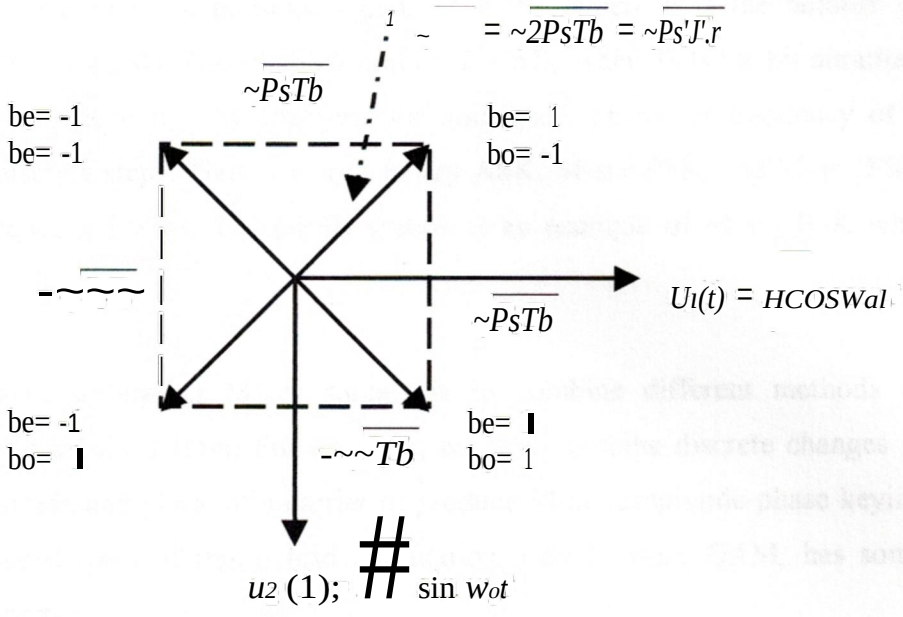


Figure 2.5 The four QPSK signals drawn in signal space [Ref 17, page 266]

We note in Fig.2.5 that points which differ in a single bit are separated by the distance

$$d = 2\sqrt{P_s T_b} = 2..\{if; \tag{2.9}$$

where Eb is the energy contained in a bit transmitted for a time Tb- This distance for QPSK is the same as for BPSK. Hence, altogether, we have the important result that, in spite of the reduction by a factor of two in the bandwidth required by QPSK in compression with BPSK, the noise immunities of two systems are the same.

2.2 M-ARY MODULATION

In an M-ary signalling scheme, we may send one of M possible signals, sı(t), gz(t), S3(t), ……, SM(t), during each signalling interval of duration T. For almost all

applications, the number of possible signals M = 2^n, where n is the number of encoded bits (n = $\log_2$ M). The symbol duration T = nTb, when Tb is the bit duration. These signals are generated by changing the amplitude, phase, or frequency of a carrier in M discrete steps. Thus, we have M-ary ASK, M-ary PSK, and M-ary FSK digital modulation schemes. The QPSK system is an example of M-ary PSK with M=4.

Another way of generating M-ary signals is to combine different methods of modulation into a hybrid form. For example, we may combine discrete changes in both the amplitude and phase of a carrier to produce M-ary amplitude-phase keying (APK). A special form of this hybrid modulation, called M-ary QAM, has some attractive properties.

M-ary signalling schemes are preferred over binary signalling schemes for transmitting digital information over band-pass channels when the requirement is to conserve bandwidth at the expense of increased power. In practise, we rarely find a communication channel that has the exact bandwidth required for transmitting the output of an information source by means of binary signalling schemes. Thus, when the bandwidth of the channel is less than the required value, we may use M-ary signalling schemes so as to utilise the channel efficiently.

To illustrate the bandwidth-conservation capability of M-ary signalling schemes, consider the transmission of information consisting of a binary sequence with bit duration Tb, If we were to transmit this information by means of binary PSK, for example, we require a bandwidth inversely proportional to Tb- However, if we take blocks of n bits and use an M-ary PSK scheme with M = 2^n and symbol duration T = nTb, the bandwidth required is inversely proportional to 1/nTb. This shows that the use ofM-ary PSK enables the reduction in transmission bandwidth by the factor n = $\log_2$M over binary PSK.

In this section we consider three different M-ary signalling schemes. They are M-ary PSK, M-ary QAM, and M-ary FSK, each of which offers virtues of its own.

2.2.1 M-ARY PSK

In M-ary PSK, the phase of the carrier takes on one of M possible values, namely, ei = 2i7t/M, where i = 0, 1, 2, ……., M-1. Accordingly, during each signalling interval of duration T, one of the M possible signals

$$s_i(t) = \sqrt{\frac{2E}{T}} \cos\left(\omega_0 t + \frac{2\pi i}{M}\right) \qquad i = 0, 1, \ldots\ldots M-1 \qquad (2.10)$$

Each si(t) may be expanded in terms of two basis function c1(t) and e:1(t) defined as

$$c_1(t) = \sqrt{\frac{2}{T}} \cos \omega_0 t \qquad (2.11)$$

$$c_2(t) = \sqrt{\frac{2}{T}} \sin \omega_0 t \qquad (2.12)$$

Both each c1(t) and c2(t) have unit energy. The signal constellation of M-ary PSK is therefore two-dimensional. The M message points are equally spaced on a circle of radius $\sqrt{E} = \sqrt{ST}$ and centre at the origin, as illustrated in Fig.2.6 for octaphase-shift-keying (i.e., M = 8). This figure also includes the corresponding decision boundaries indicated by dashed lines.

We can see from Fig. 2.6 the distance between two adjacent signal points decreases with increasing M (angle 7t/M decreases). From triangle AOB we have:

$$d = \sqrt{4E_s \sin^2 \frac{\pi}{M}} \qquad (2.13)$$

From Es = N Eh and M = 2 we have:

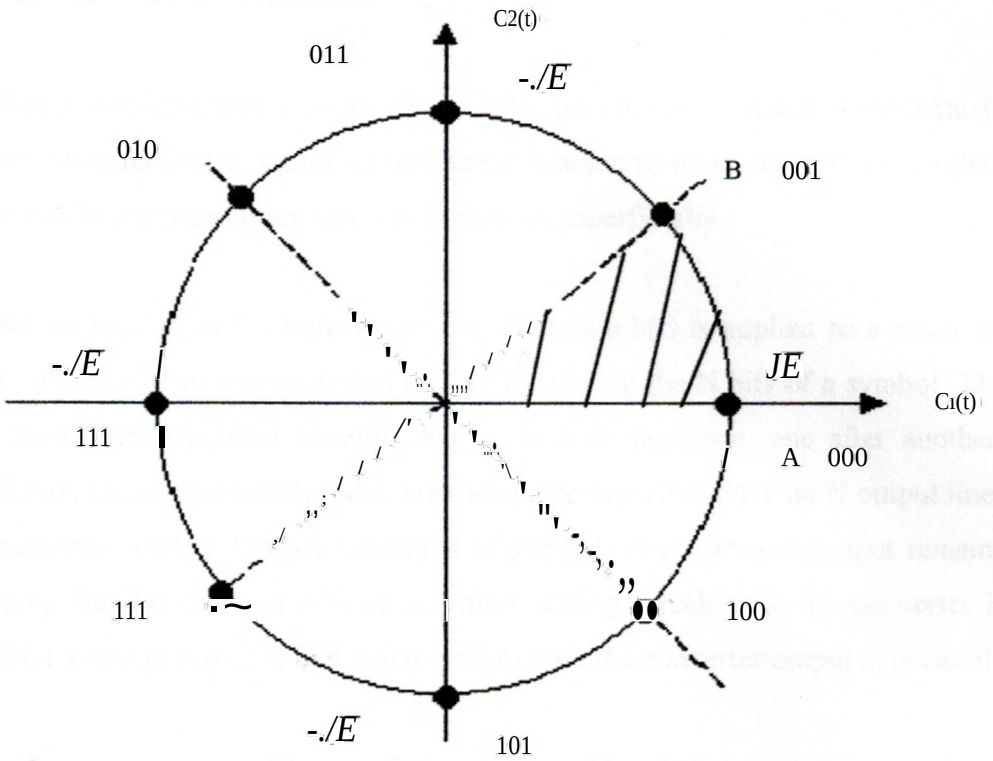


Figure 2.6 Signal constellation for octaphase-shift-keying (i.e., M = 8). The decision boundaries are shown as dashed lines. [Ref 6, page 314]

$$d = \sqrt{4NEb \sin^2 \frac{7r}{2N}} \qquad (2.14)$$

If M = 8 for 8-psk we have $d = \sim\sqrt{1.17Eb}$. (2.15)

For 16-PSK we obtain $d = \sim\sqrt{0.6Eb}$ (2.16)

Results (2.14), (2.15) and (2.16) shows that with increasing M distance of between vectors is decreased.

2.2.2 M-ARY QPSK TRANSMITTER

The physical implementation of an M-ary PSK transmission system is moderately elaborate. Such hardware is only of incidental concern to us in this text so we shall describe the M-ary transmitter-receiver somewhat superficially.

As shown in Fig.2.7, at the transmitter, the bit stream b(t) is applied to a serial-to-parallel converter. This converter has facility for storing the N bits of a symbol. The N bits have been presented serially, that is, in time sequence, one after another. These N bits, having been assembled, are then presented all at once on N output lines of the converter, that is they are presented in parallel. The converter output remains unchanging for the duration NT_b of a symbol during which time the converter is assembling a new group ofN bits. Each symbol time the converter output is updated.

The converter output is applied to a *Dl*A converter. This *Dl*A converter generates an output voltage which assumes one of $2^\circ = M$ different values in a one-to-one correspondence to the M possible symbols applied to its input. That is, the *Dl*A output is a voltage v(Si) which depends on the symbol Si (i = 0, I, ... M-1) . Finally v(Si) is applied as a control input to a special type of constant-amplitude sinusoidal signal source whose phase 0 is determined by v(Si). Altogether, then, the output is a fixed amplitude, sinusoidal waveform, whose phase has a one-to-one correspondence to the assembled N-bit symbol. The phase can change once per symbol time.

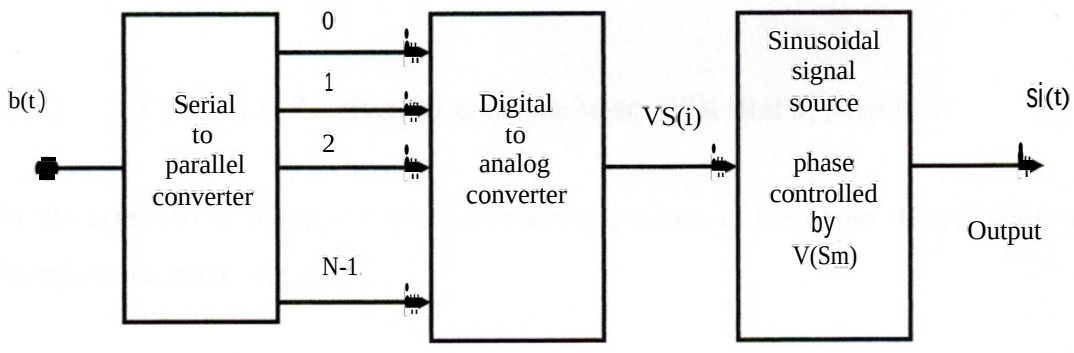


Figure 2.7 M-ary QPSK transmitter [Ref 17, page 269]

2.2.3 M-ARY QPSK RECEIVER

The optimum receiver for coherent M-ary PSK (assuming perfect synchronisation with the transmitter) is shown in block diagram form in Fig.2.8. It includes a pair of correlates with reference signals in phase quadrature. The two correlates outputs, denoted as x_I and x_Q, are fed into a phase discriminator that first computes the phase estimate

$$\hat{\theta} = \tan^{-1}\left(\frac{x_Q}{x_I}\right) = \frac{2in}{M} \qquad (2.17)$$

The phase discriminator then selects from the set {si(t), i = 0, ..., M-1} that particular signal whose phase is closest to the estimate $\hat{\theta}$.

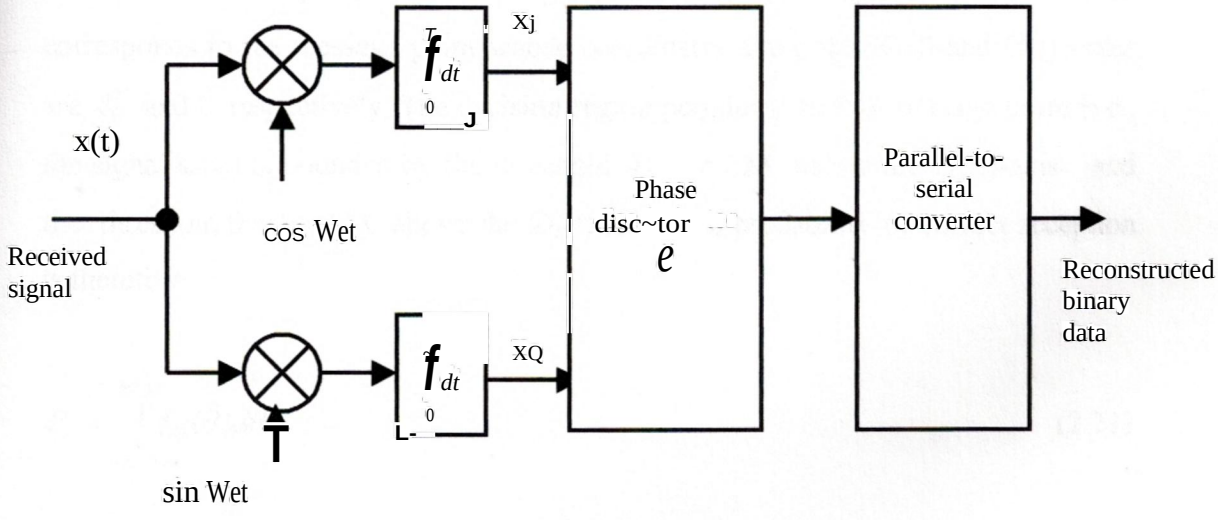


Figure 2.8 Receiver for coherent M-ary PSK [Ref 6, page 315]

In the presence of noise, the decision-making process in the phase discriminator is based on the noisy inputs.

$$x_i = \sqrt{E}\cos(\theta) + w_I \qquad i = 0, 1, \ldots, M-1 \tag{2.18}$$

and

$$x_I = -\sqrt{E}\sin(\theta) + w_Q \qquad i = 0, 1, \ldots, M-1 \tag{2.19}$$

where w_I and w_Q are samples of two independent Gaussian random variables W_I and W_Q whose mean zero and common variance equals

$$\sigma^2 = \frac{N_0}{2} \tag{2.20}$$

In Fig.2.6, we see that the message points exhibit circular symmetry. Moreover, both random variables W_I and W_Q have a symmetric probability density function. The implication of these symmetries is that in an M-ary PSK system, the average probability of symbol error, P_e, is independent of the particular signals $s_i(t)$ that is transmitted. We may therefore simplify the calculation of P_e by setting $\theta_i = 0$, which corresponds to the message point whose coordinates along the $\phi_1(t)$-and $\phi_2(t)$-axes are $\sqrt{E}$ and 0, respectively. The decision region pertaining to this message point [i.e., the signal $s_0(t)$] is bounded by the threshold $\hat{\theta} = -\pi/M$ below the $\phi_1(t)$-axis and the threshold $\theta = +\pi/M$ above the $\phi_1(t)$-axis. The probability of correct reception is therefore

$$P_c = \int_{-\pi/M}^{\pi/M} f_\Theta(\hat{\theta})\, d\hat{\theta} \tag{2.21}$$

where $f_\Theta(\theta)$ is the probability density function of the random variable Θ whose sample value equals the phase discriminator output $\hat{\theta}$ produced in response to a received signal that consists of the signal $s_0(t)$ plus AWGN. That is,

$$\theta = \tan^{-1}\left(\frac{y}{x}\right) \tag{2.22}$$

The phase $\hat{\theta}$ is recognised to be the phase of a sine wave plus narrow-band noise. As such, the probability density function $p(\theta)$ has a known value. Specifically, for $-\pi \le \theta \le \pi$, we may write

$$p(\theta) = \frac{1}{2\pi} \exp\left(-\frac{E}{N_0}\right) + \frac{1}{\sqrt{\pi}} \cos\theta \exp\left(-\frac{E}{N_0}\sin^2\theta\right)\left[1 - \frac{1}{2}\operatorname{erfc}\left(\sqrt{\frac{E}{N_0}}\cos\theta\right)\right] \quad (2.23)$$

The probability density function $f_\theta(\hat{\theta})$ is shown plotted versus θ in Fig.2.9 for various values of E/N_0. We see that it approaches an impulse-like appearance about θ as E/N_0 assumes high values.

A decision error is made if the angle θ falls outside $-(\pi/M) \le \hat{\theta} \le (\pi/M)$. The probability of symbol error is therefore

$$P_c = 1 - P_c = 1 - \int_{-\pi/M}^{\pi/M} f_\theta(\hat{\theta})\, d\theta \quad (2.24)$$

In general, the integral in Eq.2.24 does not reduce to a simple form, except for M=2 and M=4. Hence, for M > 4, it must be evaluated by using numerical integration.

However, for large M and high values of, E/N_0 we may derive an approximate formula for P_e. For high values of E/N_0 and for $|\theta| < \pi/2$, we may use the approximation

$$\operatorname{erfc}\left(\sqrt{\frac{E}{N_0}}\cos\theta\right) \approx \frac{1}{\sqrt{\pi}\sqrt{\frac{E}{N_0}}\cos\theta} \exp\left(-\frac{E}{N_0}\cos^2\theta\right) \quad (2.25)$$

Hence, using this approximation for the complementary error function in Eq. 2.23 and simplifying terms, we finally get

$$f_{8(B)} = \cos B \exp\left(-\frac{E}{No}\sin^2 B\right) \qquad |\hat{0}| < \frac{7r}{2} \tag{2.26}$$

Thus, substituting Eq.2.26 in Eq.2.24, we get

$$Pe = 1 - \int_{-1r/M}^{1r/M} \cos B \exp\left(-\frac{E}{N_0}\sin^2 B\right) dB \tag{2.27}$$

Changing the variable of integration from θ to

$$z = \sin B \tag{2.28}$$

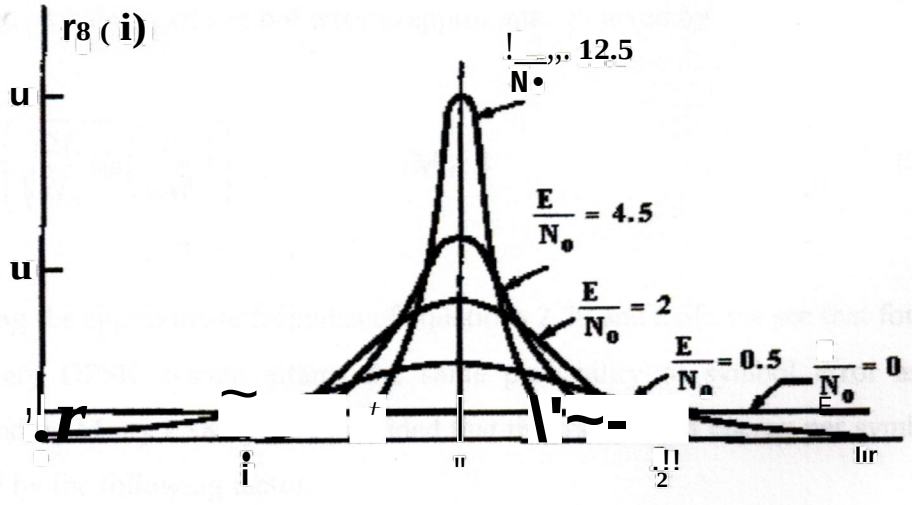


Figure 2.9 Probability density function of phase estimate θ [Ref 6, page 317]

We may rewrite Eq.2.27 as

$$p_e = 1 - \frac{2}{\sqrt{\pi}} \int_{0}^{\sqrt{E/N_0}\sin(1r/M)} \exp(-z^2)dz \tag{2.29}$$

This is the desired approximate formula for the probability of symbol error that results from the use of coherent M-ary PSK for M 2 4. The approximation becomes extremely tight, for fixed M, as EI N_0 is increased.

Coherent M-ary PSK requires exact knowledge of the carrier frequency and phase for the receiver to be accurately synchronised to the transmitter. When carrier recovery at the receiver is impractical, we may use differential encoding based on the phase difference between successive symbols at the cost of some degradation in performance. If the incoming data are encoded by a phase shift rather than by absolute phase, the receiver performs detection by comparing the phase of one symbol with that of the previous symbol, and the need for a coherent reference is thereby eliminated. The exact calculation of probability of symbol error for the differential detection of differential M-ary PSK (commonly referred to as M-ary DPSK) is much too complicated for M > 2. However, for large values of E/No and M 2 4, the probability of symbol error is approximately given by

$$P_e \approx \text{erfc}\left(\sqrt{\frac{E}{N_0}\sin^2\left(\frac{\pi}{M}\right)}\right) \qquad \text{M24} \qquad (2.30)$$

Comparing the approximate formulas of equations 2.29 and 2.30, we see that for M 2 4 an M-ary DPSK system attains the same probability of symbol error as the corresponding M-ary PSK system provided that the transmitted energy per symbol is increased by the following factor:

$$k(M) = \frac{\sin^2\left(\frac{\pi}{M}\right)}{2\sin^2\left(\frac{\pi}{M}\right)} \qquad \text{M24} \qquad (2.31)$$

For example, k(4) = 1.7. That is, differential QPSK (which is non-coherent) is approximately 2.3 dB poorer in performance than coherent QPSK.

2.3 M-ARYQAM

In BPSK, QPSK, and M-ary PSK we transmit, in any symbol interval, one signal or another which are distinguished from one another in phase but are all of the same amplitude. In each of these individual systems the end points of the signal vectors in signal space falls on the circumference of a circle. Now we have noted that our ability to distinguish one signal vector from another in the presence of noise will depend on the distance between the vector end points. It is hence rather apparent that we shall be able to improve the noise immunity of a system by allowing the signal vectors to differ, not only in their phase but also in amplitude. Thus we get a new modulation scheme called M-ary quadrature amplitude modulation (QAM). In this modulation scheme, the carrier experiences amplitude as well as phase modulation.

The signal constellation for M-ary QAM consist of a square lattice of message points, as illustrated in Fig.2.10 for M = 16. The corresponding signal constellations for the in-phase and quadrature components of the amplitude-phase modulated wave are shown in Fig.2.l la and 2.11b, respectively.

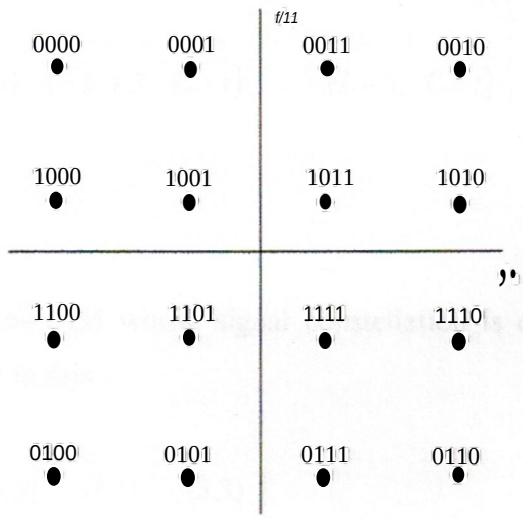


Figure 2. 10 Signal-constellation of M-ary QAM for M = 16 [Ref 6, page 318]

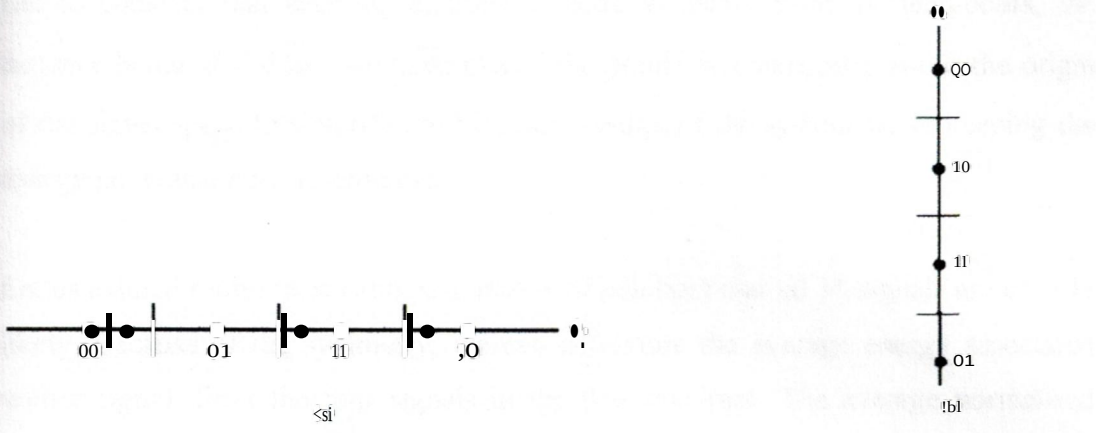


Figure 2.11 Decomposition of signal constellation of M-ary QAM (for M=l6) into two signal-space diagrams for (a) in-phase comment c₁(t), and (b) quadrature comment e₁(t). (The message points are identified by 2-bit Gray codes for later discussion.) [Ref 6, page 3 19]

The coordinates of the i-th message point are designed by L by L matrix:

$$\{a_i, b_i\} = \begin{bmatrix} (-L+1,L-1) & (-L+3,L-1) & \cdots & (L-1,L-1) \\ (-L+1,L-3) & (-L+3,L-3) & \cdots & (-L+1,L-3) \\ \vdots & \vdots & & \vdots \\ (-L+1,-L+1) & (-L+3,-L+1) & \cdots & (L-1,-L+1) \end{bmatrix} \quad (2.32)$$

$$\text{Where} L = \sqrt{M} \quad (2.33)$$

For example, for the 16-QAM whose signal constellation is depicted in Fig.2.10, where L=4, we have the matrix

$$\{a_i, b_i\} = \begin{bmatrix} (-3,3) & (-1,3) & (1,3) & (3,3) \\ (-3,1) & (-1,1) & (1,1) & (1,3) \\ (-3,-1) & (-1,-1) & (1,-1) & (3,-1) \\ (-3,-3) & (-1,-3) & (1,-3) & (3,-3) \end{bmatrix} \quad (2.34)$$

Let us consider that each signal point is equally distant from its neighbours, the distance being $d = \sqrt{1a}$. We have placed the points symmetrically about the origin of the signal space to simplify the hardware design of the system while keeping the energy per signal near a minimum.

Let us assume (quite reasonably as a matter of practice) that all 16 signals are equally likely. Because of the symmetry, we can determine the average energy associated with a signal, from the four signals in the first quadrant. The average normalised energy of a signal is:

$$Es = \frac{1}{4}[(a^2 + a^2) + (9a^2 + a^2) + (a^2 + 9a^2) + (9a^2 + 9a^2)] = 10a^2 \quad (2.35)$$

so that

$$a = \sqrt{0.1Es} \quad (2.36)$$

and

$$d = 2\sqrt{0.1Es} \quad (2.37)$$

In the present case since each symbol represents 4 bits, the normalised symbol energy is Es= 4Eb where Eb is the normalised bit energy. Hence

$$a = \sqrt{0.1Es} = \sqrt{0.4Eb} \quad \text{and} \quad d = 2\sqrt{0.4Eb} \quad (2.38)$$

This distance is significantly less than the distance between adjacent QPSK signals where, from Eq.2.9 $d = 2\sqrt{E}$; however the distance is greater for 16 QAM than for 16 MPSK where,

$$d = \sqrt{16Eb \sin^2 \frac{\pi}{16}} = 2\sqrt{0.1sEb} \quad (2.39)$$

Thus, 16 QAM will be shown to have a lower error rate than 16 MPSK, but a higher

error rate than QPSK.

A typical signal in Fig.2. 12 is

$$v_{QASK} = k_1 a c_1(t) + k_2 a c_2(t) \tag{2.40}$$

in which k_1 and k_2 are each equal to ± 1 or ± 3. Since we have that $c_1(t) = \sqrt{2/T}\cos(\omega_1 t)$, and that $c_2(t) = \sqrt{2/T}\sin(\omega_1 t)$ and $a = \sqrt{0.1E_s}$ we can write Eq.2.40 as

$$s_{QAM} = k_1 \sqrt{0.2\frac{E_s}{T_s}}\cos w_{o1} t + k_2 \sqrt{0.2\frac{E_s}{T_s}}\sin w_{o1} \tag{2.41}$$

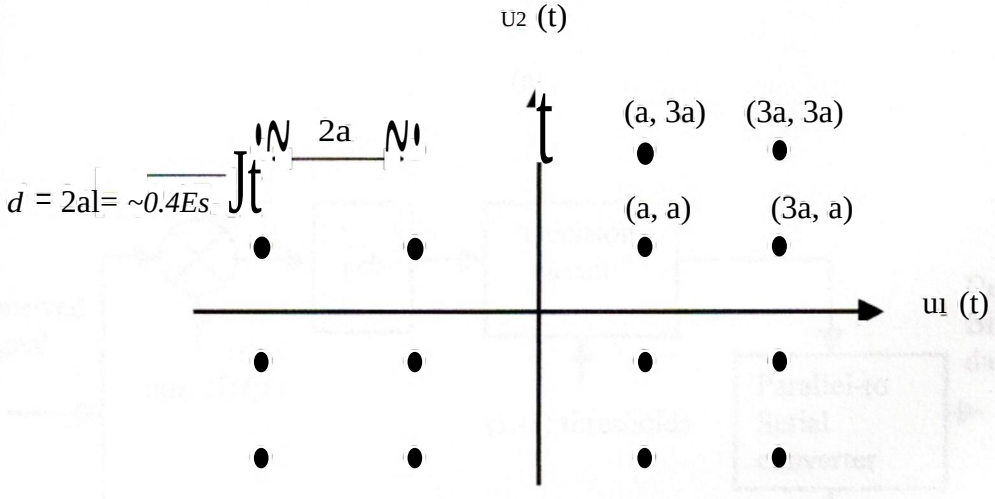


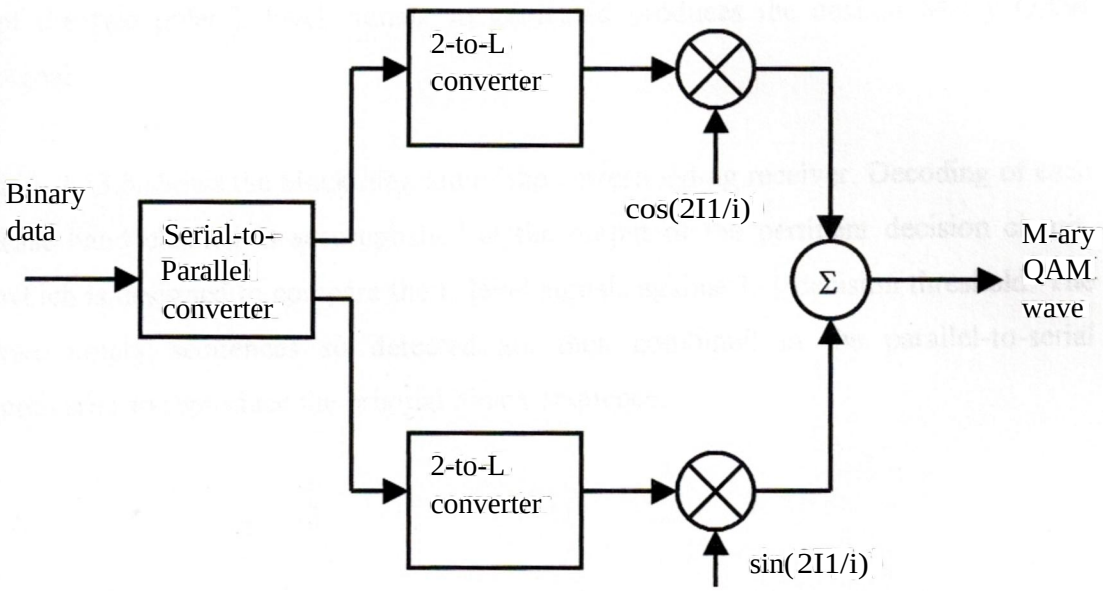
Figure 2.12 Geometrical representation of 16 signals in a QASK system [Ref 17, page 273]

And since $E_s / T_s = P_s$, we have

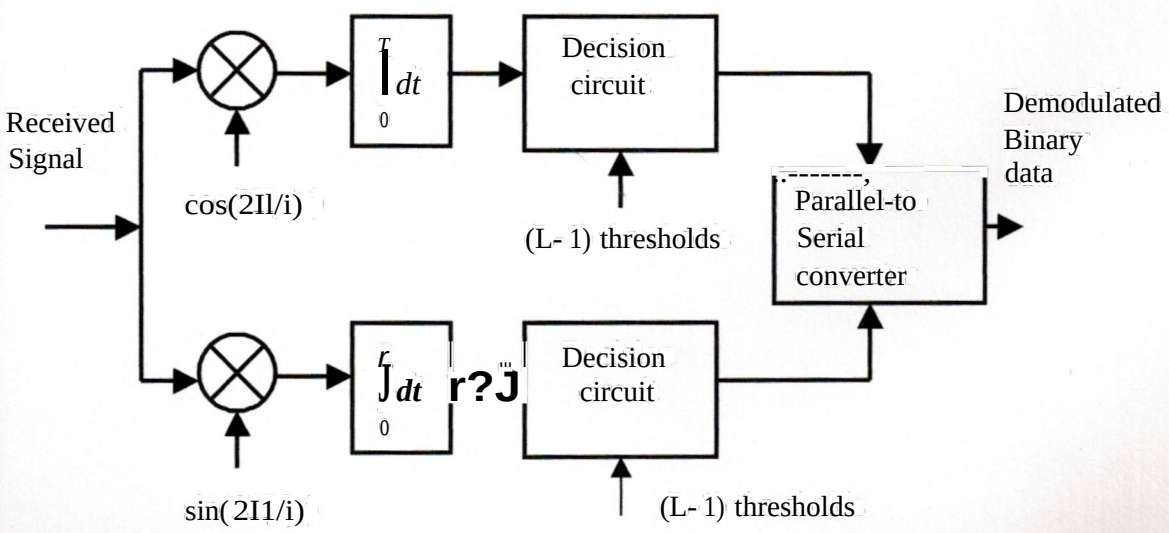
$$v_{QASK} = k_1 \sqrt{0.2 P_s}\cos(\omega_0 t) + k_2 \sqrt{0.2 P_s}\sin \omega_0 t \tag{2.42}$$

2.4 M-ARY QAM TRANSMITTER AND RECEIVER

Figure 2.13.a and 2.13.b shows that the transmitter and receiver of QAM system.



(a)



(b)

Figure 2.13 Block diagrams ofM-ary QAM system (a) Transmitter. (b) Receiver.

[Ref 6, page 322]

The serial-to-parallel converter accepts a binary sequence at a bit rate Rt, = 1 / Tb and produces two parallel binary sequences whose bit rates are Rb / 2 each. The 2-to-L level converters, where L = $\sqrt{M}$, generate polar L-level signals in response to the respective in-phase and quadrature channel inputs. Quadrature-carrier multiplexing of the two polar L-level signals so generated produces the desired M-ary QAM signal.

Fig. 2.13.b shows the block diagram of the corresponding receiver. Decoding of each base band channel is accomplished at the output of the pertinent decision circuit, which is designed to compare the L-level signals against L-1 decision threshold. The two binary sequences so detected are then combined in the parallel-to-serial converter to reproduce the original binary sequence.

CHAPTER3 ERROR PROBABILITY ANALYSIS OF THE DIGITAL MODULATION METHODS

A transmission system using binary encoding transmits a sequence of binary digits, that is, 1's and O's. These digits may be represented in a number of ways. For example, a 1 may be represented by a voltage V held for a time T, while a zero is represented by a voltage -V held for an equal time. In general the binary digits are encoded so that a 1 is represented by a signal $s_1(t)$ and a 0 by a signal s2(t), where $s_1(t)$ and s2(t) each have a duration T. The resulting signal may be transmitted directly or, as is more usually the case, used to modulate a carrier. The received signal is corrupted by noise, and hence there is a finite probability that the receiver will make an error in determining, within each time interval, whether a 1 or a 0 was transmitted.

In this chapter we make calculations of such error probabilities and discuss methods to minimize them. The discussion will lead us to the concept of the matched filter and correlator.

3.1 NOISE ANALYSIS OF THE RECEIVER

Consider that a binary-encoded signal consists of a time sequence of voltage levels +V or - V. If !ńere is sgllıı.ro j.IJJenıaJ between the bjt~ the s,iynal forms a se9uence of [illegible] n.~a\.\'ıle \)\l\<:;e<:;,. ln. e\tb.e\ case t\ıe\e is no ɋarticolar interest in preserving the waveform of the signal after reception. We are interested only in knowing within each bit interval whether the transmitted voltage was +V or -V. With noise present, the received signal and noise together will yield sample values generally different from ±V. In this case, what deduction shall we make from the sample value concerning the transmitted bit?

Suppose that the noise is Gaussian and therefore the noise voltage has a probability density which is entirely symmetrical with respect to zero volts. Then the probability that the noise has increased the sample value is the same as the probability that the noise has decreased the sample value. It then seems entirely reasonable that we can do no better than to assume that if the sample value is positive the transmitted level was +V, and if the sample value is negative the transmitted level was -V. It is, of course, possible that at the sampling time the noise voltage may be of magnitude larger than V and of a polarity opposite to the polarity assigned to the transmitted bit. In this case an error will be made as indicated in Fig.3.1. Here the transmitted bit is represented by the voltage +V which is sustained over an interval T from tı to *tı*. Noise has been superimposed on the level + V so that the voltage *v* represents the received signal and noise. If now the sampling should happen to take place at a time t = tı + ~t, an error will have been made.

We can reduce the probability of error by processing the received signal plus noise in such a manner that we are then able to find a sample time where the sample voltage due to the signal is emphasized relative to the sample voltage due to the noise. Such a processor (receiver) is shown in Fig.3.2. The signal input during a bit interval is indicated. As a matter of convenience we have set t = 0 at the beginning of the interval. The waveform of the signal s(t) before t = 0 and after t = T has not been indicated since, as will appear, the operation of the receiver during each bit interval is independent of the waveform during past and future bit intervals.

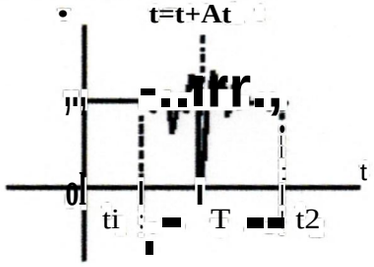


Figure 3.1 Illustration that noise may cause an error in the determination of a transmitted voltage level [Ref 17, page 442]

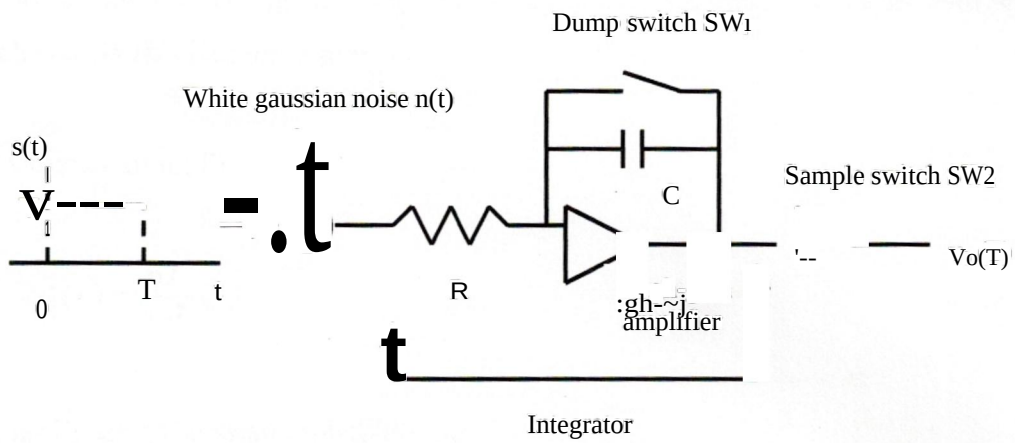


Figure 3.2 A receiver for a binary coded signal [Ref 17, page 443]

3.2 PEAK SIGNAL TO RMS NOISE OUTPUT VOLTAGE RATIO

The integrator yields an output which is the integral of its input multiplied by 1/RC. Using τ =RC, we have

$$v_o(T) = \frac{1}{T}\int_o [s(t) + n(t)]dt = \frac{1}{T}\int_o s(t)d(t) + \frac{1}{T}\int_o n(t)d(t) \qquad (3.1)$$

The sample voltage due to the signal is

$$s_o(T) = \frac{1}{T_o}\int V d(t) = \frac{VT}{T} \qquad (3.2)$$

The sample voltage due to the noise is

$$n_o(T) = \frac{1}{T}\int_o n(t)d(t) \qquad (3.3)$$

The noise-sampling voltage rıo(T) is a Gaussian random variable in contrast with n(t), which is a Gaussian random process.

The variance of no(T)

$$(Y_o^2 = \overline{n;(T)} = \frac{17T}{2\text{-}r2} \tag{3.4}$$

and, no(T) has a Gaussian probability density.

The output of the integrator, before the sampling switch, is vo(t) = so(t) + no(t). As shown in Fig.3.3.a, the signal output so(t) is a ramp, in each bit interval, of duration T. At the end of the interval the ramp attains the voltage so(T) which is +VT / ı or -VT / 1, depending on whether the bit is a 1 or a 0. At the end of each interval the switch SWı in Fig.3.2 closes momentarily to discharge the capacitor so that so(t) drops to zero. The noise no(t), shown in Fig.3.3.b, also starts each interval with rıo(O) = 0 and has the random value rıo(T) at the end of each interval. The sampling switch SW2 closes briefly just before the closing of SWı and hence reads the voltage

$$Vo(T) = So(T) + r_{1o}(T) \tag{3.5}$$

We would naturally like the output signal voltage to be as large as possible in comparison with the noise voltage. Hence a figure of merit of interest is the signal-to-noise ratio

$$\frac{[so(T)f}{[n_o(T)]_2} = \frac{3 V_2 T}{n,} \tag{3.6}$$

This result is calculated from Eqs 3.2 and 3.4. Note that the signal-to-noise ratio increases with increasing bit duration T and that it depends on V2T which is the normalized energy of the bit signal. Therefore, a bit represented by a narrow, high

amplitude signal and one by a wide, low amplitude signal are equally effective, provided V_2T is kept constant.

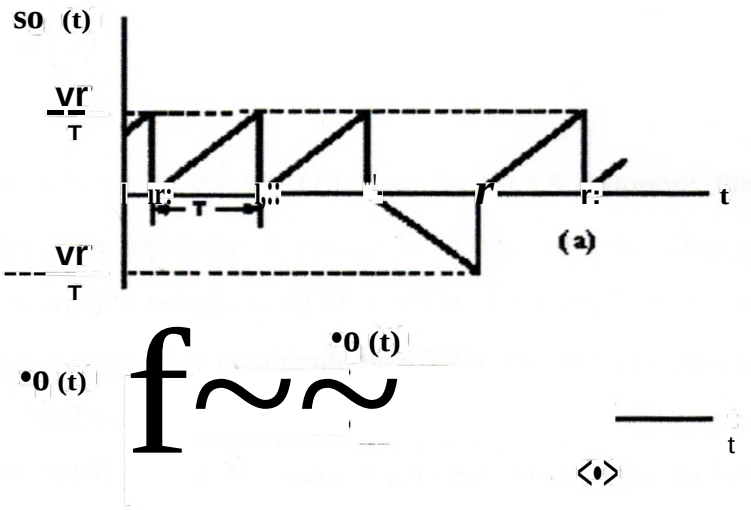


Figure 3.3 (a) The signal output and (b) the noise output of the integrator of Fig. 3.2 [Ref 17, page 444]

It is instructive to note that the integrator filters the signal and the noise such that the signal voltage increases linearly with time, while the standard deviation (rms value) of the noise increases more slowly, as $\sqrt{i}$. Thus, the integrator enhances the signal relative to the noise, and this enhancement increases with time as shown in Eq.3.6.

3.3 **PROBABILITY OF ERROR**

Since the function of a receiver of a data transmission is to distinguish the bit 1 from the bit 0 in the presence of noise, a most important characteristic is the probability that an error will be made in such a determination. We now calculate this error probability Pe for the integrate-and-dump receiver ofFig.3.2

We have seen that the probability density of the noise sample rio(T) is Gaussian and hence appears as in Fig.3. 1. The density is therefore given by

$$f[no(T)] = \frac{e^{-n_o^2(T)/2a_o^2}}{\sqrt{2\pi}\,\sigma_o} \tag{3.7}$$

where cr/, the variance, is $\sigma_o^2 = \overline{n_o^2(t)}$ given by Eq.3.4 . suppose, then, that during some bit interval the input-signal voltage is held at, say, -V. Then, at the sample time, the signal sample voltage is $s_o(T) = -VT/t$; while the noise sample is rio(T). If $n_o(T)$ is positive and larger in magnitude than VT/'t, the total sample voltage $v_o(T) = s_o(T) + r_{io}(T)$ will be positive. Such a positive sample voltage will result in an error, since as noted earlier, we have instructed the receiver to interpret such a positive sample voltage to mean that the signal voltage was +V during the bit interval. The probability of such a misinterpretation, that is,the probability that no(T) > VT/'t, is given by the area of the shaded region in Fig.3.4. The probability of error is, using Eq.3.7.

$$p_e = \int_{VJ'1-r}^{\infty} f[no(D\}ino(T) - \int_{vr\,tt}^{\infty} \frac{e^{-n_o^2(T)/2\sigma_o^2}}{\sqrt{2\pi CT2}_o}\,dn; (T) \tag{3.8}$$

Defining $x'''' \equiv no(T)/\sqrt{2}a_o$, and using Eq.3.4, Eq.3.8 may be rewritten as

$$P_e = \frac{1}{2}\int_{x=V,lT/170}^{\infty} e^{-x^2}\,dx$$

$$= \frac{1}{2}erfc\left(V\sqrt{\frac{T}{n}}\right) = \frac{1}{2}erfc\left(\frac{V^2T}{n}\right)^{1/2} = \frac{1}{2}erfc\left(\frac{E_s}{n}\right)^{1/2} \tag{3.9}$$

in which Es = V^2T is the signal energy of a bit.

If the signal voltage were held instead at +V during some bit interval, then it is clear from the symmetry of the situation that the probability of error would again be given by Pe in Eq.3.9. Hence Eq.3.9 gives Pe quite generally.

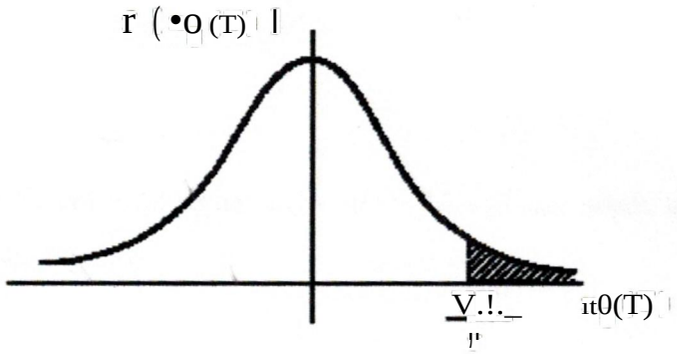


Figure 3.4 The Gaussian probability density of the noise sample n(T)
[Ref I7, page 445]

The probability of error Pe, as given by in Eq.3.9, is plotted in Fig.3.5. Note that the Pe decreases rapidly as Es/11 increases. The maximum value of Pe is $\frac{1}{2}$. Thus, even if the signal is entirely lost in the noise so that any determination of the receiver is a sheer guess, the receiver cannot be wrong more than half the time on the average.

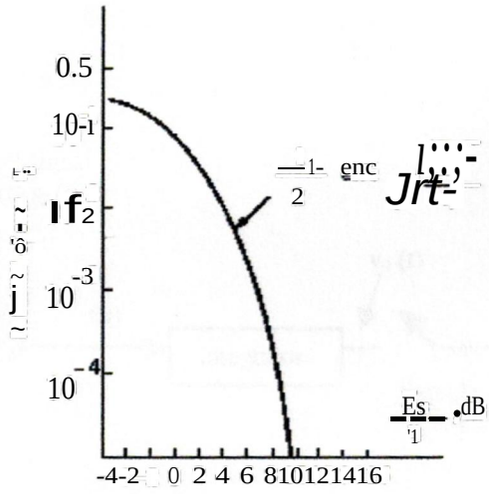


Figure 3.5 Variation of Pe versus Es/11 [Ref I7, page 446]

3.4 ERROR PROBABILITY OF THE PSK TRANSMISSION

Here the input signal is

$$S_1(t) = A \cos \text{root} \tag{3.10}$$

$$S2(t) = -A \cos C0_0 t \tag{3.11}$$

At the receiver a coherent local signal $s_1(t)-s2(t) = 2A \cos C0_0 t$ needs to be provided for the multiplier (see Fig.3.6)

Since, in PSK, $s_1(t) = -s_2(t)$. then, in PSK, as in baseband transmission.

$$P_e = \frac{1}{2} \text{euc} \sim \frac{s}{2r_1} \tag{3.12}$$

If a bit duration extends for a time T, which encompasses a whole number of cycles, then the signal energy is $E_s = A^2T / 2$ so that from Eq.3.12 the error probability is

$$P_, = \sim erfc \sim \frac{A'T}{2r_,} \tag{3.13}$$

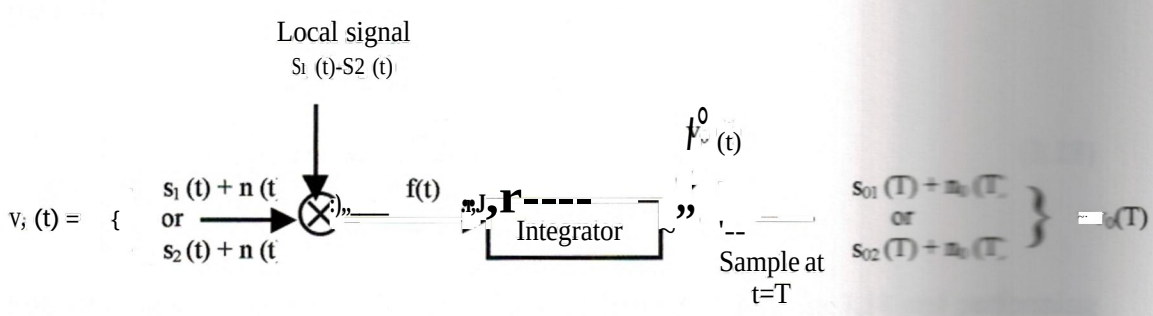


Figure 3.6 A coherent system of signal reception [Ref 17, page 454]

3.5 ERROR PROBABILITY OF THE FSK TRANSMISSION

In frequency-shift keying (FSK) the received signal is either

$$s_1(t) = A \cos(\omega_0 + \Omega)t \qquad (3.14)$$

or

$$s_2(t) = A \cos(\omega_0 - \Omega)t \qquad (3.15)$$

One way of synthesizing the matched filter is to construct the correlation receiver system shown in Fig.3.6. This receiver will give precisely the same performance as a matched filter, provided that the local waveform is $s_1(t) - s_2(t)$. In FSK the required local waveform is

$$s_1(t) - s_2(t) = A \cos(\omega_0 + \Omega)t - A \cos(\omega_0 - \Omega)t \qquad (3.16)$$

The probability of error for the matched filter

$$p_e = \frac{1}{2} erfc \left(\sqrt{\cdots} \right) \qquad (3.17)$$

The derivation was general, and would apply in the present case, except for the fact that we had assumed there that $s_1(t) = - s_2(t)$. This assumption is obviously not valid for FSK.

$$\left[\frac{p^2(T)}{\sigma_o^2}\right]_{max} = \sim \int_0 [s_1(t) - s_2(t)]^2 \, d(t) \qquad (3.18)$$

Substituting $s_1(t)$ and $s_2(t)$ as given in Eqs 3.14 and 3.15 into Eq.3.18 and performing the indicated integration, we find that

$$\left[\frac{p;(T)]}{er;}\right]_{max} = \frac{2A_2T}{n}\left[1 - \frac{sin2QT}{2QT} + \frac{1}{2}\frac{sin[2(w_0 + Q)T]}{2(w_0 + O)T}\right.$$

$$\left. - \frac{1}{2}\frac{sin[2(w_0 - Q)T]}{2(w_0 - O)T} - \frac{\sin 2w_oT}{2w_oT}\right] \quad (3.19)$$

If we assume that the offset angular frequency Ω is very small in comparison with the carrier angular frequency $r0_0$ (a situation usually encountered in physical systems), then the last three terms in Eq.3.19 each have the form $(\sin 2r_{oo}T)/2r_{o}T$. This ratio approaches zero as $r0_0T$ increases. We further assume, as is generally the case, that $r0_0T >> 1$. We may therefore neglect these last three terms. We are left with

$$\left[\frac{p;(T)]}{cr_0^2}\right]_{max} = \frac{2A_2T}{n}\left(1 - \frac{\sin 20T)}{zar}\right) \quad (3.20)$$

The quantity $[p/(T)/o\}]max$ in Eq.3.20 attains its largest value when Ω is selected so that $20T = 3n/2$. For this value of Ω we find

$$\left[\frac{p;e;)J}{(Jo}\right]_{max} = 2.42\,\frac{A_IT}{n:} = 4.84\,\frac{(Az/2)T}{T/o} \quad (3.21)$$

The probability of error, calculated using

$$p_e = \frac{1}{2}\,erfc\left[\frac{po(T)}{2\sim 2cro}\right] = \frac{1}{2}\,erfc\left[\frac{po_2(T)}{8cr_{20}}\right]^{III} \quad (3.22)$$

with $[p/(T)lcr/]max$ as given in Eq.3.21, is found to be

$$Pe=\frac{1}{2}\operatorname{erfc}\left\{\frac{1}{8}\left[\frac{P!(T)}{a_0}\right]_{max}\right\}^{1/2}=\frac{1}{2}\operatorname{erfc}(0.6\text{-}J_{211}E.)^{1/2} \quad (3.23)$$

where the signal energy is Es= A2T/2.

Comparing the probability of error obtained for FSK (Eq.3.23) with the probability of error obtained for PSK (Eq.3.12), we see that equal probability of error in each system can be achieved if the signal energy in the PSK signal is 0.6 times as large as the signal energy in FSK. As a result, a 2-dB increase in the transmitted signal power is required for FSK. Why is FSK inferior to PSK? The answer is that in PSK sı(t) = - s2(t), while in FSK this condition is not satisfied. Thus, although an optimum filter is used in each case, PSK results in considerable improvement compared with FSK.

When one of two orthogonal frequencies are transmitted, 2QT = rnn (man integer)

$$Pe=\frac{1}{2}erfc\left(\frac{E_b}{2}\right)^{1/2} \quad (3.24)$$

Since FSK can be thought of as the transmission of the output of either of two signal sources, the first at the frequency ro1 = roo + n, and the second at the frequency ro2 = roo - n, we should think that a reasonable detection system would consist of two bandpass filters, with center frequencies ro1 and ro2. The bandwidth of each filter would be adjusted to yield a maximum output when the appropriate signal is received. Thus, when filter Hı with center frequency ro1 has a larger output than filter H2 with center frequency ro2 , we would decide that sı(t) was transmitted. Similarly we would decide that s2(t) was transmitted when the output of H2 was greater than the output of H1.

When using a filter receiver, we make no use of the phase of the incoming signal. Such reception is, therefore, called non-coherent detection. The coherent matched-

filter detector, on the other hand, uses synchronization techniques to determine the phase of incoming signal. Since some valuable information concerning the signal is not used, the probability of detecting the signal is reduced. The probability of error of non-coherent FSK is found to be

$$p_e = \frac{1}{2} e^{-E/2N_0} \qquad (3.25)$$

3.6 **DIFFERENTIAL PSK**

The operation of differential phase-shift keying (DPSK) was explained before. We shall now show the suboptimum nature of DPSK by considering the system in terms of the phasor diagram shown in Fig. 3.7. In Fig.3.7.a. we see that when no noise is present the received phase is either at angle 0 or 7t. From this we draw a decision boundary at angle *n/2* and decide that a 1 was sent if the phase difference between two consecutive bits differs by more than *n/2*.

(a)

Phasor for 0 when no noise is present

Phasor for 1 when no noise is present

(b)

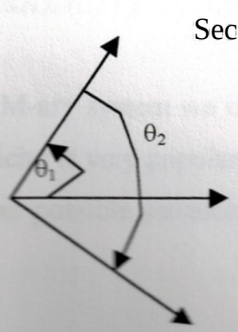


Figure 3.7 Reception of DPSK. (a) Phasors when no noise is present. (b) Phasors when noise is present [Ref 17, page 460]

Fig.3.7.b. shows three consecutive received bits. Each bit was transmitted as a 1, but because of noise each is perturbed from the horizontal axis as shown. The DPSK receiver compares bit 2 with bit 1, reads an angle 0₁ which is less than 90°, and decides that bit 2 is a 1. The DPSK receiver then compares bit 3 with bit 2, reads an angle 02 which is greater than 90°, and decides that a 0 was transmitted.

The error was due to the fact that the DPSK receiver uses only the previous bit as a reference. This method of operation is analogous to employing poor synchronization. If all the previous positive bits were somehow averaged by employing good synchronization, and this average were used as a reference, Then the DPSK receiver would have a stable reference, and the error described above would not have occurred. As a matter of fact we would than have a PSK system, not a DPSK system. Thus, DPSK is suboptimum and results in a higher probability of error than in PSK where we have a stable reference phase (when perfect synchronization is assumed).
The calculation of probability of error is complicated and will not be given here. The result is

$$Pe = \frac{1}{2} e^{-EI_s \; 770} \tag{3.26}$$

3.7 **ERROR PROBABILITY OF QPSK**

As an example of M-ary system we consider 4-phase PSK (QPSK), which, because of it relative simplicity is very popular.
In QPSK one of four possible waveforms is transmitted during each interval T. These waveforms are

$$s;(t) = A\cos\{\text{moi}+[2m-1]:) \qquad m = 1,2,3,4 \qquad 0 \text{ st } sTs = 2T \tag{3.27}$$

These four waveforms are represented in the phasor diagram of Fig.3.8. The receiver system is shown in Fig.3.9. Observe that two correlators are required and that the local reference waveforms, as indicated also in Fig.3.8, are Acosro.t and Asinoı.t, Suppose, now, that, in the absence of the noise, signal sı(t) is received. Let us use the symbol Vo to represent the corresponding output of correlator 1, i.e., V₀ = Voı(Ts) when sı(t) is received.

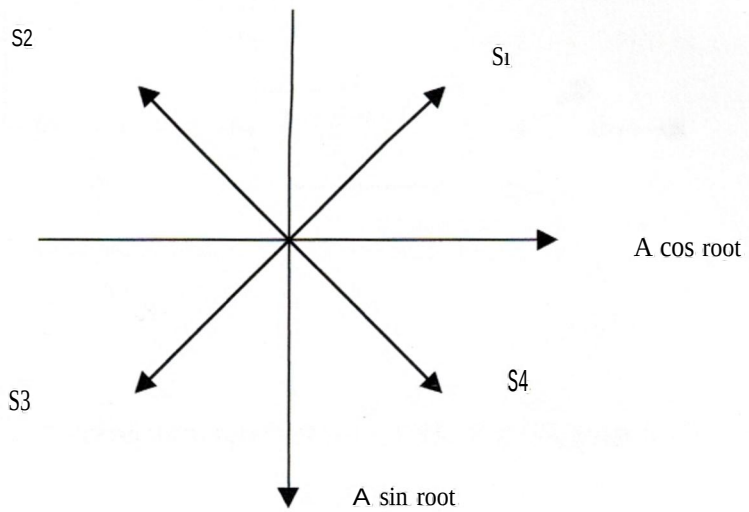


Figure 3.8 A phasor diagram representation of the signals in QPSK
[Ref 17, page 461]

Thus the transmitted signal may be recognised from a determination of the outputs of both correlators. In the presence of noise, of course, there will be some probability that an error will be made by one or both correlators.

We note from Fig. 3.8, that the reference waveform of correlator 1 is at an angle rjJ = 45° to the axes of orientation of all of the four possible signals. Since (cos45°)2= Yı, the probability that correlator I or correlator 2 will make an error is

$$P_{;,} = P_{;,} = \frac{1}{2} e_{,}fc\sim\sqrt{\frac{A^{2}T_{,}}{4r_{ı}}} = \frac{1}{2} e_{ı}fc_{,}\sqrt{\frac{Jif;}{77}} = P_{,}(BPSK) \qquad (3.29)$$

Thus the bit probability of error of QPSK and BPSK is the same.

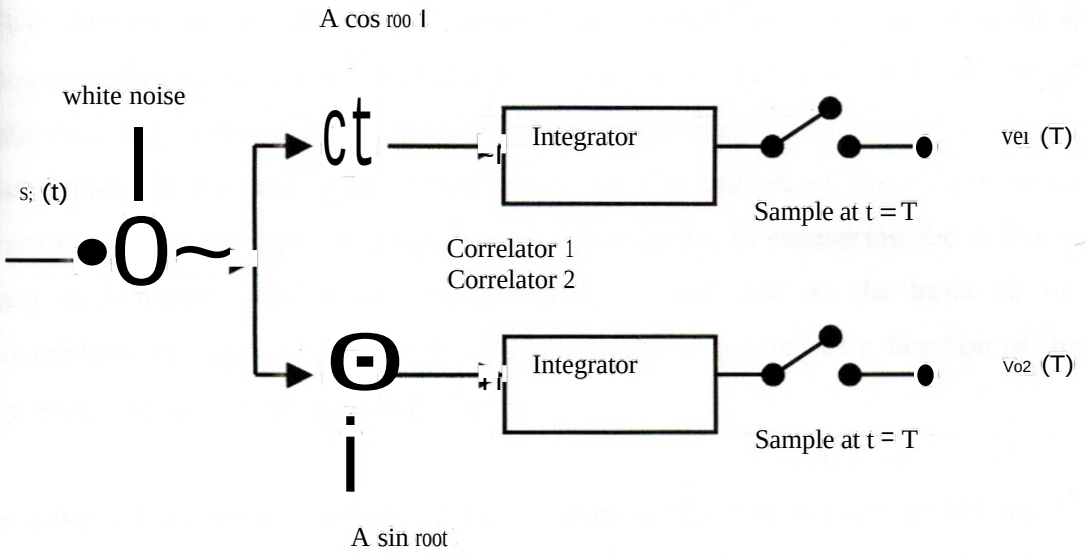


Figure 3.9 A correlation receiver for QPSK [Ref 17, page 462]

The probability $P_{;2}$ that correlator 2 will make an error is similarly given by the expression in Eq.3.28. The probability Pc that the QPSK receiver will correctly identify the transmitted signal is equal to the product of the probabilities that both correlator 1 and correlator 2 have yielded correct results. Thus using $P_e' = P_{el} = P_{e2}$

$$P_{c-} = (1 - P_e')(1 - P_e') = 1 - 2P_e' + P_e'^2 \qquad (3.30)$$

If, as is normally the case P'e<<l, the last term in Eq.3.30 may be neglected. Finally, then, the probability of error of the system is

$$P_e(QPSK) = 1 - P_c = 2P_; = erfc\left(\frac{\cdot}{1}\right) \qquad (3.31)$$

3.8 COMPARISON MODULATION TECHNIQUES

Two systems having an unequal number of symbols may be compared in a meaningful way only if they use the same amount of energy to transmit each bit of information. It is the total amount of energy needed to transmit the complete message that represents the cost of the transmission, not the amount of energy needed to transmit a particular symbol satisfactorily. Accordingly, in comparing the different data transmission systems considered before, we will use, as the basis of our comparison, the average probability of symbol error expressed as a function of the bit energy-to-noise-density ratio E_1/N_0.

In table 3.1 we have summarized the expressions for the average probability of symbol error Pe for the coherent PSK, conventional coherent FSK with one-bit decoding, DPSK, non coherent FSK, QPSK, and MSK, when operating over an AWGN channel. In Fig.3.10 we have used these expressions to plot Pe as a function of E_1/N_0. Based on the performance curves shown in Fig.3.10, the summary of formulas given in Table 3.1, and the defining equations for the pertinent modulation formats, we can make the following statements.

	Error probability, Pe
Coherent binary signalling	1/2 erfc(JEb!No)
a) Coherent PSK	erfc(JEb/No)-l/2erfc2(JEb/No)
b) Coherent detection of different encoded PSK	l/2erfc(JEb/No)
c) Coherent FSK	
Non-coherent binary signalling	
a) DPSK	1/2 exp(-E1/No)
b) Non-coherent FSK	1/2 exp(-EJ2No)
Coherent quadrature signalling	
a)QPSK	erfc(JEb/N 0)-1/4 erfc2 <JEb/N 0)
b)MSK	

Table 3. I Symbol Error Probability for Different Data Transmission System

[Ref 6, page 311]

1. The error rates for all the systems decrease monotonically with increasing values ofE_1/N_o.

2. For any value of E_1/N_0, coherent PSK produces a smaller error rate than any of the other systems. Indeed, it may be shown that in the case of systems restricted to one-bit decoding, perturbed by additive white Gaussian noise, coherent PSK system is the optimum system for transmitting binary data in the sense that it achieves the minimum probability of symbol error for a given value of E_1/N_0.

3. Coherent PSK and DPSK require an E_1/N_0 that is 3 dB less than the corresponding values for conventional coherent FSK and non-coherent FSK, respectively, to realise the same error rate.

4. At high values of E_1/N_0, DPSK and non-coherent FSK perform almost as well (to within about 1 dB) as coherent PSK and conventional coherent FSK, respectively, for the same bit rate and signal energy per bit.

5. In QPSK two orthogonal carriers $\sqrt{2/T}\cos(m_0t)$ and $\sqrt{2/T}\sin(m_0t)$ are used, where the carrier frequency f_c is an integral multiple of the symbol rate 1/T, with the result that two independent bit streams can be transmitted and subsequently detected in the receiver. At high values of E_1/N_0, coherently detected binary PSK and QPSK have about the same error rate performance for the same value of E_1/N_o.

6. In MSK the two orthogonal carriers $\sqrt{2/T_b}\cos(m_0t)$ and $\sqrt{2/T_b}\sin(m_0t)$ are modulated by the two antipodal symbol shaping pulses $\cos(7rt/2\ T_b)$ and $\sin(nt/2\ T_b)$, respectively, over $2T_b$ intervals, where T_b is the bit duration. Correspondingly, the receiver uses a coherent phase decoding process over two successive bit intervals to recover the original bit stream. We thus find that MSK has exactly the same error rate performance as QPSK.

7. MSK scheme differs from the other signalling schemes in that its receiver has memory. In particular, MSK receiver makes decisions based on observations over two successive bit intervals. Thus, although the transmitted signal has a binary format represented by the transmission of two distinct frequencies, the presence of memory in the receiver makes it assume a from that has in-phase and quadrature paths as in QPSK.

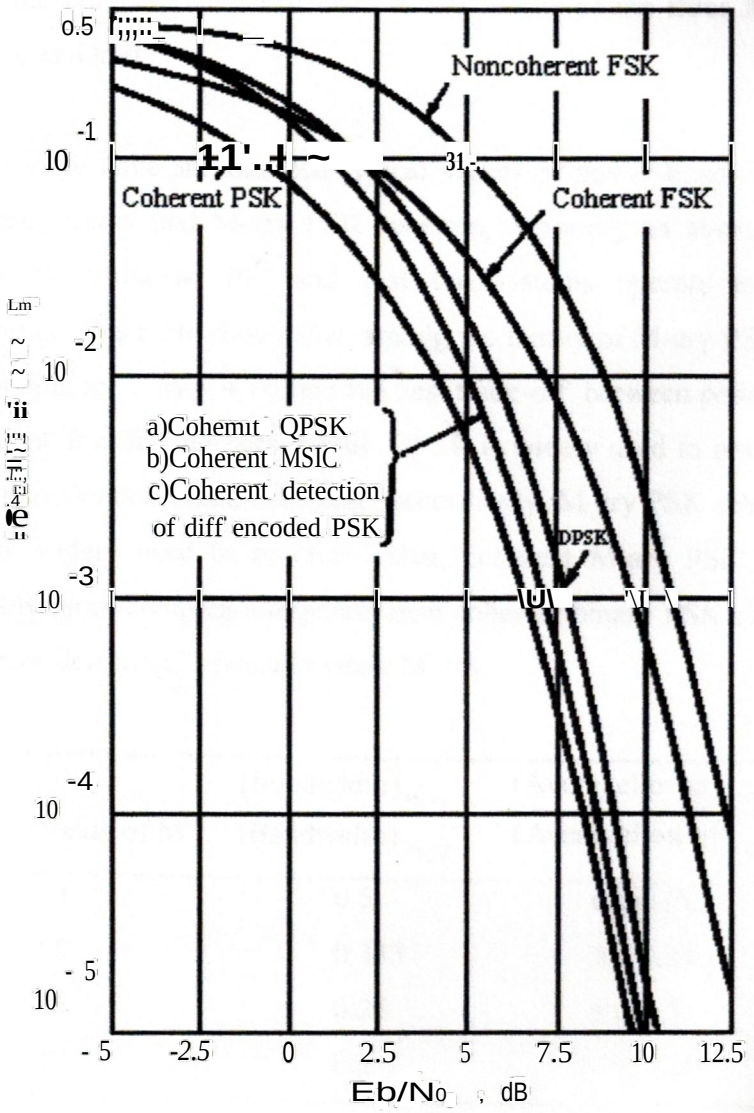


Figure 3.10 Comparison of the noise performances of different PSK and FSK schemes [Ref 6, page 312]

CHAPTER4 COMPARISON PARAMETERS OF THE DIGITAL MODULATION TECHNIQUES

4.1 POWER-BANDWIDTH REQUIREMENTS

We conclude this section on M-ary digital modulation techniques by presenting some notes on the comparative performances and merits of the three M-ary modulation schemes considered.

In table 4.1 we have summarized typical values of power-bandwidth requirements for coherent binary and M-ary PSK schemes, assuming an average probability of symbol error equal to 10^{-4} and that the systems operate in identical noise environments. This table shows that, among the family ofM-ary PSK signals, QPSK (corresponding to $M = 4$) offers the best trade-off between power and bandwidth requirements. It is for this reason that QPSK is widely used in practice. For $M > 8$, power requirements become excessive; accordingly, M-ary PSK schemes with $M > 8$ are not as widely used in practice. Also, coherent M-ary PSK schemes require considerably more complex equipment than coherent binary PSK schemes for signal generation or detection, especially when $M > 8$.

Value ofM	$\frac{(\text{Bandwidth})_{M\text{-ary}}}{(\text{Bandwidth})_{\text{Binary}}}$	$\frac{(\text{AveragePower})_{M\text{-ary}}}{(\text{AveragePower})_{\text{Binary}}}$
4	0.5	0.34 dB
8	0.333	3.91 dB
16	0.25	8.52 dB
32	0.2	13.52 dB

Table 4.1 Comparison of Power-Bandwidth Requirements for M-ary PSK with Binary PSK. Probability of Symbol Error= 10^{-4}. [Ref 6, page 324]

Basically, M-ary PSK and M-ary QAM have similar spectral and bandwidth characteristics. For M > 4, however, the two schemes have different signal constellations. For M-ary PSK the signal constellation is circular, whereas for M-ary QAM it is rectangular. Moreover, a comparison of these two constellations reveals that the distance between the message points of M-ary PSK is smaller than the distance between the message points of M-ary QAM, for a fixed peak transmitted power. This basic difference between the two schemes is illustrated in Fig.4.1 for M = 16. Accordingly, in an AWGN channel, M-ary QAM outperforms the corresponding M-ary PSK in error performance for M > 4. However, the superior performance of M-ary QAM can be realized only if the channel is free from non-linearities.

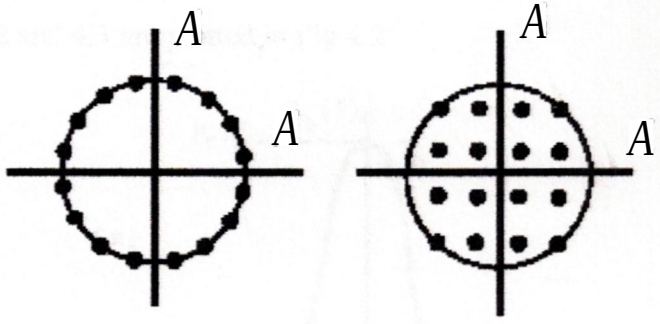


Figure 4.1 Signal constellations (a) M-ary QPSK, and (b) M-ary QAM for M=l6 [Ref 6, page 325]

4.2 SPECTRAL ANALYSIS OF DIGITAL MODULATION TECHNIQUES

4.2.1 SPECTRUM OF BPSK

The waveform b(t) is a NRZ (non-return-to-zero) binary waveform whose power spectral density is given in Eq. 4.1 for a waveform which makes excursions between $+\sqrt{P}$ and $-\sqrt{P}$.

$$\overline{|P(f)|^2} = \frac{1}{T}\{|P_1(f)|^2 + |P_2(f)|^2 + \ldots\ldots\ldots\ldots + |P_n(f)|^2\} \quad (4.1)$$

We have;

$$G(f) = P_s T_b \left(\frac{\sin \pi f T_b}{\pi f T_b}\right)^2 \quad (4.2)$$

The BPSK waveform is the NRZ waveform multiplied carrier $A\cos\omega_0 t$. The power spectral density of the BPSK signal is

$$G_{BPSK}(f) = \frac{P_s T_b}{2}\left\{\left[\frac{\sin \pi (f - f_0) T_b}{\pi (f - f_0) T_b}\right]^2 + \left[\frac{\sin \pi (f + f_0) T_b}{\pi (f + f_0) T_b}\right]^2\right\} \quad (4.3)$$

Equations 4.2 and 4.3 are plotted in Fig.4.2

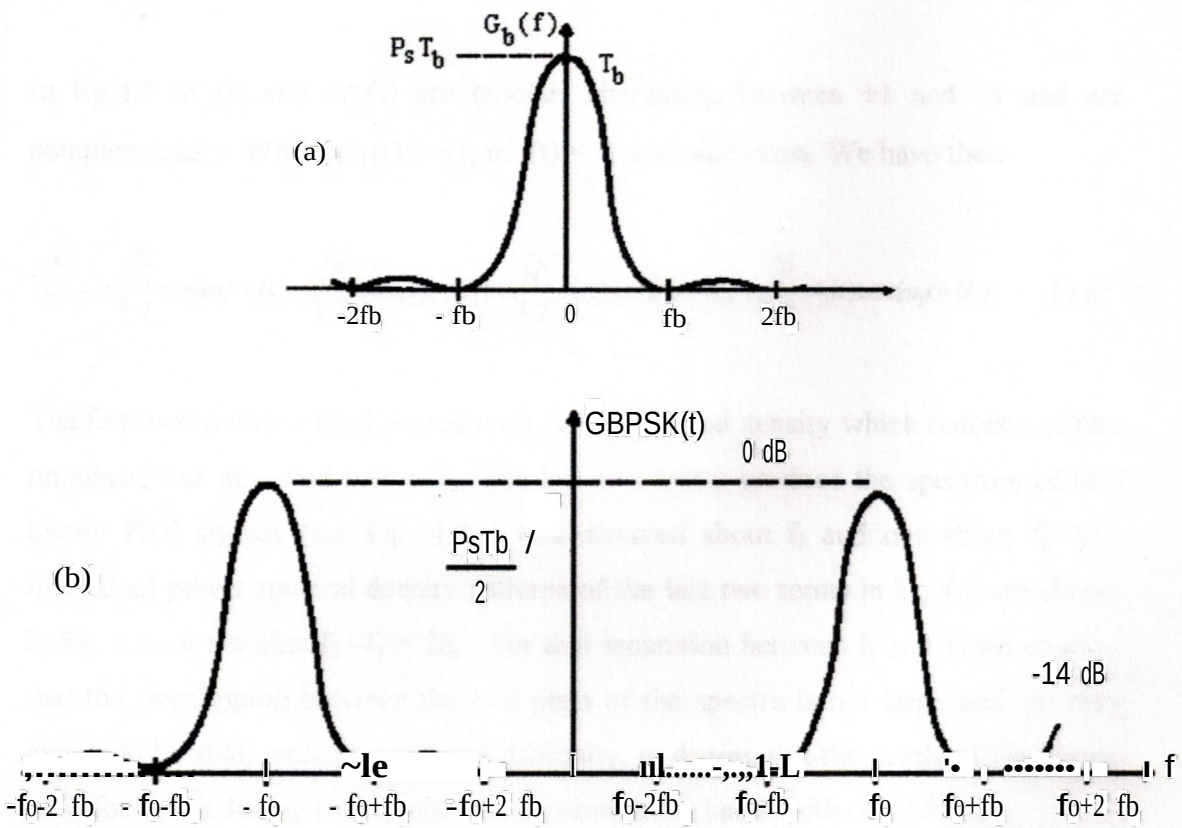


Figure 4.2 (a) Power spectral density ofNRZ data b(t). (b) Power spectral density of binary PSK [Ref 17, page 254]

In terms of the variables m(t) and m(t)the BFSK signal is

$$v_{BFSK} = \overline{J2Psm(t)}\cos(OJ_1t + B_1) + \overline{J2Psm(t)}\cos(OJ_2t + B_2) \quad (4.4)$$

where we have assumed that each of the two signals are of independent and random, uniformly distributed phase. Each of the terms in Eq.4.4 looks like the signal $Jii;b(1)coso_{1o}$ which we have encountered in BPSK. In the BPSK case, b(t) is bipolar, i.e., it alternates between +1 and -1 while in the present case m(t) and $ni(t)$ are unipolar, alternating between +1 and 0. We may, however, rewrite m(t) and $ni(t)$ as the sums of a constant and a bipolar variable, that is

$$m(t) = 0.5 + 0.5\, m'_1(t) \quad (4.5.a)$$

$$m(t) = 0.5 + 0.5\, m'_2(t) \quad (4.5.b)$$

In Eq.4.5 $m'_1(t)$ and $m'_2(t)$ are bipolar, alternating between +l and -1 and are complementary. When $m'_1(t) = +I$, $m'_2(t) = -1$ and vice versa. We have then

$$v_{BFSK} = \sqrt{if}\cos(\omega_1 t + B_1) + \sqrt{if}\cos(\omega_2 t + B_2) + \sqrt{if}\, m'_1(t)\cos(\omega_1 t + B_1) + \sqrt{if}\, m'_2(t)\cos(\omega_2 t + B_2) \quad (4.6)$$

The first two terms in Eq.4.6 produce a power spectral density which consists of two impulses, one at f_1 and one at f_2. The last two terms produce the spectrum of two binary PSK signals (see Fig. 4.2.a) one centered about f_1 and one about f_2. The individual power spectral density patterns of the last two terms in Eq.4.6 are shown in Fig.4.3 for the case $f_2 - f_1 = 2f_b$. For this separation between f_1 and f_2 we observe that the overlapping between the two parts of the spectra is not large and we may expect to be able, without excessive difficulty, to distinguish the levels of the binary waveform d(t). In any event, with this separation the bandwidth ofBFSK is

$$BW\ (BFSK) = 4f_b \quad (4.7)$$

Which is twice the bandwidth of BPSK.

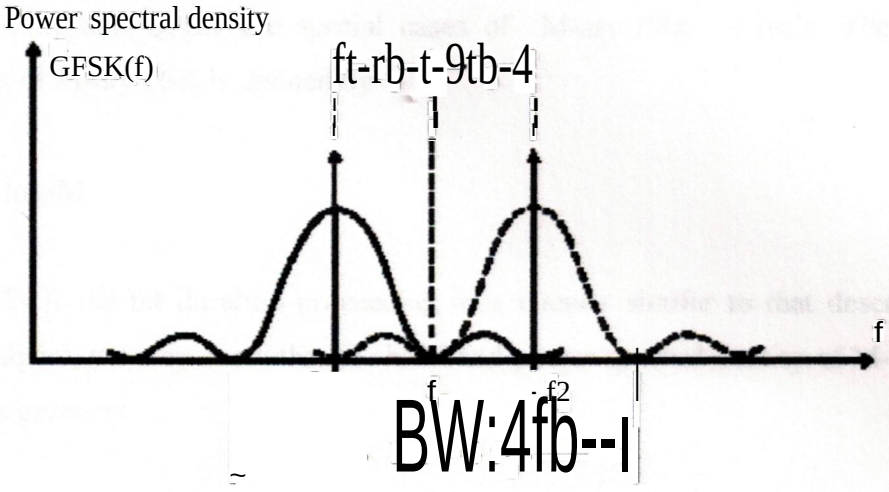


Figure 4.3 The power spectral densities of the individual terms in Eq.4.6 [Ref 17, page 278]

4.2.2 BANDWIDTH OF A QPSK SIGNAL

The power spectral density and bandwidth of a QPSK signal can be calculated by the procedure applied in the case ofM-ary PSK and is given

$$G_{QPSK}(f) = \frac{P_s T_s}{2}\left[\frac{\sin \pi(f - f_0)T_s}{\pi(f - f_0)T_s}\right]^2 + \frac{P_s T_s}{2}\left[\frac{\sin \pi(f + f_0)T_s}{\pi(f + f_0)T_s}\right]^2 \quad (4.8)$$

where Ts= NTb. The bandwidth of the QPSK signal is

$$B = 2f_1/N \quad (4.9)$$

which is the same as in the case of M-ary PSK. For the present case of QPSK with N = 4 corresponding to 16 possible distinguishable signals we have $B_{QPSK(16)} = f_1/2$ which is one-fourth of the bandwidth required for binary PSK.

4.2.3 POWER SPECTRAL DENSITY OF M-ARY PSK

Binary PSK and QPSK are special cases of M-ary PSK signals. The symbol duration ofM-ary PSK is defined by

$$Ts = Tb \log 2M \tag{4.10}$$

Where Tb is the bit duration proceeding in a manner similar to that described for QPSK signal, we may show that the baseband power spectral density of M-ary PSK signal is given by

$$GM(f) = p_s.\text{isinef}\left[\frac{\quad}{rifTs}\right]^2 \tag{4.11}$$

bandwidth of M-ary PSK

$$B = 2/Ts = 2\ fin \tag{4.12}$$

where n = log$_2$M,

We thus note that as we increase the number of bits n per symbol, the bandwidth becomes progressively smaller. On the other hand distance between symbol signal points becomes smaller and the probability of error becomes higher.

4.3 BANDWIDIB EFFICIENCY

The primary objective of spectrally efficient modulation is to maximize the bandwidth efficiency, defined as the ratio of data rate to channel bandwidth; it is measured in units of bits per second per hertz.

With the data rate denoted by R_b, and the channel bandwidth by B, we may express the bandwidth efficiency, p, as

$$P = \frac{Rb}{B} \quad \text{bits/s/Hz} \tag{4.13}$$

The data rate R_b is well defined. Unfortunately, however, there is no universally satisfying definition for the bandwidth B. This means that the bandwidth efficiency of a digital modulation scheme depends on the particular definition adopted for the bandwidth of the modulated signal. In the sequel, we consider the evaluation of the bandwidth efficiency of M-ary PSK signals, followed by that of M-ary FSK signals.

The power spectra of M-ary PSK signals possess a main lobe bounded by well defined spectral nulls (i.e., frequencies at which the power spectral density is zero). Accordingly, the spectral width of the main lobe provides a simple and popular measure for the bandwidth of M-ary PSK signals. This definition is referred to as the null-to- null bandwidth. With the null-to-null bandwidth encompassing the main lobe of the power spectrum of an M-ary signal, we find that it contains most of the signal power

The channel bandwidth required to pass M-ary PSK signals (more precisely, the main spectral lobe ofM-ary PSK signals) is given by

$$B = \frac{2}{T} \tag{4.14}$$

where T is the symbol duration. But the symbol duration T is related to the bit duration Tb. Hence, we may redefine the channel bandwidth of Eq.4.14 in terms of the bit rate R_b, as

$$B = \frac{2Rb}{\log 2M} \tag{4.15}$$

Equivalently, we may express the bandwidth efficiency of M-ary PSK signal as

$$p=-b\frac{R}{B}$$
$$=\frac{\log 2M}{2} \qquad (4.16)$$

Table 4.2 gives the values of p calculated from Eq.4.16 for varying M.

M	2	4	8	16	32	64
p (bits/s/Hz)	0.5	I	1.5	2	2.5	3

Table 4.2 Bandwidth efficiency ofM-ary PSK signals [Ref 6, page 333]

4.4 M-ARY MODULATION FORMATS VIEWED IN THE LIGHT OF CHANNEL CAPACITY THEOREM

It is informative to compare the bandwidth power exchange capabilities of M-ary PSK and M-ary FSK signals in the light of Shannon's *channel capacity theorem.* The yardstick for this comparison is provided by the ideal system for error-free transmission. By the ideal system, we mean one that follows the channel capacity theorem

$$C = B\log_2\left(1+\frac{Eb}{N0}\right) \qquad (4.17)$$

where Bis the bandwidth.

Consider first a coherent M-ary PSK system. Each signal in the set represents a K-bit word, where K=log2 M. Using the definition of null-to-null bandwidth, we may

express the bandwidth efficiency ofM-ary PSK as in Eq.4.16, which is reproduced here for convenience:

$$\frac{Rb}{B} = \frac{\log_2 M}{2} \qquad (4.18)$$

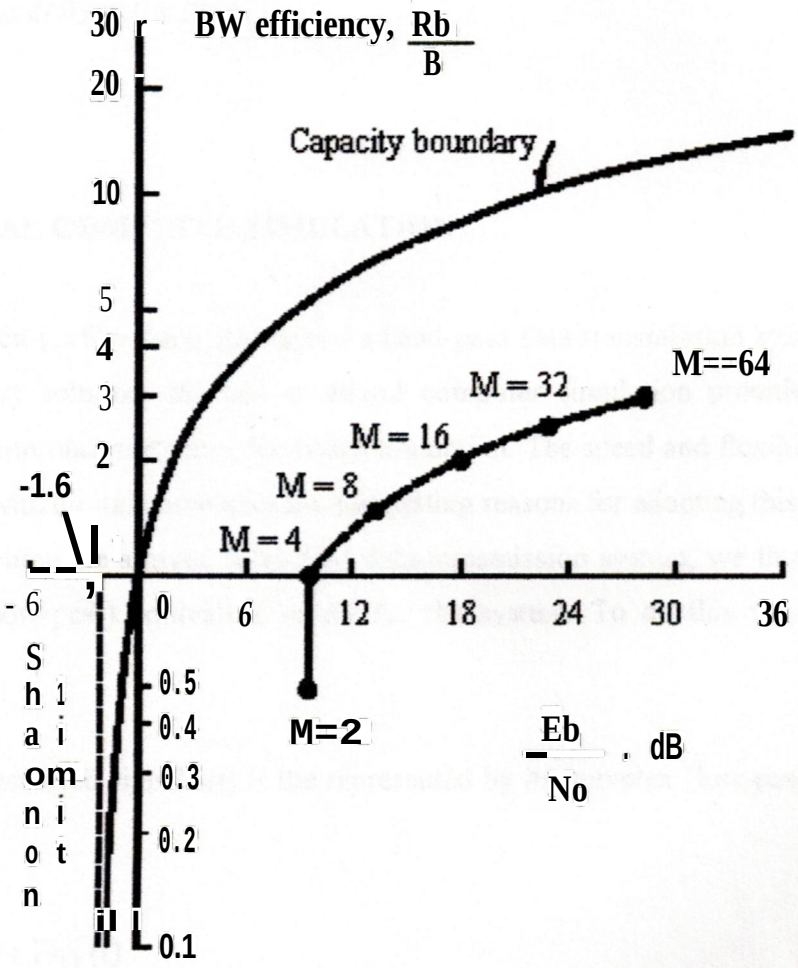


Figure 4.4 Comparison of M-ary PSK with the ideal system [Ref 6, page 335]

In Fig.4.4, we show the operating points for different numbers of phase levels M=2\ where k= 1, 2, 3, 4, 5, 6. Each point corresponds to an average probability of symbol error Pe = 10·5. In the figure we have also included the capacity curve for the ideal system. We observe from Fig.4.4 that as Mis increased, the bandwidth efficiency is improved, but the value of E1/ No. Required for error-free transmission moves away

ım the Shannon limit. This behaviour of M-ary PSK is also displayed by the curves own in the error rate diagram ofFig.4.5.

~ clearly see that as M is increased, the system approaches the Shannon limit. ,wever, the price paid for this performance is a large channel bandwidth that >roaches infinity in the limit.

DIGITAL COMPUTER SIMULATION

en explicit performance analysis of a band-pass data transmission system defines ıtisfactory solution, the use of digital computer simulation provides the only mative approach the actual hardware evaluation. The speed and flexibility usually ciated with digital computers are compelling reasons for adopting this approach. rder to simulate a given band-pass data-transmission system, we first develop a band (low-pass) equivalent model for the system. To do this we proceed as -ws:

to s(t) the

Ihe transmitted signal s(t) is the represented by its complex (low-pass) envelope $r(t)$.

$= s_1(t) + j\, s_Q(t)$

t $w_Q(t)$ are
ssian noise
2 watts per

e $s_ı(t)$ and $S_Q(t)$ are the in-phase and quadrature components of the transmitted l s(t), respectively. The characteristics of the input data waveform and the ular signalling method used to transmit the data are completely contained in the iption of the complex envelope $S(t)$. Furthermore , by using the complev ope $s(t)$, we eliminate the need for simulating the high-frequency carrier onent.

nd any band

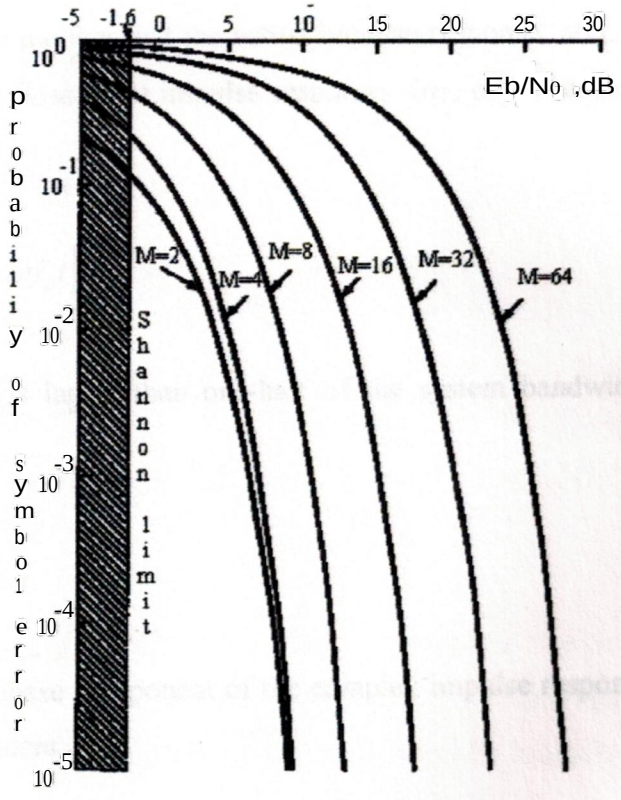


Figure 4.5 Error-rate curves for M-ary PSK [Ref 6, page 336]

2. To simulate the effect of noise at the front end of the receiver, we add to s(t) the complex envelope

$$w(t)=W_I(t)+jwQ(t)$$

where the in-phase component $w_I(t)$ and the quadrature component $w_0(t)$ are modelled as sample functions of independent, zero-mean, white Gaussian noise processes, and with each one having a power spectral density of $N_0/2$ watts per hertz. Thus the received signal is represented by the complex envelope

$$x(t) = s(t)+w(t)$$
$$= [s_I(t)+w_I(t)]+ J[sQ(t)+wQ(t)]$$

3. Correspondingly, the matched filter (or correlation) receiver and any band limiting

filter in the system are replaced by their respective complex equivalent low-pass versions. Here, we use the fact that the actual impulse response, h(t), of a band-pass filter and the complex (loss-pass) impulse response, $h(t)$, of its baseband equivalent are related by

$$h(t) = 2\mathrm{Re}[h(t)\exp(j2\pi f_c t)]$$

It is assumed that f_c is larger than one-half of the system bandwidth. Let $h(t)$ be expressed in the form

$$\tilde{h}(t) = h_I(t) + jh_Q(t)$$

where $h_I(t)$ is the in-phase component of the complex impulse response, and $h_Q(t)$ is the quadrature component.

4. The complex envelope of the band-pass system's output $y(t)$ is computed by convolving $x(t)$ with $\tilde{h}(t)$, as shown by

$$y(t) = \tilde{h}(t) * x(t)$$

where $*$ denotes convolution. Expressing $y(t)$ in terms of its in-phase component $y_I(t)$, we may also write

$$y_I(t) = h_I(t) * x_I(t) - h_Q(t) * x_Q(t) \quad (4.19)$$

and

$$y_Q(t) = h_Q(t) * x_I(t) + h_I(t) * x_Q(t) \quad (4.20)$$

The block diagram ofFig.4.6 depicts the relationships described in Eqs.4. 19 and 4.20 between the in-phase and quadrature components of the input and output signals of the system.

When the block diagram of Fig.4.6 is simulated on a digital computer, the various time functions are naturally represented in their sampled forms in accordance with the sampling theorem. Moreover, the Discrete Fourier Transform (DFT) is used to replace to time domain operation of convolution by an equivalent operation that involves the multiplication of DFTs. In this context, it is the normal practice to use an efficient procedure known as the Fast Fourier Transform (FFT) algorithm for computing the DFT.

In carrying out the simulation, it is customary to assume that the symbols of the alphabet used in the particular system under study are equally likely, and that the symbols transmitted in adjacent time slots are statistically independent. One way of accomplishing this requirement is to use linear maximal-length or pseudo-noise sequences of sufficient length. Suppose that in a particular simulation run a total of N such symbols are transmitted and, say, L of them are misinterpreted by the receiver. Then, with N assumed to be large enough, the average probability of error will (almost always) be approximately equal to

$$p_e \approx \frac{L}{N}$$

and the approximation becomes better as N approaches infinity. This suggests that in order to measure (with some degree of confidence) an average probability of symbol error as low as 10^{-5}, for example, the number N will have to be at least as large as $10^{\backslash}$ that is, 100 times the reciprocal of the error rate. This results in a standard deviation or root mean-square measurement error of no more than 10 percent.

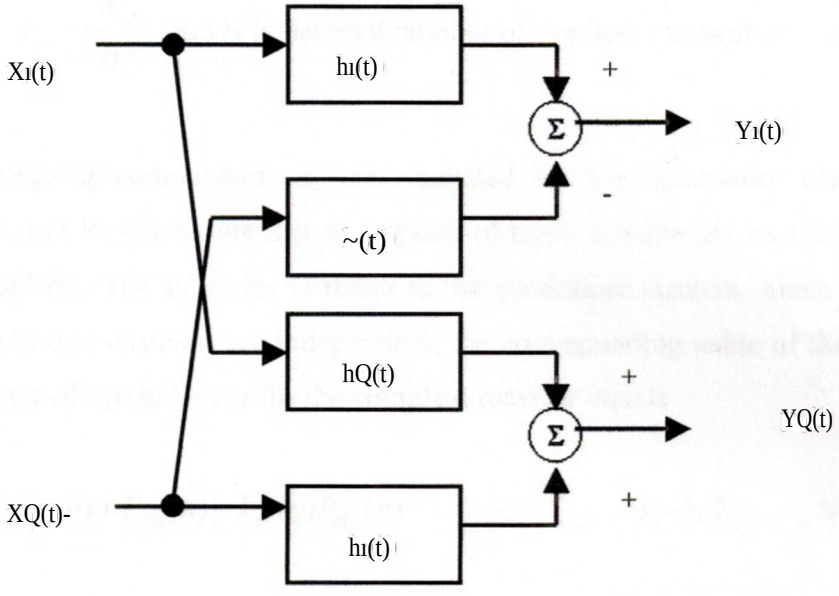


Figure 4.6 Block diagram illustrating the relationships between the in-phase and quadrature components of the response of a band-pass filter and those of the input signal. [Ref 6, page 341]

In the case of linear systems, we may avoid the use of such long simulation runs on a computer (which can be quite expensive) by applying an indirect procedure to evaluate the effects of the transmitted signal and noise separately. We illustrate the procedure by considering a quadrature signalling system. Using the baseband equivalent model of the receiver, we first compute the amplitude of the correlator output (or decision device input) in the in-phase channel of the receiver in response to the in-phase component, $s_I(t)$, of the transmitted signal. This computation is done for each transmitted symbol. Let $a_{I,n}$ denote the value this amplitude for symbol m_o, say. The subscript I refers to the in-phase channel. Next, we compute the variance of the noise at the same point in the receiver, in response to the in-phase noise component, $w_I(t)$.Let σ_I^2 denote this variance. Thus, for symbol m_o we compute the conditional probability of error $P_{eI}(n)$ by using the formula

$$P_{eI}(n) = \frac{1}{\sqrt{2\pi}\sigma_I} \int_{-\infty}^{a_{I,n}} \exp\left(-\frac{x^2}{2\sigma_I^2}\right) dx \qquad n = 1, 2, \ldots\ldots, N$$

where $\tau_{1n} = \frac{az_{n-1}}{\sigma_1}$ and N is the total number of symbols transmitted.

The foregoing computation is next repeated for the quadrature channel of the receiver. Let PeQ(n) denote this probability of error, conditional on the transmission of symbol mn. The subscript Q refers to the quadrature channel. Since the in-phase and quadrature channels are independent, the corresponding value of the conditional probability of symbol error for the complete receiver equals

$$Pe(n) = Pe_I(n) + Pe_Q(n) - Pe_I(n)Pe_Q(n) \qquad n = 1, 2, \ldots\ldots, N$$

By averaging this result over the number of transmitted symbols, N, we get the average probability of symbol error for the complete receiver as

$$Pe = \frac{1}{N}\sum_{n=1}^{N} Pe(n)$$

In the case of a binary signalling system, we have only an in-phase channel, so that PeQ(n) is zero and the average probability of symbol error reduces to

$$Pe = \frac{1}{N}\sum_{n=1}^{N} Pe_I(n)$$

By using the indirect procedure described, the length of a simulation run is reduced by several orders of magnitude compared to the direct procedure. The only requirement is that the pseudo-noise sequence used to generate the in-phase and quadrature components of the transmitted signal should have a .length that is in excess of 100, say, and that all symbols of the alphabet for the system under study occur with approximately equal frequency.

4.6 RELATIONSHIP BETWEEN ERROR PROBABILITY AND BIT ERROR RATE (BER)

Bit error rate of digital communication systems is determined by the number of bits that are corrupted as data are transmitted from source to destination BER is expressed as power of 10 (for example 10^{-5})

Consider the relationships that can be derived for 2 cases of practical interest, as shown here.

Case 1

In the first case , the mapping from binary to M-ary symbols is performed in such a way that the two binary M-tuples corresponding to any pair of adjacent symbols in the M-ary modulation scheme differ in only one bit position. This mapping constraint is satisfied by using a Gray code.

Consider, for example, the Gray-encoded version of M-ary PSK, which is shown illustrated in Fig.4.7 for M = 4 and M = 8. When the probability of symbol error Peis acceptably small, we find that the probability of mistaking one symbol for either of the two 'nearest' (in-phase) symbols is much greater than any other kind of symbol error. Moreover, given a symbol error, the most probable number of bits error is one, subject to aforementioned mapping constraint. Since there are $\log_2 M$ bits per symbol, it follows that the bit error rate is related to the probability of symbol error by the simple formula

$$BER = \frac{Pe}{\log 2M} \quad M \sim 2 \tag{4.21}$$

For example under Case 1 we may consider the Gray-encoded version of M-ary QAM. This form of modulation is ilJustrated in Fig.2.10 for M=16. The corresponding Gray-encoded versions of the in-phase and quadrature components are

shown in Figs 2.11.a and 2.11.b. It is evident from Fig 2.11 that there is a change in only one bit position as we move from any symbol to an adjacent one horizontally or vertically. When the probability of symbol error is acceptably small, we find that the probability of mistaking a symbol for an adjacent one horizontally or vertically is much greater than any other kind of symbol error. Accordingly as in M-ary PSK, the bit error rate for M-ary QAM is related to probability of symbol error Pe.

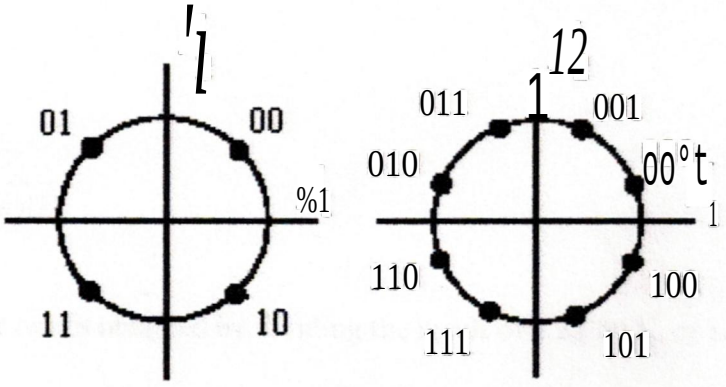


Figure 4.7 Signal constellations of M-ary PSK for (a) M = 4, and (b) M = 8 with the message points identified by 2-bit and 3-bit Gray codes, respectively.

[Ref 6, page 342]

Case 2

In the second case we assume that all symbol errors are equally likely and occur with probability

$$\frac{Pe}{M-1} = \frac{Pe}{2K-1}$$

where Pe is the average probability of symbol error and Kr=log$_2$ M. Since there are $\binom{K}{k}$ ways in which k bits out of k may be in error, it follows that the average number of bit errors perk-bit symbol is given by

$$\sum_{k=1}^{K} k\binom{K}{k}\frac{P_e}{2^K-1} = \frac{2^{K-1}}{2^K-1}KP_e \tag{4.22}$$

where

$$\binom{K}{k} = \frac{K!}{(K-k)!k!} \tag{4.23}$$

The bit error rate is obtained by dividing the result of 4.22 by K, as shown by

$$BER = \left(\frac{2^{K-1}}{2^K-1}\right)P_e \tag{4.24}$$

or equally

$$BER = \left[\frac{M}{M-1}\right]P_e \tag{4.25}$$

For large M the bit error rate approaches the limiting value Pe/2.

CHAPTERS DESIGN OF THE NON-COHERENT DPSKSYSTEM

In this chapter we will discuss our selected most advantageocs [illegible] DPSK in detail. To understand the operation of'transmissioo [illegible] modulation scheme better we will briefly discuss all the [illegible] the transmission system. These components are mentioned below in order as shown in the block diagram.

5.1 TRANSMITTER

In our frame of work we assume that we already have [illegible] signal as an input so that we do not need to go throegh the [illegible] differential encoding system, but illustration an example [illegible] input signal is 1001.

Starting from the structure of DPSK modulator we will observe [illegible] used in modem and three functions. Basically we may split [illegible] three operations. The first two parts are logical circuits that [illegible] the output line according to the input signal while the other parts [illegible] shifted version of the input clock signal. Normaliy the [illegible] modulator are

- DPSK encoder
- Parallel-to-serial code converter (PSC)
- FM modulator

The principle of the realization of DPSK encoder was considered in the section 1.5.1 (p.11-13). Now in the coming sections we will observe the principle operations of the remaining elements of the system.

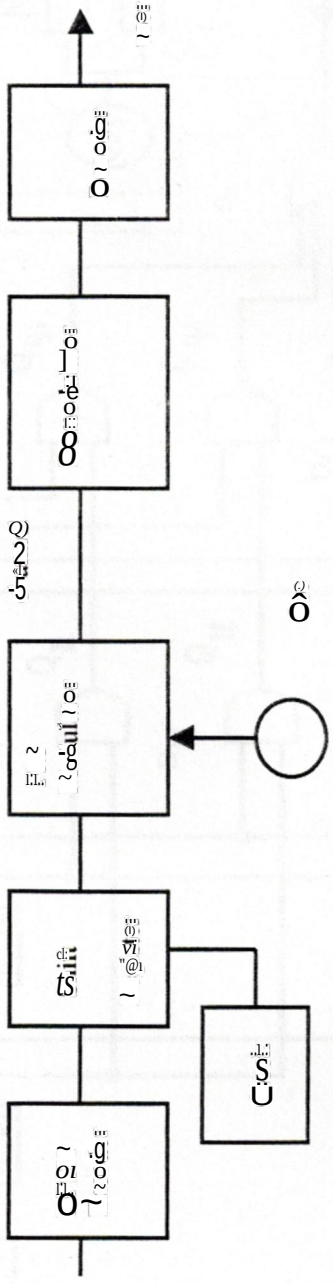
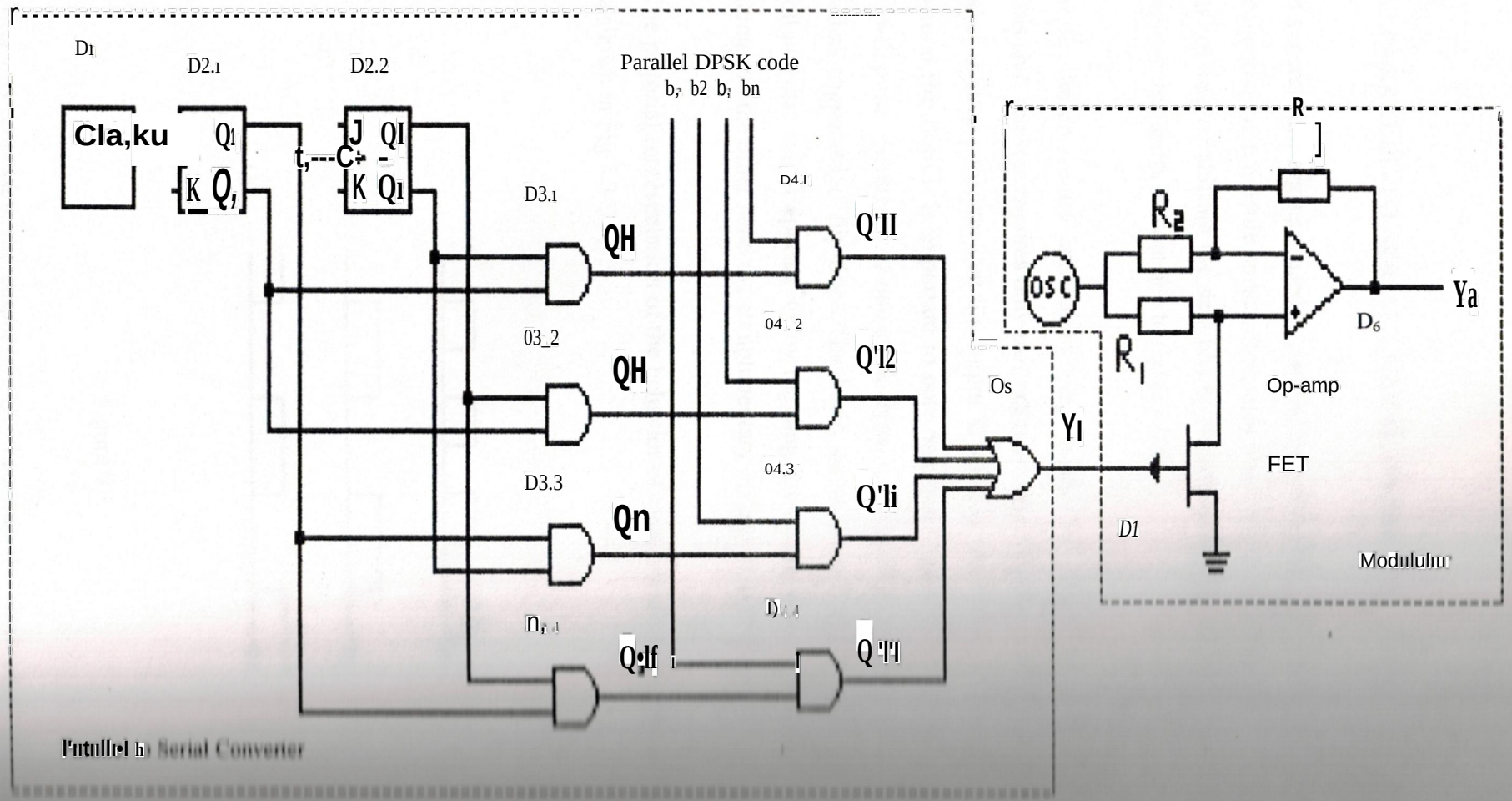


Figure 5.1 DPSK Communication System



D1 : Clock Generator
D2 : Jk flip flops
D3 : AND gates
D4 : AND gates
D5 : OR gates
D6 : Op : Amp
D7 : Field effect transistor
OSC : Oscillator
R1 , R2 , R3 : resistors

5.2 **PARALLEL-TO-SERIAL CODE CONVERTER**

In general shift registers used as parallel to serial code converter is a sequential logic module constructed from flip-flops to manipulate the binary data by shifting the data bits to the left or right. It is a register that shifts its contents to right or left.

In our design we are establishing very simple shift register using two flip-flops. This shift register requires only two negative-edge flip-flops connected to each other in such a manner that the output 'Q' of first flip-flop becomes the input of the second flip-flop. It is important to note that in our case we are using negative-edge flip-flop that requires only one clock signal as an input. Such type of flip-flop is also called trigger-edge flip-flop. The basic operation of trigger-edge flip-flop is as follows that output appears 'Q' by toggling each time when a negative pulse comes along. On the other hand the complimentary output appears at $\overline{Q}$.

The pictorial representation of the behavior of negative-edge flip-flop is shown in Fig.5.3

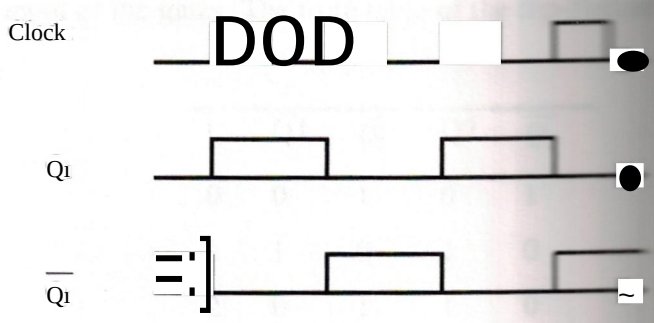


Figure 5.3

After this processing the output of 'Q1' becomes the clock input of the second flip-flop and here the same function of flip-flop starts again as shown in Fig.

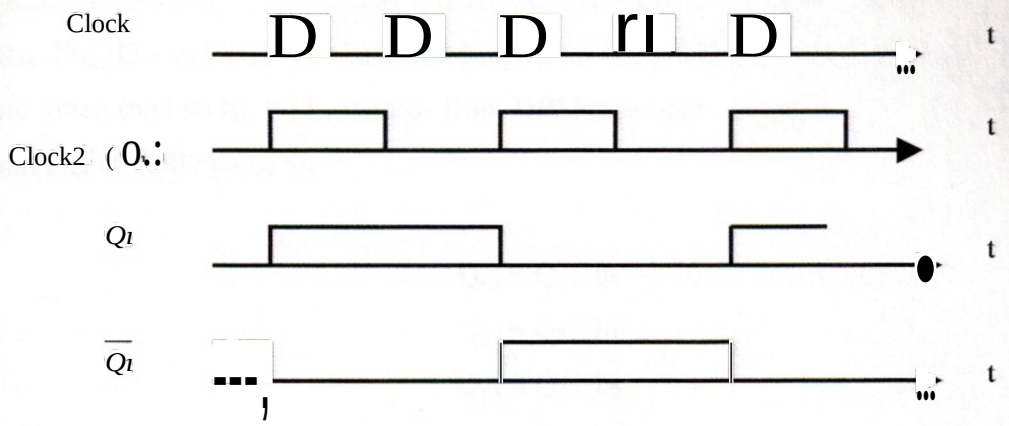


Figure 5.4

After the completion of this operation these outputs of flip-flop are connected to the 2 input AND gates D31- D34 with following input pin configuration.

$$Q31 = \overline{Q_1}.\overline{Q2}$$

$$Q32 = \overline{Q_1}.Q2$$

$$Q33 = Q_1.\overline{Q2}$$

$$Q34 = Q_1.Q2$$

Here the Q31, Q32, Q33 and Q34 are the output of the AND gates while Q_1, $\overline{Q_1}$, Q2 and $\overline{Q2}$ are the input of the gates. The truth table of the flip-flop are shown in Table 5.1.

C	QI	$\overline{Q_1}$	Q2	$\overline{Q2}$
0	0	1	0	1
1	1	0	1	0
2	0	1	1	0
3	1	0	0	1
4	0	1	0	1
5	1	0	1	0

Table 5.1

Output levels Q31, Q32, Q33 and Q34 are applied to the first inputs of the AND gates 041, 042, 043 and 044. To the second inputs of the AND gates 041, 042, 043 and 044 are given the bits bo, b1, b2, and b3 from OPSK encoder. Outputs of the 041, 042, 043 and 044 of AND gates are

$$Q41 = Q31 \cdot b_0$$
$$Q42 = Q32 \cdot b_1$$
$$Q43 = Q33 \cdot b_2$$
$$Q44 = Q34 \cdot b_3$$

combined on the single output by 4-inputs OR-gate (Ds). Thus using sequential output signals of the flip-flops 021 and 022 and combination AND-OR we cover parallel code into serial. Timing diagram of the converter is given in Fig.5.5 using code $b_0 = 0$, $b_1 = 1$, $b_2 = 0$ and $b_3 = 1$.

5.3 PSK MODULATOR

Principles of operation of modulator based on the switching inverting and non-inverting inputs of the amplifier in accordance to the bits of data stream Y_1. Modulator consist of op-amp (O_6), input bridge having the resistors R_1, R_2, R_3 and Field Effect Transistor (O?) channel resistance Rso carrier. As source for the bridge is used carrier sinusoidal signal u_c generated by oscillator OSC. Output signal of amplifier is determined using superposition principle:

$$Y_2 = u_S \cdot (1 + \frac{R_3}{R_2}) \cdot (\frac{R_{SO}}{R_1 + R_{SD}}) - (\frac{R_3}{R_2}) u_S$$

When FET transistor gate has "0" $R_{SD} \cong 0$ and amplifier operates in the inverting mode :

$$Y2 = -\frac{R3}{R4}us$$

$$= -u8 \qquad \text{if } R_3 = R_2$$

When FET gate has "1" then Rso :::0 and amplifier operates in the noninverting mode

$$Y2 = us\left(1 + \frac{R3}{R4}\right) - \frac{R3}{R4}.Us = us$$

Thus in accordance to the bits Y_1 amplifier switched one of the two way inverting and non-inverting. Timing diagram of the PSK modulator is shown in Fig.5.6.

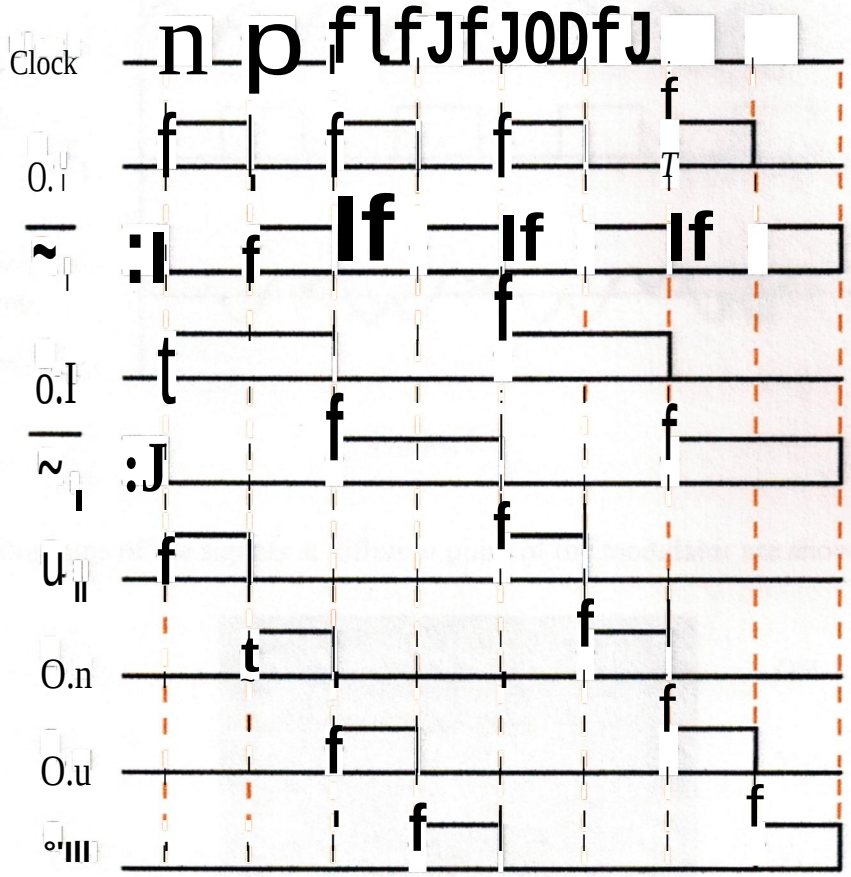


Figure 5.5

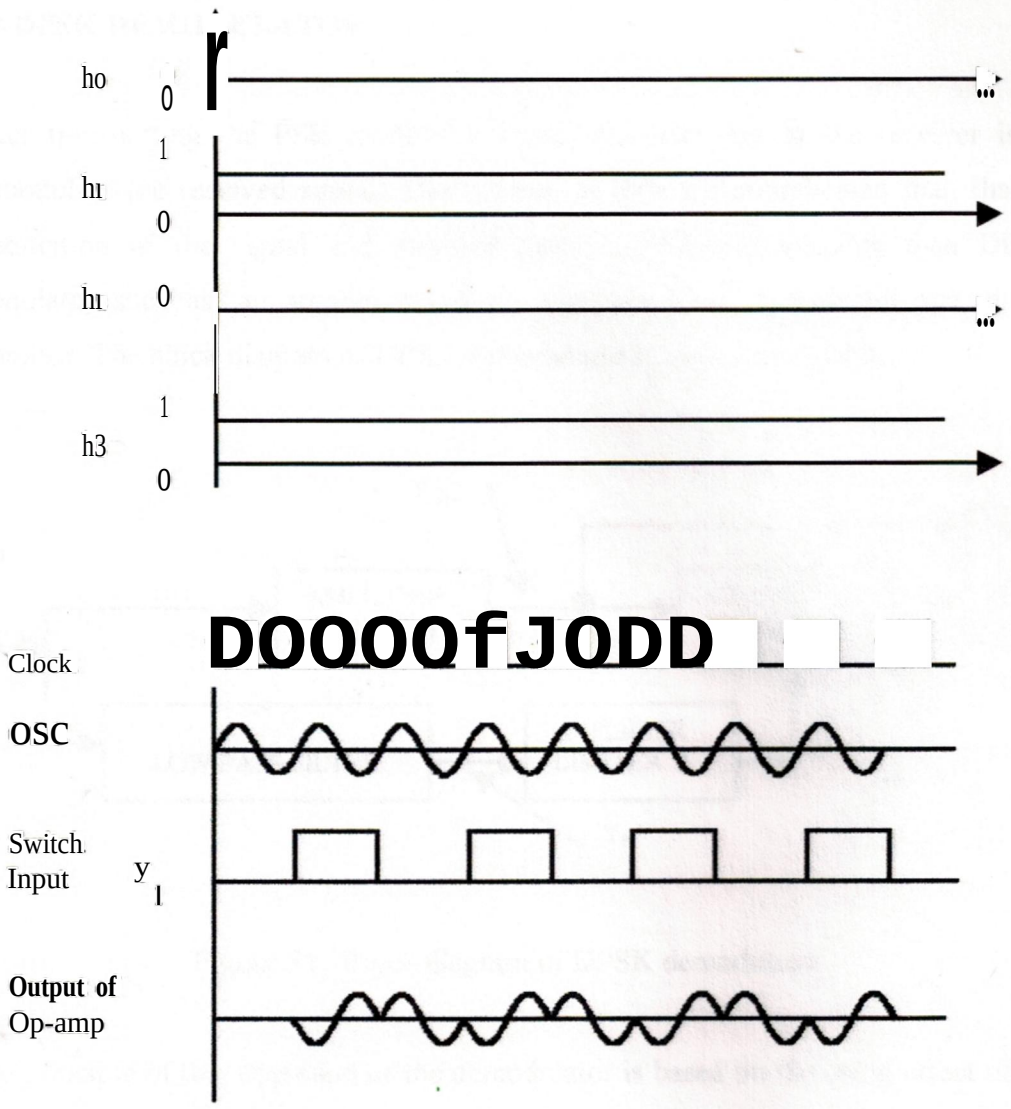


Figure 5.6

The oscillograms of the signals at different point of the modulator are shown in Fig.5.7

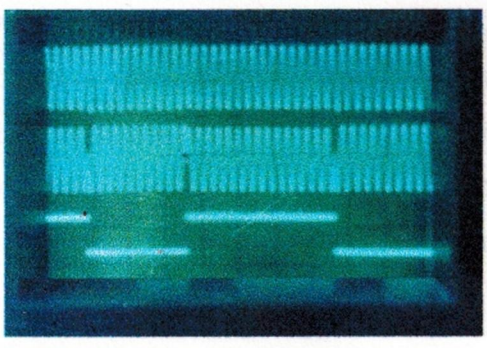


Figure 5.7

5.4 DPSK DEMODULATOR

After transmitting the PSK modulated signal the next task at the receiver is to demodulate the received signal. This process is little bit complicated than that of modulation of the signal and required more complicated circuitry than DPSK modulator such as, an amplitude limiter, low-pass filter, comparator and circuit inhibitor. The block diagram ofDPSK demodulator is shown in Fig.5.8.

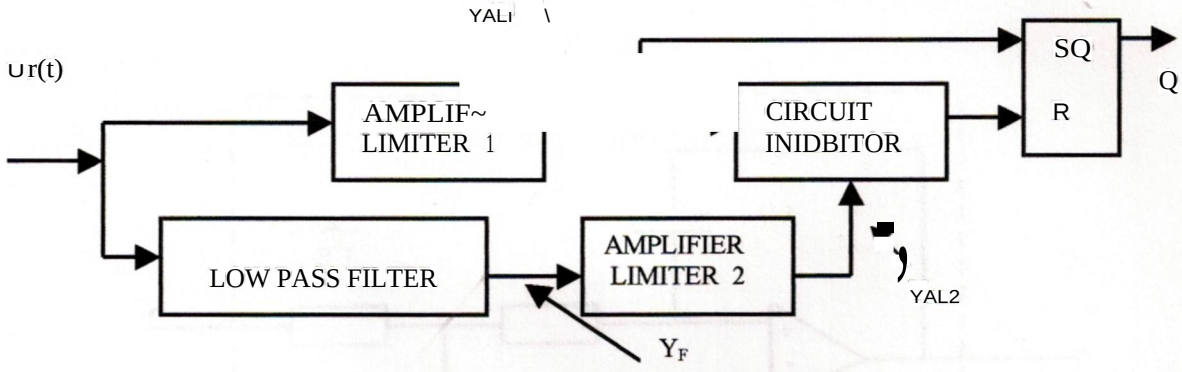


Figure 5.8 Block diagram ofDPSK demodulator.

The principle of the operation of the demodulator is based on the using effect of the amplitude variation of the output of the low pass filter when its input phase is switched from 0 to 180 and vice versa. Using this effect we avoid the complicated method of coherent detection of PSK signal that needs the exact replicas of the transmitters carrier signal in the receiver. The received PSK modulated signal at the receiver passes through two branches of the modulator. In the first branch the signal goes into the amplitude limiter or comparator, where the comparator change the input signal into the digital signal by rejecting the negative part of the message signal. In the second branch the message signal passes to another comparator via low-pass filter where the low-pass filter stable the signal for certain value of amplitude.

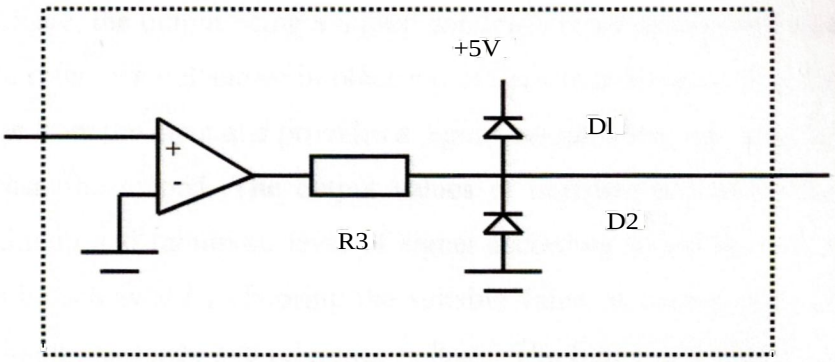


Fig 5.9 Amplifier Limiter (Comparator)

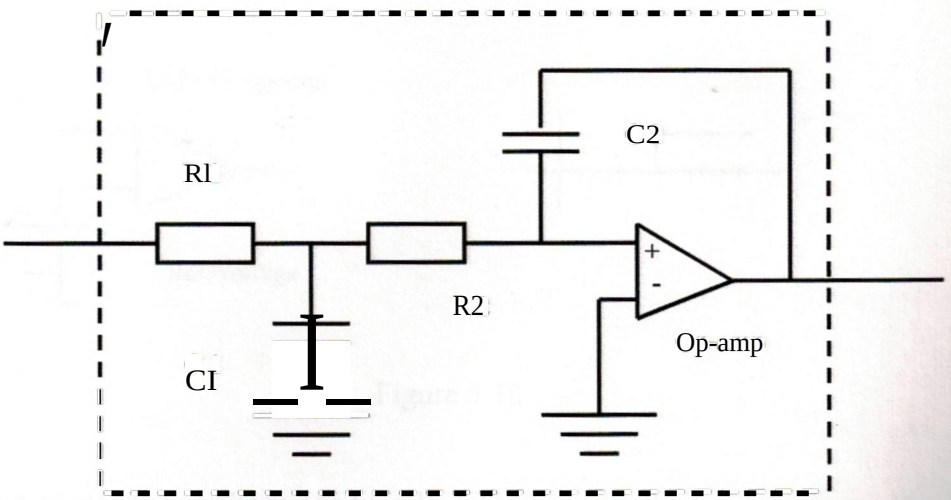


Fig 5. I0 Low Pass Filter

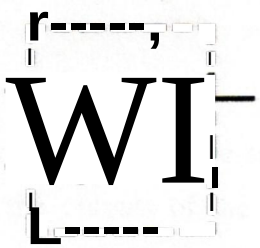


Fig 5.I I Inhibitor

A comparator circuit is one to which a linear input voltage is compared to another reference voltage, the output being a digital condition representing the input voltage exceeded the reference voltage or in other we can say that a comparator accepts the linear voltage from the input and provides a digital output when one input is less than or greater than the second. The output values of comparator can be changed to require maximum and minimum level of signal according to the need of operation and this can be achieved by choosing the suitable value of comparator parameters, such as the input resistance and reference voltage. The figure of LM339 comparator (Fig.5.12) that provided maximum 5V and minimum OV as an output and it is also a suitable choice for our purpose.

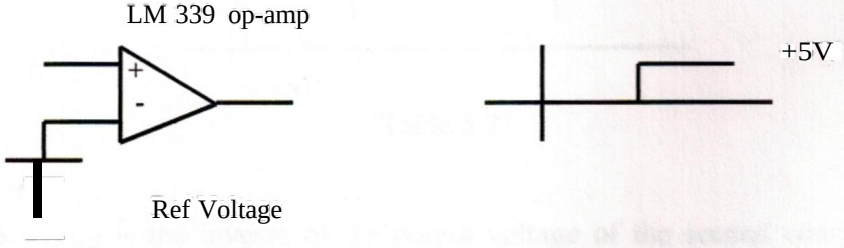


Figure 5. 12

The value of reference voltage can be calculated by using the formula shown below

$$VRr = (R{:}1 / R1+R2) * V_{cc}$$

Here, V_{cc} is the input inverting terminal voltage of comparator. Now we have two output.

This circuit consists of an inverter connected to the second output of comparators and one AND gate connected to the outputs of the both comparator. Finally the output of circuit inhibitor again inverted. The truth table of this operation is shown in Fig. 5.13

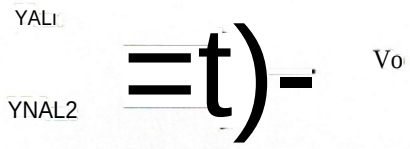


Figure 5. 13

YALI	YNAL2	Vo = YNALı . Y AL2
0	0	0
0	1	0
1	0	0
1	1	1

Table 5.2

Here the YNAL2 is the inverse of the output voltage of the second comparator and YALı is the output voltage of first comparator while the Vo is the inhibitor output and SR flip-flops RESET input. YALı is connected to SET input of RS flip-flop. The Q output of the flip flop is the demodulator output of the PSK signal. The oscillogram of demodulator signals are shown in fig 5.14

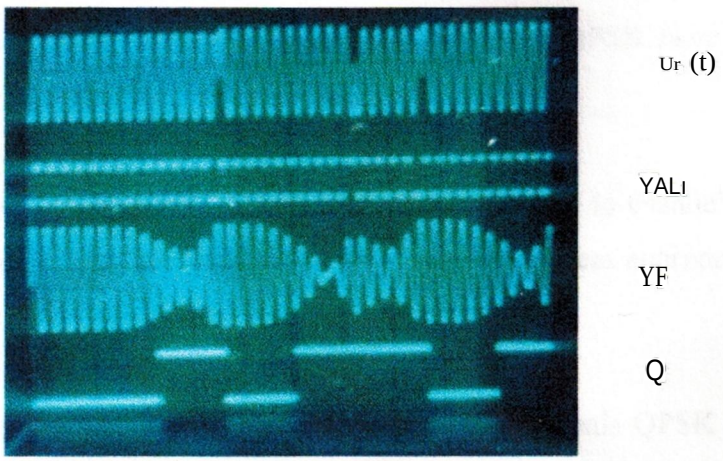


Figure 5. 14

CONCLUSION

1. In this thesis we covered performance analysis of the digital modulation techniques including FSK, PSK and M-ary PSK modulations.

2. Performance analysis has been performed with emphasis on the average probability of error transmission in the presence of the additive white noise.

3. Based on the such assumptions as equal probability symbols transmissions, limited-power of the transmitted signals and presence additive Gaussian noise we presented a detailed analysis coherent PSK modulation techniques.

4. Comparing the probability of error obtained for FSK with the probability of error obtained for PSK, we see that equal probability error in each system can be achieved if the signal energy in the PSK signal is $J0.6$ times as large as the signal energy in FSK.

5. Comparison of the different method of modulation techniques show that perturbed by additive Gaussian noise, PSK modulation is the optimum for transmitting binary data to achieve the minimum probability of symbol error. For high value of the energy to noise density ratio PSK and QPSK have about the same error rate performance.

6. Bandwidth efficiency determined by the ratio of the bit rate to channel bandwith is increasing by M. We saw that as Mis increased the system approaches to the Shannon's limit.

7. Analysis shows that among the family of M-ary PSK signals QPSK offers the best trade-off between power and bandwidth requirement.

8. M-ary PSK and M-ary QAM have similar spectral and bandwidth characteristics. Comparison of these two signals constellation reveals that the distance between the message points of M-ary PSK smaller than the message points of M-ary QAM for fixed peak transmitted power. However the superior performance M-ary QAM can be realized only if the channel is linear.

9. The using effect of amplitude variation of the output of low pass filter when its input phase is switched we design non-coherent PSK demodulation systems having high performance characteristics. This method of detection of the PSK signals do not suffer degradation due to incoherence. We design the modulation and the demodulation of non-coherent DPSK system.

APPENDIX A [Ref 9]

A.1. MODULATION & DEMODULATION STANDARDS

The two organisations responsible for most modem modulation & demodulation standards in North America are the Bell System & the CCITT in Europe. The Bell System standards were for all practical purposes the only modems used in North America through the 1960's, & modems that use the Bell System standards are still used in some slower communications applications. Many newer can fall back to the one of the Bell System standards to communicate with those older & slower modems. Today , almost all modems built for computer -to-computer communications over the telephone network adhere to the CCITT standards. A list of the more common modem standards are shown in the below Table A.I

bis	Standard	Modulation	Duplex
300	Bell 103	FSK	Full
1200	Bell 202	FSK	Half
1200	Bell 212A	4PSK	Full
1200	V.22	4PSK	Full
2400	V.22 bis	QAM	Full
9600	V.32	QAM	full
14,400	V.32 bis	QAM	Full
28,800	V.34	QAM	Full

Table A. I. Some common modulation standards for modems.

A.1.1 BELL 103:

The Bell 103 modem standards uses a 200 - Hz carrier shift for full-duplex communications at 300 *bis* over the two - wire dial-up telephone lines. The modem that originates the call uses the half the bandwidth for sending data , 6 the modem that receives the call sends data through the half of the circuit's bandwidth. A Bell 103 standard modem in the originate mode transmits a mark frequency of 1270 Hz & a space frequency of 1070 Hz . In the answer mode it transmits 2025 Hz as a space & 2225 Hz as a mark.

The Bell 103 standards were once widely used for communications between two personal computers . It has also been applied to link a bank's central computer with its automated teller machines & for communication between a credit card company's central computer & credit card verification terminals in retail stores . Today, the Bell 103 standard's 300- *bis* communication speed is considered painfully slow for most applications . The fact that Bell 103 modems can be used only in asynchronous communication systems is also a serious disadvantage. Although theBell 103 standards are out of date , most modems built for use in North America with capabilities up to 2400 *bis* have the ability to fall back to the Bell 103 standard to communicate with older modems.

The Bell 103 modem is an asynchronous modem designed to operate full duplex over switched or leased lines. Transmission speed is limited to 300 bps.

A.1.2. Bell 202 Modem

Bell 202 is another early synchronous FSK modem standards . It was d~ for half-duplex communications , & modems built to the Bell 202 standard can therefore use the full bandwidth of the telephone circuit. The greater bandwidth enables Bell 202 modems to operate at higher speed than do Bell 103 modems. Bell 202 modems can operate at 1200 *bis* over a dial - up telephone line & at 1800 b/s on a leased ,

conditioned line. They use a frequency of 1200 Hz to represent a mark & 2200 Hz to represent a space. Bell 202 modems have a low speed 5-b/s back channel that uses AM with a carrier frequency of 387 Hz that the receiver modem can use to send an ACK or NAK signal at the end of each block of data without the need of turning the circuit around.

A disadvantage with the Bell 103 - type is having to divide the existing bandwidth of the telephone lines into one half in order to obtain frequencies channels for full-duplex operation. Transmission speed is scarified in this case. The Bell 202 modem operates in the half -duplex mode .Since the transmission occurs in only one direction at a time between modems , the entire bandwidth can be utilised by the transmitted signal. A higher transmission rate is achieved For switched lines , the transmission rate is 1200 bps, whereas for leased lines with C2 conditioning, 1800 bps is used. FSK is the modulation technique employed. A mark is represented by 1200 Hz and a space is represented by 2200 Hz. Figure below illustrates the frequency assignment for the Bell 202 modem.

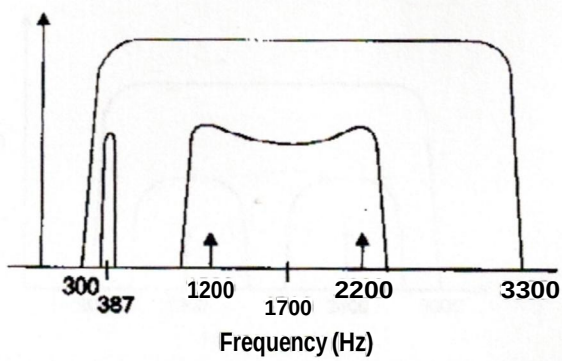


Fig A.1 Bell 202-frequency assignment.

A.I.3 Bell 212A Modem

The Bell 212A is a two-speed modem that operates full duplex and supports asynchronous or synchronous transmission modes over the switched lines. The low-speed asynchronous mode operates *in* accordance with the BELL I03 specification

with a 300-bps data transfer rate and FSK employed as the modulation technique. Transmit frequencies for the originate mode are 1070 Hz (space) and 270 Hz (mark). Receive frequencies for the originate mode are 2025 Hz (space) and 2225 Hz (mark). In the answer mode , the opposite frequencies are used to permit full-duplex operation.

In the high-speed mode , characters can be transmitted synchronously or synchronously at 1200 bps. Four-phase DPSK is used to phase shift a 200-Hz none for the originate mode and a 2400-Hz tone for the answer mode. Figure below illustrates the Bell 212A frequency assignment for the high-speed mode. A mark and a space are not represented by two discrete frequencies , as in the case with FSK. Instead, each consecutive two bits of the serial binary data sent to the 212A modem are encoded into a single-phase change of the carrier frequency. The encoded two bits are called debits. Since a debit represents two bits , there are four possible phase changes that the carrier frequency can undergo. This is shown in the phasor diagram of figure below. Notice that the encoded bits are Gray coded. Four-phase DPSK is also referred to as quadrature PSK (DPSK).

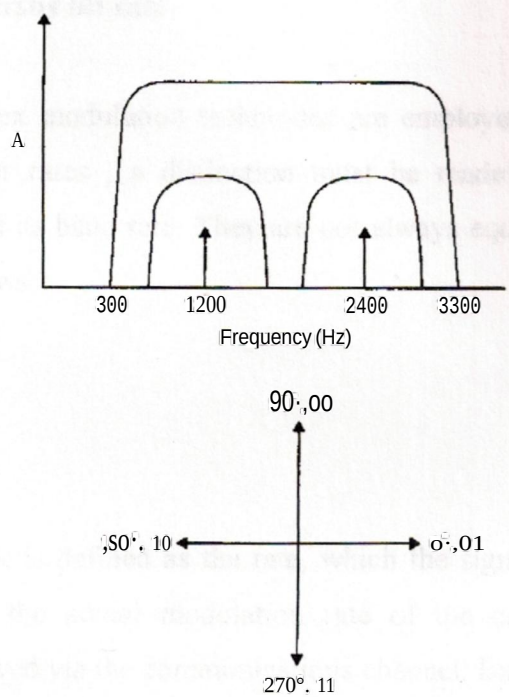


Fig A.3 The Bell family of modems.

A.1.4. M-ARY

When PSK or QAM is used as a modulation technique the term M-ary , derived from bi-nary , is used to denote the number of encoded bits used to modulate the carrier frequency. M-ary is governed by the equation n=log2 M where n is the number of encoded bits used to represent a carrier state, M-ary , and Mis the number of state changes that the carrier can undergo represented by n bits.

Example : The Bell 208 modem employs eight-phase DPSK as its modulation techniques. Compute the M-ary.

Solution: n = log2M

= log2 8

=3

Therefore , M-ary = 3 bits.

A.1.5 Baud rate versus bit rate

When more complex modulation techniques are employed by modems to achieve higher data transfer rates , a distinction must be made between the transmitted signal's bit rate and its baud rate. They are not always equal. Bit rate and baud rate are defined as follows:

A.1.5.1 Baud rate:

A signal's baud rate is defined as the rate, which the signal changes per unit time. For modems it is the actual modulation rate of the carrier frequency as it is transmitted or received via the communications channel. Baud rate also [illegible] as signalling rate.

Al.5.2 Bit rate:

A signal's bit rate is the actual number of binary bits transmitted per second (bps) onto the communications channel.

Bell 212A modems have a modulation rate of 600 baud when operating in the high-speed mode. This is equal to one-half of its bit rate of 1200 bps since its carrier frequency is phase shifted at dibit intervals (1200=2*600). In its low-speed mode , however, the baud rate and bit rate (300) are equal; that is , the carrier is frequency shifted at the same rate as the binary serial data stream.

A.1.6 Bell 201 B/C Modem

The Bell 201 family of modems is designed to operate at a fixed data transfer rate o 2400 bps over the basic , unconditioned , 3002-type line or two- or four-wire private line. The Bell 201A is an obsolete 2000-bps modem , the Bell 201B is for private or leased line applications , and the Bell 201C is for switched or leased line applications. Each modem is designed for half-duplex operation over the switched line or full-duplex operation operation over the four-wire private line. Four phase DPSK is the modulation technique employed to achieve 2400 bps. The phasor diagram for the Bell 201B/C is shown in figure below.

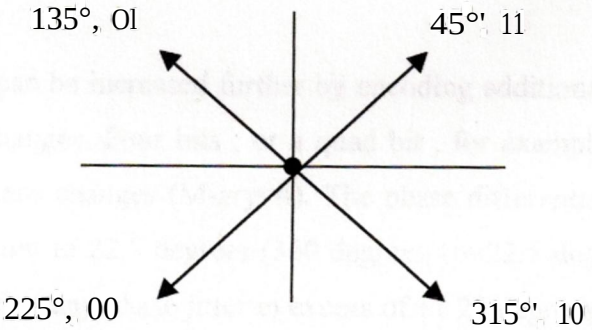


Fig A.4 Phasor diagram for Bell 201 b/c modem.

A.1.7 Bell 208A and 208B Modems

Bell 208A and 208B modems are designed for synchronous transmission and reception of data at 4800 bps over four-wire private leased lines and switched lines , respectively. Eight-phase DPSK is employed on a 800-Hz carrier frequency. Each consecutive three bits , called tribits , of the binary serial input data are encoded into a single-phase change of the carrier frequency. The encoding of three bits into a tribit allows the representations eight possible phase changes of the carrier frequency. A transmission rate of three times the baud rate of 1600 is achieved (4800=1600*3). Figure below depicts the phasor diagram for the Bell 208A modem. Notice , here again , that a Gray code is used.

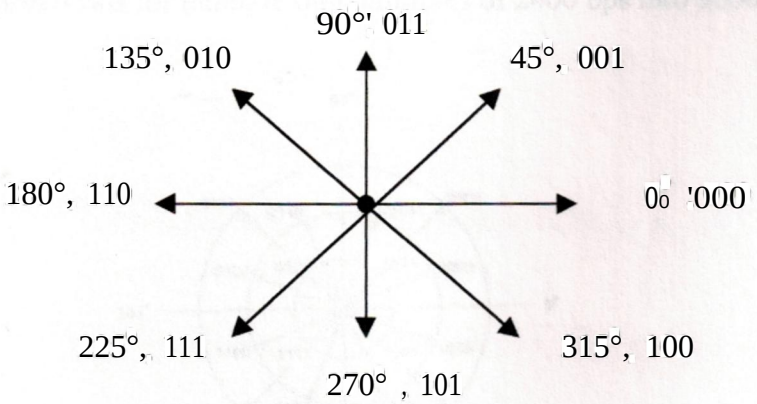


Fig a.5 Phasor diagram for the Bell 208a modem

A.1.8 Bell 209A Modem

Data transfer rates can be increased further by encoding additional bits into a greater number of phase changes. Four bits , or a quad bit , for example , can be encoded into 16 possible phase changes (M-ary=4). The phase differential between adjacent phasors would amount to 22.5 degrees (360 degrees/16=22.5 degrees). The problem here, however, is that any phase jitter in excess of 11.25 degrees would result in the detection of erroneous data. This amount of phase jitter is not uncommon in long-

haul networks that utilise regenerative repeaters and digital multiplexers. For this reason , lô-phase PSK is generally not used.

To avoid the problem of phase jitter, the Bell 209A modem employs a combination of ASK and PSK called quadrature amplitude modulation (QAM). QAM , pronounced -Kwamm , is a modulation technique that uses 12 different phases and three different amplitudes to represent 16 possible carrier states. Susceptibility to phase jitter is effectively reduced by increasing the separation between adjacent phasors. The phasor diagram for the Bell 209A QAM signal is shown in Figure below. Each state is represented by one of 16 possible quadbits. By employing QAM , 9600-bps full-duplex synchronous communications is achieved using a baud rate of 2400 (9600=4*2400) over private four-wire lines with Dl conditioning. The Bell 209A also has provisions for multiplexing multiples of 2400 bps into 9600 bps.

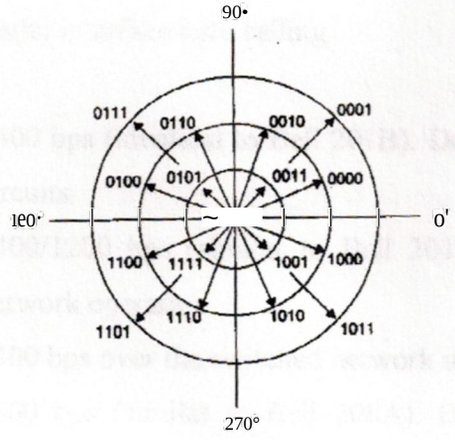


Fig A.6 Phasor diagram for the Bell 209A modem (QAM).

A.2. CCITT MODEMS AND RECOMMENDATIONS

Data transmission standards outside the United States are set by CCITT , which is part of the International Telecommunications Union , headquartered in Geneva , Switzerland. Standards V.21 , V.23 , and V.26 describe modems similar to the Bell 103,202, and 201, respectively, V.22 describes modems similar to the Bell 212A ,

and V.29 is similar to the Bell 209A specification. Table below lists CCITT modems and recommendations.

Recommendations	Description
V.21	0 to 200 (300) bps (similar to Bell 103). Defined for FOX switched network operation
V.22	1200-bps, FOX, switched, and leased line network operation
V.22b	1200/2400-bps , FOX , switched , and leased line network operation
V.23	600/1200=bps (similar to Bell 202). Defined for HDX switched network operation. Optional 75-bps reverse channel
V.24	Definition of interchange circuits (similar to EIA RS -232-C).
V.25	Automatic calling units (similar to Bell 80)
V.25b	Serial interface auto calling
V.26	2400 bps (identical to Bell 201B). Defined for four-wire leased circuits.
V.26b	2400/1200 bps (similar to Bell 201C). Defined for switched network operation
V.26ter	2400 bps over the switched network using echo cancelling.
V.27	4800 bps (similar to Bell 208A). Defined for leased circuits using manual equalisers.
V.27b	4800/2400 bps with auto equalisers for leased lines.
V.27ter	4800/2400 bps for use on switched lines.
V.29	9600-bps FDX (similar to Bell 209). Defined for leased circuits.
V.32	9600-bps FDX for switched or leased-line circuits using echo cancelling
V.32b	14,400-bps FDX for switched or leased-line circuits using echo cancelling
V.33	14,400-bps FDX for leased lines.

V.42	Error-correction procedures for DCEs using asynchronous to synchronous conversion
V.42b	An extension ofV.42 that defines data compression for use with V.42
V.43	(V.FAST) ITU-TS 28,800 bps standard.

Table A.2

A.2.1 CCITT Modern Recommendation V.22bis

CCITT's V.22 bis (bis means second revision in French and ter means third revision) specification provides for 1200- and 2400-bps synchronous full-duplex communication over switched and two-wire leased lines. Four-phase DPSK is employed as the modulation technique for modem operation at 1200 bps. QAM is used to achieve a data transfer rate of 2400 bps. Modulation rate is specified at 600 baud for both operating speeds. *Full-duplex* operation is achieved by phase and amplitude shift keying a low-channel carrier frequency of 1200 Hz and a high-channel carrier frequency of 2400 Hz.

Phase and amplitude assignment for dibit (1200 bps) and quadbit (2400 bps) encoding is depicted by CCITT as a Iô-point signal constellation rather than a phasor diagram. They are essentially the same. Figure below illustrates the signal constellation for the V.22bis specification. For 1200-bps operation , the data stream is divided into groups of two consecutive bits or dibits. Each dibit is encoded into a quadrant phase change relative to the preceding phase of the carrier frequency. This is shown in table below. For 2400-bps operation, the data stream divided into groups of four consecutive bits or quadbits. The two least significant bits of the quad bit are encoded into a quadran phase change in the same manner as for 1200-bps operation. The most significant two bits of the quadbit define one of four signalling elements associated with the new quadrant.

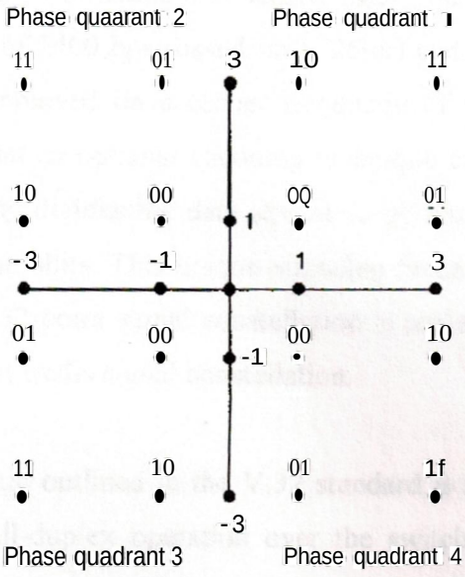


Fig A.7 V.22 16 point signal constellation.

A.2.2 CCITT Modem Recommendation V.29

CCITT V.29 specification is the first internationally recognised standard for 9600-bps communications. This standard provides for synchronous data transmission over four-wire leased lines. The same lô-point QAM signal constellation used for V.22bis is used for the V.29 specification. The higher data transfer rate is made possible by using a single carrier frequency of 1700 Hz and increasing the baud rate from V.22bis's 600 baud to 2400 baud. The entire bandwidth is utilised. Some modern manufacturers have elected to use V.29-compatible modems in half-duplex mode over the switched lines. Psuedo-full-duplex operation over the switched lines is also performed by one of two techniques: ping-pong or statistical duplexing. These are described next.

A.2.3 CCITT Modem Recommendation V.32

CCITT's V.32 recommendation is intended for the use of9600-bps synchronous

modems on connections to switched and leased lines. The recommendation also specifies signaling rates of 2400 bps (based on V.26ter) and 4800 bps. QAM is the modulation technique employed on a carrier frequency of 1800 Hz. V.32 is very similar to V.29 except that an optional encoding technique called trellis encoding is specified. Trellis encoding divides the data stream to be transmitted into groups of five consecutive bits of quinbits. This unique encoding technique results in superior signal-to-noise ratios. A 32-point signal constellation is achieved (M-ary=5). Figure below depicts the 32-point trellis signal constellation.

One principal characteristic outlined in the V.32 standard is to provide for a 9600-bps modem with true full-duplex operation over the switched lines. Through the advanced technology of digital signal processors (DSPs) , full-duplex operation is achieved by a technique called echo cancellation. Echo cancellation is performed by adding an inverted replica of the transmitted signal to the received data stream. This permits the transmitted data from each modem to use the same carrier frequency and modulation technique simultaneously. The two clashing signals are separated by the receiver section of each modem.

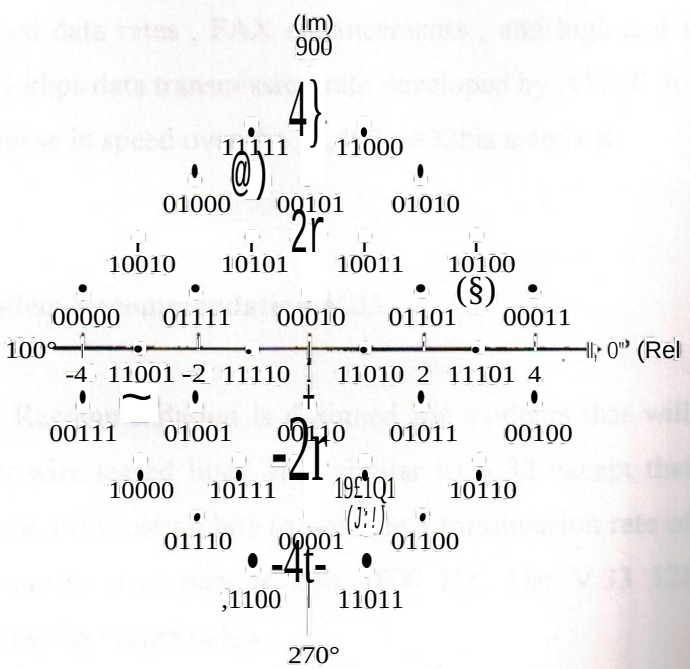


Fig a.8 V.32 constellation diagram.

A.2.4 CCITT Modem Recommendation V.32bis and V.32 terb

In 1991 , the V.32bis standard created a new benchmark in the industry , allowing modem speeds of 14,400 bits per second (bps) , 50% faster than the V.32 9600 bps modem standard at the time. Instead of using a 16-point signal constellation (four bits per baud) as in the V.32 standard , V.32bis uses a 64-point signal constellation (six bits per baud) and maintains the same 2400-baud rate as V.32. Thus , 14,400 bps(6*2400=14,400) , full-duplex operation over the two-wire switched lines is achieved. Another improvement of V.32bis over V.32 is the inclusions of automatic fall forward , the ability to return to a higher transmission speed when the line quality improves. V.32bis modems can also fall back or quickly slow down to 12,200 bps , 9600 , or 4800 bps if line quality degrades. Most V.32bis modems also support Group III fax. Group III fax is a standard for fax communication that specifies the connection procedure between two fax machines or fax modems and the data compression procedure that will be followed during the transmission.

In August 1993 , U.S. Robotics Inc. announced a major evolution to its product line: the V.32 turbo protocol with its property Adaptive Speed Leveling technology which boosts modem speeds to 21.6 kbps . These new features fall into three new categories: increased data rates, FAX enhancements , and high-end features. V.32 terbo is the new 19-kbps data transmission rate developed by AT&T. It is designed to deliver a 33% increase in speed over the 14,400-v>32bis standard.

A.2.5 CCITT Modem Recommendation V.33

The CCITT V.33 Recommendation is designed for modems that will operate over point-to-point four-wire leased lines. It is similar to V.32 except that it encodes a redundant bit and six information bits to produce a transmission rate of 14,400 bps a 2400 baud. The carrier frequency is also 1800 Hz. The V.33 128-point signal constellation is shown in Figure below.

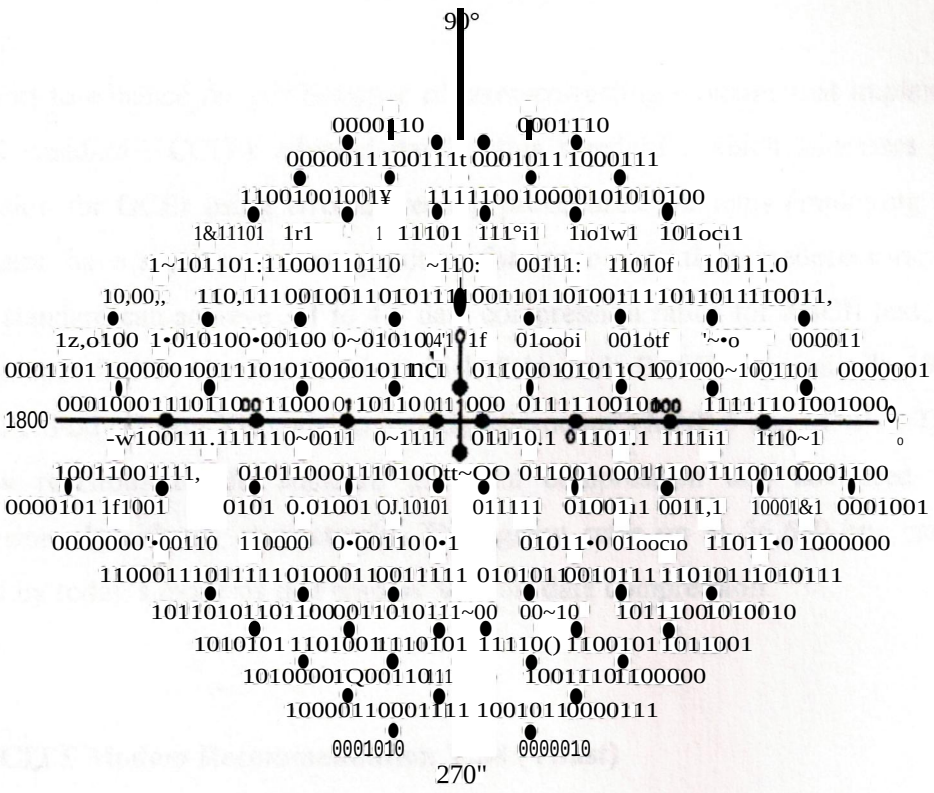


Fig A.9 V.33 signal constellation diagram

A.2.6 CCITT Modem Recommendation V.42

A relatively new modem protocol adopted in 1988 by CCITT is the V.42 standard: Error Correcting Procedures for DCEs. The V.42 standard is designed to address asynchronous-to-synchronous conversions , error detection and correction , and modems that do not have such protocols. V.42's main impetus revolves around a new protocol called Link Access Procedure for Modems (LAP M). LAP Mis similar to the packet switching protocol used in the X.25 standard. An alternative procedure developed by Micricom Inc. has also been adopted by the V.42 standard. This procedure is called Microcom Networking Protocol (MNP). Both MNP and LAP M are discussed later in this chapter.

A.2.7 CCITT Modem Recommendation V.42bis

In an effort to enhance the performance of error-correcting modems that implement the V.42 standard, CCITT adopted the V.24bis standard, which addresses data compression for DCEs using error-correcting procedures. Modems employing data compression have significant throughput pe;±~ over their predecessors. The V.42bis standard can achieve 3:1 to 4:1 data aL:.;i:SSm11 ratios 5 I algorithm specified by the standard is British Te~ 's BTLZ technique. In 1990, the CCITT Study Group XII voted to include Microcom's MNP 5 and MNP 7. These two new revisions to the standard are dara compression and advanced data compression algorithms, respectively. Throughput rates up to 56,000 bps can be achieved by today's modems that employ V.42bis data compression.

A.2.8 CCITT Modem Recommendation V.34 (V.fast)

The International Standards Union - Telecommunications Standardization Sector (ITU - TS and formerly CCITT) established the TR-30 Group (formerly SG XVII) to work on a recommendation for the next generation of =o:em: - V.fast. V.fast was officially adopted in June of 1994 and has been designed V.34. The new standard's speed is 28,800 bps without data compressicz With data compression, the new modems will be able to send asynchronous data two to three times as fast, thus dramatically reducing telephone costs. V.34 will al!:n• a ı it; •• to line conditions an adjust its speed up or down to ensure data imegrity.

Increasing both complexity and speed doesn't come easy ~ h::w There are definite boundaries for both and V.34 pushes these limits..-\ ,, : CC:- 1/C: - enable V.34 to go faster.

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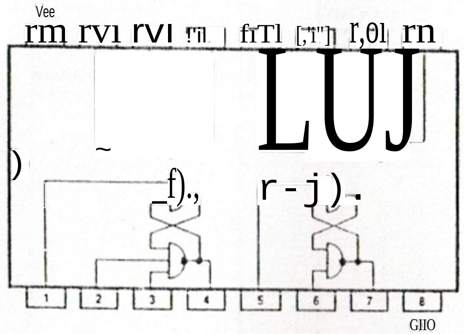

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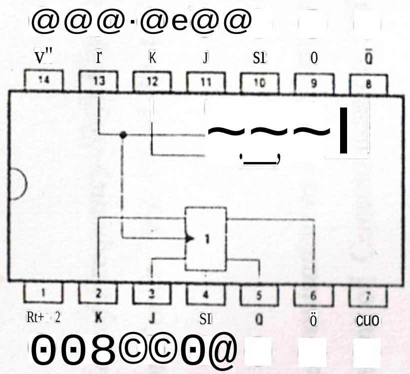

Pin	LS	S
R,6	7	
S	3	3.5

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Impulso di cadenza · Pulsa del reloj

Input tn				Output tn+1	
S	A	J	K	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*	*
H	H	L	L	Qn	Q̄n
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H	H	H	H	Q̄n	Qn

* Dieser Zustand ist nicht stabil
* This state is not stable
* Cet état n'est pas stable
* Questo stato non e stabile
* Este estado no es estable

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