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COMPUTER ENGINEERING
DEPARTMENT

S P E C I A L P R O J E C T R E P O R T

C O M 4 0 0

INTERFACING TECHNIQUES OF RAM DEVICES TO THE MICROPROCESSOR

J U N E 1 9 9 5

ADVISOR:
HALIL ADAHAN.

BY:
AYNUR TURKKAL.
RAMIS YAVAS.

AYNUR TURKKAL

COMPUTER ENGINEERING DEPT.

90220.

RAMIS YAVAS.

COMPUTER ENGINEERING DEPT.

91530.

C O N T E N T S

A C K N O W L E D G E M E N T S

We would like to thanks Mr. Halil ADAHAN for his valuable help in preparation of our report.

P R E F A C E

This report has been written from students who are in COMPUTER ENGINEERING DEPARTMENT at NEAR EAST UNIVERSITY for graduation project.

The purpose of this work is to provide to explain the microprocessor interfacing.

INTRODUCTION

Most microprocessors in a stand alone fashion do not contain substantial memory. To increase the power of a microprocessor we have to interface I/O modules. The interconnection, or linkage, of the parts within this system is called interfacing. Generally, an interface is a shared between two or more devices which utilize information. Other considerations in interfacing include synchronization, direction of data transmission, and sometimes the adjustment of signal levels or models.

Interfacing deals with the synchronization and transmission of data to and from the MPU, and therefore the software as well as the hardware must be considered in great detail.

Generally, data transfers in and out of the MPU over the busses take the form of one of these activities:

1- Memory read
2- Memory write
3- I/O read
4- I/O write
5- Interrupt or reset handling.

When it is said that is input from another device, it means input in relation to the MPU. Likewise, an output would be output from the microprocessor unit. Generally, the microprocessor is the focus of all operations, but in some cases the MPU relases control of the address and data bus so that the peripheral device may access the main system memory directly going to the MPU. This is called DMA (Direct Memory Access).

The processor itself uses MPU, ROM, and RAM externally, and its of importance that the manifactures produce peripheral interface adapters that are compatable with other microprocessors units. These are generally general purpose in that they can be programmed to function as either input or output interface programmable communication devices. Manufactures produce specialised interface component IC (Integrated circuit)'s which are programmable DMA controllers, programmable interrupt controllers, diskette controllers, synchronous data link controllers, and keyboard/display controllers.

General purpose of interfacing, microprocessor can READ/WRITE using memory (ROM or RAM) capacities or more memory capacities.

CHAPTER 1

THE MICROPROCESSORS IN GENERAL

A microprocessor may be briefly defined as a very large scale Integration (VLSI) chip that performs the tasks of a control processing unit of a microprocessor or other automatic control system. Microprocessors (except the 8080) require a +5 V direct current (dc) regulated power supply. Microprocessors are commonly classified as either 4-,8-,16-,or 32-bit units.

The bit size of a microprocessor is sometimes referred to as its world size. The width of the accumulator register is a good clue as to the word size of a microprocessor. The 8080/8085, 6800/6502 and Z80 are common 8-bit microprocessors. The 8086, 8088, 68000 and 65816 are typical 16-bit MPUs. The 80386 and 68020 are examples of advanced 32-bit microprocessors. Microprocessors transfer data or instructions between the MPU and memory (or I/O) via a bidirectional data bus. The 6800, 6502, Z80, and 8088 are processors that use 8-bit external data busses. Many 8080 family members multiplex either address or control information or the data lines part of the time. Most order microprocessors (8080/8085, 6800, 6502) use 16-bit address busses which can address only 64 KB of memory. Most microprocessors would feature some or all of the following control lines.

1- Clock lines
2- Read/Write lines
3- Input output lines
4- Interrupt lines
5- Reset lines
6- Bus control lines
7- Cycle Status lines.

INTERNAL REGISTERS

Program Counter:

The program counter (PC) isa the register that holds the address of the reset program instruction. The width of the program counter is the same as the width of the address bus. The program counter typically contains 16 bits in 8-bit microprocessors but is wider in 16- and 32-bit MPUs.

Accumulator:

The accumulator is the register(s) associated with the ALU operations and sometimes I/O operations. It may be 8, 16 or 32

bits wide. The 8080/8085, 6800, and 6502 MPU's all have 8-bit accumulators. Some processors (68000 and Z80) have only general purpose registers that may be used as accumulators.

Status Register or Flags:

The status register is available on all microprocessors. The individual bits in the register are called flags. The conditions of the flags are generally associated with ALU operations and are used by subsequent branch and jump instructions for decision making.

General Purpose Registers:

General purpose registers may be used to temporarily store data or hold an address. They are not assigned a specific task. In 8-bit microprocessors, general purpose registers cannot function as an accumulator in ALU and I/O operations. However, 16-bit MPUs usually allow general purpose register to be used as accumulators.

Index Register:

The index register is used to hold the address of an operand when the indexed address mode is used (8080/8085, 6800, 6502, Z80, 8086). General-purpose registers are used as index registers on the Z80 and 68000 microprocessors.

Stack pointer Register:

The Stack pointer (SP) is a specialized register that keeps track of the next available memory location in the stack. The stack is reserved area in RAM used for temporary storage of data, return addresses, and content of registers.
The stack is used during subroutine calls and interrupts.

ADDRESSING MODES:

An addressing mode is the technique used to fetch the desired operand during the execution of an instruction.
Induvidual microprocessors may not use all of the addressing modes listed below:

1 - Inherent (implied) addressing mode
2 - Immediate addressing mode
3 - Extended or absolute addressing mode
4 - Register addressing mode
5 - Register indirect addressing mode
6 - Index addressing mode
7 - Zero page (direct) addressing mode
8 - Relative addressing mode
9 - Based addressing mode
10- Based index addressing mode
11- String addressing mode
12- I/O addressing mode
13- Status register addressing mode.

Generally, the more modern 16-bit computers have powerful and flexible addressing modes.

CHAPTER II

THE MOTOROLA 6800 MICROPROCESSOR

The motorola MC6800 is an 8-bit microprocessor functionally, the data bus is 8-bit and the address bus is 16-bits.
An MPU chip such as the 68HC11,includes an 8-bit microprocessor a timer, ROM, RAM, and A/D converter, and an on-chip oscillator the functionalities providing also programmable I/O lines and an EPROM.

The MC68000 is an advanced 16-bit microprocessor other members of the motorola family are the 68HC000 (CMOS), 68008, 68010, 68020, and 68030. The 68000 MPU features and 32 bit internal architecture with a 16 bit external data bus and it can address 16 MB of memory. The 68010 is an updated 16 bit external/32 bit internal virtual memory.

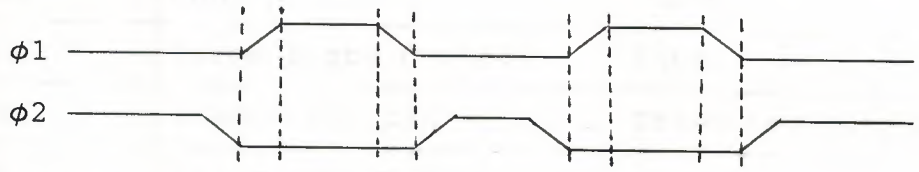
The 68020 supports a 32 bit internal/external virtual memory is a advanced feature of MPU's.
Virtual memory means that a programmer can write programs as it memory capacity is un limited.
Type of PC programs that use virtual memory.

1- WINDOWS
2- ACAD
3- MICROSOFT EXEL
4- 3D STDIO
5- COREL DRAW
6- MATHEMEDICA
7- MAT LAB.

The virtual memory technique permits program to be larger than the capacity of the main memory. The extra part of the program is stored on a secondary storage medium (DISK).

CLOCK $\phi 1$, $\phi 2$

$\phi 1$: Supplies the required clock cycles to increment the internal register.
$\phi 2$: Provides the necessary clock cycles to fetch and execute an instruction.



ROM (READ ONLY MEMORY)

ROM is a read only memory containing monitor subroutines + display routines + timer control subroutines.
It is medium-scale integration (MSI).

RAM (RANDOM ACCESS MEMORY)

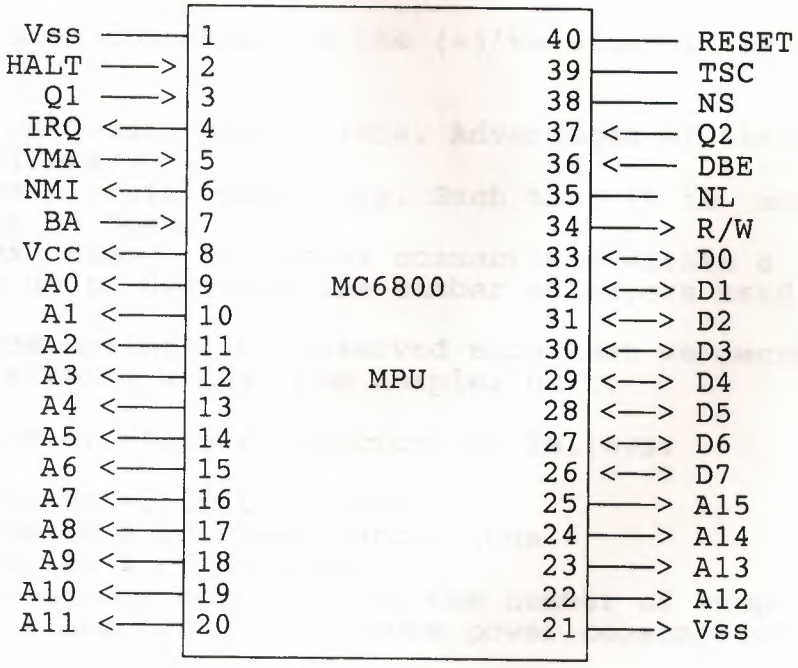
Where the programs are executed.

PIA (PERIPHERAL INTERFACE ADAPTER)

PIA has two I/O parts. Each port is 8-bit ports A & B can be programmed to interface I/O devices.

THE 6800 PIN DIAGRAM

The motorola 6800 is an 8-bit microprocessor placed in 40 pin DIP (Dual in Line Package).



PIN NAME	DESCRIPTION	STATE, TYPES
AO - A15	Address lines	Tristate, output
D0 - D7	Databus Lines	Tristate, Bidirectional
HALT	HALT	Input
TSC	Three State Control	Input
R/W	Read/Write pin	Tristate, output
VMA	Valid Memory Address	output
DBE	Data bus enable	input
BA	Bus Available	Output
IRQ	Interrupt Request	Input
RESET	RESET Pin	Input
NMI	Non-maskable interrupt	Input
ϕ1, ϕ2	Two non overloping clock signals	Input
Vss, Vcc	Power Inputs	Input

PIN DEFINITIONS

GROUND (Vss) (Pins 1 and 21)

These pins are connected to the (-)'ve side of +5V dc power supply.

There are two ground connections. Advantages of these connections as follows:
1- Decreases circuit complexity. Such that it is easier for the designer to trace.
2- Decreases number of cross connections within a circuit. This allows us to decrease the number of layers used within a circuit.
3- Power consumption is preserved such that we decrease the capacitive effects within the complex unit.

Disadvantages of these connections as follows:

1- Increases circuit complexity
2- Increases # of cross connections
3- Increases # of pins used.

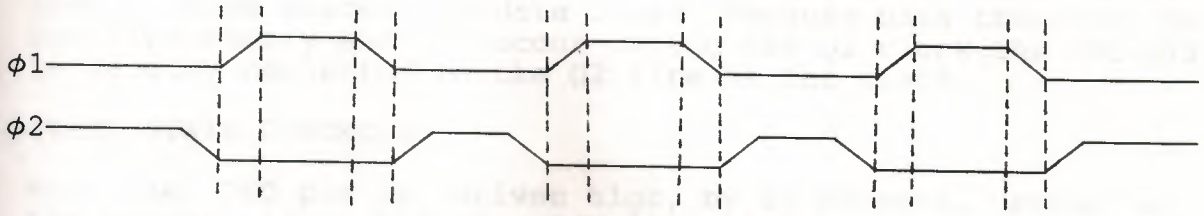
Therefore we occupy more space & the number of components used with increase, leading to more power consumption.

HALT (Pin 2)

When the halt input is activated by a LOW, the 6800 MPU enters the halt mode. In this mode the tri-state lines go to their high impedence state and the processor stops executing instructions. This input could be used for "single stepping" in a program in the debugging process. The halt input is disabled by connecting it to +5 V dc.

CLOCKS (ϕ1 and ϕ2) (Pins 3, 37)

These two input pins receive nonoverloping clock signals from the external clock circuity.



INTERRUPT REQUEST LINE (IRQ) (Pin 4)

When the IRQ is activated by a LOW, the MPU will complete the current instruction, push all programmable registers to the stack, set the I flag (interrupt flag) and jump to the interrupt service routine pointed at address FFF8 H and FFF9 H. The IRQ can be masked.

VALID MEMORY ADDRESS (VMA) (Pin 5)

When the VMA output goes it signals other system devices that the address on the address bus is valid.

NON-MASKABLE INTERRUPT (NMI) (Pin 6)

When the NMI goes LOW, its response is similar to the IRQ. The NMI is nonmaskable and its vector address is found in memory locations FFFC H and FFFD H. The connects of FFFC H and FFFD H point to the start of nonmaskable routine.

BUS AVAILABLE (BA) (Pin 7)

When the BA output goes HIGH, it signals the external devices that the microprocessor has stopped executed the instructions because of the wait instruction (WAI) or the HALT interrupt.

The BA control line provides a method of telling the external devices that the MPU's data and address bus are three stated and may be used as DMA operations.

READ WRITE (R/W) CONTROL (Pin 34)

The R/W output is a control line that signals the external devices (i.e RAM, ROM etc.) whenever the MPU is reading or writing.

A high output signals a READ, and a LOW output signals the write operation.

DATA BUS ENABLE (DBE) (Pin 36)

The DBE input controls the data bus drivers. A high output on the DBE pin enables the data lines, while a low input disables or three states the data lines. Because data transfer to and from memory and I/O occur during the Q2 clock,the DBE pin is usually connected to the Q2 line of the clock.

THREE STATE CONTROLS

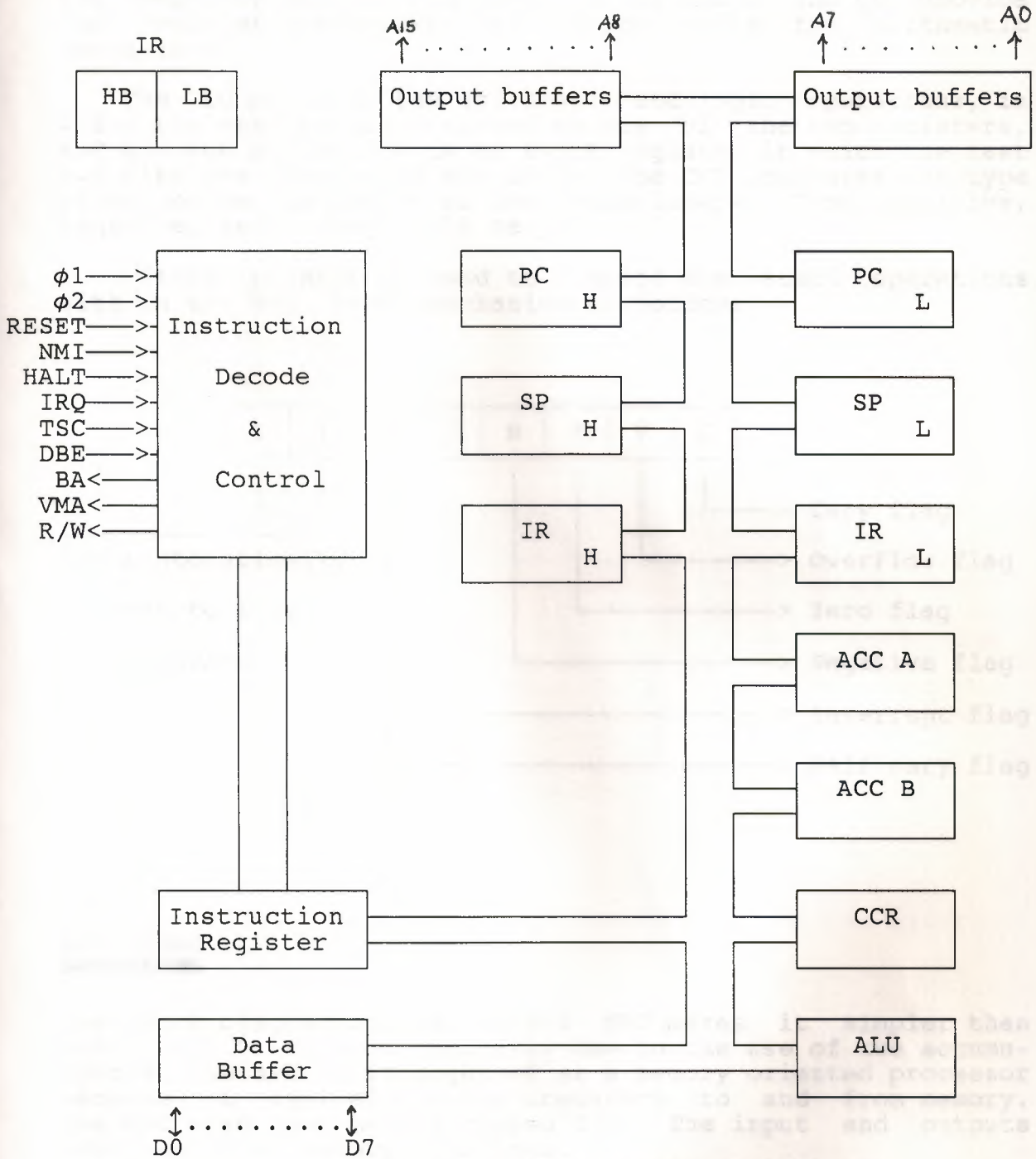
When the TSC pin is driven high, by an external device all the address lines and the R/W line will be three stated. The TSC is used in DMA configurations.
When DMA is not used, the TSC pin is grounded.

RESET LINE (RESET) (Pin 40)

When the reset pin is driven from to low, the MPU sets the I flag to 1, jumps to the reset routine. The RESET input is typically used to initialize or reset the system.

THE 6800 ARCHITECTURE

A block diagram of the internal organization of 6800 is given below.

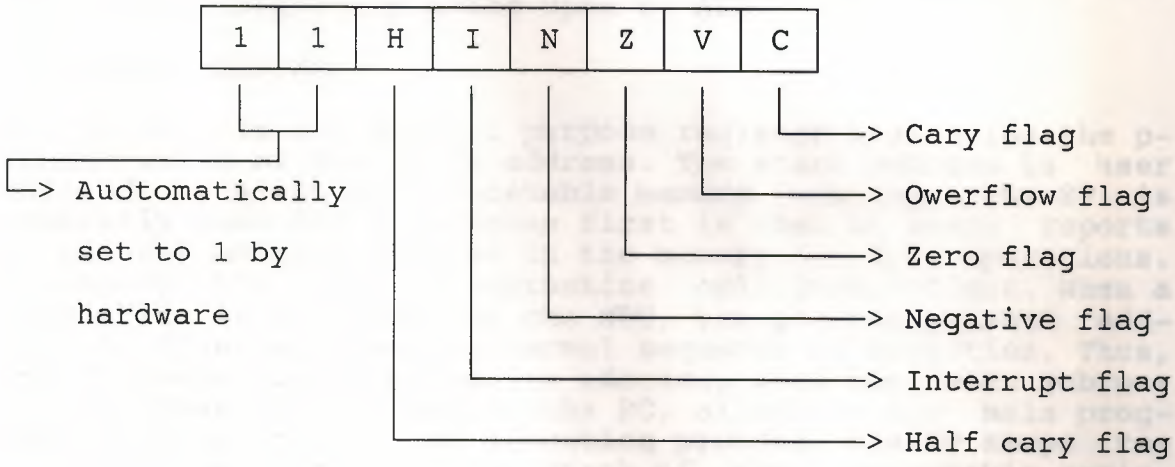


FUNCTIONAL BLOCK DIAGRAM OF 6800 MPU

The MPU has an 8-bit three state buffered data bus (D0-D7). There are 16-bit buffered address bus. The MPU has 16-bit program counter, a 16-bit stack pointer, and a 16-bit IR. The temporary storage registers ACC A, ACC B, and CCR provide the register (temporary) allocation units for arithmetic operations.

The ALU performs the arithmetic and logic operations, in which the results are returned to any of the two registers, ACC A, ACC B, the CCR is an 8-bit register in which the test two bits are internally set of 1. The CCR indicates the type of the number in either of the accumulators (Type: positive, negative, zero, cary, half cary).

Stack pointer is used to control the stack operations with in the MPU. Stack mechanism as follows.



REGISTERS

The block diagram of the MC6800 MPU makes it simpler than 8085 unit. This is primerly due to the use of two accumulators. The MPU is throught of as a memory oriented processor because it typically makes transfers to and from memory. The MPU also uses memory mapped I/O. The input and outputs are treated as memory locations.

The 6800 MPU registers are;

1-) The two bits accumulators (ACC A, ACC B) are the focus

of a large shane of the microprocessor operations. Accumulator operation include arithmetic, logic, load, store, input and output. The second accumulator ACC B is just a general purpose register but a real accumulator in that all operations that can be performed in ACC B.

2-) The program counter(PC) is a 16-bit register that holds the address of the next instruction to be executed.

3-) The stack pointer(SP) is a 16-bit general purpose register. The SP from a 16-bit address defines the top of the stack in the RAM.

4-) The index register(IR) is a general purpose register. Its primary use is to point and modify address.

5-) The condition code register (CCR) is an 8 bit register that contains the 6 flags which indicates the type of either the data or magnitude acted upon by ALU.

THE STACK POINTER

The SP is a 16 bit general purpose register that holds the present value of the stack address. The stack address is user defined by a set of allocatable memory locations. The SP is generally used for 2 purposes first is that it keeps reports of pointer address defined in the memory for I/O operations. Secondary it's used in subroutine call instructions. When a subroutine is activated by the MPU, the process present address is diverted from its normal sequence of execution. Thus, the SP keeps record of return address, such that when subroutine address is returned to the PC, allocates the main program address. In such an execution process, the SP keeps record of the address in the stack of the programmable registers.

FLAGS

The MC 6800 uses six condition code flags. Thus is illustrated below

```
          1 0 0 0   1 0 0 0
          1 0 0 0   1 0 0 0
          ---------------------
STACK --> | 1  0 0 0 0   0 0 0 0 |
          ---------------------
```

These flags are used in branch instructions. Hence, each conditional and unconditional branch instruction is decided based on these six flags operated by the ALU.

Condition code register only reflects the condition of either ACC A or ACC B.

THE ARITHMETIC & LOGIC UNIT

The ALU is the heart of the microprocessor. It performs all arithmetic and logical operations. The result of the operations performed is stored either of the accumulators. The ALU performs such operations as adding, subtructing, comparing AND'ing, OR'ing, and XOR'ing.

INSTRUCTION DECODER

The instruction decoder interprets results from the instruction register. Based on these inputs, the instruction decoder directs the control section for execute the instruction.

THE INTERRUPT and CONTROL UNIT

The MPU will accept the interrupt signal from the interrupt input (INTR). Interrupts are generally classified to two types. First one is the software driven interrupt, which is activated by the MPU, and the hardware interrupt is activated using a hardware input using external devices.

CHAPTER III

MICROPROCESSOR INTERFACING

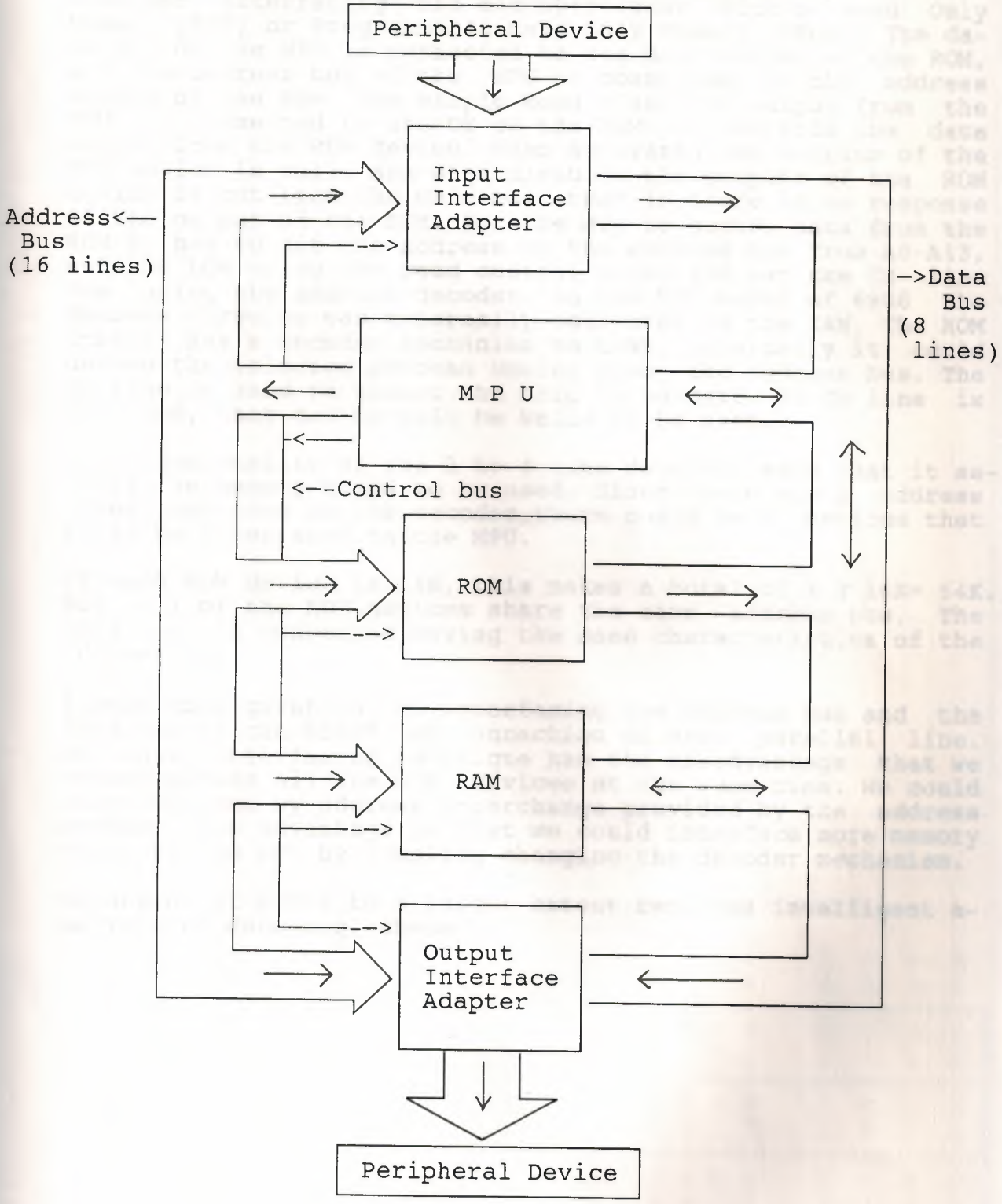
Our topic is microprocessor interfacing. Interfacing means that relation between the MPU and the memories. Introduction division is including the microprocessor interfacing.

General purpose of interfacing, microprocessor can write/read to/from memory (RAM/ROM) capacities or more memory capacities.

The block diagram of microprocessor based design. Suggests that the MPU, ROM, RAM, input interface adapter, and output interface adapter are separate devices. This may or may not be true depending on the specific system. It is quite common for manufacturers to produce peripheral interface adapters that are compatible with their microprocessor units. These are usually general-purpose in that thay can typically be programmed to function as either an input or an output interface device.

Some manufacturers integrate RAM and I/O ports or ROM and I/O ports on the same IC to decrease system component numbers. Manufacturers also produce specialized interface components in IC form. Some of these specialized components include programmable communications interfaces, programmable DMA controllers, programmable interrupt controllers, diskette controllers, synchronous data link controllers, CRT controllers, and keyboard/display controllers.

BLOCK DIAGRAM OF MICROPROCESSOR-BASED DESIGN



INTERFACING WITH 16Kx8 ROM

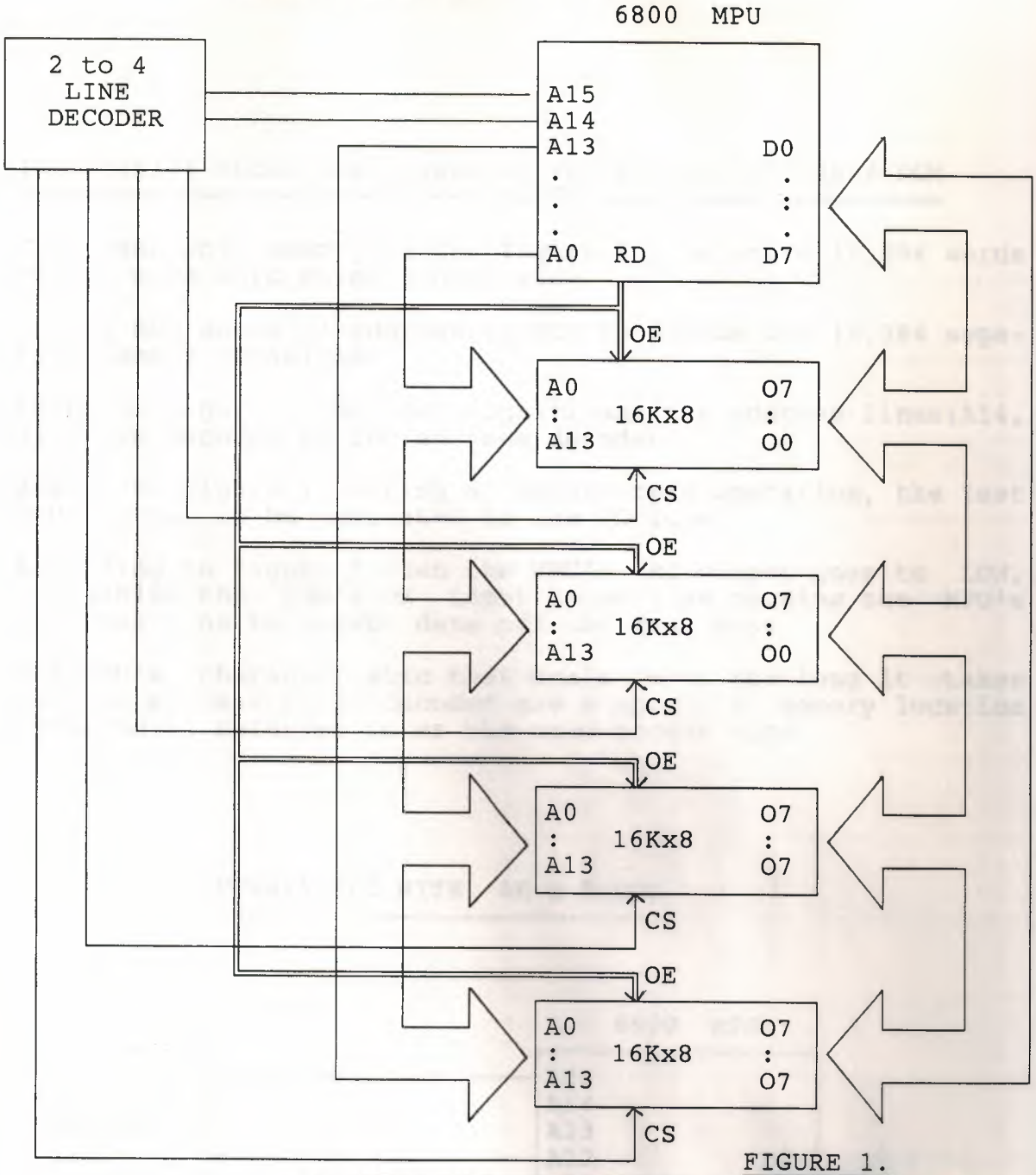


FIGURE 1.

ADDRESS MAP FOR FIGURE 1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#2	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#4	C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Information about the figure of interfacing of 16Kx8 ROM

The read-only memory in the figure 1 can store 16,384 words words, each word being 8 bits wide.

A 16K ROM needs 14 address inputs to decode the 16,384 separate memory locations.

Refer to figure 1 the most significant two address lines(A14, A15) are decoded by the address decoder.

Refer to figure 1 during a memory read operation, the last MPU output to be activated is the RD line.

According to figure 1 when the MPU's RD output goes to LOW, it enables the ROM's OE input as well as causing the MPU's data bus pins to accept data off the data bus.

The ROM's characteristic that deals with how long it takes for the address to be decoded and a specific memory location accessed is referred to as the read access time.

INTERFACING WITH 4K x 8 ROM

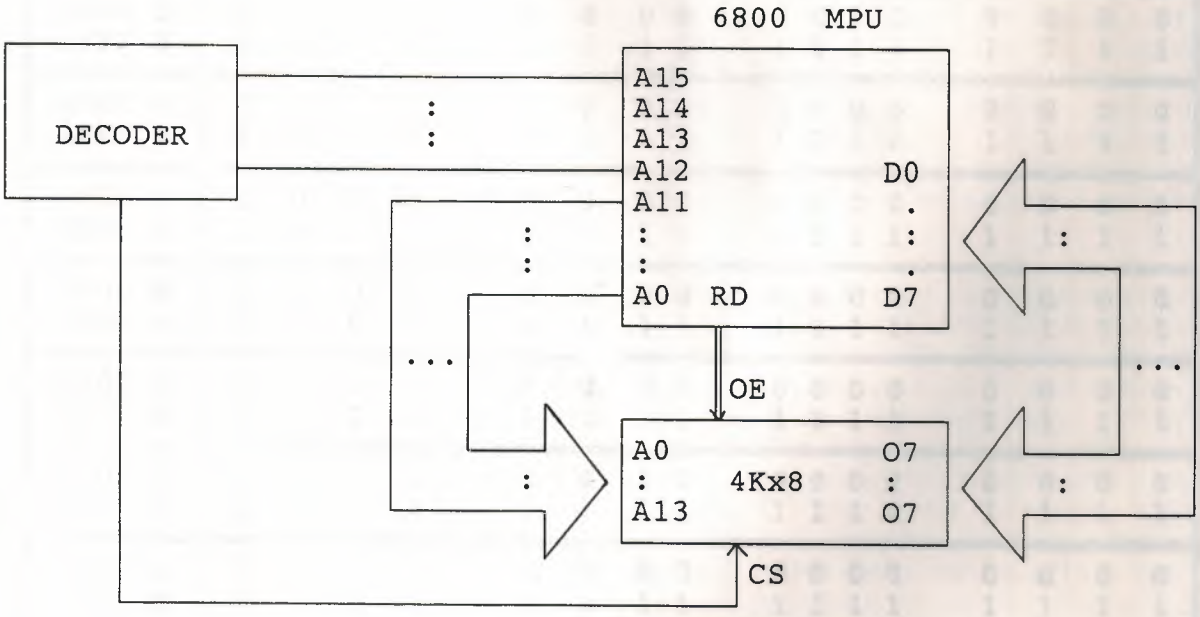


FIGURE 2.

ADDRESS MAP FOR FIGURE 2

	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8FFF H	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
9000 H	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
9FFF H	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
A000 H	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
AFFF H	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
B000 H	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CFFF H	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
D000 H	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
DFFF H	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
E000 H	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
EFFF H	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
F000 H	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Information about the Figure 2 of interfacing of 4Kx8 ROM

All 8 data bus lines are connected to the output terminals (O0-O7) of the ROM. The single read output (RD) goes from the MPU to the output enable (OE) input of the ROM.

The least significant 12 bits of the address bus (A0-A11) are connected to the 4Kx8 ROM. The ROM IC's built-in decoder can access any one of 4096 (4K) 8-bit read-only memory words using the 12 address inputs. The most significant 4 address lines (A12-A15) goto a combinational logic element called an address decoder. To access and read data from the ROM the MPU must:

1- Set address on address lines A0 through A11.
2- Set OE LOW using the read control line.
3- Set CS LOW using the address decoder and chip-select line.

Assume the MPU wants to access memory location 0000H (0000 0000 0000 0000). The least significant 12 bits applied directly to the ² ROM's decoding circuitry via address lines A0 through A11. The most significant 4 bits (A12-A15) also are part of the address. These are decoded by an address decoder. If A12 through A15=0000 ,then the address decoder will output a LOW which will enable the chip-select (CS) input of the ROM in the figure 2.

The memory map drawn in figure might help explain thejob performed by the address decoder. The memory map symbolizes a unit having 64K (actually 65,536) memory locations. This memory map is divided into sixteen 4K segments. The task of the address decoder is to help the MPU access only one of the 4K segments at a time. If the 4 inputs to the address decoder were 0000, then segment 0 (memory locations 0000-0FFFH) would be accessed. However, if the input to the address decoder were 0001, then segment 1 (memory locations 1000-1FFFH) would be accessed, etc. In summary, the most significant 4 address lines select a segment ofmemory whereas the least significant 12 bits determine the specific memory location within that 4K segment.

When interfacing the MPU with ROM, the important considerations are addressing and timing. Addressing has been discussed. According the figure 2 ,address lines A0 through A11,activate the address inputs of the ROM while A12 through A15 are decoded by the address decoder activating the chip-select (CS) input of the ROM. A short time later the read output (RD) of the MPU enables the output enable of the ROM. Stored data is placed on the data bus and collected off the data bus by the MPU. After the address lines have settled to their respective logic levels and the CS ROM input has been activated, it takes a given amount of time to access the memory word. This is called the read access time and is a characteristic of the particular ROM or PROM being used. It is the time required for the internal ROM decoders to locate the correct byte in memory.

INTERFACING WITH RAM

Read/write devices that the MPU access are commonly refered as RAM. RAM's are divided into 2.

1-) Static RAM characteristics
   a) Basic elements are the flip flops
   b) It occupies larger area
   c) Faster
   d) It occupies more power to operate

2-) Dynamic Memories (Capacitors)
   a) Can be constructed densly
   b) Slower because of its capasitive effects
   c) Required periodic refreshing. 50 timed/sec.

The interfacing technique is similar to the ROM interface, except that R/W control line is added to the circuit. The data bus could be programmed in two ways.
The decoder mechanism works in the same way, such that many RAM modules could be interfaced to the MPU by the module select line (MS).

If we are to write to RAM device, we bring the RD line and the R/W line LOW. The I/O ports of the RAM are internally programmed as inputs. Hence the MPU selects the data to be written to the required memory location and places the address on the address bus. To activate the RAM device to be used its selected by address lines A12-A15. The decoder selects the appropriate device to be used at the decoder output. Similarly to read from the RAM, initially WR line is held HIGH so that the I/O ports of the RAM are programmed as outputs.

Data to be acted on is fetched from the data bus of the RAM, which is selected from the address line inputs. Some discussions for the expansion of the RAM is also valid for the interfacing of RAM.

INTERFACING WITH 4K x 8 RAM

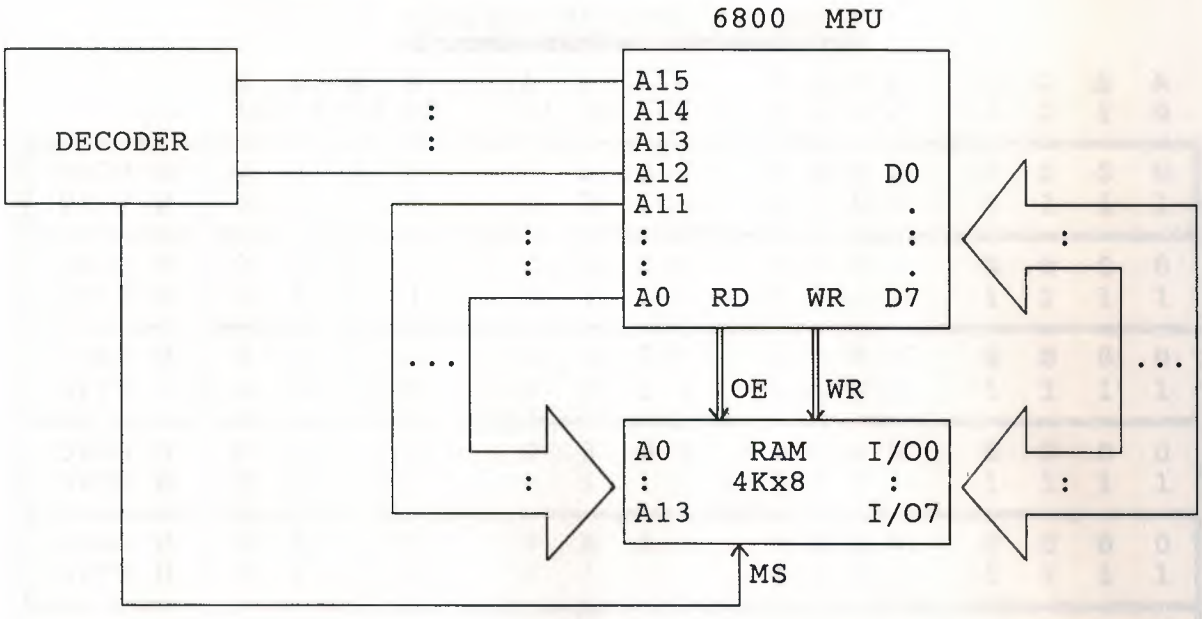


FIGURE 1.

The MPU and the RAM section of a system which is diagrammed figure1. The RAM is organized as a 4K (4096 words)x8 bit unit. It contains 4096 words each 8 bits wide. It is common for this large a static RAM unit to be made up of many RAM ICs. One such 4K x 8 bit memory module contains 32 static 1024 x 1 bit RAM IC's. The memory module or memory card also contains about 10 extra ICs for gating and buffering. This 4K x 8 bit RAM memory unit diagramed as a block in above is in itself a complex system.

As with the ROM, the address decoder in figure 1 will have the task of generating an enable signal on the device select line. The address decoder will send a LOW pulse to the module-select (MS) input to enable the RAM only when the most significant 4 address lines (A12-A15) equal 0010 .As with the ROM the decoding of the least significant 12 ^{2} address lines (A0-A11) is performed by RAM decoding circuitry.

The data bus becomes a two way 8-bit path for data read from or written into the RAM in the figure 1.The least significant 12 MPU address lines go directly to the address inputs of the RAM module via the address bus. The most significant 4 MPU address lines are connected to the address decoder. The write output (WR) of the MPU is connected via the write control line to the R/W input of the RAM. Note that this RAM input is a read/write input. This means that when the MPU is not enabling the write output with a LOW, the WR terminal puts out a HIGH which specifies a read operation to the RAM. The MPU's read (RD) output is connected via the read control line to

the output enable (OE) of the RAM. A LOW on the read control line will enable the outputs of the RAM module.

ADDRESS MAP FOR FIGURE 1

	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8FFF H	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
9000 H	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
9FFF H	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
A000 H	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
AFFF H	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
B000 H	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CFFF H	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
D000 H	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
DFFF H	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
E000 H	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
EFFF H	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
F000 H	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The MPU's address lines are set to a valid address, and then the read output(RD) goes LOW. The data bus goes from a tree-state to an input condition. The MPU is ready to accept data of the data bus. The RAM's module select(MS) and output enable (OE) inputs are both driven LOW or enabled by the address decoder and the read control line from the MPU. The read/write(R/W) input is held HIGH or in the read mode. Shortly after the output enable (OE) goes LOW, the data outputs are activated. Stored data is placed on the data bus by the outputs of the RAM. As on a ROM, the read access time is an important characteristic of the RAM. The maximum read access time might range from 250 to 1000 ns for common static RAMs.

INTERFACING WITH 2K x 8 RAM

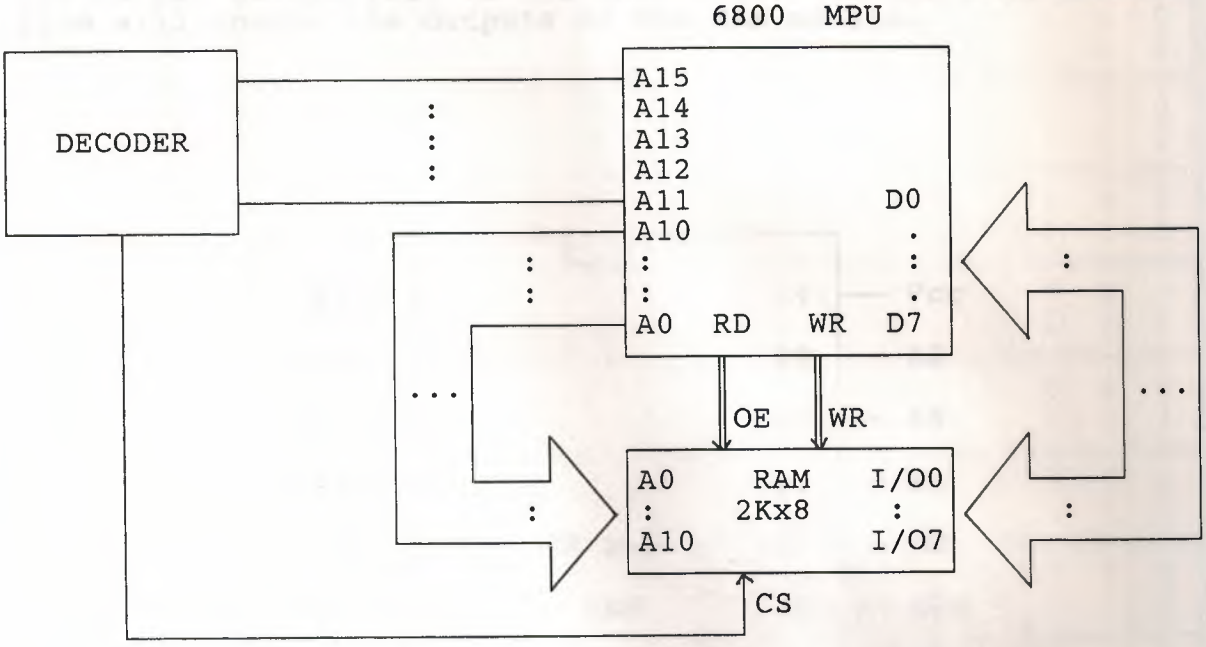


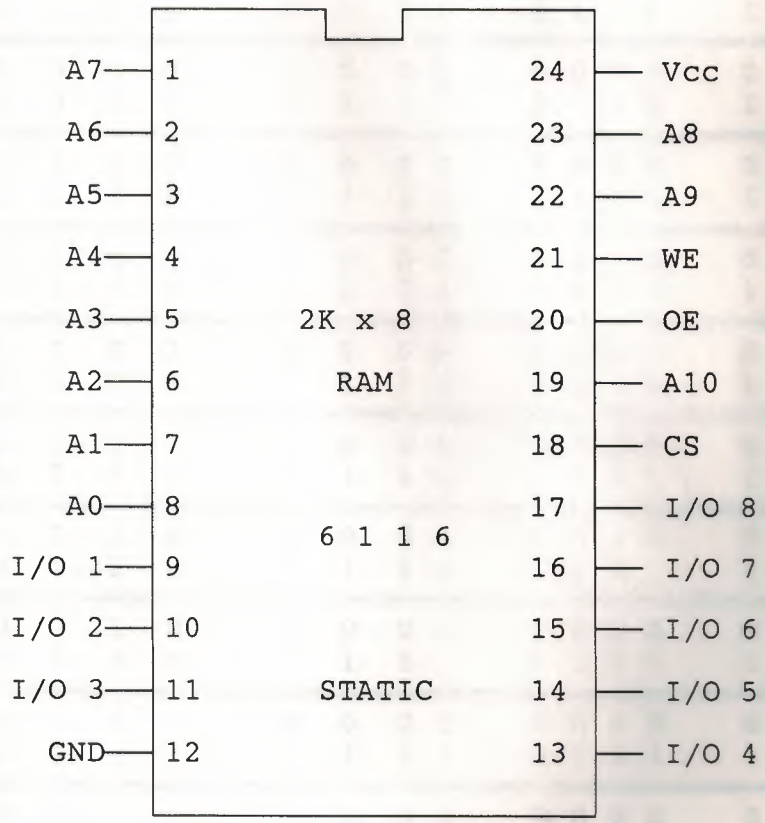
FIGURE 2.

The MPU and the RAM section of a system which is diagrammed in the figure 2. The RAM is organized as a 2K (2048 words)x8 bit unit. It contains 2048 words each 8 bits wide. It is common for this large a static RAM unit to be made up of many RAM ICs. One such 2K x 8 bit memory module contains 32 static 1024 x 1 bit RAM IC's. The memory module or memory card also contains about 10 extra ICs for gating and buffering. This 2K x 8-bit RAM memory unit diagrammed as a block in figure 2 is in itself a complex system.

As with the ROM, the address decoder in figure 2 will have the task of generating an enable signal on the device select line. The address decoder will send a LOW pulse to the

module-select (MS) input to enable the RAM only when the most significant 5 address lines (A11-A15) equal 0010 .As with the ROM the decoding of the least significant 11 ² address lines (A0-A10) is performed by RAM decoding circuitry.

The data bus becomes a two way 8-bit path for data read from or written into the RAM in the figure 2.The least significant 11 MPU address lines go directly to the address inputs of the RAM module via the address bus. The most significant 5 MPU address lines are connected to the address decoder. The write output (WR) of the MPU is connected via the write control line to the R/W input of the RAM. Note that this RAM input is a read/write input. This means that when the MPU is not enabling the write output with a LOW, the WR terminal puts out a HIGH which specifies a read operation to the RAM. The MPU's read (RD) output is connected via the read control line to the output enable (OE) of the RAM. A LOW on the read control line will enable the outputs of the RAM module.



PIN DIAGRAM OF 2K x 8 RAM.

ADDRESS MAP FOR FIGURE 2

	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
27FF H	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
2800 H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
37FF H	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
3800 H	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
47FF H	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
4800 H	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
57FF H	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
5800 H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
67FF H	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
6800 H	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
77FF H	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
7800 H	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
87FF H	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
8800 H	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
8FFF H	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
9000 H	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
97FF H	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
9800 H	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
9FFF H	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
A000 H	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
A7FF H	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
A800 H	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
AFFF H	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
B000 H	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
B7FF H	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
B800 H	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C7FF H	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
C800 H	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
CFFF H	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
D000 H	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
D7FF H	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
D800 H	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
DFFF H	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
E000 H	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
E7FF H	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
E800 H	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
EFFF H	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
F000 H	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
F7FF H	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
F800 H	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

C O N C L U S I O N

After the successfull interfacing of devices (ROMs or RAM)s, the microprocessor can read/write to/from memories(ROMs or RAMs). We can interface more memory units to the MPU then its maximum capacity. By using a decoder we could select any memory unit to be interfaced to the MPU providing easy access to all memory units.

APPENDIX A

INTERFACING WITH 1Kx8 RAM

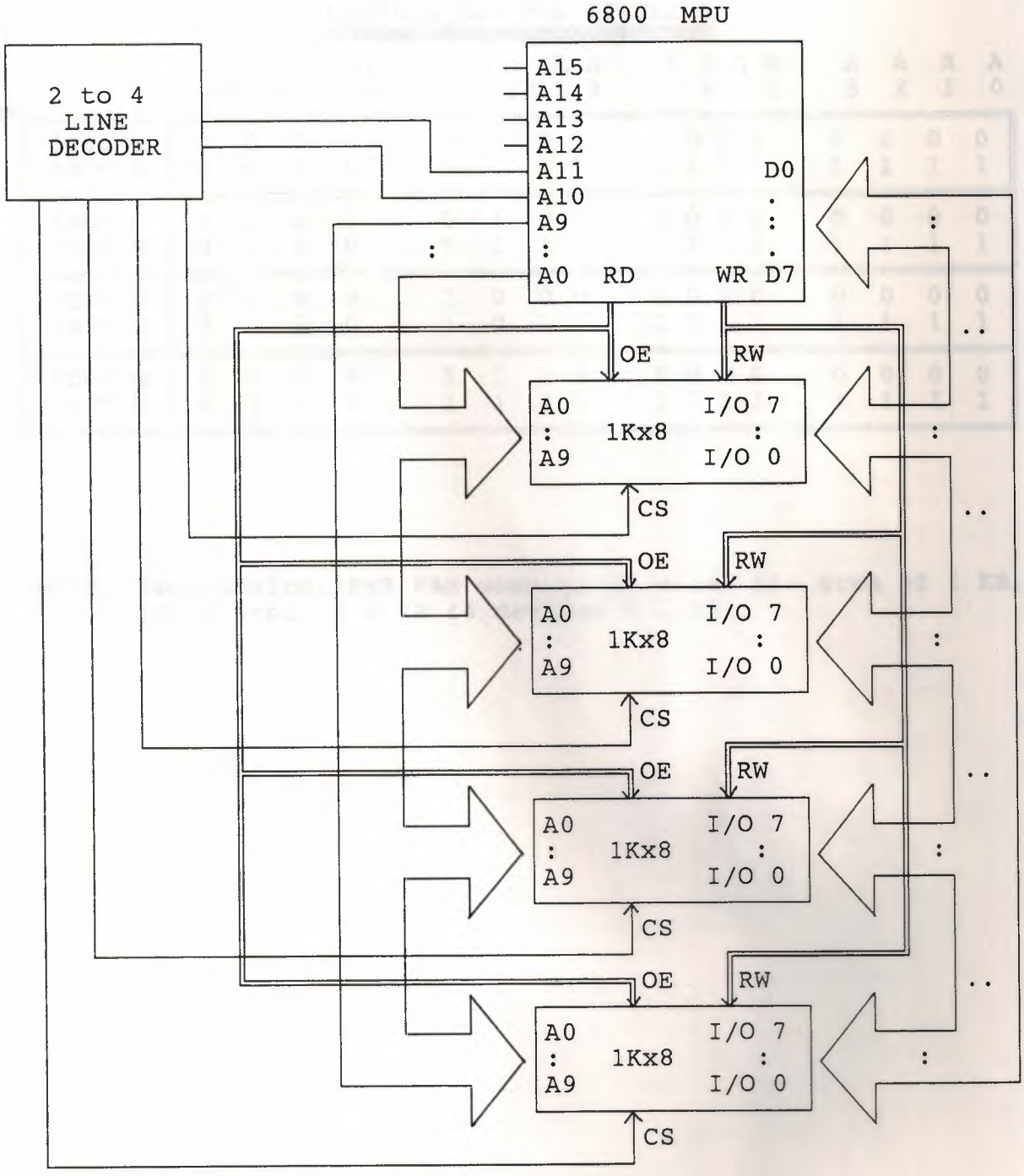


FIGURE 1.

ADDRESS MAP FOR FIGURE 1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	03FF H	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
#2	0400 H	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
#3	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0BFF H	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
#4	0C00 H	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(1Kx8 RAM memory) is using the area of 1 KB.
Total area is 4 KB (4 devices x 1 KB).

INTERFACING WITH 1Kx8 RAM

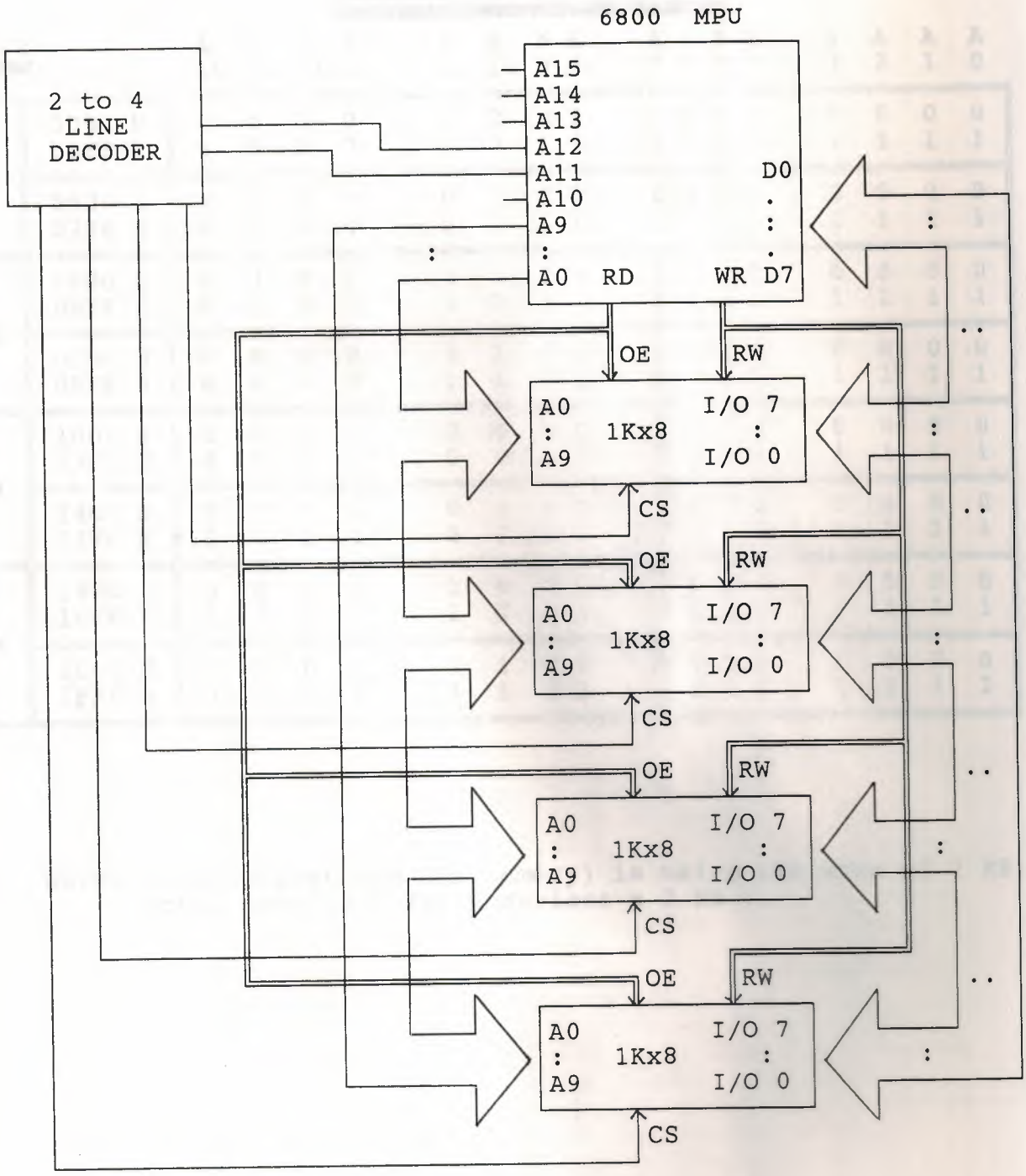


FIGURE 2.

ADDRESS MAP FOR FIGURE 2

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	03FF H	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	0400 H	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
#2	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0BFF H	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	0C00 H	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
#3	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	13FF H	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	1400 H	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
#4	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1BFF H	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	1C00 H	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(1Kx8 RAM memory) is using the area of 2 KB.
Total area is 8 KB(4 devices x 2 KB).

INTERFACING WITH 1Kx8 RAM

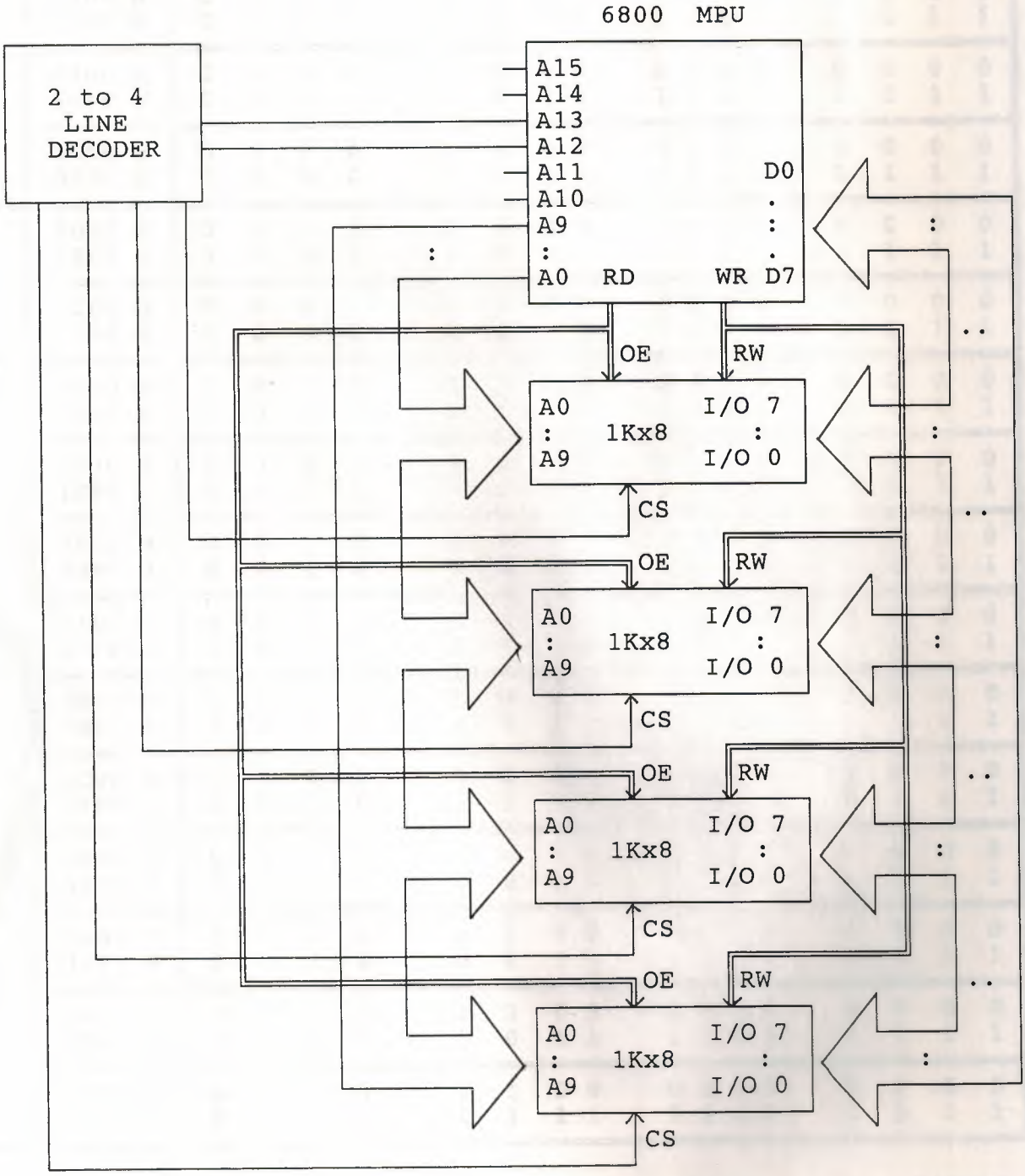


FIGURE 3.

NEAR EAST UNIVERSITY
LIBRARY
1988 – LEFKOSA

ADDRESS MAP FOR FIGURE 3

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	03FF H	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	0400 H	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0BFF H	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	0C00 H	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
#2	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	13FF H	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	1400 H	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1BFF H	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	1C00 H	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	23FF H	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	2400 H	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
	27FF H	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	2800 H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	2BFF H	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	2C00 H	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
#4	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	33FF H	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	3400 H	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	37FF H	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	3800 H	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	3BFF H	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	3C00 H	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(1Kx8 RAM memory) is using the area of 4 KB.
Total area is 16 KB(4 devices x 4 KB).

INTERFACING WITH 1Kx8 RAM

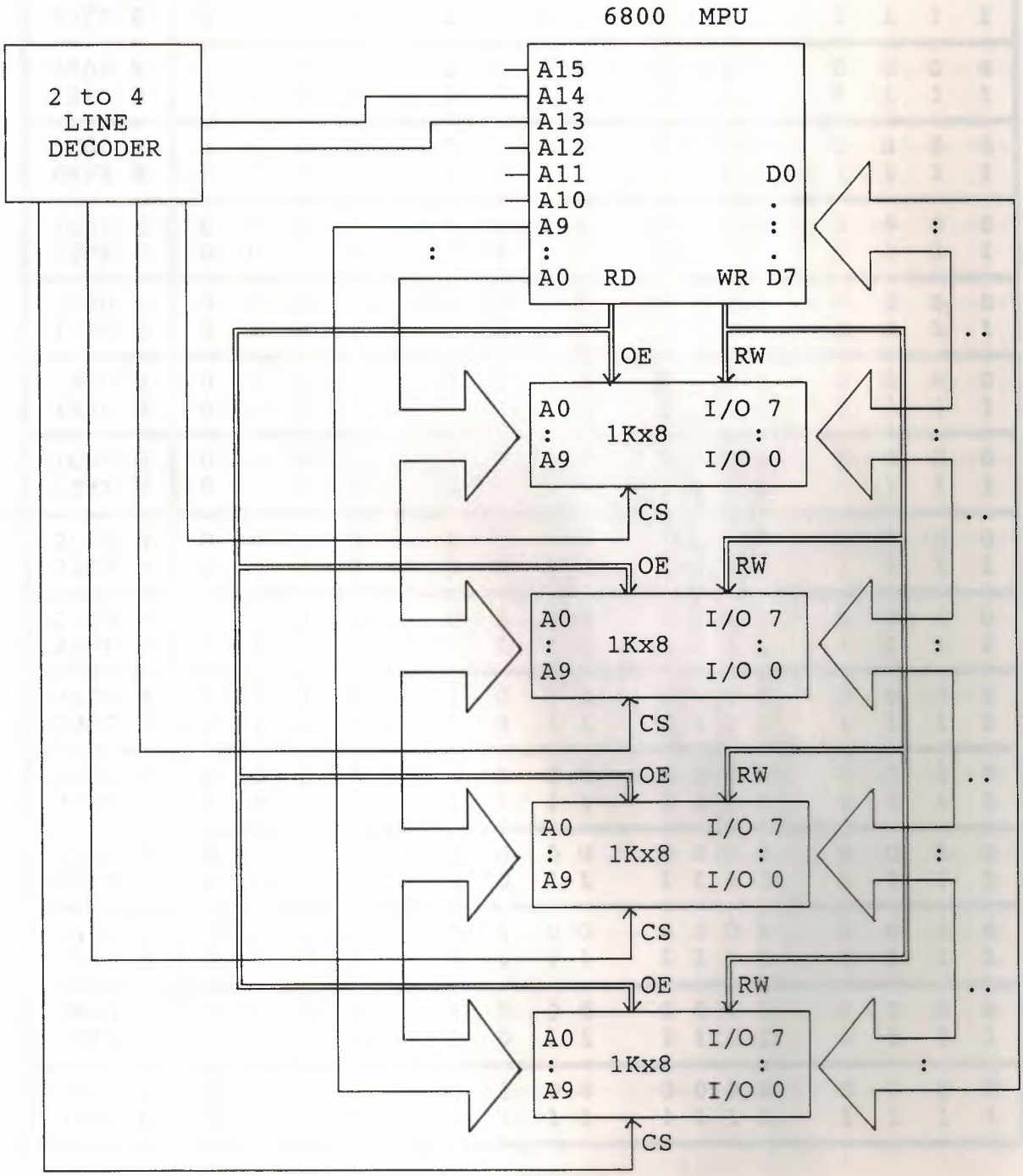


FIGURE 4.

ADDRESS MAP FOR FIGURE 4

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	03FF H	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	0400 H	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0BFF H	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	0C00 H	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	13FF H	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	1400 H	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1BFF H	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	1C00 H	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#2	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	23FF H	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	2400 H	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
	27FF H	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	2800 H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	2BFF H	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	2C00 H	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	33FF H	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	3400 H	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	37FF H	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	3800 H	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	3BFF H	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	3C00 H	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#3	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	43FF H	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	4400 H	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	47FF H	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	4800 H	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	4BFF H	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	4C00 H	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	53FF H	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	5400 H	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	57FF H	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	5800 H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	5BFF H	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	5C00 H	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#4	6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	63FF H	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	6400 H	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
	67FF H	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	6800 H	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	6BFF H	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	6C00 H	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	73FF H	0	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	7400 H	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	77FF H	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	7800 H	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	7BFF H	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	7C00 H	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(1Kx8 RAM memory) is using the area of 8 KB.
Total area is 32 KB(4 devices x 8 KB).

INTERFACING WITH 1Kx8 RAM

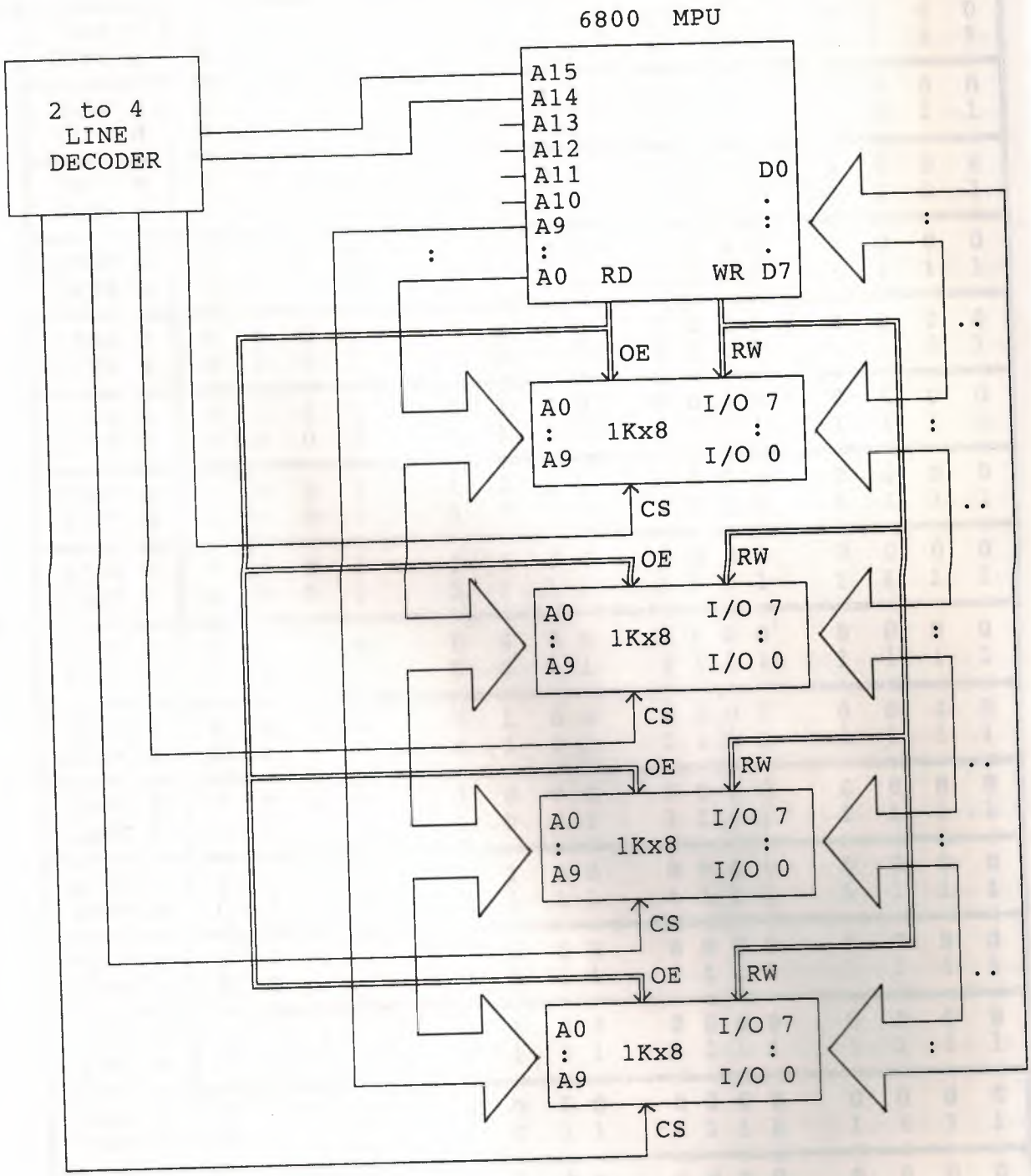


FIGURE 5.

ADDRESS MAP FOR FIGURE 5

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	03FF H	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	0400 H	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0BFF H	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	0C00 H	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	13FF H	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	1400 H	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1BFF H	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	1C00 H	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	23FF H	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	2400 H	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
	27FF H	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	2800 H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	2BFF H	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	2C00 H	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	33FF H	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	3400 H	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	37FF H	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	3800 H	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	3BFF H	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	3C00 H	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#2	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	43FF H	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	4400 H	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	47FF H	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	4800 H	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	4BFF H	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	4C00 H	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	53FF H	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	5400 H	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	57FF H	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	5800 H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	5BFF H	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	5C00 H	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	63FF H	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	6400 H	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
	67FF H	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	6800 H	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	6BFF H	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	6C00 H	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	73FF H	0	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	7400 H	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	77FF H	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	7800 H	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	7BFF H	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	7C00 H	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#3	8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	83FF H	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	8400 H	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	87FF H	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	8800 H	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	8BFF H	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	8C00 H	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	8FFF H	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	9000 H	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	93FF H	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	9400 H	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	97FF H	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	9800 H	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	9BFF H	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	9C00 H	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	9FFF H	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	A000 H	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	A3FF H	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	A400 H	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
	A7FF H	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	A800 H	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	ABFF H	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	AC00 H	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	AFFF H	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	B000 H	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	B3FF H	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	B400 H	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	B7FF H	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	B800 H	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	BBFF H	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	BC00 H	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#4	C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	C3FF H	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	C400 H	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	C7FF H	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	C800 H	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	CBFF H	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	CC00 H	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	CFFF H	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	D000 H	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	D3FF H	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
	D400 H	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	D7FF H	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	D800 H	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	DBFF H	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	DC00 H	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
	DFFF H	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	E000 H	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	E3FF H	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	E400 H	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
	E7FF H	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	E800 H	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	EBFF H	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	EC00 H	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	EFFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	F000 H	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	F3FF H	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	F400 H	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	F7FF H	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	F800 H	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	FBFF H	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	FC00 H	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(1Kx8 RAM memory) is using the area of 16 KB.
Total area is 64 KB(4 devices x 16 KB).

INTERFACING WITH 2Kx8 RAM

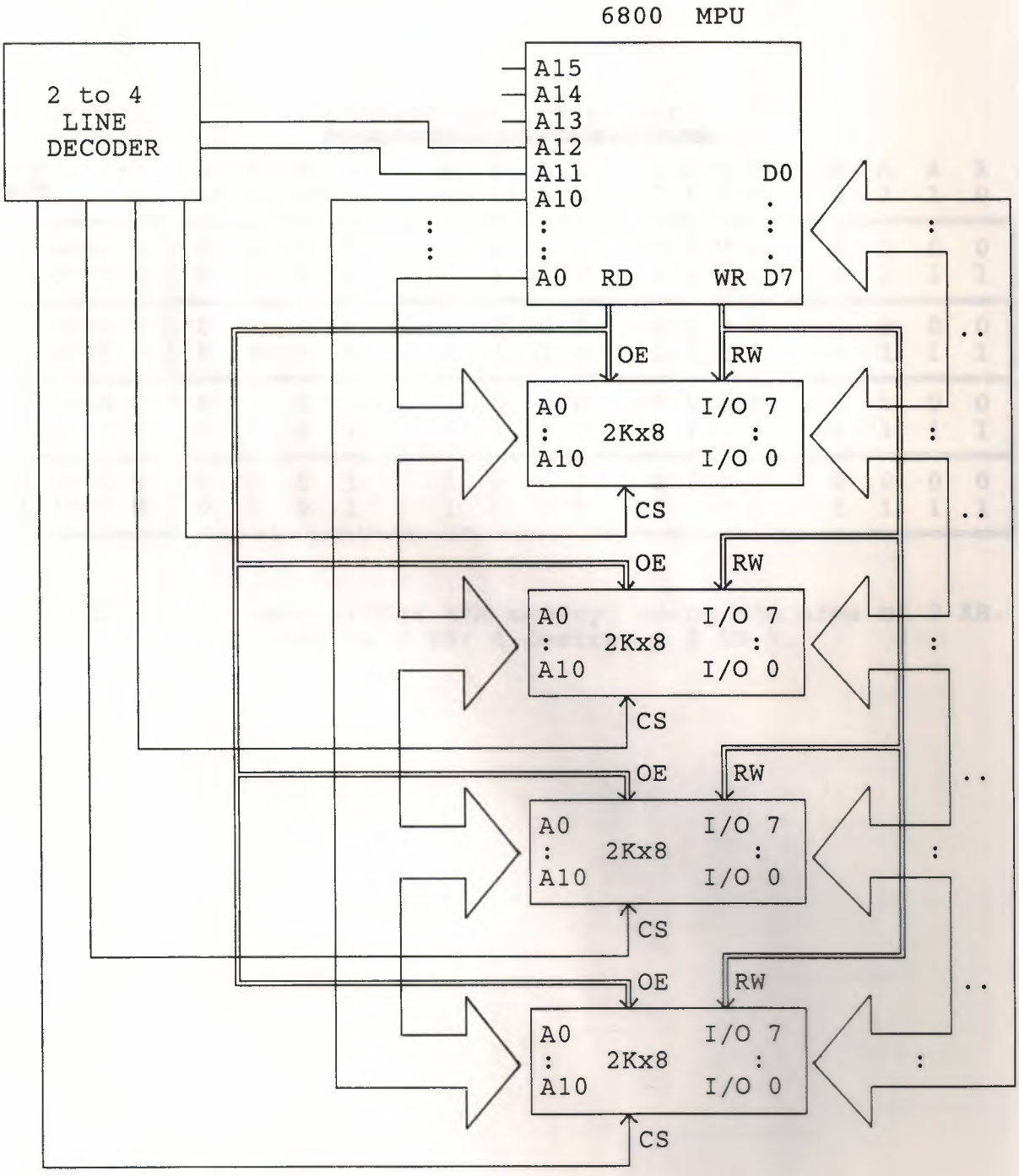


FIGURE 1.

ADDRESS MAP FOR FIGURE 1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
#2	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
#3	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
#4	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(2Kx8 RAM memory) using the area of 2 KB.
Total area is 8 KB(4 devices x 2 KB).

INTERFACING WITH 2Kx8 RAM

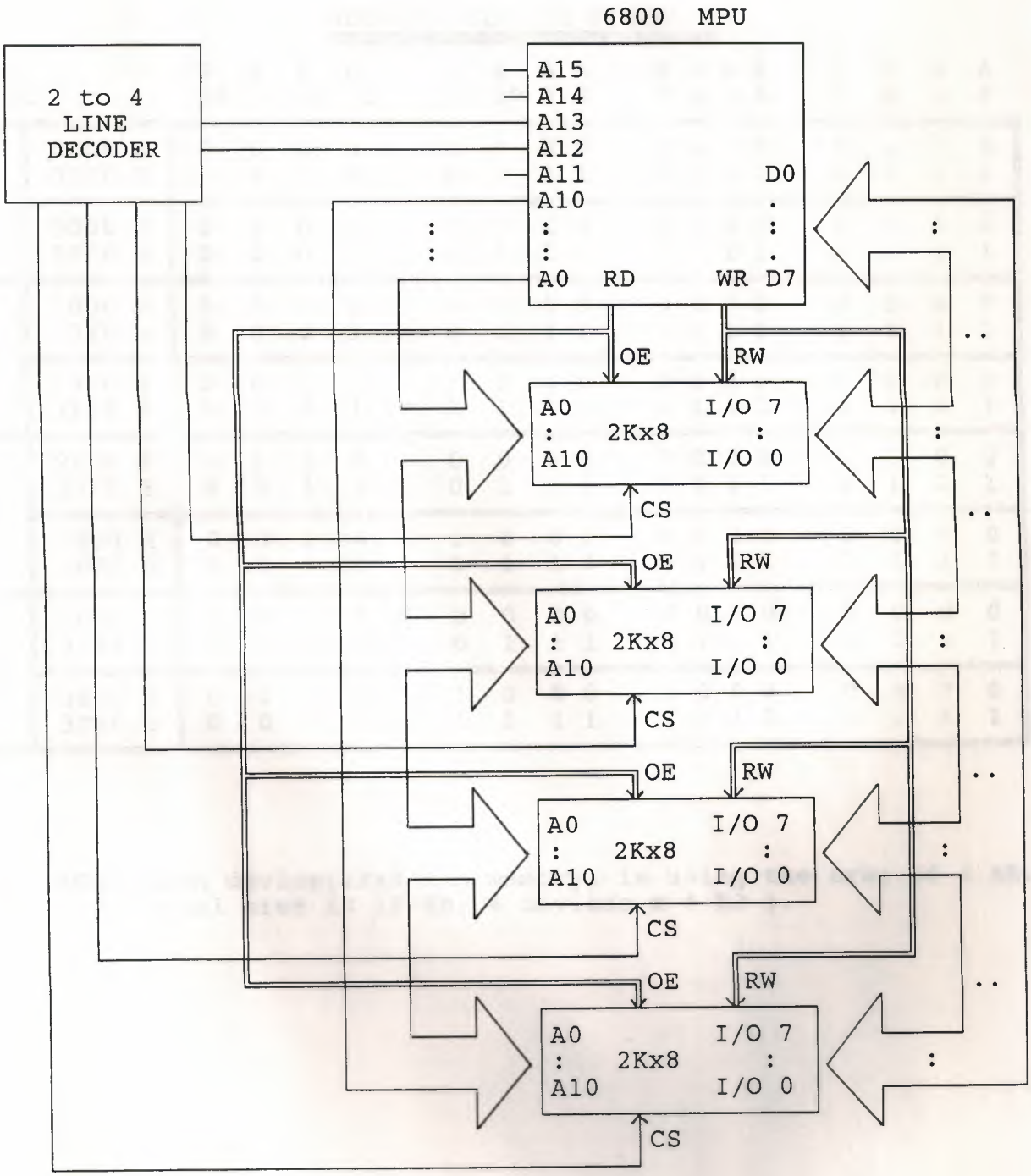


FIGURE 2.

ADDRESS MAP FOR FIGURE 2

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
#2	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	27FF H	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	2800 H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
#4	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	37FF H	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	3800 H	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(2Kx8 RAM memory) is using the area of 4 KB.
Total area is 16 KB(4 devices x 4 KB).

INTERFACING WITH 2Kx8 RAM

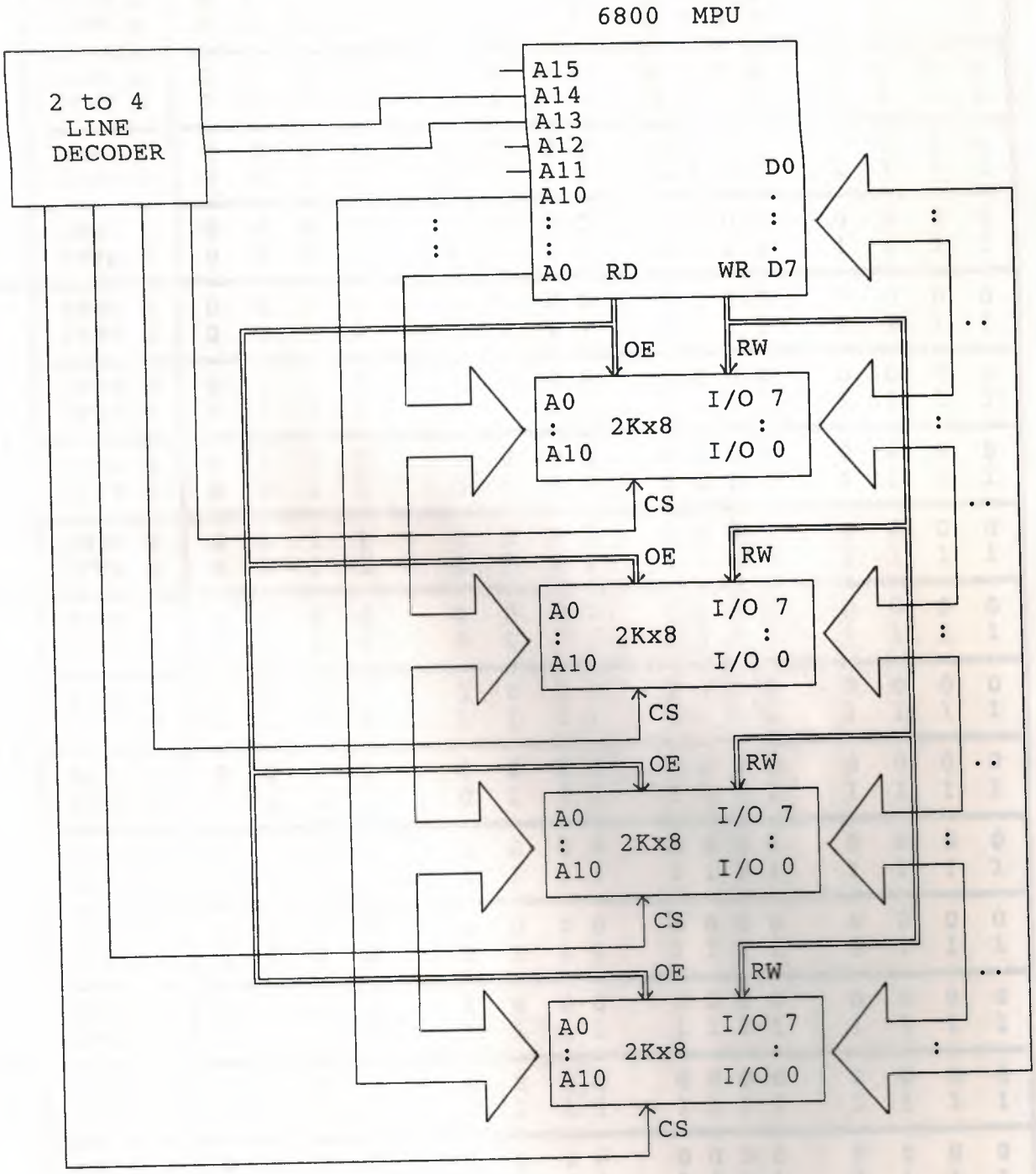


FIGURE 3.

ADDRESS MAP FOR FIGURE 3

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#2	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	27FF H	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	2800 H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	37FF H	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	3800 H	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	47FF H	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	4800 H	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	57FF H	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	5800 H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#4	6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	67FF H	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	6800 H	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	77FF H	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	7800 H	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(2Kx8 RAM memory) using the area of 8 KB.
Total area is 32 KB(4 devices x 8 KB).

INTERFACING WITH 2Kx8 RAM

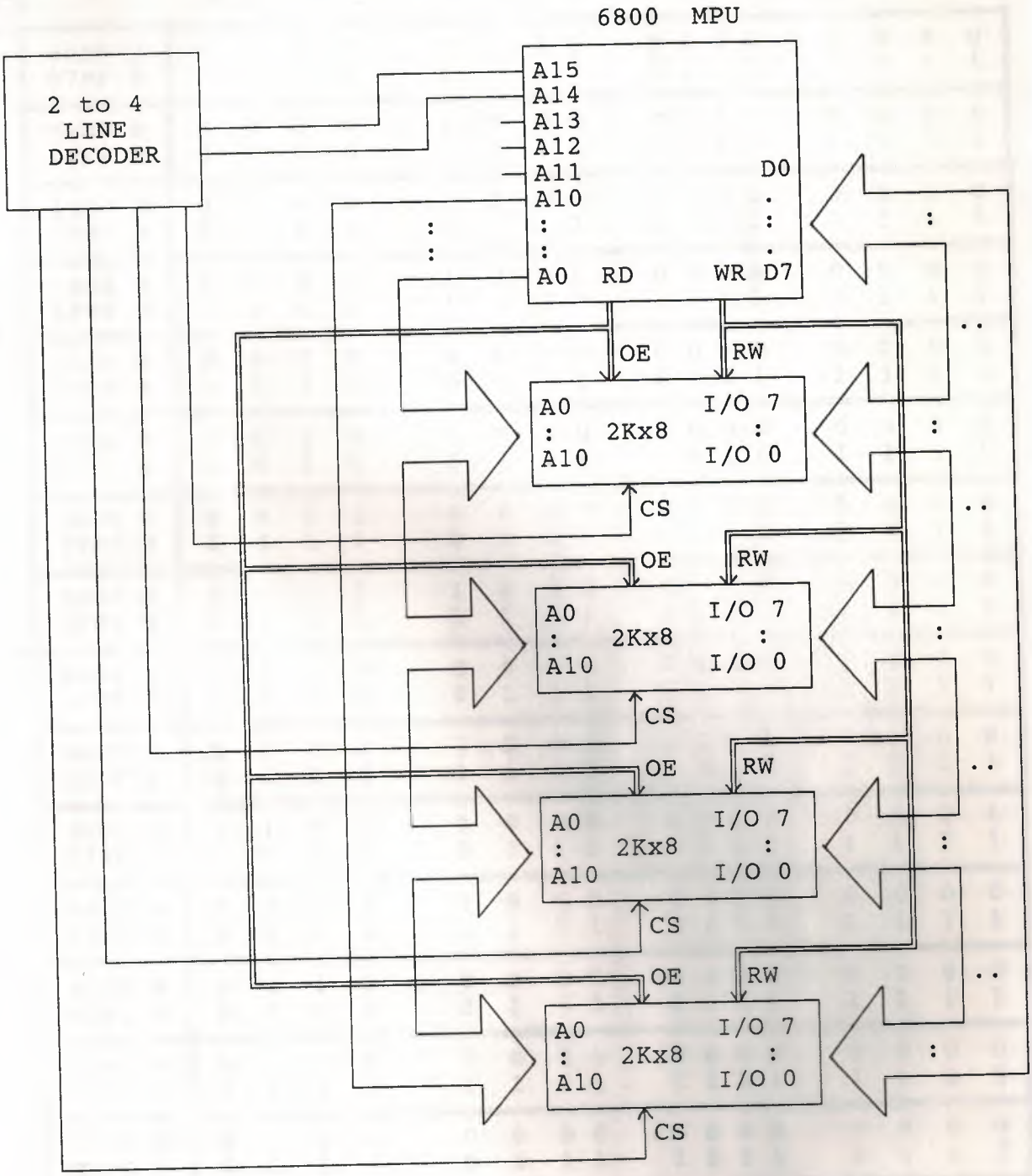


FIGURE 4.

ADDRESS MAP FOR FIGURE 4

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FF H	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0800 H	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	17FF H	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	1800 H	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	27FF H	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	2800 H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	37FF H	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	3800 H	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#2	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	47FF H	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	4800 H	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	57FF H	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	5800 H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	67FF H	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	6800 H	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	77FF H	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	7800 H	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#3	8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	87FF H	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	8800 H	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	8FFF H	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	9000 H	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	97FF H	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	9800 H	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	9FFF H	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	A000 H	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	A7FF H	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	A800 H	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	AFFF H	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	B000 H	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	B7FF H	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	B800 H	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#4	C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	C7FF H	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	C800 H	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	CFFF H	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	D000 H	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	D7FF H	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	D800 H	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	DFFF H	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	E000 H	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	E7FF H	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
	E800 H	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	EFFF H	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	F000 H	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	F7FF H	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	F800 H	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(2Kx8 RAM memory) using the area of 16 KB.
Total area is 64 KB(4 devices x 16 KB).

INTERFACING WITH 4Kx8 RAM

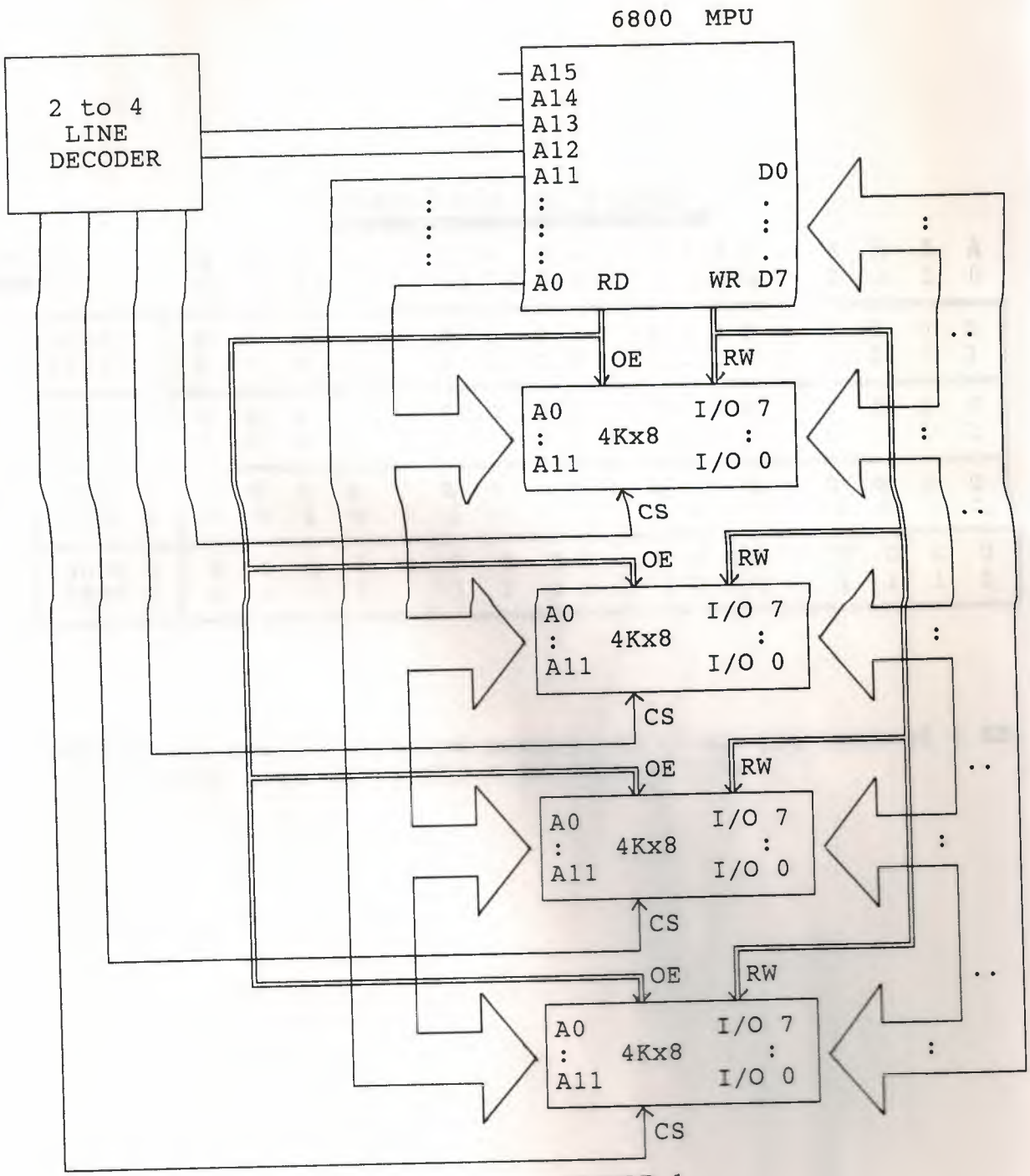


FIGURE 1.

ADDRESS MAP FOR FIGURE 1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
#2	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
#4	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(4Kx8 RAM memory) is using the area of 4 KB.
Total area is 16 KB(4 devices x 4 KB).

INTERFACING WITH 4Kx8 RAM

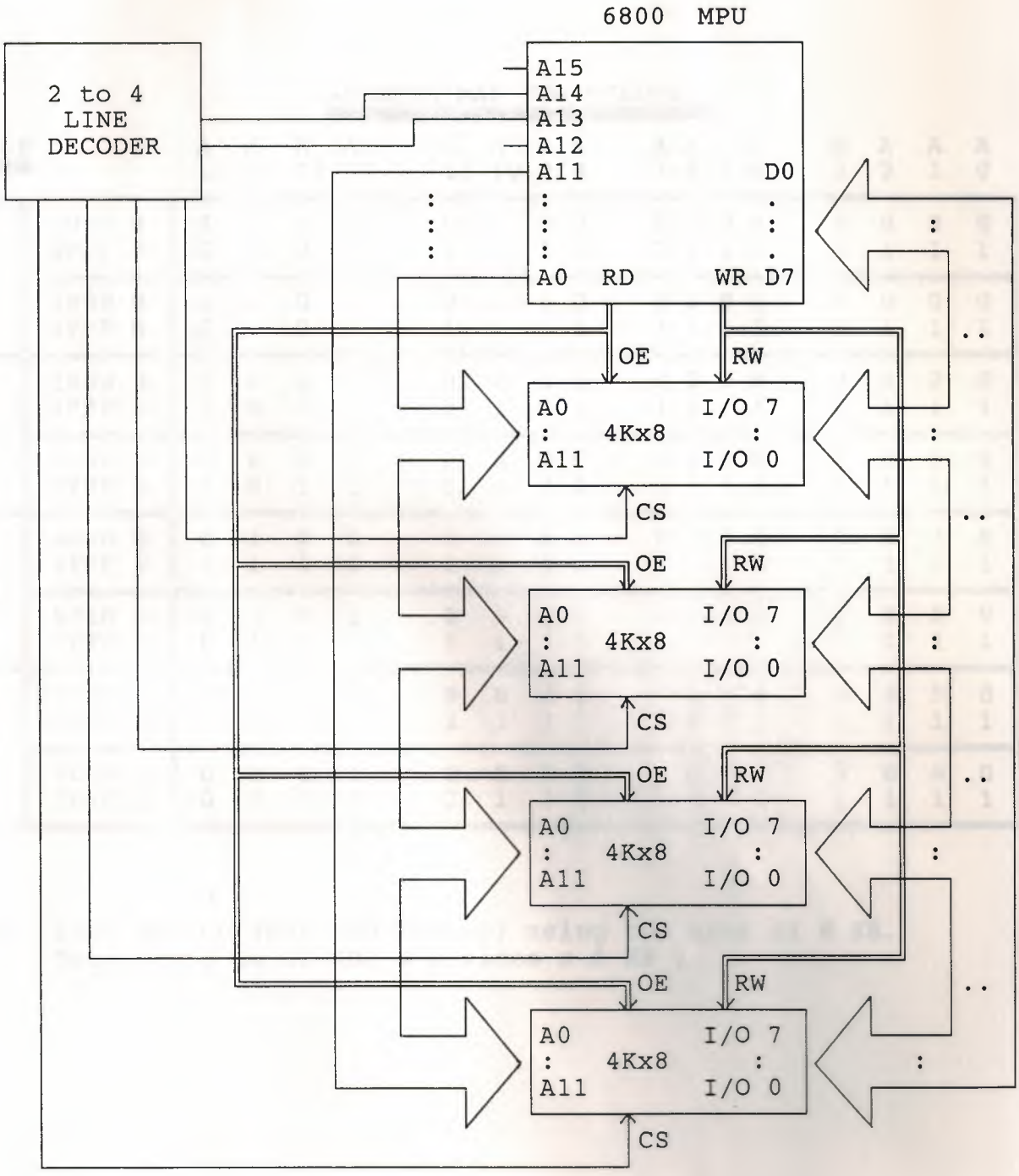


FIGURE 2.

ADDRESS MAP FOR FIGURE 2

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#2	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
#4	6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(4Kx8 RAM memory) using the area of 8 KB.
Total area is 32 KB(4 devices x 8 KB).

INTERFACING WITH 4Kx8 RAM

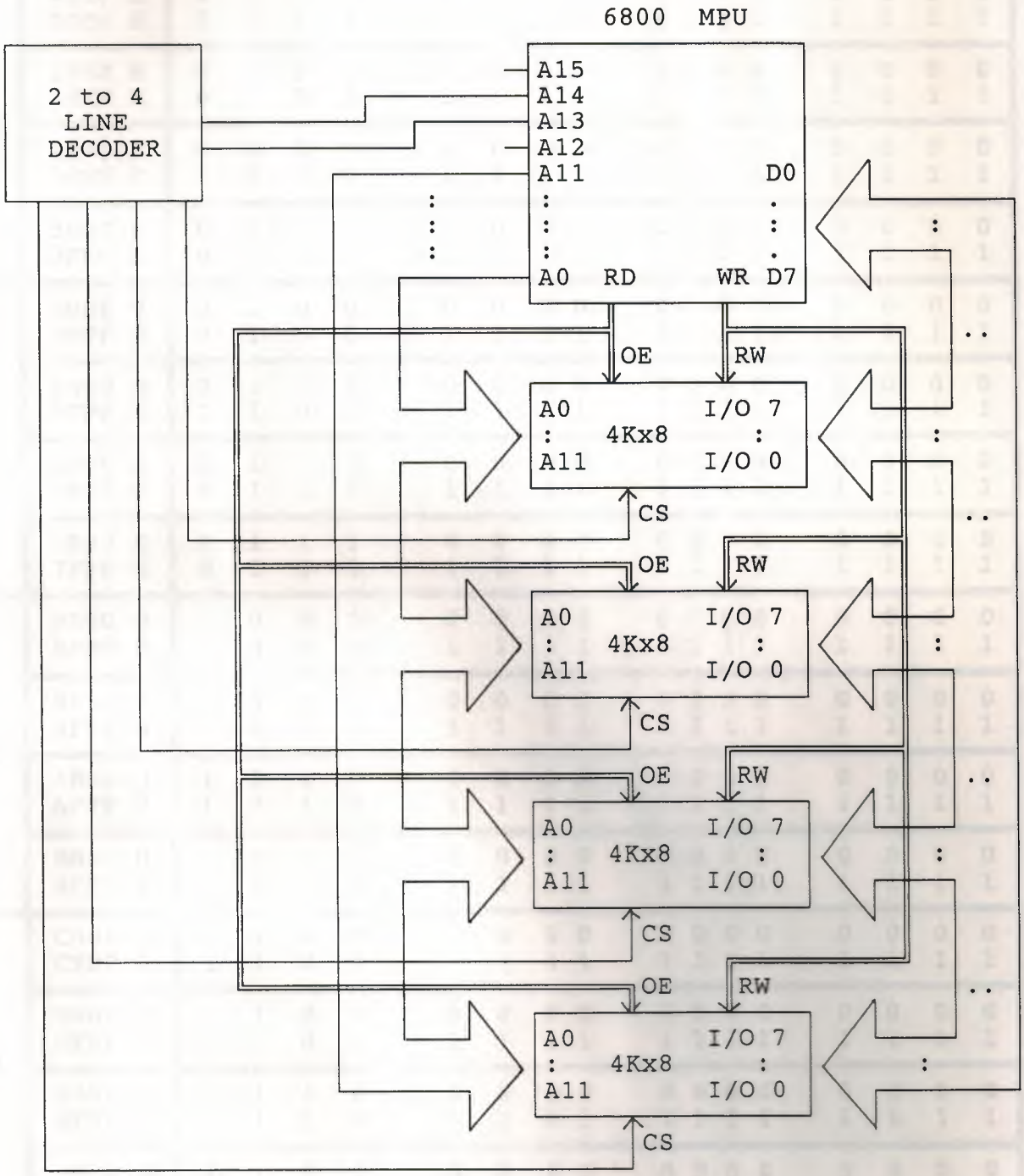


FIGURE 3.

ADDRESS MAP FOR FIGURE 3

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0FFF H	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	1000 H	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	1FFF H	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	2000 H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	2FFF H	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	3000 H	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#2	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4FFF H	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	5000 H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	5FFF H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	6000 H	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	6FFF H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	7000 H	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8FFF H	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	9000 H	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	9FFF H	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	A000 H	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	AFFF H	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	B000 H	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#4	C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	CFFF H	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	D000 H	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	DFFF H	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	E000 H	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	EFFF H	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	F000 H	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(4Kx8 RAM memory) is using the area of 16 KB.
Total area is 64 KB(4 devices x 16 KB).

INTERFACING WITH 16Kx8 RAM

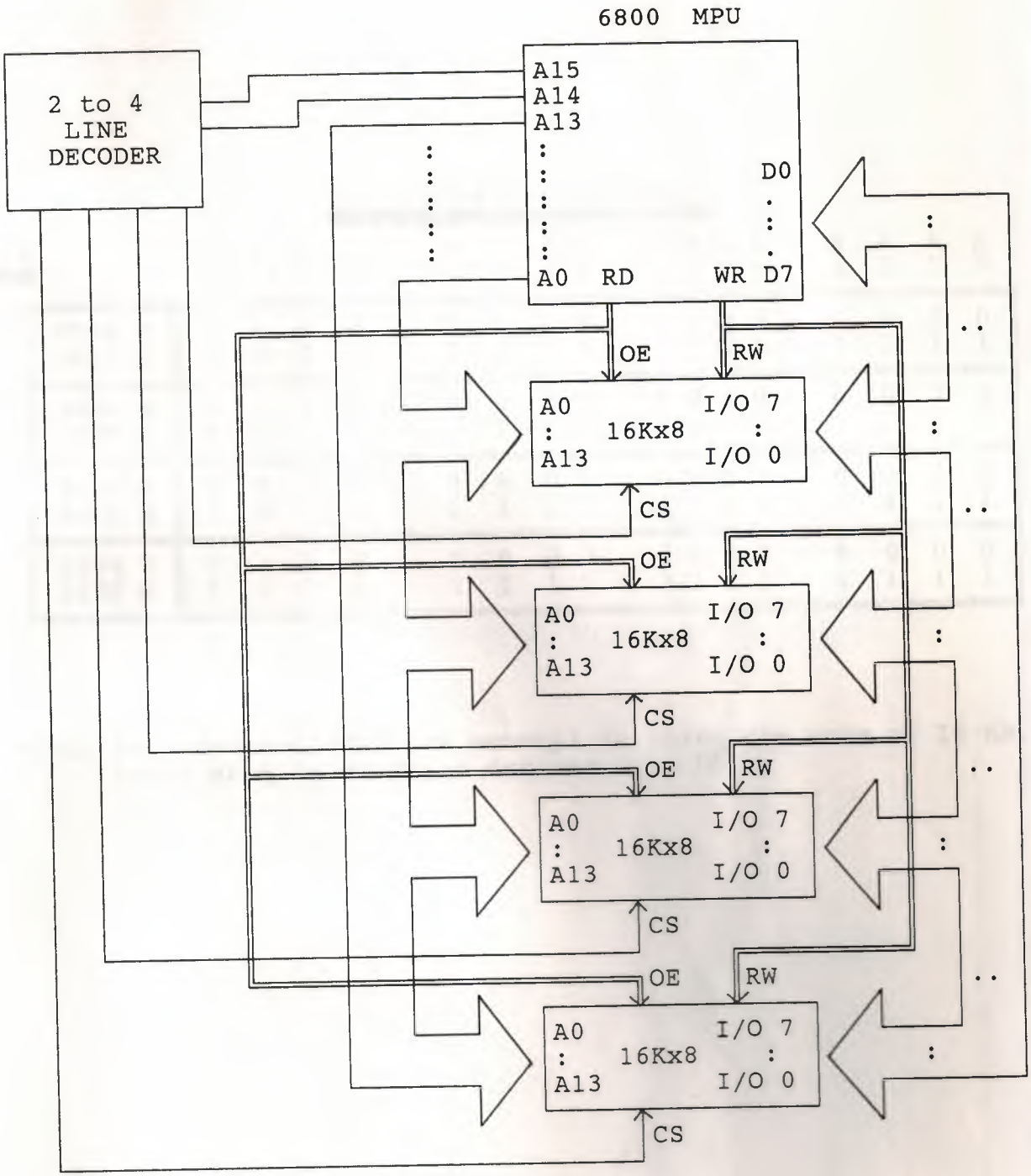


FIGURE 1.

ADDRESS MAP FOR FIGURE 1

DEVICE		A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0
#1	0000 H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3FFF H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#2	4000 H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	7FFF H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#3	8000 H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BFFF H	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
#4	C000 H	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	FFFF H	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Each device(16Kx8 RAM memory) is using the area of 16 KB.
Total area is 64 KB(4 devices x 16 KB).

APPENDIX B

National Semiconductor

MM54HC32/MM74HC32
Quad 2-Input OR Gate

General Description

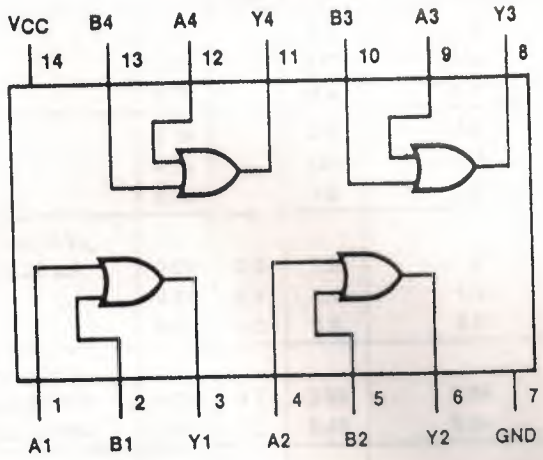
These OR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

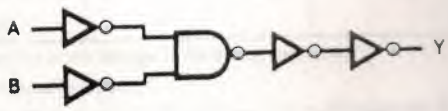


TL/F/5132–1

Top View

Order Number MM54HC32* or MM74HC32*

*Please look into Section 8, Appendix D for availability of various package types.



$Y = A + B$

TL/F/5132–2

(1 of 4)

bsolute Maximum Ratings (Notes 1 & 2)

Military/Aerospace specified devices are required, ntact the National Semiconductor Sales Office/ stributors for availability and specifications.

pply Voltage (V_{CC})	−0.5 to +7.0V
Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
mp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
orage Temperature Range (T_{STG})	−65°C to +150°C
wer Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
ad Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

C Electrical Characteristics (Note 4)

mbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
H	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.7	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
L	Maximum Low Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
C	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

ote 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

ote 2: Unless otherwise specified all voltages are referenced to ground.

ote 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

ote 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when esigning with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, C, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

ymbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
HL, t_{PLH}	Maximum Propagation Delay		10	18	ns

C Electrical Characteristics

= 2.0V to 6.0V, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

nbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay		2.0V	30	100	125	150 ns
			4.5V	12	20	25	30 ns
			6.0V	9	17	21	25 ns
t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110 ns
			4.5V	8	15	19	22 ns
			6.0V	7	13	16	19 ns
	Power Dissipation Capacitance (Note 5)	(per gate)		50			pF
	Maximum Input Capacitance			5	10	10	10 pF

te 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HC04/MM74HC04 Hex Inverter

General Description

These inverters utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

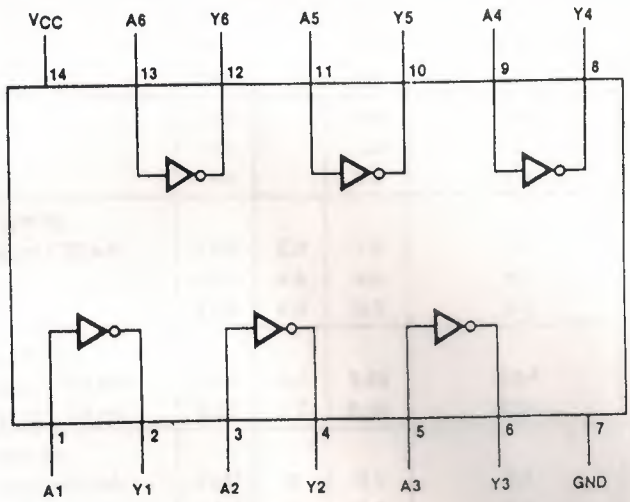
The MM54HC04/MM74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: 10 μW maximum at room temperature
- Low input current: 1 μA maximum

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5069–1

Top View

Order Number MM54HC04* or MM74HC04*

*Please look into Section 8, Appendix D for availability of various package types.

1 of 6 Inverters

TL/F/5069–2

olute Maximum Ratings (Notes 1 & 2)

ary/Aerospace specified devices are required, t the National Semiconductor Sales Office/ utors for availability and specifications.

Voltage (V_{CC})	−0.5 to +7.0V
ut Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
put Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Diode Current (I_{IK}, I_{OK})	±20 mA
put Current, per pin (I_{OUT})	±25 mA
C or GND Current, per pin (I_{CC})	±50 mA
e Temperature Range (T_{STG})	−65°C to +150°C
Dissipation (P_D)	
e 3)	600 mW
Package only	500 mW
Temperature (T_L)	
dering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Electrical Characteristics (Note 4)

	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7 V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2 V
	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN} = V_{IH} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4 V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4 V
	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40 μA

1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

2: Unless otherwise specified all voltages are referenced to ground.

3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

4: For a power supply of 5V ± 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

* limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Qr. CY'89

lectrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

ool	Parameter	Conditions	Typ	Guaranteed Limit	Units
PLH	Maximum Propagation Delay		8	15	ns

Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
H	Maximum Propagation Delay		2.0V	55	95	120	145	ns
			4.5V	11	19	24	29	ns
			6.0V	9	16	20	24	ns
HL	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
	Maximum Input Capacitance			5	10	10	10	pF

C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

IM54HC138/MM74HC138
-to-8 Line Decoder

eneral Description

is decoder utilizes advanced silicon-gate CMOS technol-gy, and is well suited to memory address decoding or data uting applications. The circuit features high noise immuni- and low power consumption usually associated with MOS circuitry, yet has speeds comparable to low power chottky TTL logic.

he MM54HC138/MM74HC138 has 3 binary select inputs A, B, and C). If the device is enabled these inputs deter-ine which one of the eight normally high outputs will go w. Two active low and one active high enables (G1, $\overline{G2A}$ nd $\overline{G2B}$) are provided to ease the cascading of decoders.

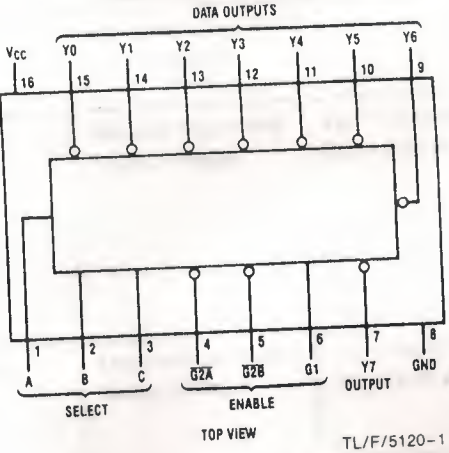
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

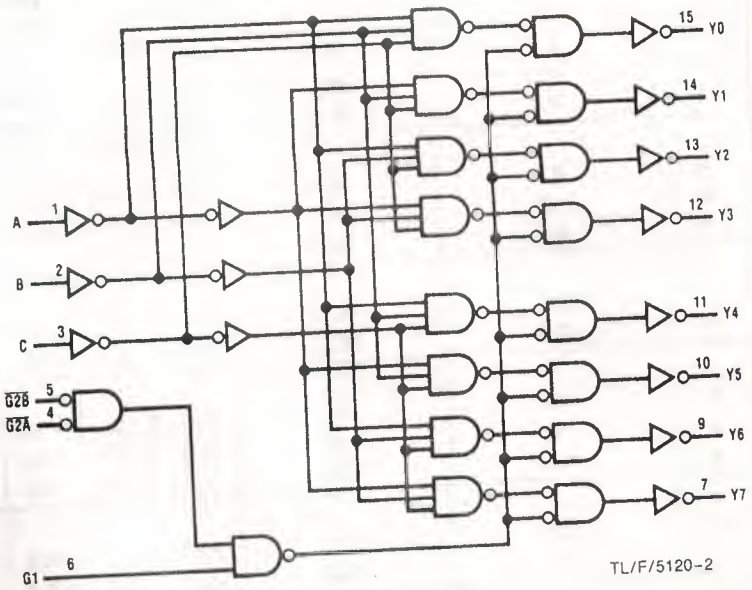
Dual-In-Line Package



TL/F/5120–1

Order Number MM54HC138* or MM74HC138*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5120–2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = G2A + G2B$

H = high level, L = low level, X = don't care

bsolute Maximum Ratings (Notes 1 & 2)

Military/Aerospace specified devices are required, ntact the National Semiconductor Sales Office/ stributors for availability and specifications.

pply Voltage (V_{CC})	−0.5 to +7.0V
C Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
C Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
amp Diode Current (I_{IK}, I_{OK})	±20 mA
C Output Current, per pin (I_{OUT})	±25 mA
C V_{CC} or GND Current, per pin (I_{CC})	±50 mA
torage Temperature Range (T_{STG})	−65°C to +150°C
ower Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
ead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5 V
			4.5V		3.15	3.15	3.15 V
			6.0V		4.2	4.2	4.2 V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5 V
			4.5V		1.35	1.35	1.35 V
			6.0V		1.8	1.8	1.8 V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9 V
			4.5V	4.5	4.4	4.4	4.4 V
			6.0V	6.0	5.9	5.9	5.9 V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7 V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4 V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160 μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, Binary Select to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay, Binary Select to any Output		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, G1 to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		23	30	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		18	25	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{LH}	Maximum Propagation Delay Binary Select to any Output Low to High		2.0V	75	150	189	224 ns
			4.5V	15	30	38	45 ns
			6.0V	13	26	32	38 ns
t_{HL}	Maximum Propagation Delay Binary Select to any Output High to Low		2.0V	100	200	252	298 ns
			4.5V	20	40	50	60 ns
			6.0V	17	34	43	51 ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay G1 to any Output		2.0V	75	150	189	224 ns
			4.5V	15	30	38	45 ns
			6.0V	13	26	32	38 ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	82	175	221	261 ns
			4.5V	28	35	44	52 ns
			6.0V	22	30	37	44 ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	75	150	189	224 ns
			4.5V	15	30	38	45 ns
			6.0V	13	26	32	38 ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	30	75	95	110 ns
			4.5V	8	15	19	22 ns
			6.0V	7	13	16	19 ns
C_{IN}	Maximum Input Capacitance			3	10	10	10 pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		75			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.