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GRADUATION PROJECT

WATTS DC TO AC INVERTER & POWER AC

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ELECTRICAL & ELECTRONICS ENGINEERING

PREFACE

Inverter is a very useful unit. Depending upon the output power the inverter has the capability of supplying power for many items that normally don't go on camping trips, such as TV, a stereo, an electric razor, or a desk lamp. However, it also has many other uses, such as supplies for computers, variable speed ac motor drives to power the oscilloscope or soldering iron when doing electronic work in the field.

My project is about the inverter, that draws a max.of 5 amp, which is completely safe for an automobile cigarette lighter socket, and no load current is only half an amp. The output voltage is regulated and remains fairly constant from no load to full load.

INTRODUCTION

Inverters convert dc power to ac power at some desired output and frequency. Application of inverter include stand by power supplies, uninterruptible power supplies for computers, variable speed ac motor drives, aircraft power supplies, induction heating and output of the dc transmission lines.

In most of the inverter applications, it is necessary to control both the output voltage and the output frequency. The controllable voltage requirement may arise out of the need to overcome regulation in the connected ac equipment or to maintain constant flux in ac motors driven at variable speed by variation of their supply frequency. If the dc input voltage is controllable, then an inverter with a fixed ratio of dc input voltage to ac output voltage may be satisfactory. If the dc input voltage is not controllable, then control of the output voltage must be obtained by employing pulse width modulation.

The output voltage wave form of an inverter is non sinusoidal and in most applications the voltage harmonics have a significant effect on the overall system performance. These harmonics may be reduced at the cost of increasing the complexity of the inverter circuit, and an economic decision must be made on the degree to which this should be done.

Inverter circuit designs are generally divided into

two classifications. First there are amplifier type inverter: those inverters that use transistors as amplifier, operating in nonsaturation condition. Second, there are the saturated switch types of inverter: these inverters operate with the switches either in a fully saturated conducting mode, or in cut off blocking mode.

CHAPTER ONE

DESIGN CONSIDERATIONS FOR STATIC INVERTERS

Inverters convert d.c. power to a.c power at some desired output voltage and frequency. Applications of inverters include the following.

1. Stand by power supplies.
2. Uninterruptable power supplies for computers.
3. Variable-speed ac motor drives.
4. Aircraft power supplies.
5. Output of dc transmission lines.

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297$_1$2$_6$ 7089784$_0$2
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±WAX$_A$i*A`+Ad±

INVERTERS:-

A Static inverter is a solid state (semiconductor)

device designed to convert a dc electrical power input into an ac electrical power output with a sinusoidal wave form, without an operational dependance on relative mechanical motion between component parts.

A static inverter must provide the following:

. dc to ac power conversion

. conversion to a fixed-frequency output voltage

. a sinusoidal wave shape for variations of both dc input distortion.

. output voltage regulation for variation of both dc input voltage and ac load including power factor.

. some means of protecting the inverter from over loads on the output.

The static inverter is composed of the following functional components:

. A power stage or number of power stages that convert the dc input into relatively crude ac output.

The ac contains not only the fundamental ac frequency desired, but also unwanted harmonic frequencies. The power stage is the simplest power stage that can produce an ac voltage. By definition the stage uses four semiconductor switches (transistor or SCR) which can only produce square wave or two valued voltage.

. An ac output filter that eliminates the unwanted harmonics generated by the power stage. So as to provide the load a sinusoidal wave form with a given max. distortion.

The amount of deviation between a true sine wave and the

output voltage can be measured in the form of total distortion (THD). The ac filter size is determined only the amount of unwanted harmonics in the power but-also by the frequencies of these harmonics.

The lower the harmonic frequencies generated by the stage the larger will be the ac filter. Consequently if order frequencies in the power stage wave form (3rd, etc.) can be reduced in magnitude or eliminated the ac size can be made smaller.

logic to provide proper sequential control over the SCR's the power stage or power stages such as to provide one or of the following:

(a) frequency control
(b) Voltage regulation
(c) Current limiting (for over load protection)
(d) synchronization to external sources
(e) paralleling of inverters (with load sharing)

Inverter circuit designs are generally divided into two classifications. First, there are the amplifier-type inverter: those inverters that are transistors as amplifiers, operating in a non saturated condition. Second, there are the saturated-switch types of inverters (using either transistor or SCR's) these inverters operate with the switches either in a fully saturated conducting mode, or in cutoff blocking mode

The amplifier-type inverter circuit are characterized by lower efficiencies, high power dissipation in the transistor

...ers, cross over distortions (in class B and C push-...types), as well as many other well known problems. These ...of inverters are quite satisfactory of the applications ...carefully selected, if the power level are low if the ...factor loads are not a consideration, and if efficiency ...not of the key criteria to the inverter design. Because of ...limited applications, the amplifier type inverters are ...very practical.

1.2 INVERTER REQUIREMENTS:-

Each requirement must be considered in terms of total ...ight, efficiencies, and reliability.

...ypical electrical performance characteristics for static ...verters are listed below:

-output power 500 to 1500 VA, 1000 VA nominal

-output voltage 115 to 200 V rms, 3 phase, +/- 0.5%

-output frequency 400Hz + 0.01%

-output harmonic distortion 3%

-power factor range max. variation of 0.2

-efficiency 75%

-input voltage 24 to 30 V DC

-output phase angle 120 (+ 2)

-temperature range -35 C to +71 C

The inverter should have overload protection, be able to withstand environmental conditions.

1.3 CONSIDERATIONS COMMON TO ALL INVERTERS.

There are several design considerations that are common to

inverters, and these are as follows:

FEED BACK IN AN INVERTER:-

A static inverter is comparable to an oscillator driving power amplifier; an arrangement used by early low-powered static inverters. A 400 Hz sinusoidal signal is produced in the oscillator, and this signal is power amplified in conventional class A or class B power amplifier stages. This operation is still practical for inverters of less than 50 VA per phase, but at higher levels, low frequency makes the technique inadequate.

It is possible to have as many as three different types of feed back in static inverter: Voltage, current and phase feedback. They are generally defined as follows.

(i) VOLTAGE FEED BACK:-

Regulation of ac output voltage with changes in input dc voltage output load is provided by voltage feedback. Normally the output ac voltage is detected and rectified to provide a dc voltage is detected and rectified to provide a dc voltage. This dc voltage is compared with a Zenner reference diode, and the error voltage is fed back to the driver or power stage, to control the ac output amplitude. Such detection any be root-mean-square, average, or peak sensing and may occur either before or after the filter. The largest variations in static inverter design arise from the exact manner in which this dc error signal regulates the ac output.

In a three phase inverter, either combined or single phase voltage feed back may be used. A three phase detector is used in the combined system and the same error signal is applied to all these phase. If large load and power factor unbalances are expected, it is better to regulate the system as through it were three separate single inverters.

(ii) CURRENT FEED BACK:-

Current feed back provide overload protection for the static inverter. This protection may be either or the types. In first, current in excess of the maximum results in shutdown of the inverter. That is, the output voltage drops to zero, this protecting the unit. With this type of shutdown, the output turns on and off with in a period, preventing damage to any of the components. The second type of current feedback results in the inverter as constant current generator for load current in excess of maximum . This protects the unit and often maintains the operation of loads during transistor over-load. In general, this latter system is better through some what more difficult to achieve. Normally, a current feedback system is designed to work in conjunction with the voltage feedback system, and in effect, over rides the voltage feedback during overload condition.

(iii) PHASE FEED BACK:-

Phase feed back is sometimes used in three phase static

verter to ensure an exact 120 phase angle between output voltages. Normally, the inverter oscillator provides exact 120 phase angle at the input to the driver stages. If each phase is equally loaded, the phase shift thought the driver, power, and filter stages if each phase is equal resulting in the same 120 phase angle at the output. Frequently however, the loads or power factor are unbalanced, which may result in different phase shift through each phase.

Phase feed back is applied by comparing the angle of two phases with respect to the third and generating two feed back signals proportional to the differences from the nominal 120. these two feed back signals then act in phase shifting circuit in two of these three oscillator output signals in such a way that the inverter output are held at an exact 120 with respect to each other.

(b) POWER STAGE DESIGN:-

Power variation in the design of static inverter power stages are few, but good design in this area is more important then elsewhere, since most if the dissipated power occurs here and in the filter. In general, inverters may be grouped as bridge or parallel inverters, with different basic circuit resulting in the power stage. Following figure shows the

schematic diagram of a basic parallel inverter power stage.

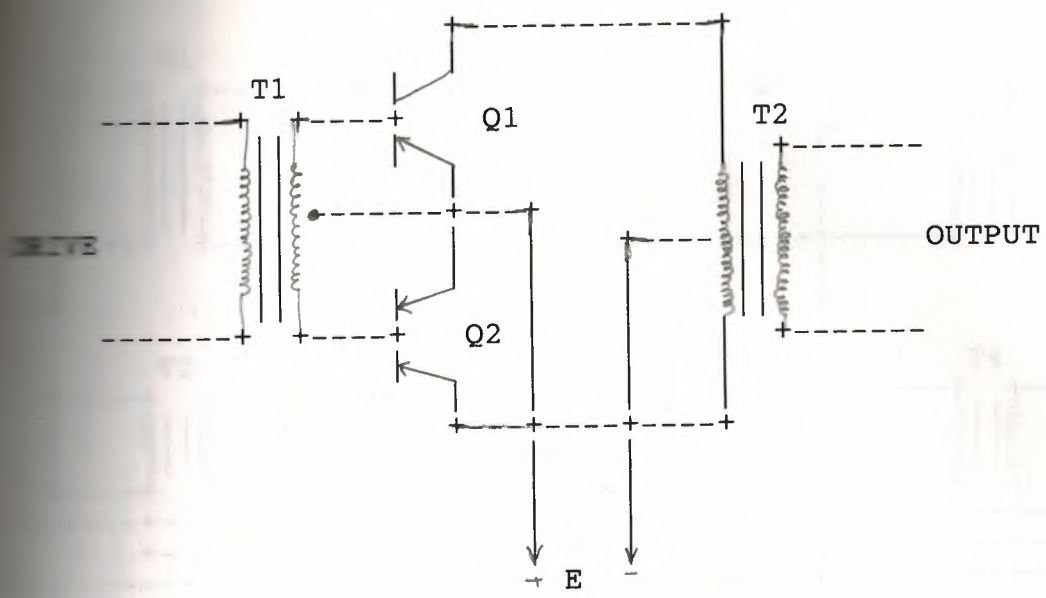

fig. 1.1

Transistor Q and Qz operate in push pull, each during one half of the cycle. Transformer T2 is the power output transformer. Parallel inverters are more common than bridge inverters. A typical bridge inverter power stage is shown in fig 1.2.

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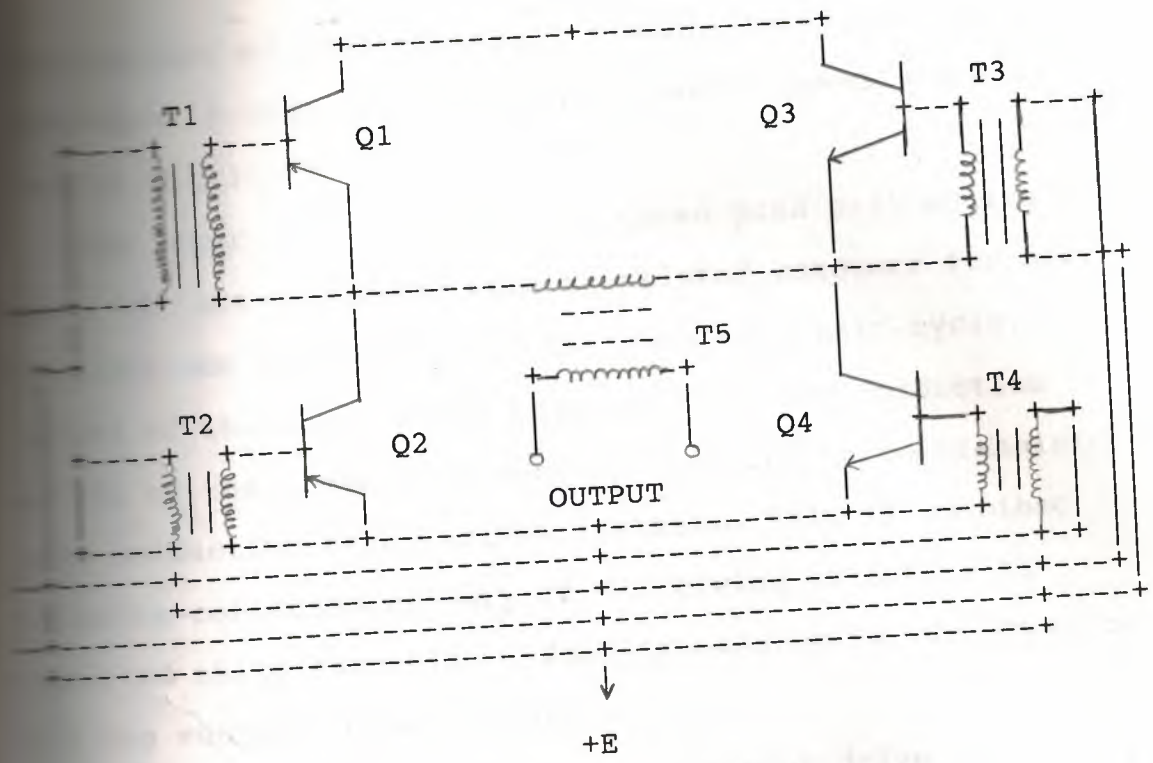


fig.1.2

Transformer T5 is the output transformer, which has terminals that are alternately switched from plus to minus by action of Q1, Q2, Q3 and Q4 arranged as a bridge. Transistors Q1 and Q3 operate together, as do Q2 and Q4. In a bridge inverter, each transistor is subjected only to the supply voltage during cut off because there is no induced voltage present. This indicates that the bridge inverter will operate safely with twice the supply voltage for a given transistor type. This primary disadvantage of the bridge inverter is its greater complexity. Since it requires twice the number of transistors for the same power rating and at the same supply voltage as compared to the parallel inverter. It is possible with three-phase inverters to eliminate the

disadvantages of bridge inverters while retaining their advantages. A three-phase bridge inverter power stage is shown in fig 1.3

The input drive consists of three push pull square waves, 120 out of phase. Each transistor conducts for half cycle and non conducting for the remaining half-cycle. Because of the three-phase relationship, the conduction periods of the transistor overlap, causing three transistor to be conducting at any given instants. This is combined in the delta-connected primary of T1, giving outputs with cancelled third harmonics. Each transistor is subjected to only the supply voltage during cut off.

Proper design of the power transistor drive circuitry, the output transformer, and the filter are necessary for efficient switching of the power transistors. The design of the output transformer is of particular importance. In

general, this transformer should be designed with low leakage inductance and good high-frequency response. The three-phase transformer have to achieve an efficiency of about 95% in order to achieve an over all inverter efficiency of 85% (assuming filter efficiency of 95% and switching transistor efficiency of 95%)

INDUCTANCE SWITCHING IN TRANSISTORS:-

The ability of an inverter to operate into power factor loads, and the ability of the main power transistor to switch a square pattern and directly related. Under normal unity power factor operation, the switching pattern or the transistor begins to look more like the circular pattern illustrated in fig 1.4

fig. 1.4

In order to optimize the efficiency of the power transistor in switching mode, switching patterns may be produced on an oscilloscope and analyzed to determine regions of transistor operation with high dissipation. Circuit adjustments, filter and load changes may be made and their

effect on the transistor may be made by means of the switching pattern.

EFFICIENCY:

The efficiency of an ac. device where power factor is a consideration, is often misunderstood. Efficiency is usually defined as "watts output divided by watts input multiplied by 100, expressed as percentage ". For dc input, this rule holds true and is a excellent measure of performance of a piece of equipment. For a static inverter operating under power factor load, this is often very misleading as a measure of performance.

For example, a static inverter operating at maximum volt- ampere output into a zero power factor load would reflect a zero efficiency by the above definition. Because the voltage and current are phase-shifted full 90 degree. There are no output watts to measure, since the inverter is producing no real power in watt. The inverter is, however, operating at full volt-ampere load, and requiring very real power in watts from the dc input.

By this, it can be seen that a power factor has a severe effect on the "apparent efficiency" of the inverter. The only true indication of performance of the inverter is when efficiency is measured at unity power load.

Take the example of 350 VA static inverter that operates at 80% efficiency into a 350 VA resistive load (unity performance). The internal losses of inverter are

approximately 87 W total.

This same inverter operating into a 350 VA load at 0.65 power factor would be delivering a real power of only 350 * 0.65 or approximately 227 W. This 227W is a power that goes straight through the inverter. In addition 350 VA at the above power factor of 0.65 represents also plain reactive power of 350*[{1-(0.65)(0.65)} E 0.5] or 256 VA. the only way a dc source can simulate a power factor, is to deliver the power to the inverter, then receive it back from the inverter.

In this manner, assuming the handling efficiency of the inverter at 80% then the inverter's internal losses could be computed by the two formulas :

80% = 227 / [227 + (internal loss A)]

80% = 265 / [265 + (internal loss B)]

Total internal Losses = A+B = 123W. Total efficiency is therefore, by definition

227W /[227 + 127] = approximately 65 %

This is no doubt, an extreme example, but it illustrate the severe impact that a power factor has on the apparent efficiency of an inverter.

Inverter losses (that determine efficiency) can be classified into three general categories.

(i) There are fixed losses. These are generally easy to measure, simply by removing all loads from the inverter, and measuring its power consumed. These are no load losses and

are always fixed.

(ii) Second, there are the losses that are directly proportional to the output power. These are semiconductor saturation resistance losses, etc.

(iii) Third, there are losses that rise quadratically with the output power. There are flux density losses, etc. This is what causes the inverter efficiency to reach a maximum point, then decrease as additional loads are applied.

Losses are really the best measure of an inverter's efficiency, and in general, losses and not the efficiency should be specified in an inverter specification.

An other factor to be considered is the size(volt-ampere output rating) of the inverter. High power inverter can always be more efficient than lower power inverter, if all other factors are equal. One basic reason for this fact is the internal efficiency of the transformer.

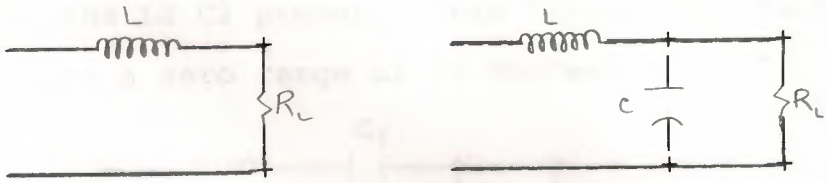
(e) OUTPUT FILTERS:-

The design of the static inverter output filters is an extremely difficult task. If the requirements are constant, the task is eased, if, however, the load and/or power factor varies widely and very low harmonics content is necessary, the design is difficult, and the filter will be heavy.

The filter should be efficient(95% overall efficiency). Its input impedance at higher frequencies should be capacitive (never inductive if possible), and it should be of maximum weight. The maximum harmonics permitted from most

missile or aircraft inverter is 5%, same systems require as low as 2% harmonics.

Now resonant, first and second order critically damped filter, as shown in the fig. 1.5



1st. order 2nd. order

fig 1.5

A common filter of 4th order is shown in the fig 1.6. In this filter, L2 and C2 are made resonant at the fifth order.

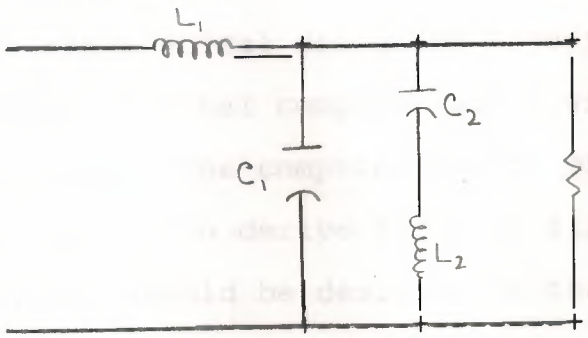


fig.1.6

A disadvantage with these filters is that their filtering ability is the function of their loading capacity, and the input impedance of the filter is not resistive at the

fundamental. These objections are overcome by the 4th. order resonant filter shown in fig. 1.7. In this filter L1 and C1 are tuned to series resonance at the fundamental, and L2 and C2 are tuned to shunt the load impedance. This filter actually works better if L1 and C1 are tuned above 350 Hz and if L2 and C2 are tuned to about 450 Hz. Also L2 should predominate in the L2 C2 product. This filter will filter to 2% harmonics over a zero range of 20 degrees.

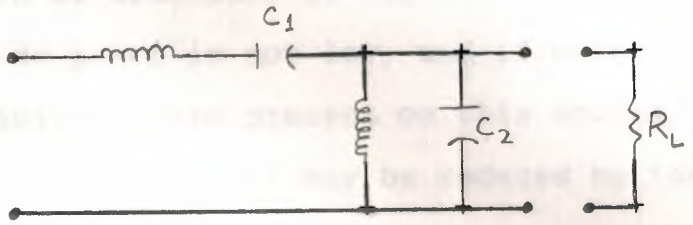


fig 1.7

The physical size of the filter components is often a problem and may be partially overcome by the use of transformers to scale the filter components values.

Only a few general rules for filter design have been indicated. The mathematical design of such filter is so complicated that a digital computer might will be used in the design of the filter. The computer may be programed to vary a great many parameters to derive the best filter for the weight. The filter should be designed so that the reactance of the load is used as the part of the filter. For example, if the load has a lagging power factor of 0.4, this inductance should be figured as part of L2 when using the 4th. order resonant filter. This would make the static inverter higher than if the power were unity. In general the

more lagging or leading the power factor, the higher the filter becomes.

(e) INPUT FILTER:-

The function of the input filter is two folds. the filter is intended to remove the transient from the dc input line. It must prevent transients and noise from being produced on dc line by the action of static inverter.

The reduction of transient is difficult if the source impedance of the dc power is not low, and if other loads which are being switched are present on this source. Usually, this sort of transient may be reduced by the use of low-pass T-section filter.

(1.4) SATURATED SWITCH TYPE INVERTERS:-

Under this topic we will discuss only the voltage driven inverter.

VOLTAGE DRIVEN INVERTERS:

The voltage driven inverter circuit is the generally accepted circuit employed in most of the today's static inverter design. A power source is connected through a pair of semiconductor switches, into the end of a center tapped transformer primary. The power source is a betray, with more than adequate capacity, and with a source impedance so low that it is negligiable. A schematic representation of the voltag-driven inverter is illustrated in fig. 1.8.

A voltage driven inverter is defined as follows:
A voltage driven inverter in which the design of the circuit connects the dc voltage source through the semiconductor switches directly to the primary of the transformer.

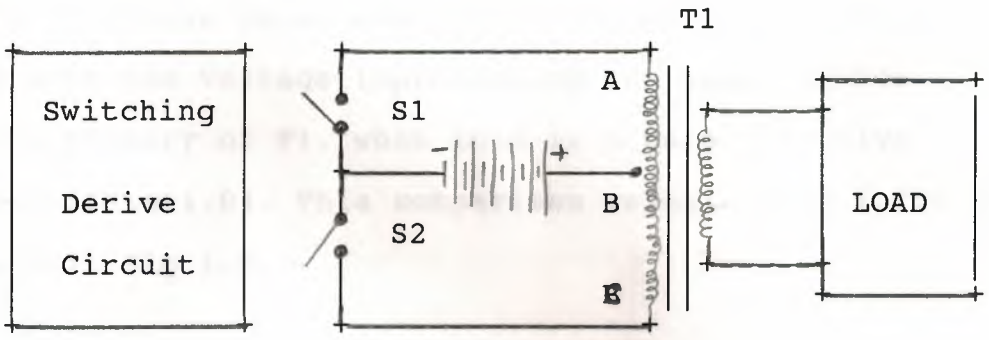


fig. 1.8

This means that when S1 is closed, the full source voltage(minus the semi conductor saturation losses, which we will ignore) appear across the AB primary of the transformer T1, and conversely, when S2 is closed, the full source voltage BC primary.

The switching drive circuit alternately saturates and cuts off the semiconductor switches, causing a alternating voltage to be generated across the windings of the transformer T1, and to be deliver to the load. The power source voltage is directly imposed onto the primary of the transformer T1, and therefore, the voltage across the transformer is always a square wave, no matter what the load and no matter how the load power facto varies. The current wave form in the primary of the transformer T1, is a different story. It is affected by changes in load, and most

important, it is affected by changes in power factor.

(i) THE EFFECTS OF POWER FACTOR:-

Now let us examine the current wave form in the primary of T1, under various power factor conditions. The current wave form (in phase relationship) in the primary of T1 is composed with the voltage impressed by the power source across the primary of T1, when load is a pure resistive load(power factor1.0). This comparison reveals wave forms as illustratedin fig 1.9.

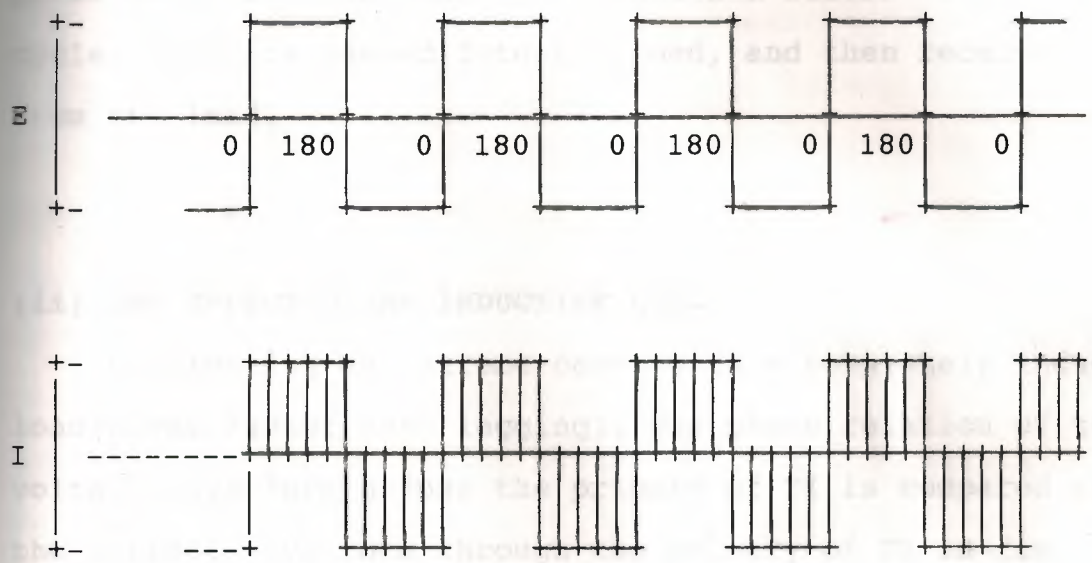


fig. 1.9

The current wave form will be identical to the voltage

wave form. It can be seen that each switch is conducting a full 180 degrees, and current through the switch , and through the transformer primary, is as high as required to deliver the power demanded by the load. The power delivered by each switch through the transformer primary is represented by the formula P= E I dt. When the voltage and current are both in phase, and square in wave form, then the cross hatched areas in the current wave forms are proportional to the power delivered by the each semiconductor switch.

An AC power source that is operating into a power factor load, is delivering power to the load, and then receiving power back from the load. This function occurs with each half cycle. Power is pushed into the load, and then received back from the load.

(ii) THE EFFECT OF AN INDUCTIVE LOAD:-

Considering an extreme case, with a completely inductive load(power factor zero lagging). The phase relation of the voltage wave form across the primary of T1 is compared with the current wave form through the primary of T1 in fig. 1.10.

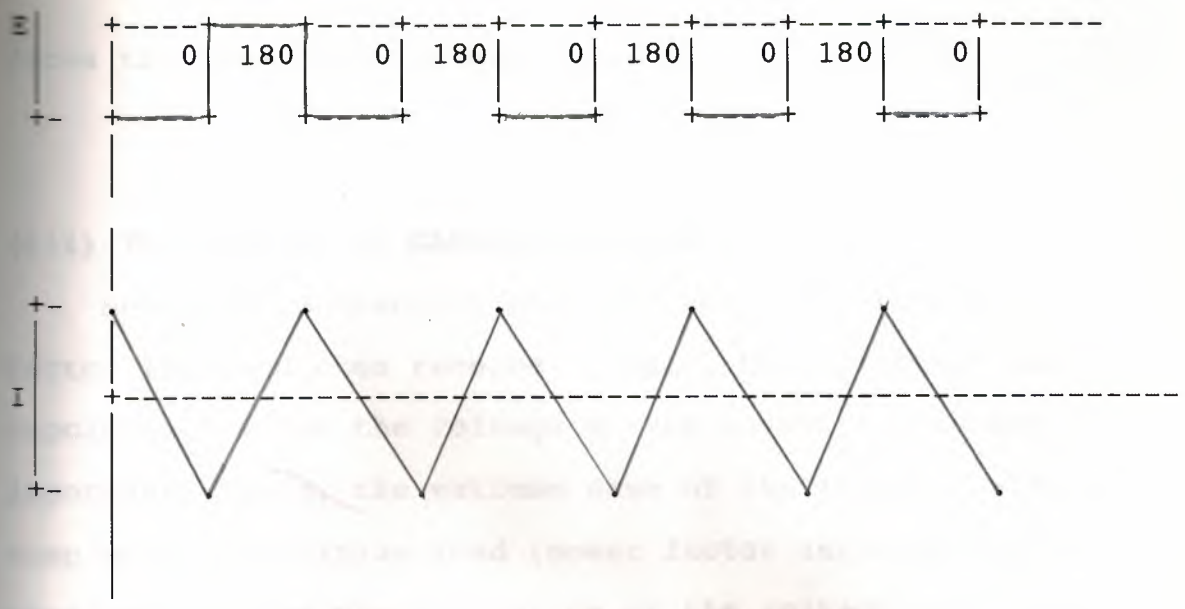


fig. 1.10

When the voltage driven inverter must operate into an inductive load, the power that the load attempts to feed back in to transformer T1 effects the current wave form in the primary, semiconductor switch S1 should begin conduction at the 0 degree conduction angle, but the inductive load is attempting to force a reverse current flow through the switch. Because all semiconductor switches are unidirectional, the switch blocks the required reverse current. This interruption of the current flow from the load, when it is at its maximum point, causes a reverse voltage spike to build up on the primary of T1, and this spike rises until it fails(short circuits) the semiconductor switch. In theory, the spike could rise to an infinite voltage, and therefore, the voltage rating of the semiconductor switch is of no consequence; it still will fail. When switch S2 attempts to conduct, at the 180 degree conduction angle, it

faces the same untimely end.

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(iii) THE EFFECTS OF CAPACITIVE LOAD:-

Because the inverter must deliver power into a power factor load and then receive it back, the effect of the capcitive load on the voltage driven inverter also are important. Again, the extreme case of the inverter with a completely capacitive load (power factor zero leading) is examined and the phase relation of the voltage wave form across the primary of T1 is compared with the current wave form through the primary of T1 in fig. 1.11.

Similarly to the situation encountered with the inductive load, a capacitive load changes the current wave form through the primary of T1, but the voltage remains uneffected. The voltage wave form remains square wave, but tremendous current spikes now appear in the primary each time the semiconductor swatches begin to conduct. When the switches begin conducting, they are supplying power to reverse charge
the capacitor through a very low impedance. With a voltage constant, the current rises to extremely high levels. Until the capacitor charge rises, there is a very little impedance to slow the current in rush, other than the slight resistance in the transformer wire and the saturation resistance of the semiconductor switches.

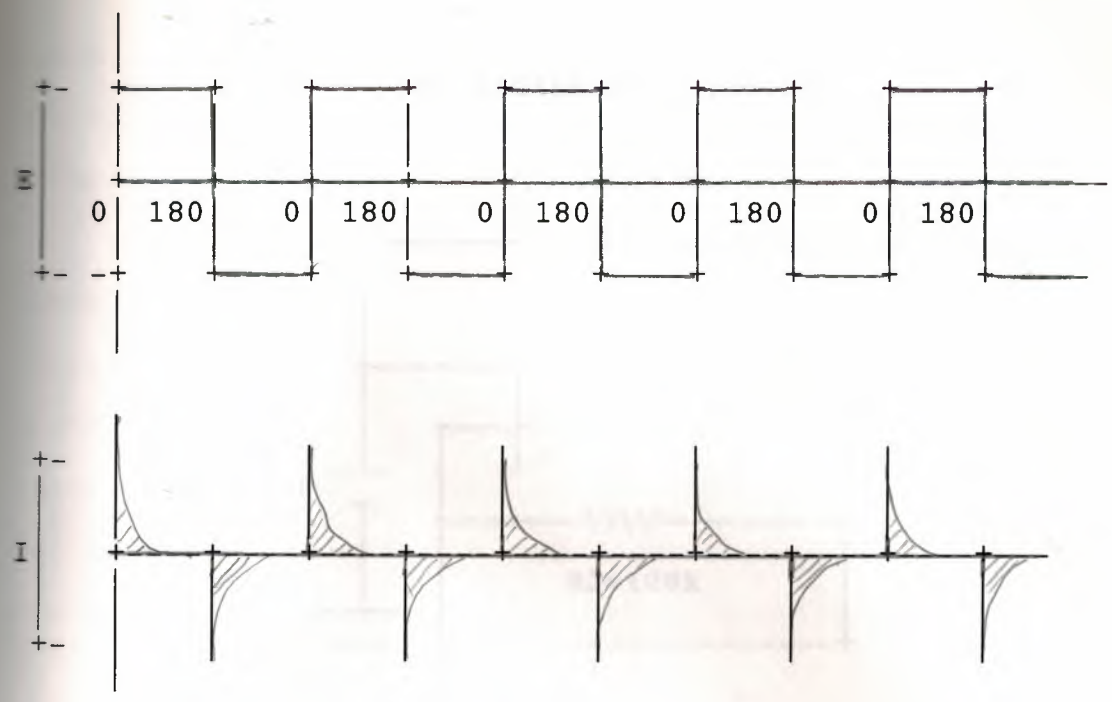


fig. 1.11

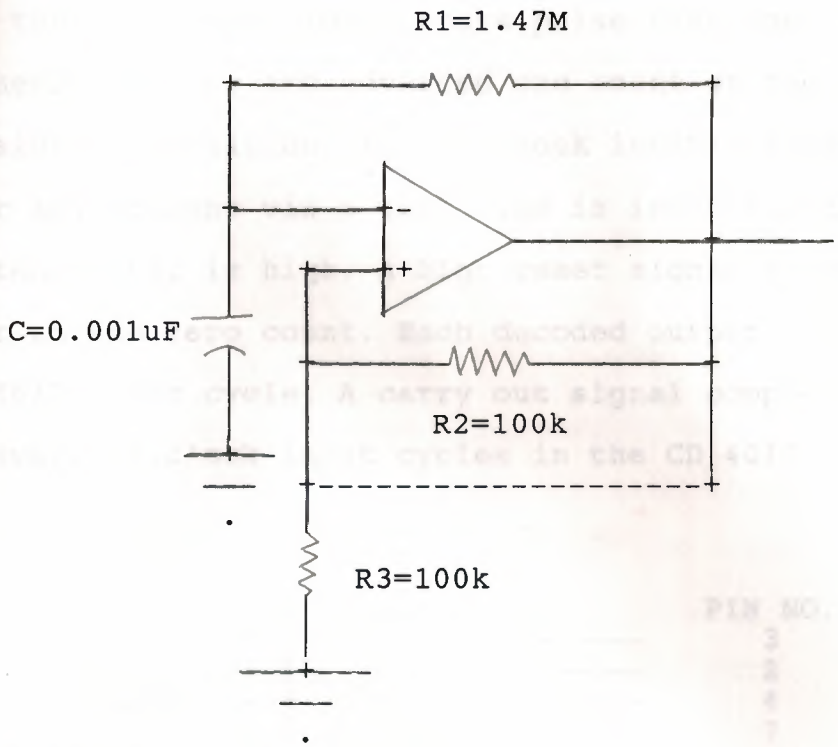
Because the current level rise to such a extremely high values as each switch begins to conduct, the I*I*R losses in the inverter suddenly rise to a very high values, and the efficiency decreases.

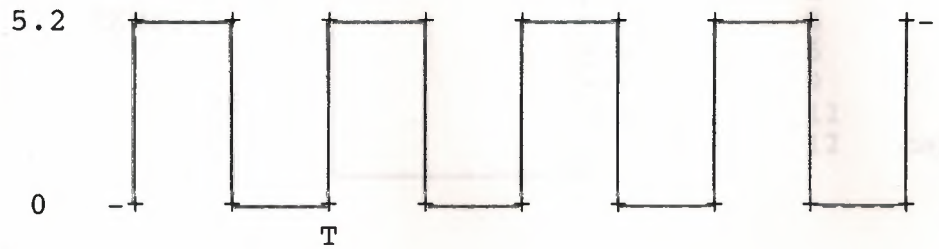
The end result of these current spikes on the operation of the semiconductor switches is permanent device destruction. The high peak currents cause transistor switches to run out of the drive power and pull out of saturation into a high dissipation mode of operation. In very short time they burn out. SCR switches simply generate instantaneous hot spots due to the extremely high peak currents and also burn out.

CHAPTER TWO

ANALYSIS AND OPERATION

THE OSCILLATOR CIRCUIT





$$T = R1\ C\ \ln \frac{1+B}{1-B}$$

$$B = \frac{R2}{R1+R2} = \frac{100}{200} = 0.5$$

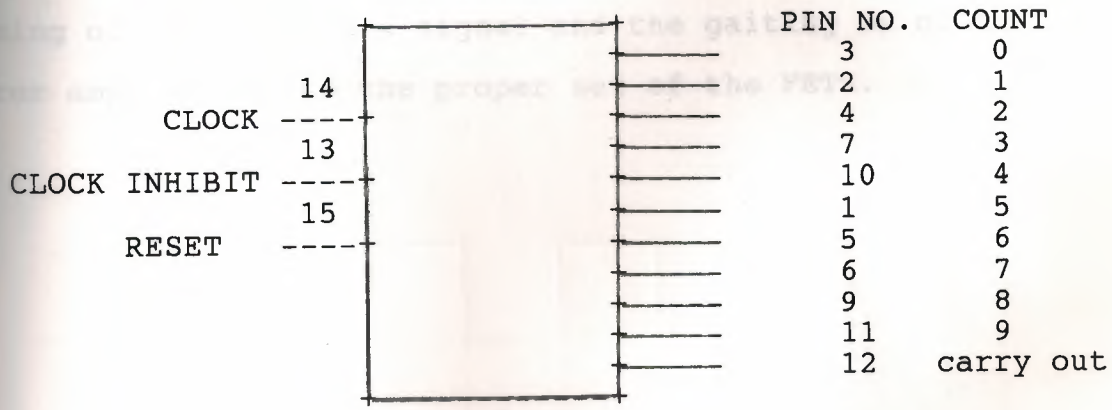
$$T = 309.6\ \text{Hz}$$

IC2:THE DECADE COUNTER

It is decade counter with 10 outputs. Inputs include a

clock, a reset, and a clock inhibit signal. Schmitt trigger action in the clock input circuit provides pulse shaping that allows the unlimited clock inputs pulse rise and fall time.

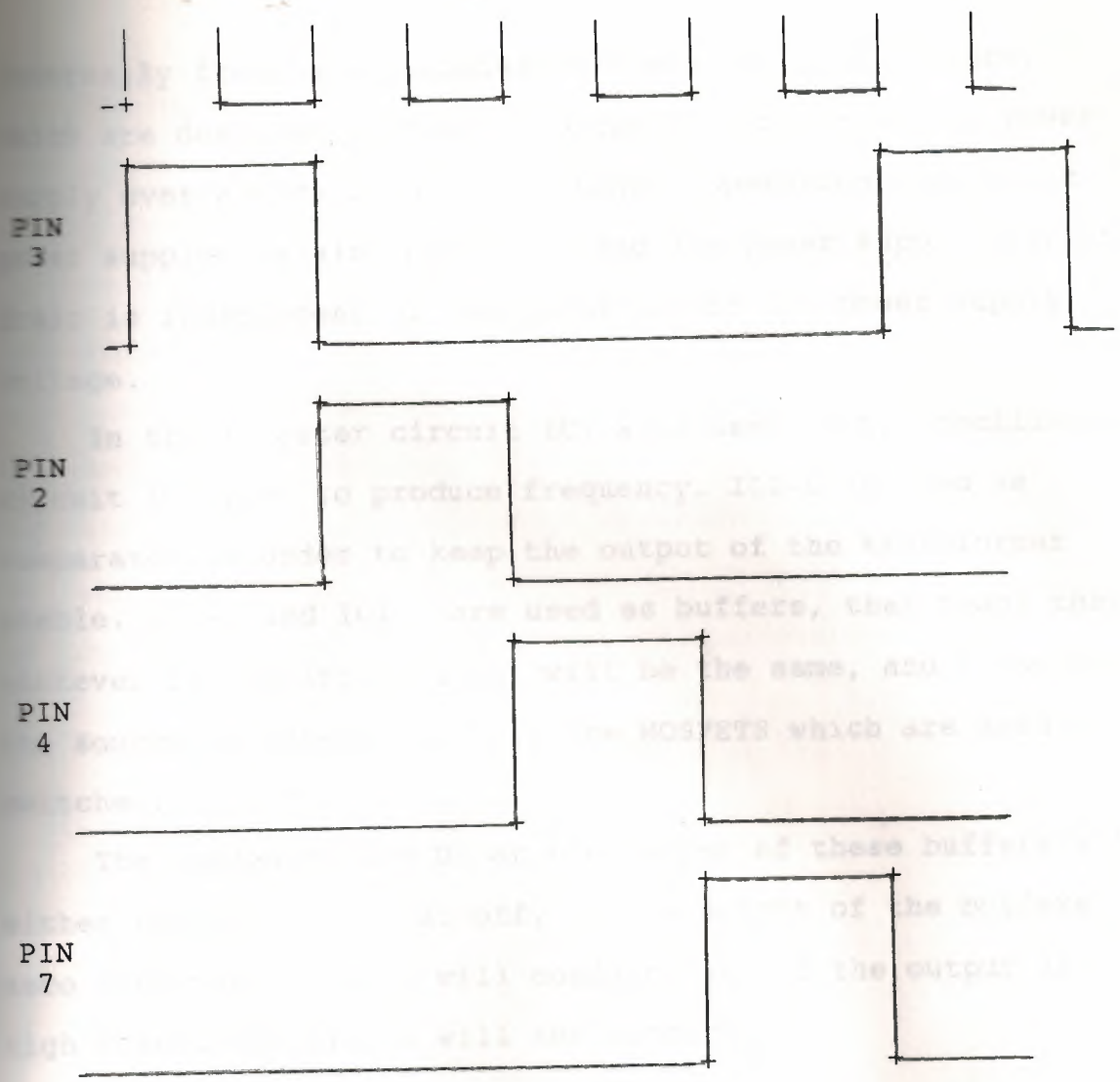
These counters are advanced one count at the positive clock signal transition, if the clock inhibit signal is low. Counter advancement via a lock line is inhibited the clock inhibited signal is high. A high reset signal clears the counter to the zero count. Each decoded output remains high for a full clock cycle. A carry out signal completes one cycle every 10 clock input cycles in the CD 4017.



FEATURES:-

- Faulty static operation.
- Medium speed operation (10 M Hz at Vdd = 10v)
- 100% tested for quiescent current at 20V.
- 5v,10v and15v parametric ratings

In inverter circuit the 4017 is used as the frequency divider. It divides the frequency of the clock input by 4. Since pin 10 is connected to pin 15, so after counting 3 , it will reset and start counting from zero again. The frequency produced by the oscillator is 309.6Hz and this counter divides the frequency by 4, and it becomes 77.4Hz. The 77.4 rather then 60 Hz is used to avoid transformer saturation. Decade counter IC2 controls the timing of the reference signal and the gaiting ON of the error amp. signal to the proper set of the FETS.



IC1: LM 324

The LM 324 consists of four independent, high gain,

internally frequency compensated operational amplifiers, which are designed specially to operate from a single power supply over a wide range of voltages. Operation from split power supples is also possible, and low power supply current drain is independent of the magnitude of the power supply voltage.

In the inverter circuit IC1-a is used in the oscillator circuit in order to produce frequency. IC1-b is used as comparator in order to keep the output of the transformer stable. IC1-c and IC1-d are used as buffers, that means that whatever is the input output will be the same, and these are the source to gate-ON and off the MOSFETS which are used as switches.

The diodes D1 and D2 at the output of these buffers will either conduct or in cut off. If the output of the buffers is zero then these diodes will conduct, and if the output is high then these diodes will not conduct.

IC3-LM 7805: THE VOLTAGE REGULATOR

The LM-78XX series of three terminals regulators is available with several fixed output voltages, making them useful in wide range of applications. One of these is located on card regulation, eliminating the distribution problems, associated with single point regulation. The voltage available, allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipments. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

FEATURES:-

- Output current in excess of 1A.
- Internal thermal over load protection
- No external components required.
- Output transistor safe area protection
- Internal short circuit current limit.

In the inverter circuit LM_7805 is used, so the voltage range is 5 volts, which is used as a reference voltage.

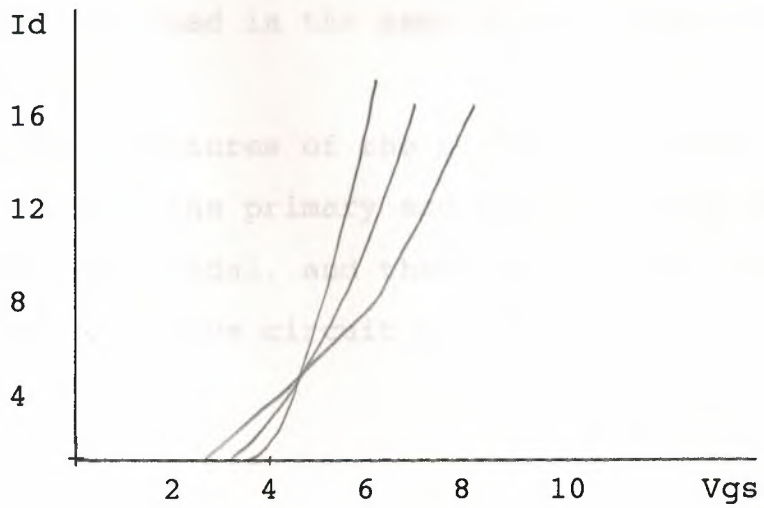
THE IRF-511 60 volts 3.5amp. MOSFET

The IRF-511 power MOSFET transistors have very low ON-state resistance combined with high transconductance and great device raggedness.

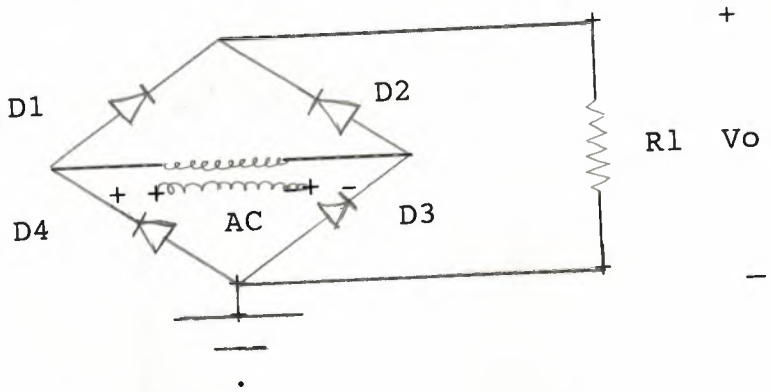
These transistors also feature all of the well established advantages of the MOSFETS such as voltage control, freedom from second break down, very fast switching, ease of the paralleling, and temperature stability of electrical parameters.

In the inverter circuit, these are used as switches. When ever the gate source voltage (Vgs) is low, these are gated off and when the gate source voltage is high these are gated-ON. These mosfets behave as excellent switches.

Characteristic of the MOSFET



THE BRIDGE RECTIFIER

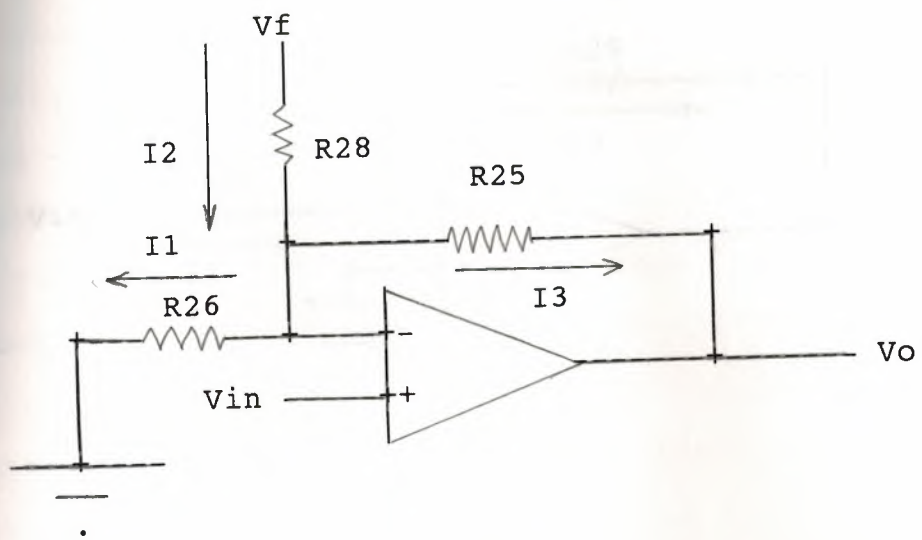


The circuit shown above is bridge rectifier. To understand the operation of this circuit, it is necessary only to note that two diodes conducts simultaneously. For example during the portion of cycle when the transformer polarity is that which is shown in the fig. D1 and D3 are conducting, and current passes from positive to the negative of the load. During the next half cycle, the transformer voltage reverses its polarity, and diodes 2 and 4 send current through the load in the same direction as during the previous half cycle.

The principal features of the bridge rectifier are, the current down in both the primary and the secondary of the transformer are sinusoidal, and therefore smaller transformer may be used for full wave circuit of the same output.

TRANSISTOR NOT CONDUCTING

The simplified fig. is as follows:



$$Vin = 5v$$

$$I1 = Vin/R26$$

$$I2 = \frac{Vf-Vin}{R28}$$

$$I2 = I1 + I3$$

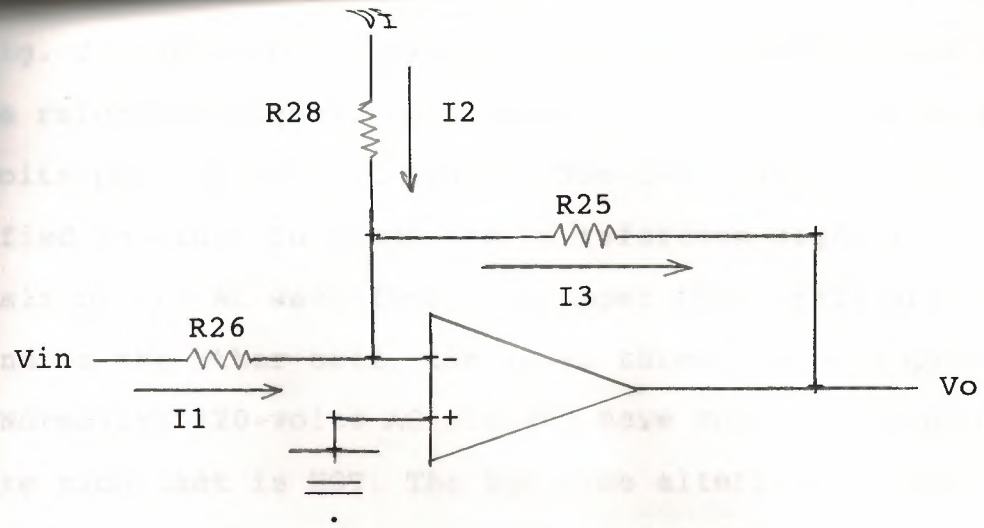
$$I3 = I2 - I1$$

$$Vo = R26 * (-I3) - R25\ (I1)$$

$$Vo = V1 - R25[(Vf - Vin)/ R28 - Vin/R26]$$

$$Vo = 2.23\ Vin - 0.213\ Vf$$

TRANSISTOR NOT CONDUCTING



$$Vin = 5v$$

$$I1 = Vin/R26$$

$$I3 = I1 + I2$$

$$I3 = [\ Vin/R26 + Vf/R28]$$

$$Vo = -\ R25 * I3$$

$$Vo = -\ R25\ [\ Vin/R26 + Vf/R28]$$

$$Vo = -(Vin + 0.213\ Vf)$$

INVERTER OPERATION

The inverter, the schematic diagram of which is shown in

the fig. 2.1 is actually push-pull audio amplifier. The input or the reference signal, is 5 volts square wave. The output 340 volts peak to peak AC signal. The feed back signal is rectified in order to match the DC reference signal. On the one half of the AC wave form, the upper three FETs are gated ON, and on the other half, the lower three FETs are gated ON.

Normally, 120-volts AC outlets have one side at ground and one side that is HOT. The hot side alternates from -170-170 volts. The inverter output is little different. On one half of the AC cycle, one side is nearly ground and other is at +170. During the other half of the cycle the situation is reversed.

Operation amplifier IC1-a and its associated components form approximately 300 Hz clock oscillator and the counter IC-2 divides the clock signal by four to obtain a 75 Hz inverter frequency and after counting four pulses that is counting 0, 1, 2, 3 it RESETS and start counting again from zero, since pin 10 is connected to pin 15 which the RESET pin. The 75 Hz rather than 60 Hz is used to avoid transformer saturation. Some electronic clocks will run fast with that frequency, but most electronic gear will work just fine. Decade counter IC2 controls the timing of the reference signal and the gating on of the error amplifier signal to the proper set of the FETs. The timing diagram is shown below.

CLOCK 

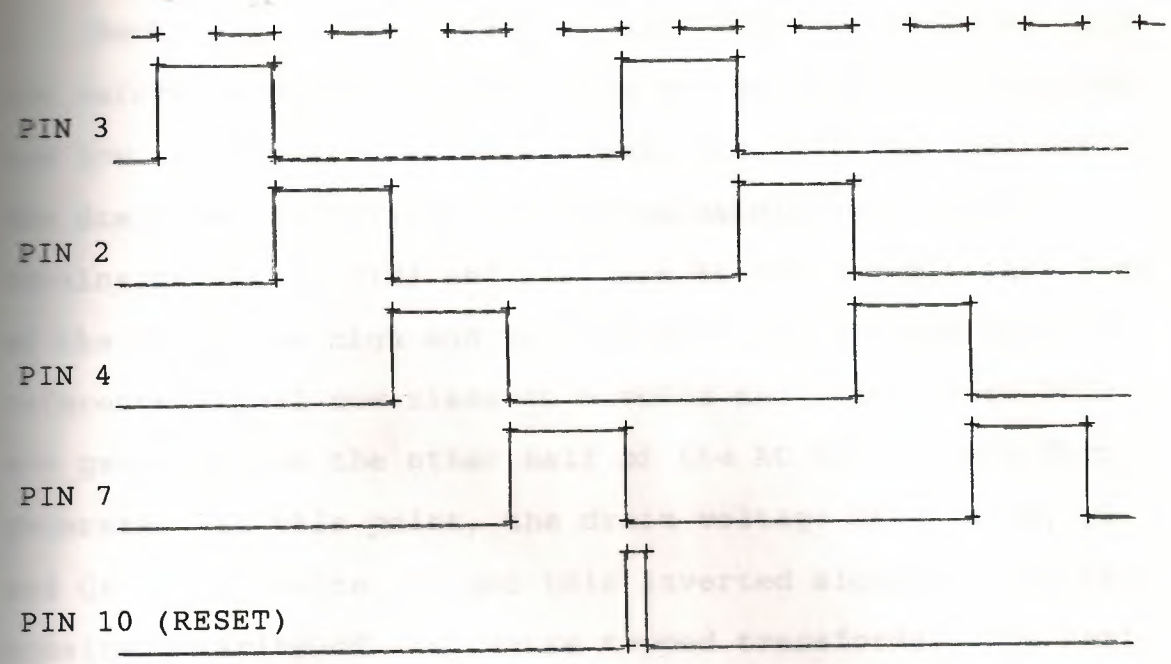


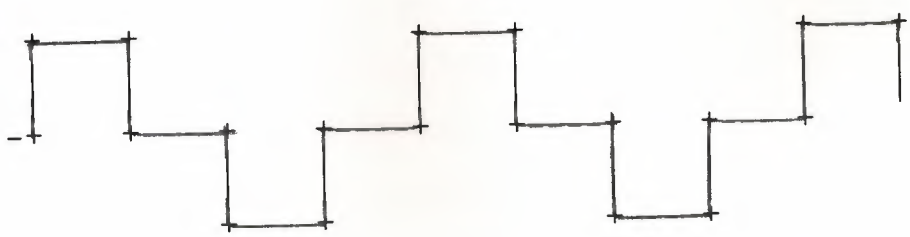
FIG 2.1

When IC2, pin 3 goes high, the output of the buffer IC1-c is high, that reverse biases the D1 and allows the error amplifier signal to reach Q1, Q2, Q3 and the common drain of the Q1, Q2 and Q3 which is attached to the primary of the centre tapped transformer T1, are at 12 volts till the output of the pin3 remains high.

At the same time, IC2 pin 4 is low which causes the output of the buffer IC1-d to be low, that grounds the gates of Q4, Q5, and Q6 and therefore turning them OFF. A 5 volts reference from the regulator IC3 is now present at the error amplifier IC1-b, non inverting input. The reference signal rise time is slowed by R12 and C2 in order to avoid the output overshoot, and the gain and the frequency response of the error amplifier is set by R15, R25 and C3.

Next, pin2 of the IC2 goes high which turns Q7 on, and the reference signal is pulled to ground. PIN3 and PIN4 are now low and the FETs gates are grounded, turning them OFF, the drain of the FETs is now approximately zero, and it remains zero till PIN3 and PIN4 are at zero level. Then PIN4 of the IC-2 goes high and reverse bias the D2, and the reference signal now rises to 5 volts and other three FETs are gated ON and the other half of the AC output wave form is generated. at this point, the drain voltage of FETs Q4, Q5 and Q6 is -12 volts. We got this inverted signal due to the oposite polarity of the centre tapped transformer. The next clock pulse causes the pin7 of the IC2 to go high, all FETs are now OFF and the reference is set to zero. The following clock pulse resets IC2 and another cycle begins.

If we consider the FETs Q1, Q@, and Q3 as a switch A and FETs Q4, Q5 and Q6 as the switch B, then the output of these two switches in accordance to the timing diagram is shown below.



A filter that protects the CMOS circuitry against

alternates spikes and reverse input polarity is formed by R7, C8 and D7. Components R9 and C4, filter output spikes, and R18-R21 are pre load resistors to stabilize the inverter when no load is connected. Although the FETs have no current-equalizing source resistors, they still share current fairly equally. (When a FET Hog current, it heats up more and its on resistance increases, causing it to draw less current).

CHAPTER THREE

SUMMARY AND CONCLUSION

SUMMARY OF THE VOLTAGE-DRIVEN INVERTER PROBLEM

A summary of the problems inherent in the voltage driven inverter circuit, and the reasons why these problems are present is presented below.

(i) The voltage-driven inverter can handle inductive power factor only through a limited range, and only with difficulty. This is because the voltage-driven inverter holds the voltage fixed in phase relative to a switch conduction, being unidirectional current device, will not operate in this mode. Auxiliary circuit are necessary to either burn up the power, fed back from the inductive load, or bypass the switches and return the power to the power source.

(ii) The voltage driven inverter can not handle a capacitive power factor. Bleeder resistor to modify the power factor have to be used, or a series impedance in the output is necessary to restrict the current surges. The inverter will still destroy the switches if the power factor of the load becomes leaking to an approximate extent.

(iii) The voltage driven inverter utilization of the semiconductor switches is poor. The current rating of the switches must be several times larger than necessary to handle the current peaks created by the power factor loads. The high peak currents for short durations are not a desirable condition for the operation of semiconductors, therefore the reliability of the switches is not good.

(iv) The voltage driven inverter utilization of the output of

the power transistor is poor. Because of the short conduction time, causing high peak currents as required by the power factor loads, and will be larger and heavier than necessary.

(v) The voltage driven inverter circuits will have to be large and heavy. The actual volt-ampere circulating in the filter circuits will be large, causing losses and driving up the size and weight of the filter section.

(vi) Voltage driven inverter can not use simple, efficient pulse-width modulation as a means of regulation because of the transformer problem, and because of the circulating currents required by the filter section. Almost with out exception, voltage driven inverter use pre regulator, decreasing efficiency due to double conversion losses, or they use phase shift, forcing the use of multiple inverters for every output provided.

(vii)Voltage driven inverters are never satisfactory when they operate with motors as loads, because the current surge capacity required during motor start up is always coupled with highly inductive power factors, and these conditions change through wide ranges, as the motor comes up to speed. The worst case condition for the voltage driven inverter is when a single motor constitute the only load that the inverter has to drive.

(viii) The voltage driven inverter is a highly intensity generator of radiated and conducted EMI. This is inherent in the circuit. Extensive fixes must be incorporated in each different voltage driven inverter, depending on its

application to reduce these EMI levels. Even with the fixes, it is seldom that the radiated and conducted EMI can ever be brought down to acceptable levels of MIL-I-26600 or MIL-I-6181, standards and keep the inverter size and weight with in reason.

GENERAL CONCLUSION

This project gives a comprehensive knowledge about INVERTERS. Inverter is a device which coverts DC power to AC power at some desired output and frequency. There are several design considerations that are common to all inverters, that include, the feed back which might be of voltage feed back, current feed back or phase feed back. Then comes the design of the power stage, it is most important part since most of the power is dissipated here. Inductive switching in transistors, efficiency and input and output filters are also key points to be considered for the inverter design.

The INVERTERS are classified in two categories. Firstly the voltage driven inverters, secondly, the current driven inverters. My project is based on the first type, that is the voltage driven inverters. The voltage driven inverter is the one in which the design of the circuit connects the DC voltage source through the semiconductor switches, directly to the primary of the transformer.

The switching drive circuit alternately saturates and cuts off the semiconductor switches, causing an alternating voltage to be generated across the windings of the transformer, and to be delivered to the load. The power source voltage is directly impressed on the primary of the transformer, and therefore, the voltage across the transformer is always a square wave, no matter what the load and no matter how the load power factor varies.

To my father, mother, brothers & sister.

ACKNOWLEDGMENT

I would like to express my special thanks to my supervisor Assoc.Prof.Dr Senol Bektas , who gave me a lot of knowledge and skills to carry on with this project. Also I would like to thank my friends who helped me in completing this project.

The output of the buffers should be the same as the
t but I observed that output of the buffers is different
the input . There should be two voltage levels but I
erved three levels , these are approximately 9.0 , 1.6 ,
0 volts . At the high level the switches should be at ON
te and at lower level these should be in OFF state . But
the third level which is 1.6 volts these FETs conduct
tially and because of this the output of the inverter is
troyed . The cause of this third level is due to the
F-SET voltage of the buffers .

This problem may be solved by using the buffers with
ry low OFF-SET voltage .

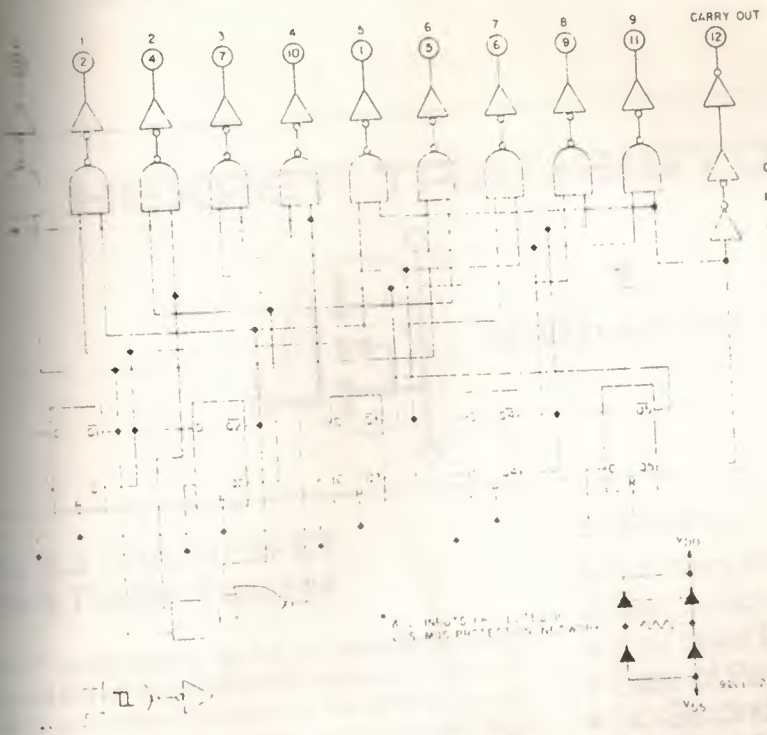


Fig. 1 – Logic diagram for CD4017B

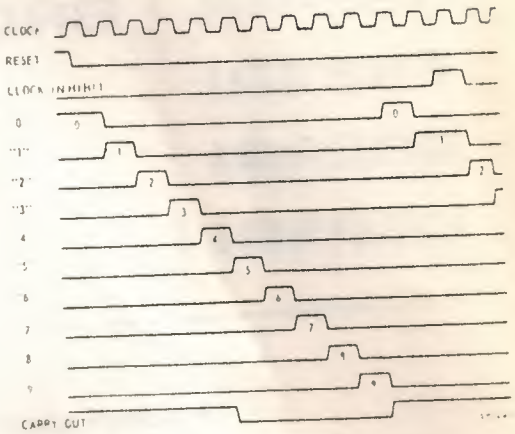


Fig. 2 – Timing diagram for CD4017B.

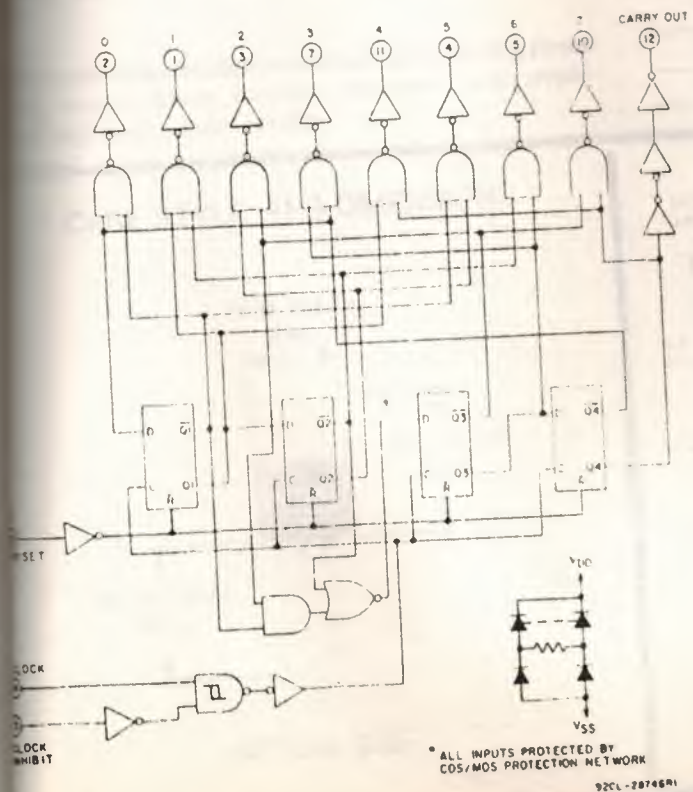


Fig. 3 – Logic diagram for CD4022B.

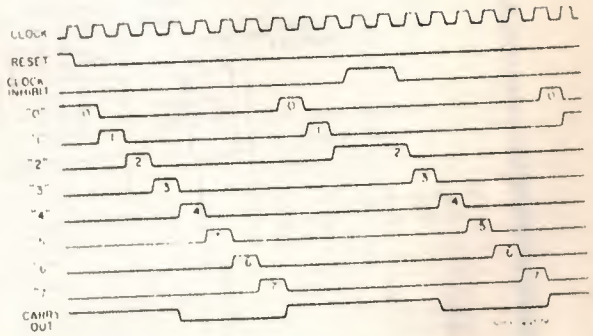
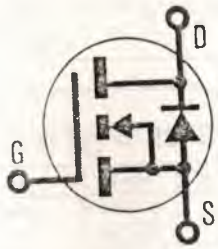


Fig. 4 – Timing diagram for CD4022B.

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF520
IRF521
IRF522
IRF523



N-Channel

0.3 Ohm HEXFET
AB Plastic Package

technology is the key to International Recti- line of power MOSFET transistors. The effi- and unique processing of the HEXFET design low on-state resistance combined with high nce and great device ruggedness.

transistors also feature all of the well estab- ages of MOSFETs such as voltage control, free- second breakdown, very fast switching, ease of and temperature stability of the electrical param-

suited for applications such as switching power tor controls, inverters, choppers, audio amplifi- energy pulse circuits.

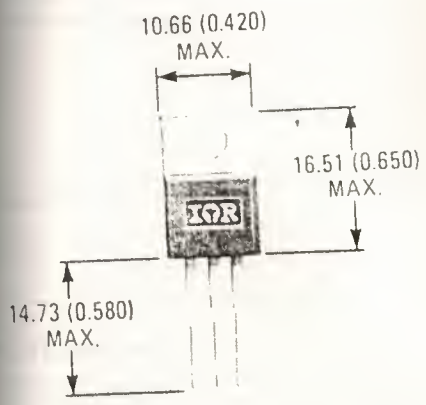
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

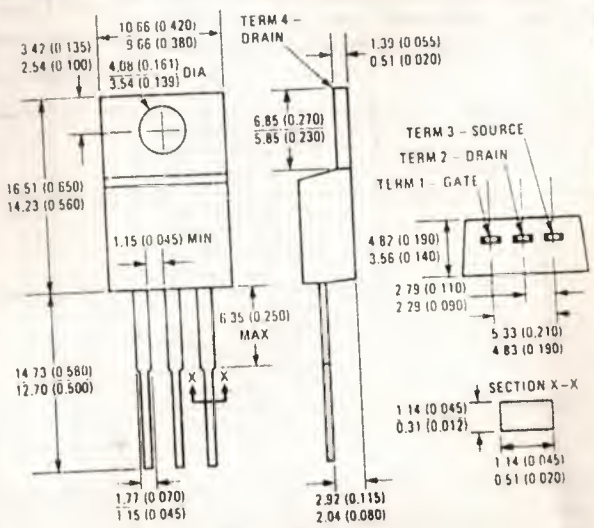
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF520	100V	0.30Ω	8.0A
IRF521	60V	0.30Ω	8.0A
IRF522	100V	0.40Ω	7.0A
IRF523	60V	0.40Ω	7.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

IRF521, IRF522, IRF523 Devices

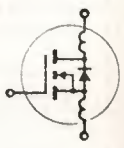
Maximum Ratings

Parameter	IRF520	IRF521	IRF522	IRF523	Units
Drain - Source Voltage ①	100	60	100	60	V
Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
Continuous Drain Current	8.0	8.0	7.0	7.0	A
Continuous Drain Current	5.0	5.0	4.0	4.0	A
Pulsed Drain Current ③	32	32	28	28	A
Gate - Source Voltage	±20				V
Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/K
Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				
	32	32	28	28	A
Operating Junction and Storage Temperature Range	−55 to 150				°C
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
Source Breakdown Voltage	IRF520, IRF522	100	–	–	V	V_{GS} = 0V
	IRF521, IRF523	60	–	–	V	I_D = 250μA
Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = -20V
Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
Drain Current ②	IRF520, IRF521	8.0	–		A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
	IRF522, IRF523	7.0	–	–	A	
Drain-Source On-State Resistance ②	IRF520, IRF521	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
	IRF522, IRF523	–	0.30	0.40	Ω	
Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
Capacitance	ALL	–	200	400	pF	
Transfer Capacitance	ALL	–	50	100	pF	
On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Time	ALL	–	35	70	ns	
Off Delay Time	ALL	–	50	100	ns	
Time	ALL	–	35	70	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 15V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	ALL	–	6.0	–	nC	
Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
		–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

Junction-to-Case	ALL	–	–	3.12	K/W	
Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF520 IRF521	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF522 IRF523	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF520 IRF521	–	–	32	A	
		IRF522 IRF523	–	–	28	A	
V_{SD}	Diode Forward Voltage (2)	IRF520 IRF521	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF522 IRF523	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

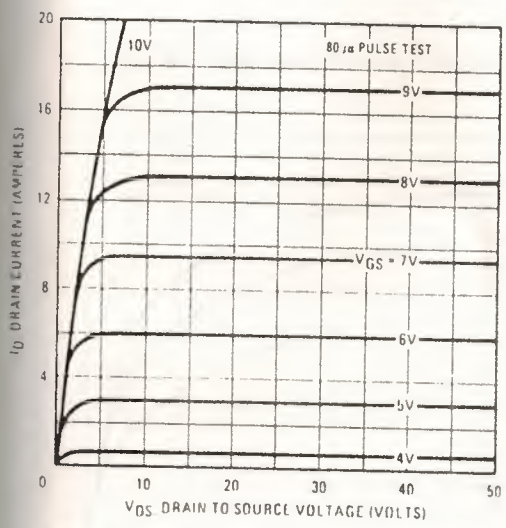


Fig. 1 — Typical Output Characteristics

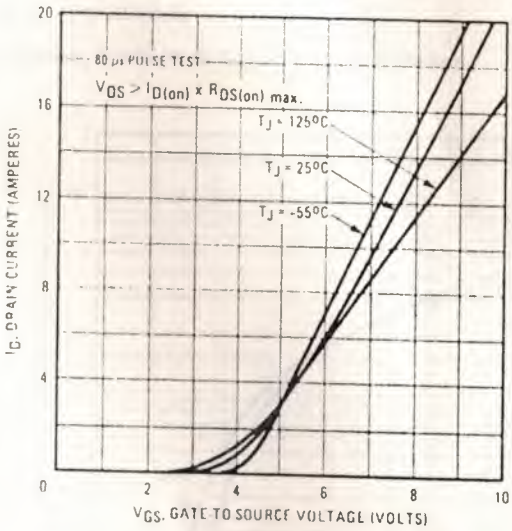


Fig. 2 — Typical Transfer Characteristics

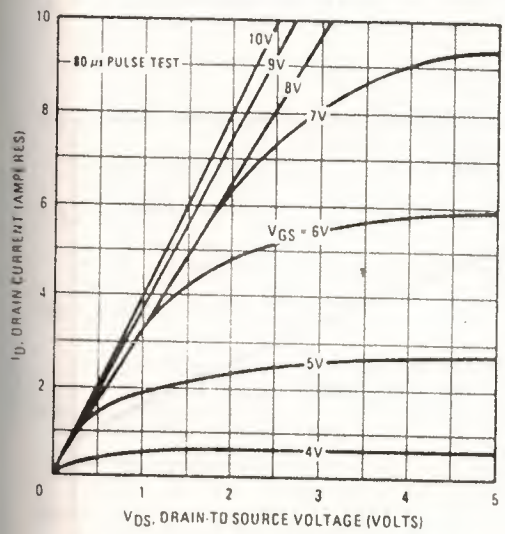


Fig. 3 — Typical Saturation Characteristics

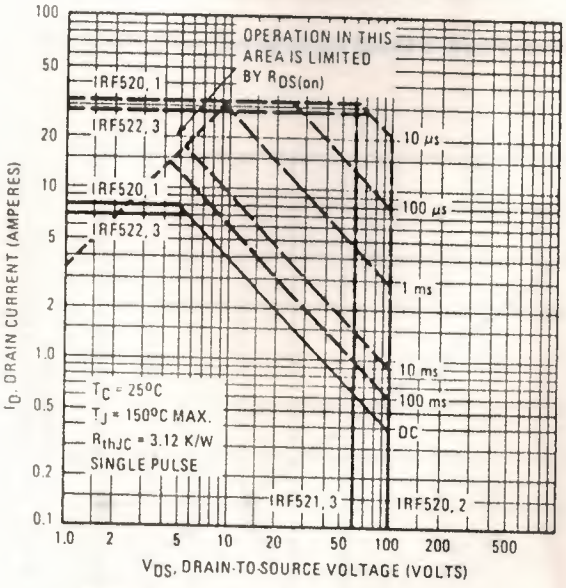


Fig. 4 — Maximum Safe Operating Area

20, IRF521, IRF522, IRF523 Devices

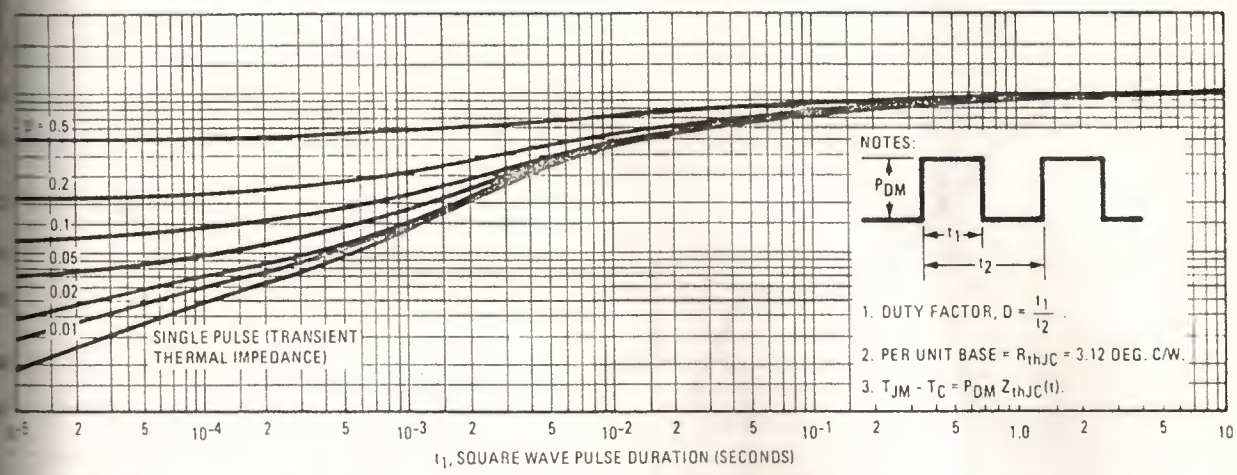


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

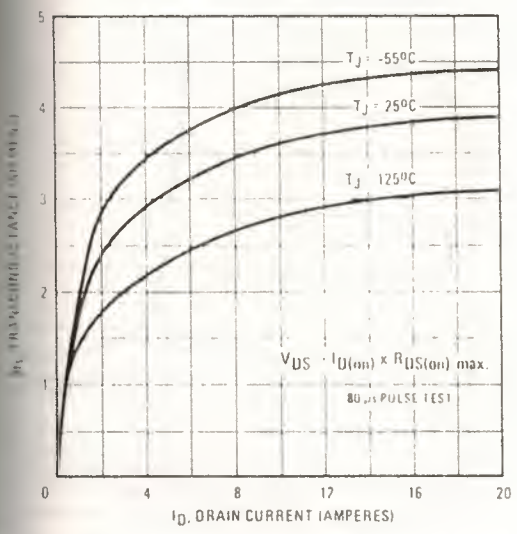


Fig. 6 – Typical Transconductance Vs. Drain Current

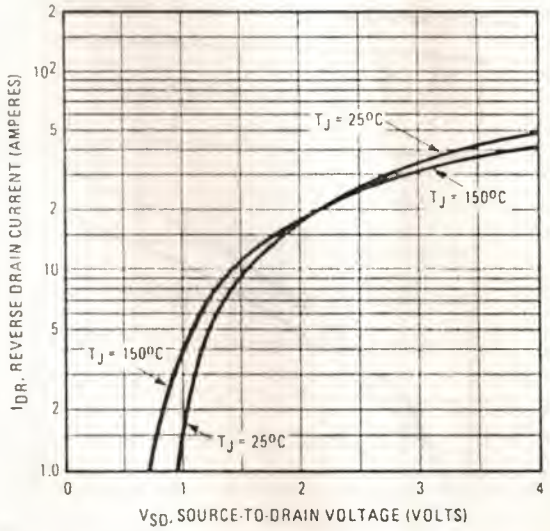


Fig. 7 – Typical Source-Drain Diode Forward Voltage

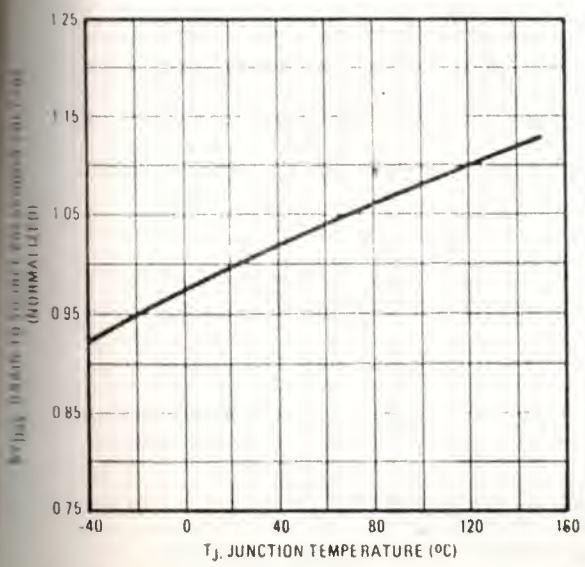


Fig. 8 – Breakdown Voltage Vs. Temperature

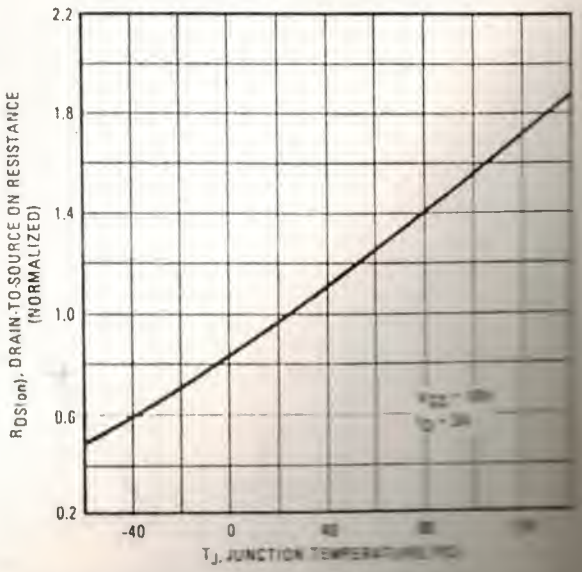
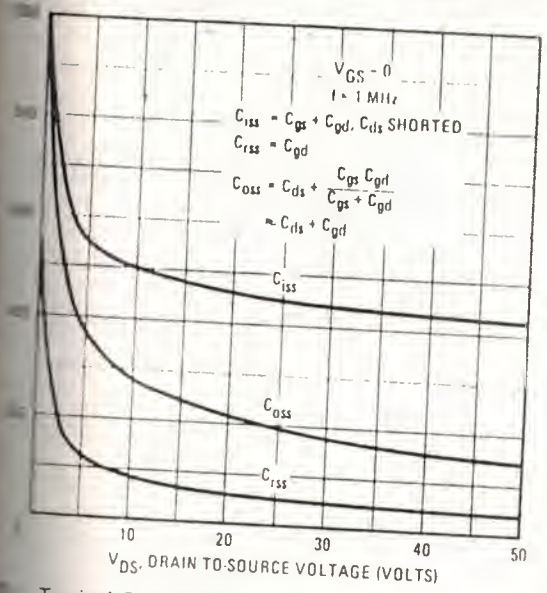


Fig. 9 – Normalized On-Resistance Vs. Temperature



– Typical Capacitance Vs. Drain-to-Source Voltage

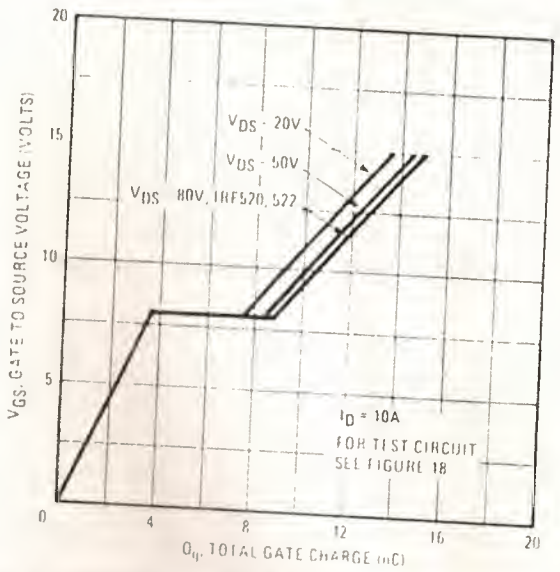
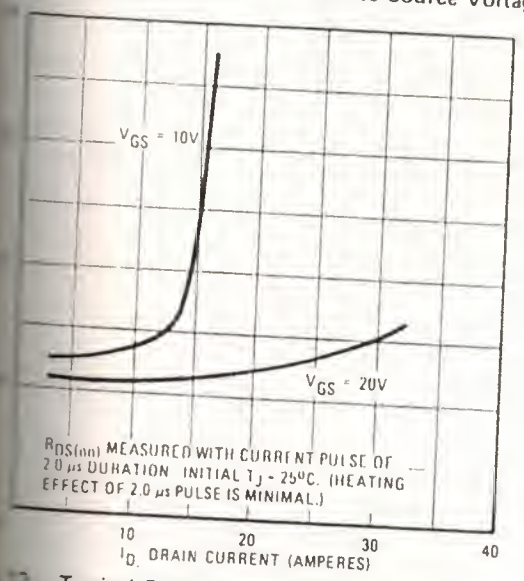


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage



2 – Typical On-Resistance Vs. Drain Current

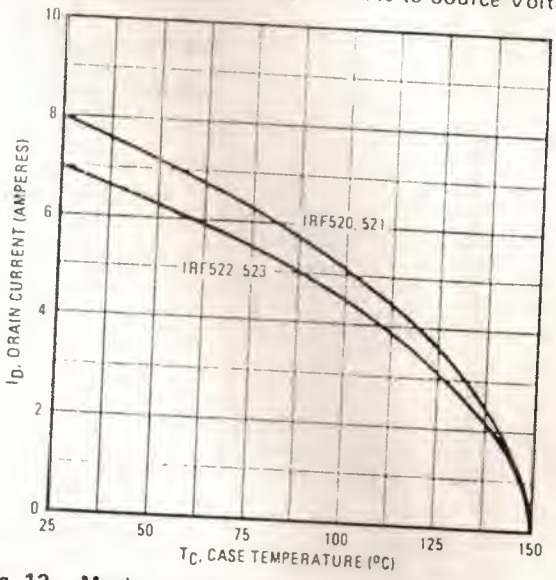


Fig. 13 – Maximum Drain Current Vs. Case Temperature

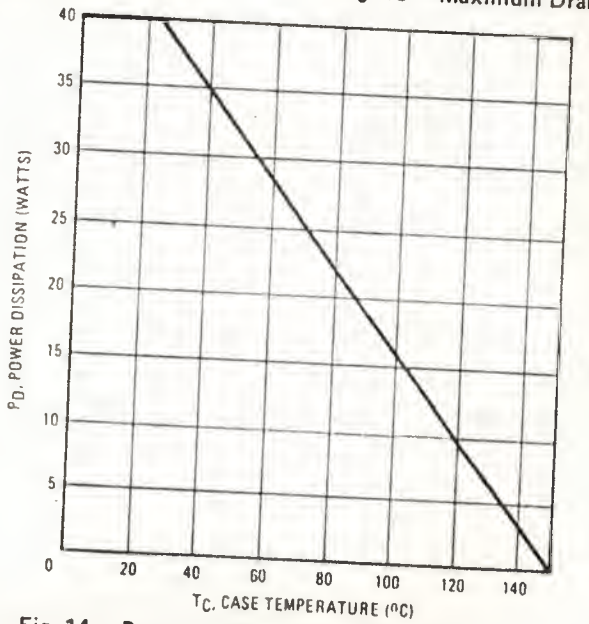


Fig. 14 – Power Vs. Temperature Derating Curve

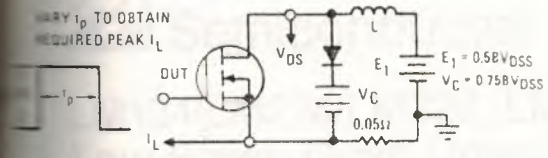


Fig. 15 — Clamped Inductive Test Circuit

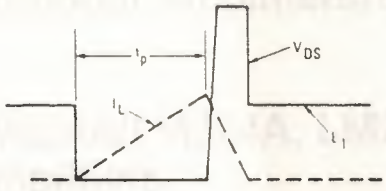


Fig. 16 — Clamped Inductive Waveforms

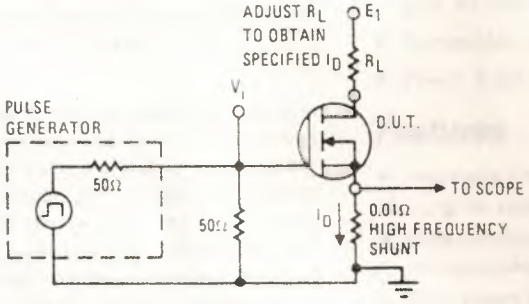


Fig. 17 — Switching Time Test Circuit

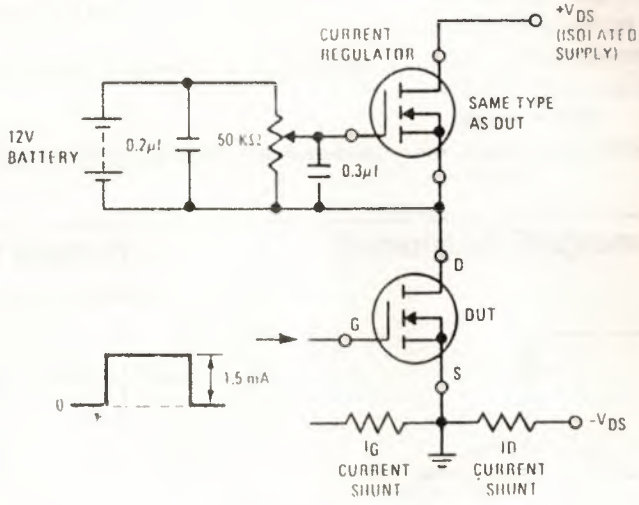


Fig. 18 — Gate Charge Test Circuit

National Semiconductor

Operational Amplifiers/Buffers

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

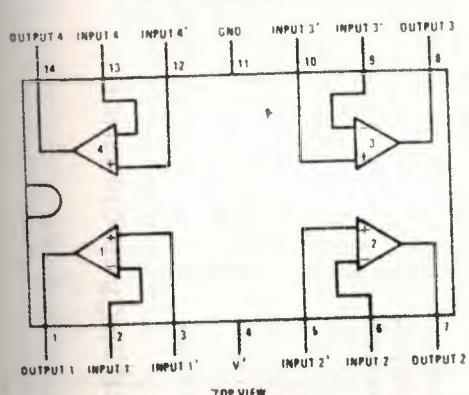
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain — 100 dB
- Wide bandwidth (unity gain) (temperature compensated) — 1 MHz
- Wide power supply range:
  - Single supply — 3 V_{DC} to 30 V_{DC}
  - or dual supplies — ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800μA) – essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated) — 45 nA_{DC}
- Low input offset voltage — 2 mV_{DC}
- and offset current — 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — 0 V_{DC} to V+ − 1.5 V_{DC}

Connection Diagram

Dual-In-Line Package

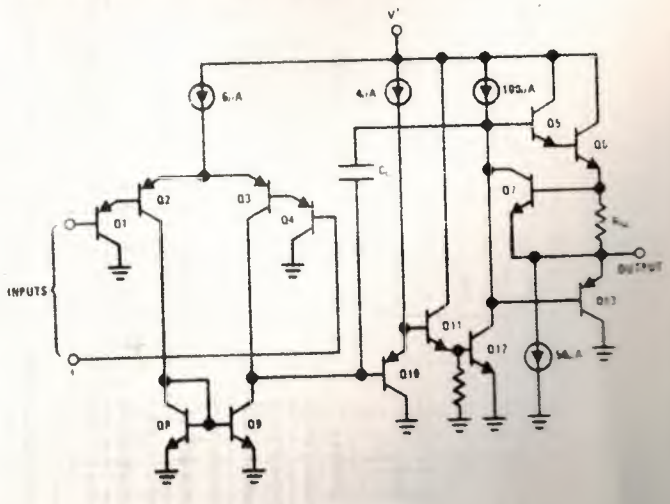


TOP VIEW

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N

Schematic Diagram (Each Amplifier)



Input Voltage	0.3 VDC to +32 VDC	-0.3 VDC to +26 VDC			
Power Dissipation (Note 1)					
Molded DIP	570 mW	570 mW	LM324, LM324A	0 C to +70 C	
Cavity DIP	900 mW		LM224, LM224A	25 C to +85 C	
Flat Pack	800 mW		LM124, LM124A	-55 C to +125 C	
Output Short-Circuit to GND (One Amplifier) (Note 2)	Continuous	Continuous	Storage Temperature Range	-65 C to +150 C	-65 C to +150 C
$V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$			Lead Temperature (Soldering, 10 seconds)	300 C	300 C

Electrical Characteristics ($V^+ = +5.0\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25$ C, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25$ C		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25$ C		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, $T_A = 25$ C	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2902 $V_{CC} = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA_{DC}
	$R_L = \infty$ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
	Over Full Temperature Range																			
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$, $T_A = 25$ C	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25$ C (LM2902 $R_L \geq 10\ k\Omega$)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, $T_A = 25$ C (Input Referred)		-120			-120			-120			-120			-120			-120		dB
Output Current																				
Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25$ C	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25$ C	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $T_A = 25°C$, $V_O = 200\ mV_{DC}$	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mADC

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7		$\mu V/^\circ C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/^\circ C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$, the LM324/LM324A temperature specifications are limited to $0^\circ C \leq T_A \leq +70^\circ C$, and the LM2902 specifications are limited to $-40^\circ C \leq T_A \leq +85^\circ C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$).

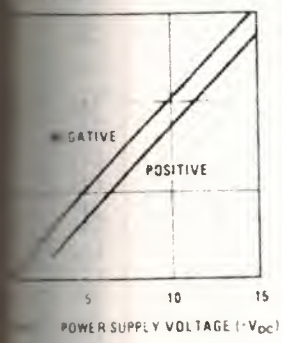
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).

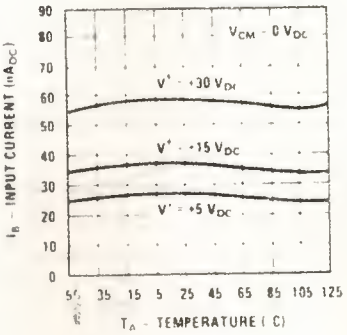
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Performance Characteristics

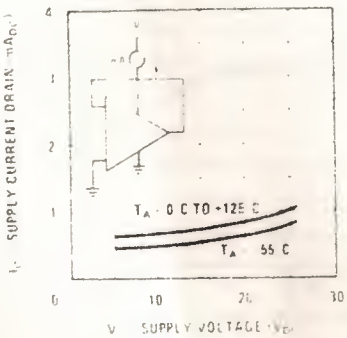
Voltage Range



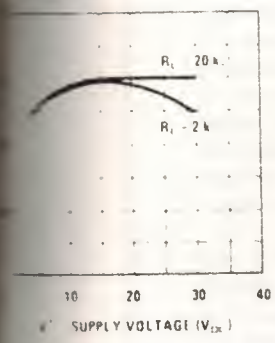
Input Current



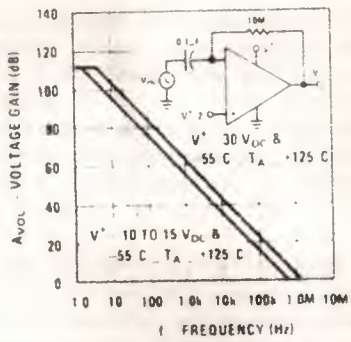
Supply Current



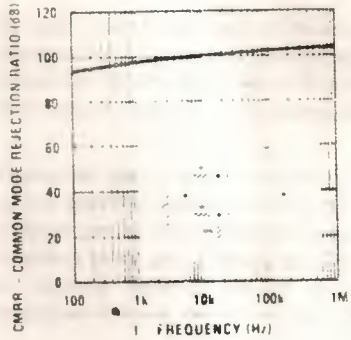
Voltage Gain



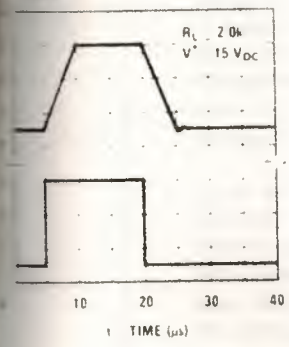
Open Loop Frequency Response



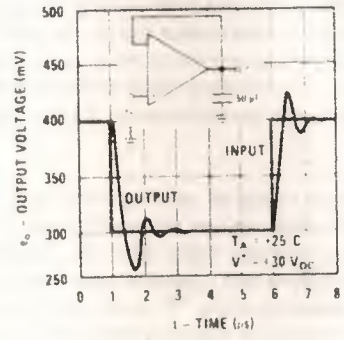
Common Mode Rejection Ratio



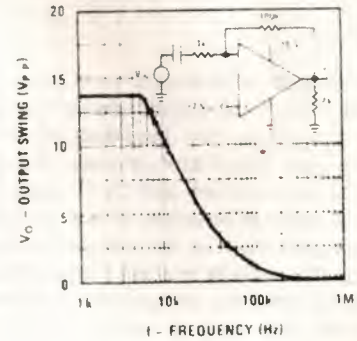
Voltage Follower Pulse Response



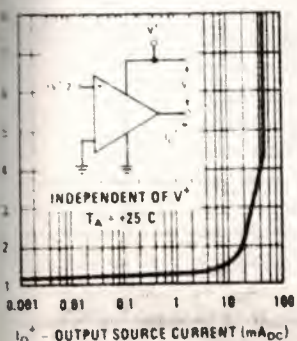
Voltage Follower Pulse Response (Small Signal)



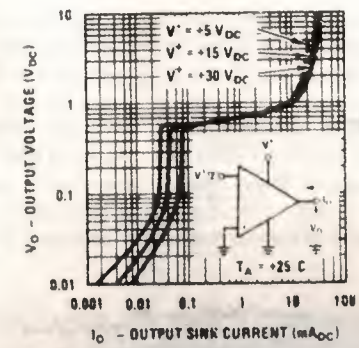
Large Signal Frequency Response



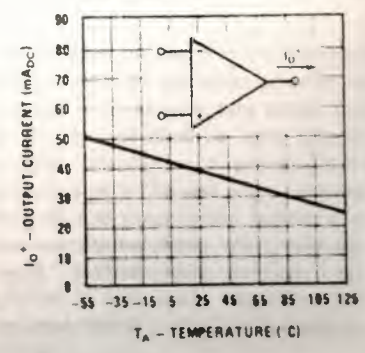
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

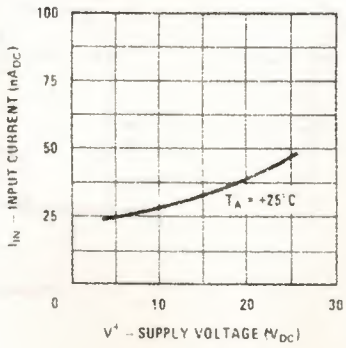


Current Limiting

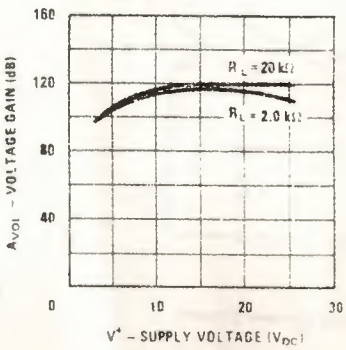


Typical Performance Characteristics (LM2902 only)

Input Current



Voltage Gain



Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

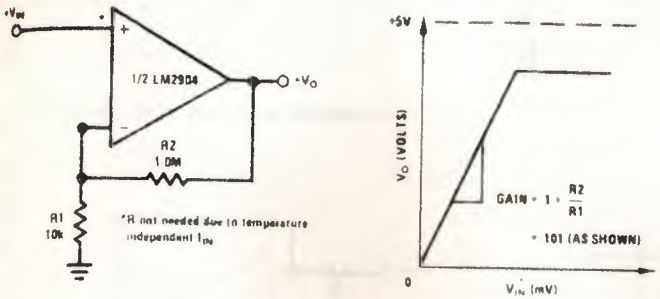
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

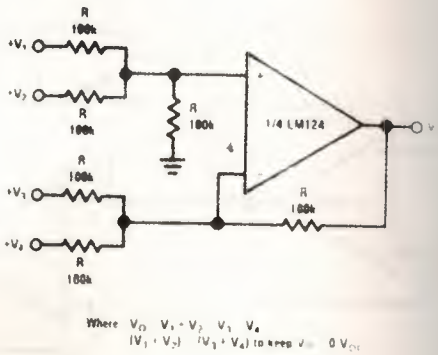
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

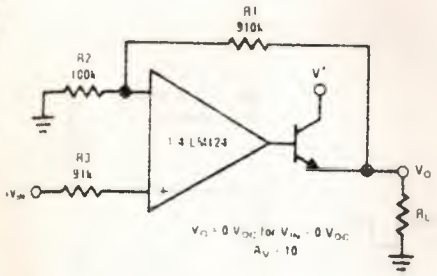
Non-Inverting DC Gain (0V Input = 0V Output)



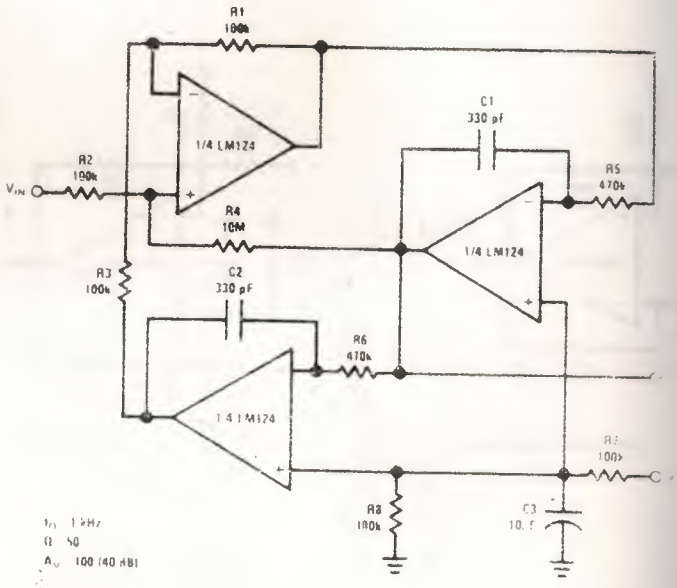
DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} AND V_O ≥ 0 V_{DC})



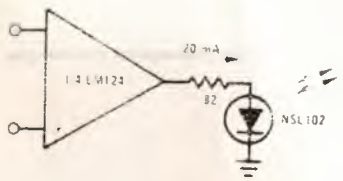
Power Amplifier



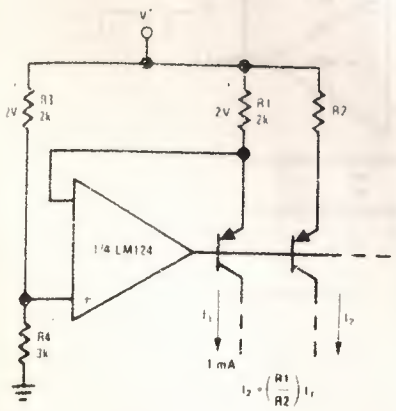
"BI-QUAD" RC Active Bandpass Filter



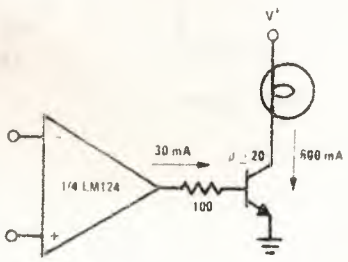
LED Driver



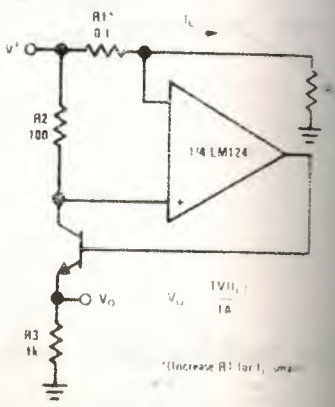
Fixed Current Sources



Lamp Driver

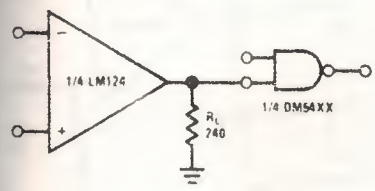


Current Monitor

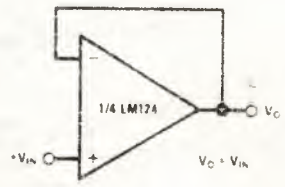


Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

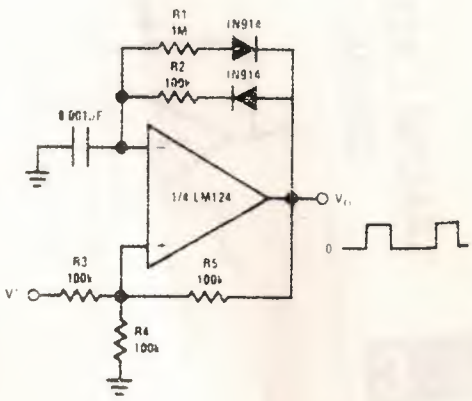
Driving TTL



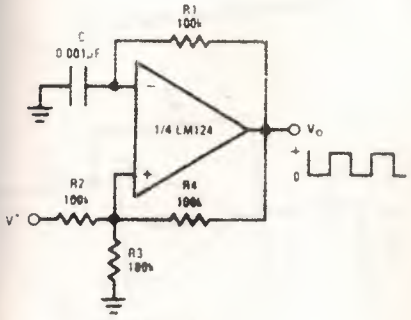
Voltage Follower



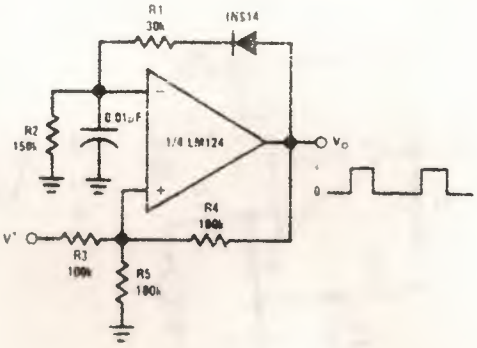
Pulse Generator



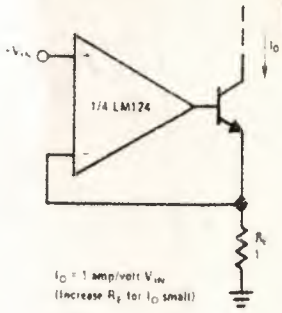
Squarewave Oscillator



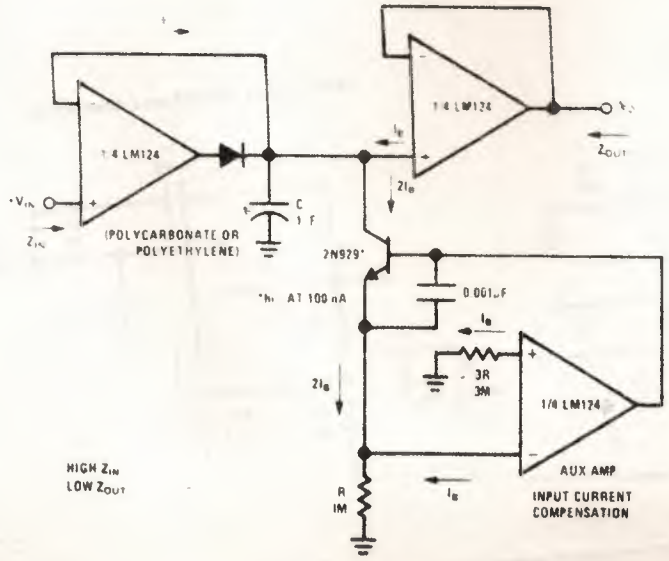
Pulse Generator



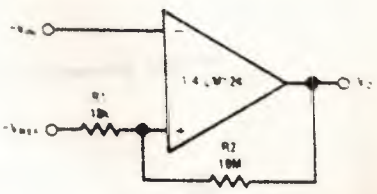
High Compliance Current Sink



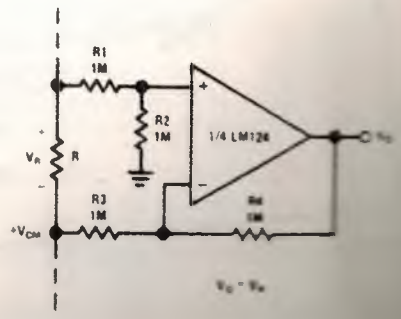
Low Drift Peak Detector



Comparator with Hysteresis



Ground Referencing A Differential Input Signal



Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

Voltage Controlled Oscillator Circuit

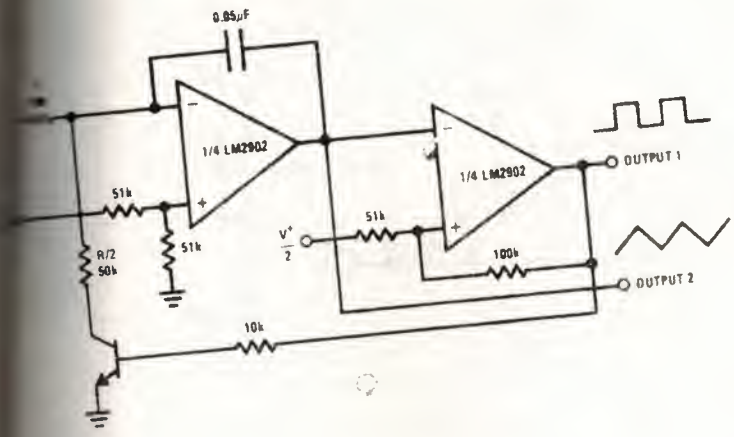
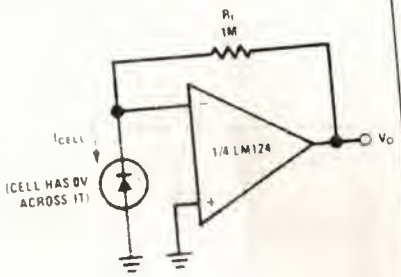
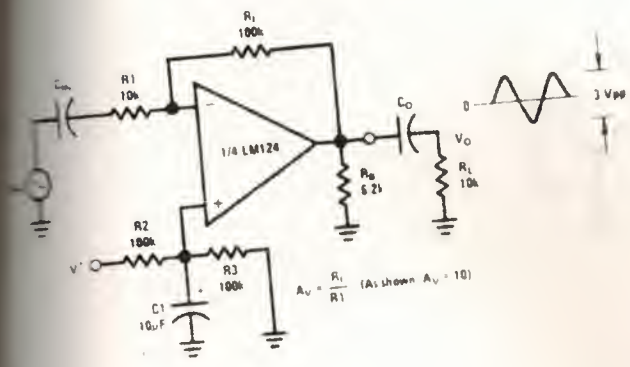


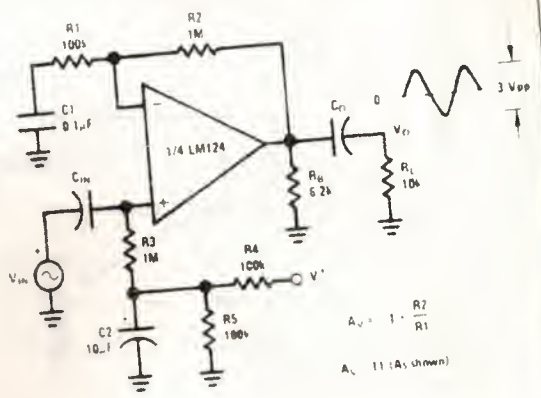
Photo Voltaic-Cell Amplifier



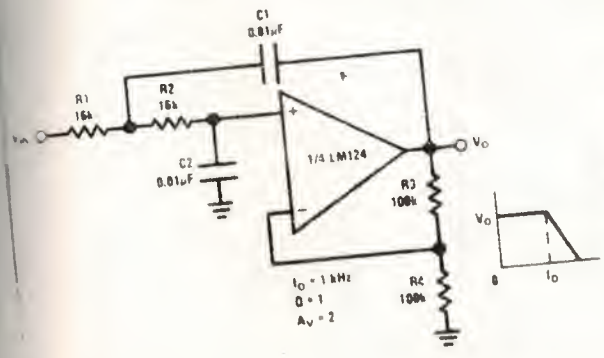
AC Coupled Inverting Amplifier



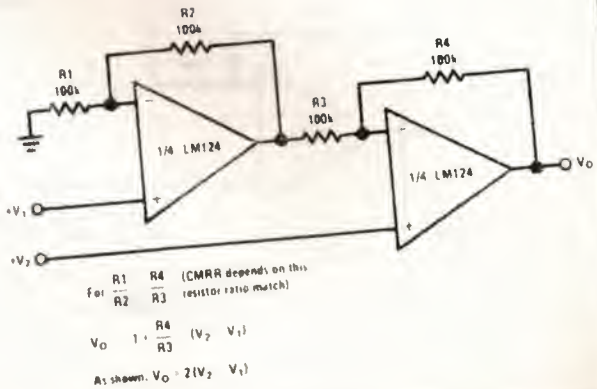
AC Coupled Non-Inverting Amplifier



DC Coupled Low-Pass RC Active Filter



High Input Z, DC Differential Amplifier



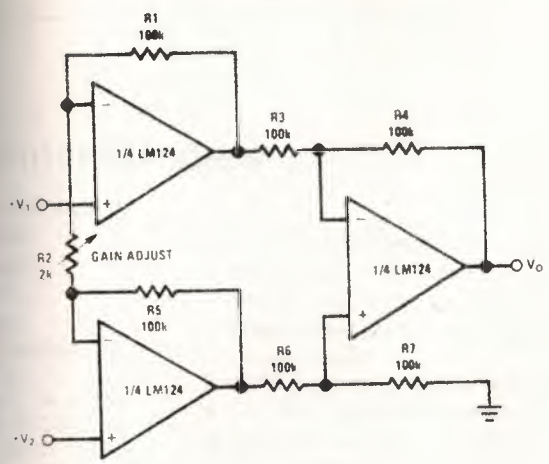
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown, $V_O = 2(V_2 - V_1)$

Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

High Input Z Adjustable-Gain DC Instrumentation Amplifier

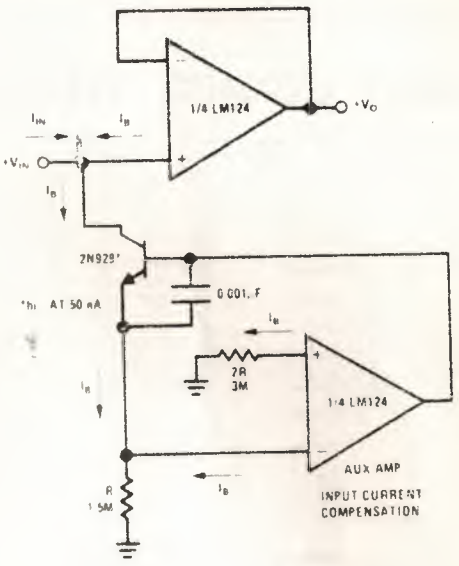


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

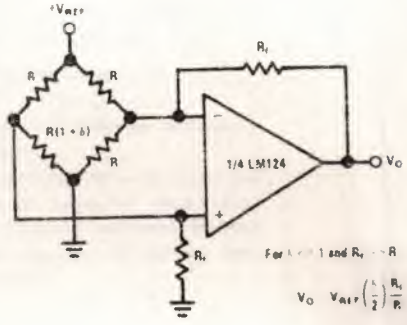
$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



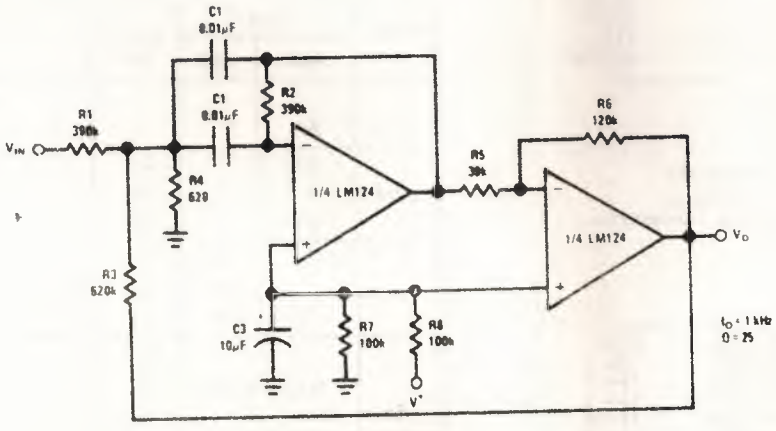
Bridge Current Amplifier



For $\delta \ll 1$ and $R_f = R$

$$V_O = V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Bandpass Active Filter



CS Counter/Dividers

(20-Volt Rating)
Counter with
Outputs
unter with
Outputs

and CD4022B are 5-
Johnson counters having
outputs, respectively.
CLOCK, a RESET, and a
signal. Schmitt trigger
input circuit provides
allows unlimited clock
fall times.

advanced one count at
gative transition of the
signal is low. Counter
the clock line is inhibited
INHIBIT signal is high.
clears the counter to
of the Johnson counter
high-speed operation,
ping and spike-free de-
lock gating is provided,
counting sequence. The
are normally low and go
respective decoded time
output remains high for
cycle. A CARRY-OUT signal
cycle every 10 clock input
CD4017B or every 8 clock
the CD4022B and is used to

Features:

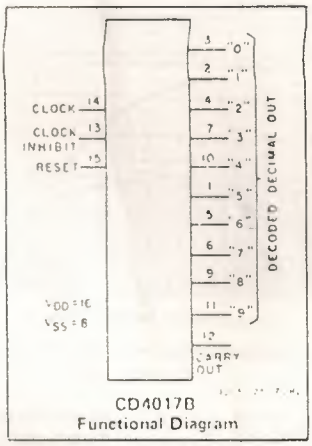
- Fully static operation
- Medium-speed operation . . . 10 MHz (typ.) at V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

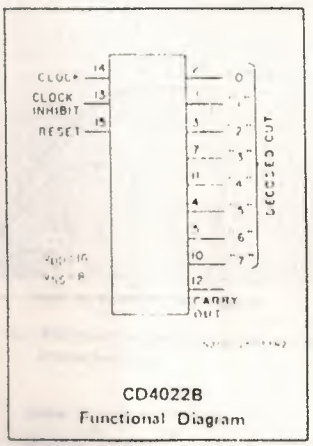
- Decade counter/decimal decode display (CD4017B)
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide-by-N counting
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"

ripple clock the succeeding device in a multi-device counting chain.

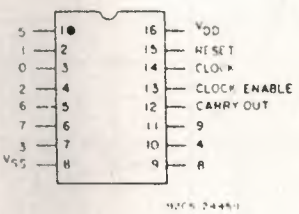
The CD4017B and CD4022B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



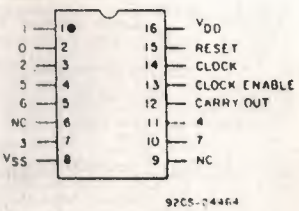
CD4017B
Functional Diagram



CD4022B
Functional Diagram



TOP VIEW
CD4017B
TERMINAL DIAGRAM



TOP VIEW
NC = no connection
CD4022B
TERMINAL DIAGRAM

ENDED OPERATING CONDITIONS

For reliability, nominal operating conditions should be selected so that operation within the following ranges:

CHARACTERISTICS	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Range (For T_A = Full Package-Range)		3	18	V
Frequency, f_{CL}	5		2.5	MHz
	10	–	5	
	15	–	5.5	
Width, t_W	5	200	–	ns
	10	90	–	
	16	60	–	
& Fall Time, t_{rCL}, t_{fCL}	5	UNLIMITED		
	10			
	15			
Setup Time, t_s	5	230	–	ns
	10	100	–	
	15	70	–	
Width, t_{RW}	5	260	–	ns
	10	110	–	
	15	60	–	
Removal Time, t_{rem}	5	400	–	ns
	10	280	–	
	15	150	–	

GS, *Absolute-Maximum Values:*

RANGE, (V_{DD})	
to V_{SS} Terminal)	−0.5 to +20 V
ANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
ANY ONE INPUT	±10 mA
PER PACKAGE (P_D)	
°C (PACKAGE TYPE E)	500 mW
°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
°C (PACKAGE TYPES D, F)	500 mW
°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
PER OUTPUT TRANSISTOR	
PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
ERATURE RANGE (T_A)	
D, F, H	−55 to +125°C
E	−40 to +85°C
ATURE RANGE (T_{stg})	−65 to +150°C
URE (DURING SOLDERING)	
± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

TRICAL CHARACTERISTICS

CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
							+25			
V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
–	0,5	5	5	5	150	150	–	0.04	5	µA
–	0,10	10	10	10	300	300	–	0.04	10	
–	0,15	15	20	20	600	600	–	0.04	20	
–	0,20	20	100	100	3000	3000	–	0.08	100	
0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
9.5	0,10	10	1.6	−1.5	−1.1	0.9	−1.3	−2.6	–	
13.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
	0,5	5	0.05					0	0.05	V
	0,10	10	0.05				–	0	0.05	
	0,15	15	0.05				–	0	0.05	
–	0,5	5	4.95				4.95	5	–	
–	0,10	10	9.95				9.95	10	–	
–	0,15	15	14.95				14.95	15	–	
0.5,4.5	–	5	1.5				–	–	1.5	V
1.9	–	10	3				–	–	3	
1.5,13.5	–	15	4				–	–	4	
0.5,4.5	–	5	3.5				3.5	–	–	
1.9	–	10	7				7	–	–	
1.5,13.5	–	15	11				11	–	–	
	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA

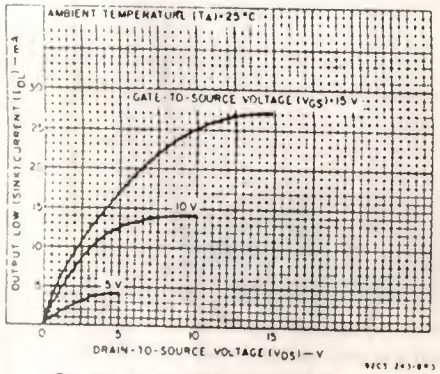


Fig. 5– Typical output low (sink) current characteristics.

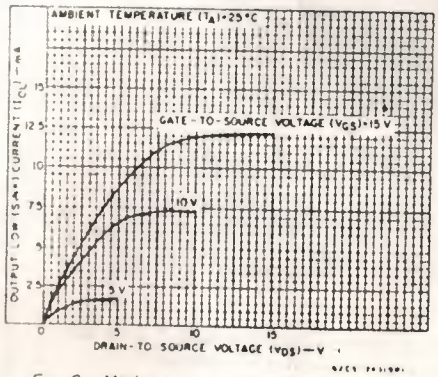


Fig. 6– Minimum output low (sink) current characteristics.

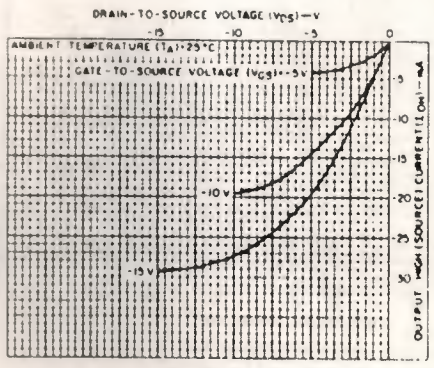


Fig. 7– Typical output high (source) current characteristics.

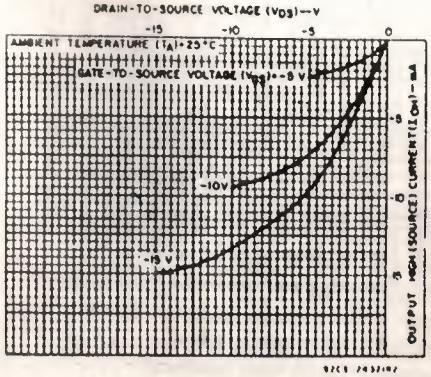


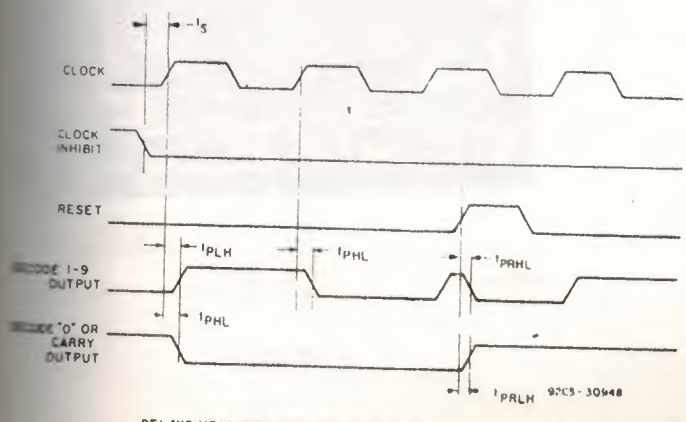
Fig. 8– Minimum output high (source) current characteristics.

C ELECTRICAL CHARACTERISTICS

25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CTERISTIC	CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
OPERATION					
Delay Time, t_{PHL}, t_{PLH} Out	5	–	325	650	ns
	10	–	135	270	
	15	–	85	170	
Out	5	–	300	600	
	10	–	125	250	
	15	–	80	160	
Time, t_{THL}, t_{TLH} or Decode Out Line	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Clock Input Frequency, f_{CL}*	5	2.5	5	–	MHz
	10	5	10	–	
	15	5.5	11	–	
Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	45	90	
	15	–	30	60	
Fall Time, t_rCL, t_fCL	5, 10, 15	UNLIMITED			
Clock Inhibit Setup Time, t_s	5	–	115	230	ns
	10	–	50	100	
	15	–	35	7.5	
tance, C_{IN}	Any Input	–	5	–	pF
PERATION					
Delay Time, t_{PHL}, t_{PLH} or Decode Out Lines	5	–	265	530	ns
	10	–	115	230	
	15	–	85	170	
Reset Pulse Width, t_W	5	–	130	260	ns
	10	–	55	110	
	15	–	30	60	
Reset Removal Time	5	–	200	400	ns
	10	–	140	280	
	15	–	75	150	

respect to carry output line.



DELAYS MEASURED BETWEEN 50 % LEVELS ON ALL WAVEFORMS

Fig. 9— Propagation delay, setup, and hold time waveforms.

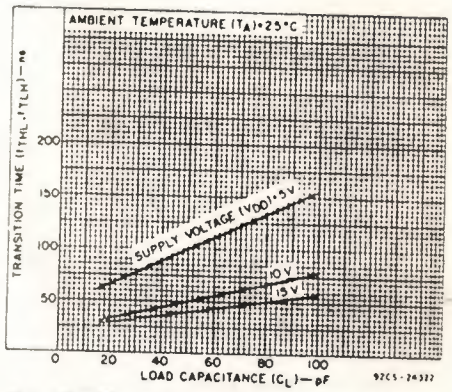


Fig. 10 – Typical transition time as a function of load capacitance.

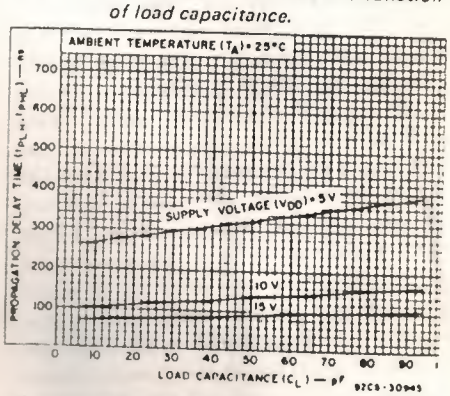


Fig. 11 – Typical propagation delay time as a function of load capacitance (clock to decode output).

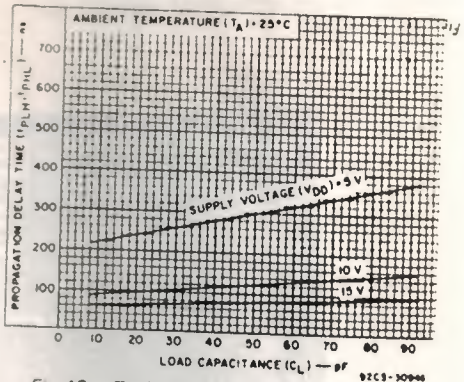


Fig. 12 – Typical propagation delay time as a function of load capacitance (clock to carry-out).

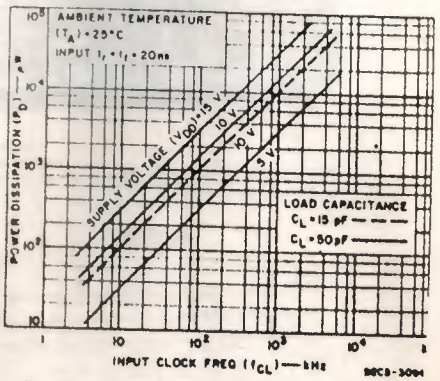
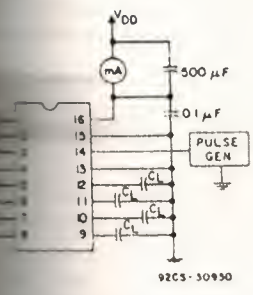


Fig. 13 – Typical dynamic power dissipation as function of clock input frequency.



power dissipation test circuit.

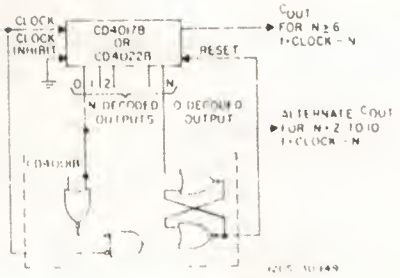
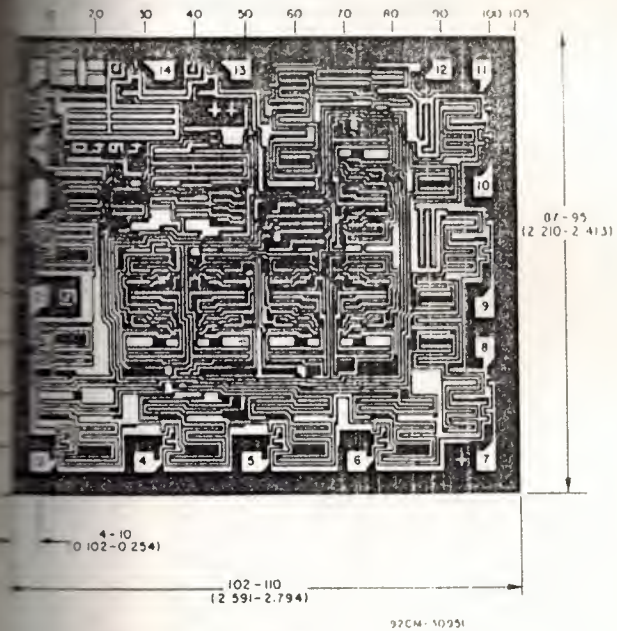
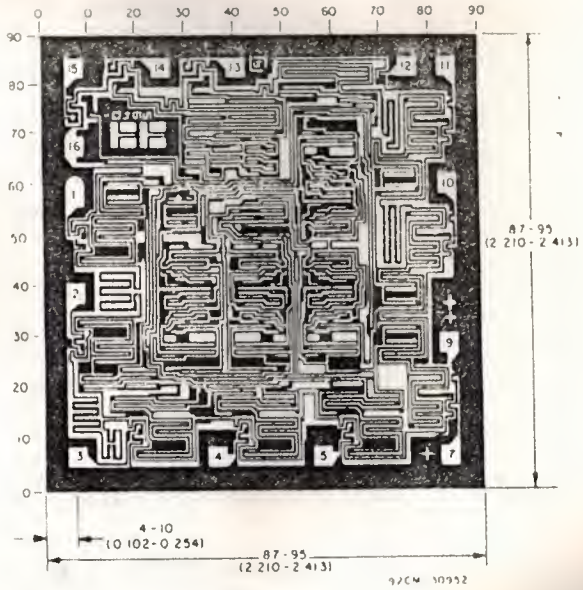


Fig. 18 - Divide by N counter (N = 10) with N decoded outputs.

When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip flop (constructed from two NOR gates of the CD40018) generates a reset pulse which clears the CD4017B or CD4022B to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6 in the CD4017B or 5 in the CD4022B, the C_{OUT} line goes high to clock the next CD4017B or CD4022B counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017B or CD4022B. If the N^{th} decoded output is less than 6 (CD4017B) or 5 (CD4022B), the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.



CD4017BH



CD4022BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

ational Semiconductor

Voltage Regulators

XX Series Voltage Regulators

Description

eries of three terminal regulators is veral fixed output voltages making them range of applications. One of these is egulation, eliminating the distribution ed with single point regulation. The allow these regulators to be used in strumentation, HiFi, and other solid quipment. Although designed primarily egulators these devices can be used mponents to obtain adjustable voltages

is available in an aluminum TO 3 will allow over 1.0A load current if king is provided. Current limiting is the peak output current to a safe value. for the output transistor is provided power dissipation. If internal power too high for the heat sinking hermal shutdown circuit takes over C from overheating.

ort was expended to make the LM78XX rs easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

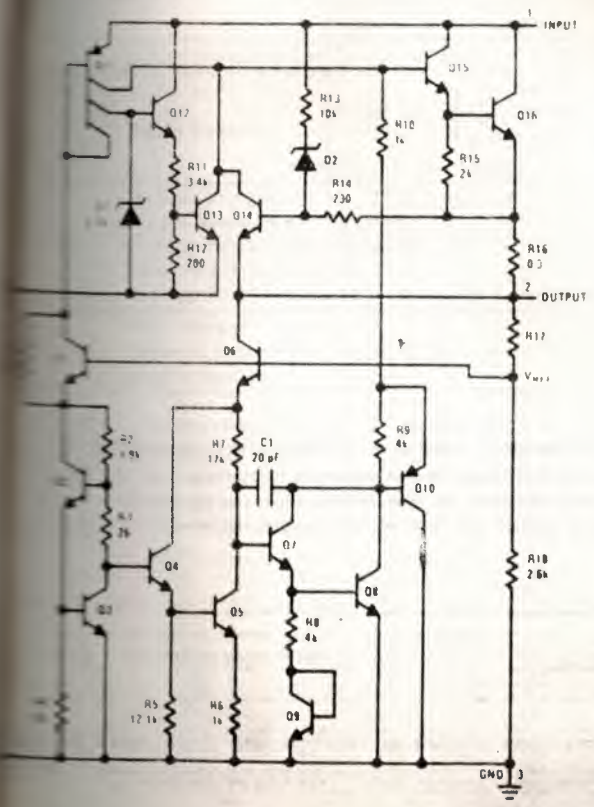
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

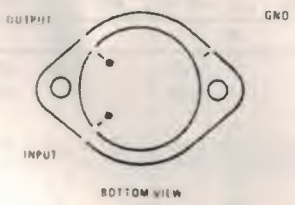
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

atic and Connection Diagrams

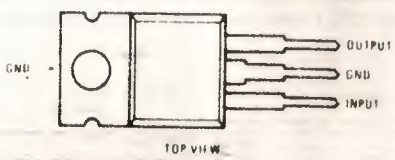


Metal Can Package
TO-3 (K)
Aluminum



Order Numbers
LM7805CK
LM7812CK
LM7815CK
See Package KC02A

Plastic Package
TO-220 (T)



Order Numbers:
LM7805CT
LM7812CT
LM7815CT
See Package T03B

solute Maximum Ratings

Voltage (V_O = 5V, 12V and 15V)	35V
nal Power Dissipation (Note 1)	Internally Limited
rating Temperature Range (T_A)	0°C to +70°C
imum Junction Temperature	
(K Package)	150°C
(T Package)	125°C
rage Temperature Range	−65°C to +150°C
d Temperature (Soldering, 10 seconds)	
TO-3 Package K	300°C
TO-220 Package T	230°C

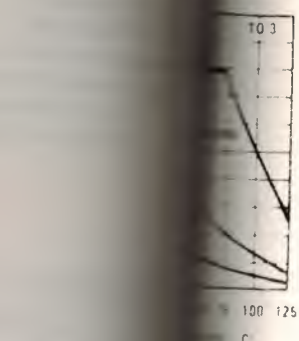
Electrical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

UTPUT VOLTAGE			5V			12V			15V		
PUT VOLTAGE (unless otherwise noted)			10V			19V			23V		
PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
	T_j = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6
Output Voltage	P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}		4.75 (7 ≤ V_{IN} ≤ 20)		5.25	11.4 (14.5 ≤ V_{IN} ≤ 27)		12.6	14.25 (17.5 ≤ V_{IN} ≤ 30)		15.75
Line Regulation	I_O = 500 mA	T_j = 25°C, ΔV_{IN}		3 (7 ≤ V_{IN} ≤ 25)	50		4 (14.5 ≤ V_{IN} ≤ 30)	120		4 (17.5 ≤ V_{IN} ≤ 30)	150
		0°C ≤ T_j ≤ +125°C, ΔV_{IN}		(8 ≤ V_{IN} ≤ 20)	50		(15 ≤ V_{IN} ≤ 27)	120		(18.5 ≤ V_{IN} ≤ 30)	150
	I_O ≤ 1A	T_j = 25°C, ΔV_{IN}		(7.3 ≤ V_{IN} ≤ 20)	50		(14.6 ≤ V_{IN} ≤ 27)	120		(17.7 ≤ V_{IN} ≤ 30)	150
		0°C ≤ T_j ≤ +125°C, ΔV_{IN}		(8 ≤ V_{IN} ≤ 12)	25		(16 ≤ V_{IN} ≤ 22)	60		(20 ≤ V_{IN} ≤ 26)	75
Load Regulation	T_j = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150
		250 mA ≤ I_O ≤ 750 mA			25			60			75
	5 mA ≤ I_O ≤ 1A, 0°C ≤ T_j ≤ +125°C				50			120			150
Quiescent Current	I_O ≤ 1A	T_j = 25°C			8			8			8
		0°C ≤ T_j ≤ +125°C			8.5			8.5			8.5
Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5
	T_j = 25°C, I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(7.5 ≤ V_{IN} ≤ 20)	1.0		(14.8 ≤ V_{IN} ≤ 27)	1.0		(17.9 ≤ V_{IN} ≤ 30)	1.0
	I_O ≤ 500 mA, 0°C ≤ T_j ≤ +125°C, V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(7 ≤ V_{IN} ≤ 25)	1.0		(14.5 ≤ V_{IN} ≤ 30)	1.0		(17.5 ≤ V_{IN} ≤ 30)	1.0
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90	
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ Ripple Rejection	f = 120 Hz, I_O ≤ 1A, T_j = 25°C or I_O ≤ 500 mA, 0°C ≤ T_j ≤ +125°C		62	80		55	72		54	70	
	V_{MIN} ≤ V_{IN} ≤ V_{MAX}		62 (8 ≤ V_{IN} ≤ 18)			55 (15 ≤ V_{IN} ≤ 25)			54 (18.5 ≤ V_{IN} ≤ 28.5)		
Dropout Voltage	T_j = 25°C, I_{OUT} = 1A			2.0			2.0			2.0	
R_O Output Resistance	f = 1 kHz			8			18			19	
Short-Circuit Current	T_j = 25°C			2.1			1.5			1.2	
Peak Output Current	T_j = 25°C			2.4			2.4			2.4	
Average TC of V_{OUT}	0°C ≤ T_j ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8	
Input Voltage Required to Maintain Line Regulation V_{IN}	T_j = 25°C, I_O = 1A		7.3			14.6			17.7		

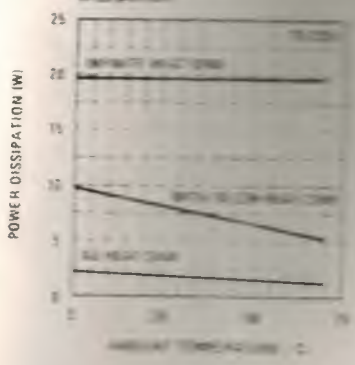
NOTE 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistar TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

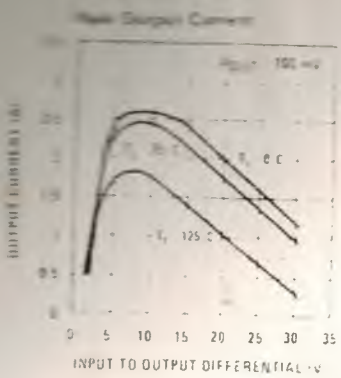
NOTE 2: All characteristics are measured with capacitor across the inut of 0.22 µF, and a capacitor across the output of 0.1 µF. All characte cept noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage chang changes in internal temperature must be taken into account separately.

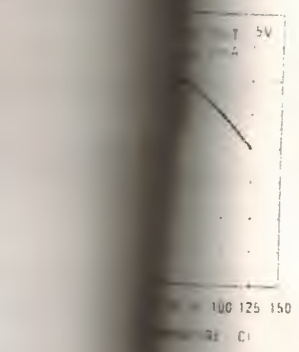
ce Characteristics



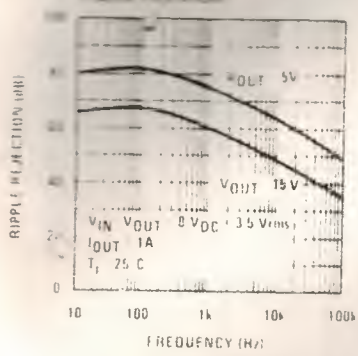
Maximum Average Power Dissipation



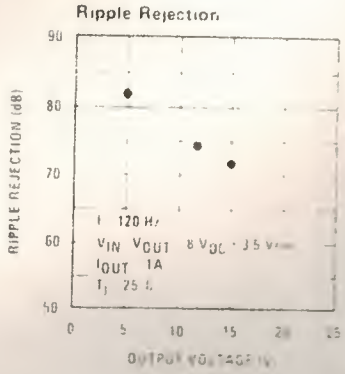


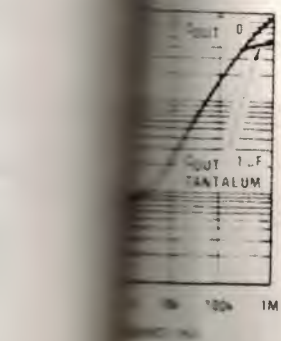


Ripple Rejection

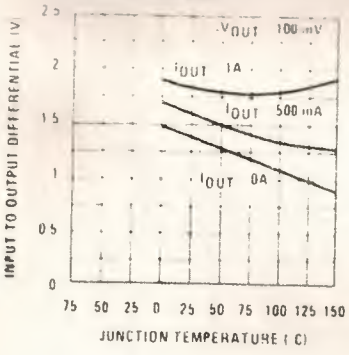


Ripple Rejection

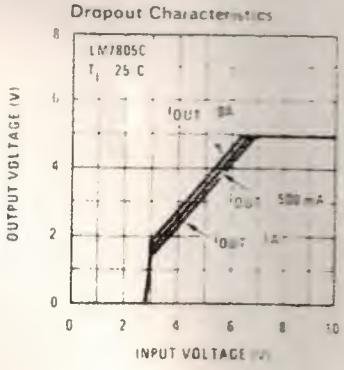




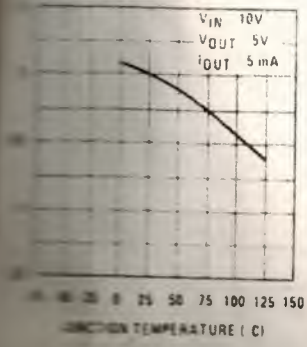
Dropout Voltage



Dropout Characteristics



Quiescent Current



Quiescent Current