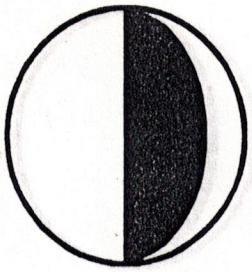


1988

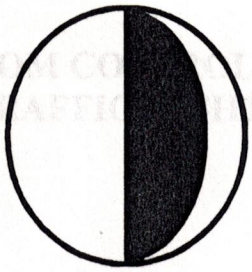
NEAR EAST UNIVERSITY

FACULTY OF ENGINEERING

DEPARTMENT OF
ELECTRICAL. & ELECTRONIC
ENGINEERING

SENIOR SPECIAL PROJECT

INSTRUCTOR : Assoc. Prof. Dr. Şenol Bektaş



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EPROM CONTROLLED

TRAFFIC LIGHTS

EPROM CONTROLLED TRAFFIC LIGHTS

BY

DiCLE ERDEL

A final Project
submitted in partial fulfillment
of the requirements for the degree
Bachelor of Science

NEAR EAST UNIVERSITY
1994

DEDICATIONS

WITH LOTS OF LOVE TO MY PARENTS

BROTHER, SISTER, RELATIVES

TO ALL MY TEACHERS

TO ALL MY FRIENDS.

DEDICATIONS

WITH LOTS OF LOVE TO MY PARENTS

BROTHER, SISTER, RELATIVES

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TO ALL MY FRIENDS.

The Final Project of DiCLE ERDEL
is approved, and is acceptable in quality and form.

Assoc Prof. Dr. Senol Bektas

NEAR EAST UNIVERSITY

1994

EPROM CONTROLLED TRAFFIC LIGHTS

BY
DICLEERDEL

BACHELOR OF SCIENCE DEGREE

NEAR EAST UNIVERSITY
LEFKOSA
TURKISH REPUPLIC OF NORTHERN CYPRUS
1994

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A special appreciations and thanks are extended to Prof. Dr. Haldun Gurmen, the Chairman of the Department of Electrical and Electronic Engineering. A truly gentlemen, he had a distinguished career both as teacher and advisor and as a practicing engineer. The intellect and spirit of my teacher, colleague, and friend appears on every page of this project.

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I extend my deepest thanks to all my friends helped me, directly or indirectly, during my studies.

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Finally, my special thanks to my mother and father and to every person of my family for their everlasting support, because they respect my studying choice, Electrical and Electronic Engineering.

ABSTRACT:

In this project the traffic lighting control system analyzed and constructed electroni,c~IJI,on a four way road.

The priority and durations of lights are obtained from the Traffic Authority of Nicosia. According to the datas the Eprom is programmed in machine language. The counters are used to transfer the contents of the Eprom to the solid-state relays. The relays which are used in this project are optically isolated. All the circuits are installed on a PC board.

TABLE OF CONTENTS

CHAPTER 1. INTRODUCTION

Nowadays, the control of traffic lights is done by modern advanced systems especially where the traffic jam is high. All these techniques are basically microprocessor controlled. In some places the priority and duration of the lights are obtained by using the special lights or weight transducers which are installed on the road. The dates used in this project are get statistically from the Traffic Authority of Famagusta. As an example the on/off pulse duration of the green light in main road is hold longer than the cross road. If in the future, the priority and duration of lights are want to be changed, the Eprom should be reprogrammed. This gives a great advantage to the system.

After the getting,of pulse durations, the Eprom should be programmed in machine language. The 27~16 Eprom is used as a 2K byte ROM in project. But only 256 lines are used. The number of lines of Eprom are controlled by the eight bit counter. The counters are directly connected to the address lines of Eprom. The contents of Eprom are then transferred to the solid state relays. The reason of using th• solid state relay~ are due to the separating high-voltage circuits from the low-voltage circuits.

CHAPTER 2. CIRCUIT DESCRIPTION:

2.1 THE BASIC T74LS90 DECADE COUNTER

The T74LS90 is high speed 4 bit ripple type counter partitioned into two sect ions l, Each counter has a divide by two section and either a divide by five (LS90), divide by six (LS92), or divide by eight (LS93) . section which are triggered by a HIGH TO LOW transition on the clock inputs .Each section can be used separately or tied together (Q to CP) to form BCD. bi-quinary, modulo-12,or modulo-16 counters . All of the counters have a 2 input gated Master Reset (Clear), and the LS90 also has a 2' input gated Master Set (Preset 9) .

. **LOW POWER CONSUMTION ...** TYPICALLY 45 mW

. **HIGH OUTPUT RATES ....** TYPICALLY 50 MHz

. **CHOICE OF~OUNTING MODES . . .** BCD. BI QUIN ARY,

• DIVIDE BY TWELVE ,BINARY .

. **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

. **FULLY TTL AND CMOS COMPATIBLE .**

2.2 T74LS193 PRESETIABLE 4-BIT BINARY UP/DOWN COUNTER

The T74LS193 is an UP/DOWN MODUL0-16 Binary Counter .

Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages "without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously oyerride the clocks.

. **LOW POWER•••....• 95mW** TYPICAL DISSIPATION

. **HIGH SPEED.~~... .40MHz.** TYPİCAL COUNT FREQUENCY

• SYNCHRONOUS COUNTil\rG

• ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD

pto

- INDIVIDUAL PRESET INPUTS
- CASCADING CIRCUITRY INTERNALLY PROVIDED
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

FUNCTIONAL DESCRIPTION OF T74LS193

The LS193 is .Asynchronously Presettable Decade and 4-bit Binary Synchronous UP/DOWN (Reversible) Counters.The operating modes of the LS193 binary counter and LS192 are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops,with internal gating and steering logic to provide master reset,individual preset, count up and count down operations.

Each flip-flop contain JK feedback from slave to master such that a LOW toHIGH transition on its T input causes the slave, and thus the Q output to change state.Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line,thereby causing all state charges to be initiated simultaneously. A LOW to HIGH transition on the Count Up input will advance the count by one, a similar transition on the Count Down input will decrease the count by one. While counting with one clock input,the other should be held HIGH.Otherwise, the circuit will either count by twos or not at all, depending on the state of the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up (TCu) andTerminal Count Down(TCD) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192 ,5 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause TCu to go LOW. TCU will stay LOW until CPU goes HİGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly,the TCD output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel Load(PL) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (PO ,P3) is loaded into the counter and appears on the ,outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q outputirı the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate

signal and will be counted.

2.3 THE 2716 EPROM

16K (2Kx8) UV ERASABLE PROGRAMMABLE ROM

The: Intel 2716 is a 16,384 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5 volt power supply, has a static standby mode, and features fast single addres location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an acces time up to 350ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available. for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing acces time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs - single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time - either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

ERASURE CHARACTERISfICS OF EPROM 2716

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (A) . It should be noted that sunlight and. certain types of fluorescent lamps have wavelengths in the 3000-4000 A range . Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years , while it wouTd take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prewent unintentional erasure.

The recommended erasure procedure for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose(i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2 .. The erasure time with this dosage

is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 W/cm² power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

THE OPERATION OF 271(> EPROM

The five modes of operation of the 2716 are listed in Table 1. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +SV Vee and a Vpp. The Vpp power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

READ MODE OF 2716 EPROM

The 2716 has t\VO control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output cont rol and should be used to gate data. to the. output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least t_{ACC} - t_{OE}.

/

STANDBY MODE OF 2716 EPROM

The 2716 has a standby mode which reduces the active power dissipation by 75% , from 525mW to 132mW. The 2716 is placed in the standby mode by applying a TTL high signal to the CE input. When in standby mode, the outputs are in a high impedance state, independent of the OE inputs.

OUTPUT OR TIEING FOR 2716 EPROM

Because 2716's are usually used in larger memory arrays Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus connection will not occur.

To most efficiently use these two control lines, it is recommended that CE (pin 18) be decoded and used as the primary device selecting function, while OE (pin 20) be made a common connection to all

devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING OF THE EPROM 2716

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "O's" into the desired bit locations. Although only "O's" will be programmed, both "1's" and "O's" can be presented in the data word. The only way to change a "O" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the Vpp power supply is at 25V and OE is at VIH. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the CE/PGM input.

Programming of multiple 2'916s in parallel with the same data can be easily accomplished due to the simplicity of the programming requireıpents. Lik~-inputs of the paralleled 2716s may be connected together' when they are -programmed **with** the •same data. A high level TTL pulse applied to the CE/PGM **input** programs the paralleled 2716s.

PROGRAM INHIBIT OF EPROM 2716

Prograrpming of multiple 2716s in parallel with different data is also easily accomplished. Except for CE/PGM, all like inputs (includingOE) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's CE/PGM input with Vpp at 25V will program that 2716. A low level CE/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY OF THE EPROM 2716

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with Vpp at 25V. Except during programming and program verify, Vpp must be at 5V.

2.4 SOLID Sf ATE RELAYS

-Having ,1 =ea.1ed coria t r=uct i.o n wi +h no -nowi rig parts, t_hese solid s t a t e r-e Lay a a.r= particuJ.arly suited to ~oc. switching applications requiring long life arid high reliability c 'fhe switching is silent, cau~2s no arcing and is unaffected by vibration ~nd corrosive ·ıtmos-pc.eres o ·rhe control input is o:ptica:llY isolated: fro111 the zez-o vol ta.ge 9wi -tchin circuit which produces ·ıfirtually no H.F interference o I.'llay b,., operateü oy 'fTL O!)en collectoı::.· „ üutnut circuit is ' nominall.y open' o When an inducti Ye load is to be switched an additional snubber networks (ego 238-463 for 24Q V ~nd 623-~~R for J15 V 3Uupli~s) may be beneficial *but the* nFtworJc is munda*tory* for *the* dual-in-line arıd 7)lug-i~pin .styi es which do not have integral snubber networks o ror- prot0ction against the effects of tna.nsients. r.ne eo r.nec t i.on of a ·ne tal oxide varistor a.cross a n inducti YA Load can help to minimise the t.r-anemt s s i.o n)f transients o lie ne rally no dera ting is required for lamn loads due to the excellent surge cap ab i.L i ty o.

CHAPTER 3. CIRCUIT OPERATIONS

3.1 EPROM CONTROLLED TRAFFIC LIGHTS OPERATION

The basic circuit diagram and the timing diagram are shown in appendix. As it is seen on the timing diagram, the all required signal and time duration are encoded in machine language. This program is then stored in Eprom. Tha total duration or period of one cycle is 129 seconds. The number of address lines are 8. Therefore, the number of address location will be 256. Each address location of the Eprom should be enable at 129/256 sec or 0.5 sec. The required clock frequency is 2 Hz. The main idea behind of the machine language is that at each 0.5 second intervals the one period of cycle is encoded. Then the binary numbers are converted to Raxadecimal. The complete Eprom contents are shown below.

Eprom List

Address.	Hex. Code.	YRd. G	C.Rc4. RY G
0000-0034	84	1 0 0	0 0 1
0035-0040	48	1 0 0	0 1 0
0041- 0058	90	1 0 0	1 0 0
0059-0064	00	1 1 0	1 0 0
0065- 006C	30	0 0 1	1 0 0
006D- 00E8	50	0 1 0	1 0 0
00E9-00F4	90	1 0 0	1 0 0
00F5-00FF	98	1 0 0	1 1 0

The main blocks of the system are Divider, Counter, Eprom, Relay drivers and Power Supply.

The main clock frequency which is used in the system is 50 Hz. This f~equency as it is explained before is very high for enabling the contents of Eprom at each 0.5 sec. The required clock frequency is 2 Hz. Therefore the main clock frequency should be divided by 25. It is used two 7490 TTL IC divider. Each divider divides by 5 and they are cascaded to have 25 division. The 2 Hz frequency is then applied to Up/Down Counter (74193). The counter which is used in the system is 4 bit binary counter. The down is hold at 5 volts and clock input is applied to Up pin. Therefore it counts from 0000 to 1111. When it is reached to maximum count 1111 it returns again 0000 state and will cause to change the state of carry, In order to get 8-bit binary cdunter~· the two 74193 TTL IC should be cascaded. The carry output' of the ,first counter is used as an input to the second counter. This'· enable us to have 8-bit binary counter.

At each clock pulse, the output o~ the counter is changing and when it is reached to maximum count, all 8-bit returns to zero state.

The 2716 Eprom which is used in the circuit is 2K byte. Only the 256 lines are used. There~ore the output of 8-bit binary counter is applied to the 8-bit address lines of the Eprom. At each setting of the address lines the corresponding data which is stored in the Eprom is transferred to the output. When the 256 lines are completed, it returns again to first address and one period of cycle (128 sec) is completed. These are continuously repeated until the energy of the system is o~f. The output,of the Eprom are feed the solid state Relayis via open coll·ector inverter <7406). Solid state relay~.isolate control circuits from hazards associated with high-voltage and high-power circuits. The~ ~f~•r.~he advantages of separating high-voltage circuits from low-voltage circuits.

CHAPTER ,4. POWER SUPPLY UNIT

POWER REGULATION

The purpose of the power supply is used to convert ac to de current feed the circuit direct current and constant voltage. This circuit mainly consist of six parts these are step down trans~ormers, bridge by power diodes, capacitors, resistances ~ith 7815, 7805, 7915 and LM 317.

The main application of power diodes is as recti~ying elements to convert *ac* to de. Ac is the ,observation -for alternating and de fot· direct <constant> current ·. Electrical power is distributed in ".,, and.,ac f-orm but many industrial,., proc.esses machines ;,1;;::-;.electric.a.l and .. most. elec.tr.onic\;equ·ipments, . required de. power supply .for their oper.ation.

As rectifying elements power diodes find application in dc power supplies of electronic equipments in de supplies.

A very popular form of full-wave rectifier is the bridge rectifier circuit shown in fig 2.1. This circuit enables the full secondary voltage to be effectively impressed across the load and does away with the necessity of using a center topped secondary winding. The four diodes making up the bridge may be obtained in a unit bloc with two pair connections available for connecting the load and the ac input.

On positive half-cycle ie. when terminal J is positiv.e, diode 01 and 02 are forward biased, current therefore ~low~ to the load along th~ path J,K,L,M,N on nega't,i.ve. ·hal:f-cycle, J goes ııe'gat·i~e''with respect to N (,~ N ·hs in fact normally earthen and therefore at zero volt> which forward bias diode 03 and 04 then flows to

L along the path N,L,M,K,J. The ac input voltage and load current and wave forms are sketched in fig 2.2.

In a power gupply we need the voltage to be constant. Voltage by using the <IC> which names is 78xx, 79xx, and LM 317 used in power supply unit. It has some advantage over the zener diode stabilizing c:irc:uit.

1> They are provide with internal current limiting.

2> They are protect internally against thermal overload.

~exx versions· are fixed positive model. For exa~ple a.7815 is a positive 15 volt- model that can J;~rox.i,qe. at;F le.ast 1 ampere o-f output cur.r errc . But .the .on..ı;yy·when :the regulator drop is low enough to avoid overheating.

79xx versions are fixe~ negative model. The LM 317 models are adjustable positive and 500mA of output.

In many rectifier circuit it is common practical apply the ac input voltage via transformer. We shall therefore starts this subsection with a brief description of the function over transformer. The winding of the input side are known as the primary winding and those on the output as secondary windings. The transformer has the property of stepping up or stepping down the amplitude of an applied ac voltage. If the number of primary turns is N1, the voltage is V1, then the amplitude of the output voltage induced across the terminal of the secondary winding is

$$V2 = N2 / N1 \; i \; V1$$

where N2 is -econdary winding~ When N2 > N1 ie. a step up;.situation When N2 < N1 ie. a step ,:down, situat)on.

Thus by employing trans~ormer with suitable turns ratio< Nl/N2 >. We can select the value of ac voltage amplitude applied to *a* rectifier circuit. ie. If we are operating from the main where the peak amplitude is root 2A1/2*240=339 volt < 240 volt mean square rms value o~ the main supply> and we wish to rectifier to a maximum de voltage of 20 volts which has we will soon show m~ans the~secondary voltage amplitude required is 20 volts we would select

N2 / Nl = V2 / Vl = 20 / 339 = 0.06

that is the secondary winding would need to have six turn for every loop on the primary.

CHAPTER 5. CONCLUSION AND RECOMMENDATION

The circuit which is used in this project is more versatile and accurate. The reason of using this technique is to get a minimum deviation in the pulses. In addition to that the clock pulse of the system is derived from the mains so that it is synchronized. It is avoided to use RC elements in the timing sections.

Another advantage of the system is that it makes the contents of the Eprom renewable in the long run.

To prevent the system from the interference it should be well grounded. Otherwise the states of lights can be changed.

APPENDIXES:

EXAMPLE Pr~or~~Y Xntersect~ons~
Gap and Lag Acceptance

The operation of priority highway intersections and the function of lag and gap acceptance can be described as follows;

The observations given below were obtained at a priority intersection, the unbiased and biased mean gap ~nd lag acceptances together with their standard deviations and the critical lag can be calculated. The relationships between these values, can be illustrated as fol lows;

1	2		3	
	first decisions number		all decisions number	
lag or gap class (S)	accepted	rejected	accepted	rejected

0.5-1.4	0	30	0	181
1.5-2.4	0	33	0	168
[illegible]	(3	41	10	105
3.5-4.4	30	26	40	64
4.5-5.4	38	15	52	31
5.5-6.4	[illegible]	5	[illegible]	[illegible]
6.5-7.4	27	3	45	3
7.5-8.4	18	1	25	1
8.5-9.4	15	0	17	0
9.5-10.4	4	0	0	0

The simplest form of highway intersection is where control over the. con~licting traffic movements is exercised by assigning priority to a major road stream of vehicles so requiring a conflicting stream of minor roa'.d ve:hic le.s to give way.~· This form 0-f control is to be found in a variety of forms ranging from the

simplest Step and Give Way controls to the regulation of the merging action at motorway intersections.

Priority intersections function because minor road vehicles are able to enter or cross the major road traffic stream using the larger headways or gaps in the major road flow. It is generally assumed that minor road drivers waiting to enter the major road make a decision whether to enter a gap in the major road on the basis of the size of the gap. If a driver arrives at a Give Way line and immediately enters the major road then the vehicle would not normally enter a complete gap between two vehicles but only a portion of a gap, usually referred to as a lag. Frequently gaps and lags are not differentiated in traffic engineering practice.

When a minor road driver waits at a stop or give way line then the driver may or may not enter a given gap or lag. If the driver enters, then the driver is said to accept the gap or lag, conversely the driver is said to reject the gap or lag if he does not enter the major road.

Driver reactions vary, some are more cautious than others and the acceleration performance of Vehicles also varies; this means that there is a wide range of minimum gaps or lags which drivers will accept. Frequently it is necessary to find the mean value of the accepted gap or lag for all drivers passing through and intersection. As well as determining the mean value, observations can also be used to find the form of the distribution of gap or lag acceptance.

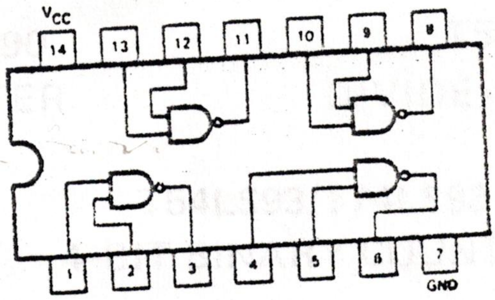
When making observations to determine the mean lag or gap accepted by drivers particular care has to be taken to ensure that the results are not biased by the slower drivers, who will reject many gaps before accepting one gap, in comparison with faster drivers who will reject few gaps before accepting a gap.

Frequently to prevent this bias occurring only the decision of a minor road driver when he first arrives at the junction is recorded. A note is taken of the size of the gap in the major road traffic and whether the driver accepts or rejects this gap. As an alternative all the rejections or drivers are recorded and a mathematical relationship used to determine the unbiased value of the average gap which is accepted.

In early traffic studies of gap acceptance the critical lag was frequently used. This was defined as that lag which had a value such that the number of

rejected lags greater than the critical lag is equal to the number of accepted lags less than the critical lag. The critical lag is by definition a measure of first or unbiased driver decisions and there is a mathematical connection between the critical lag and the unbiased mean value.

QUAD 2-INPUT NANO GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	TYP	MAX	l'EMPEAATUAE
T54LS00X	Hı V	5.0V	6.5 V	- 5s~c ıo 12SₒC
T74LS00X	4.75 V	5.0V	5.25 V	0-C ıo -,.1o•c

X = package ıy!M; D for C ,emic Olp; S' tor Plaıııç. Oip,.SM PKU9ill9 lolormııion Sec;tiorı for pac:1<.aoe• aveiıub.te an. ınıı prod..ıct.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
VıH	lnpul HIGH voııaıı•		2.0			V	Guaranı~<l ınrul HIGH '/ol:iı<,~
lıl,_	ı"put LOW voltaııe	54'			0.7	V	Guarıntf"'.d Input LOW Yol'.d9"
		1.-			08		
VCO	Input Cl.amp Dı<XUl Yoliaıı•			-065	-1.5	V	Vee" MIN. lı!II * -19 mA
\' OH	Qu•pul HIGH Voliaoe	5.ıl	2.5	3.4		V	Vee"' M:N. ıo:, ~ -,\00 μA '/'..'I~ ılıL
		7'	2.7	34			
Vot.	Output LOW voiıııııe	64,74		0.25	0.4	V	Yee"' MIN. lr)L • 4 c) mA. Vı.'l ~ 2.0 V
		74		0.35	0.5	ı/	Vee ~ MIN, '0,. a.0 rnA.Vı~ı ~ 'L.0 V
lIH	ınııuı HIGH Current			1.0	20	μA	Yrr ~ MAX. VıN ~ 2 7 V
					0.1	-mA	Vee"' MA)ıVıN, 10~-:--~
\r'...	lnouı LOW Cuırı,nt				-036	mA	Vee"' MAX, VıN ~ 0.4 V
0s	Ouıpuı Short Cırcuıı Çurreoı '(Note 3)		-20		-100	mA	"cc • MAX."our:" ov
IççH	supply curreot HIGH			0.a	1.6	mA	Vee"' MAX. VıN ~ 0 V
'CCı,	Sııwlv Current LOW			2.4	4.4	mA	Vçc ~ MAX, Jııpuıı: Open

(See Page 273 for Waveforms)

AC CHARACTERISTICS: TA = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
tpLH	Turn Oft Oelıy. lnpul ıo Ouınıuı	3.0	50	10	nı	Vçç"50V
'PHİ	ıurııv ~ ... inqut to Output	3.0	5.0	10	ns	Cı_,• 15 pF

NOTES

2. ~~~;a:~:lll ,,.., VCC • S.0 V, TA • 25° C.

J. Noı n,or• ıh~n one ouıouı ıhould be lhO<Hdatı time.

T54LS90!T74LS90

DECADE COUNTER

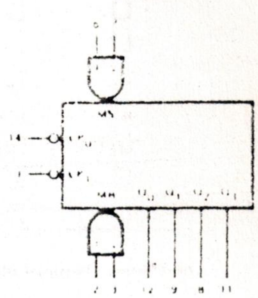
T54LS92/T74LS92

DIVIDE-BY-TWELVE COUNTER

T54LS93/T7 4LS93

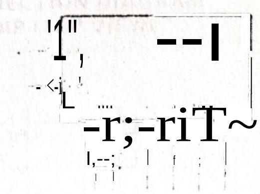
4-BIT BINARY COUNlER

ut:. SC.: I, 11' TIU N !hu f54LS0U/ I/4L.S~U. I ~ 4 I. :,'.L! / I / 41. :,;J / uııd I ',,;I :.i:JJi I /41. S'.JJ """ lııı,lı ,pu,:ı.I 4 lııt ıııplt: lypı: cuııııtt:ıs µ,,ı ıııuııcd ıfı ı o ıı.:,,ı :.,t..:LlI<Jıı) (ıH.:lı cuuıııtt:ı ıııus J dıvu iet ıy twu sec t ıoı ııld t:ııtıer ıJ divıdc lıy trv e H :::.J,Jl. ,Jıvı,.Jc l,ı,, '' IL.'.::/):!) ur <Jııı<Jıı lıy .;,utıı ll.S93) sec l to o wtııclı "" ı, ".J(JUlc(I lıv ,,)IICH tu L.UW t(ıJrı::ıııtıL)II un thtt cluL~ ıııputS>. Ei.H.:h)t::t.ıLHI ı:Jri h~ uSA:ıU ,cııc11.,ıcly l,ıı ııcıJ lu<Jellıı,ı I() lu C̄P) to lurıı BCD, L,ı-qıııııııy, rnuıJıılu 12, ur """Jıılu I b cuııııı:ı s. All *ut* lltı cuuru eı s lıuııc d '/ ıııırnt yJh,d MJ>lcr I {esuı (Clı:..ıı I. ,ııJ ı tı e I ',;'JO <>i>U iıJS d 2 ııpul '.).ılCJ M.ıstcı Se I (Pr cse I 9).



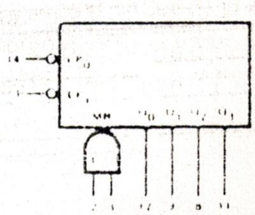
- LOW POWER CONSUMPTION ... TYPICALLY 45 mW
- IIIGH COUNT RATES. . . . TYPICALLY 50 Mlü
- CHOICE OF COUNTING MODES . . . BCD. BI QUINARY, DIVIDE BY TWELVE. BINARY
- !1JPUT CLAMP DIODES LIMIT HIGH ~PEED TtHMINAIlON EFFECTS
- 1--IJl.LY TTL ,'\ND CMOS COMPATIULE

LSc!2



f'lrJ NM,1tS		LOADINC; INuıe ul	
		i 1l (j j l	(0W
i',:	Clock (Active LOW going edge) Input to 2 Section	1 () I) L	I 5 1! L
\,/" !	l;lııJ.. [Ar.tı vu I U\'V ijuıııy t:.:dıjc) lıq.HJI to ~ St.:ı:tıuıı (l ~.;~U). ti ~t:Ltıııı IL~~2)	/ U \J L	.' (J \) I.
C['	Cluı.~ {Acli'I'ı: I U\/J IjUl.llIj cl.lUC) lııJHd tu lj ~cLlIlJıı {I.~/jJ)	I (J. IJ I.	I U u.I
f-.\lı I J.111,	/.ıl,ııl:ı t-c ı c l (I:.! cJı) 111~Jıı l)	il 5 il l	Ü 25 11 I.
MS1, MS2	M.ı'>lı:, ~)ı.:t.(Pıc~c.I IJ. LSUUJ Jıq:~ıt)	U 5 U.L	U 2-5 I) I.:
\l	Uııq,uı lıı,ııı L Scctıuıı ın,.!c, IJ & C/	I Ü 'lJ, L.	5(251UL
\'}I (jJ.. UJ	IJutpııt, lı.ııı 5 lI.S!.ltll. ti il Si.1.11. :l:l I l S:nı !::ic,.tuııı\ (Note tıl	I Ot; L	5(i 51 U L

LS93



NOTES

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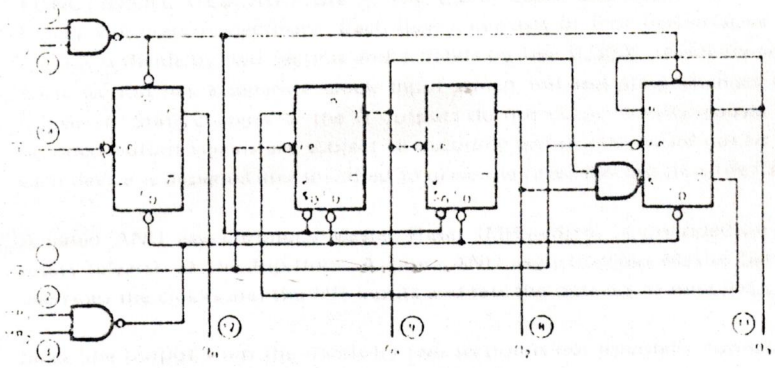
b II,,: (ı,ıqıut II)ı/J ,lı, t.,ıtı,• •\ :I'~ IJL lııı Md•t••v (!..)4) ,..,,d lı ıı,, Lı,ıııııı.:ıt.•.ıl I/4) Jt•ıı

c ltı.: llu th,t•"ıl' Jr..:'.J"•u.ıı,ıı:~.ı ı• dıı.-.ı ıııu I~.ıı I •,. l.,ur 1ı1ta ılıu t.P ,ı,p,ıı ı,l ttıu lh•")~c

LOGIC DIAGfl/\M

LS90



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Vc;c•r,n5
Ç;r'·;ıü • Pın 10

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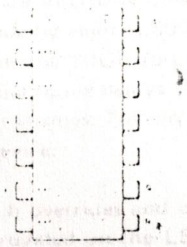
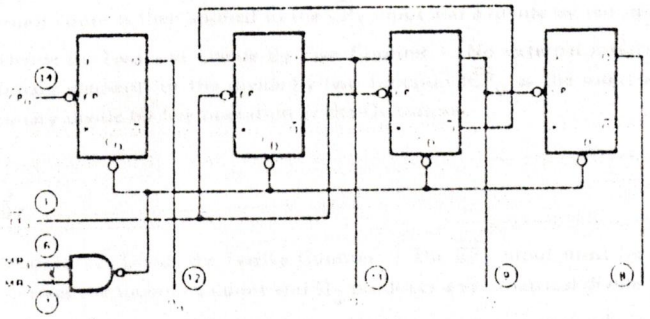


NC - No Internal Connection

LOGIC Dlı\GfIAM

LS92



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V CC • p,,, 5
(;NO •. P,n 10

CCINNt:CTION DIAGnAM
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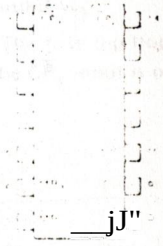
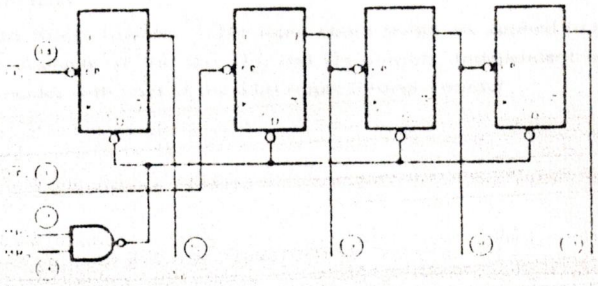


fJC - Nn

LOGIC DIAGRAM

LS93



/'·I - rm fJuınhrı\
VCC P,n S
<;NI) rı,·

CONNECTION DI/\(~n/\M
DIP i

f ur•JCTIONAL DESCHIPTION - The LSUO, L~2 .ııJ L.S93 ur e tl t,it r uıp!e l vp e L)ec;~.ıe, Cfr,ı(!ı, t.lv-Tw+:!v". unJ !,ıı;.ııy Cuu nt er s ı e suect ivetv. Eacn device cuns ıst s ot four r1lctS1er/)lıJve tlıp-tlı)pS ı:..ıtuı:hue ıııı.:rıı·dly ı_;_,rırı~c!~do .. vı,lc J ı|ıvu le lJ'; ıvvu sect ion .ın<.J a urviueuvtive (LS901. Jividı.:-lJy-sıx (L.S921, uı dl\·ıJe·lıv ""Jılt l_~SJ) >eı.,tıun. t .••.l, ,ccıiun lıcı; a sı::p.,rate clock ını.ıuı wlıdı ıni ıiaı es sıat e clı.anycs ut l he cuunt,:ı un t:ıe !i1Ci1-tu-Ll)W clock t,Jıı)ıtıun. Stdlt.:. ı.;hüıiycs of ıht: O ouı put s du nut occur sjrnu l l aneou slv 1JCC<Hışc: ot ıı ıte ı ıcıl ıı;Jı,le ılöL..1ys. Tb ere t or e, ıtL., u\lt:d ou ı nu t ')l<jlldls ar e subject to L1t.:codınu sp ik e s and slıuuld ııoı l:ıc used fur cloc+s ..ıı \lriHıcs. Tl,,_-. (:Jo uııput üf c,ıc.lı ı.Iev u.e ıs Jusıyıı"J ,ııJ Spt!citıed tu drive ı he ıölt:d t.ııı out plus ı ne CPı uu ı u t ut l l ıe ı ı ev u e.

,\ JcıiL'd A~-JU c1syndıruıuu, M..ıslcı Restl l!\ı1HıMH2l ıs ıprovıJeı.J uıı ıll cuuıııı:ıs ı-vlıın:lı ..ıveııJes Jnı.J clo ck s aııc.J ,,,,eıı kie.ıı>) ull ıı,c_ tııp-~lopıs. A .ua·1.tec.J ,ANO dsyndıunous Milster Sei lMS1•MS2) ıs pıuvıdı.:.J uıı t h e LS90 wh ict: "vı.:ııı,lcs ıhe cluck, uııd l tıe MR inputs aıic.J se l s l ne ouıput s tu nine OIL.l.HI.

:.;ıııu: ıtıı: uııtput fruın,.th~ dıv ıde-bv-two sec uon ıs nut ıııtı:ındlly cuııiec:ıcd ~u tlıı: succeeuıın<J sı.,,ıes. tlie devıces may l ıt· ı;pcr .ı ft!d ııı vur ıous count HHJ rnocies ..

L S90

A llCU Decode (cl-17 l l ı:u,ıııtcı rıııı CP l ıııpuı ıı\Jı!: tıe t',tt:rııdily cur ın ect ed tu the Cla uııpııı l'he CPo 111µ:l[ıı,ceıveS tlıe ıııcuııµıı~ cuuııt d/10 d BCD count sequence ı; pr ouuceu.

lJ,::ı.,,ıııet,ıı.:...I !Jı quın.ııv Dıvıde l:h:!erı Counter - I'he O3 output rnu~ı be externally cuıınccıau tu t lıe 60 ırıpul. The ı,,pu(ı:,Jltfll ı, ttıcıı dpplıed tu ıne CPı ıııµut dllJ ıl divıık·lıv te n 141Jdftl WdVe ıı OIlldlIltd ıl o u tput cıu.

l., l)ıvıu~ !Jy l wu o•uJ Uıvıdıı Uy Fı•e Cou,uer - No e x rernat ıntercuıııeı.;ıiuııı dit ıcquıieıJ Tıı- tıı·,ı t:,v ne!o ıc u~ed as d l,ıııoıy cleııicıı tor t he Jıvıı.Jcı bvtwo tuııcıicııı (CPO dı th<ı ıııput aııJ OO d~ the ouruut l lhe (Pı ıırııı ,, used tu 0btaın l,ı,ı,ıy Jıvı.Je Iıv lıve upt:<olıun dl rne O3 uuıpuı.

L :,'JI

A ı"JuıJ,ılu l J. Dıvıdc.: e,- Lvvelve Counter - The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input ıı;Lı:1Vl!~ lh~ tıll.UIIHlHJ Lüuııt d(H..ı] ()J pıutJucc~ d)y'lfHl\t:lflCal dıvıdt.:·lıy·twı-:lıJt:' squdft: vvevc {J!ılpul

B l;ıvıdt ti)C T wo dHd Ln vnle Hy Sıx Cuuılt!r iJo e x t er nal ırHt!rcuınt<.tıun~ are ı e qu ır e d l~ır: f!fJl ılı~; /!cıµ ı:ı u'.t::U as a lııı.,ı, el;"lt:/1[tor the dıvıde ov t wo tuı,ctıuıı The CPı ınpı,[,, uıeu ıo ülıl,dlll Jıvıuc tıy titret: U(K.ld[IUH ,il ttre O, ;,r,d O2 :ııtıllıl) dlHl dıvıdc l)y ~ıx uµt:rdtıun dl t tıe O3 out put

L S'.JJ

A ~ ~iıl Hı!ıplc Cuı,ıtcı Tlıe outµul (~) ıııııx(tıt: t:ı<lt:rndtly cuı1ııt:ctt..:J to ıııµut $\overline{CP}_1$ Tht: ınpuı uJ\-ı! ınıl:ı,csJtc ~ppiied ıo ııqııl (J'u ~ııııılJIIC(.llÜ dı"j!)ıüll~ ot l., ı ti. anc1 16 dit' pcı toıını-:d dı l ne Oo, U1, n, ..ıııd ()-~ ,,ıııın,!~ ,) ~lıo·.ıvıı ın the \ ı ı{1ı l.~(;lt'.

B 5 Ll,t Hqıplt; (.vıııırt:ı llı e ıııjıul cuuı,ı pııht!) ,,Jlı' Jµplıt:J ld ıııplıt $\overline{CP}_1$ SıııııJlli:Sf\Cı.)il'ı 1l'1HIC ıı'~ı~lıJ/1) uf 2. 4. dfld 8 J•ı: .ı.Jıl"t,lt: c t ıht: Uı ()~>. Jııd Ü] (Hıtpıı!5: 1ıll.h!pcıu .ıt:ııt U)r: uf t t ıe tı~l tlıµ tl0p ı) aveuı u«: ıf l l ı· ıt:'ıt.:l luııı..;tıuıı l ı..ıııudc!. ·vıl l ı ı cs c t ul tlıı.: J l,II, ,pµl•; thrııı,Jlı ı.<HJfl{Cf

LS90 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS92 AND LS93 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS90 BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

LS92 TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q_0 connected to input CP_1.

LS93 TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc) for CP	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (VCC) MIN	TYP	MAX	TEMPERATURE
T!.14LS90X f!j4LSD2X Tt:>'1L.S9JX	4 5 V	50V	5 5 V	55"C lo 125°C
T/4LS90X T /41. SD2X T/4lSD3X	4 75 V	:,O V	5 25 V	0·C to ,10·C

T! p,ockay• tYP•. il tur Ce,arııoc Oıp_ U t,,, Pı,ı,ııc (Jıp ::ee Pa, '''''''\I tııl̃o,011),11ıııı Socı,.,n 1,ı, '''' • ,qe, ,,.,..ı.,ı,1, '''' ,ll,, proıt, ":ı

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		20			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0 7	V	Guaranteed Input LOW Voltage for All Inputs
		74			00		
V_{CD}	Input Clamp Diode Voltage			0 65	1 5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	54	2 5	3 4		V	V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2 7	3 4			
V_{OL}	Output LOW Voltage	64, 74		0 25	0.4	V	I_{OL} = 4.0 mA, V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0 3S	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current MS, MR				20	µA	V_{CC} = MAX, V_{IN} = 2 7 V
	$\overline{CP}_0$				120		
	$\overline{CP}_1$ (LS93)				40		
	$\overline{CP}_1$ (LS90, LS92)				80		
	MS, MR				0 1	mA	V_{CC} = MAX, V_{IN} = 5 5 V
	$\overline{CP}_0$, $\overline{CP}_1$ (LS93)				0 4		
	$\overline{CP}_1$ (LS90, LS92)				08		
I_{IL}	Input LOW Current MS, MR				-0 4	mA	V_{CC} = MAX, V_{IN} = 0 4 V
	$\overline{CP}_0$				-2 4		
	$\overline{CP}_1$ (LS93)				-1 6		
	$\overline{CP}_1$ (LS90, LS92)				-3 2		
I_{OS}	Output Short Circuit Current (Note 4)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES
1 Conditions for testing, not shown in the table, are chosen to guarantee operation under the worst case conditions.
2 The specified LIMITS represent the worst case value for the parameter. Since these worst case values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard bands can be achieved by decreasing the allowable system operating ranges.
3 Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4 Not more than one output should be shorted at a time.

T54LS192/T74LS192
T54LS193/T74LS193

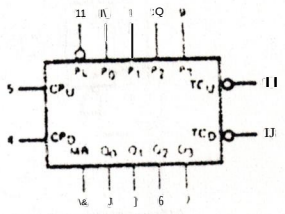
BCD/DECADE UP/DOWN COUNTER
4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION - The T54LS192/T74LS192 is an UP/DOWN BCD Decade [8421] Counter and the T54LS193/T74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Individual Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counters. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs override the clocks.

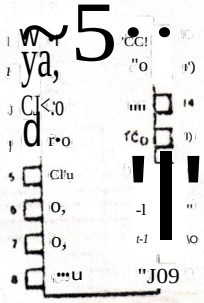
- LOW POWER, 95 mW TYPICAL DISSIPATION
- HIGH SPEED ... 40 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- SYNCHRONOUS MASTER RESET AND PARALLEL LOAD
- INDIVIDUAL PRESET INPUTS
- CASCADING CIRCUITRY INTERNALLY PROVIDED
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



Vcc = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

CP_U	Count Up Clock Pulse Input
CP_D	Count Down Clock Pulse Input
MR	Asynchronous Master Reset (Clear) Input
PL	Asynchronous Parallel Load (Active LOW) Input
P_n	Parallel Data Inputs
Q_n	Flip-flop Outputs (Note b)
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)

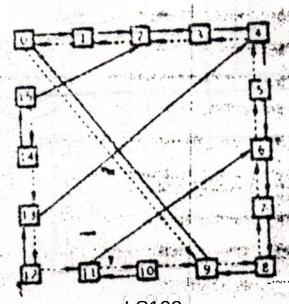
LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.6 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.6 U.L.	0.25 U.L.
10 U.L.	5(2.5) U.L.
10 U.L.	5(2.5) U.L.
10 U.L.	5(2.5) U.L.

NOTES:

a. 1 U.L. = Unit Load (0.1 mA HIGH/1.6 mA LOW).
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

STATE DIAGRAMS



LS192

LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

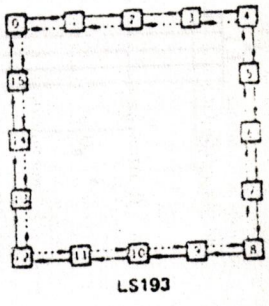
LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

COUNT UP ——

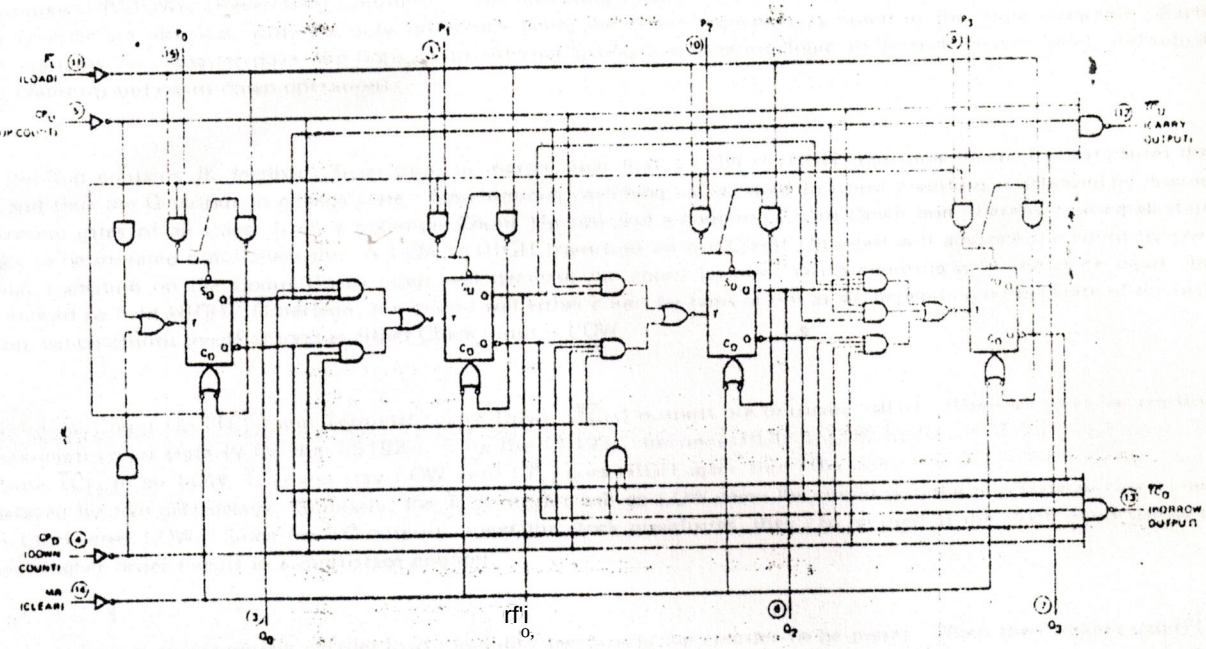
COUNTDOWN ·····



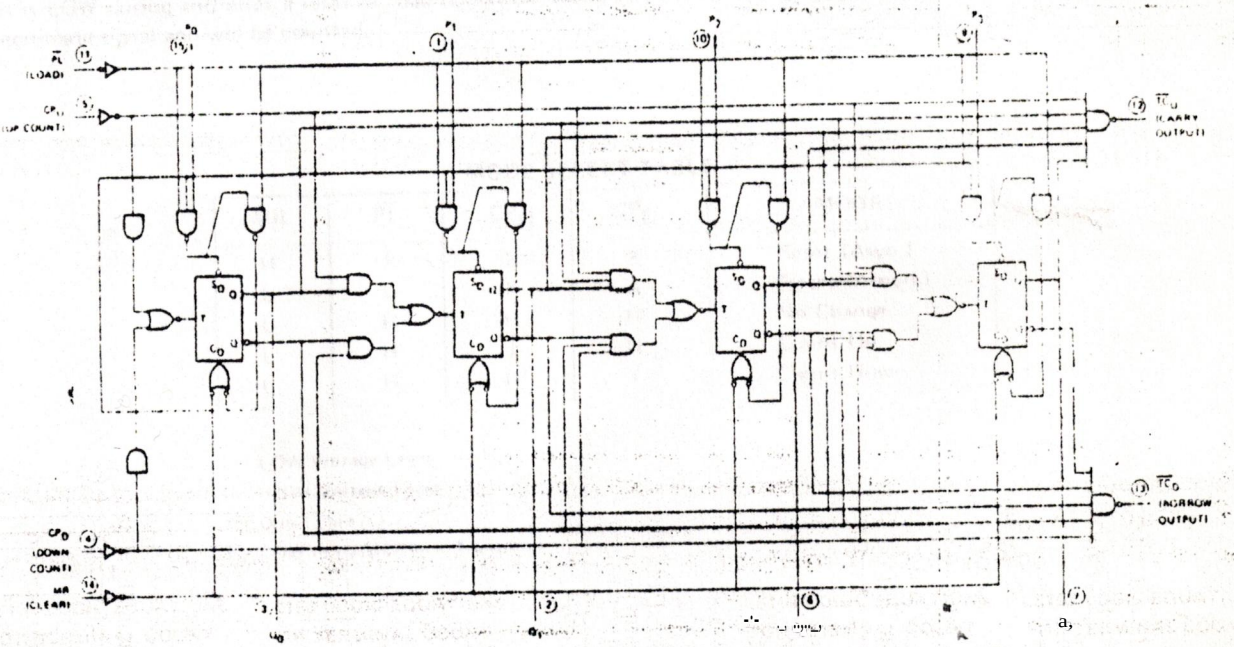
LS193

LOGIC DIAGRAMS

LS192



LS193.



VCC = Pin 16
GND = Pin 8
Ü = Pin Number

FUNCTIONAL DESCRIPTION Tlı" L'.:,l'l') a11rl 1.S 193 aıl' ı\svın lıo11,111~iyıesrtt:ıtıl" llı•ı:a•le ,11d ı\ n,ı Rıııaıv $y11dıınıınııs ur:DOWN (Rı>v,:>ıs;ılıll'}C:nııııtrıs Tlır nppıatııHJ ıııodı><·,f llıP l sıg7 rlf'ı·;ıdf>(1)•1111<•1 :ıııol ılıe i sııı.1 hınaıy çnıını~r ar~ id<'ntiral. with thP. only tiilh~r('rWf' hıııı•111q ıtu~,:nıııı(~~q,wrıcr,c; ,ıs notf'd ııı ttı" ~r;ı!r> [.)ı;ı(Jı;:ırn~ F;\dı ı:ıırııı ronıaın~ [r u ı r nıa~tP.r/sl:ıvr flır,-fl0r,\. wı t h ıntrınal l],ıtinq ,ıı•d q,l~r,nq 1nqıc l,, pıl1v,ı1,, rıı.ı•;rı•r rrı,;rıf. ıııtdıvıdıı.ıl prrsı>t, r:ouııt ııp .11,ıl ı:nur1t down opEJratıon~

Each flııı flnp coıııaıııs JK fl'Pdh;ıck fıom ıı a,r. to ııı~strı suclı ılı;ıı ;ı I.OW ı-ı Hl(iH ııa11sıı,rnı n,ı ı c l ııpııı raıısrs ıtır slavP., and thuı., llf' 0 output to ch anqn state Syrıchronoıııı; t.wıtılınq. npposrd tn ııppl1ı rq,11\tııt). ıı: ;ırlııPvrıd ıv drıvıııq thP sterrııı.ı ,ptrs. n(,ıll sı.ıqf!s froııı,a cor,ıırrwıı Count Uıı lirıı> aıırl ı çnrııııoıı Cıııııt rlnwrı lıııı>. ılırırhy r·~,ısıı•qall q,,ıe chanqcs to be in,ııated ,ımıılt;nwoıısly. A LOW to HIGH ırarısıtıoıı ,,rı ılır Ccnııııt lip ırıpıı will ad.,~ıH'Pılı" rrı,ırıt ı,v nııe. a sıınil;ır u ansıuon (ll) thP Coıınt Down input wıll dP.(f('jl~(' ıtır! r.011111 by nııP VVlllılr roııııırıq \\'ı1tı nıın ı:lrw·k ıııpııf, tlıt' ottrr r ,;hoıılrl he helrl HIGH Othrıwi~P.. lhf' r:lfctııt wıll ~ıthrr r ourrt lıv twn<.nr ınl .ıı alt dııp,nd,,,q ,ır, tlıo f;ı~ıı· r!ıı•fıı~ı lı,n flop, wiııt:lı caıırınt 10qqlr a~loııq as eithP.r.Çlock_iııput is LOW. ,t

TlıP ~<·111\IIIJCu,ııı IJı.•(T(u) aııd Tı)fl]linal ;;011111 Dnwıı (T̅C̅u) oıııııoı" ,ıır 11nııı.1llv1111;11 l.':1,rrı ;; ,·ıır•,•l lı,c "'o,·l""! ı:ı,' ,ııaxıııııııı roıııt sıa ıe (9 for tlır> LS197. :l lor ıııe t.S193). ıtw ,,,,,ı llll;H "' LOW ıı:ı"""" ,,ı ;, wıll c:ıııs ı• TCu ı o qn l.(•W. TLu wıll srnv lJ)I/J uıııl CPıı (Jlll'Sill(ill :ıq:ıirı. ılııı< rff,•1·!,vf'i·, r,•;ır""'• ;,... ,·., ·••, but ılrl,ıvr.cı by two çıaır rlı•l;ıys Sunil arlv. tlı<' TC0 ,n,ıııuı will qo LUW wlıPll ılıe cırı:ııl ,, "' tlı<• ıeın 11,111' ,, ·· ı "" '."""" Orıwıı yl.,d: qo=s LOW. SırıcP.thr TC outpııs rPpı>~tılıP clock w;ıvl'fıııırıı ıh•"! ,·,111 lı" tıseri ıs ılıı•, :,,,,l, oı·ı,,,ı ·,,qıı.ıis 11 (hl', ıır~t :111.jllPr (1f,j(!! Cill:llit 111 a nıtıltııtacr C()I/fllPr

Each r:ırc,ııt lı;ıı an asynchrorıoııs parallel load capalııılity perıııııtıırıq tlı<' couııtrr ın hP ;-ı•esrı Wlwıı the r:ıı:ıllr.l t ,ı.vl IF'I.) and ılır Master Reset (MR) inputs are LOW. ıııfoıııaıtıon present oıı ıtır raıall~l Daıa inputs lr0 F'3l ıs l(larlr.d ıııo tlıP coıııııer aııd appears on the outpu ts ıegardleıs of the conditions of thr> -lock inp,ıts A HIGH sıqnal rııı rhe Mastor n,•seı ıııpııı wıll dısalıle the preset gates, override tıoıh Clock ııpııts. aııd latch eadı () nıııpııt "' lhP t.OW sıat" lf""" nl ılı• c:,ıı l, ınpııı·, ,, I.OW duıing and after a ıeset or load operation. tlıP nr~t LOW to ltlGH tıansıiinıı ,ıf th;ıı (lnd' wıll lır ııırrrıı"ted as J lrqıtıınatr> signal and wıll he counted.

MODE SELECT TABLF.

MR	PL	CPu	cr0	MODF
H	X	X	X	flf'<•'t (ı\svıı
L	L	X	X,	rr P<;PT (/\Sr1'/ll
L	H	H	l!	Nıı (lı;ıııqP
l.	H	r	lt	Cıııııı; llıı
L	H	il	r	(~ıl 111 l)c ıw11

; · l. OVV Volf~Qf'l l_Pvt''l

I I ~ Hl(1H VolFitQP l PVPI

X - On,ı·ı r!:,,,,.

f - LOW ın·tltGH Cine~. Tı,ı"""""

~BSOLUTE MAXIMUM RATINGS !above wlıiclı tlır ıısr.ltıl lıfı>ıııay lw ıınp,ııPıl)

:Sthfag~ Temperature	!i!>'C ın ı l'.ıO C
Tr-mner aıur e (Ambient) Under Bia~	55' C «› 175 C
Vee Pin Potr.ntial to Ground Pin	05Vırıı/OV
• input Vol t aqe (del	0 'i V ıo 1'i V
• lıpııt Cur ı ent (del	JO ııı/ı l,, 5 0 ,,.rı,
Vnlt~qc Applir.d to Outputs (Output HIGH)	(1SVııı10 V
Ou ı out C:urıı,nt (de) (Output LOW)	ı50 ııı/\

• EılhP.f !ııpuı vnı,--~ır. 111111 oı lııpu, \.uıP.lH limiı ıs <ıffırı~lll ,,, pır,uır.ı lhP ,npı,ı•,

GUARANTEED OPERATING RANGES

f'AHT NUMtıt:HS	SUPPLY VOLTAGE IVCCI MIN	TYP	MAX	T[MP1:RATUAE
I ;41 ; I .J.'X I !I-11 ;j 1U.1X	45 V	5 OV	5 5 V	:C,5··C :o · f ZS «:
I /-1 (;; I U)X I /41 S I'.JJX	4 75 V	5.0 V	525 V	o•c1o•1o·c

X package type, D for Ceramic Dip, B for Plastic Dip. See Packaging Information Section for packages available on this product

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise spftcifiedJ

::iYMl:lül	PAAAMEIER	I.IMITS MIN	TYP	MAX	UNITS	TEST C0ND1Ti0NS
V_{IH}	lııı,uı ttıGl1 Voltıtgıı	20			V	Guoıııınıcıed Input HI(jH Vı:,lıeuıı foı All Inpuıs
V_{IL}	ınput LOW Vultıııııı	!>4 74		0 8	V	Guısıı,nı.,o<I Input LOW Voltage,
V_{CD}	l<ıı,111 (ldmı, Oıoor Voltag	54	.2·5·	o36	V	
V_{OH}	Ouıpu: HIGH Votıınor	74	2 7	3 4	V	VIN ~ VIH uı Vil ,,,,, Tıuıh r~tıl"
V_{OL}	Oıııı,uı LOW Volıogr	54 74 74				
I_{IH}	ınpuı HIGl1 Cuıtıuıı			,o	μA	tVcc-MA'(I/I's -27V
				0 1	mA	Vu_ - MAX VIN - / OV
I_{IL}	lııııuı l OW Cuıreııı			- 0 4	mA	Vee - MAX. VIN - 0 4 V
I_{OS}	üuıpuı Slıurı Cırcuıı t~uıc,ııt tNcıt~ 4)	-2~l		100	ıuA	Ycc " MAX. Vour o V
I_{CC}	)Juweı SulJn&y Cuuttot		19	34	mA	Ycc " MAX

r·H.J It~

1 ~.ı•ıJıuı,n) fuı_ ıe,ı,ııy. ıııuw .t,own ın ıhe ••lı'•. ••• c..hoıan hJ IJU-I'••lIN vpeı.ıllUn unue, "w,.ıı,ı cc.ıc l:ünt.Jıııuııı.

2 Ilıe ,.~~ıllıeı.J \ Mt IS ,c·p,~ıetll the "woııı (;in•" v•£ue fo, the P•••nı•ıe, Sıııı.:eıtı•ıa ..._u,ıı <-•••" volun ııoıraıullv ııu_.uı .ı ttıııı tetnpeı• ;u~c dl)~ hJ~i;lV 'clUil~<J• ~.1ulleulel. cu.kJ~HQ;\4M;'.,0;1tııımuıı(y .ınd gJtUı.J ı.J4ıkJıff) C4U btı dA,;hıcv•tJ l.Jy dı,c:ıc:auııy me dllO._.dJlff \VlIMfl ı~~c•<Jl•"•J ı•.,VI:-1

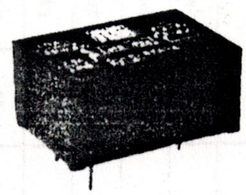
J 1,p ", ol l,ııııl\ •C ", V CC · 5 OV, TA - 2~[0] C, 4ntJ fHc,,unu,,n hı.dın9

4 N,.ı ııı.,,e th•ıı vıııı ,·Jı,ıput •hout<J L4ı ,huıetJ •••lune

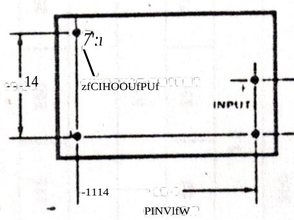
Solid State Relays

Havinq n scaled construction witlı 110 rıioving parts ılıı.,sc solid state relays me particularly suited to a.c. switchinq applications rcquiri11g lonq life and Iıiglı mlinbitiv. Tlıc switchinq is silent, causos no arcing and is ıın;11fr~ctcdıy vibration and corrosive auuo suherus. The control input is optici111y~isolatm1 froın llı!! ,mo voltage switchiııu circuit which prodıices virtuallv 11oRF iıterfercncc. May ile oper.rtr,d lıy TTL open collector. Output circuit is 'nominallv onou'. Whmı an iııdııctivc load is to be switcltPd a11 ndditioıı.11 snubber nntwnrk (O.tJ. 238. -1G3 for ,~OV ,111<1623-338 for 415 V supplies] rmıy.tio·'- hmıl?fici;ıl hut the nutwı ır k is mnnCkıtory-for the dunl-in-line i11d plug-in 8-pin styles which do noi !wvı• ııııı•qıal snubber ıwtwork~. For protection iHlitıl~t tln- <'fir.cıs of transiunts. thr. connection of a ıı~ı_Hal oxidı? varistor (o.q. 649, IGG I[ır 2i\O V :u1<i G40-2 73 Inr 415 V suppliosl across tlıc relay output is rcconıııııcıid,~d. ııı addition, ıhc couuoction of a rneta! oxidP varistor across an inductive load can licIp to nıiriı111is. ılıe transmission nf transients. Generally no fı,r,ııiııg is required for larnp loads due to tho ~xccllerıı surge capability.

PCB Mounting



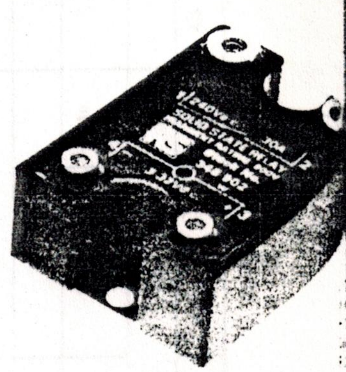
l.38·1 W2S~ lt.17A
riıı lrm~ıh A Oi;ı 0-H



S.S.M.	
type	stock no.
25A	349-692

Surface Mounting Power

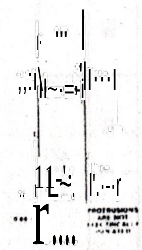
Pll!alffl.Y
Hm)Ol1Cf0 I...l



/\ rnıt,ıı (ıf ~~ıırf.:H:c ınoiıı,ting optically coue-sıat,~ ı ı~l:ıys iri tho irnlı ıstry standard rectanc packaıqc. Availal ıln v/itl ı n.c. or d.c. conuone L.Hıd ff?öltrillU zero voltcr<Je switching to mr,' l:ıruc currunt suıqcs nııd n.F.-1. Output deve-citlım trinc or inverse parnllel thyristors iS.C. lı1ttcr being prcfcrnhlo in applications invol,·. liric voltrıqes or lıi!Jlıly inductive loads. Allt·.;. suuanio for sinqlo or tlırf)e nhnse switching npplicnıions. All relays are ııtr.rııllly R.C. heat sink sırctı as RS stock rıo. ~01·958 (in!' Snmicondı ıctnrs. Ht>ntsirıks:SodetsiAccs; slıoııld hu u~ed ;ıııd it is essential thaı h'IJ cornpoırrıd (RS stock rıo. S5~·311. in the El Services ı\id~ section 17) is applir!d. Seeait.., dıta t;ılılı, for lıııl SfH'cificnıioıı Approvnl~ in process:VOE, CSA. VL

max load rating	transient rating	stock no.
3-32V d.e. controlled input		
1OA 250V	600V	346-895
1OA 250V	800V	346-889
25A 250V	600V	346-918
JOA 250V	800V	346-902
45A 250V	600V	346,687
1OA 480V	1200V	eJS0,490
2511 480V	1200V	352,503
45A 530V	1200V	a 352.s90
85-280V a.c. controlled input		
10A 250V	650V	352-519
25A 250V	650V	352·525
45A 250V	650V	352.531

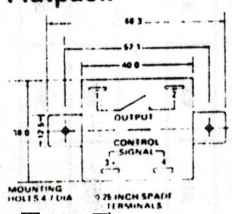
Dil



Solid state relay in industry staridarıt T0116 nackaqe, ratcu ar' 1 /\ wıthouı heat sink at ılp to 35"C ambient ıcnıpcraıure.

S.S.M.	
type	stock no.
1A	346-671

Flatpack

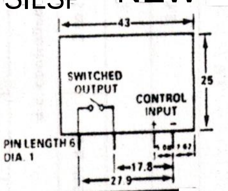


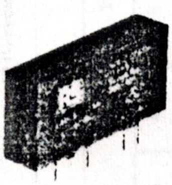
T --rT\ rn
"(ı-;·;··l uh
JTr,::L

5 A solid state relay housed in tlat pnckag<' with lıolt down lıigs nııd 0·25 in flat spc'.Hh? tı?rr11iıınls rıccorıııııerııtr,d heat sirık 2"CW 1153 153 1'fi mm nhıı11iniuın).

S.S.M.	
type	stock no.
5A	346-384

SILSP NEW~



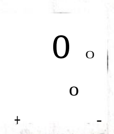


101][" ~NVII~ 'j}el

Compact package with single in-line 0·1 in pitch COJIIH~CIIOII pins.
Approvals in process: VDE. CSA, UL.

S.S.M.	
type	stock no.
2;5A	348-431
4·0A	[iii 353-001

8-Pin Plug-In



H.llınılyl 55
0.35
W35

Solid state relay housed in an 8-pirı plug-in module. Connectiohs to tho nor molly open output switch and ,·.d.ç~c.orıtrol ii:ıput ore pin cornoauute with RS octal elçct.romechaı:ical relays. Suitable for use in environments w~ere rnnchanical contacts may he contmninoıed or cquse unrtosirahle arcing.

S.S.M.	
type	stock no.
7A	348-598

See also mlcroprocesıcn Input/output moduleiii ProceH Control and Computing/PLC'n

Data po

Il nrıy;ıl M;iil Pnrcets Service

How ta Order

- Plt-ı,,• o,d,. tlttt numbe, of pricPd urıttı yourwqui,e of NCtı str,r,lır 11,ımb.r,nıurtg,91hıt fhfl quantity ordefed •• diviiiltlt' by thf :i.S.M.
- P,...ıu,ı. •" only nttllable lft multiplee of the I.S.M.
- Fo, moı• infomıation. 1Nthe fi,ıt ı,a,ıeof thlı uteıoıı,e

At 25 C when mounted on a heat sink 1 C/W 10/25 A; 0·5 C 45 A	Units	346-671	348-431	[illegible]	349-692	346-384	348-598	[illegible]	346-902	[illegible]	[illegible]	352-890	[illegible]	[illegible]	[illegible]
CONTROL CIRCUIT		[illegible]						d.c. controlled					a.c. controlled		
V_{in} Input voltage range – max.	V	3.8 to 32V d.c.	3 to [illegible]V		[illegible] to [illegible]V d.c.		[illegible]V d.c.	[illegible] 32V d.c.			[illegible] 40V d.c.		[illegible] 280V a.c.		
Z_{in} Nominal input impedence	kΩ	1.0	1.5					1.5			1.0	[illegible]	43		
V_{on} Must-operate voltage	V	3.8	[illegible].0					[illegible].0			[illegible].0		80		
V_{off} Must-release voltage	V	1.3	1.0				[illegible]	1.0					10		
tr Response time – max. at 50 Hz	ms	10 (½ cycle)						10 (½ cycle)					10 (½ cycle)		
LOAD CIRCUIT															
Output devices		SCR	TRIAC					TRIAC			[illegible]		[illegible]		
I_{max} Load current – max.	A r.m.s.	1	2.5	4.0	[illegible]	[illegible]	[illegible]	[illegible]0	25	30	45	10	[illegible]	45	10	25	[illegible]
V_{max} Load circuit voltage range	V r.m.s.	[illegible] 280	28 to 280		[illegible] 280		[illegible] 280	28 to 280				50 to 530			24 to 280		
I_{max} Single cycle peak current overload	A pk	[illegible]	85	[illegible]	[illegible]0	[illegible]	100	115	300	250	[illegible]	[illegible]	260	390	115	250	375
I_{min} Minimum recommended load current	mA r.m.s.	20	50	100	50			100	150	500		500			100	500	500
I_{osm} Off-state leakage current – max.	mA r.m.s.	[illegible]0	[illegible]		[illegible]0	[illegible]	[illegible]0	[illegible]				[illegible]			6.5		
I^2t For fuse selection – 10 ms	A²S	5	36	66	30	[illegible]0	66	66	450	310	700	66	338	760	[illegible]	310	700
V_t On state volt drop – max.	V pk	[illegible].[illegible]		1.6	1.25	[illegible].[illegible]	[illegible].[illegible]	[illegible].[illegible]	[illegible] 1	1.5	1.6				1.6		
dv/dt Critical rate of rise of voltage – min.	V/μS	[illegible]	[illegible]00		50	[illegible]0		200	50	200					100	200	200
dv/dt Commutating Snubbed for 0.5 PF		[illegible]0	[illegible]				[illegible]0	yes							yes		
V_{DRM} Peak repetitive off-state voltage – min.	V pk	400	600				400	600 or 800	600	800	600	1200			600		
GENERAL																	
V_{is} Isolation voltage input to output	kV r.m.s.	2.5	[illegible]0				[illegible].[illegible]	[illegible]0			[illegible]0				[illegible]0		
V_{isb} Isolation voltage input/output to base	kV r.m.s.					[illegible]0		[illegible]	[illegible]	[illegible]0	[illegible]0				2.5		
T_{op} Operating temperature range	°C	– 40 to – 100	– [illegible] to + [illegible]0			– 40 to – 100	– [illegible]5 to + 80	– [illegible]5 to + [illegible]00			– [illegible]0 to + 80		– 40 to + 80		– 40 to + [illegible]0		
F_{op} Operating frequency range	Hz	47 to 70	[illegible]0 to [illegible]5				10 to 440	47 to 63							47 to [illegible]5		
θjc Thermal resistance (° θja)	°C/w	60.0°				11.0		[illegible]0	1.8	1.1	[illegible]5	4.1	1.1	[illegible]0	[illegible] 4.3	[illegible].1	0.9

† Constant current input

intel

2716
16K (2K x 8) UV ERASABLE PROGRAMMABLE EPRJM

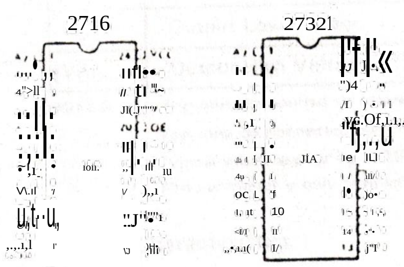
- Fast Access Time
  - 350 ns Max. 2716-1
  - 390 ns ~ax. 2716-2
  - 450 ns Max. 2716
  - 490 ns Max. 2716-5
  - 650 ns Max. 2716-6
- Single +5V Power Supply
- Low Power Dissipation
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power
- Inputs and Outputs TTL Compatible during Read and Program
- Completely Static

Tt.e lmer' 2716 ii" 16,384 tit ultraviolet erasable anJ etecu icaiiv programm.iule reaJ-only memory (EPROMI. The 2716 c,peiistcs from J iingle S·iiült power supply, has a s iauc standby mode, arnJ features fast iinyle aiJdieo location program· miny. It rii.~es ucsiyiiny with EPROMI taster, easier oniJ more economical.

Il\,I' 17.16, witli it> ,ingle 5· volt supply aniJ with an access time up to 350 us. is iiJeal for use with tne newer hiyh pdrformanci 5V miii;roprucessors such as Intel's 8085 anJ 8086. A selected 2716-5 and 2716-6 is availablt for slower speed applications. The 2716 is .il>o ·thu first EPROM with a static standby moue which reiJ~ces uie power dissipauon without increiisiriy access iiine. Tlic iii.i,.ii.nii,ii ~uivc power d)~sipatioii is 525 mW whiili uie maximum siandliy power ulssipauon is only 132 mW, a 1~·1:. suvu I~f,.

The 2716 has the iinplest and fastest method yet devised for programming EPROMs - single pulse TTL level proyramming. Nu iietd to, hiyti vultöijti pulsing because ·all prograriiimiiig contr ols are handleiJ uy TTL sigiials. Program any locauon at any iiine. eimei iidivii.lu.illy, sequiintially or at random. with the 2716's single address location prograinrning. Total programming """' lor ail 1ti.J84 bits is only 100 seconds.

PIN CONFIGURATION

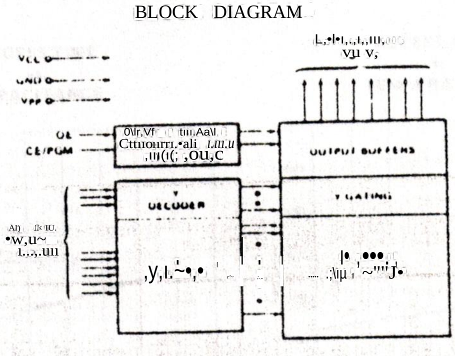


t Refer to 2lJ2 Ll•ta sheet tor ~pt:lı fı<.;4tıuns

MODE SELECTION

PINS / MODE	CE/PGM	OE	VPP	VCC	OUTPUTS
Read	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Standby	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Program	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

BLOCK DIAGRAM



PIN NAMES

A_0 - A_{10}	ADDRESSES
CE/PGM	CHIP ENABLE/PROGRAM
OE	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

PROGRAMMING

The programming specificarions are described in the Dara Catstoq PROM/ROM Prn9raınmin<1 Irıs tt ırtuııis Senin,/

Absolute Maximum Ratinqs "

Teınnerature Under Bias. . . . .-10°c to .soc
Stu, age TenıpP.rature . . . . .r,5"c lo 125 C
/\II Input or Output Voltages wiılı ňpsprct to Grounıd . . . . ıGV ın -O .IV
Vrr Sunplv Volt~ge with Resper.! ıo Ground During Proqram . . . . •2G.5V ıo·-0.3V

·coMMENT

DC and AC Operating Conditions During Read

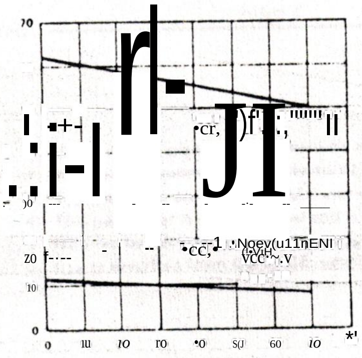
READ OPERATION

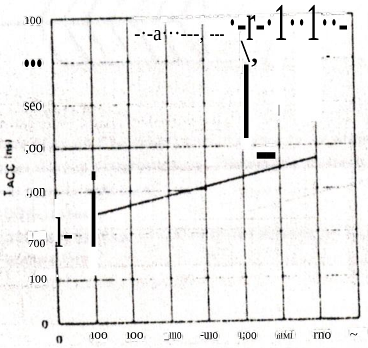
O.C. and Operating Characteristics

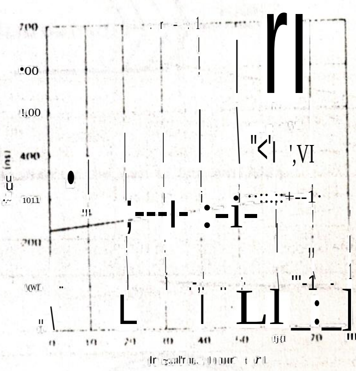
Symbol	Parameter	Limits Min.	Limits Typ.[3]	Limits Max.	Unit	Conditions
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.25V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.25V$
I_{PP1} [1]	Vpp Current			5	mA	$V_{PP} = 5.25V$
I_{CC1} [2]	Vcc Current (Standby)		10	25	mA	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$
I_{CC2} [1]	V_{CC} Current (Active)		57	100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

NOTES:
1. Vee mus t be npplıttd simult:,nr.ou,çly or hP.loıe Vpp and ıı~ıııovNI sıııull,'UIAOUSiy nr ;ıl lP,f Vrr-
2. Vpp mav be connecıed directly to Vee excent during proqı,ıııııııır~. Thr. suoruv ı:uııı:ııı wmılıl ihru ıiP ihr<: <:ıOıı nf Icc ;ııHI rrı
3. Typical vaı'uP.1are for T/\"" 2S"C and nominal suourv ı.ııılt<1<Jf!S.
4. This pareme ter is only sample1·i and is not 100o/" tP.Sted.

Typical Characteristics







2-8

A.C. Characteristics

Symbol	Parameter	Limits (ns) 2716 Min.	2716 Max.	2716-1 Min.	2716-1 Max.	2716-2 Min.	2716-2 Max.	2716-5 Min.	2716-5 Max.	2716-6 Min.	2716-6 Max.	Test Conditions
t_{ACC}	Address to Output Delay		450		350		390		450		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390		490		650	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120		120		160		200	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	0	100	0	100	0	100	$\overline{CE} = V_{IL}$
t_{oh}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

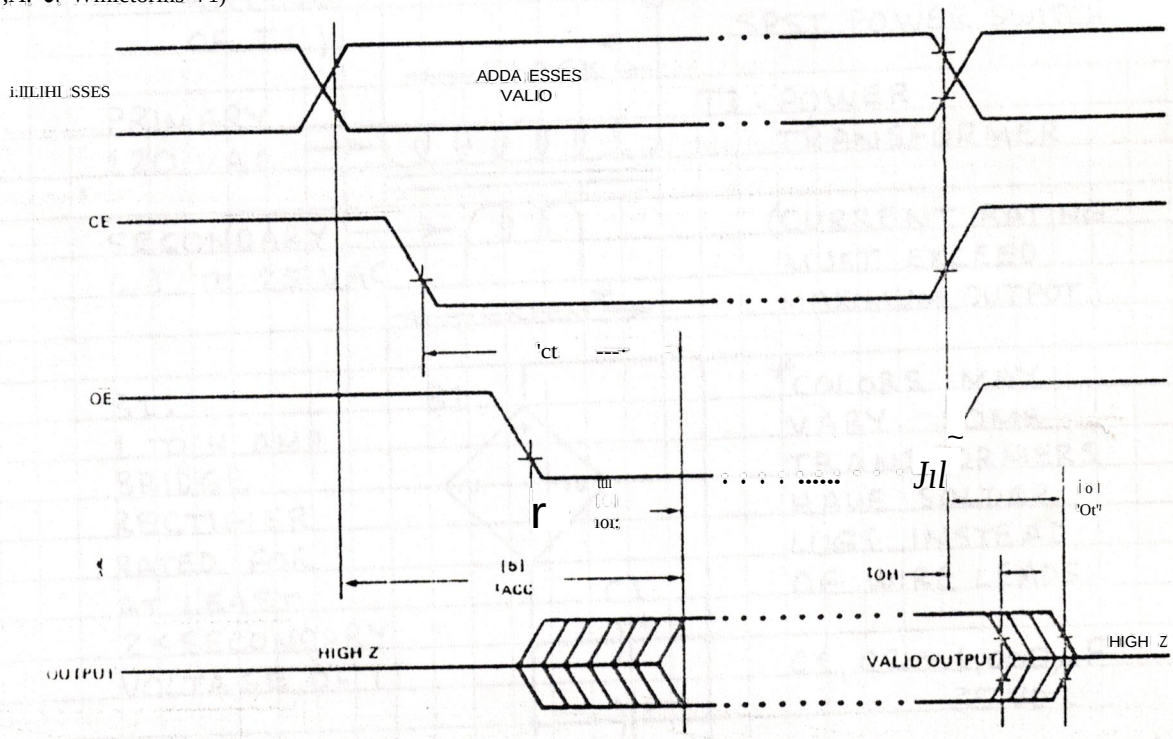
Capacitance [4] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. Test Conditions:

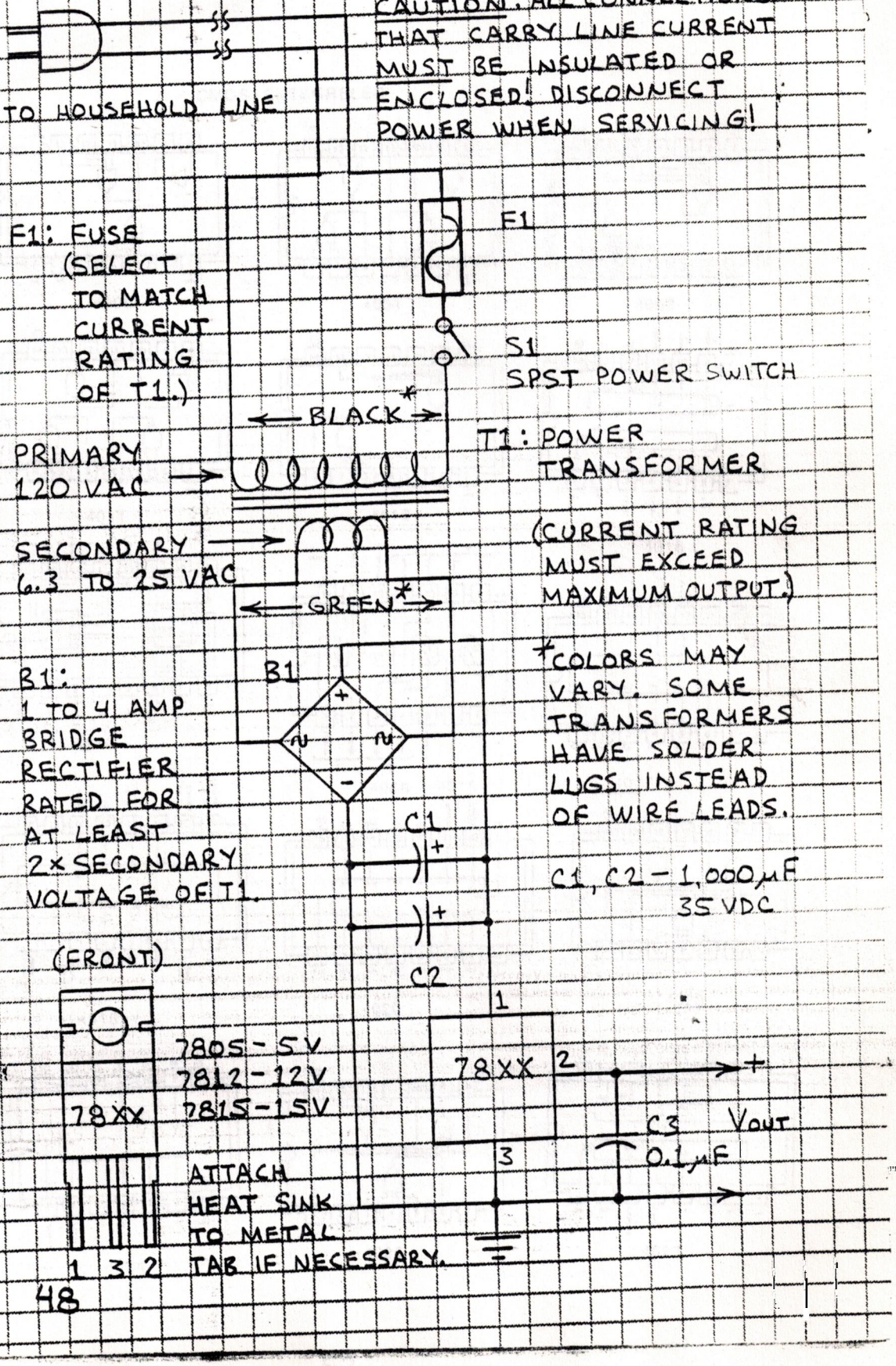
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms [1]



1. Vee may be connected directly to Vpp, except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
2. Vpp may be connected directly to Vee except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
5. Output Float is defined as the point where data is no longer driven — see timing diagram.
6. t_{DF} is measured from $\overline{OE}$ or $\overline{CE}$, whichever occurred first.

LINE-POWERED SUPPLY



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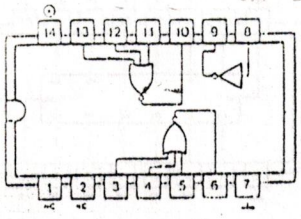

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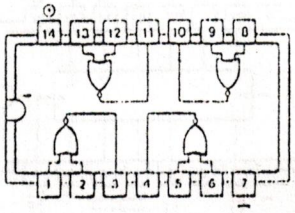

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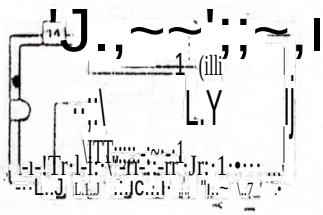

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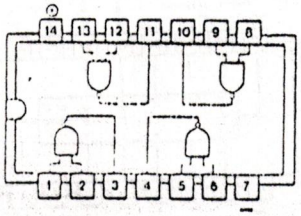

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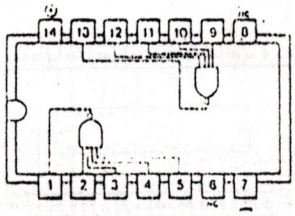

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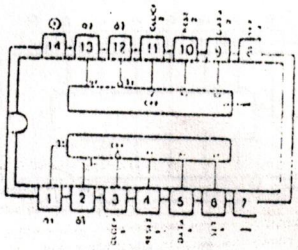

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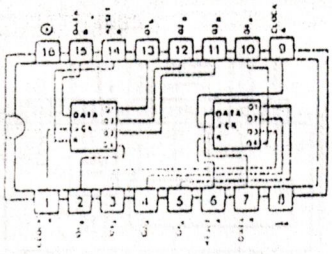

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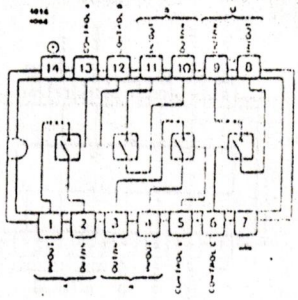
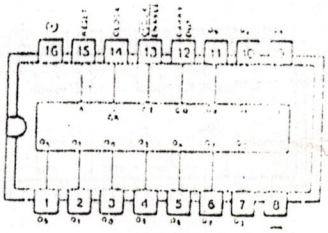


4066 4016



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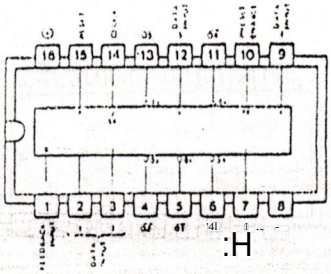

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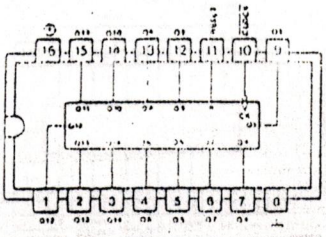

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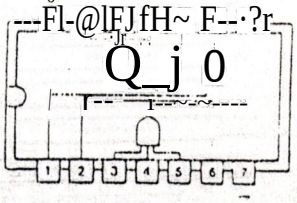

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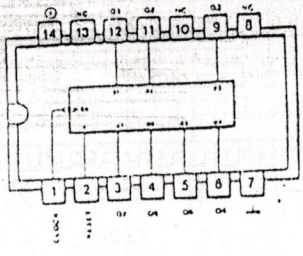

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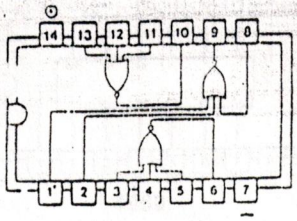

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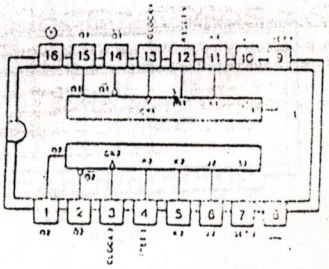

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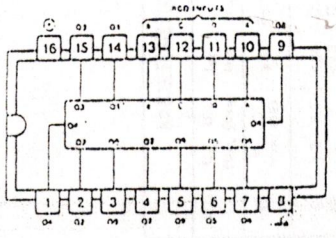

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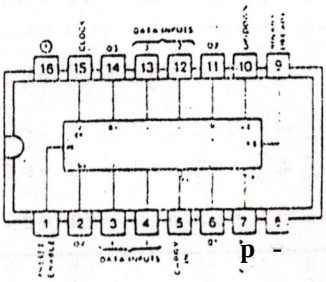

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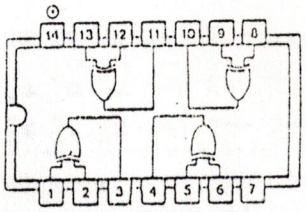

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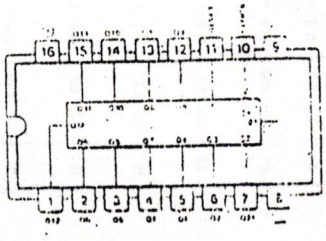

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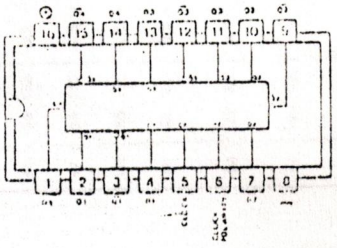

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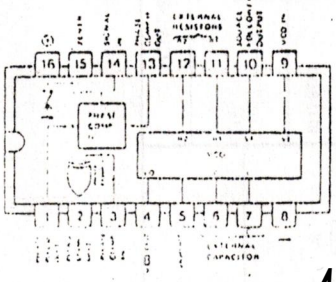

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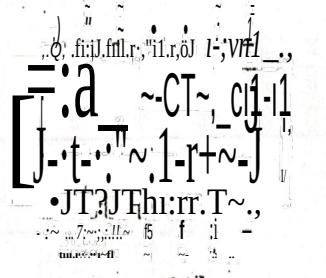

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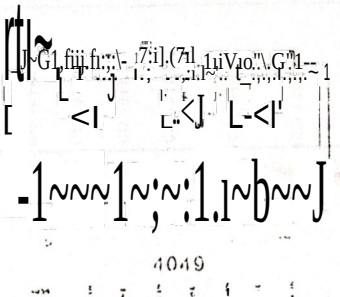

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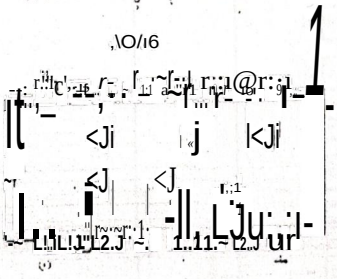

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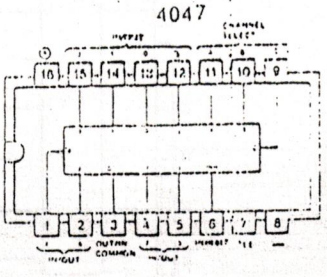

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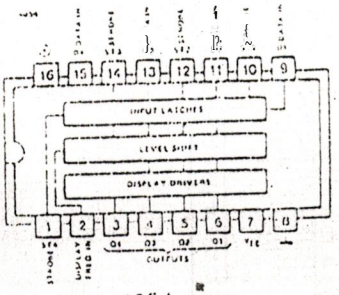

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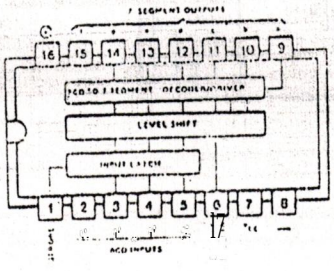

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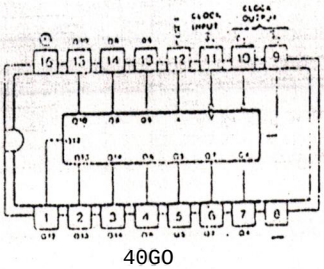

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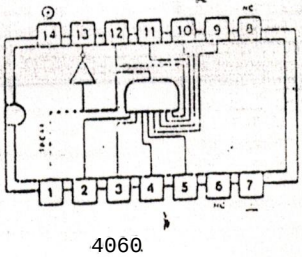

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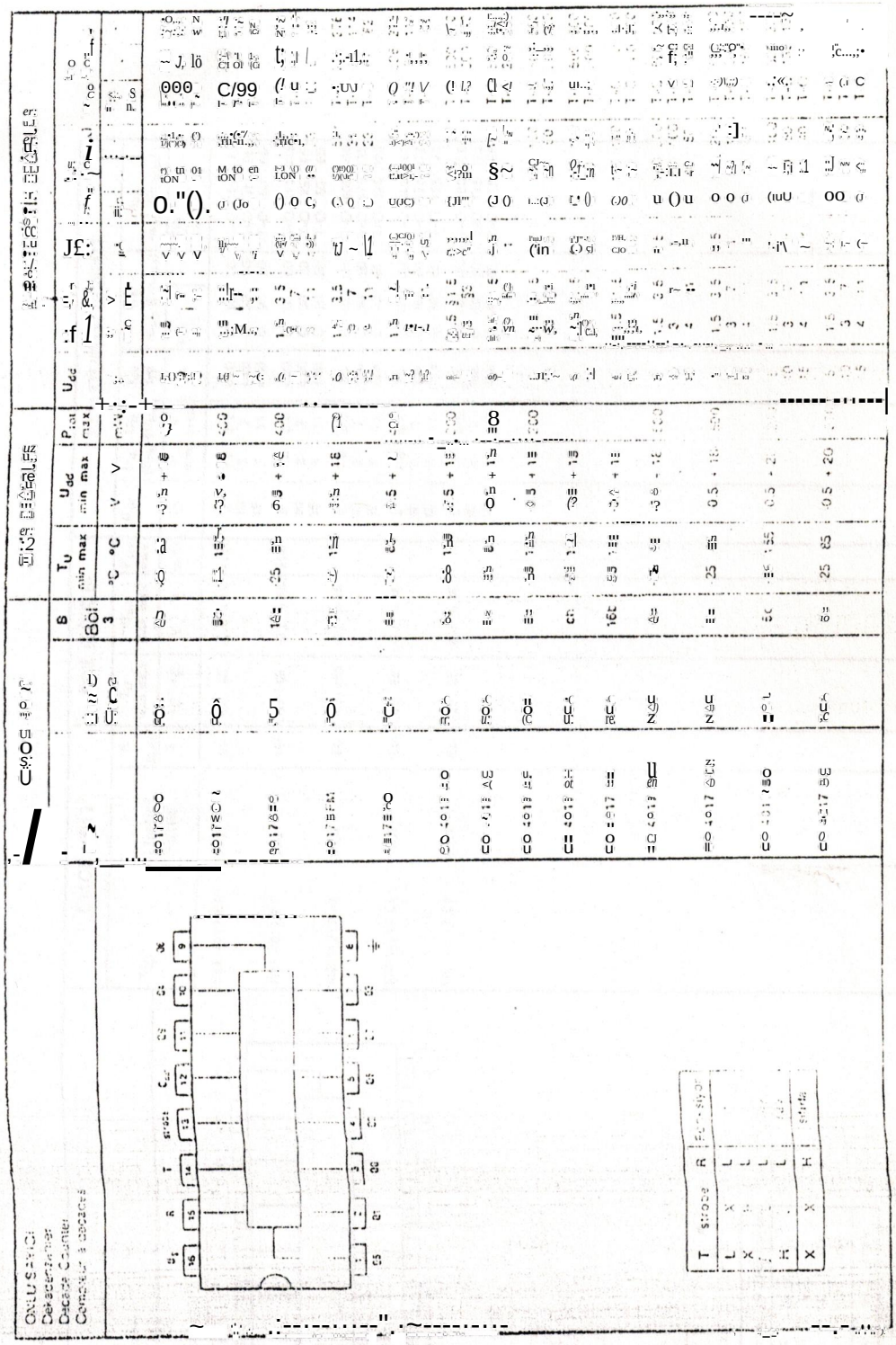
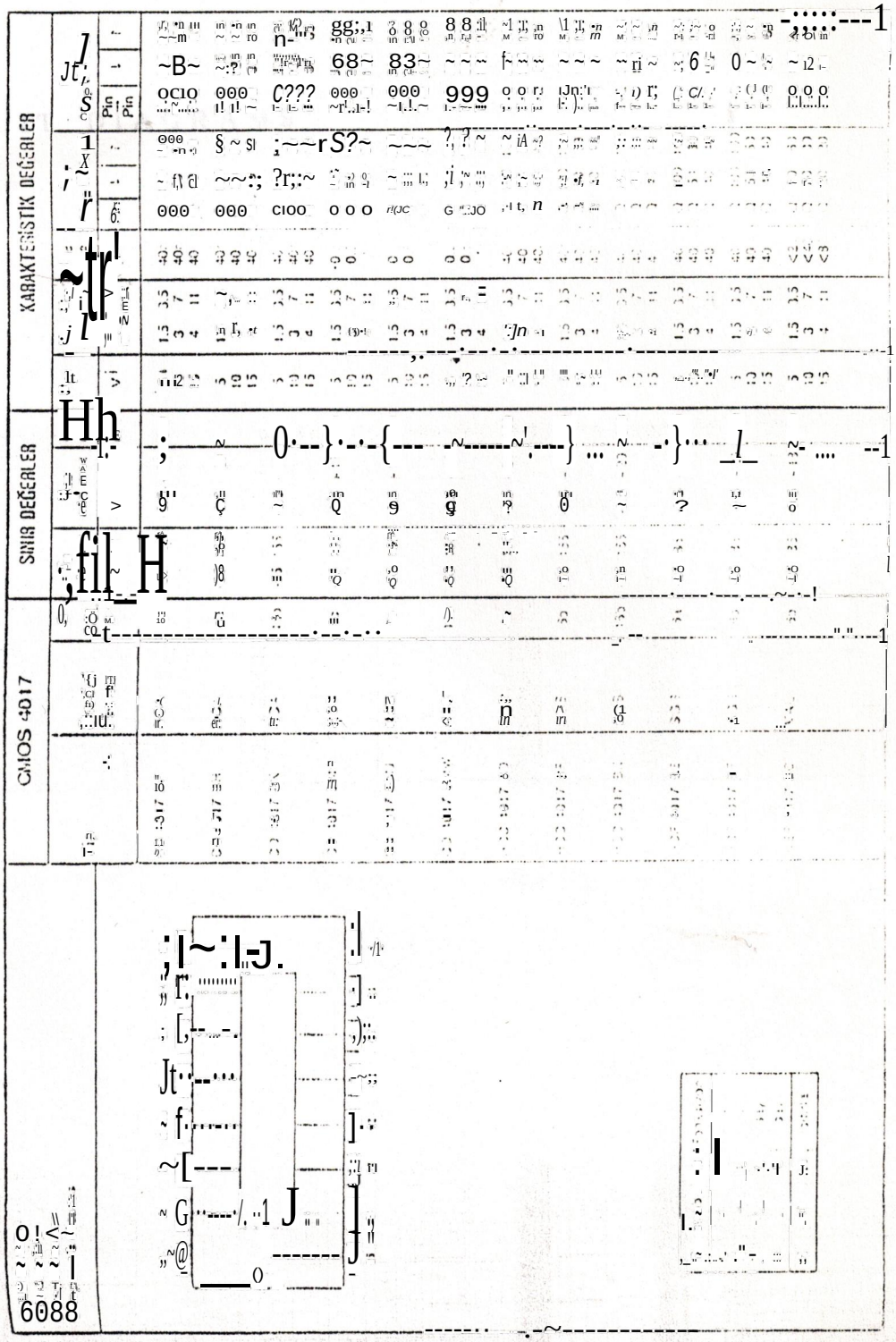
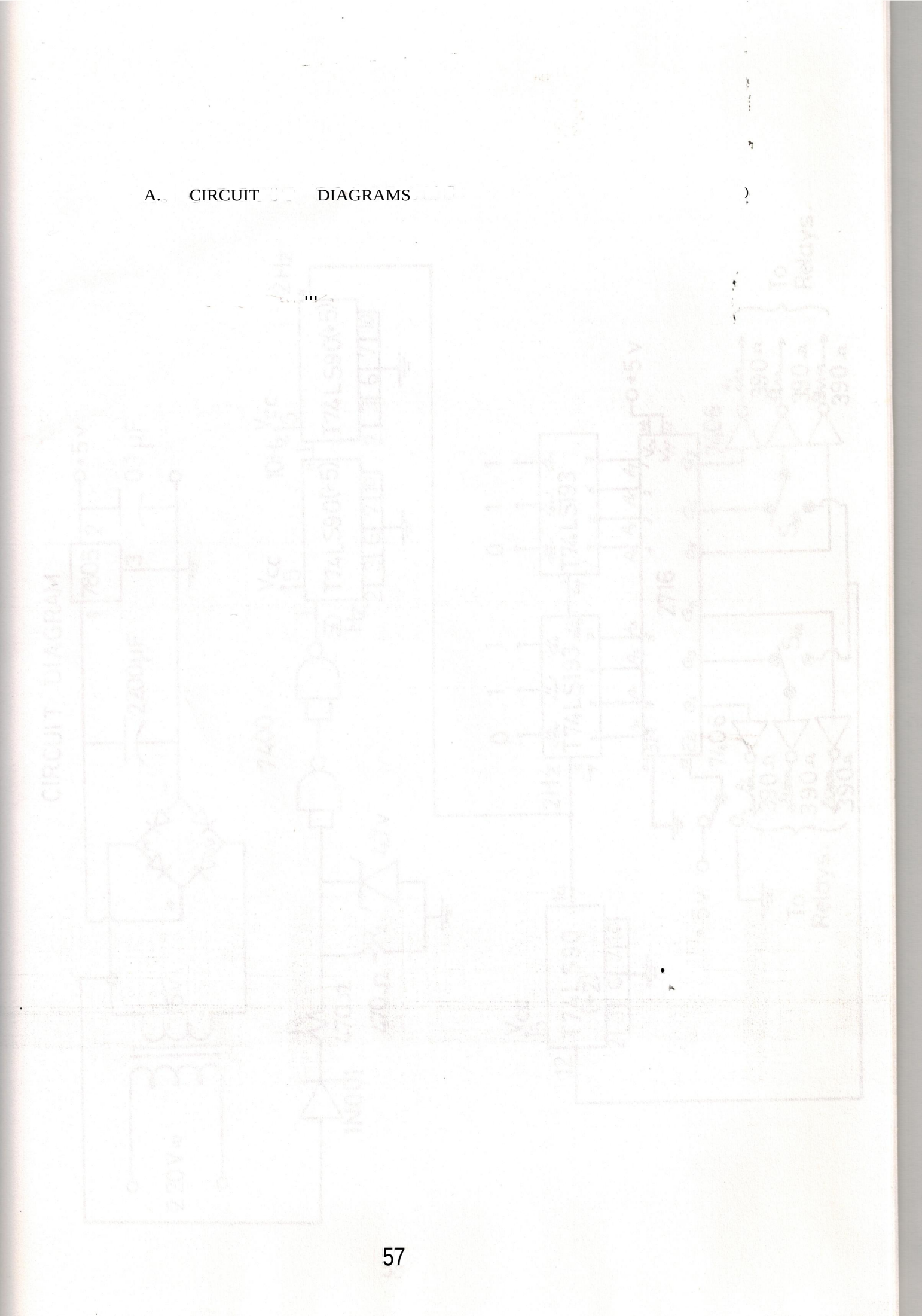
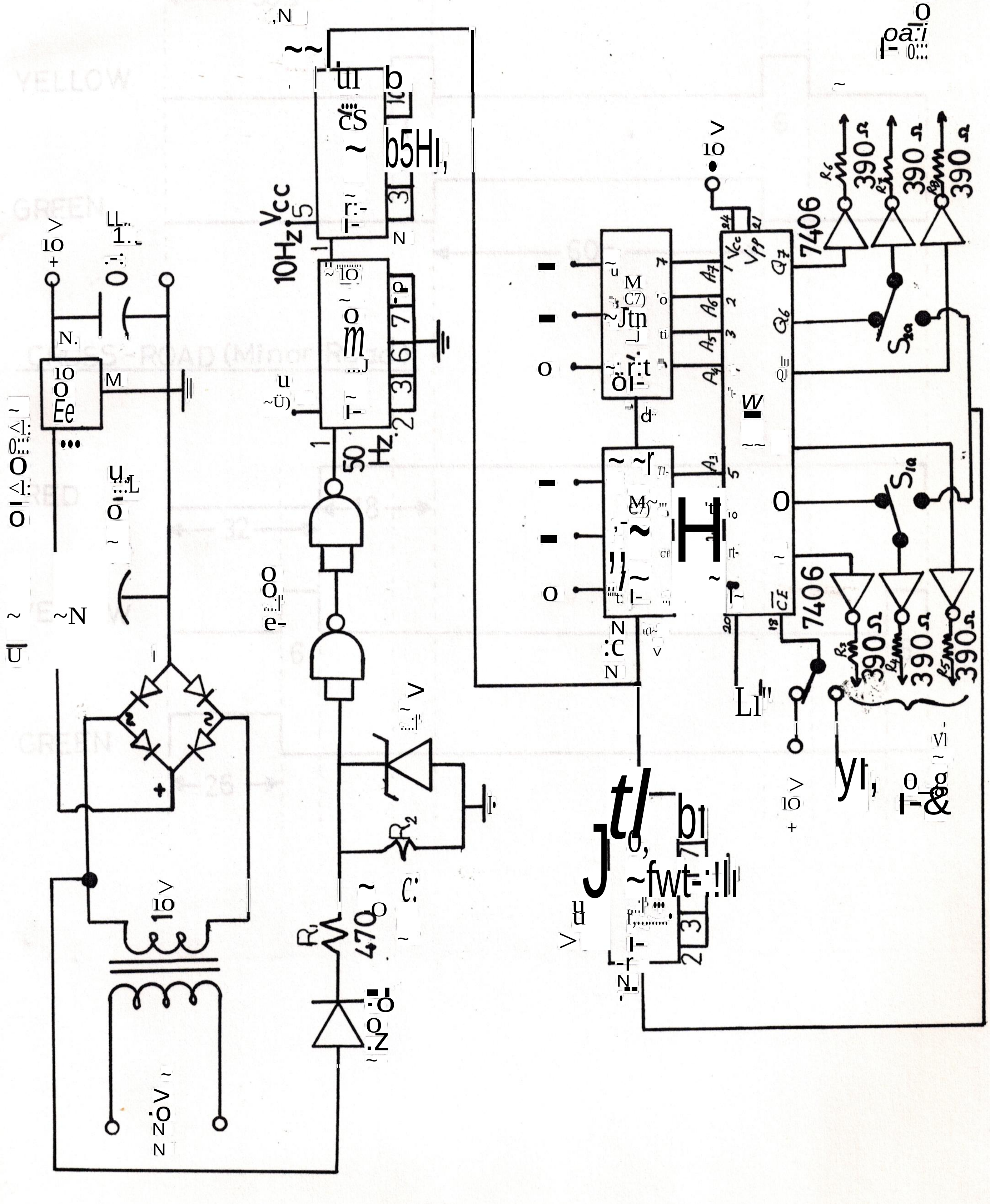


ONLU SAYICI
Dekadenzähler
Décade Counter
Compteur à décades


KARAKTERİSTİK DEĞERLER
SINIR DEĞERLER
CMOS 4017

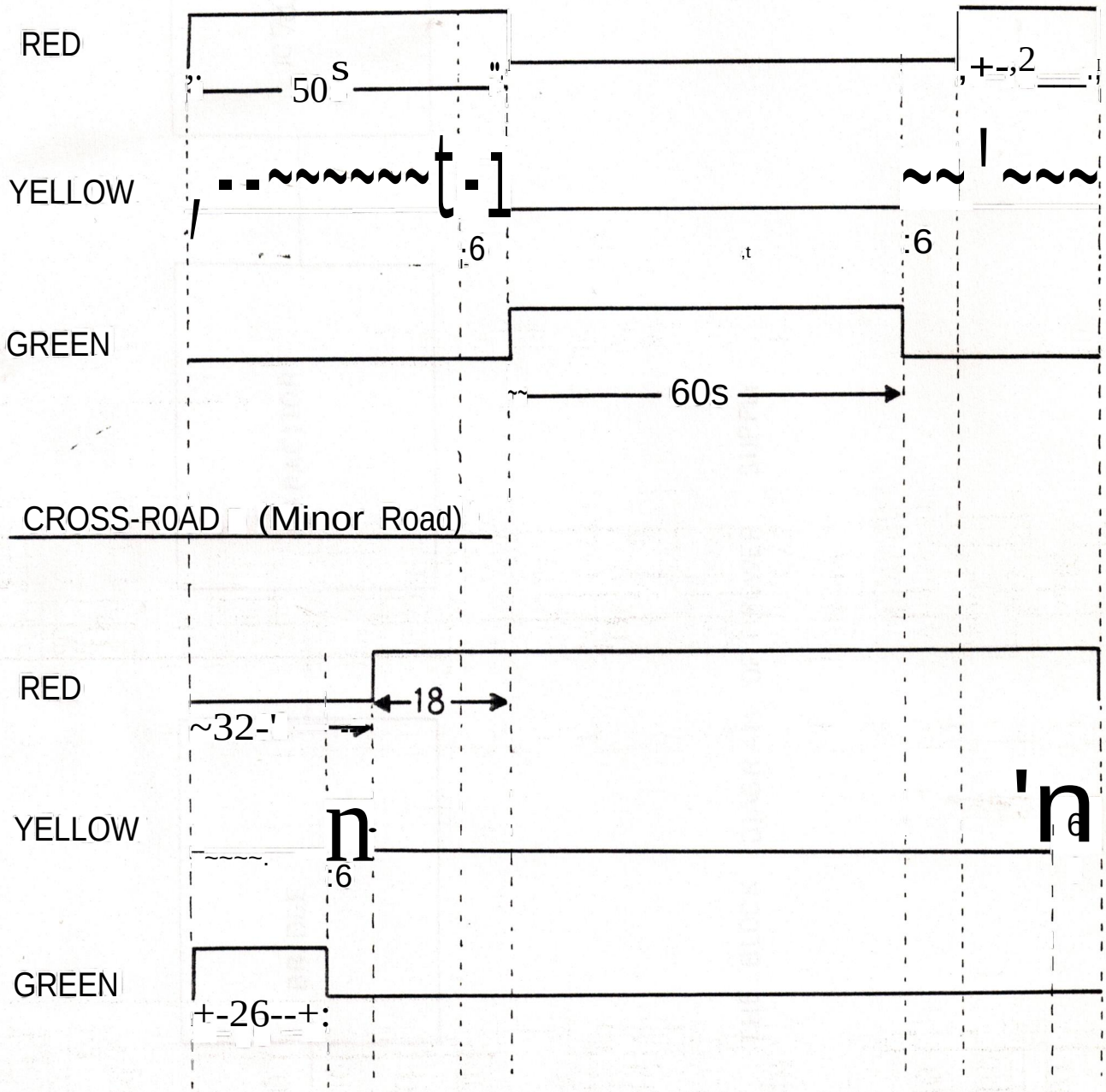
A. CIRCUIT DIAGRAMS




7406
7406
390 Ω
Vcc
10Hz
50 Hz
470

TIMING DIAGRAM

HIGHWAY (Major Road)



BLOCK DIAGRAM OF

B. PART LIST

B.. PAR'r LIST

R1 == R2 ... 470 5l

R3- ... R4 =R5 = R6 = R7 = R8 = 390sl

C1 = 2200 μF

C2 = 0.1 μF

Regula.tors (x2) = 7805

Diode =. 1N.oa1

Z-ener D1od·.e = 4o-7 VJ-

ID.= 7400
If2 = IC3 ::,IC4= == T.7 4LS90
IC5 = Ic6 = 'f74LS 193
Ic:J = 7 406

ZFROM =2716

SSR.::: Solid S.tate Relays (x6) = (SIEMENS*V~3103* -S20)2-
- B402) 3-30v DC, 240v .:..C, 2.5A o

Socke.t.s (:x4)' =-1pin., 2.pins }pins , 6pins

connec tors (1.2 pin x 4).

Lamos (x12.) ... 4 red ~ 4 green , 4 yellow

Laff!!) holder (x12

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