NEAR EAST UNIVERSITY

Faculty of Engineering

Department of Computer Engineering

SWITCHING IN ATM NETWORK

Graduation Project

COM-400

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Acknowledgement

I am grateful to my supervisor, Dr. Halil Adahan for his supervision, encouragement, patience, support and suggestions throughout my studies.

I would also like to thank to my house friends , brother and classmate for giving me the books and related paper that I needed for the preparation of my project.

Finally, I want to dedicate this project to my family who supported me with their love and patience.

Abstract

Modern applications in today's Computer Networks include the use of types of network system such as ISDN ATM. The extensive use of ATM makes it possible to bring various applications into progress to facilitate application development. ATM technology not only applies with modern Computer Network standards. In this project subject is switcching in ATM networks..

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Chapter I: Introduction

Introduction

Asynchronous transfer mode (ATM) is rapidly become the primary transfer mode for implementing broadband itegrated services digital netwrors (B-ISDN) These ISDN networks carry data, full motion video, audio, etc. Nowadays, networks, with transfer demanding even high transfer rates of 100 mega bits per second (MBPS) to 622 MBPS are common with users demanding even high tansfer rates. Giga bits per second (GBPS) and tera bits per second (TBPS) networks are beging designe and tested, to satisfy the increased bandwith requiremnts.

ATM netwrorks consist of two major parts; transfer medium and switches. The medium typically used is optical fiber, which can theoritically support infinite bandwith. Hence, It is not limiting factor, but rather ATM switches are the bottleneck to achieving high transfer rates. An ATM switch consists of two main components; switching elements and aswitching fabric. The switching fabric is composed of ideal elements, which are interconnected in a specific toology.

In the past, various switching arthitectures were developed for different applications, such as voice and data based on transfer modes like synhronous transfer mode (STM) and PTM are not directly applicable to broadband ATM.

The three main factor that have impact on the implementation of broadband ATM switching arthitectures are :

1. The high speed at which the switch has to oparate (from 150 to 600 MBPS).
2. The statistical behavior of the ATM streams passing through the ATM switch.

ATM is connection oriented. There for the switching elements have pre-defined relating tables to minimize the complexity of single switch routing.

In this reports an ATM switch, the ATM cells are transported from an input port (out of N input ports) to one or more output ports (out of M output ports). This switching from input port to output port might be combined with concentration, expansion, multiplexing and de-multiplexing of ATM traffic An ATM switching system is much more than a fabric that simply routes and buffers cells (as is usually meant by an ATM switch), rather it comprises an integrated set of modules. Switching systems not only relay cells, but also perform control and management functions. Moreover, they must support a set of traffic control requirements.

This survey is organized as follows. First, how to operate ATM switches basically and various switching functions snd requirements, and then switch fabric are discussed. Then a generic functional model for a switching architecture is presented to simplify the ensuing discussion. The core of the switch, the switch architecture, basic operation of the switches and switch fabric.

Chapter II: ATM Switch Arhitectures

Basic Operations of ATM Switches

2.1 Switching

Switching is the transportation of information from an incoming ATM channel to an outgoing logical channel. A logical channel is characterized by

1. A physical input port / output port having a physical port number.
2. A virtual channel identifier (VCI) and virtual path identifier (VPI).

To perform switching, both the input port and incoming virtual channel/path identifier have to be related to the output port and outgoing virtual channel/path identifier. In any ATM switching system these two functions have to be implemented and can be compared to functions applied in classical STM switching systems, as shown in Figure 2.1.

Information from input port 1 is transported to output port *3,* whereas information from input port 3 is transported to output port M. An important aspect of space switching is routing. Relating virtual channel/path identifiers is comparable to a time slot interchange (T) in a time switch as shown in Figure 2.2. Information from time slot i is switched to time slot j, whereas information from time slot k is transported to time slot 1.

Modern STM switches are often composed of these S and T stages, in different sorts of combinations like STSTS, STSSTS, or TSTTST. In ATM switching systems, however, the time identification in a fixed frame is replaced by logical channel identification. Since the pre-assigned time slot concept disappears in ATM switching systems, contention problems arise if 2 or more logical channels contend for the same time slot. This can be solved by temporarily queuing the ATM cells before sending them out This queuing function is the second important aspect of ATM switching systems.

2.2 Concentration / Multiplexing

In ATM, the distinction between multiplexing and concentration is rather vague. Multiplexing is used when the emphasis is put on the statistical merging of different ATM virtual channels (cell streams) on a single ATM stream. Concentration is used when the stress is on the reduction of a number of input ports to a smaller number of output ports.

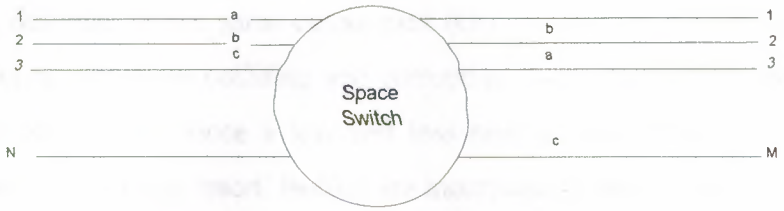

Figure 2.1.1 Space switch

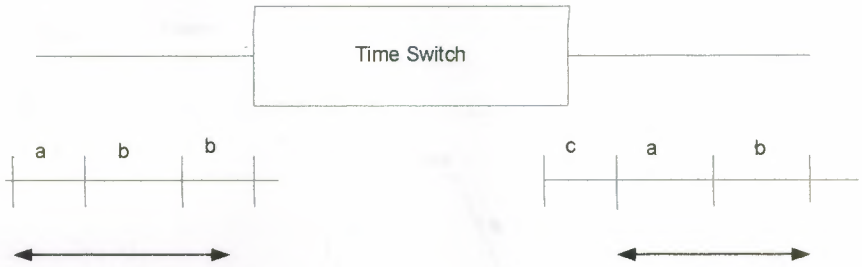

Figure 2.2.1 Time Switch

2.3 Basic Function of an ATM Switch

The basic function of an ATM switch is shown in Figure 2.3 Incoming ATM cells are physically switched from an input port li to an output port Oj, and at the same time their header value is translated from an incoming value of a to an outgoing value of b. On each incoming and outgoing link, the values of the header are unique, but identical headers can be found on different links. For example, in Figure 2.3 and Table 2.1., x appears on two input ports II and In. All cells which have a header equal to y on incoming link II are switched to output port Oq and their header value is changed to m.

All cells with a header x on link hi are switched to output port Ol and their header value is set to n. Two main tasks that need to be performed by an ATM switch are:

1. VPI/VCl translation.
2. Cell transport from its input to its dedicated output.

An ATM switch performs VPI / VCI translation by modifying the cell header. Cell transport from its input to its dedicated output is achieved by space switching. It is possible for two cells arriving simultaneously from different input ports of the ATM switch, destined for the same output port (Ol). To prevent the two cells destined for the same output port from colliding and corrupting each other, either one of them has to be dropped or queued. Since a low cell loss rate is desired for ATM switches, cells are dropped only as a last resort. Buffers are incorporated into the design of an ATM switch to queue the cell that cannot be routed.

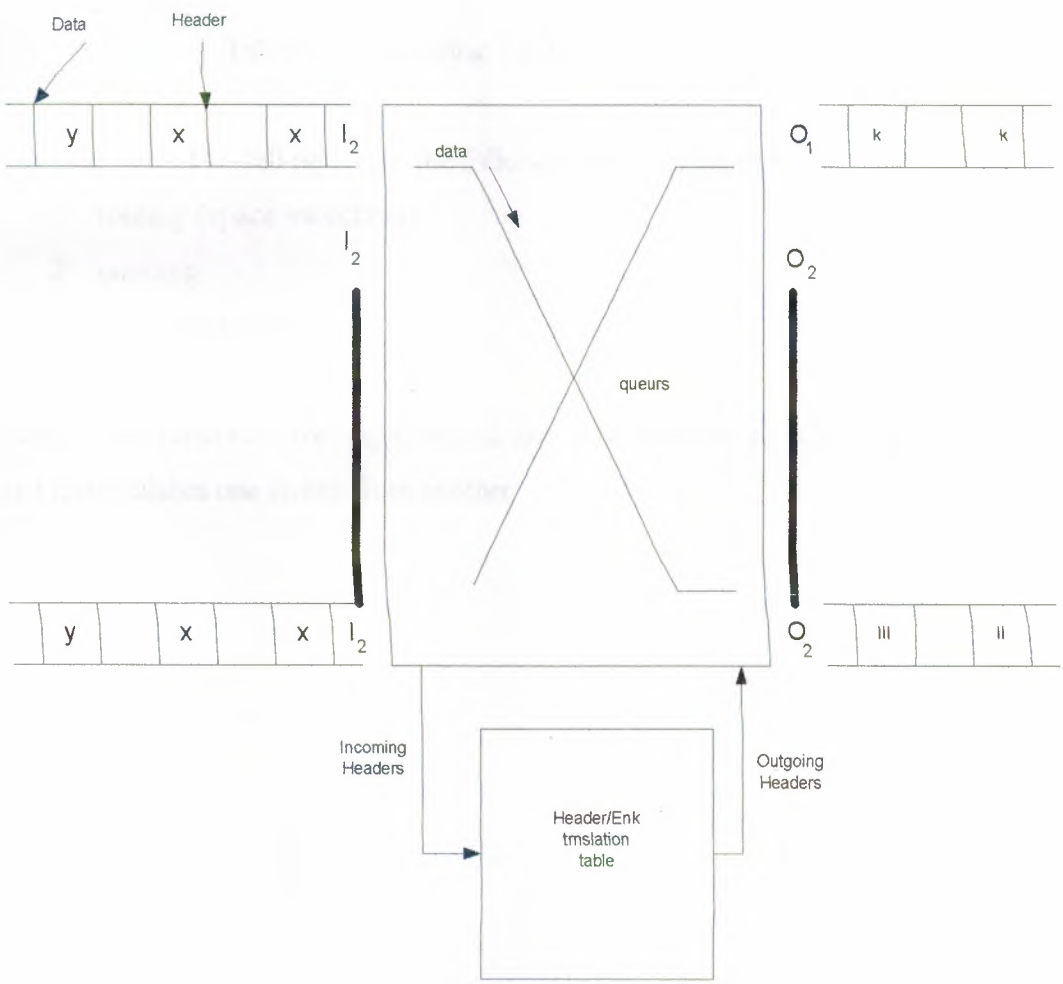

Figure 2.3.1: ATM Switch Principles

Incoming link	Header	Outgoing link	Header
I_1	X	O_1	K
	Y	O_4	M
	Z	O_2	I
I_2	X	O_1	N
	S	O_2	I
	Y	O_4	G

Table 2.1.2: Routing Table

To conclude, an ATM cell performs the following three functions:

1. routing (space switching)
2. queuing
3. header translation

The way these functions are implemented and where in the switch these functions are located distinguishes one switch from another.

Chapter III: Switching Requirements

Introduction

Broadband networks must be capable of transporting all kinds of information, ranging from voice to high quality video. These services have different requirements in terms of bit-rate (from a few KBPS up to hundreds of MBPS)$_5$ behavior in time (constant bit-rate or variable bit-rate), semantic transparency (cell loss rate and bit error rate) and time transparency (delay and delay jitter). These different service requirements have to be met by broadband ATM switches.

3.1 Information Rate

Since the information rates of the different services are very diverse, a large number of information rates must be supported in broadband switches. These rates range from a few KBPS (e.g. for voice) up to values of 150 MBPS (e.g. for: high definition television (HDTV)). If an ATM switch operates at 150 MBPS, it does not mean that the switch internally operates at 150 MBPS. Its internal operating speed may be lower or greater than 150 MBPS depending on its architecture. For example, switching can be realized over parallel wires resulting in a lower internal speed, or several 150 MBPS input ports can be multiplexed on a single link resulting in a higher internal speed.

3.2 Performance

The performance of classical STM switches is mainly characterized by the switch's throughput, connection blocking probability, bit error rate and switching delay.In an ATM environment, however, two other parameters are important, namely the cell loss or cell miss-insertion probability and the delay jitter, hi ATM switches, as in STM switches, the fabrication technology and dimension of the switch mainly determine the throughput and the bit error rate The effect of connection blocking, cell loss / miss-insertion probability and switching delay are different in ATM switches and are described below.

3.3 Connection blocking

Since ATM is connection oriented during the connection set-up phase, a logical connection needs to be established between a logical input port and output port. The probability of not finding enough resources between the input and output ports of the switch to guarantee the quality of all existing connections and the new connection is defined as connection blocking.

Some switch implementations do not have internal connections. This means that if enough resources (i.e. bandwidth and header values) are available on the input port and the output port of the switch, no new connection is blocked. Thus, a new connection is always accepted if enough resources are available on the external links, without an explicit check of the internal switch resources. Other switch implementations that have internal connections exhibit internal connection blocking. Internal connection blocking occurs when there are not enough resources for the new connection that can be allocated within the switch. Their dimension, the number of existing internal connections, and the load on those connections determine the blocking probability of internal connection blocking switches.

3.4 Cell Loss and Cell Miss-Insertion Probability

In ATM switches, it is possible for many cells to be destined for the same link (this link can be internal or external to the switch). This may cause more cells than the queue's capacity to compete for the queue's storage space, resulting in cells being dropped or lost. 28 The probability of losing a cell must be kept within limits to ensure a high semantic transparency (clear communication between the transmitting and receiving application) Typical values for cell loss probability for ATM switches range between 10 and 10^{-n}

Some switch architectures are designed in such a way that they do not suffer from cells competing for the same resource internally (e.g. a queue). These architectures do not lose ATM cells internally, but may lose cells only at their input and output ports. These switches are called internally non-blocking switches.

Sometimes cells in an ATM switch may be misrouted only to arrive erroneously on another logical connection. This occurs when the cell header gets corrupted during transmission and it goes undetected through the error checking stage. The probability of this cell miss-insertion must be kept within limits. Typical, cell miss-insertion values are a factor of 1000 times less than the cell loss rate.

3.5 Switching Delay

Switching delay is the time to transmit an ATM cell through the switch. Typical values for the switching delay of ATM switches range between 10 and 1000 micro-seconds with a jitter of few 100 micro-seconds or less, described in. Jitter is determined by the probability that the delay of the switch will exceed a certain value. For example a jitter of 100 microseconds for 10^{10} cells, means that the probability that the delay in the switch is larger than 100 microseconds is smaller than 10^{-10}

Chapter IV: GENERAL STRUCTURE OF AN ATM SWITCH

The basic architecture of a butterfly based ATM switch is shown in Figure 4.1, In general an ATM switch consists of two parts: switching elements and switching fabric. The switching element is the generic building block used to construct an ATM switching fabric. Switching elements are also called basic switching blocks A switching fabric is composed of identical basic switching elements interconnected in a specific topology. Thus, a switching fabric is defined when its topology is determined and when the switching elements are defined.

4.1 Switching Elements

ATM switching elements have a small number of input and output ports. Typical sizes for switching elements are 2 by 2 to 16 by 16. The operating speed of most switching elements ranges from 150 MBPS to 2.4 GBPS or greater. The size (number of input and output ports) and speed depend on the fabrication technology and the level of integration used, this section discusses the queuing problems of a switching element. If two ATM cells arrive at two input ports of the switching element for the same output during the duration of one cell, one of them has to be queued for a later cell time. Depending on the particular architecture of the switching element and the required internal speed, it is possible to queue cells at the input port, output port, or internally in the switching element There are some switching element architectures which have a fully non-blocking (per cell) switch fabric. Such architectures do not need to maintain internal queues. This contention-free characteristic guarantees that if all incoming cells of the switch architectures are destined for a different output port, no internal contention will arise. Switching elements which buffer cells destined for the same output port can *be* categorized into three categories determined by the physical location of the bufters : at the input, at the output, or central in the switching element.

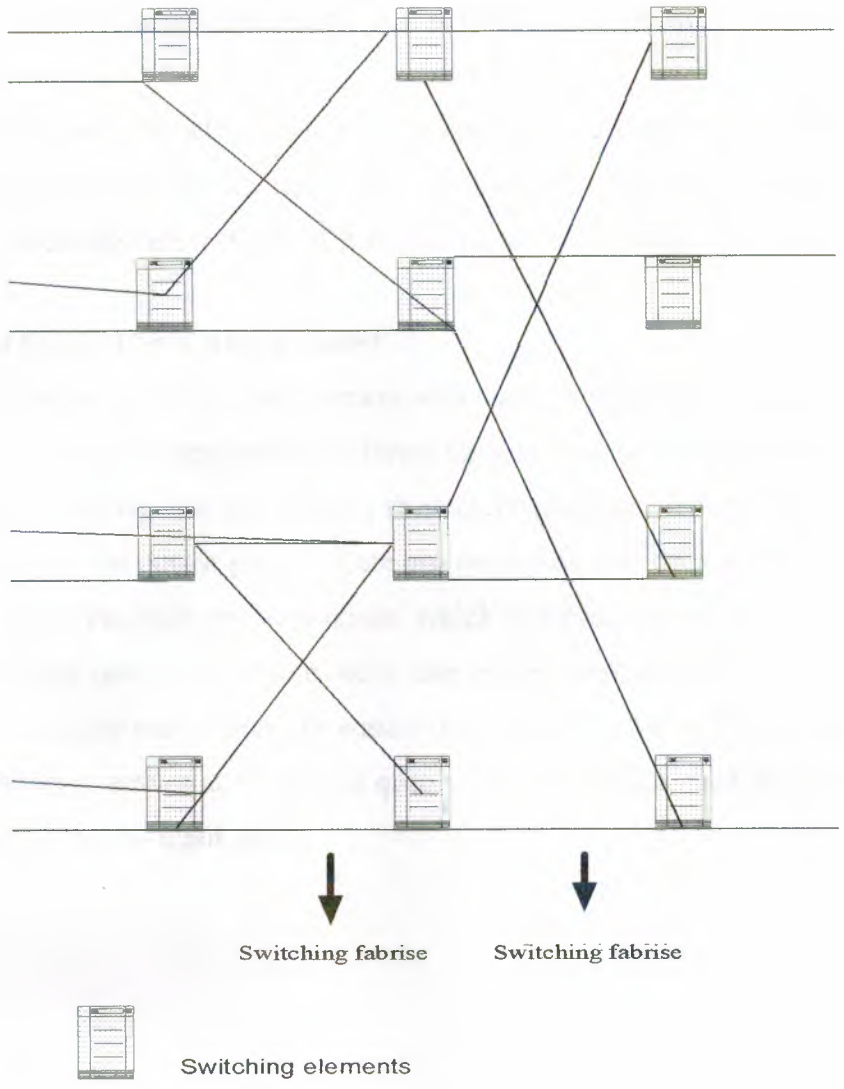

Figure 4.1.1 Basic Architecture of switches

4.2 Input Queued Switching Element

The block diagram of a switching element with input queuing is shown in Figure 4.2 In an input queued switching element all incoming cells are queued in a buffer at the input port. The arbitration logic determines which cell to serve in case of contention. The switching transfer medium then transfers the ATM cells from the input queues to the output port without internal contention. The arbitration logic which decides which input port to serve can range from very simple, such as round robin to quite complex, such as, taking into account the input buffer filling levels, delays of cells, etc. Input queued switching elements have a major disadvantage called head of the line (HOL) blocking. Suppose that the cell of input port i is selected to be transferred to output port p. If input

port j also has a cell destined for output port p, this cell will be stopped, together with all following cells.

Suppose that the second cell in the queue of input port j is destined to an output port q for which there is currently no cell waiting in the other queues. Then this cell cannot be served, since the cell in front of it in the queue is blocking the transfer.

4.3 Output Queued Switching Element

The block diagram of a switching element with output queuing is shown in Figure 4.3 In the output queued switches, cells of different input ports destined to the same output port are transferred during one cell time to their corresponding output port. Only a single cell is served at the output port. If there are more than one cells destined to the same output port, a contention problem arises, which is solved by having a separate queue for each output port. In principle, cells can arrive simultaneously at all input ports destined to a single output port. To ensure that no cells is lost in the switching transfer medium before it arrives at the output queue, the cell transfer must be performed at N times the speed of the input ports.

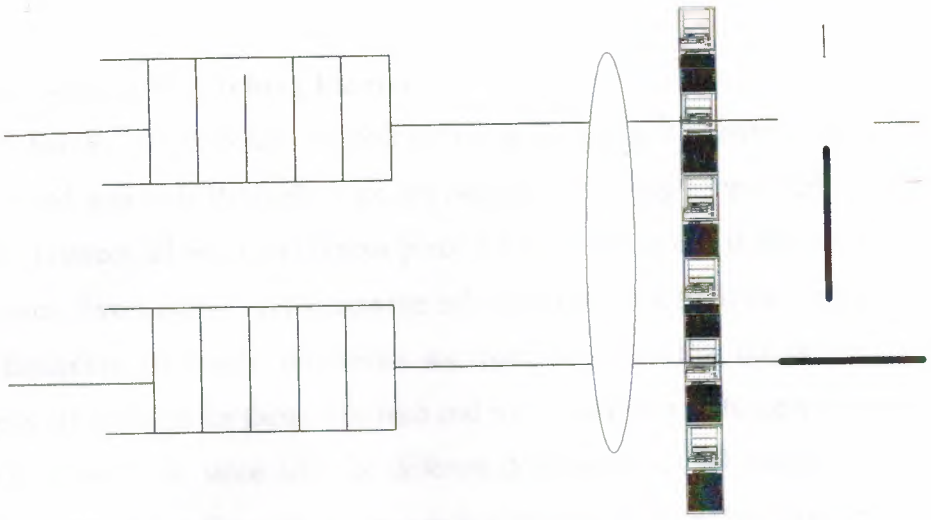

Figure 4.2.1 Switching Elements with Input Queue

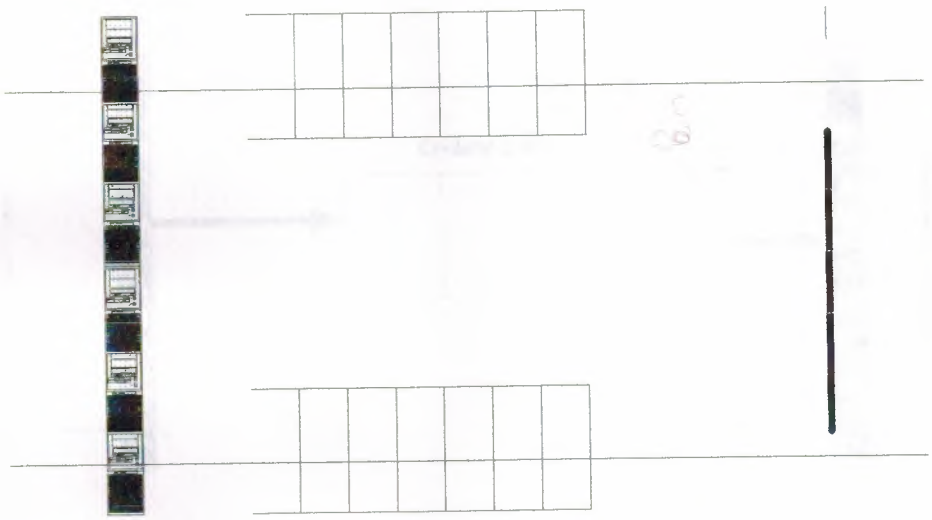

Figure 4.2.2: Switching Element with Output Queue

The system must be able to write N cells in the queues during one cell times, in the switching transfer medium, no arbitration logic is required. The control of the output queues is based on a simple first in first out (FIFO) discipline to ensure that cells remain in the correct sequence.

4.4 Central Queued Switching Element

The block diagram of a switching element with central queuing is shown in Figure 4.4. In the central queued approach, the buffers are not dedicated to a single input port or output port, but shared between all input and output ports. Each incoming cell is directly stored in the central queue. Every output port selects the cells destined for it from the central memory in a FIFO discipline. Internally, provisions are made to ensure that the output ports know which cells are destined for them. The read and write discipline ofthe central queue is not a simple FIFO discipline, since cells for different destinations are all merged in to a single queue. This means that the central memory is addressed in a random manner. The logical queues apply the FIFO discipline. Since cells can be written and read at random memory locations, a rather complex memory management system has to be used.

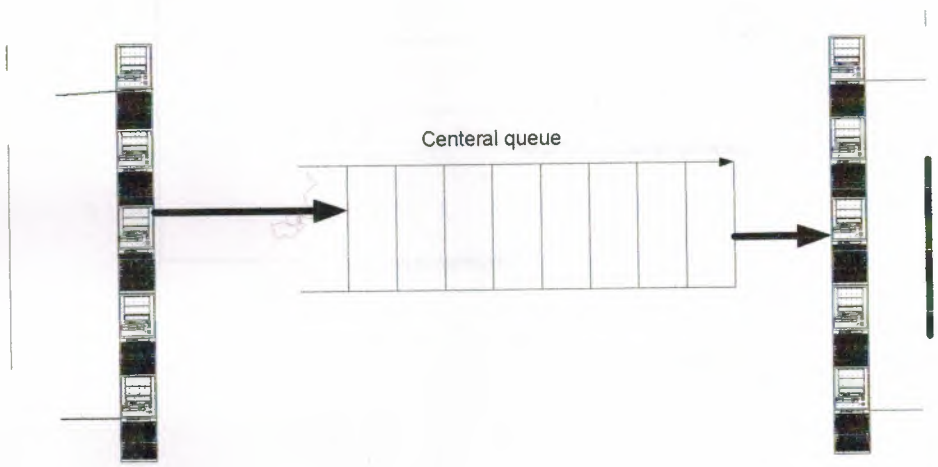

Figure 4.4.1: Switching Elements with Central Queue.

Chapter V: Switching Fabrics

Introduction

This section gives a general classification of switching networks . Figure 5.1 gives a classification of switching networks. Switching fabrics are categorized into two general categories depending on the number of stages. A switching fabric is also known as a switching network.

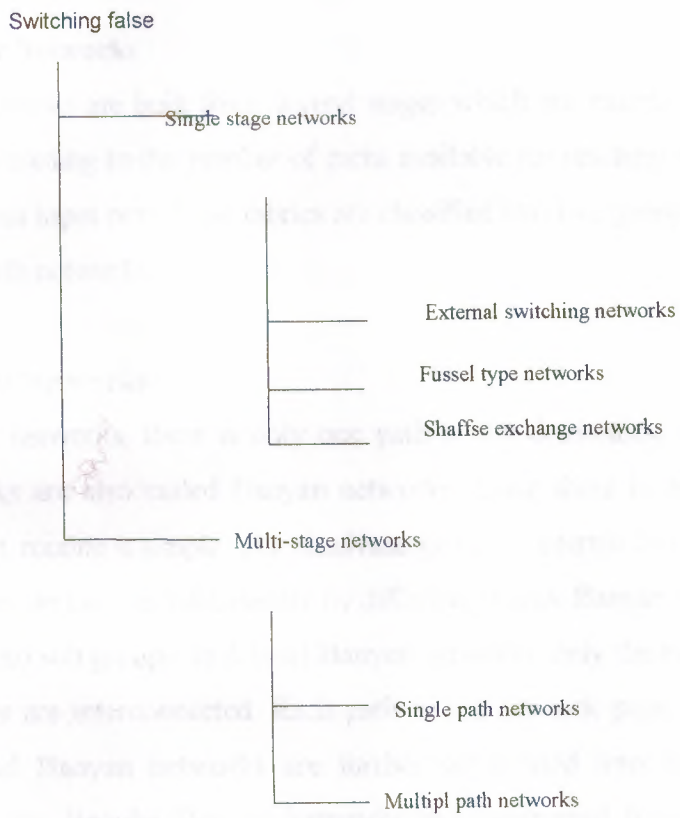

Figure 5.1.1: Switching Network

5.1 Single Stage Networks

A single stage network is characterized by a single stage of switching elements connected to the inputs and output ports of the switching network/ fabric. Categories of single stage fabrics are extended switching matrices, funnel type networks and shuffle-exchange networks. Single stage fabrics are useful for constructing smaller switches. With the increase in the number inputs, the number of switching elements also has to be increased, which in turn increases the delay in switching cells. To construct switches with 128 or more input / output ports, multi-stage fabrics are preferred.

5.2 Multi-Stage Networks

Multi-stage networks are built from several stages which are interconnected in a certain link pattern. According to the number of paths available for reaching a destination output port from a given input port, these fabrics are classified into two groups called single-path and multiple-path networks.

5.3 Single Path Networks

In single path networks, there is only one path to the destination from a given input. These networks are also called Banyan networks. Since there is only one path to the destination port, routing is simple. The disadvantage is that internal blocking can occur as an internal link can be used simultaneously by different groups. Banyan networks can further be classified into sub groups. In L level Banyan networks, only the switching elements of adjacent stages are interconnected. Each path in the network passes through exactly L stages. L level Banyan networks are further subdivided into regular and irregular Banyan networks. Regular Banyan Networks are constructed from identical switching elements, whereas irregular Banyan36 networks use different types of switching elements. Regular Banyan networks have an advantage that they can be implemented easily because of they are constructed from identical elements.

5.4 Multiple Path Networks

In multiple-path networks, a multiplicity of alternative paths exists to the destination output from a given input port. This property has the advantage that internal blocking can be reduced or avoided altogether In most multiple-path networks, the internal path is determined during the connection setup phase. All cells on the connection *use* the same internal path. As all cells follow the same path, switching elements can uses a FIFO policy without worrying about cell sequence integrity.

Multiple path networks are further subdivided into folded and unfolded networks, tn folded networks, all inputs and outputs are located at the same side of the switching network and the network's internal links operate in both directions. Folded networks have the advantage mat the paths are short. For example, if the input and output ports are connected to the same switching element, cells can be reflected at the switching element and need not be passes to the last stage. The number of switching elements that the cells of a connection have to pass through depends on the location of the input and output lines. In unfolded networks, the inputs are located on one side and the outputs on title opposite side of the network. Internal links are unidirectional and all cells have to pass through the same number of switching elements.

Multiple-path networks can also be realized by using several planes of Banyan networks in parallel. This is called vertical stacking. All cells belonging to the same connection pass through the same plane. The plane and the path within the plane are determined during the connection setup phase. An incoming cell is switched to its appropriate plane by a distribution unit located at each input port.

5.5 Cell Header Processing in Switching Fabrics

Switching fabrics need to perform VPI / VCI translation and route the cells to the correct output port. In order to fulfill these tasks, two approaches can be used

1. Self-routing principle
2. Table-controlled routing principle

Studies have been made to decide which principle is superior. For large multi-stage *switching networks the self-routing principle is preferred because it is superior in terms of* control complexity and failure behavior. The need for a higher internal bit rate because of the cell extension in self-routing networks is not critical.

5.6 Self Routing Switching Elements

When using self-routing elements, VPI/VCI translation only has to be performed at the input port of the switching network. After the translation, a switching network internal header is added to the cell. This header precedes the cell header. Because of the cell header extension an increased internal network speed has to be maintained. In a network with k stages, the internal header is subdivided into *k* sub-fields. Sub-field /', contains the destination output port number of the switching element in stage / of the switching fabric. Figure 5.2 shows the cell header processing in a switching network built up of self-routing switching elements Figure 5.3 shows a generic block diagram of a self-routing switching element.

It contains a central memory with logical output queues and is controlled by the routing information included in the internal cell header. In order to keep the buffer access speed within a realistic range a wide parallel memory interface is used requiring serial-to-parallel conversion at the input and parallel-to-serial conversion at the output.

5.7 Table Controlled Switching Elements

in table controlled switching elements, the VPI / VCI of the cell header is translated into a new identifier in each switching element. Therefore, the cell length does not need to be altered.

Figure 5.4 shows the header processing in a switching network which consists of table controlled switching elements. The contents of the table are updated during the connection setup phase. Each table entry consists of the new VPI / VCI and the number of the appropriate output link.

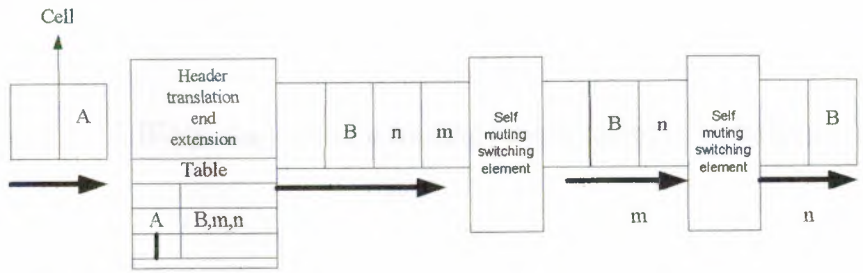

Figure 5.2.1 Cell Header Processing

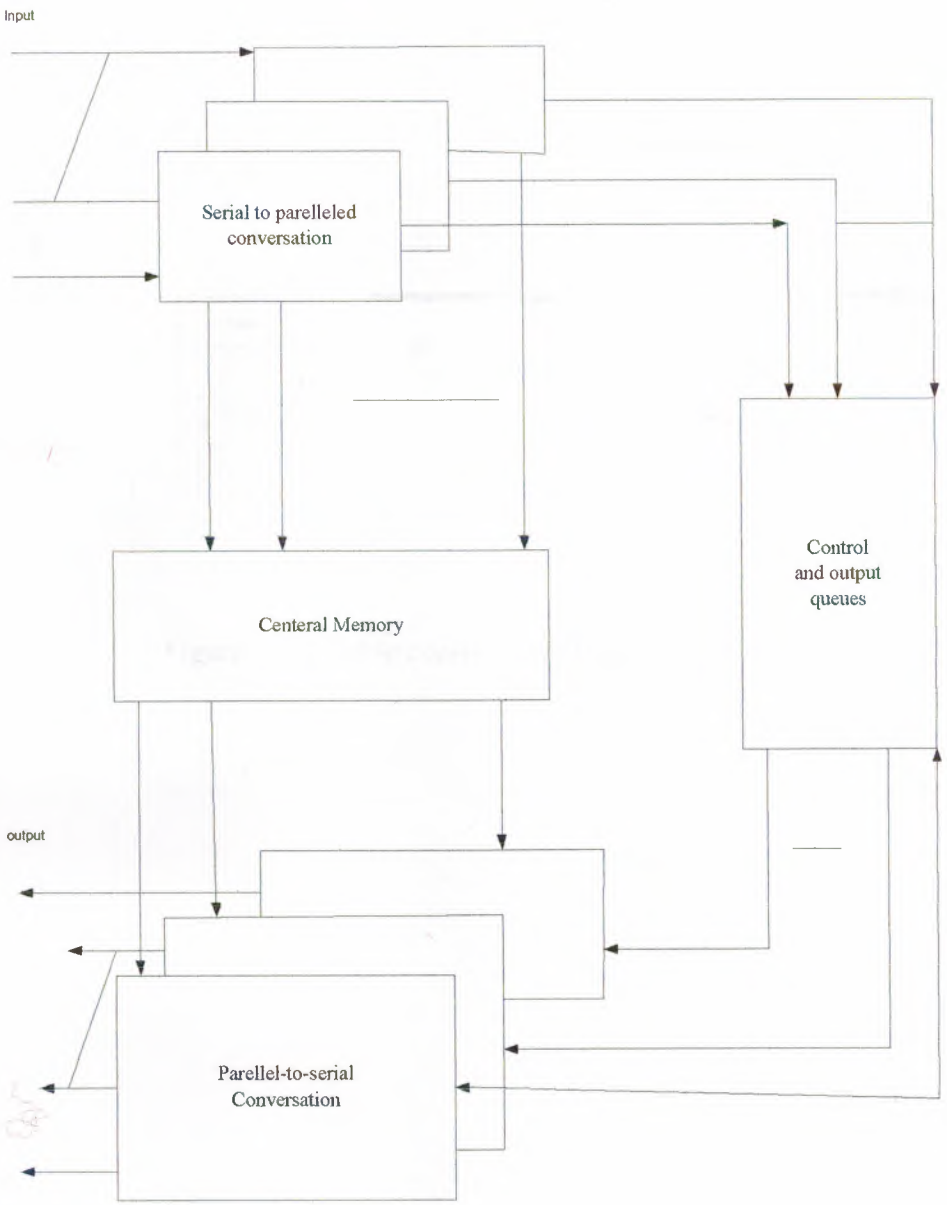

Figure 5.3.1 Block diagram of a routing central memory switching element

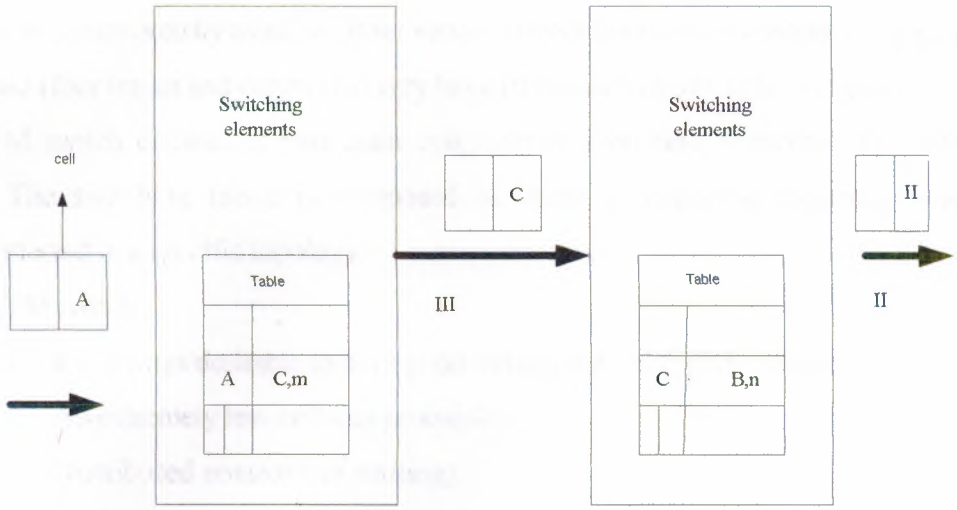

Figure 5.4.1 Table control switching element

Summary and Conclusion

The small fixed cell size and a limited functionality cell header have an important influence on the definition of an optimal ATM switching architecture. A number of ATM switches are commercially available from various telecommunication companies ranging from very small (four inputs and outputs) to very large (thousands of inputs and outputs).

An ATM switch consists of two main components; switching elements and a switching fabric. The switching fabric is composed of identical switching elements, which are interconnected in a specific topology.

In an ATM switch:

1. It is always desirable to have good throughput-delay performance.
2. An extremely low cell loss probability.
3. Distributed control (for routing).
4. Preservation of cell sequencing.
5. Ability to easily incorporate priority.
6. Multicast function.

In practice, there is a tradeoff between these desirable features and cost

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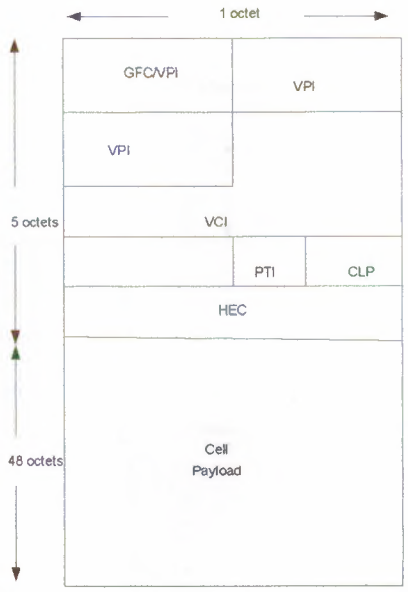
[4] http://www cs.umbc.edu.

[5] http://www.atmforum.com

[6] http:// www.mstm.okstate.edu [6] http://www.cisco.com

Appendix

ATM Cell Format



1. Uni

-Genetic Flow Control (GFC)~ not used

-Virtual Path/Channel Identifier (VPI/VCI) Payload

-Type Identifier (PTI)

2. User data maintence flow
3. Congestion experiences
4. End of message (for AAL/S)

-Cell Loss Priority (CLP)

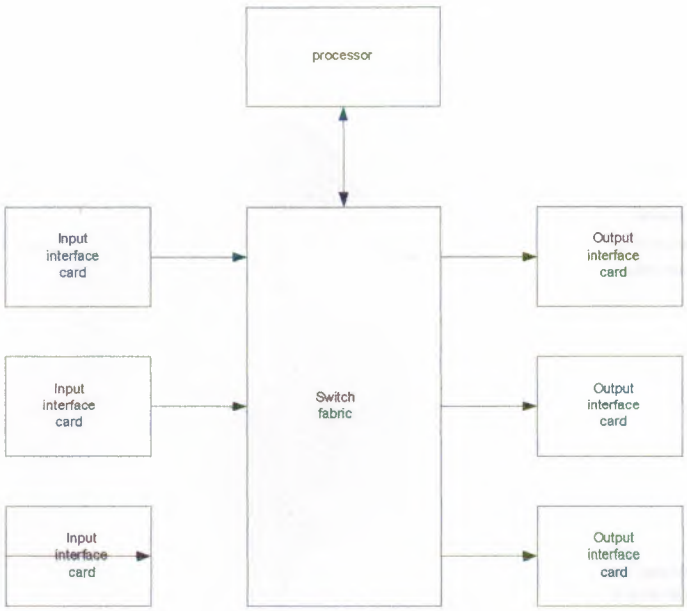
-Header Error Control (HEC)

5. NNI

-No GHEC field larger VPI field instead

-Larger VPI field for making

Inside a Switch



Input interface card:

1. pysical layer processing
2. memory buffers to hold incoming packe

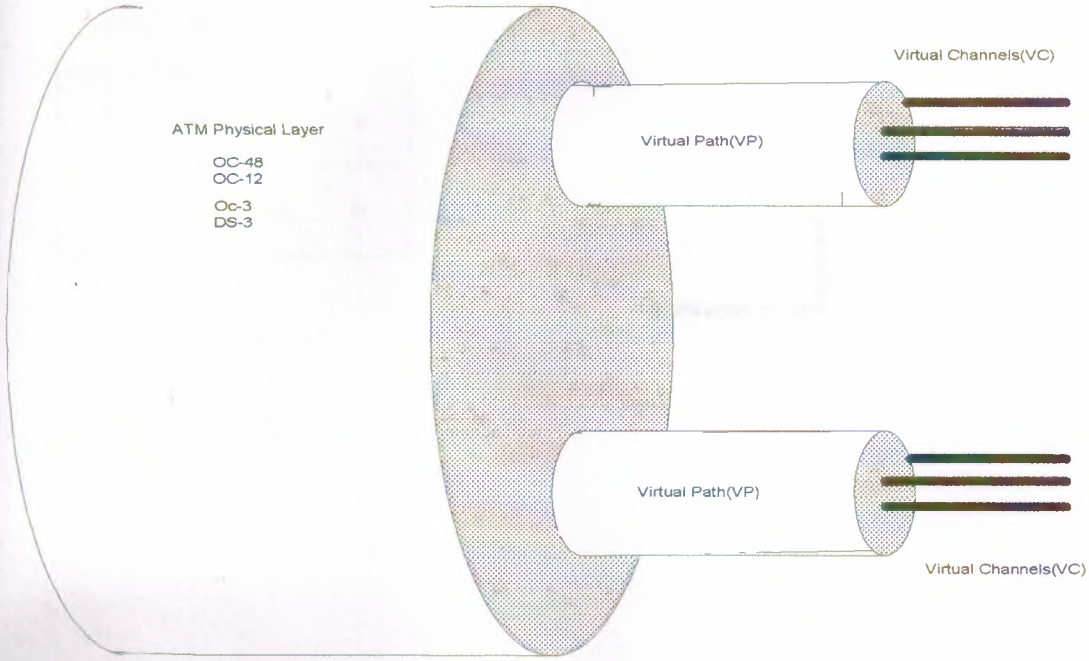
Switch fabric:

3. to move packets hold outgoing packets
4. physical layer processing

Control processor: routing updates supervisory (management) functions

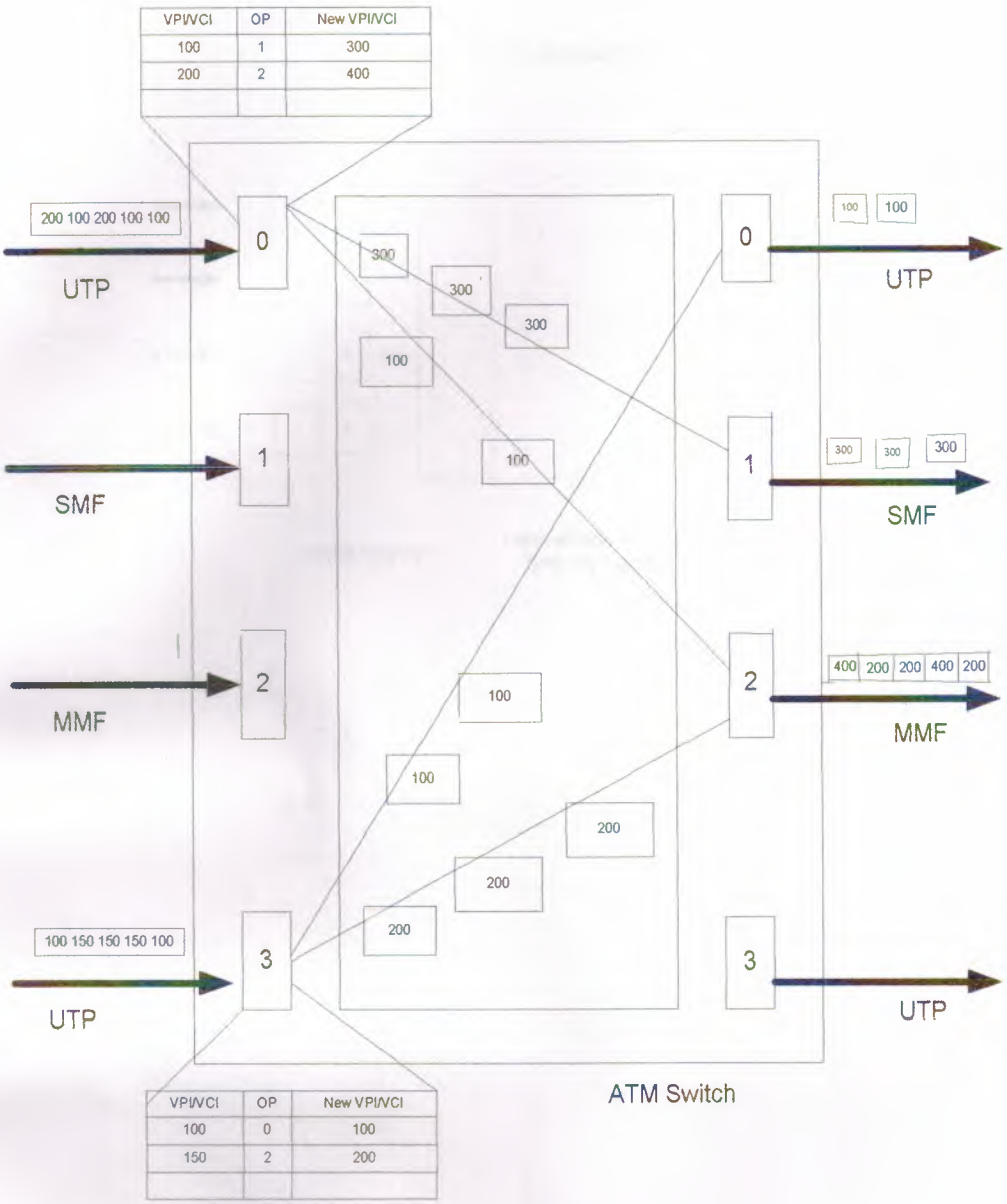
5. will typiclly not tough the packets begin switched

Adressing: Virtual path and virtual channel



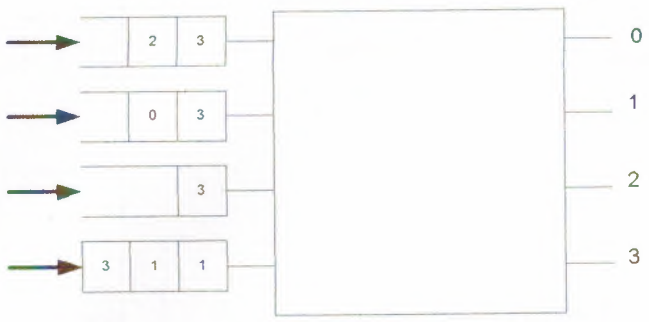
1. VP is simply a bundle of VCs
2. ATM switch switches can individual VC or VP

Figure 2.1 : ATM Switch Operations



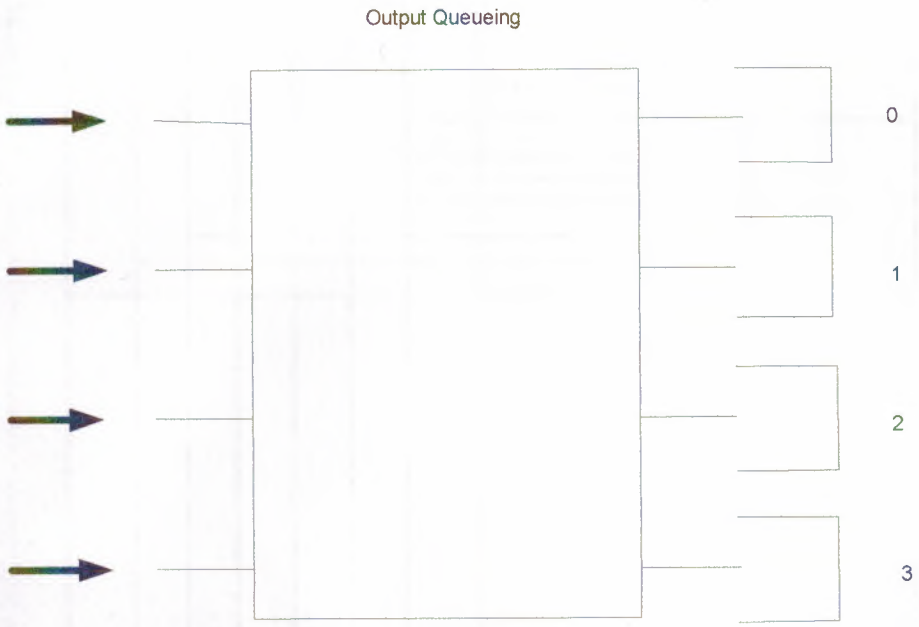
Cell Multiplexing and Cell switching Examples

Input Queuueing

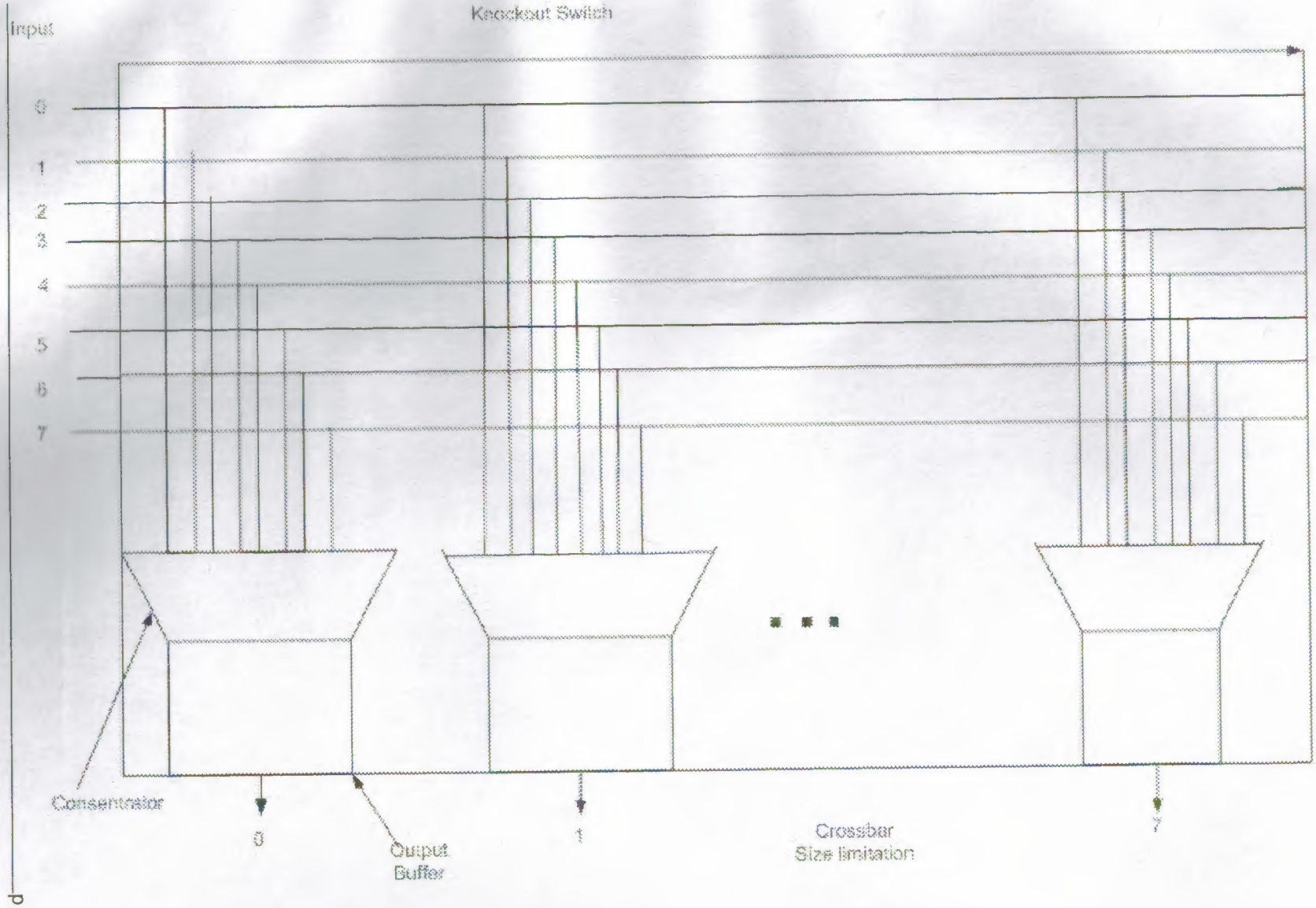


Input Queues

Head-of-line blocking
58% throughput



100% Throughput
N-fold increase in cyle time
for NxN switch


Knockout Switch
Input
0
1
2
3
4
5
6
7
p
Concentrator
0
1
Output
Buffer
Crossbar
Size limitation