# NEAR EAST UNIVERSITY 

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## Department of Electrical and Electronic Engineering

## AC ELECTRONICS MOTOR CONTROL

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Student:
Mustafa AI-Far (20010692)

Supervisor:
Mr. Özgür Özerdem


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## IN THE NAME OF ALLAH, MOST GRACIOUS, MOST MERCIFUL

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#### Abstract

ABSRTACT

Electronic systems and controls have gained wide acceptance in power technology; consequently, it has become almost indispensable to know something about control power electronics in motor AC system.

We can explain in simple terms the behavior of a large number of electronic power circuit, including those most commonly used today.

As far as electronic devises are concerned, we will cover diodes and thyristors. They are found in all electronic systems involve the conversion of AC power to DC power and vice versa. We then go on to discuss the application of more recent devises such as gate turn-off thyristors ( GTOs ), bipolar junction transistors (BJTs), metal oxide semiconductor field effect transistors ( power MOSFETs), and insulated gate bipolar transistors (IGBTs). Their action on a circuit is basically no different from that of a thyristors and its associated switching circuitry. In power electronics all these devises act basically as high-speed swatches; so much so, that much of power electronics can be explained by the opening and closing of circuit at precise instants of time. However, we should not conclude that circuits containing these components and devises are simple they are not, but their behavior can be understood without having an extensive background in semiconductor theory.


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## INTRODUCTION

The electronic controls of D.C enables use to obtain high efficiency at all torques and speed. Full 4-quadrant control is possible to meet precise high-speed industrial standards. We find that squirrel-cage and wound-rotor induction motor, as well as Synchronous motors, lend themselves well to electronic control. Whereas de machines are controlled by varying the voltage and current, AC machines are controlled by varying the voltage and frequency. Now, we may ask, if dc machines do such out standing job, why do we also use AC machines?

There are several reasons:

- AC machines have no commutators and brushes; consequently, they require less maintenance.
- AC machines cost less (and weigh less) than DC machines.
- AC machines are more rugged and work better in hostile environment.
- AC machines can operate at much higher voltages: up to 25 kV . DC machines are limited to about 1000 V .
- AC machines can be built in much larger size: up to 50000 kW . DC machines are limited to about 2000 kW .
- AC machine can run at speed up to $100000 \mathrm{r} / \mathrm{min}$, whereas large DC machine are limited to about $2000 \mathrm{r} / \mathrm{min}$.


## CHAPTER 1 <br> NOISELESS A.C. CONTROL

### 1.1 Overview

Controlling an a.c. induction motor by the technique of sine wave-weighted pulse-width modulation (PWM) switching gives the benefits of smooth torque at low speeds, and also complete speed control from zero up to the nominal rated speed of the motor, with only small additional motor losses.

Traditional power switches such as thyristors need switching frequencies in the audible range, typically between 400 and 1500 Hz . In industrial environments, the small amount of acoustic noise produced by the motor with this type of control can be regarded as insignificant. By contrast, however, the same amount of noise in a domestic or office application, such as speed control of a ventilation fan, might prove to be unacceptable.

Now, however, with the advent of power MOSFETs, three-phase PWM inverters operating at ultrasonic frequencies can be designed. A three-phase motor usually makes even less noise when being driven from such a system than when being run directly from the mains because the PWM synthesis generates a purer sine wave than is normally obtainable from the mains.

The carrier frequency is generally about 20 kHz and so it is far removed from the modulation frequency, which is typically less than 50 Hz , making it economic to use a low-pass filter between the inverter and the motor. By removing the carrier frequency and its sidebands and harmonics, the waveform delivered via the motor leads can be made almost perfectly sinusoidal. RFI radiated by the motor leads, or conducted by the winding-to-frame capacitance of the motor, is therefore almost entirely eliminated. Furthermore, because of the high carrier frequency, it is possible to drive motors which are designed for frequencies higher than the mains, such as 400 Hz aircraft motors.

This section describes a three-phase a.c. motor control system which is powered from the single-phase a.c. mains. It is capable of controlling a motor with up to 1 kW of shaft
output power. Before details are given, the general principles of PWM motor control are outlined.

### 1.2 Principles of Pulse-Width Modulation

Pulse-width modulation (PWM) is the technique of using switching devices to produce the effect of a continuously varying analogue signal; this PWM conversion generally has very high electrical efficiency. In controlling either a three-phase synchronous motor or a three-phase induction motor it is desirable to create three perfectly sinusoidal current waveforms in the motor windings, with relative phase displacements of $120^{\circ}$. The production of sine wave power via a linear amplifier system would have low efficiency, at best $64 \%$. If instead of the linear circuitry, fast electronic switching devices are used, and then the efficiency can be greater than $95 \%$, depending on the characteristics of the semiconductor power switch.


Figure1.1 Half-bridge switching circuit


Figure1.2 Waveforms in PWM inverter
(a) Un modulated carrier
(b) Modulated carrier
(c) Current in inductive load

The half-bridge switching circuit in Fig. 1.1 is given as an example: the switches can be any suitable switching semiconductors. If these two switches are turned on alternately for equal times, then the voltage waveform across the load is as shown in Fig.1.2a. The mean value of this waveform, averaged over one switching cycle is 0 . This square wave with a constant $50 \%$ duty ratio is known as the 'carrier' frequency. The waveform in Fig. 1.2b shows the effect of a slow variation or 'modulation' of the duty ratio; the mean voltage varies with the duty ratio. The waveform of the resultant load current depends on the impedance of the load $Z$. If $Z$ is mainly resistive, then the - waveform of the current will closely follow that of the modulated square wave. If, however, Z is largely inductive, as with a motor winding or a filter choke, then the switching square wave will be integrated by the inductor. The result is a load current waveform that depends mainly on the modulation of the duty ratio.

If the duty ratio is varied sinusoid ally in time, then the current in an inductive load has the form of a sine wave at the modulation frequency, lagging in phase, and carrying ripple at the switching frequency as shown in Fig.1.2c. The amplitude of the current can
be adjusted by controlling the depth of modulation, that is, the deviation of the duty ratio from $50 \%$. For example, a sine wave PWM signal which varies from $5 \%$ to $95 \%$, giving $90 \%$ modulation, will produce a current nine times greater than that produced by a signal which varies only from $45 \%$ to $55 \%$, giving only $10 \%$ modulation.

For three-phase a.c. motor control, three such waveforms are required, necessitating three pairs of switches like those shown in Fig.1.1, connected in a three-phase bridge. The inductance required to integrate the waveform can usually be provided by the inductance of the stator windings of the motor, although in some instances it might be provided by the inductance of a separate low-pass filter. The modulations in the three switching waveforms must be maintained at a constant relative phase difference of $120^{\circ}$, so as to maintain motor current sine waves which are them selves at a constant $120^{\circ}$ phase difference. The modulation depth must be varied with the modulation frequency so as to keep the magnetic flux in the motor at approximately the design level.

In practice, the frequency of the modulation is usually between zero and 50 Hz . The switching frequency depends on the type of power device that is to be used: until recently, the only devices available were power thyristors or the relatively slow bipolar transistors, and therefore the switching frequency was limited to a maximum of about 1 kHz . With thyristors, this frequency limit was set by the need to provide forced commutation of the thyristors by an external commutation circuit using an additional thyristors, a diode, a capacitor, and an inductor, in a process that takes at least 40 s . With transistors, the switching frequency was limited by their switching frequency and their long storage times.

- In this earlier type of control circuit, therefore, the ratio of carrier frequency to modulation frequency was only about 20:1. Under these conditions the exact duty-ratios and carrier frequencies had to be selected so as to avoid all sub-harmonic torques, that is, torque components at frequencies lower than the modulation frequency.

This was done by synchronizing the carrier to a selected multiple of the fundamental frequency; the HEF4752V, an excellent IC purpose-designed for a.c. motor control, uses this particular approach.

The 1 kHz technique is still extremely useful for control of large motors because whenever shaft output powers of more than a few kW are required, three-phase mains input must be used, and there are, as yet, few available switching devices with combined high voltage rating, current rating, and switching speed. However, using MOSFETs with switching times of much less than $1 \square \mathrm{~s}$, the carrier frequency can be raised to the ultrasonic region, that is, to 20 kHz or more. There are obvious system benefits with this higher frequency, but there are also several aspects of PWM waveform generation that become easier. It is possible to use a fixed carrier frequency because the sub-harmonics that are produced as a result of the non-synchronization of the carrier frequency with a multiple of the fundamental are insignificant when the ratio of the carrier frequency to the fundamental frequency is typically about $400: 1$. Fig. 3 20 kHz AC motor controller


Figure 1.320 kHz AC motor controller

To maintain good waveform balance, and thus avoid any D.C. in the motor, and therefore also avoid parasitic torques, A digital waveform generation technique is appropriate. The waveform can be stored as a 'look-up' table of numbers representing
the sine wave. To generate the three phases, this table can be read at three points that have the correct $120^{\circ}$ phase relationship. The numbers taken from the table represent the duty ratios corresponding to $100 \%$ modulation: these numbers can then be scaled down by multiplication or some equivalent technique to give the correct duty-ratio numbers for the modulation depth required.

The speed of the motor is controlled by the rate at which the reading pointers scan the look-up table and this can be as slow as desired. If the pointers are stationary, then the system will be 'frozen' at a particular point on the three-phase sine wave waveform, giving the possibility of obtaining static torque from a synchronous motor at zero speed. The rate at which the numbers are produced by this read-out process from the look-up table is constant and determines the carrier frequency. To convert these three simultaneous parallel digital numbers into time lengths for pulses, three digital counters are needed. The counters can be designed to give double-edged modulation, such that both the leading edge and the trailing edge of each pulse move with respect to the un modulated carrier.

The line-to-line voltage across the load will have most of its ripple at a frequency of twice the switching frequency, and will have a spectrum with minimum even harmonics and no significant component below twice the switching frequency. Motor ripple current is therefore low and motor losses are reduced.

There is a further advantage to be obtained from the high ratio of carrier to modulation frequency: by adding a small amount of modulation at the third harmonic frequency of the basic fundamental modulation frequency, the maximum line-to-line output voltage obtainable from the inverter can be increased, for the following reason. The effect of the - third harmonic on the output voltage of each phase is to flatten the top of the waveform, thus allowing a higher amplitude of fundamental while still reaching a peak modulation of $100 \%$. When the difference voltage between any two phases is measured, the third harmonic terms cancel, leaving a pure sine wave at the fundamental frequency. This allows the inverter output to deliver the same voltage as the mains input without any significant distortion, and thus to reduce insertion losses to virtually zero.

### 1.3 Practical system

The principles outlined above are applied to a typical system shown in Fig.1.3. The incoming a.c. mains is rectified and smoothed to produce about 300 V and this is fed to the three-phase inverter via a current-sensing circuit. The inverter chops the D.C. to give 300 V peak-to-peak PWM waves at 20 kHz , each having low-frequency modulation of its mark-space ratio. The output of the inverter is filtered to remove the 20 kHz carrier frequency, and the resultant sine waves are fed to the a.c. motor.


Figure 1.4 Waveform generator circuit

The six switches in the inverter are under the command of a waveform-generation circuit which determines the conduction time of each switch. Because the control terminals of the six switches are not at the same potential, the outputs of the waveformgeneration circuits must be isolated and buffered. A low-voltage power supply feeds the
signal processing circuit, and a further low-voltage power supply drives a switch-mode isolating stage to provide floating power supplies to the gate drive circuits.

### 1.4 Signal processing

Fig. 1.4 shows a block diagram of the circuit which generates the PWM control signals for the inverter. The input to the system is a speed-demand voltage and this is also used for setting the required direction of rotation: the analogue speed signal is then separated from the digital direction signal. The speed-demand voltage sets the frequency of the voltage-controlled oscillator (VCO). Information to determine the modulation depth is derived from the speed-control signal by a simple non-linear circuit and is then converted by an analogue-to-digital converter into an 8-bit parallel digital signal.

The output signals of the microcomputer are in the form of three 8 -bit parallel numbers: each representing the duty-ratio for the next $50 \mu \mathrm{~s}$ switching cycle for one pair of inverter switches, on a scale which represents $0 \%$ to $100 \%$ on-time for the upper switch and therefore also $100 \%$ to $0 \%$ on-time for the complementary lower switch.

A dedicated logic circuit applies these three numbers from the microcomputer to digital counters and converts each number to a pair of pulse-widths. The two signals produced for each phase are complementary except for a small 'under lap' delay. This delay is necessary to ensure that the switch being turned off recovers its blocking voltage before its partner is turned on, thus preventing 'shoot-through'.


Figure 1.5 DC link, low voltage and floating power supplies

Other inputs to the microcomputer are the on/off switches, the motor direction logic signal, and the current-sensing signal. Each input triggers a processor interrupt, causing the appropriate action to be taken. The STOP switch and the over current sense signals have the same effect, that of causing the microcomputer to instruct all six power switches in the inverter to turn off. The RUN switch causes the microcomputer to start producing output pulses. Any change in the direction signal first stops the microcomputer which then determines the new direction of rotation and adjusts its output phase rotation accordingly.

### 1.5 D.C. link and power supplies

The D.C. link and the low-voltage power supplies for the system are shown in Fig.1.5. The high voltage D.C. supply for the inverter is derived from a mains-fed bridge rectifier with a smoothing capacitor; the capacitor conducts both the 100 Hzripple from the rectified single-phase mains, and also the inverter switching ripple. A resistor, or alternatively a thermistor, limits the peak current in the rectifier while the capacitor is being charged initially. This resistor is shorted out by a relay after a time delay, so that the resistor does not dissipate power while the motor is running. As a safety measure, a second resistor discharges the D.C. link capacitor when the mains current is removed.

One of the D.C. link lines carries low-value resistor to sense the D.C. link current. A simple opto-isolation circuit transmits a D.C. link current overload signal back to the signal processing circuit.

The logic circuitry of the waveform generator is powered conventionally by a 50 Hz mains transformer, bridge rectifier, and smoothing capacitor. The transformer has two secondary windings; the second one provides power to a switched-mode power supply (SMPS), in which there is a switching transistor driven at about 60 kHz to switch power through isolating transformers. Rectifying the a.c. outputs from the isolating transformers provides floating power supplies for the inverter gate drive circuits. As will be seen below, one supply is needed for the three 'lower' power switches (connected to a common D.C. link negative line), but three separate power supplies are needed for the three 'upper' switches (connected to the three inverter outputs).

Thus four isolating transformers are required for the gate supply circuits. For low power systems the gate supplies can be derived directly from the d.c. link without excessive loss. To prevent spurious turn-on of any inverter switch during the start-up process, the floating power supply to the lower three gate-drive circuits is connected only after a delay. The same delay is used for this as is used for the D.C. link charging-resistor bypass switch.


Figure 1.6 Signal isolation, gate drive, inverter and filter (one phase of three)

### 1.6 Signal isolation, gate drive, and inverter

The most important part of the system is the power inverter and it is the use of MOSFETs, with their short switching times, which makes it possible for the inverter to switch at 20 kHz . It is in the area of the drive circuits to the power switches that using MOSFETs gives a saving in the number of components needed. Driving MOSFETs is relatively easy: the total power needed is very small because all that must be provided is the capability to charge and discharge
the gate-source capacitance (typically between 1 and 2 nF ) by a few volts in a short time (less than 100 ns ). This ensures that the quality of the waveform is not degraded, and that switching losses are minimized.

In this circuit the six pulse outputs from the dedicated logic part of the waveform generator section are coupled to the MOSFET gate driver stages via pulse transformers. (see Fig.1.6). Each gate drive circuit is powered from one of the four floating power supplies described above. The three 'lower' stages share a common power supply, as the source terminals of the three 'lower' MOSFETs are all at the same potential. Each of the three 'upper' stages has its own floating power supply. The isolated signals are coupled to the gate terminals of the six MOSFETs by small amplifiers capable of delivering a few amperes peak current for a short time. Alternative gate driver circuits may use level shifting devices or opto-couplers. (Refer to "Power MOSFET Gate Drive Circuits" for further details.)

It will be seen from Fig. 1.6 that each MOSFET has two associated diodes. These are necessary because the MOSFETs have built-in anti-parallel diodes with relatively long reverse-recovery times. If these internal diodes were allowed to conduct, then whenever load current commutated from a diode to the opposite MOSFET, a large current would be drawn from the d.c. supply for the duration of the diode reverse-recovery time. This would greatly increase the dissipation in the inverter. To avoid this, an external fast epitaxial diode is connected in anti-parallel with the MOSFET. Because the internal diode of the MOSFET has a very low forward voltage drop, a second low-voltage epitaxial diode must be connected in series with each MOSFET to prevent the internal diode from conducting at all. Thus, whenever the MOSFET is reverse-biased, it is the external anti-parallel diode which conducts, rather than the internal one. FREDFETs have internal diodes which are much faster than those of MOSFETs, opening the way for a further cost-saving by omitting the twelve diodes from the 3-phase inverter.

### 1.7 Output low-pass filter

For conventional, lower frequency inverters the size, weight and cost of output filter stages have held back their proliferation. An advantage of the constant high carrier frequency is that a small, economical low-pass filter can be designed to remove the
carrier from the inverter output waveform. Compared with low frequency systems the filter component has been reduced by an order of magnitude, and can often be eliminated completely. In unfiltered systems cable screening becomes an important issue although on balance the increased cost of screening is less than the cost and weight of filter components. A typical filter arrangement was shown in Fig.1.6. As an example, for a 50 Hz motor-drive the filter would be designed with a corner-frequency of 100 Hz , so that the attenuation at 20 kHz would be about 46 dB . The carrier frequency component superimposed on the output sine wave would therefore be only a few mV in 200 Vrms . Fig. 1.6 shows the relative spectral characteristics of different types of inverter switching strategies.

There are two main advantages in supplying the motor with pure sine wave power. First, the motor losses are small, because there is no rms motor current at the switching frequency, and second, there is less radio-frequency interference (RFI), because the switching frequency current components circulate entirely within the inverter and filter and do not reach the outside world.

### 1.8 Advantages of a 20 kHz system

- Controller and motor are acoustically quiet.
- PWM waveform is simple and thus easy to generate.
- Output filter for removal of carrier is economic.
- RFI is low because of output filter.
- No snubbers are required on power devices.
- High efficiency is easily obtainable AND -No insertion loss.


## CHAPTER 2

## THE EFFECT OF MOSFET

### 2.1 The Effect of a MOSFET's Peak to Average Current Rating On Inverter Efficiency

The control of induction motors using a synthesized sine wave generated using pulse width modulation (PWM) control is becoming increasingly popular. The peak current requirement of switches used for the inverter bridge is based on the maximum current when the output is short circuited. The over current during a short circuit fault is limited by an inductor connected in series with the switches. There is therefore a trade off between the peaks current carrying capability of the switch and the size of the inductor. It is demonstrated in this note that the efficiency of the circuit during normal operation of the inverter is affected by the size of this choke. The ratio of peak to average current carrying capability of Philips PowerMOS is typically about four. This compares favorably with the typical ratio of Insulated Gate Bipolar Transistors (IGBTs) which is about three.

A simplified diagram of the inverter and the windings of the induction motor is shown in Fig.2.1.The MOSFET sare driven with a PWM signal as shown in Fig.2.2. The voltages at the outputs of each leg of the inverter are smoothed using a low pass filter and the inductance of the motor windings. The system has the following advantages; it uses an induction motor which is relatively cheap and maintenance free and it has the facility for 0 to $100 \%$ speed control. The near perfect sine wave generated by the PWM technique produce a smooth torque, audible noise is reduced and filtering is made easier since MOSFETs make possible the use of switching frequencies above 20 kHz


Figure 2.1 A simplified diagram of the inverter


Figure 2.2 PWM drive signal for the inverter MOSFETs

If the output of the inverter is short circuited there will be a rapid rise of current in the switches. To limit this peak current an inductor, Ls, is often connected in each leg of the inverter as shown in Fig 2.3. The rate of rise of current under short circuit conditions is then given in equation 1 .

$$
\begin{equation*}
\frac{\mathrm{dI}_{\mathrm{T}}}{\mathrm{dt}}=\frac{\mathrm{V}_{\mathrm{D}}}{\mathrm{~L}_{8}} \tag{1}
\end{equation*}
$$



Figure 2.3 Inverter bridge leg with di/dt limiting inductor

When the MOSFETs turn this fault current (ISC) off the energy in the inductor is transferred to a snobbier capacitor, CS. The over voltage across the MOSFETs is given by equation 2 .

$$
\begin{equation*}
V=\sqrt{\frac{L_{i}}{C_{i}}} I_{S C} \tag{2}
\end{equation*}
$$

The presence of inductor LS affects the normal operation of the inverter. When the MOSFET M1 in Fig.2.3 turns off the diode D2 does not turn on until the voltage across CS is equal to the d.c. link voltage, VD. If the diode did turn on then the rate of rise of - current in LS would be given by equation 3 .

$$
\begin{equation*}
\frac{\mathrm{dI}_{\mathrm{M1}}}{\mathrm{dt}}=\frac{\mathrm{V}_{\mathrm{D}}-\mathrm{V}_{\mathrm{CS}}-\mathrm{V}_{\text {diode }}}{\mathrm{L}_{\mathrm{s}}} \tag{3}
\end{equation*}
$$

This would be greater than the rate of rise of motor current so $\gg$ lrear and the diode would have to conduct in the reverse direction, which is clearly not possible.

During the time when the capacitor CS is charging up to VD, the voltage across LS will always be such as to increase the current in the bottom MOSFET, IM1. When VCS=VD the voltage across LS will reverse and IM1 will fall. Diode D2 will now turn on. The energy stored in LS will now be transferred to CS. This energy will subsequently be dissipated in RS and the MOSFET.

If the ratio of peak to average current carrying capability of the switch is large then it follows from equation 1 that LS can be made smaller. This reduces the energy that is transferred to CS when the MOSFETs switch off during normal operation. Hence the efficiency of the inverter is improved.

The short circuit fault current can be limited by connecting an inductor in the d.c. link as shown in Fig.2.4. In this case analysis similar to that outlined above shows that the excellent ratio of peak to average current carrying capability Of Philips PowerMOS again reduces the losses in the inverter. It has been shown that components chosen to ensure safe shutdown of inverters for motor drives can have deleterious effects on the efficiency of the inverter. In particular the addition of an inductor to limit the peak current through the semiconductor switches when the output is short circuited can increase the switching losses. The high peak to average current carrying capability of Philips PowerMOS reduces the size of this choke and the losses it causes


Figure 2.4 Modified inverter circuit to limit short circuit current

## CHAPTER 3

## MOSFET AND FREDFET FOR MOTOR

### 3.1 Overview

The paper discusses the properties of the FREDFET, a technology which yields a MOSFET with a very fast built-in reverse diode with properties similar to a discrete fast epitaxial rectifier. It is shown that its characteristics make the device an excellent choice for high frequency bridge leg systems such as 20 kHz AC motor control systems.

Investigations have been carried out in dedicated test circuits as well as in a 20 kHz ACMC system which show that the FREDFET exhibits very low diode losses. It compares favorably with a discrete solution, using two extra diodes to overcome the slow speed of the standard built-in diode, and also with devices from the present standard ranges.

### 3.2 Introduction

The Power MOSFET has inherent in its structure a large built-in diode which is present between the source and drain of the device. Under single switch applications such as forward and fly back converters, this diode isn't forward biased and consequently its presence can be ignored. In the case of bridge legs, however, this diode is forced into forward conduction and the properties of the diode become of prime importance. The reverse recovery of the built-in diode is relatively slow when compared with discrete fast recovery epitaxial diodes (FRED's). As a consequence, the currents flowing through the MOSFET and its diode can be high and the losses considerable.


Figure3.1 ACMC bridge leg.

These losses can be reduced through the application of two extra diodes as discussed in section 2. A more elegant solution is a MOSFET with a built-in diode which exhibits properties similar to discrete fast epitaxial rectifiers. The FREDFET has been designed to satisfy this requirement. This paper presents the results of studies, carried out with new FREDFETs, comparing them with both the conventional MOSFET and the discrete solution.

### 3.3 MOSFETS in half bridge circuits

MOSFETS have gained popularity in high frequency AC motor controllers, since they enable frequencies above 20 kHz to be used. The short on-times required in ACMC systems make the use of bipolar devices very difficult, due to the storage times. Both the short switching times and the ease of drive of the MOSFET are essential ingredients in the design of a ultrasonic ACMC. Difficulties can arise, however, when trying to use the built in source to drain diode of the MOSFETs.

One bridge leg of an ACMC is shown in Fig.3.1. When current is flowing out of the load, MOSFET T1 and freewheel diode D2 conduct alternately. Conversely, when
flowing into the load, the current alternates between TR2 and D1. Consider the case when current is being delivered by the load, such that the pair TR1/D2 carries the current. When the MOSFET conducts current, the voltage at the drain is almost zero and the diode blocks. When the MOSFET is turned off by the drive circuit, the inductive load forces the voltage to increase making diode D2 conductive. Associated with conduction of the diode is a volume of stored charge which must be removed as the MOSFET TR1 returns to its on-state.


Figure 3.2 Recovery waveforms
Top: VDS, ID of TR1 turning on
Bottom: VD, ID of D2. ( $\mathrm{t}=200 \mathrm{~ns} / \mathrm{div}$ )

The waveforms appropriate to this situation can be found in Fig.3.2. One may observe that during the diode recovery time, the voltage across the MOSFET remains high whilst at the same time its current increases rapidly. Temporarily the drain current will increase to a level higher than the load current since the diode recovery current is added to it. Long recovery times and excessive charge storage result in a very high power dissipation in the MOSFET.


Figure3.3 Network with extra diodes.

Using the inherent source drain diode of a conventional MOSFET as the free wheel diode results in considerable losses, since it is not optimized for fast switching or low stored charge. To avoid such losses the internal diode is usually deactivated by means of a special circuit (see Fig.3.3). This circuit, using two diodes D2 and D3, ensures that all freewheel current is flowing through the external diode D2 and not through the internal diode D1. When the MOSFET is switched on, the current flows via D3. This circuit is required for each MOSFET in the bridge. The FREDFET, which has a fast built-in diode, offers the prospect of a much neater solution for these kinds of circuits.

### 3.4 Technology of the FREDFET



Figure3.4 FREDFET cross section.

The power MOSFET is a majority carrier device and features fast turn-on and, in particular, fast turn-off. There are no charge storage effects such as in bipolar devices. In bridge leg applications the internal diode can become forward biased and the N epitaxial region (see Fig.3.4) is flooded with holes, which must later be removed when the source becomes negatively biased again with respect to the drain.

The stored charge can be removed by holes diffusing from the N - epilayer into the $\mathrm{P}+$ and P -body regions, and also by recombination of holes and electrons in the N - epitaxial region. A significant reduction in the stored charge Qrr can be achieved by doping the devices with heavy metal atoms to introduce recombination centers. A standard MOSFET will normally have a low concentration of recombination centers. In the FREDFET the heavy metal doping does not have any significant effects on the threshold voltage or the trans conductance, however, the efficiency with which then extra recombination centers remove the stored charge is improved substantially. This can be observed when comparing Qrr and trr results for killed and non-killed devices as described in the next section.

## CHAPTER 4 <br> DISEGNERE GUIDE

### 4.1 Overview

This section is intended to be used as a designers guide to the use and selection of power MOSFETS and FREDFETS in a.c. motor control (ACMC) applications. It is particularly concerned with the variable speed operation of induction motors using pulse width modulation (PWM) techniques. One of the most important considerations in the design of ACMC inverters is the optimum choice of power switching device and heat sinking arrangement. Other factors which relate to the losses in the power switch are switching speed and design of suitable gate drive circuits. This section addresses each of these factors and presents a series of design graphs relating system operating temperature to device type and heat sink size for systems rated up to 2.2 kW and operated from a single phase supply. It should be noted that this article refers to some products which may not be available at this time.

### 4.2 Introduction

Variable speed control of induction motors is a widespread requirement in both industrial and domestic applications. The advantages of an induction motor drive over alternative systems such as D.C. motor controllers include:

- high reliability and long life
- low maintenance requirements
- brushless operation
- availability of standard machines

With the advent of power switching devices able to provide the required ratings for ACMC applications and the availability of fast PWM pattern generation circuits these advantages have lead to an increasing number of applications where the inverter-fed induction motor system produces a cost effective drive. Before considering in detail the use of MOSFETs and FREDFETs in ACMC inverters it is worth briefly considering the
principles and operation of the induction motor, the PWM method of voltage control and the characteristics of the switching devices.

### 4.3 The induction motor

Induction motors are three phase machines where the speed of rotation of the stator field (the synchronous speed, Ns) is determined by the number of poles, p , and the frequency of the applied voltage waveforms, fs.

$$
\begin{equation*}
\mathrm{N}_{\mathrm{s}}=\frac{120 . \mathrm{f}_{\mathrm{s}}}{\mathrm{p}} \quad(\mathrm{rpm}) \tag{1}
\end{equation*}
$$

Torque production in an induction motor is due to the interaction of the rotating stator field and currents in the rotor conductors. Torque is developed when the rotor speed 'slips' behind the synchronous speed of the stator traveling field. Fig.4.1 shows the torque-speed characteristic of an induction motor where $\square \mathrm{s}$ is the speed of the stator field ( $s=2 \mathrm{fs}$ ) and r is the rotor speed. The difference between the two is usually relatively small and is the slip speed. The solid portion of the characteristic is the main region of interest where the motor is operating at rated flux and at low slip. In this region the rotor speed is approximately proportional to the stator supply frequency, except at very low speeds. The operating point of the motor on its torque-speed characteristic is at the intersection of the load torque line and the motor characteristic. For small amounts of slip and at constant air gap flux the motor torque is proportional to the slip speed.


Figure4.1 AC induction motor, Torque-Speed characteristic.


Figure4.2 Torque-Speed characteristics, Variable speed operation.

### 4.4 The PWM Inverter

A variable voltage, variable frequency three phase supply for the a.c. induction motor can be generated by the use of a pulse width modulated (PWM) inverter. A schematic diagram of the system is shown in Fig.4.3. The system consists of a rectified single phase a.c. supply, which is usually smoothed to provide the D.C. supply rails for the main switching devices. Alternate devices in each inverter leg are switched at a high carrier frequency in order to provide the applied voltage waveforms to the motor. During each switching cycle the motor current remains approximately constant due to the inductive nature of the AC motor load.


Figure4.3 PWM inverter, block diagram.

In the circuit of Fig. 4.3 the main switching devices are MOSFETs and each MOSFET has a freewheeling diode connected in ant parallel. The motor load current is determined by the circuit conditions. When the load current in a particular phase is flowing into the motor then conduction alternates between the top MOSFET and the bottom free wheel diode in that inverter leg. When the load current is flowing from the motor then the bottom MOSFET and top diode conduct alternately. Fig. 4.4 shows a typical


Figure4.4 PWM phase voltage waveform.

Sinusoidal PWM voltage waveform for one motor phase. The three phases are maintained at $120^{\circ}$ relative to each other.

Both the frequency and amplitude of the fundamental component of the output voltage waveform can be varied by controlling the timing of the switching signals to the inverter devices. A dedicated a.c. is usually used to generate the switching signals in order to maintain the required $v / f$ ratio for a particular system. (1) The PWM algorithm introduces a delay between the switching signals applied to the MOSFET $\sin$ each ${ }^{\circ}$ inverter leg which allows for the finite switching times of the devices and thus protects the system from shoot-through conditions.
*Additional harmonic components of output voltage, such as the third harmonic, can be added to the PWM switching waveform. $(2,3)$ The effect of adding third harmonic to the output voltage waveform is to increase the amplitude of the fundamental component of output voltage from a fixed D.C. link voltage. This is shown in Fig.4.5. The third harmonic component of output phase voltage does not appear in the output line voltage due to the voltage cancellation which occurs in a balanced three phase system. Using
this technique it is possible to obtain an output line voltage at the motor terminals which is nearly equal to the voltage of the single phase supply to the system.

For many applications the PWM ACMC system is operated at switching speeds in the range 1 kHz to 20 kHz and above. Operation at ultrasonic frequencies has advantages that the audible noise and RFI interference are considerably reduced. The advantages of PowerMOS devices over bipolar switching devices are most significant at these switching speeds due to the low switching times of PowerMOS devices. Additional advantages include good overload capability and the fact that snubbed circuits are not usually required. It is usually straightforward to operate PowerMOS devices in parallel to achieve higher system currents than can be achieved with single devices. This is because the devices have a positive temperature coefficient of resistance and so share the load current equally. The simple gate drive requirements of PowerMOS devices means that a single gate circuit can often be used for a range of devices without modification.

### 4.5 Current rating

The nameplate rating of an induction motor is usually quoted in terms of its power (W) and power factor $(\cos \varphi)$.

The VA requirement of the inverter is found from the simple equation:

$$
\begin{equation*}
\operatorname{Power}(W)=\eta \cdot \cos \varphi \cdot V A \tag{6}
\end{equation*}
$$

Where ${ }^{11}$. is the efficiency. In terms of the rms motor line voltage (Vline) and output current (IL):

$$
\begin{equation*}
V A=\sqrt{ } 3 \cdot V_{\text {line }} \cdot I_{L} \tag{7}
\end{equation*}
$$

The efficiency of small ac induction motors can be quite high but they usually run at quite poor power factors, even at rated conditions. For small induction motors $(<2.2 \mathrm{~kW})$ the efficiency-power factor product is typically in the range 0.55 to 0.65 . The exact value will vary from motor to motor and improves with increasing size. Thus from
equations (6) and (7) it is possible to calculate the approximate rms current requirement. The peak device current for sinusoidal operation is given by equation (8). (NB. The devices will experience currents in excess of this value at switching instants.)

$$
\begin{equation*}
I_{\max }=\sqrt{2} \cdot I_{L} \tag{8}
\end{equation*}
$$

### 4.6 Device package

The device package chosen for a particular application will depend upon device rating, as discussed above, as well as circuit layout and heat sinking considerations. Philips PowerMOS devices are available in a range of package types to suit most applications.

### 4.7 Gate drive circuits for ACMC inverters

The previous section discussed device switching waveforms using a resistive gate drive circuit. In this section various alternative gate drive circuits for ACMC applications are presented and compared .The discussion assumes that each MOSFET gate drive circuit is isolated and driven using a CMOS buffer capable of sinking and sourcing the required gate current. In un buffered gate drive circuits the leakage inductance of an isolating pulse transformer can increase the gate impedance, thus reducing the maximum possible switching rate and making the MOSFET more susceptible to parasitic turn-on. A zener diode clamp protects the gate-source boundary from destructive over voltages. Identical drivers are used for the top and bottom devices in each inverter leg. The gate drive circuits presented here were tested using BUK638500A FREDFETS and BUK438-500A MOSFETS in a $20 \mathrm{kHz}, 2.2 \mathrm{~kW}$ ACMC system.

Figure 4.5 shows the simplest arrangement which gives independent control of the turnon and turn-off of then MOSFET. Increasing the gate impedance to reduced VDS/DT levels will raise the susceptibility to parasitic turn-on problems. The gate-source voltage can be clamped


Figure 4.5 Gate drive circuit with different turn-on and turn-off paths

When we use Circuit Maker, we will find the fig. 4.5 by put a 50 V as following:


```
xa: 5.000u xb: 0.000 a-b: 5.000u freq; 200.0k
Yc: 3.00e-15 yd:-15.0e-15 c-d: 18.0e-15
```



Figure 4.5 by using Circuit Maker


Figure 4.6 Gate drive circuit with improved parasitic turn-on
Immunity
more effectively if the dynamic impedance between gate and source is reduced as shown in the circuit of Fig.4.6.

An alternative circuit which may be used to hold the MOSFET off-state gate-source voltage below its threshold value is shown in Fig.4.7. The PNP transistor turns on if the gate-source voltage is pulled up via CGD and CGS and thus the device remains clamped off.


Figure 4.7 Alternative gate drive circuit with improved Parasitic turn immunity

### 4.8 Paralleling of PowerMOS devices

Moving to a system using paralleled MOSFETs requires only slight modifications to the gate drive circuit. One consideration may be the capability of the drive buffer to provide the currents required at the switching instants. The switching speed of the system can be maintained. Using a lower impedance gate drive. It is recommended that small differential resistors, as shown in Fig.4.8, are used to damp out any oscillations which may occur between the switching devices and the rest of the circuit. The circuit of Fig.4.6 can be modified for operation with parallel Ed devices to that shown in Fig.4.9.

### 4.9 Circuit layout considerations

The effects of poor circuit design and layout are to increase RFI and noise and to compromise the performance and speed of the system due to stray inductances. The precautions which must be taken to minimize the amount of stray inductance in the circuit include:

- positioning the gate drive circuits, especially zener diodes
and $\mathrm{dv} / \mathrm{dt}$ clamping circuits as close as possible to the power MOSFETs.
- reducing circuit board track lengths to a minimum and using twisted pairs for all interconnections.
- For paralleled devices, keeping the devices close to each other and keeping all connections short and symmetrical.


Figure 4.8 Gate drive circuit for paralleled devices


Figure 4.9 Gate drive circuit for paralleled devices with improved parasitic turn-on immunity

### 4.10 Device losses in ACMC inverters

It is important to be able to calculate the losses which occur in the switching devices in order to ensure that device operating temperatures remain within safe limits. Cooling arrangements for the MOSFETs or FREDFETs in an ACMC system will depend on maximum allowable operating temperatures, ambient temperature and operating conditions for the system. The components of loss can be examined in more detail:

### 4.11 MOSFET Conduction losses

When a MOSFET or FREDFET is on and carrying load current from drain to source then the conduction 'i2R' loss can be calculated. It is important to note that the device current is not the same as the output current, as Demonstrated by the waveforms of Fig.4.10. The figures how a sinusoidal motor load current waveform and the top and bottom MOSFET currents. The envelopes of the MOSFET currents are half sinusoids; however the actual device currents are interrupted by the instants when the load current flows through the freewheel diodes. For the purposes of calculating MOSFET conduction losses it is acceptable to neglect the 'gaps' which occur when the freewheel diodes are conducting for the following reasons:


Figure 4.10 Motor current and device current waveforms in a PWM inverter
-When the motor load current is near its maximum value the switching duty cycle is also near its maximum and so the proportion of time when the diode conducts is quite small and can be neglected.
-When the motor load current is near zero then the switching duty cycle is low but the MOSFET is only conducting small amounts of current. As the MOSFET current is low then the contribution to total conduction loss is small.

Thus if the MOSFET is assumed to be conducting load current for the whole half-period then the conduction losses can be calculated using the current envelope of Fig.4.10. These losses will be overestimated but the discrepancy will be small. The conduction losses can be given by:

$$
\begin{equation*}
P_{\text {MON }}=I_{T}^{2} \cdot R_{\text {DSON }}\left(T_{j}\right) \tag{13}
\end{equation*}
$$

Where IT is the rms value of the half sinusoid MOSFET current envelope.

$$
\begin{equation*}
\text { And: } \quad R_{\text {osions }( }\left(T_{1}\right)=R_{\text {Dsiow }}\left(25^{\circ} \mathrm{C}\right) \cdot e^{k(T-26)} \tag{14}
\end{equation*}
$$

Where $\mathrm{k}=0.007$ for a 500 V MOSFET, and $\mathrm{k}=0.006$ for a 500 V FREDFET.

IT is related to the rms motor current, IL, by:

$$
\begin{equation*}
I_{\mathrm{T}}=\frac{I_{\max }}{2}=\frac{I_{\mathrm{L}}}{\sqrt{2}} \tag{15}
\end{equation*}
$$

PHILIPS 500V FREDFETS
Frequency $=5 \mathrm{kHz}$


PHILIPS 500V FREDFETS
Frequency $=20 \mathrm{kHz}$



Figure 4.11 Selection graphs for a 1.7A motor
NB. Device selection notation: 1X655-A denotes a single BUK655-500A FREDFET, etc.

Additionally in a MOSFET inverter the series blocking Scotty diode (D3 of Fig.4.8) has conduction losses. The current in this diode is the main MOSFET current and so its loss is approximated by:

$$
\begin{equation*}
P_{\text {San }(0 n)}=V_{( }\left(T_{i}\right) \cdot I_{T} \tag{16}
\end{equation*}
$$

### 4.12 Diode conduction losses

In a MOSFET inverter the freewheel diode losses occur in a discrete device (D2 of Fig.4.8) although this device is often mounted on the same heat sink as the main switching device. In a FREDFET circuit the diode losses occur in the main device package. The freewheeling diode carries the 'gaps' of current shown in Fig.4.10 during the periods when its complimentary MOSFET is off. Following the argument used above the diode conduction loss is small and can be neglected. Using this simplification we have effectively transferred the diode conduction loss and included it in the figure for MOSFET conduction loss.

### 4.13 MOSFET switching losses

During the half-cycle of MOSFET conduction the load current switched at each instant is different (Fig.4.10). The amount of current switched will also depend on the reverse recovery of the bridge leg diodes and hence on the

$$
\begin{gathered}
\text { PHILIPS 500V FREDFETS } \\
\text { Frequency }=5 \mathrm{kHz}
\end{gathered}
$$



## PHILIPS 500V FREDFETS

## Frequency $=20 \mathrm{kHz}$



PHILIPS 500V MOSFETS (+ diode network)
Frequency $=5 \mathrm{kHz}$



Figure 4.12 Selection graphs for a 3.4A motor
NB. Device selection notation: 1X655-A denotes a single BUK655-500A FREDFET, etc.
temperature of the devices. The total turn-on loss (PM(SW)) will be a summation of the losses at each switching instant:

$$
\begin{equation*}
\mathrm{P}_{\text {Masw }}=\sum_{n=0}^{\infty} f\left(\mathrm{~T}_{j ;} \mathrm{I}_{n}\right) \tag{17}
\end{equation*}
$$

MOSFET turn-off times are usually only limited by $\mathrm{dv} / \mathrm{dt}$ considerations and hence are as short as possible. The turn-off loss of the MOSFETs or FREDFETs in an inverter is small compared with the turn-on loss and can usually be neglected.

### 4.14 Diode switching losses

Diode turn-off loss (PD (SW)) is calculated in a similar manner to the MOSFET turn-on loss. The factors which affect the diode turn-off waveforms have been discussed earlier. Diode turn-on loss is usually small since the diode will not conduct current unless forward biased. Thus at turn-on the diode is never simultaneously supporting a high voltage and carrying current.

### 4.15 Gate drive losses

Some loss will occur in the gate drive circuit of a PowerMOS device. As the gate drive is only delivering short pulses of current during the switching instants then these losses are negligibly small.

PHILIPS 500V FREDFETS
Frequency $=5 \mathrm{kHz}$


PHILIPS 500V FREDFETS
Frequency $=20 \mathrm{kHz}$


$$
\begin{array}{cccccc}
\text { 1X638-A } & 2 \times 637-A & 3 \times 637-A & 2 \times 638-A & 3 \times 638-A & 1 \times 617-A E \\
\square & -A & \cdots & -\cdots & -
\end{array}
$$



PHILIPS 500V MOSFETS (+ diode network)
Frequency $=20 \mathrm{kHz}$

Heatsink temperature, T_hs



Figure 4.13 Selection graphs for a 6.8 A motor
NB. Device selection notation: 1X638-A denotes a single BUK638-500A FREDFET, etc.

### 4.16 System operating temperatures

In this section the device losses discussed in the previous section are calculated and used to produce a design guide for the correct selection of Philips PowerMOS devices and appropriate heat sink arrangements for ACMC applications. The following factors must be taking into account when calculating the total system loss, PLOSS:

- Device characteristics.
- Switching frequency.
- Operating temperature.
- Load current.
- Number of devices used in parallel.
- Additional snobbier or di/dt limiting networks.

$$
\begin{equation*}
\text { PLOSS }=\mathrm{PM}(\mathrm{ON})+\mathrm{PM}(\mathrm{SW})+\mathrm{PD}(\mathrm{SW})+\mathrm{PSch}(\mathrm{ON}) \tag{18}
\end{equation*}
$$

For the results presented here the device parameters were taken for the Philips range of 500 V MOSFETs and FREDFETs. The on-state losses can be calculated from the equations given above. For this analysis the device switching losses were measured experimentally as functions of device temperature and load current. As there are six sets of devices in an $A C M C$ inverter then the total heat sink requirement can be found from:

$$
\begin{align*}
& \text { Ths }=\text { Tahs }+6 . \text { PLOSS.Rth (hs-ahs) }  \tag{19}\\
& \mathrm{Tj}=\text { Ths }+ \text { PLOSS.Rth }(\mathrm{j}-\mathrm{hs}) \tag{20}
\end{align*}
$$

## PHILIPS 500V FREDFETS <br> Frequency $=5 \mathrm{kHz}$

Heatsink temperature, T_hs



PHILIPS 500V FREDFETS
Frequency $=\mathbf{2 0 k H z}$


PHILIPS 500 V MOSFETS (+ diode network) Frequency $=5 \mathrm{kHz}$



PHILIPS 500 V MOSFETS (+ dlode network)
Frequency $=20 \mathrm{kHz}$


Figure 4.14 Selection graphs for a 10A motor
NB. Device selection notation: 2X638-A denotes two paralleled BUK638-500A FREDFETs, etc.

Equations 18 to 20 can be used to find the heat sink size (Rth (hs-ahs)) required for a particular application which will keep the heat sink temperature (Ths) within a required design value. Results are plotted in Figures 4.10 to 4.11 for motor currents of $\mathrm{IL}=1.7 \mathrm{~A}$,
$3.4 \mathrm{~A}, 6.8 \mathrm{~A}$ and 10.0 A . These currents correspond to the ratings of several standard induction motor sizes. The results assume unsnapped devices, an ambient temperature of Tahs $=40^{\circ} \mathrm{C}$, and are plotted for inverter switching frequencies of 5 kHz and 20 kHz .

Two examples showing how these results may be used are given below:

1) The first selection graph in Fig4.11 shows the possible device selections for 500 V FREDFETs in a 5 kHzACMC system where the full load RMS motor current is 1.7A. Using a BUK655-500A FREDFET, Ths can be maintained below $70^{\circ} \mathrm{C}$ with a total heat sink requirement of $1.2 \mathrm{~K} / \mathrm{W}$ (if each FREDFET was mounted on a separate heat sink then each device would need a $7.2 \mathrm{~K} / \mathrm{W}$ heat sink). The same heat sinking arrangement will give Ths $=50^{\circ} \mathrm{C}$ using a BUK638-500A. Alternatively Ths can be maintained below $70^{\circ} \mathrm{C}$ using a $2 \mathrm{~K} / \mathrm{W}$ heat sink $(12 \mathrm{~K} / \mathrm{W}$ per device) and the BUK637-500B.
2) In Fig.4.14 the selection graphs for a 10A system are given. The fourth selection graph is for a 20 kHz switching frequency using 500 V MOSFETs. Here two BUK438-500A devices connected in parallel for each switch will require a total heat sink size of $0.3 \mathrm{~K} / \mathrm{W}$ if the heat sink temperature is to remain below $90^{\circ} \mathrm{C}$. The same temperature can be maintained using a $0.5 \mathrm{~K} / \mathrm{W}$ heat sink and a single BUK417500AE ISOTOP device.

For different motor currents or alternative PWM switching frequencies the appropriate device and heat sink arrangement for a particular application can be found by interpolating the results presented here.

## CONCLUISION

This section has outlined the basic principles and operation of PWM inverters for ACMC applications using Philips PowerMOS devices. MOSFETs and FREDFETs are the most suitable devices for ACMC systems, especially at high switching speeds. This section has been concerned with systems rated up to 2.2 kW operating from a single
phase supply and has shown that there is a range of Philips PowerMOS devices ideally suited for these systems.

The characteristics and performance of MOSFETs and FREDFETs in inverter circuits and the effect of gate drive design on their switching performance has been discussed. The possibility of parasitic turn-on of MOSFETs in an inverter bridge leg can be avoided by appropriate gate drive circuit design. Experimental and simulated results have shown that good switching performance and immunity to parasitic turn-on can be achieved using the Philips range of PowerMOS devices in ACMC applications. Using the device selection graphs presented here the correct MOSFET or FREDFET for a particular application can be chosen. This guide can be used to select the heat sink size and device according to the required motor current, switching frequency and operating temperature.

## CHAPTER 5 <br> HIGH FECUENCY INVERTOR POLE BY (300V, 40A)

### 5.1 Overview

Voltage source inverters which are switched using some form of pulse width modulation are now the standard in low to medium rated AC and brushless DC variable speed drives. At present, because of device limitations the switching (modulation) frequencies used in all but the lowest drive ratings are restricted to a few kHz . There is however a strong technical advantage in using much higher ultrasonic switching frequencies in excess of 20 kHz , the benefits of which include:
i) The low frequency distortion components in the inverter output waveform are negligible. As a result there is no longer a need to derate the electrical machine in the drive as a consequence of harmonic loss.
ii) The supply derived acoustic noise is eliminated.
iii) The DC link filter component values are reduced.

The device best suited for high switching frequencies is the power MOSFET because of its extremely fast switching time and the absence of secondary breakdown. However, being surface conduction devices, high power rated MOSFETs are difficult and expensive to manufacture and at present single MOSFETs are only suitable for inverter ratings of typically 1-2 KVA per pole. Although higher rated power devices such as bipolar transistors and IGBTs can be switched at medium to high frequencies, the switching losses in these circuits are such that frequencies in excess of 20 kHz are at present difficult to achieve.

Switches with high ratings and fast switching times can be constructed by hard paralleling several lower rated power devices. MOSFETs are particularly suitable because the positive temperature coefficient of the channel resistance tends to enforce good steady-state current sharing between parallel devices. However to achieve good
dynamic current sharing during switching, considerable care must be taken in the geometric layout of the paralleled devices on the common heat sink. In addition, the device characteristics may need to be closely matched. As a result modules of paralleled MOSFETs are often expensive.


Within each mdule: Good transient + steady state load sharing Isolated drive circuit

Figure5.1

An alternative approach to paralleling is to use small switching aid networks which overcome the constraints of hard paralleling by improving the dynamic load sharing of the individual devices. It is possible to envisage an inverter design where each pole consists of a number of identical pole modules which share a common supply and have outputs connected in parallel, as shown in Fig.5.1. Each module is designed to operate individually as an inverter pole and contains two power MOSFETs with associated isolated gate drive circuitry. When the modules are connected in parallel their design is such that they will exhibit good transient and steady-state load sharing, the only requirement being that they are mounted on a common heat sink. In this manner any inverter volt-amp rating can be accommodated by paralleling a sufficient number of pole modules.

### 5.2 Pole module

The power circuit diagram of an individual pole module which is suitable for the second form of paralleling is shown in Fig.5.2. The design makes use of the integral body diode of the main switching devices and for this purpose the fast recovery characteristics of FREDFETs are particularly suitable. Two snobbier circuits and a centre tapped inductance are included in the circuit. These small switching aid networks perform a number of functions in the circuit:


Figure 5.2
i) They act to improve the dynamic current sharing between the pole modules when connected in parallel.
ii) They ensure safe operation of the MOSFET integral body diode. The central inductance controls the peak reverse current of the diode and the snobbier network prevents secondary breakdown of the MOSFET parasitic internal transistor as the integral body diode recovers.
iii) They reduce the switching losses within the main power devices and thus allow maxinum ase of the available rating.


Figure 5.3

The operation of the circuit is typical of this form of inverter pole. The commutation of the integral body diode will be discussed in detail since it is from this section of the operation that the optimal component values of the switching aid network are determined. The value of the inductor L is chosen to give a minimum energy loss in the circuit and the snubbed network is designed to ensure safe recovery of the integral diode at this condition. For example consider the case when there is an inductive load current IL flowing out of the pole via the integral body diode of the lower MOSFET just prior to the switching of the upper MOSFET. With reference to Fig5.3, the subsequent operation is described by the following regions:

Region A: Upper MOSFET is switched on. The current in the lower integral body diode falls at a rate ( $\mathrm{di} / \mathrm{dt}$ ) equal to the DC link voltage VDD divided by the total inductance L of the centre tapped inductance.

Region B: The diode current becomes negative and continues to increase until the junction stored charge has been removed, at which stage the diode recovers corresponding to a peak reverse current IRR.

Region C: The voltage across the lower device increases at a rate (dv/dt) determined by the capacitance Cs of the lower snobbier network. The current in the upper MOSFET and the inductor continues to increase and reaches a peak when the voltage across the lower device has risen to the DC link value. At this point the diode Dc becomes forward biased and the stored energy in the inductor begins to discharge through the series resistance RC .

The energy E1 gained by the switching aid a network over the above interval is given by:

$$
\begin{equation*}
E_{1}=\frac{1}{2} I_{R R}^{2}+\frac{1}{2} C_{S} V_{D D}^{2} \tag{1}
\end{equation*}
$$

And is ultimately dissipated in the network resistors Rs, Rc. For a given forward current, the peak reverses current IRR of the diode will increase with increasing di/dt and can be approximately represented by a constant stored charge, (QRR) model, where:

$$
\begin{equation*}
I_{R R}=\sqrt{2\left(\frac{d I}{d t}\right) Q_{R R}} \tag{2}
\end{equation*}
$$

Although in practice IRR will tend to increase at a slightly faster rate than that given by equation (2). Since in the inverter pole circuit

$$
\begin{align*}
& \frac{d I}{d t}=\frac{V}{L}  \tag{3}\\
& I=\sqrt{\frac{2 V_{D D} Q_{R R}}{L}} \tag{4}
\end{align*}
$$

Inspection of equations (1) and (4) shows that the energy loss E1 remains approximately constant as L is varied. During the subsequent operation of the inverter pole when the upper MOSFET is turned off and the load current IL returns to the integral body diode *of the lower device, an energy loss E2 occurs in the inductor and the upper snobbier equal to:

$$
\begin{equation*}
E_{2}=\frac{1}{2} L_{L}^{2}+\frac{1}{2} C C_{S D}^{2} \tag{5}
\end{equation*}
$$

This loss can be seen to reduce with $L$. However as $L$ is reduced both IRR and the peak current in the upper MOSFET will increase and result in higher switching loss in the diode and higher conduction loss in the channel resistance of the upper device.

The value of L which gives minimum energy loss in the pole occurs when there is an optimal balance between the effects described above. Typical measured dependencies of the total energy loss on the peak reverse diode current as $L$ is varied. The characteristics of a similarly rated conventional MOSFET and a fast recovery FREDFET are compared in the figure. In both cases the minimum energy loss occurs at the value of L which gives a reverse recovery current approximately equal to the design load current. However the loss in the FREDFET circuit is considerably lower than with the conventional device. The optimal value of L can be found from the manufacturer's specified value of stored charge using equation (4), where

$$
\begin{equation*}
L_{o p t}=\frac{2 V_{D D} Q_{R R}}{L_{L}^{2}} \tag{6}
\end{equation*}
$$

The snubbed capacitor value Cs is chosen to limit the $\mathrm{dv} / \mathrm{dt}$ across the integral body diode as it recovers. Experience has shown that a value of $1 \mathrm{~V} / \mathrm{nS}$ will ensure safe operation, hence:

$$
\begin{equation*}
C=\left(C_{L}\right) n F \tag{7}
\end{equation*}
$$

The resistive component of the switching aid networks are chosen in the usual manner.

### 5.3 Parallel operation of pole modules

The principle behind the 'soft' paralleling adopted here is to simply connect the outputs of the required number of modules together and feed them with a common DC link and control signals. The transient load sharing between the parallel modules will be influenced by the tolerances in the individual inductor and snobbier capacitor values and any variations in the switching instances of the power devices, the latter being as a result of differences in device. Characteristics and tolerances in the gate drive circuitry. These effects were investigated using the SPICE circuit simulation package. The SPICE representation of the modules, in which the upper MOSFET channel is modeled by an ideal switch with a series resistance RDS. The full SPICE diode model is used for the lower MOSFET integral body diode; however ideal diode representations are sufficient
for the devices in the switching aid networks. The load is assumed to act as a constant current sink over the switching interval.

From the SPICE simulation an estimate of the peak transient current imbalance between the MOSFETs of the two modules was obtained for various differences in the inductors, capacitors and device turn-on times. It was found that the transient current sharing was most sensitive to unequal device switching times. An example of the results obtained from a simulation of two paralleled modules using BUK638-500B FREDFETs. With good gate drive design the difference between device switching times is unlikely to exceed 50 nS resulting in a peak transient current mismatch of less than $10 \%$. The load sharing would improve if the value of inductor is increased but this has to be traded off against the increase in switching loss. The effect of the tolerance of the inductor values on the load sharing is given for the same module, where it can be seen that a reasonable tolerance of $10 \%$ results in only a $7 \%$ imbalance in the currents. The load sharing was found to be relatively insensitive to tolerances in the snobbier capacitor values.

## CHAPTER 6 POLE MODULE DESIGN BY (300V, 10A)

### 6.1 Overview

The conventional R-C snobbier network has been replaced by the active circuit shown in Fig. 1 and involves the use of a second, low rated BUK455-500B MOSFET which is made to act as a capacitance by invoking the 'Miller' effect. The active snobbier is more efficient at low load currents because it tends to maintain a constant (dv/dt) regardless of the load, and thus the snobbier loss is proportional to the current, as opposed to the conventional circuit in which the loss remains constant. In addition the active circuit is compact and lends itself more readily to a hybrid assembly. The major component costs are the secondary MOSFET and a low voltage power diode and compare favorably with those of the conventional high voltage capacitor and high voltage diode.


Figure6.1


Figure6.2

The losses of an individual module switched at 20 kHz are plotted in Fig. 6.3 as a function of output current. They mainly stem from conduction loss, the switching loss representing only a third of the maximum loss. Because the switching loss occurs mainly in the aid networks the main FREDFETs can be used at close to their full rating. Similarly operation at higher frequencies will not result in a substantial reduction in efficiency, for example at $40 \mathrm{kHz}, 10 \mathrm{~A}$ operation the losses are 95 W .

Four modules were connected in parallel and mounted on a common heat sink. The modules operated successfully at 300 V with total loads in excess of 40 A , four times their individual rating. The common heat sink, which had a thermal resistance to ambient of $0.33^{\circ} \mathrm{C} / \mathrm{W}$ was sufficient to achieve the full $40 \mathrm{~A}, 300 \mathrm{~V}$ continuous rating of the parallel units at 20 kHz . The current waveforms of the upper FREDFETs in each module are overlaid in Fig.6.4, where it can be seen that the load sharing is very even, particularly after the initial switching transients.


Figure6.3

$5 \mathrm{~A} / \mathrm{div}$
$2 \mathrm{~ms} /$ div
Figure6.4 FREDFET current waveforms

## CONCLOUSION

Parallel, separate MOSFET pole modules provide a method of designing medium rated inverter poles, which can be switched efficiently at frequencies in excess of 20 kHz . The approach is flexible since a single pole module design can be used to achieve a range of inverter volt-amp ratings by paralleling a sufficient number of units. Through the use of small switching aid networks it is possible to obtain excellent transient and steady-state current sharing between the paralleled modules. The current sharing remains good even if there are substantial Variations in component tolerances and the power device switching times. The switching aid network also reduces the switching losses in the main devices and allows them to be used to their full rating. The presented design of a $300 \mathrm{~V}, 10 \mathrm{~A}$ module based on BUK638-500B, FREDFETs has a full load loss of only 70 W . Four of these modules connected in parallel and mounted on a $0.33^{\circ} \mathrm{C} / \mathrm{W}$ heat sink 20 gave an inverter pole with a $300 \mathrm{~V}, 40 \mathrm{~A}$ continuous rating when switched at 20 kHz . Excellent current sharing between these modules was observed and as a result there would seem to be no technical reasons why further modules could not be paralleled to achieve even higher ratings.

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