NEAR EAST UNIVERSITY

Faculty of Engineering

Department of Electrical and Electronic Engineering

ONE LINE TRAFFIC CONTROLLER

Graduation Project
EE- 400

Student: Latif Nizipli (970333)

Supervisor: Kaan Uyar

Nicosia - 2000

ACKNOWLEDGMENTS

I want to thanks to my supervisor Mr. Kaan Uyar for his helps. I also want to thanks to Prof Dr. Khalil Ismailov for his creative ideas.

ABSTRACT

In this project you will see the logic world and where it can be used for the solving problems We divided this project into three main chapters. The first chapter is give the basic introduction about the project. In the second chapter we gave some introduction about the TTL gates. The last chapter consist of all details of the circuit it's parts and the jobs of each parts.

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1. INTRODUCTION

Everyone saw a one-line bridge in his/her life at least one time so that you will know that there is only one-way traffic currently flows at a time. You can see such a bridge in the appendix part. First picture is from SOSYAL KONUTLAR arca of the Lefkoşa. Also second picture is the same bridge but different view. The last picture is taken from the MARMARA area of the Lefkoşa. But driving on these bridge is very dangerous and so boring for the drivers. So traffic lights have to be used on such a bridges to control of traffic currency. Also this Lights must be apply different green time for different traffic. Also this lights must be operate for the cars that is passing through the bridge. I mean that if there is a car which is passing through the bridge the lights must be wait to change it's position. There is different ways to control of these parameters One of these ways is of course logic controller.

We used logic idea for this job. In this project everything is depends on the logical operation and logic idea. Before beginning we wants to give some information about **TTL** gates.

2. INTRODUCTION TO TTL GATES

In this chapter we want to give some information about the Transistor-Transistor Logic (TTL) family.

2.1 7400 Devices:

The 7400 series a line of TTL circuits introduced by Texas instruments in 1964 has become the most widely used of all bipolar IC's. This TTL contains a variety of SSI and MSI chips that allow you to build all kinds of digital circuits and systems.

2.2 Propagation Delay Time and Power Dissipation:

Two quantities needed for our later discussion are power dissipation and propagation delay time. A standard TTL gate has a power dissipation of about lOmWJt may vary from this value because of signal levels, tolerances. Etc.; but on the average it is 10 mW per gate.

The propagation delay time is the amount of time it takes for the output of a gate to change after the inputs have changed. The propagation delay time of a TTL gate is in the vicinity of l0 ns.

2.3 Device Numbers:

If you look at the Table 1.1 you can see some of 7400-series TTL gates. For instance, the 7400 is a chip with four 2-input NAND gates in one package. Similarly the 7402 have four 2-input NOR gates the 7404 have six inverters and so on.

Device number	Description
7400	Quadra 2-input NAND gates
7402	Quadra 2-input NOR gates
7404	Hex inverter
7408	Quadra 2-input AND gates
7410	Triple 3-input NAND gates
7411	Triple 3-input AND gates
7420	Dual 4-input NAND gates
7421	Dual 4-input AND gates
7427	Triple 3-input NOR gates
7430	8-input NAND gate
7486	Quadra 2-input XOR gates

Table 2.1 : Some of the TTL gates and its Numbers

2.4 5400 Series :

Any devices in the 7400 series works over a temperature range of 0₀ to 70C₀ and over a supply range of 4.75 to 5.25 V This is adequate for commercial applications. The 5400 series, developed for the military applications has the same logic functions as the 7400 series, except that it works over a temperature range of -5 5 to 125C₀ and over a supply range of 4.5 to 5.5V.A1though 5400-series devices can replace 7400-series devices, they are rarely used commercially because of their much higher cost.

2.5 High Speed TTL:

By decreasing the resistances a manufacturer can lower the internal time constants ; this decreases the propagation delay time. The smaller resistances, however, increase the power dissipation. This variation is known as High Speed TTL. Devices of this type is numbered 74HOO, 74H01, 74H02 etc. A High Speed TTL gate has a power dissipation around 22mW and a propagation delay time of approximately 5 ns.

2.6 Low Power TTL :

By increasing the internal resistances a manufacturer can reduce the power dissipation of TTL gates. Devices of this type are called Low Power TTL and are numbered 74LOO, 74L01, 74L02 etc. These devices are slower than the standard TTL because of the larger internal time constants. A Low Power TTL gate has a power dissipation of approximately 1 mW and a propagation delay time around 3 5 ns.

2.7 Schottky TTL:

With standard TTL, High Speed TTL and Low Power TTL the transistors go into saturation causing extra carriers to flood the base. If you try to switch this transistor from saturation to cutoff, you have to wait for the extra carriers to flow out of the base; the delay is known as the saturation delay time.

One way to reduce the saturation delay time is with Schottky TTL. The idea is to fabricate a Schottky diode along with each bipolar transistor of a TTL circuit, Because the Schottky diode has a forward voltage of only 0.4 V, it prevents the transistor from saturating fully. This virtually eliminates saturation delay time , which means better switching speed. This variation is called Schottky TTL ; These devices are numbered as 74SOO, 74S01 , 74S02 etc.

Schottky TTL devices are very fast , capable of operating reliably at 100 MHz . The 74s00 has a power dissipation around 20mW per gate and a propagation delay time of approximately 3 ns.

2.8 Low Power Schottky TTL :

By increasing the internal resistance as well as using Schottky diodes manufacturers have come up with the best compromise between low power and high speed ' Low Power Schottky TTL. Devices of this type are numbered 74LSOO, 74LS01

,74LS02 etc. A Low Power Schottky gate has a power dissipation of around 2 mW and propagation delay time is approximately 10 ns as shown in table 2.2.

Standard TTL and low-power Schottky TTL are the main stays of the digital designer. In other words of the five TTL types listed in table 2.2 , standard TTL and low power Schottky TTL have emerged as the favorites of the digital designers You will see them more than any other bipolar types.

TYPE	Power mW	Delay Time ns
Low-Power	1	35
Low-Power Schottky	2	10
Standard	10	10
High-Speed	22	6
Schottky	20	

Table 2.2 : TTL Power-Delay values

2.9.1 Worst-Case Input Voltage

Table 2.3 shows us the TTL inverter with an input voltage of Vi and an output voltage of Vo. When Vi is 0 V (Grounded) the output voltage is high. With TTL devices, we can raise Vi to 0.8 V and still have a output. The maximum low-level input voltage is designated V_{IL} . Data sheets list this worst-case low input as

$$V_{IL} = 0.8 \text{ V}$$

Take the other extreme. Suppose Vi is 5 V in table 2.3 this is a high input ; therefore the output of the inverter is low , Vi can decrease all the way down to 2 V , and the output will still be low .Data sheets list this worst-case high input as

$$V_{NI} = 2\ V$$

In other words , any input voltage from 2 to 5 V is a high input for TTL devices.

2.9.2 Worst-Case Output Voltages

Ideally 0 V is the low output and 5 V is the high output . We cannot attain these ideal values because of internal voltage drops. Any voltage from 0 to 0.4 V is a low output. This means that the worst-case output values are

$$V_{OL} = 0.4\ V \qquad V_{OH} = 2.4$$

	Output V	**Input** V
Low	0.4	0.8
High	2.4	2

Table 2.3 TTL states (Worst Case)

2.9.3 Standard Loading :

A TTL device can source current (high output) or it can sink current (Low output) .Data sheets of standard TTL devices indicate that any 7400-series device can sink up to 16 ms designated as

$$I_{OL} = 16\ mA$$

And can source up to 400 μA

$$İon = -400\ \mu A$$

Minus sign means that the current is out of the device and a plus sign means that it's into the device.A single TTL load has a low-level input current of 1.6 mA and a high-level input current of 400 μA since the maximum output current is 10 times greater than input so that we can connect 10 TTL emitters to any TTL output In the next table (Table 2.4) you can see the number ofloads for each type TTL.

	TTL load				
TTL DRIVER	74	74H	74L	74S	74LS
74	10	8	40	8	20
74H	12	10	50	10	25
74L	2	1	20	1	10
74S	12	10	100	10	50
74LS	5	4	40	4	20

Table 2.4 Fan-outs

3. WORKING PRINCIPLE OF THE CIRCUIT

3.1 Two-way traffic on a one-lane road

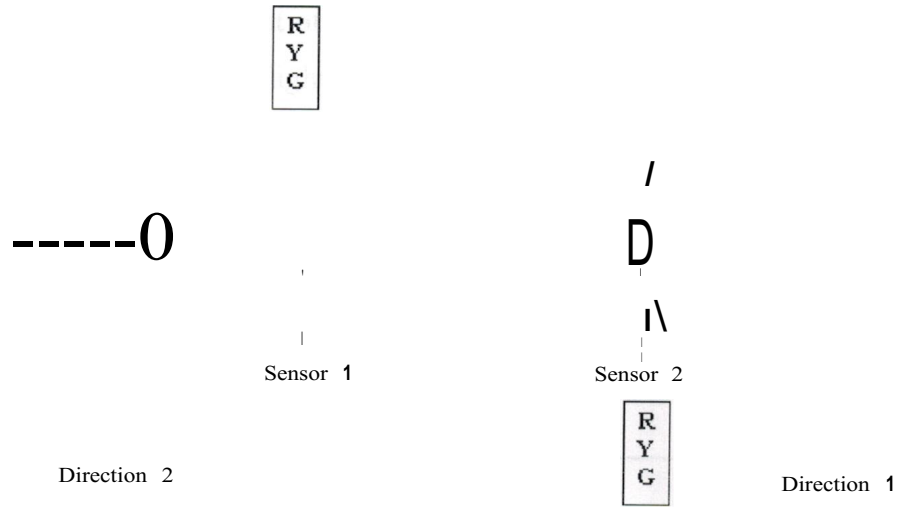

Figure 3.1 One-lane road

A sensor will be positioned at each end of the road to detect cars entering and leaving the road. Time will be allocated to traffic flow in each direction according to traffic flow measurements obtained from the sensors during each 5-minute period.

To control the two-way traffic in this single lane requires special traffic signals at each end of the single lane road that allow traffic to move in one direction for a period of time and then stop it to allow traffic to flow in the other direction, alternating back and forth. For each direction change the traffic signal controller must halt traffic in one direction and wait until the lane is clear before allowing traffic to proceed in the opposite direction. To achieve optimum traffic flow the period of time allotted to traffic in each direction should be adjusted according to the traffic conditions, with the direction corresponding to heavier traffic allocated a longer period of time than the other. Traffic flow measurements can be made by using sensors embedded in the road at each end of the lane.

G1	Green light of direction	1
Y1	Yellow light of direction	1
R1	Red light of direction	1
G2	Green light of direction	2
Y2	Yellow light of direction	2
R2	Red light of direction	2
S1	Sensor light of direction	1
S2	Sensor light of direction	2

Each sensor generates a pulse whenever crossed by a car. A manual RESET button will also be provided to initialize the controller.

Figure 3.2 : Timing Diagram of the Circuit

T tot : is a total amount of green light time and will be aplitic between directions 1 and 2 according to the relative traffic flow in each directions. Now let us see the block diagram of the circuit.

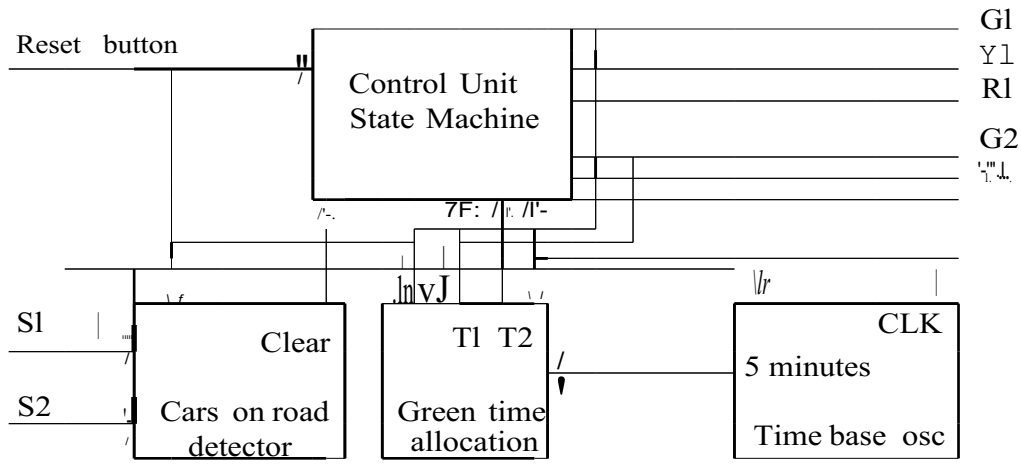

Figure 3.3 Block diagram of the circuit

3.2. Circuits

3.2.1 Control Unit State Machine

The states designed as follow.

State	Light I	Light2
A	Green	Red
B	Yellow	Red
C	Red	Red
D	Red	Green
E	Red	Yellow
F	Red	Red

According to this states the state diagram designed as in Figure 3.4.

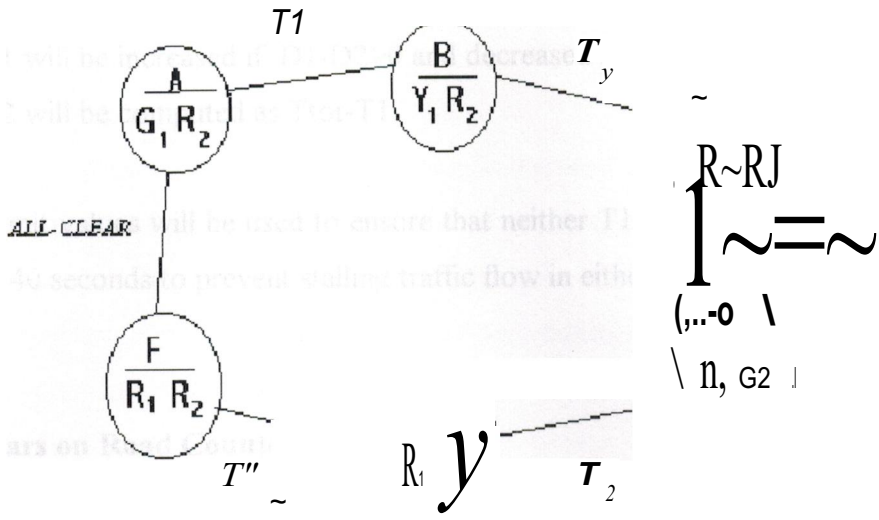

Figure 3.4 : State Diagram of the Circuit

3.2.2 Time-base Oscillator

The time oscillator will generate a clock signal that will be used to compute the times at which lights will be switched. Assume 10-second yellow light period will be the shortest event in this system. All other switching times *will* be computed as multiples of 10 sec.

The amount of green light time allocated to each direction will be recomputed every 5 minutes therefore the oscillator will increment a counter that will be used to generate a pulse every 5 minutes.

3.2.3 Green Time Allocation Circuit

This module will re-compute the green light durations T1 and T2 at the end of each 5 minute period based on the output of the traffic counter.

D1 : Traffic count in direction 1

D2 : Traffic count in direction 2

Tl will be increased if Dl-D2>0 and decreased if Dl-D2<0.

T2 will be computed as Ttot-Tl.

Limit values will be used to ensure that neither Tl or T2 drop below a minimum period of 40 seconds to prevent stalling traffic flow in either direction.

3.2.4 Cars on Road Counter

To determine whether cars remain on the road prior to activating a green light a counter will be used to compute the difference between the number of cars entering the road Ne and the number cars leaving the road NI. The road is assumed to be all clear whenever

Ne-Nl=0.

An up/down counter will be used that will be incremented by pulses from sensor S1 and decremented by pulses from sensor S2. a counter output signal will indicate the condition

Ne-Nl=0.

3.2.5 Traffic Counter

To determine the relative amount of green light time allocated to each direction a counter will be used to compute the difference the numbers of cars traversing the read in each direction. The traffic counter will be incremented by cars moving in one direction and decremented by cars moving in the opposite direction. Pulses form S1 will be used in both cases. The count will be sampled every 5 minutes signaled by a pulse from the time base oscillator after which the counter will be reset to zero to begin the next 5 minutes period. Electronic circuit of traffic counter is shown bellow. Now let us see the circuit.

CONCLUSION

In this project we used fourth-seven integrated circuit. Cost of this project is about a hundred million TL. So that this is to much expensive way ; .Also as you see before this project is so complicated and difficult to setup as you see. To decrease the cost and complexity we can use a microprocessor controlled circuit. For this job a 8085 microprocessor and 8155 PIO card will be enough. By writing simple assembly program we can control all of these jobs.

For future application of this project, we can apply this circuit for the connection point of the four road by making some changes of the circuit. So this project can be expandable and useful for the signalization of the bridges or roads.

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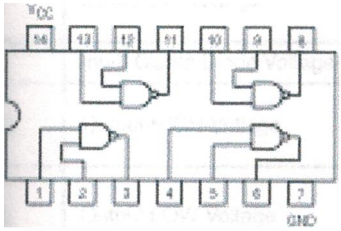

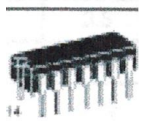

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ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
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ED OPERATING RANGES

	Parameter
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	Output Current — High
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-DtARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
VIL	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	Vee= MIN, I1N =-18 mA	
VOH	Output HIGH Voltage	54	2.5	3.5		V	Vee= MIN, IoH = MAX, VIN = VIH or VIL per Truth Table	
		74	2.7	3.5		V		
VOL	Output LOW Voltage	54, 74		0.25	0.4	V	IoL=4.0 mA	Vee= Vee MIN, VIN = VIL or VIH per Truth Table
		74		0.35	0.5	V	'01, =8.0 mA	
IIH	Input HIGH Current				20	µA	Vee= MAX, VIN = 2.7 V	
					0.1	mA	Vee = MAX, VIN = 7.0 V	
IIL	Input LOW Current				-0.4	mA	Vee= MAX, VIN = 0.4 V	
IOS	Short Circuit Current (Note 1)		-20		-100	mA	Vee =MAX	
ICC	Power Supply Current Total, Output HIGH				1.6	mA	Vcc=MAX	
	Total, Output LOW				4.4			

,t more than one output should be shorted at a time, nor for more than 1 second.

RACTERISTICS (TA = 25°C)

Spiibol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
tPLH	Turn-Off Delay, Input to Output		9.0	15	ns	Vee =5.o V CL=15pF
tPHL	Turn-On Delay, Input to Output		10	15	ns	

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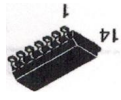

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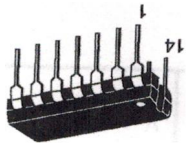

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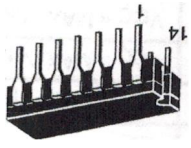

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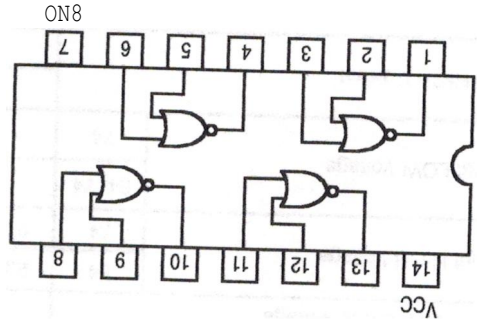

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IC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

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~	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
'L.	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
~	Input Clamp Diode Voltage			-0.65	-1.5	V	Vee= MIN, I1N =-18 mA
~	Output HIGH Voltage	54	2.5	3.5		V	Vee= MIN, IoH = MAX, VIN = VIH or VIL per Truth Table
		74	2.7	3.5		V	
~	Output LOW Voltage	54, 74		0.25	0.4	V	IOL =4.0 mA; Vee= Vee MIN, VIN = VIL or VIH per Truth Table
		74		0.35	0.5	V	IoL =8.0 mA
~	Input HIGH Current				20	µA	Vee= MAX, VIN = 2.7 V
					0.1	mA	Vee= MAX, VIN = 7.0 V
~	Input LOW Current				-0.4	mA	Vee= MAX, VIN = 0.4 V
lice,	Short Circuit Current (Note 1)		-20		-100	mA	Vee= MAX
~	Power Supply Current Total, Output HIGH				3.2	mA	Vcc=MAX
	Total, Output LOW				5.4		

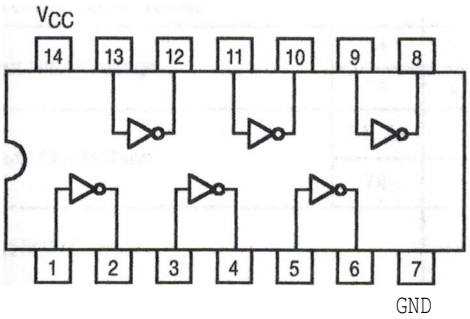
• • 'IC1 more than one output should be shorted at a time, nor for more than 1 second.

S CHARACTERISTICS (TA = 25°C)

-.II-OI	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
II._;;;	Turn-Off Delay, Input to Output		10	15	ns	Vee= 5.o v CL= 15 pF
~	Turn-On Delay, Input to Output		10	15	ns	

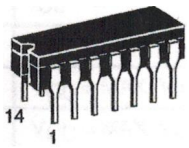
HEX INVERTER

SN54/74LS04



HEX INVERTER

LOW POWER SCHOTTKY



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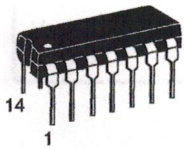
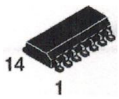
CASE 632-08



NSUFFIX
PLASTIC
CASE 646-06



DSUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74				V
T_A	Operating Ambient Temperature Range	54 74	-55 0		125 70	
I_{OH}	Output Current — High	54, 74				
I_{OL}	Output Current - Low					mA

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions
	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
	Input Clamp Diode Voltage			-0.65	-1.5	V	Vee= MIN, IIN =-18 mA
	Output HIGH Voltage	54	2.5	3.5		V	Vee= MIN, IoH = MAX, VIN = VIH or VIL per Truth Table
		74	2.7	3.5		V	
	Output LOW Voltage	54, 74		0.25	0.4	V	IOI. = 4.0 rnA Vee= Vee MIN, VIN = VIL or VIH per Truth Table
		74		0.35	0.5	V	IoL=8.0mA
	Input HIGH Current				20	µA	Vee= MAX, VIN = 2.7 V
					0.1	mA	Vee= MAX, VIN = 7.0 V
	Input LOW Current				-0.4	mA	Vee= MAX, VIN = 0.4 V
	Short Circuit Current (Note 1)		-20		-100	rnA	Vcc=MAX
	Power Supply Current Total, Output HIGH				2.4	mA	Vcc=MAX
	Total, Output LOW				6.6		

'Ct more than one output should be shorted at a time, nor for more than 1 second.

OiARACTERISTICS (TA= 25°C)

	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
	Turn-Off Delay, Input to Output		9.0	15	ns	Vee =5.o V CL=15pF
	Turn-On Delay, Input to Output		10	15	ns	

CTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
L	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
	Input Clamp Diode Voltage			-0.65	-1.5	V	Vee= MIN, I1N = -18 mA	
	Output HIGH Voltage	54	2.5	3.5		V	Vee= MIN, IoH = MAX, VIN = VIH or VIL per Truth Table	
		74	2.7	3.5		V		
I.	Output LOW Voltage	54, 74		0.25	0.4	V	t01. =4.0 mA	Vee= Vee MIN, V1N = VIL or VIH per Truth Table
		74		0.35	0.5	V	IoL=8.0 mA	
	Input HIGH Current				20	µA	Vee= MAX, VIN = 2.7 V	
					0.1	mA	Vee= MAX, VIN = 7.0 V	
	Input LOW Current				-0.4	mA	Vee= MAX, VIN = 0.4 V	
	Short Circuit Current (Note 1)		-20		-100	mA	Vee= MAX	
c;	Power Supply Current Total, Output HIGH				4.8	mA	Vcc=MAX	
	Total, Output LOW				8.8			

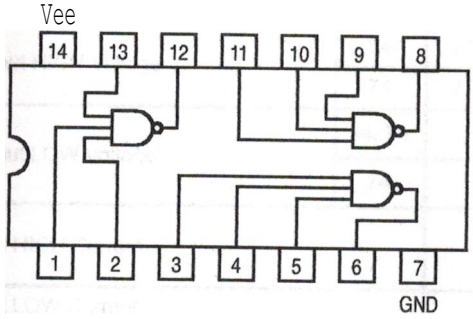
-.ore than one output should be shorted at a time, nor for more than 1 second.

ARACTERISTICS (T_A = 25°C)

	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
	Turn-Off Delay, Input to Output		8.0	15	ns	Vee= 5.o V CL=15pF
	Turn-On Delay, Input to Output		10	20	ns	

SN54/74LS10

TRIPLE 3-INPUT NANO GATE



TRIPLE 3-INPUT NANO GATE

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08

NSUFFIX
PLASTIC
CASE 646-06

DSUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current - High	54, 74			-0.4	mA
I_{OL}	Output Current - Low	54			4.0	mA
		74			8.0	

CTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
Input LOW *Voltage*	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
	74			0.8			
Input Clamp Diode Voltage			-0.65	-1.5	V	Vee= MIN, I1N =-18 mA	
Output HIGH *Voltage*	54	2.5	3.5		V	Vee= MIN, IoH = MAX, VIN = VIH or VIL per Truth Table	
	74	2.7	3.5		V		
Output LOW Voltage	54, 74		0.25	0.4	*V*	IoL=4.0 mA	*Vee*= Vee MIN, VIN = VIL or VIH per Truth Table
	74		0.35	0.5	V	I0I. = 8.0 mA	
Input HIGH Current				20	µA	Vee= MAX, VIN = 2.7 V	
				0.1	mA	*Vee*= MAX, VIN = 7.0 *V*	
Input LOW Current				-0.4	mA	Vee= MAX, VIN = 0.4 V	
Short Circuit Current (Note 1)		-20		-100	mA	Vee= MAX	
Power Supply Current Total, Output HIGH				1.2	mA	Vcc=MAX	
Total, Output LOW				3.3			

-.ore than one output should be shorted at a time, nor for more than 1 second.

~vii::nii:Jiiv..;;,\iA-c..vvi

Parameter	Limits Min	Typ	Max	Unit	Test Conditions
Turn-Off Delay, Input to Output		9.0	15	ns	Vee= 5.o V CL=15pF
Turn-On Delay, Input to Output		10	15	ns	

SDLS100

SN5432, SN64LS32, SN54S32, SN7432, SN74LS32, SN74S32 QUADRUPLE 2-INPUT POSITIVE-OR GATES.

DECEMBER1983 -REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic D1Ps
- Dependable Texas Instruments Quality and Reliability

description

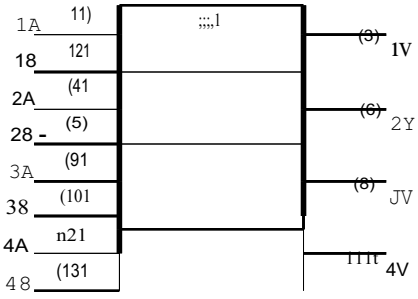
These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125cc. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0 cc to 70 cc.

FUNCTION TABLE (each gatel

INPUTS		OUTPUT
A	B	y
H	X	ti
X	H	H
L	L	L

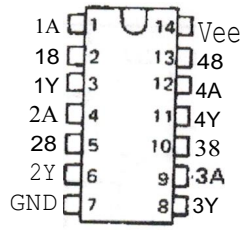
logic symbol t



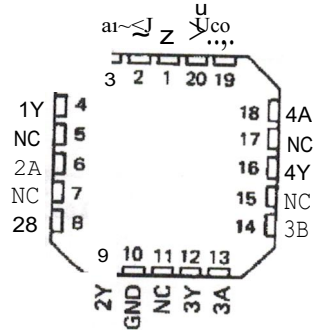
· This symbol is in accordance w•th ANSI:IEEE Std 91 · 1 984 and IEC Publication 617-12.

"ın numbers shown are for D. J. N. or W packages.

SN5432, SN54LS32, SN54S32 ... J OR W PACKAGE
SN7432 ... N PACKAGE
SN74LS32, SN74S32 ... D OR N PACKAGE
(TOP VIEWI

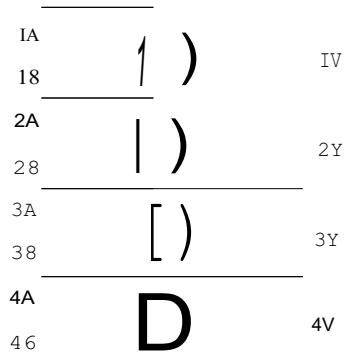


SN64LS32, SN54S32 ... FK PACKAGE
ITOP VIEW)



NC - No internal connection

logic diagram

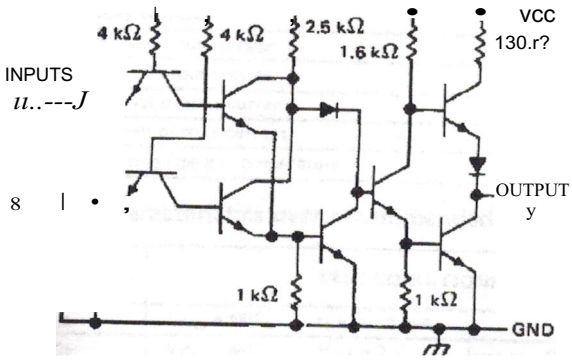


positive logic

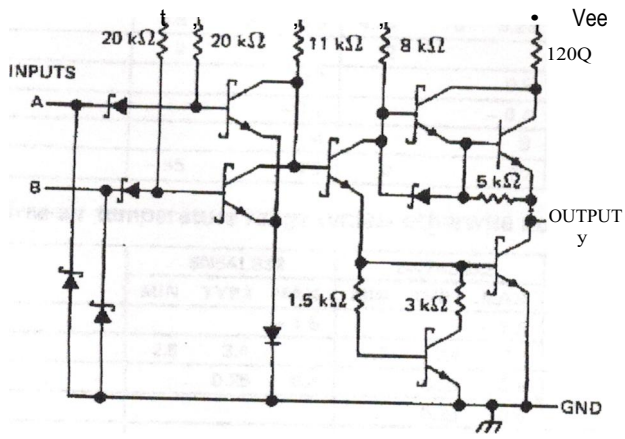
Y = A + B or Y = A • li

schematics (each gate)

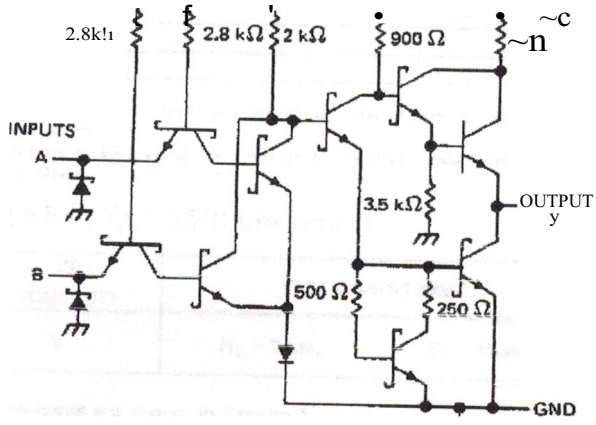
'32



'LS32



'S3Z



Resistor values shown are nominal.

ı,$0/ute maximum ratings over operating free-air temperature range (unless otherwise noted}

Supply voltage, Vee(~ Note 1)	7 V
input voltage: '32, 'S32	5.5 V
'LS32	7 V
ôperating tree-air temperature: SN54'	-55"C to 125.ıC
SN74'	0₀C to 70°C
Storage temperature range	-65 "C to 1.50°c

NOTE 1: Voltage values are with respect to network ground terminal.

ıecommended operating conditions

		SN64S32			SN74S32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
'rIH	High-levelinput voltage	2			2			V
.-IL	Low-levelinput voltage			0.B			0.S	V
·C-I	High-lı,vı,Ioutput current			-1			-1	mA
-:>L	Low-lıiveloutput current			20			20	mA
4	Operating free-air temperature	-55		125	0		70	<>c

ieaı characteristics over recommenr.fed operating free-air temperature range (unless otherwise noted)

JIIARAMETER	TEST CONDITIONS t			SN54S32			SN74S32			UNIT
				MIN	ryp;	MAX	MIN	TVP1	MAX	
VıK	VCC= MIN,	11 =-18 mA				-1.2			1.2	V
VoH	Vee= MIN.	VıH=2V.	IQH =- I mA	2.5	3.4		2.7	3.4		V
VoL	Vcc=MIN,	V1L•0.8V,	IOL = 20 mA			0.5			0.5	V
Iı	Vee •MAX,	Vı •5.5 V				1			1	mA
I1H	Vee •MAX,	Vı =2.7 V				50			50	„A
Iu,	Vee =MAX,	Vı -o.s v				−2			−2	mA
ıos§	Vee• MAX			-40		-100	-40		-100	mA
leCH	VCC> MAX,	See Nete 2			18	32		18	32	mA
'CCI,	Vee= MAX.	Vı m OV			38	68		38	es	mA

For condition••lıown N MIN or MAX, uu tlıe appropriato valua op..,lfled under racommended nceratlng conditionı.
t All typical vah.ı• nre et Vee - S V, TA - 25°c.
ot more the" o"e output ıhould be shorted •t • time ar,d the duratio,ı of th• thort-elrcult ohould not •ı<ceedone ıecond.
CTe 2: Ona inıiur Bt4.1)v •• ll Others It GND.

·· hing characteristics, Vee = 5 V, TA = 25° C (sea note 3)

PARAMETER	FROM IINPUTI	TO IOUTPUTI	TEST CONCITIONS		MIN	TVP	MAX	UNIT
'l>LH	A or B	y	RL =2B0n,	CL•15pF		4	7	nı
tPHL						4	7	ns
lPLH	Aor 8	y	RL ~ 280!2,	CL• 50 pF		5		ns
tPHL						6		ns

iTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54/74LS85

IT MAGNITUDE MPARATOR

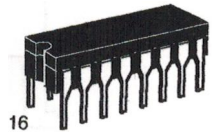
SN54/74LS85 is a 4-Bit Magnitude Camparator which compares two lllliihıorrts (A, B), each word having four Parallel Inputs (Ao-A3, Bo-B3); A3, the most significant inputs. Operation is not restricted to binary the device will work with any monotonic code. Three Outputs are : "A greater than B" (OA> B), "A less than B" (OA< s), "A equal to B" -s). Three Expander Inputs, IA> B, IA< B, IA= B, allow cascading without gates. For proper compare operation, the Expander Inputs to the ı...r.sıgnificant position must be connected as follows: IA< S= IA> B = L, IA= B ---serial (ripple) expansion, the OA>B, OA<B and OA=B Outputs are ed respectively to the IA>B, IA<B, and IA=B Inputs of the next most tcarıt comparator, as shown in Figure 1. Refer to Applications section of saeet for high speed method of comparing large words.

Truth Table on the following page describes the operation of the 74LS85 under all possible logic conditions. The upper 11 lines describe al operation under all conditions that will occur in a single device or series expansion scheme. The lower five lines describe the operation abnormal conditions on the cascading inputs. These conditions occur e parallel expansion technique is used.

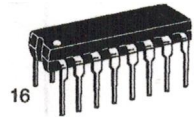
Expandable
ary or BCD Comparison
>8, OA<B, and OA=B Outputs Available

4-BIT MAGNITUDE COMPARATOR

LOW POWER SCHOTTKY



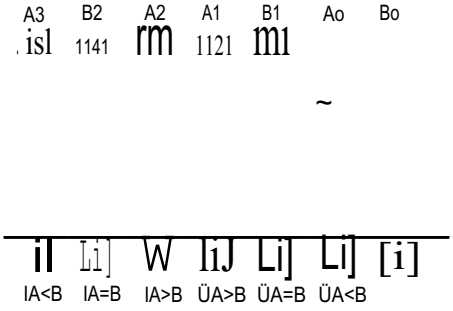
J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

O SUFFIX
SOIC
CASE 751B-03

CONNECTION DIAGRAM DIP (TOP VIEW)

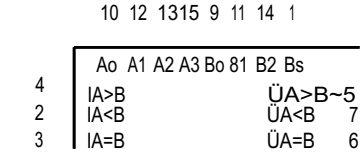


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL

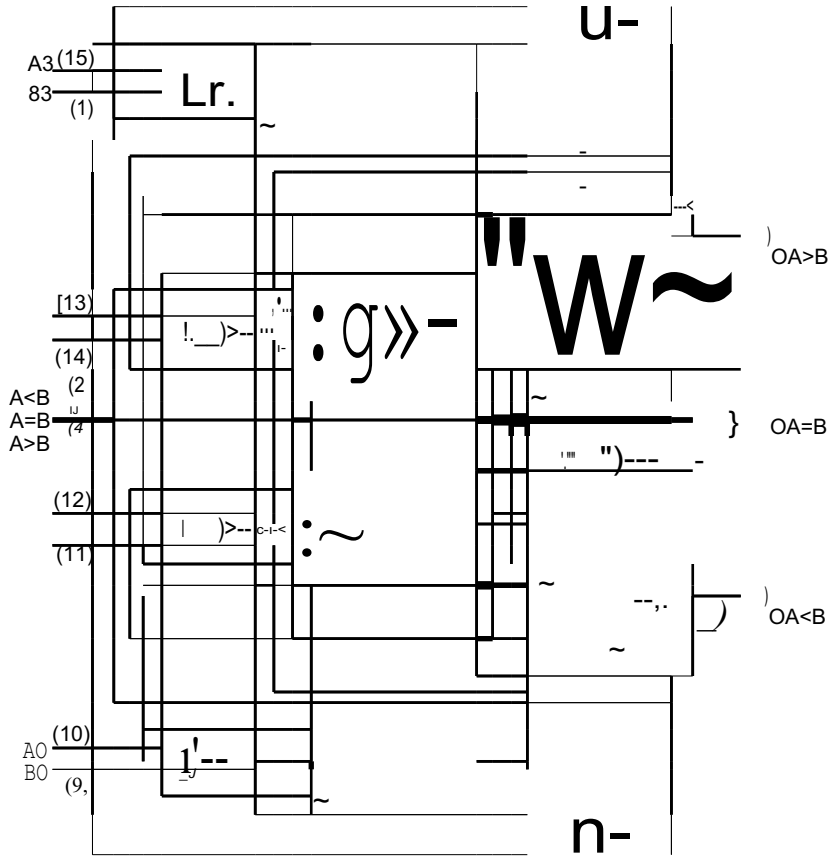


Vcc=PIN 16
GND=PIN8

NAMES

		LOADING (Note a)	
		HIGH	LOW
-A3, Bo-B3	Parallel Inputs	1.5 U.L.	0.75 U.L.
=B	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
<B, IA>B	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
A>B	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
A<B	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
A=B	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

=S:
"Tl, Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
--e Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) -~rature Ranges.



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,83	A2,B2	A1,B1	Ao,Bo	IA>B	IA<B	IA=B	0A>B	0A<B	OA=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=83	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	Ao>Bo	X	X	X	H	L	L
~=83	A2=B2	A1=B1	Ao<Bo	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	Ao=Bo	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	Ao=Bo	L	H	L	L	H	L
~=83	A2=B2	A1=B1	Ao=Bo	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	Ao=Bo	H	H	L	L	L	L
A3=B::ı	A2=B2	A1=B1	An=Bo	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

ED OPERATING RANGES

Parameter		Min	Typ	Max	Unit
Supply Voltage			5.0 5.0	5.5 5.25	V
Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	0C
Output Current - High	54, 74			-0.4	mA
Output Current - Low	54 74			4.0 8.0	mA

F-8 DECODER/ ULTIPLEXER

SN54/74LS138

a high speed 1-of-8 Decoder / III-IIIoexer. This device is ideally suited for high speed bipolar memory ~ address decoding. The multiple input enables allow parallel ex- a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 .:ısing four LS 138s and one inverter. The LS 138 is fabricated with the carrier diode process for high speed and is completely compatible torola TIL families.

E ·pıexing Capability
Input Enable for Easy Expansion
Power Dissipation of 32 mW
e Low Mutually Exclusive Outputs
Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)

02 03 04 05 05
131 1121 Gil

~

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

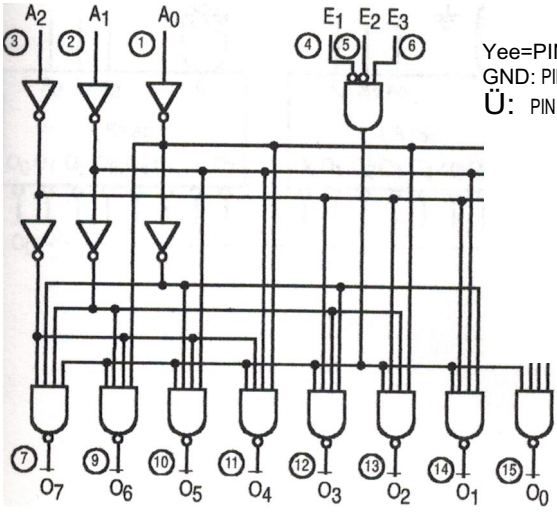
iJli.JWWW WJ
A1 A2 E1 E2 E3 07 GND

NAMES

	LOADING (Note a)	
	HIGH	LOW
Address Inputs	0.5 U.L.	0.25 U.L.
Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

-- Jnit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
:Julput LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) -ature Ranges.

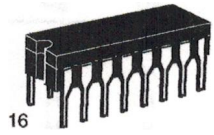
DIAGRAM



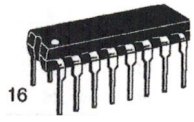
Yee=PIN 16
GND: PIN 8
Ü: PIN NUMBERS

1-0F-8 DECODER/ DEMULTIPLEXER

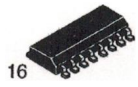
LOW POWER SCHOTIKY



J SUFFIX
CERAMIC
CASE 620-09



NSUFFIX
PLASTIC
CASE 648-08

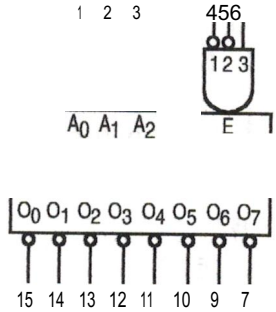


O SUFFIX
SOIC
CASE 751 8-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



Vee: PIN 16
GND: PINS

~L DESCRIPTION

38 is a high speed 1-of-8 Decoder/Demultiplexer fth the low power Schottky barrier diode process. eraccepts three binary weighted inputs {Ao, A1, A2) enabled ınovides eight mutually exclusive active {Oo-07}_, Ttıe LS138 features three Enable indive LOW (E1, E2)_andone active HIGH (E3). All be HIGH unless E1 and E2 are LOW and E3 is s multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS					OUTPUTS							
E2	E3	Ao	A1	A2	Oo	01	02	03	04	05	05	0-,
X	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
L	H	H	L	L	H	L	H	H	H	H	H	H
L	H	L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	L	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

age Level
ge Level

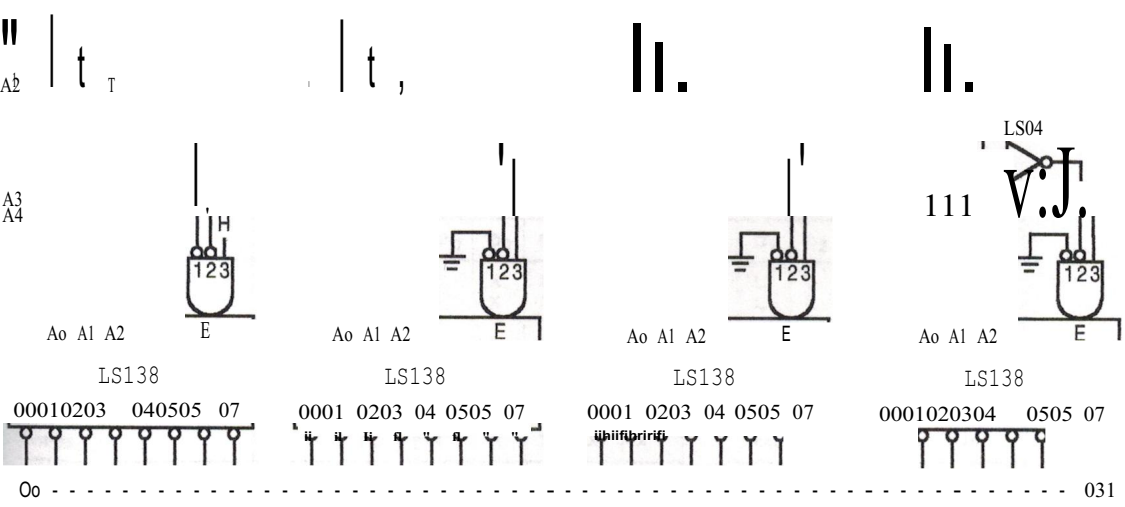
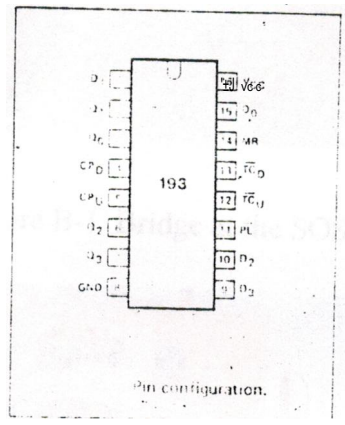


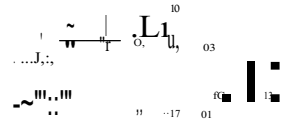
Figure a

A.9 – 74LS193 (4 – Bit Preprogrammable Binnary Ripple Counter)

PIN NO.	SYMBOL	NAME .'I.NO FUNCTION
3, 2, 6, 7	~)0 to G3	flip-fieμ outputs
4	CPo	count down ctocx input·
5	CPu	count uo clock input ii
8	GND	3round \OV}
11	$\overline{PL}$	asynchronous μaraliei load input !active LOW)
12·	$\overline{TC_U}$	terminal count up !c.ırry) output !active LOW)
13	$\overline{TC_D}$	terminal count down (borrow) output (actıve LOW)
14	MR	asvncnronousmasterresetinput {active HIGH)
15, 1 10, 9	Do to 03	data inputs
16	V_{CC}	--·----~ositive :~uupıyv~lt.1ge



Pin configuration.



Logic symbol.

OPERATING MODE	INPUTS								OUTPUTS					
	MR	PT	CPu	CPo	D0	D1	D2	D3	Q0	Q1	Q2	Q3	TCU	TCD
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	L	H
	H	X	X	H	X	X	X	X	L	L	L	L	L	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H		H	X	X	X	X	count up				H*	H
Count down	L	HJH			X	X	X	X	count-down				H	H**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

•. Teu = C?u at terminal count up \HHHH) "·
•• .~Q = CPo at terminal count aown ! LLLLI

ENDIX - B One-line road photos

Figure B-1 Bridge at the SOSYAL KONUTLAR, Nicosia

Figure B-2 Bridge at the SOSYAL KONUTLAR, Nicosia

Figure B-3 Bridge at the MARMARA, Nicosia

APPENDIX - B The Circuit :