NEAR EAST UNIVERSITY

Faculty of Engineering

Department of Electrical and Electronic Engineering

LAMP CHASER CIRCUIT DESIGN WITH POWER ELECTRONICS COMPONENTS

GRADUATION PROJECT
EE- 400

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I do not want to specialize and write a name of any of my dear friends in case of forgetting any of them, so I want to thank them all because they were always my brothers during my study period in NEU.

Finally, I want to thank my family especially my parents. Without their endless support and love for me, I would never achieve my current position. I really want to thank my brothers Ibraheem, Mohammed, and sammer from the bottom of my heart. I wish my mother lives happily always, and my father in heaven be proud of me.

ABSTRACT

To make sure of understanding this project you need to know: What is power electronics?

Power electronics is the application of electronic circuits to energy conversion. You may have more interaction with power electronics than you think. If you drive a car, use a computer, cook with a microwave, talk on any type of telephone, listen to a stereo, or make holes with a cordless drill, then you come in contact with power electronics. Thanks to power electronics, the electricity needed to run the things you use everyday is processed, filtered, and delivered with maximum efficiency, smallest size and minimal weight. In formal terms,

"This technology encompasses the use of electronic components, the application of circuit theory and design techniques, and the development of analytical tools toward efficient electronic conversion, control, and conditioning of electric power."

Power electronics is everywhere you look. For example, power electronics is used in

- Computers
- Automobiles
- Telecommunications
- Space systems and satellites
- Motors
- Lighting
- Alternative energy (like solar and wind).

In this project the power electronics elements were essential and successful to provide a lamp chaser circuit, and make its operation goes directly to the aim that it has built for. That aim was performed by using thyristors and transistors, depending upon them characteristics of providing the time delay functioning with association and presentation of the capacitors and the resistors.

TABLE OF CONTENTS

INTRODUCTION

Power electronics is a critical technology for a vast array of applications including transportation, telecommunications, robotics and automation, and electronic equipment of all types. The primary function of power electronic circuits is the processing and control of electrical energy. Such circuits enable unprecedented control over physical systems, resulting in levels of functionality, performance, and efficiency that are not attainable otherwise.

Power semiconductor devices are at the heart of power electronics circuits. Overall system reliability and efficiency depend on the quality of semiconductor switches and how these devices are used. Throughout the last 50 years, power electronics technology mostly evolved with the availability of new and improved power semiconductor devices. In the past few years, device technology has made tremendous progress. High power bipolar transistors have become mature products and have been used for many applications such as motor drives, uninterruptible power supplies(UPS), and solid-state relays.

Chaser circuits are based on power electronics to occur and do its subjected jobs.

Lamp chasers are circuits in which a number of lights are arranged so that they turn on sequentially, with present time delay between each operation (lamp control circuit), until they finally on together. See the following examples for the lamp chaser circuits.

CHAPTER 1

POWER ELECTRONICS AND LAMP CHASER CIRCUITS

1.1. Introduction to Power Electronics

1.1.1. Definition

Power electronics refers to control and conversion of electrical power by power semiconductor devices wherein these devices operate as switches. Advent of silicon-controlled rectifiers, abbreviated as SCRs, led to the development of a new area of application called the power electronics. Prior to the introduction of SCRs, mercury-arc rectifiers were used for controlling electrical power, but such rectifier circuits were part of industrial electronics and the scope for applications of mercury-arc rectifiers was limited. Once the SCRs were available, the application area spread to many fields such as drives, power supplies, aviation electronics, high frequency inverters and power electronics originated.

1.1.2. Main Task of Power Electronics

Power electronics has applications that span the whole field of electrical power systems, with the power range of these applications extending from a few VA/Watts to several MVA / MW.

The main task of power electronics is to control and convert electrical power from one form to another. The four main forms of conversion are:

- Rectification referring to conversion of ac voltage to dc voltage,
- DC-to-AC conversion,
- DC-to DC conversion and
- AC-to-AC conversion.

"Electronic power converter" is the term that is used to refer to a power electronic circuit that converts voltage and current from one form to another. These converters can be classified as:

- Rectifier converting an ac voltage to a dc voltage,
- Inverter converting a dc voltage to an ac voltage,
- Chopper or a switch-mode power supply that converts a dc voltage to another dc voltage, and
- Cycloconverter and cycloinverter converting an ac voltage to another ac voltage.

In addition, SCRs and other power semiconductor devices are used as static switches.

1.2. Semiconductors

A semiconductor is a substance, usually a solid chemical element or compound; hat can conduct electricity under some conditions but not others, making it a good medium for the control of electrical current. Its conductance varies depending on the current or voltage applied to a control electrode, or on the intensity of irradiation by infrared (IR), visible light, ultraviolet (UV), or X rays.

The specific properties of a semiconductor depend on the impurities, or depart, added to it. An N-type semiconductor carries current mainly in the form of negatively-charged electrons, in a manner similar to the conduction of current in a wire. A *P-type* semiconductor carries current predominantly as electron deficiencies called holes. A hole has a positive electric charge, equal and opposite to the charge on an electron. In a semiconductor material, the flow of holes occurs in a direction opposite to the flow of electrons.

Elemental semiconductors include antimony, arsenic, boron, carbon, germanium, selenium, silicon, sulfur, and tellurium. silicon is the best-known of these, forming the basis of most integrated circuits (ICs). Common semiconductor compounds include gallium arsenide, indium antimonide, and the oxides of most metals. Of these, gallium arsenide (GaAs) is widely used in low-noise, high-gain, weak-signal amplifying devices.

A semiconductor device can perform the function of a vacuum tube having hundreds of times its volume. A single integrated circuit (IC), such as a microprocessor chip, can do the work of a set of vacuum tubes that would fill a large building and require its own electric generating plant.

1.3. Lamp Chaser

Lamp chasers are circuits in which a number of lights are arranged so that they turn on sequentially, with present time delay between each operation (lamp control circuit) , until they finally on together . See the following examples for the lamp chaser circuits:

1.3.1. Chaser

The chaser was developed out of an urgent need by one of the directors of a show I was involved in. It was designed, de-bugged and constructed in a single evening because the director wouldn't take no for an answer. Consequently, it is simple in the extreme but still effective.

It is based on a CMOS 4017 decade counter, forced to reset at the nine count and resume from count 1. There are eight steps in each cycle before it repeats itself. Outputs are routed through the usual diode-coupled precedence hook-up. Input is either from the bass-beat extractor or from the free-run oscillator.

The circuit uses transistors to buffer the outputs from the CMOS counter. This is done for two reasons. Firstly, the output current from a CMOS IC is not great, and secondly the buffers provide protection from external static fields, which will damage a CMOS device instantly. All transistors are BC548 or similar (e.g. 2N2222), and diodes are 1N4148, resistors are 1/4W. Capacitors should be rated at 25V minimum.

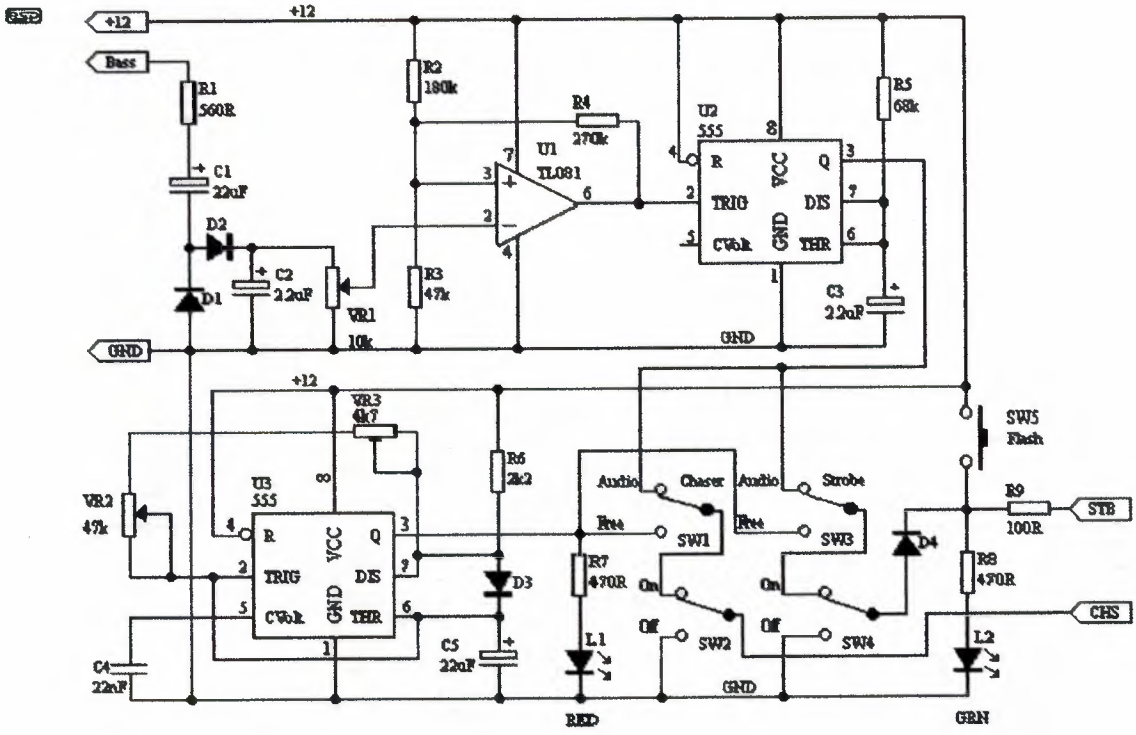


Figure 1.2 Strobe and Chaser Controller

The first section is used to capture the bass peaks. The sensitivity of the bass beat extractor is adjusted with VR1. The free running oscillator is based on U3, a 555 timer. The speed is controlled by VR2, and VR3 (a trimpot) is used to set the maximum frequency. The switching determines if the strobe and/or chaser are controlled by the oscillator or the bass beat, and each is independently selectable. The signal to either can also be switched off entirely. The Flash button is used to create a single strobe flash - really useful for creating lightning effects. Diodes are 1N4148, resistors are 1/4W. Capacitors should be rated at 25V minimum.

1.3.3. 120VAC Lamp Chaser

This circuit is basically the same as the 10 channel LED sequencer with the addition of solid state relays to control the AC lamps. The relay shown in the diagram is a Radio Shack 3 amp unit (part no. 275-310) that requires 1.2 volts DC to activate. No current spec was given but I assume it needs just a few milliamps to light the internal LED. A 360 ohm resistor is shown which would limit the current to 17 mA using a 9 volt supply. I tested the circuit using a solid state relay (of unknown type) which required only 1.5 mA at 3 volts but operates up to 30 volts DC and a much higher current. The chaser circuit can be expanded up to 10 channels with additional relays and driver

transistors. The 4017 decade counter reset line (pin 15) is connected to the fifth count (pin 10) so that the lamps sequence from 1 to 4 and then repeat. For additional stages the reset pin would be connected to a higher count.

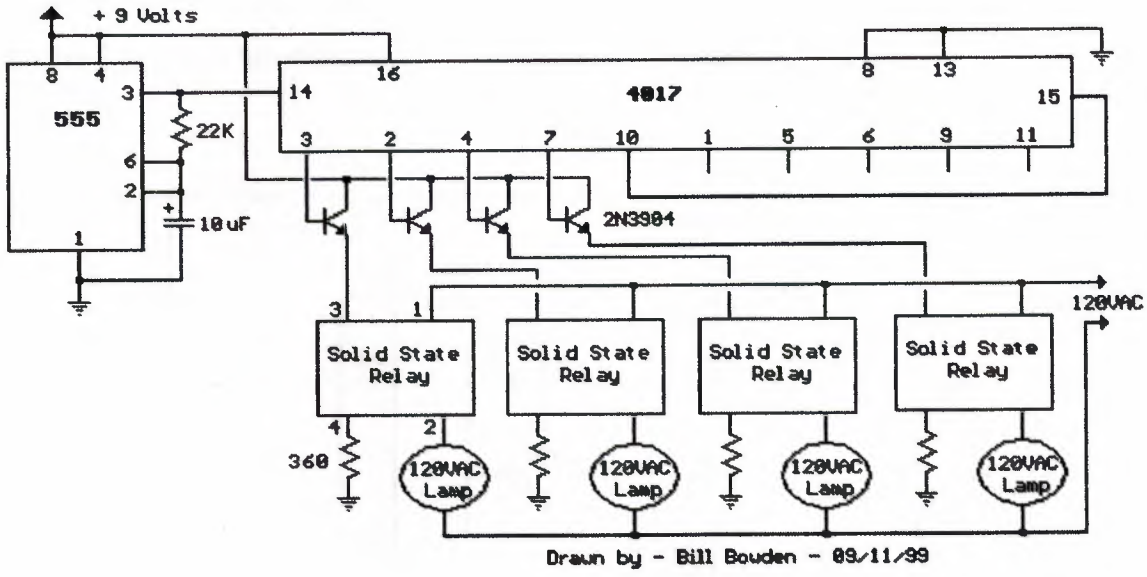


Figure1.3 120VAC Lamp Chaser

1.4. D.C. LAMP CHASER PROJECT

1.4.1. Circuit Descriptions

Normally, switch S_1 open, all lamps and s.c.r.s are off, and all capacitors are discharged. When S_1 is first closed power is applied to lamp1 and to Q1 u.j.t time delay circuit, and C_1 starts to charge exponentially via R_1. Note at this stage that all s.c.r.s are off, so zero power is applied to Q2 or Q3 networks. After a preset delay C_1 reaches the firing voltage of Q1, and Q1 fires and applies trigger pulse to the gate of SCR_1, and SCR_1 and lamp 2 turn on.

As lamp2 turns on it applies power to the Q2 u.j.t. time delay network. After another preset delay, therefore Q2 fires and turns $S.C.R_2$ and lamp3 on, and lamp3 applies power to Q3 and initiates a further timing period which culminates in the firing of $S.C.R._3$ and the turning on of lamp 4. The circuit action is then complete, and all lamps are finally on together. The circuit can extended incorporate as many lamps as required

by simply wiring in a u.j.t. time-delay and an s.c.r. network for each additional lamp stage. Figure (1-4) shows a practical d.c. lamp chaser.

Notice that the circuit built up using power electronics elements such as thyristors of kind (IR 106 Y1), and field effect transistors FET of kind (IR2160).

In addition we have 10$^{\mu}$F capacitors, resistors, and 12V lamps.

Chapter 2 contains full discussions about the circuit elements.

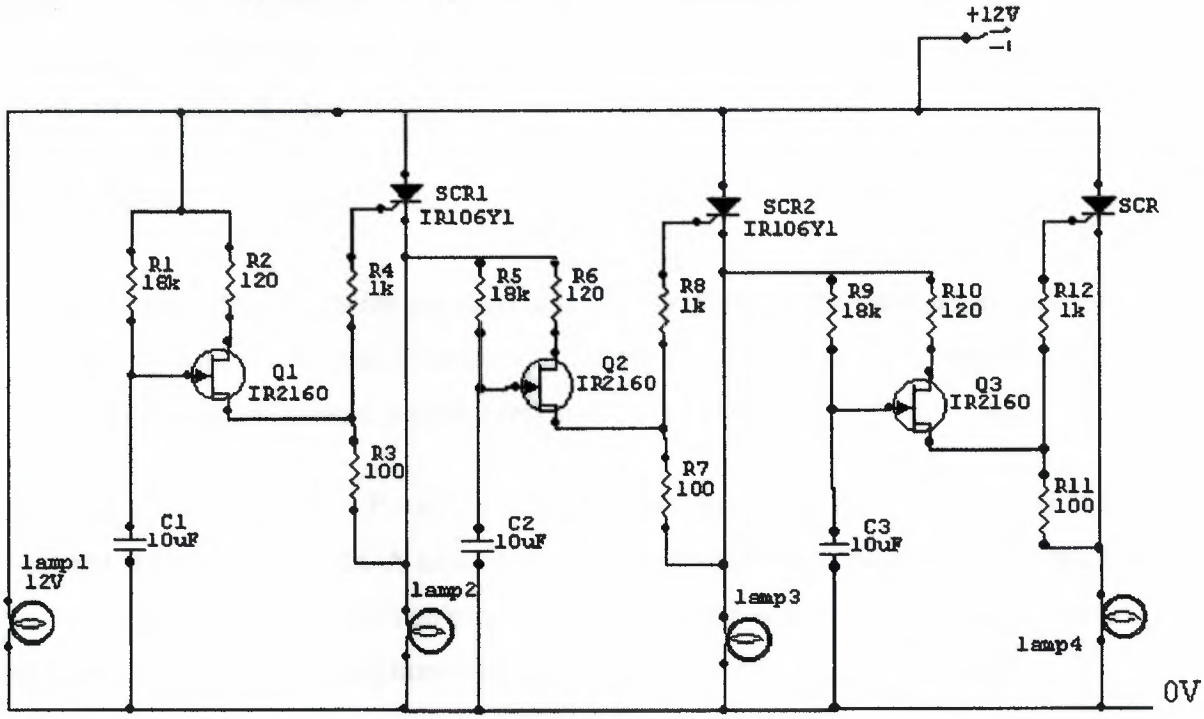


Figure 1.4 D.C lamp chaser. All lamps are 12V types with current rating less than 2A.

1.5. Capacitor

A capacitor is a passive electronic component that stores energy in the form of an electrostatic field. In its simplest form, a capacitor consists of two conducting plates separated by an insulating material called the dielectric. The capacitance is directly proportional to the surface areas of the plates, and is inversely proportional to the separation between the plates. Capacitance also depends on the dielectric constant of the substance separating the plates.

The standard unit of capacitance is the farad, abbreviated F. This is a large unit; more common units are the microfarad, abbreviated μF (1 μF = 10^{-6} F) and the picofarad, abbreviated pF (1 pF = 10^{-12} F).

Capacitors can be fabricated onto integrated circuit (IC) chips. They are commonly used in conjunction with transistors in dynamic random access memory (DRAM). The capacitors help maintain the contents of memory. Because of their tiny physical size, these components have low capacitance. They must be recharged thousands of times per second or the DRAM will lose its data.

Large capacitors are used in the power supplies of electronic equipment of all types, including computers and their peripherals. In these systems, the capacitors smooth out the rectified utility AC, providing pure, battery-like DC.1

1.5.1. Farad

The farad (symbolized F) is the standard unit of capacitance in the International System of Units (SI). Reduced to base SI units, one farad is the equivalent of one second to the fourth power ampere squared per kilogram per meter squared ($s^4 \cdot A^2 \cdot kg^{-1} \cdot m^{-2}$).

When the voltage across a 1 F capacitor changes at a rate of one volt per second (1 V/s), a current flow of 1 A results. A capacitance of 1 F produces 1 V of potential difference for an electric charge of one coulomb (1 C). The farad is an extremely large unit of capacitance. In practice, capacitors with values this large are almost never seen.

In common electrical and electronic circuits, units of microfarads (μF), where 1 μF = 10^{-6} F, and picofarads (pF), where 1 pF = 10^{-12} F, are used. At radio frequencies (RF), capacitances range from about 1 pF to 1,000 pF in tuned circuits, and from about 0.001 μF to 0.1 μF for blocking and bypassing. At audio frequencies (AF), capacitances range from about 0.1 μF to 100 μF. In power-supply filters, capacitances can be as high as 10,000 μF.

1.5.2. Capacitor Basics

A capacitor is an electronic component that is capable of storing energy for later release. The basic capacitor consists of two metallic plates that are isolated from each other by a non-conducting dielectric material.

When an electrical current is applied to the capacitor, the electrons in the current begin piling up on one of the metallic plates because they cannot pass through the non-

conducting dielectric material to reach the other metallic plate. The electron's negative charge repels an equal number of electrons from the opposite metallic plate. This continues until the voltage across the capacitor is equal to the applied voltage, and the current ceases flowing. The capacitor now is "charged" up with energy and will remain charged until a load is applied across the capacitor plates. The capacitor will then "discharge" its energy through the load until it reaches its original uncharged state.

1.5.3. What is Capacitance?

Capacitance is a measure of the energy that the capacitor is capable of storing. There are several internal construction factors that determine how much capacitance a given capacitor will have including: the size of the metallic plates, the composition of the dielectric material, and how close the metallic plates are to each other (thickness of dielectric material). Capacitance is measured in "farads" which were named for the eighteenth century English scientist Michael Faraday. A capacitor would have a capacitance of one farad if a one volt source charged it with one coulomb of electricity (six million trillion electrons). For most capacitors, a farad is not a practical unit of measurement because of its large value, so a majority of capacitors are measured in micro-farads (millionths of a farad, abbreviated uF), nano-farads (billionths of a farad, abbreviated nF), or pico-farads (trillionths of a farad, abbreviated pF). For example, a capacitor with a value of 2uF could also be written as $2x10^{-6}$ Farads, a capacitor with a value of 2nF would be $2x10^{-9}$ Farads, and a capacitor with a value of 2pF would be $2x10^{-12}$ Farads. Sometimes, a conversion between the units is required. A .03uF capacitor could also be written as 30nF, and a .6nF capacitor could also be written as 600pF.

1.5.4. Source Voltage - AC or DC ?

The description of the basic capacitor up to this point applies to direct current (DC) applications. DC voltage is the type of voltage produced by power sources such as batteries, where the electrical current only flows in one direction.

Capacitors behave differently in alternating current (AC) applications than in DC applications. For AC applications, the current changes polarity (switches direction) at some defined frequency rate. For example, U.S. households are supplied with 110 volt

AC current that changes polarity at a rate of 60 Hz (60 times a second). As the polarity of the AC current changes, the capacitor charges and then discharges following this change in polarity. From a circuit point of view, it appears that the AC current is being passed through the capacitor even though no electrons in the current actually pass through its dielectric material. This property is important for some applications.

1.5.5. Capacitor Types

Capacitors are classified in different ways. Some capacitors are grouped according to their dielectric material such as film and ceramic capacitors. Others are classified according to their plate material such as aluminum and tantalum capacitors. They are also grouped according to their application such as trimmer capacitors, motor start and run capacitors, and microwave capacitors.:

1.5.6. Variable Capacitors

Some applications require the ability to change the capacitor's capacitance value. Some of these applications require frequent capacitance changing while others do not. For example, a variable capacitor used in a radio tuning circuit needs to withstand frequent changing, while one used in a trimming application is usually adjusted only once to the required set point.

1.5.7. Fixed Capacitors

Fixed capacitors have capacitance values that cannot be physically adjusted. They can be divided into electrolytic, electrostatic, and electrochemical categories.

Electrolytic capacitors use either a solid or liquid electrolyte in their construction. Electrolytic capacitors have high capacitance values and offer the highest energy densities (most capacitance per case size). Electrolytic capacitors are inherently polar due to their construction, but non-polar ratings are available in some product classes. A polar capacitor can only handle current flow in only one direction.

Electrostatic capacitors use an insulating material in between the metallic plates to act as the dielectric material. Electrostatic capacitors have lower capacitance values than electrolytic capacitors, do not use an electrolyte, and are non-polar.

Electrochemical or Double Layer capacitors are a new type of capacitor that is just now being introduced in the marketplace. These capacitors are also known as ultra-capacitors or super-capacitors, because their capacitance values can measure as high as several hundred farads. These capacitors are being targeted toward battery assist applications such as cell phones and electric vehicles.

1.5.8. Capacitor Characteristics

The measurement of capacitance on most capacitor types is standardized throughout the industry. Capacitance is typically measured at 25°C on an electronic piece of equipment called a capacitance bridge. The frequency conditions under which capacitance is measured is typically 120Hz for electrolytic capacitors and 1KHz for electrostatic capacitors.

Manufacturers always specify capacitors with a nominal capacitance and a tolerance range. The tolerance range is a percentage of the nominal capacitance and can range from 1% to 50% (5%, 10%, and 20% are standard). For example, a capacitor that has a nominal capacitance rating of 10uF with a tolerance range of ± 10% could actually measure anywhere from 9uF to 11uF and still be within the capacitance specification limits.

Equivalent Series Resistance (ESR) is expressed in ohms (Ω) or milli-ohms (mΩ) and represents the capacitor's energy losses in terms of an equivalent single resistance in series with an ideal capacitor. ESR can be measured with a capacitance bridge. The ESR is frequency dependent, so the measurement frequency must also be specified.

Dissipation Factor (DF) is another way to represent the energy losses in the capacitor. It is expressed in percentage and can be measured with a capacitance bridge. DF is also frequency dependent.

If either DF or ESR is known for a capacitor, the other value can be calculated using one of the following formulas:

ESR (Ohms) = DF/(2*π*f*C*100) **or**
DF (%) = ESR*(2*π*f*C)*100
Where:

C= Capacitance in farads

f = Frequency at which the capacitance is measured

Power Factor (PF) is yet another way to represent the energy losses in a capacitor. It is typically used for AC capacitors such as motor start capacitors and represents the fraction of input power dissipated in the capacitor dielectric.

Working Voltage is the maximum voltage at which a capacitor can be continuously operated at a specified temperature. A capacitor can be rated for DC voltage (WVDC) and/or AC voltage (WVAC). Electrolytic capacitors are typically rated only for DC voltage, although motor start capacitors are rated for intermittent AC use. Electrostatic capacitors can be rated for either type of voltage, and some types are rated for both AC and DC voltages.

Capacitors may also have a surge voltage rating which includes the ripple voltage, power-line fluctuations, and transient voltages. Exceeding the rated surge voltage level may damage the capacitor and will usually void the manufacturer's warranty. Some capacitors must be "de-rated" at higher temperature levels. This means that the working voltage of the capacitor must be lower at these temperature levels. The manufacturer will provide these de-rating levels in table or graph form.

Capacitance Stability usually refers to how much the capacitance changes over the capacitor's rated temperature range. Electrolytic capacitors generally have good capacitance stability while the manufacturers of electrostatic capacitors often provide tables or graphs showing how much the capacitance will change over the temperature range.

Insulation Resistance is a measure of a capacitor's ability to retain a charge over time. An ideal capacitor would hold a charge forever or until it is discharged, but real capacitors always exhibit some kind of leakage behavior. Insulation resistance is most often specified for electrostatic capacitors and is measured in mega-ohms (MΩ) or as a time constant measured at MΩ - uF.

DC Leakage Current (DCL) is also a measure of a capacitor's ability to retain a charge over time. Leakage current is usually specified for electrolytic capacitors and is measured in milli-amps (mA) or micro-amps (uA).

Impedance (Z) represents the overall complex resistance a capacitor shows to the input voltage and is measured in Ohms (Ω) or milli-Ohms (mΩ). Impedance is the sum of the ESR and capacitive reactance (or inductive resistance). What is important to know about impedance is that it is frequency dependent and affects how the capacitor works in the circuit. Figure 1.4 shows a possible impedance curve for a capacitor. At frequencies less than the resonant frequency, the capacitor works as intended. For frequencies higher than the resonant frequency, the capacitor looks more like an inductor to the circuit. The shape of the impedance curve and the resonant frequency varies significantly among the different types of capacitors, so technical literature or technical personnel should be consulted if there is a frequency concern.

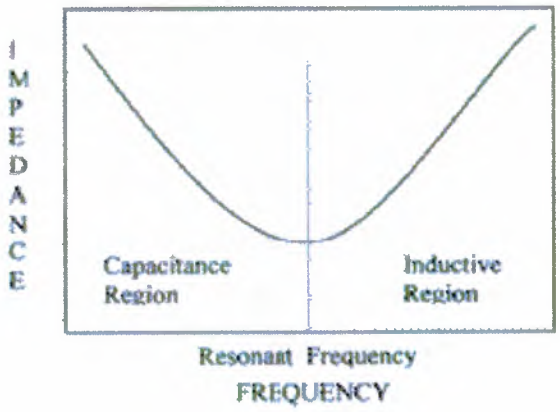


Figure 1.4 a possible impedance curve for a capacitor

1.5.9. Capacitor Applications

Capacitors are basically used one of three ways: to store and release energy, to discriminate between DC and AC current, or to discriminate between higher and lower AC frequencies. A basic description of the most popular applications is as follows:

Filtering is the smoothing out of pulsating DC current (ripple current) that comes from rectifying the AC current in a DC power supply application. Typically, capacitors and usually inductors are put on the input side of the circuit to supply ripple free current to the rest of the circuit. Almost all of the capacitor properties are important in this application including capacitance, working voltage, surge voltage rating, ripple current rating, and ESR. The working voltage of the capacitor should be great enough to handle

the combination of applied DC voltage, peak ripple voltage, surge voltages, and any voltage transients.

Bypassing is the use of a capacitor to keep the AC voltages out of portions of the circuit where they are not wanted. Important capacitor characteristics include the impedance frequency response and ESR. Aluminum electrolytics are commonly used for audio bypassing, but tantalum capacitors are used at higher frequencies. At very high frequencies, film, mica, and ceramic capacitors can be used.

Coupling is using a capacitor to block DC voltage. Once a capacitor is fully charged, it appears as an open circuit to DC voltage while passing audio or RF currents. Aluminum electrolytics can be used for audio and sub-audio de-coupling, and tantalum capacitors can be used for higher frequency coupling. In very low or very high frequency applications, electrostatic capacitors are typically used.

Tuning is the use of a capacitor and inductor to form a tuned circuit that discriminates sharply against all frequencies but the tuned (resonant) frequency. Capacitors in this application must have a high insulation resistance and very low ESR. Temperature-stable and compensating ceramics can be used in combination or with other capacitors.

Trimming is a special type of tuning in which trimming capacitors are used with the capacitor-inductor tuned circuit for better tuning control. Trimming capacitors specifically designed for this application are available.

Timing Circuits are used extensively in electronic design. Since it takes a finite amount of time to charge or discharge a capacitor, this characteristic can be used when timing is needed (i.e., delay three seconds before something happens). Important capacitor characteristics include capacitance and DC leakage. Small time delays can be serviced by electrostatic capacitors, and large time delays can be serviced by electrolytic capacitors. If the time delay needs to be critically controlled, capacitors designed for low DCL values should be used.

Energy Storage applications are ones in which a brief pulse of energy from a capacitor is required. The main requirement for this application is a high capacitance value, so electrolytic capacitors are commonly used. This is one application area where electrochemical capacitors may also eventually be used.

Application Specific capacitors are available for applications typically titled: motor start, motor run, spark arrestors (ceramic), X type filter (ceramic), X1-Y1 type filter (ceramic), interference suppressors (dc film), RC snubber network (dc film), microwave, and trimming.

1.6. RESİSTANCE

Resistance is the opposition that a substance offers to the flow of electric current. It is represented by the uppercase letter R. The standard unit of resistance is the ohm, sometimes written out as a word, and sometimes symbolized by the uppercase Greek letter omega. When an electric current of one ampere passes through a component across which a potential difference (voltage) of one volt exists, then the resistance of that component is one ohm.

In general, when the applied voltage is held constant, the current in a direct-current (DC) electrical circuit is inversely proportional to the resistance. If the resistance is doubled, the current is cut in half; if the resistance is halved, the current is doubled. This rule also holds true for most low-frequency alternating-current (AC) systems, such as household utility circuits. In some AC circuits, especially at high frequencies, the situation is more complex, because some components in these systems can store and release energy, as well as dissipating or converting it.

The electrical resistance per unit length, area, or volume of a substance is known as resistivity. Resistivity figures are often specified for copper and aluminum wire, in ohms per kilometer.

Opposition to AC, but not to DC, is a property known as reactance. In an AC circuit, the resistance and reactance combine vectorially to yield impedance.

1.6.1 ohm'slaw

Ohm's Law is the mathematical relationship among electric current, resistance, and voltage. The principle is named after the German scientist Georg Simon Ohm.

In direct-current (DC) circuits, Ohm's Law is simple and linear. Suppose a resistance having a value of R ohms carries a current of I amperes. Then the voltage across the resistor is equal to the product IR. There are two corollaries. If a DC power source

providing E volts is placed across a resistance of R ohms, then the current through the resistance is equal to E/R amperes. Also, in a DC circuit, if E volts appear across a component that carries I amperes, then the resistance of that component is equal to E/I ohms.

Mathematically, Ohm's Law for DC circuits can be stated as three equations:

$E = IR$

$I = E/R$

$R = E/I$

When making calculations, compatible units must be used. If the units are other than ohms (for resistance), amperes (for current), and volts (for voltage), then unit conversions should be made before calculations are done. For example, kilohms should be converted to ohms, and microamperes should be converted to amperes.

CHAPTER 2

THE FIELD EFFECT TRANSISTOR

2.1. The JFET

The first kind of FET that we discuss is the *junction* FE T, abbreviated JFET. Here is the basic idea behind a JFET. Figure 2-1a shows a piece of n-type semiconductor. This is not a JFET, but it is the first step in making a JFET. The lower end is called the source, and the upper end is called the *drain.* The supply voltage V_{DD} forces free electrons to flow from the source to the drain. The source and drain of a JFET are analogous to the emitter and collector of a bipolar transistor. To produce a JFET, a manufacturer diffuses two areas of p-type semiconductor into the n-type semiconductor, as shown in Fig. 2-1b. Each of these *p* regions is called a gate. When a manufacturer connects a separate lead to each gate, the device is called a dual-gate JFET. The main use of a dual-gate JFET is with a mixer, a special circuit used in communications equipment.

Most JFETS have the two gapes connected internally to get a single external gate lead as shown in Fig. 2-1c. Because the two bates are

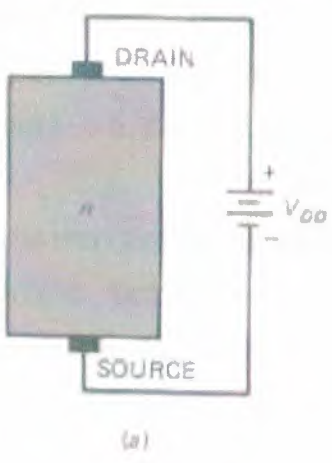


Figure 2.1(a)
Part of JFET

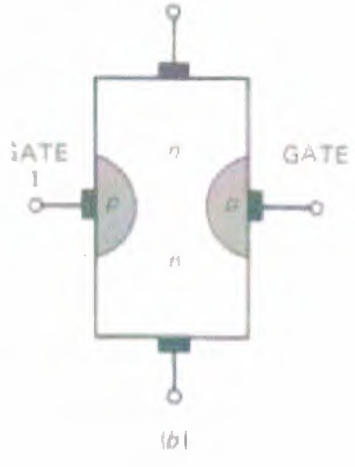


Figure 2.1(b)
dual-gate JFET

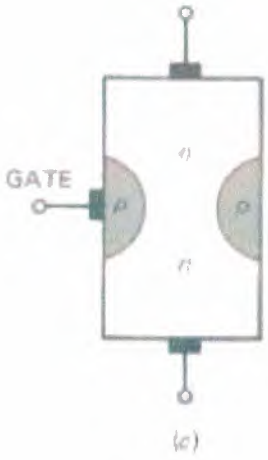


Figure 2.1 (c)
single-gate JFET

2.2. The Biased JIET

Figure 2-2a shows the normal way to bias a JFET. Look carefully and notice that this is distinctly different from the way we bias a bipolar transistor. See if you can figure out what the specific difference is before you continue reading.

2.2.1. Gate Current

The big difference is this: In a bipolar transistor, we forward-bias the base-emitter diode, but in a JFET, we always reverse-bias the gate-source diode. Because of the reverse bias, only a very small reverse current can

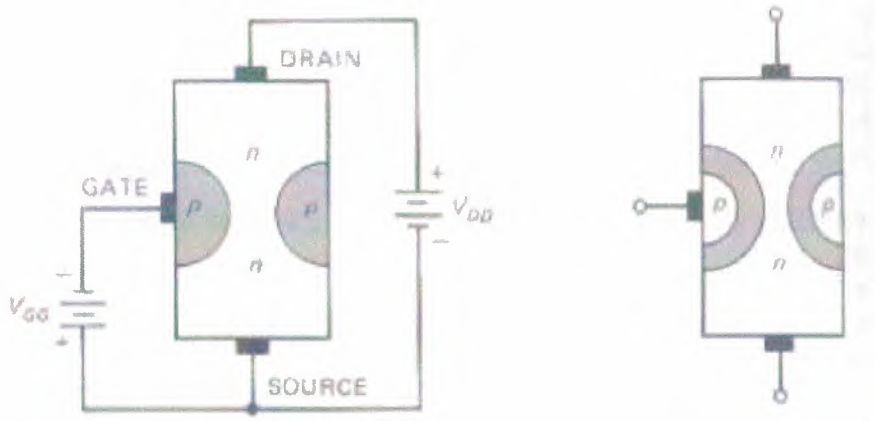


Figure 2.2 (a) >Normal biasing of JFET. (b) Depletion layers.

exist in the gate lead. As an approximation, the gate current is zero. In symbols,

$I_G = 0$ (2-1)

If a device has no input current, what does that tell you about its input resistance?

It tells you that the device has an infinite input resistance. For instance, if $V_{GG} = 2$ V and $I_G = 0$, the input resistance is

$$R_{IN} = 2V/0 = \text{infinity} \quad (2\text{-}2)$$

The reality of the situation is that I_G is not quite zero, so the input resistance is not quite infinite. But it's close. A typical JFET has an input resistance in the hundreds of megohms. This is the big advantage that a JFET has over a bipolar transistor. And it is the reason that JFETS excel in applications where a high input impedance is required. One of the most important applications of the JFET is the source follower, a circuit that is analogous to the emitter follower, except that the input impedance is in the hundreds of megohms for lower frequencies.

2.2.2 Field Effect

The term field effect is related to the depletion layers around each *p* region as shown in Fig. 2-2b. The junctions between each *p* region and the *n* regions have depletion layers because free electrons diffuse from the *n* regions into the *p* regions. The recombination

of free electrons and holes then creates the depletion layers shown by the shaded areas of Fig. 2-2b. When electrons bow from the source to the drain, they must pass through the narrow channel between the two depletion layers. The more negative the gate voltage is, the tighter the channel becomes. In other words, the gate voltage can control the current through the channel. The more negative the gate voltage, the smaller the current between the source and the drain.

Since the gate of a JFET is reverse-biased rather than forward-biased, the JFET act: as a voltage-controlled device rather than a current-controlled device. In a JFET, the controlling input quantity is the gate-to-source voltage V_{GS}. Changes in V_{GS} determine how much current can flow from source to drain. This is distinctly different from the bipolar transistor where the controlling input quantity is the base current *N*. In Fig. 2-2a, the drain supply voltage is positive, and the gate supply voltage is negative. Because of this, the voltage between the gate and the drain is negative. Therefore, the gate-drain diode is reverse-biased. As you see, both diodes in a JFET are reverse-biased for normal operation. There are no exceptions.

2.2.3 How It Works

At the instant the drain supply voltage is applied to the circuit, free electrons start to bow from the source to the drain. These free electrons have to pass through the narrow channel between the depletion layers. The gate voltage controls the width of this channel. The more negative

the gate voltage, the narrower the channel and the smaller the drain current. Almost a11 the free electrons passing through the channel bow to the drain. Because of this,

$$I_D = I_S \qquad (2\text{-}3)$$

2.2.4. The Price

Sometimes the strength of a device is also its weakness. The JFET has almost infinite input impedance, but the price paid for this is a loss of control over the output current. In other words, a JFET is less sensitive to changes in the input voltage than a bipolar transistor. In almost any JFET a change in V_{GS} of 0.1 V produces a change in the drain current of less than 10 mA. But in a bipolar transistor the some change in mss produces a change in the output current much greater than 10 mA. What does this mean? It means a JFET amplifier has much less voltage gain than a bipolar amplifier. For this reason, the first design rule governing the two devices is this: Use bipolars for large voltage gain, and use JFETS for high input impedance. Often, a designer combines a JFET and

gain, and use JFETS for high input impedance. Often, a designer combines a JFET and a bipolar transistor to get the best of all worlds. For instance, the first stage may be a JFET source follower, and the second stage may be a bipolar CE amplifier. This gives a multistage amplifier a high input imbalance and a large voltage gain.

2.2.5. Schematic Symbol

The JFET we have been discussing is called an n-channel JFET because the channel between the depletion layers is made of n-type semiconductor. Figure 2-3 shows the schematic symbol for an n-channel JFET. In many low-frequency applications, the source and the drain are interchangeable because you can use either end as the source and the other end as drain.

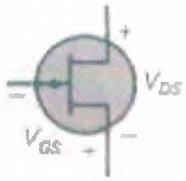


Figure 2.3 Schematic symbol

for n-channel JFET. Although either end of most JFETS may be up as the source at low frequencies, this is not true at high frequencies. Almost always the manufacturer minimizes the internal capacitance on the drain side of the JFET. AII you need to know now is this: The capacitance between the gate and the drain is smaller then the capacitance between the gate and the source. There is also a p-channel JFET. It consists of a p-type material with diffused islands of n-type material. The schematic symbol for a p-channel JFET is similar to that for the n-channel JFET, except that the gate arrow mints from the channel to the gate. The action of a p-channel JFET is complementary, which means that all voltages and currents are reversed.

2.3. Drain Curves

Figure 2-4a shows a JFET with normal biasing voltages. In this circuit, the gate-source voltage V_{GS} equals the gate supply voltage V_{GG}, and the drain-source voltage V_{DS} equals the drain supply voltage V_{DD}.

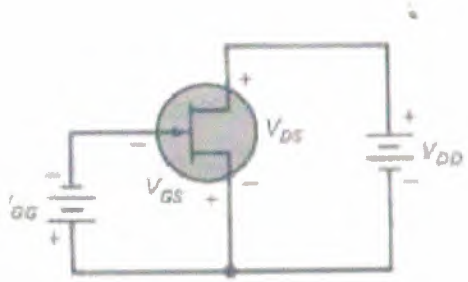


Figure 2.4 (a) Normal bias for JFET.

2.3.1. Maximum Drain Current

The maximum drain current out of a JFET occurs when the gate-source voltage is zero as shown in Fig. 2-4b. Here you see the gate supply voltage replaced by a short circuit, which guarantees that. $V_{GS} = 0$

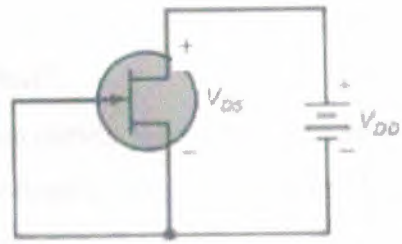


Figure 2.4 (b) Zero voltage gate.

Figure 2-4c shows the corresponding graph of drain current I_D versus drain-source voltage V_{DS}. Notice the similarity to a collector curve. The drain current increases rapidly at first, then levels off and becomes almost horizontal. In the region between V_P and $V_{DS(max)}$, the drain current is almost constant. If the drain voltage is too large, the JFET breaks down as shown.

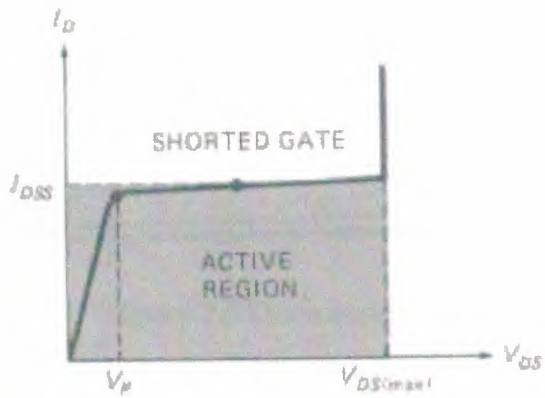


Figure 2.4 (c) Shorted gate drain current

.Similar. to a bipolar transistor, a JFET ants like a current source when it is operating Along the almost-horizontal part of the drain curve. This almost-horizontal part of the drain curve is between a minimum voltage of V_P and a maximum voltage of $V_{DS(max)}$. The minimum voltage V_P is called the pickoff voltage, and maximum voltage $V_{DS(max)}$ is called the breakdown voltage. Between pickoff and breakdown, the JFET acts approximately like a current source with a value of I_{DSS}.

I_{DSS} stands for the current from drain to source with a shorted gate,

and I_{DSS} is the maximum drain current a JFET can produce. All datasheets for JFETS list the value of I_{DSS}. This is one of the most important JFET quantities and you should always look for it first because it gives the limitation on the JFET current. For instance, the MPF102 has a typical I_{DSS} of 6 mA. This tells you that no matter what the circuit design is, the drain current will be between 0 and 6 my for a typical MPF102.

2.3.2. Gate Cutoff and Pinchoff

Figure 2-5 shows a set of drain curves for a JFET with an I_{DSS} of 10 mA. The top curve is for $V_{GS} = 0$. The pickoff voltage is 4 V, and the breakdown voltage is 30 V. The next curve down is for $V_{GS} = -1$ Vs

the next for $V_{GS} = -2$ V, and so on. As you see, the more negative the gate-source voltage, the smaller the drain current. The bottom curve is especially important. Notice that a V_{GS} of - 4 V

reduces the drain current to almost zero. This voltage is called the gate-source cutoff voltage.

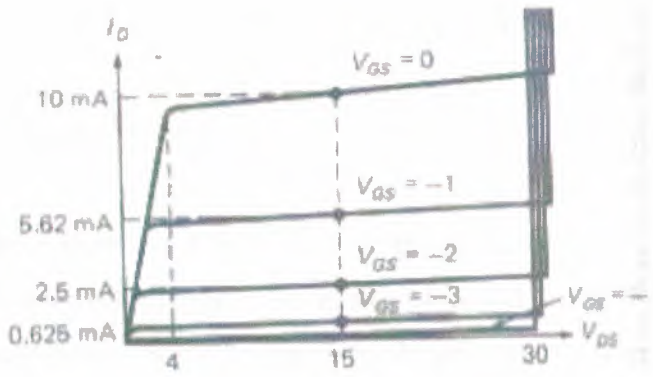


Figure 2.5 Drain curves.

On data sheets, it is symbolized as $V_{GS(max)}$. In Fig.2-5, notice that:

$$V_{GS(off)} = -4V \text{ and, } V_P = 4\ V$$

Is this a coincidence? Not at all. For advanced reasons that we won't go into, the magnitudes of these two voltages are always equal. This is worth remembering because many data sheets will list one value but not the other.

They do this because everyone is supposed to know that the two voltages are equal in magnitude. Giving you the value of one is equivalent to giving you the other. For instance, the data sheet of an MPF102 gives

$$V_{GS(off)} = -8V$$

For the gate-source cutoff voltage. Although the kirchoff value is not given, we know automatically the $V_P = 8$ V.

Here is a formal reminder of how the gate-source cutoff voltage is related to the kirchoff voltage:

$$V_{GS(off)} = - V_P \qquad (2\text{-}4)$$

This says the gate-source voltage equals the negative of the kirchoff voltage.

2.3.3. The Ohmic Region

In Fig. 2-5, the kirchoff voltage is the voltage where the highest drain curve changes from almost vertical to almost horizontal. It is a very important voltage because it separates two major operating regions of the JFET. The almost-vertical part of the drain curve is called the ohmic region, equivalent to the saturation region of a bipolar transistor. When operated in the ohmic region, a JFET ants as a small resistor with a value

of approximately, $R_{DS}=V_P/I_{DSS}$. (2-5)

2.4. The Transcondutance Curve

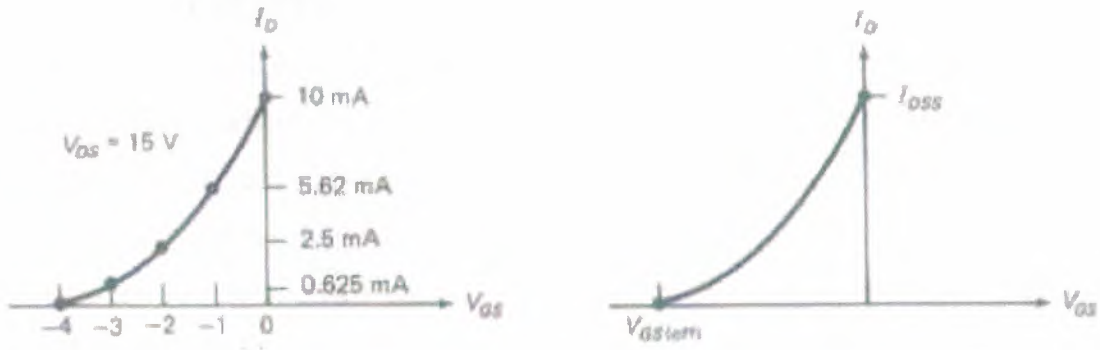
The transconductance curve of a JFET is a graph of drain current versus gate-source voltage, or I_D versus V_{GS}. By reading the values of I_D and V_{GS} in Fig. 2-5, we can plot the transconductance curve shown in Fig. 2-6a. In general, the transconductance curve of any JFET will have the same shape as Fig. 2-6a only the numbers will be different.

Figure 2-6b shows how the transconductance curve of any JFET will appear. Why is this? The physics behind JFET operation is the some for all JFETS. Only the size of the doped regions, the level of doping, etc.

doped regions, the level of doping, etc.

change from one JFET to the next. Because of this, all JFETS have a transconductance curve that is the graph of the following equation:

I_D =IDSS [(1-VGS/VGS).(1-VGS/VGS)]. (2-6)



(a) (b)

Figure 2.6 (a), (b) Transcondutance carves.

This equation can be derived with advanced physics and mathematics. We do not show the derivation because it is too complicated. With Eq. (2-6), we can calculate the drain current given the maximum drain current, the gate-source cutoff voltage, and the gate voltage. This is the algebraic way to and the drain current. On the other hand, some data sheets include graphs like Fig. 2-6a. In this case, you don't have to use Eq. (2-6). You can read the values of drain current directly from the graphs. This is the graphical way to and the drain current. For instance, Fig. 2-6a is good for quick and approximate answers. You ran see at a glance that the maximum drain current is 10 my and that the gate-source cutoff voltage is - 4 V. In between these extreme mints on the graph, you can see that the graph is nonlinear. In fact, the sham of this graph is part of a parabola, a curve that exists when quantities are squared. The quantity that multiplies *Inn* in the foregoing equation is the *K* factor, given by

$$K= [(1-V_{GS} / V_{GS(off)})(1-V_{GS} / V_{GS(off)})] \quad (2\text{-}7)$$

We are going to use the *K* factor in later discussions. For now, notice that we can rewrite Eq. (13-6) as

$$I_D=K\ I_{DSS} \quad (2\text{-}8)$$

If we have the value of *K* for any circuit, we can quickly calculate the value of drain current, given the maximum drain current. Incidentally, square law is another name for

parabolic. This is why JFETS are often called square-law devices. And this is another big difference between a bipolar transistor and a JFET. The square-law property gives JFETS a major advantage over bipolar transistors when it comes to mixers-circuits used in communications equipment.

2.5. JFET APPROXIMATIONS

As with bipolar transistors, exact analysis of JFET circuits is a waste of time. The manufacturing spreads of JFETS are even worse than they are for bipolar transistors. For instance, a 2N3904 has minimum and maximum β values of 100 to 300, a 3:1 spread. An MPF102 has minimum and maximum I_{DSS} values of 2 and 20 mA, a 10:1 spread. When you have a10:1 spread like this, the only sensible approach is to use reasonable approximations.

2.5.1. The Ideal JFET

AT this time, we are going to discuss two dc approximations for any JFET. Both approximations are derived as follows: If a manufacturer could produce an ideal JFET, here is what would happen to the curves of Fig. 2-5. First, there would be no breakdown region. Second, all drain curves would superimpose in the ohmic region. Third, all drain curves would be horizontal in the current-source region. Figure 2-7 shows the drain curves of an ideal JFET and a typical dc load line. The ideal JFET has two major regions of operation: the ohmic region (saturation) and the current-source region (active). The ohmic region of the JFET is highly desirable because it can be used in all kinds of analog-switching applications. This is why we have included the almost-vertical part of the drain curves in Fig. 2-7. When we want a JFET to

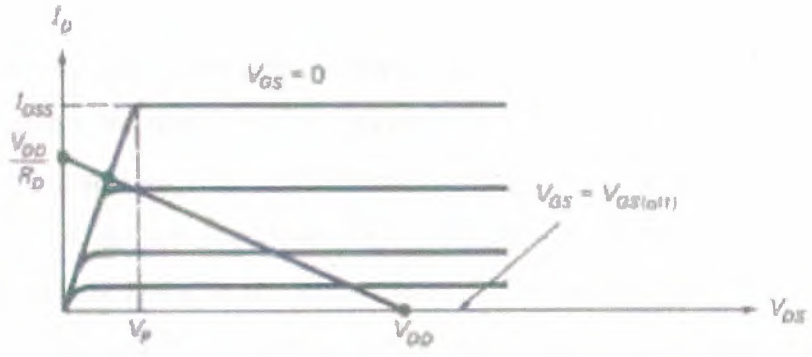


Figure 2.7 Load line

Act like a resistor, we have to make sure that the JFET is saturated, that .It is operating point is on the almost-vertical part when we want a JFET to act as a current source, we have to make sure that the operating point is on the horizontal part of the drain curves.

Since there are two major regions of operation, we need two basic models or equivalent circuits to describe dc operation. First, we approximate a JFET by the dc model shown in Fig. 2-8a. As you see, the input side of the JFET has a dc input resistance of Res. If necessary, you can estimate its value by taking the ratio of the V_P and V_{DSS} values given on the data sheet. But most of the time, you can ignore R_{GS} because it is almost infinite. On the output side of Fig. 2-8a, the JFET acts like a current source of KI_{DSS}. This is the dc model that we can use when the JFET operates in the active region. Recall that the pickoff voltage is the clue here.

When V_{DS} is greater than V_P the JFET will act like a current source for any gate voltage. Given I_{DSS} and $V_{GS(off)}$, we can calculate the value of K for any V_{GS} input voltage. Figure 2-8b shows a second model for a JFET. This is the ohmic model because it is valid whenever the JFET is operating on the almost-vertical part of the drain curves. Notice that the JFET is no longer a current source on the output side. Rather, it acts like a resistance of D_{DS}. You can estimate the value of D_{DS} by the ratio of $V`_P$, to I_{DSS}.

2.5.2. Proportional Pinchoff

The kirchoff voltage of Fig. 2-7 separates the ohmic region from the active region when V_{GS} is zero. When V_{GS} does not equal zero, we can use the proportional kirchoff voltage as our guide. Symbolized $V`_P$ this voltage is the border between the ohmic region and the current-source region for any value of V_{GS}. This quantity is given by

$$V`_P = I_D R_{DS} \qquad (2\text{-}9)$$

Here is how you use this equation. First, you calculate R_{DS} by dividing Vp by Joss. Then you multiply R_{DS} by the actual drain current to find the value of $V`_P$. This value is the border between the two operating regions.

Figure 2-9 shows you why Eq. (2-9) is valid. Here you see the ohmic region of an ideal JFET. The highest point in the ohmic region has coordinates of I_{DSS} and Vp. The other point represents any point in the ohmic region. The coordinates of any point in the ohmic region are I_D and $V`_P$ with basic geometry; you can see this proportional relation:

$$V'_P / I_D = V_P / I_{DSS} \quad (2\text{-}10)$$

But this is the equivalent to: $V'_P / I_D = R_{DS}$ (2-11)

If you solve this for V'_P, you get Eq. (2-9)

Designers use the JFET m two basic ways: as a resistor and as a current source. When you analyze JFET circuits, you have to figure out which way the JFET is being used. Then you will know whether to use the current-source model (fig. 13-8a) or the ohmic model

(Fig. 2-8b).Here is the process for deciding which model to use:

1. Divide V_P by I_{DSS} to get R_{DS}.
2. Multiply ID by R_{DS} to get V'_P.
3. If $V_{DS} > V'_P$, use the current-source model.
4. If $V_{DS} < V'_P$, use the ohmic model.

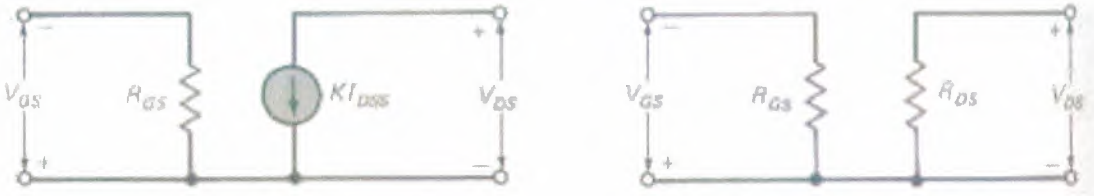


Figure 2.8 (a) Current source model (b) Ohmic model

2.5.3. Analyzing JFET Circuits

We are about to look at several examples of analyzing a JFET. Before we do, let us summarize the important quantities and equations that we need. To begin, we must have I_{DSS} and $V_{GS(off)}$ Without them, you don't have enough information to analyze the circuit. Depending on how the analysis goes, you will need some of or all the following useful formulas:

$$V_P = - V_{GS(off)} \quad (2\text{-}12)$$

$$R_{DS} = V_P / I_{DSS} \quad (2\text{-}13)$$

$$K = [(1 - V_{GS}/V_{GS(off)})(1 - V_{GS}/V_{GS(off)})] \quad (2\text{-}14)$$

$$I_D = KI_{DSS} \quad (2\text{-}15)$$

$$V'_P = I_D R_{DS} \quad (2\text{-}16)$$

2.5.4. Reduction and absurdum

You already know about reduction and absurdum, which was introduced with bipolar transistors. Recall the basic idea. When you are not sure which region a device is operating in, you assume an operating region and see if your calculations produce an absurd or a contradictory result.

If so, then you know the device cannot operate in the assumed region.

If you are analyzing a JFET circuit and you are not sure of the operating region, then proceed as follows:

1. Assume the current-source region.
2. Carry out your calculations.
3. If an absurd answer arises ,the assumption is false.
4. change to the ohmic model.

The calculation for V_{DS} is identical to the calculation for V_{DS} in a bipolar transistor, except for a change in the subscripts. Here is how the calculation looks as a JFET formula:

$$V_{DS} = V_{DD} - I_D R_D \qquad (2\text{-}17)$$

The corresponding bipolar formula is

$$V_{CE} = V_{CC} - I_C R_C \qquad (2\text{-}18)$$

The two equations have the same format; they differ only in their subscripts.

This is an example of what we mean by analogy. When an old system and a new system are governed by the Rome fundamental lawny their final equations are the same in appearance. If you already know a lot about the old system, you don't have to rediscover everything for the new system. You can take advantage of the similarities in the old system to understand the new system.

The Analogy between bipolar and JFET circuits gives us all kinds of powerful shortcuts for solving new JFET circuits with old bipolar methods.

Since Ohm's and Kirchhoff's laws are the fundamental laws behind bipolar and JFET circuits, many JFET equations are nothing more than bipolar equations with their subscripts changed as follows:

Bipolar	JFET
E	S
B	G
C	D

Because of the analogy between bipolars and JFETS, many of the new JFET formulas you see will be a lot easier to remember.

2.6. THE DEPLETOIN-MODE MOSFET

The metal-oxide semiconductor FE T or MOSFET, has a source, gate, and drain. Unlike a JFET, however, the gate is electrically insulated from the channel. Because of this, the gate current is extremely small whether the gate is positive or negative. The MOSFET is sometimes referred to as an IGFET, which stands for insulated-gate FET.

2.6.1. The Basic Idea

Figure 2-9 shows an Ai-channel depletion-mode MOSFET. It is a piece of n material with a *p* region on the right and an insulated gate on the

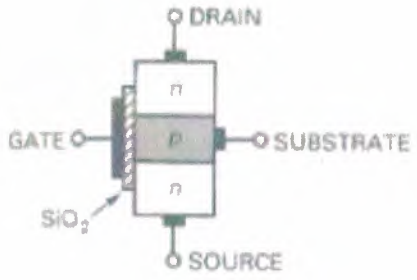


Figure 2.9 Depletion-mode MOSFET.

left. Free electrons can flow from the source to the drain through the *n* material. The *p* region is called the *substrate* (or body). Electrons flowing from source to drain must pass through the narrow channel between the gate and the *p* region.

A thin layer of silicon dioxide (SiO2) is deposited on the left side of the channel. Silicon dioxide is the some as glass, which is an insulator. In a MOSFET, the gate is metallic. Because the metallic gate is insulated from the channel, negligible gate current flows even when the gate voltage is positive .

Figure 2-10a shows a depletion-mode MOSFET with a negative gate.

The V_{DD} supply forces free electrons to Now from source to drain. These electrons bow through the narrow channel on the left of the *p* substrate. As with a JFET, the gate voltage controls the width of the channel. The more negative the gate voltage, the smaller the drain current. When the gate voltage is negative enough, the drain current is cut off. Therefore, the operation of a MOSFET is similar to that of a JFET when V_{GS} is

negative.

Because the gate of a MOSFET is electrically insulated from the channel, we can apply a positive voltage to the gate, as shown in Fig. 2-10b. The positive gate voltage increases the number of free electrons flowing through the channel.

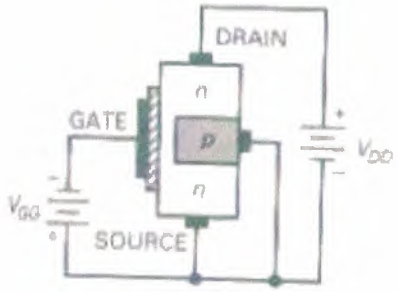


Figure 2.10 (a) Negative gate voltage .

The more positive the gate voltage, the greater the conduction from source to drain. Being able to use a positive gate voltage is what distinguishes the depletion-mode MOSFET from the JFET

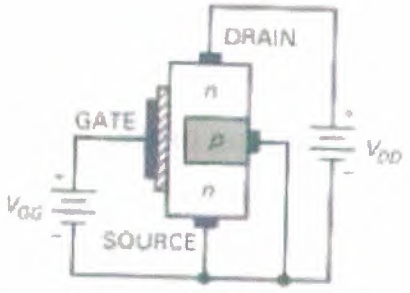


Figure 2.10 (b) Positive gate voltage.

2.6.2. Graphs

Figure 2-11a shows typical drain curves for an n-channel MOSFET. Notice that the upper curves have a positive V_{GS} and the lower curves have a negative V_{GS}. The bottom drain curve is for $V_{GS} = V_{GS(off)}$.

Along this cutoff curve, the drain current is approximately zero. When V_{GS} is between $V_{GS(off)}$ and zero, we get depletion-mode operation.And V_{GS} greater than zero gives enhancement-mode operation. These drain curves again display an ohmic region, a current-source region, and a cutoff region. Like the JFET, the depletion-mode MOSFET has two major applications: a current source or a resistance.

Figure 2-11a is transconductance curve of a depletion-mode MOSFET and I_{DSS} is the drain current with a shorted gate. Since the curve extends to the right of the origin I_{DSS},

is no longer the maximum possible drain current. Mathematically, this curve is still part of a parabola, and the 'me square-law relation exists as

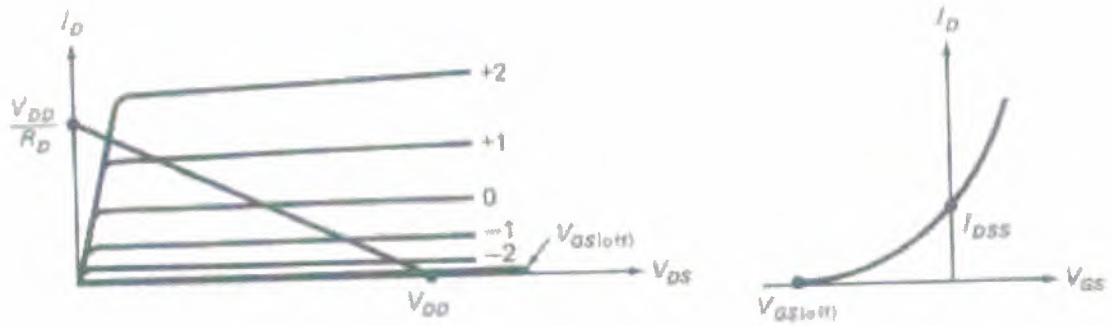


Figure 2.11 (a) Drain curve , (b)Transcoductance carve.

with a JFET. In fact, the depletion-mode MOSFET has a drain current given by the same trans- conductance equation as before, Eq. (2-6). Furthermore, it has the same equivalent circuits as a JFET. Because of this, the analysis of a depletion- mode MOSFET circuit is almost identical to that of a JFET circuit. The only difference is the analysis for a lenitive gate, but even here the same basic formulas are used to find the drain current, gate-source voltage, etc.

2.6.3. Schematic Symbol

Figure2-12a shows the schematic symbol for a depletion-mode MOSFET. Just to the right of the gate is the thin vertical line representing the channel. The drain lead comes out the top of the channel, and the source lead connects to the bottom. The arrow on the *p* substrate points to the *n* material. In some applications, a voltage can be applied to the substrate for added control of the drain current. For this reason, some depletion-mode MOSFETS have four external leads. But in most applications, the substrate is connected to the source. Usually, the manufacturer internally connects the substrate to the source. This results in a three- terminal device whose schematic symbol is shown in Fig. 2-12b.

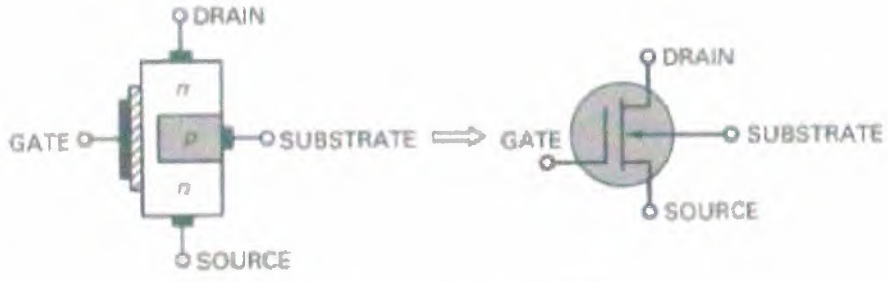


Figure 2.12 (a) Schematic symbols.

Figure 2.12 (b) Schematic symbols.

There is also a p-channel depletion-type MOSFET. It consists of a piece of p material wit an n region on the right and an insulated gate on the left. The schematic symbol of a p-channel MOSFET is similar to that of an n-channel MOSFET, except that the arrow mints outward. In the remainder of this chapters we emphasize the n-channel MOSFET. The action of a p-channel MOSFET is complementary, meaning that all voltages and currents are reversed.

2.7. THE ENHANCEMENT-MODE MOSFET

Although the depletion-mode MOSFET is useful in special situations. It played an important role in history because it was part of the evolution toward the enhancement-mode MOSFET, a device that has revolutionized the electronics industry. This second type of MOSFET has become enormously important in digital electronics and computers. Without it, the personal computers that are now so widespread would not exist.

2.7.1. The Basic Idea

Figure 2-13a shows an n-channel enhancement-type MOSFET. The substrate extends all the way to the silicon dioxide. As you see, there no longer is an n channel between the source and the drain.

How does it work? Figure 2-13b shows normal biasing polarities. When the gate voltage is zero, the V_{DD} supply tries to force free electrons from source to drain, but the, p substrate has only a few thermally produced free electrons. Aside from these minority carriers and some surface leakage, the current between source and drain is zero. For this reason, an enhancement-mode MOSFET is normally off when the gate voltage is zero. This is completely different from depletion-mode devices like the JFET or the depletion-mode MOSFET.

When the gate is positive enough, it attracts free electrons into the *p* region. The free

electrons recombine with the holes next to the silicon dioxide. When the gate voltage is positive enough, all the holes touching the silicon dioxide are felled and free electrons begin to bow from the source to the drain. The effect is the same as creating a thin layer of a-type material next to the silicon dioxide. This conducting layer is called the *n-type inversion layer.* When it exists, the normally off device suddenly turns on and free electrons Now easily from the source to the drain. The minimum V_{GS} that creates the n-type inversion layer is called the threshold voltage, symbolized $V_{GS(th)}$. When V_{GS} is less than $V_{GS(th)}$ the drain current is zero. But when V_{GS} is greater than $V_{GS(th)}$, an n-type inversion layer connects the source to the drain and the drain current is large. Depending on the particular device being used, $V_{GS(th)}$. can vary from less than 1 to more than 5 V.

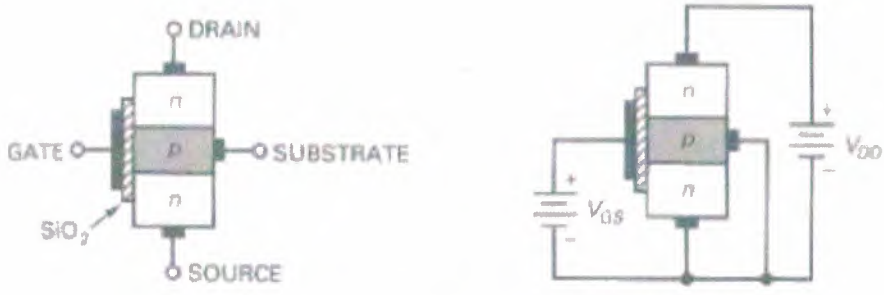


Figure 2.12 (a), (b) Enhancement-mode MOSFET.

JFETS and depletion-mode MOSFETS are classified as depletion-mode devices because their conductivity defends on the action of depletion layers. The enhancement-mode MOSFET is classified as an enhancement- mode device because its conductivity depends on the action of the n-type inversion layer. Depletion-mode devices are normally on when the gate voltage is zero, whereas enhancement-mode devices are normally off when the gate voltage is zero.

2.7.2. Graphs and Formulas

Figure 2-14a shows a set of drain curves for an enhancement-mode MOSFET and a typical load line. The lowest curve is the $V_{GS(th)}$ curve.

When V_{GS} is less $V_{GS(th)}$, the drain current is approximately zero. When V_{GS} is greater than $V_{GS(th)}$, the device thorns on and the drain current is controlled by the gate voltage. Again, notice the almost- vertical and almost-horizontal parts of the curves. The almost-vertical part

corresponds to the ohmic region, and the almost-horizontal parts correspond to the

current-source region. The enhancement-mode MOSFET can operate in either of these recons. In other words, it can act as a current source or as a resistor.

Figure 2-14b shows a typical transconductance curve. Again, the curve is parabolic or square-law. The vertex (starting point) of the parable is at $V_{GS(th)}$. Because of this, tile equation for the parabola is different from before. It now equals

$$I_D=k\ (V_{GS(th)}-\mathbf{VGS(th)^2}) \qquad (2\text{-}19)$$

where k is a constant that demands on the particular MOSFET. Any data sheet for an enhancement-mode FET will include the current, $I_{D(on)}$ and the voltage, $V_{GS(on)}$, for one point well above the threshold as shown in figure 2.14b.

With JFETs and depletion-mode MOSFETS, the values of I_{DSS} and $V_{GS(off)}$ Are the key quantities need for analysis. With enhancement-mode MOSFETS the key quantities are $I_{D(on)}$, $V_{GS(th)}$ and $V_{GS(on)}$, shown in Fig. 2-14b these three quantities are the first items to look for on

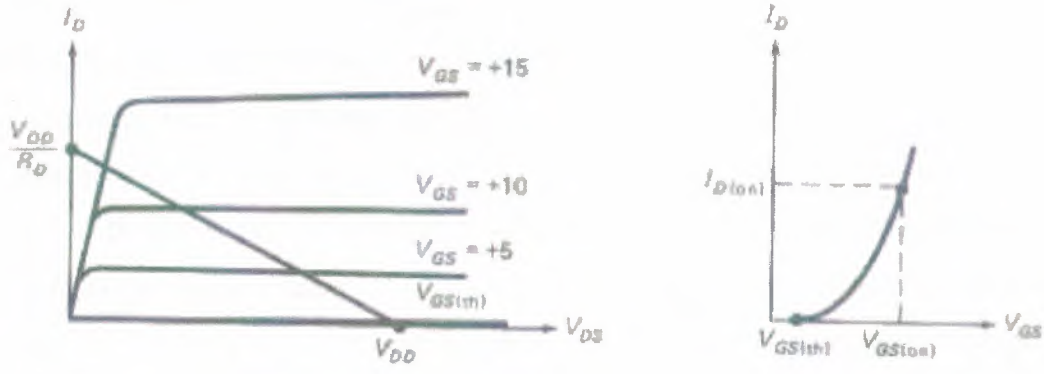


Figure 2.12 (a) Drain curves. (b) Transconductance carves.

A data sheet. By substituting these quantities into Eq. (2-19), we can rearrange the equation in a more useful form:

$$I_D = KI_{D(on)} \qquad (2\text{-}20)$$

Where,

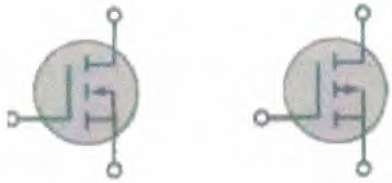
$$K = [(V_{GS}- V_{GS(th)})/ (V_{GS(on)}- V_{GS(th)})]^2 \qquad (2\text{-}22)$$

This expression appears formidable at first, but it is easy to work with after you get used to it.

2.7.3. Schematic symbol

When $V_{GS} = 0$, the enhancement-mode MOSFET is off because there is no conducting channel between source and drain. The schematic symbol of Fig. 2-15a has a broken

channel line to indicate this normally off condition. As you know, a gate voltage greater than the threshold voltage creates an n-type inversion layer that connects the source to the drain. The arrow mints to this inversion layer, which ants like an *n* channel when the device is conducting. There is also a p-channel enhancement- mode MOSFET. The schematic symbol is similar, except that the arrow points outward, as shown in Fig. 2-15b.



(a) n-channel (b)p-channel

Figure 2.13 Schematic symbols.

2.7.4. Maximum Gate-Source Voltage

MOSFETS have a thin layer of silicon dioxide, an insulator that prevents gate current for positive as well as negative gate voltages. This insulating layer is kept as thin as possible to give the gate more control over the drain current. because the insulating layer is so thin, it is easily destroyed by excessive gate-source voltage. For instance, a 2N3796 has a $V_{GS(max)}$ rating of $\pm$ 30 V. lf the gate-source voltage becomes more positive than + 30 V or more negative than - 30 V, the thin insulating layer will be destroyed.

Aside from directly applying an excessive V_{GS}, you ran destroy the thin insulating layer in more subtle ways. If you remove or insert a MOSFET into a circuit while the power is on, transient voltages caused by inductive kickback and other effects may exceed the $V_{GS(max)}$ rating. This will wipe out the MOSFET. Even picking up a MOSFET may deposit enough static charge to exceed the $V_{GS(max)}$ rating. This is the reason why MOSFETS are often shipped with a wire ring around the leads. You remove the ring after the MOSFET is connected in the circuit. Some MOSFETS are protected by built-in zener diodes in parallel with the gate and the source. The zener voltage is less than the $V_{GS(max)}$ rating. Therefore, the zener diode breaks down before any damage to the thin insulating layer occurs. The disadvantage of these internal zener diodes is that they reduce the MOSFET'S high input resistance. The trade-off is worth it in some applications because expensive MOSFETS are easily destroyed without zener protection.

Remember this idea: MOSFET devices are delicate and can be easily destroyed. You have to handle them carefully. Furthermore, you should never connect or disconnect them while the power is on. Finally before you pick up a MOSFET device, you should ground your body by touching the chassis of equipment you are working on.

2.7.5. Equivalent Circuits

Figure 2-16 shows ideal drain curves for an enhancement-mode MOSFET. First, there is no breakdown region. Second, all drain curves superimpose in the ohmic region to produce a single, almost-vertical line. Third, all drain curves are horizontal in the current-source region. These ideal drain curves are similar to depletion-mode curves, except for the proportional knee voltage V'_k.This voltage is given by

$$V'_k = I_D R_{DS} \qquad (2\text{-}23)$$

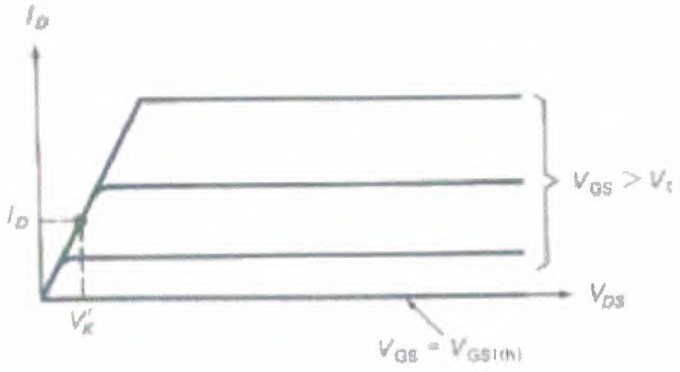
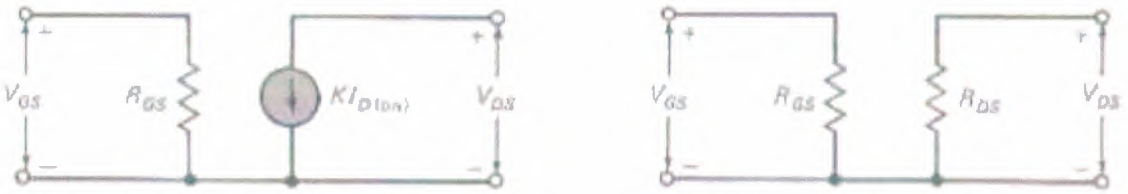


Figure 2.16 Ideal drain curves.

This voltage is the border between the ohmic region and the current- source region in an ideal enhancement-mode device. The border concept is identical to V'_P. The reason for not using V'_P is because enhancement- mode MOSFETS don't have a pickoff voltage where depletion layers come together. Instead, they have an inversion layer. Because a different physical mechanism is involved, we use the symbol V'_k for the border between the two regions.

Figure 13-21 shows the two ideal equivalent circuits. As you see, these equivalent circuits are the some as for a JFET, except for loon) and the positive gate voltage. In other words, the enhancement-mode MOSFET can act like a current source or like a



(a) (b)

Figure 2.15 (a), (b) Ideal equivalent circuits.

Depends on where the operating mint is. The proportional knee voltage is your guide. When V_{DS} is greater than V'_k the device is a current source. When V_{DS} is less than V'_k, the device is a resistor. Here is the process for deciding which model to use:

1. Calculate V'_k.
2. If $V_{DS} > V'_k$, use a current-source equivalent circuit.
3. If $V_{DS} < V'_k$, use an ohmic equivalent circuit.

2.8. Summary of Chapter 2

The aim of this chapter is to make the reader able to:

1. Describe the basic construction of a JFET, and draw a diagram showing how it is normally biased.
2. Identify and describe the significant regions of JFET drain curves and transconductance curves.
3. Calculate the proportional kirchoff voltage and determine which region a JFET is operating in.
4. Illustrate the construction of and describe the operation of the depletion-mode MOSFET.
5. Illustrate the construction of and describe the operation of the enhancement-mode MOSFET.

CHAPTER 3
THE FOUR LAYER DIODE ANALYSİS

3.1. The Four Layer Diode

The word thyristor comes from the Greek and means 'door' as in opening a door and letting something pass through it. As a start, you can think of a thyristor as a new kind of switch. All thyristors can be explained in terms of the circuit shown in Fig. 3-la. Notice that the upper transistor Ql is a pnp device and the lower transistor Q2 is an npn device. The collector of Ql drives the base of Q2, and the collector of Q2 drives the base of Ql.

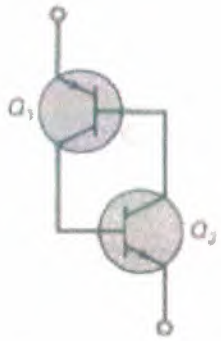


Figure 3.1 (a) Thyristor latch.

3.1.1. Positive feedback

Because of the unusual connection of Fig. 3-1a, we have positive feedback. A change in current at any point in the feedback loop is amplified and returned to the starting point with the same phase. For instance, if the Q2 base current increases, the Q2 collector current increases. This forces mare base current through Q1. In turn, this produces a larger Ql collector current, which drives the Q2 base harder. This buildup in currents will continue until both transistors are driven into saturation. In this case, the circuit ants as a closed switch (Fig. 3-1b).

But if something causes the Q2 base current to decrease, the Q2 collector current will decrease. This reduces the Q1 base current. In turn, there will be less Q1 collector current, which reduces the Q2 base current even more. This positive feedback continues until both transistors are driven into cutoff. Then, the circuit acts as an open switch (Fig. 3-1c). The switching circuit can be in either of two states: closed or open. It will remain in either state indefinitely. If the switching circuit is closed, it stays closed until

else forces the currents to increase. Because this kind of switching action is based on positive feedback, the circuit has been called a latch.

(b) (c)

Figure3.1 (b), (c) Tthyristor latch.

3.1.2. Closing a Latch

Assume the latch of Fig. 3-2a is open. Then the equivalent circuit is an open switch as shown in Fig. 3-2b. Because there is no current through the load resistor, the output voltage equals the supply voltage. This means the operating point is at the lower end of the load line (Fig. 3-2d).

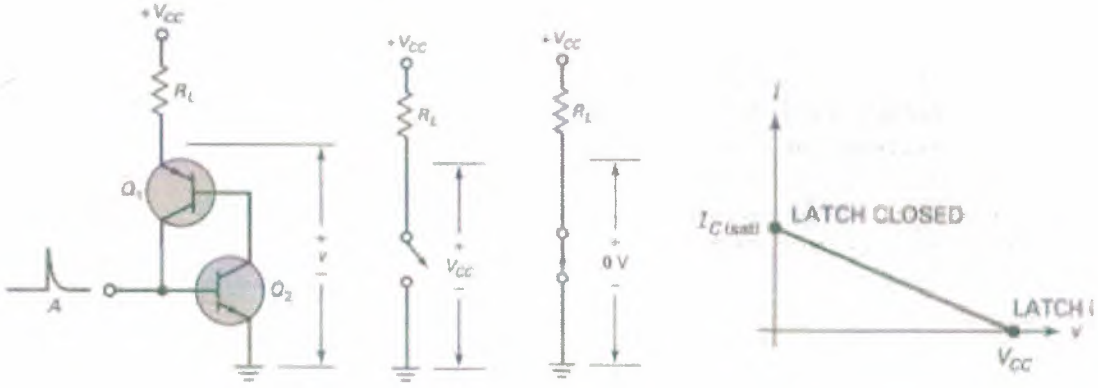
How can we close the latch? One way is by triggering. The idea is to apply a trigger (sharp pulse) to forward-bias the Q2 base-emitter diode in Fig.3-2a. At point A in timed the trigger momentarily turns on the Q2 base current. The Q2 collector current suddenly comes on and forces the base current trough Q1. In turn, the Q1 collector current comes on and drives the Q2 base harder. Since the Q1 collector now supplies the Q2 base current, the trigger pulse is no longer needed. Once the positive Feedback Starts, it will sustain itself and drive both transistors into saturation. minimum input current needed to start the switching action is called the trigger *current.*

When saturated, both transistors ideally look like short circuits, and the latch is closed (Fig. 3-2c). Ideally, the latch has zero voltage across it when it is closed, and the operating point is at the upper end of the load line (Fig. 3-2d).

Another way to close a latch is by breakover. This means using a large enough supply voltage V_{CC} to break down either collector diode. Once the breakdown begins, current comes out of one of the collectors and drives the other base. The effect is the same as if the base had received

a trigger. Although breakover starts with a breakdown of one of the collector diodes, it

ends with both transistors in the saturated state. This is why the term breakover is used instead of breakdown to describe this kind of latch closing.



(a) (b) (c) (d)

Figure 3.2 Thyristor latch with trigger inpot.

3.1.3. Opening a Latch

How do we own an ideal latch? One way is to reduce the load current to zero. This forces the transistors to come out of saturation and return to the open state. For instance, in Fig. 3-2a we can open the load resistor. Alternatively, we can reduce the Vcc supply to zero. In either case, a closed latch will be forced to open. We call this type of opening a low-current drop out because it depends on reducing the latch current to a low value.

Another way to open the latch is to apply a reverse-bias trigger in Fig. 3-2a.When a negative trigger is used instead of a positive one, the Q2 base current decreases. This forces the QI base current to decrease.

Since the Ql collector current also decreases, the positive feedback will rapidly drive both transistors into cutoff, which owns the latch.

Here are the basic ways to close and open a latch:

1. We can close a latch by forward-bias triggering or by breakover.
2. We can open a latch by reverse-bias triggering or by low-current drop out.

There are many different kinds of thyristors. The simplest type can only be closed with breakover and be opened with low-current drop out. The most popular types are closed by triggering and are opened by low-current drop out. Some rare types can be closed and opened in any of the ways described here.

3.1.4. The Shockley Diode

Figure 3-3a is called a four-layer diode (also known as a Shockley diode). It is classified as a dice because it has only two external leads. Because of its four doped regions, it's often called a *pnpn* diode. The easiest way to understand how it works is to visualize it separated into two halves, as

shown in Fig. 15-3b The left half is a pnp transistor, and the right half

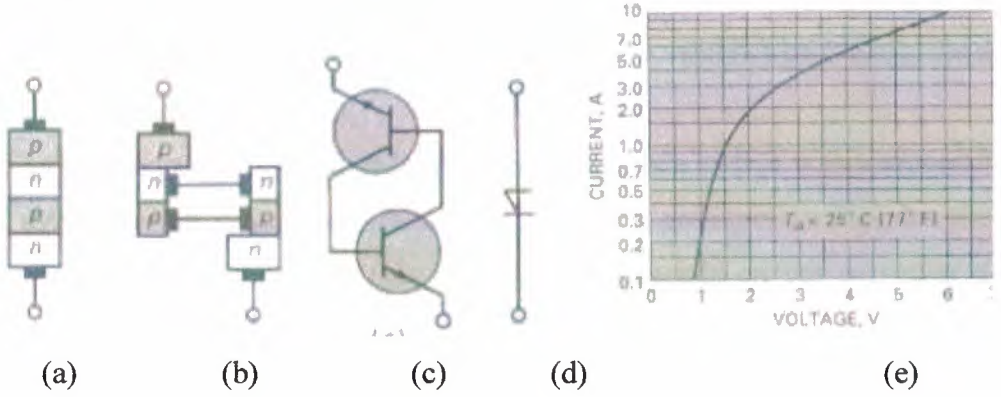


Figure 3.3 Four-layer diode.

is an npn transistor. Therefore, the four-layer diode is equivalent to the latch shown in Fig. 3-3c.

Because there are no trigger inputs, the only way to close a four-layer diode is by breakover, and the only way to open it is by low-current dropout. With a four-layer diode it is not necessary to reduce the current a11the way to zero to open the latch.

The internal transistors of the four-layer lode will come out of saturation when the current is reduced to alow value called the holding current. Figure 3-3d shows the schematic symbol for a four-layer diode.

After a four-layer diode breaks over, the voltage across it drops to a low value, depending on how much current there is. For instance, Fig. 3-3e shows the current versus voltage for a 1N5158. Notice that the voltage increases with the current through the device: 1 V at 0.2 A,

1.5 V at 0.95 A, 2 V at 1.8 A, and so forth.

3.1.5. Breakover Characteristic

Figure 3-4 shows the graph of current versus voltage for a breakover diode. The device has two operating regions: nonconducting and conducting. When it is nonconducting, it

operates on the lower line with no current and a voltage less than V_B. If the voltage tries to exceed V_B , the four-layer diode breaks over and switches along the dashed line to the conducting region. The dashed line in this graph indicates an unstable or a temporary condition. The device can have current and voltage values on this dashed line only briery as it switches between the two stable operating regions. When the four-layer diode is conducting, it is operating on the upper line. As long as the current through it is greater than the holding current I_H, then the voltage across it is slightly larger than V_K. If the current tries to decrease to less than I_H , the device switches back along the dashed line to the nonconducting region.

The ideal approximation of a four-layer diode is an open switch when nonconducting and a closed switch when conducting. The second approximation includes the knee voltage V_K shown in Fig. 3-4. This knee voltage depends on the particular device. Often, it is near 0.7 V. To keep

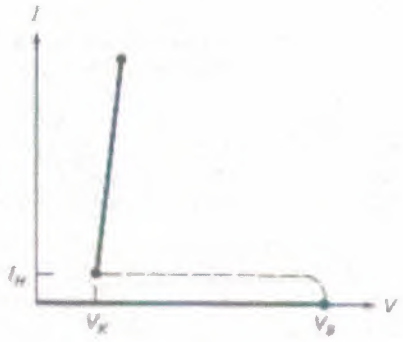


Figure 3.4 Breakover characteristic

things simple and easy to remembers we will use 0.7 V unless a more accurate knee voltage is available from a data sheet. For the third approximation, we can include the bulk resistance of the diode in calculating the total diode voltage:

$$V_D = V_K + I_D R_B \qquad (3\text{-}1)$$

If you are wondering what the circuit does, here is a brief explanation.When Power is first applied to the circuit, the capacitor voltage is zer . The capacitor charges, And its voltage increases from 0 toward 15V. When the capacitor voltage is slightly greater than 9V , the four layer diode breaks over and becomes equivalent to a closed switch . this forces the capacitor to discharge through the 100 ohm . As the capacitor discharges, its voltage decreases, and this causes the diode current to decrease. When the diode current is slightly less than the holding current, the diode owns. The capacitor then starts to

charge a11 over again. The cycle repeats with the diode breaking over, discharging the capacitor, and so on. The output of the circuit is a sharp voltage pulse across the load resistor. This sharp voltage pulse appears when the diode breaks over. The pulse is very short in duration because the capacitor quickly discharges.

3.2. THE SILICON CONTROLLED RECTIFIER

The silicon controlled rectifier (SCR) is more useful than a four-layer diode because it has an extra lead connected to the base of the npn section, as shown in Fig. 3-5a. Again, you can visualize the four doped regions separated into two transistors, as shown in Fig. 3-5b. Therefore, the SCR is equivalent to a latch with a trigger input (Fig. 3-5c). Schematic diagrams use the symbol of Fig. 3-5d. Whenever you see this, remember that it is equivalent to a latch with a trigger input.

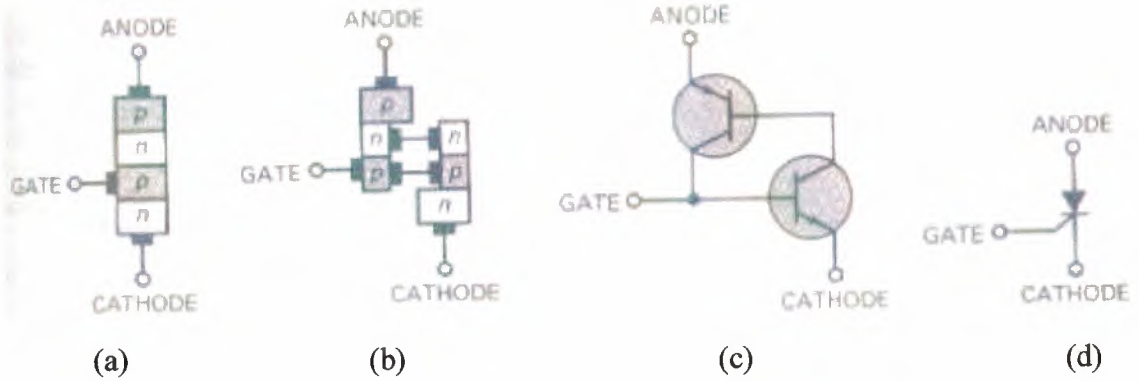


Figure 3.5 Silicon controlled rectifier .

3.2.1. Gate Trigging

The gate of a SCR is approximately equivalent to a diode (see Fig. 3-5c). For this reason, it takes abreast 0.7 V to triggers SCR. Furthermore, to get the positive feedback steed, a animus input current is required. Data sheets list the *trigger voltage* and *trigger current* for SCRS. For example, tilt data sheet of a 2N444 1 gives a typical trigger voltage of 0.75 V and a trigger current of 10 mA. The source driving the gate of a 2N4441 has to be able to supply at least 10 mA at 0.75 V; otherwise, the SCR will not latch shut.

When a SCR is conducting, it has a low voltage across it. For instance, a 2N4441 has 1

V across it when it is turned on. To open a SCR, the action is similar to that for a four-layer diode. You have to decrease the SCR current to less than its holding current. For example, the 2N4441 has a holding current of 6 mA. To shut off this SCR, the anode current must decrease to less than 6 mA. Then it will suddenly stop conducting and become an open circuit.

3.2.2. Blocking Voltage

SCRS are not intended for breakover operation. Breakover voltages range from around 50 to more than 2500 V, depending on the SCR type number. Most SCRS are designed for trigger closing and low-current opening. In other words, a SCR stays open until a trigger drives its gate (Fig. 3-5d. Then the SCR latches and remains closed, even though the trigger disappears. The only way to open a SCR is with low-current drop out. Most people think of a SCR as a device that blocks voltage until the trigger closes it. For this reason, the breakover voltage is often called the forward blocking voltage on data sheets. For instance, the 2N4441 has a forward blocking voltage of 50 V. As long as the supply voltage is less than 50 V, the SCR cannot break over. The only way to close it is with a gate trigger.

3.2.3. High Currents

Almost all SCRS are industrial devices that can handle large currents ranging from less than 1 to more than 2500 A, defending on the type number. Because they are high-current devices, SCRS have relatively large trigger and holding currents. The 2N4441 can conduct up to 8 A.

Continuously; its trigger current is 10 mA, and so is its holding current.

This means that you have to supply the gate with at least 10 mA to control up to 8 A of anode current. (The anode and cathode are shown in Fig.(3-5d.) As another exampled the C701 is a SCR that can conduct up to 1250 A with a trigger current of 500 mA and a holding current of50 mA.

3.2.4. Critical Rate of Rise

In many applications, an ac supply voltage is used with the SCR. By triggering the gate at a certain point in the cycle, we can control large amounts of ac power to a load such as a motor, a heater, or some other load. Because of junction capacitances inside the SCR, it is possible fora rapidly changing supply voltage to trigger the SCR. Put another

way, if the rate of rise of forward voltage is high enough, the capacitive charging current can initiate the positive feedback.

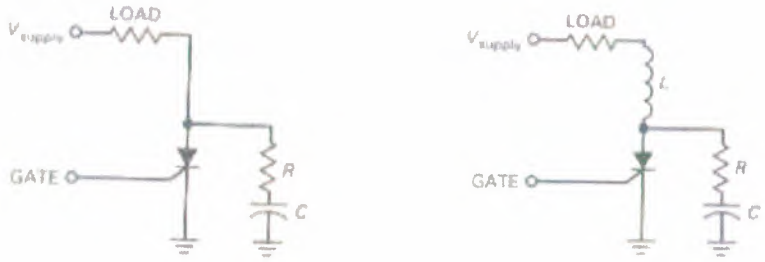
To avoid false triggering of a SCR, the anode rate of voltage change must not exceed the *critical rate of voltage rise* listed on the data sheet.

For instance, a 2N4441 has a critical rate of voltage rise of 50 V/μs. To avoid a false triggering, the anode voltage must not rise faster than 50 V/μs. As another example, the C701 has a critical rate of voltage rise of 200 V/μs. To avoid a false closure, the anode voltage must not increase

faster than 200 V/μs.

Switching transients are the main cause of exceeding the critical rate of voltage rise. One way to reduce the effects of switching transients is with an RC snubber, shown in Fig. 3-6a.If a high-speed switching transient does appear on the supply voltage, its rate of rise is reduced at the anode because of the RC circuit. The rate of the anode voltage rise, depends on the load resistance as well as on the R and C values.

Larger SCRS also have a critical rate of current rise. For instance, the C701 has a critical rate of current rise of 150 Aμs. If the anode current tries to rise faster than this, the SCR may be destroyed. Including an inductor in series, as shown in Fig. 3-6b, reduces the rate of current rise as well as helps the RC snubber decrease the rate of voltage rise.



(a) (b)

Figure 3.6 (a) Snubber, (b) Inductor protects SCR

3.2.5. Trigger Current and Voltage

A SCR like the one shown in Fig. 3-7 has a gate voltage V_G. When this gate voltage is in the vicinity of 0.7 V, the SCR will turn on and the output voltage will drop from + Vcc to a low value. When a gate resistor is used as shown here, you can calculate the input voltage needed to

trigger a SCR by using this equation:

$$Vin = V_T + I_T R_G \qquad (3\text{-}2)$$

In this equation, V_T and I_T are the trigger voltage and trigger current, respectively, needed for the gate of the device. You will find this information on data sheets. For instance, the data sheet of a 2N!441 gives $V_T = 0.75$ V and $I_T = 10$ mA. When you have the value of R_G, the calculation of Vin is straightforward. Sometimes a gate resistor is not used. In this case, R_G is the Thevenin resistance of the circuit driving the gate. Unless Eq. (3-2) is satisfied, the SCR cannot turn on. After the SCR has turned on, it stays on even though you reduce Fin to zero. In this case, the output voltage remains low indefinitely. The only way to reset the SCR is to reduce its current to less than the holding current. One way to do this is by opening R_C. Another way to do this is by reducing Vcc to a low value. There are other ways to turn off the SCR, which are discussed later.

3.2.6. SCR Crowbar

If anything happens inside a power supply to cause its output voltage to go high, the results can be devastating. Why? Because some loads suchas expensive ICs cannot withstand excessive supply voltage without being destroyed. One of the most important applications of the SCR is to protect delicate and expensive loads against over-voltages from a power supply. Figure 3-8 shows a positive supply of Vcc applied to a protected load. The load is protected by the zener diode, resistor, and SCR. Under normal conditions, Vcc is less than the breakdown voltage of the zener diode. In this case, there is no voltage across R, and the SCR remains open. The load receives a voltage of Vcc, and all is well.

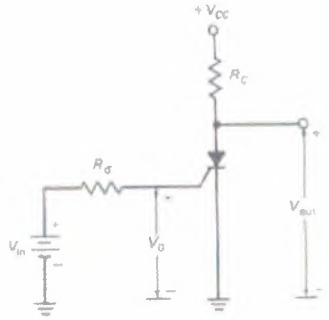


Figure 3.7 SCR circuit

Now, assume the supply voltage increases for any reason whatever. When Vcc is too large, the zener diode conducts and a voltage appears across R. If this voltage is greater

than the trigger voltage of the SCR (typically 0.7 V), the SCR turns on and conducts heavily. The action is similar to throwing a. crowbar across the load terminals. Because the SCR turn-on is very fast

(1μs for a 2N4441), the load is quickly overvoltage against the damaging effects of a large overvoltage.

Crowbarring, though a drastic form of protection, is necessary with many digital ICs; they can't take much overvoltage. Rather than destroy expensive ICs, therefore, we can use a SCR crowbar to short the load terminals at the first sign of overvoltage. Power supplies with a SCR crowbar need a fuse or current limiting to prevent excessive current when

the SCR closes.

The crowbar of Fig. 3-8 is a popular design. It is adequate for many applications, provided the components have low tolerances. More advanced crowbar circuits include transistors to improve the turn-on action. In fact, special ICs such as the RCA 5K9345 series are off-the-shelf, ready-to-use crowbars. These IC crowbars contain a zener diode, a couple of transistors, and a SCR. If you want more information on practical crowbar circuits, incidentally, there is no separate gate resistor in Fig. 3-8 as shown it Fig. 3-7. In this case, V_{in} and R_G are interpreted as the V_{TH} and R_{TH} respectively, of the circuit facing the gate of the SCR. What is this Thevenin resistance in Fig. 3-8 Looking back from the gate, you set the zener resistance in parallel with R. In a typical design, the Thevenin resistance is small. This means the equivalent input voltage needed to trigger the SCR is only slightly more than 0.7 V.

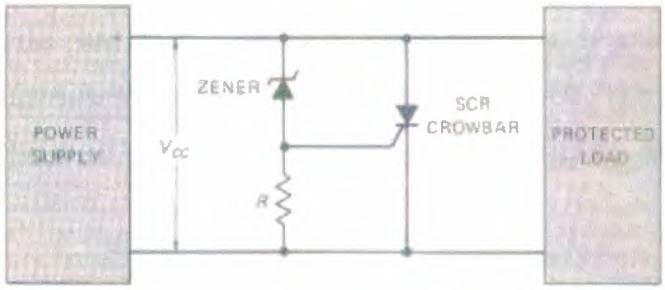


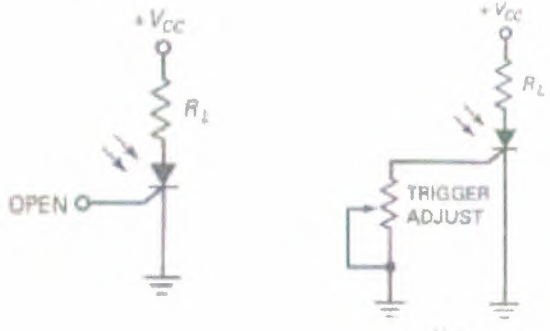
Figure 3.8 SCR crowbar

3.3. VARIATION OF THE SCR

There are other pnpn devices whose action is similar to that of the SCR.
What follows is a brief description of these SCR variations. The devices discussed are for low-power applications.

3.3.1. Photo-SCR

Figure 3-9a shows a photo-SCR also known as a light-activated SCR (LASER). The arrows represent incoming light that passes through a window and hits the depletion layers. When the light is strong enough, valence electrons are dislodged from their orbits and become free electrons.



(a) (b)

Figure 3.9 (a), (b) Photo-SCR.

When these free electrons how out of the collector of one transistor into the base of the other, the positive feedback starts and the photo-SCR closes.After a light trigger has closed the photo-stilt, it remains closed, even though the light disappears. For maximum sensitivity to light, the gate is left open, as shown m Fig. 3-9a. If you want an adjustable trip point, you can include the trigger adjust shown in Fig. 3-9b, The gate resistordiverts some of the light-produced electrons and changes the sensitivity of the circuit to the incoming light.

3.3.2. Gate-Controlled Switch

As mentioned earlier, low-current drop out is the normal way to open a SCR. But the gate-controlled switch (GCS) is designed for easy opening with a reverse-biased trigger. A GCS is closed by a positive trigger and opened by a negative trigger (or by low-

current drop out). Figure 3-10 shows a GCS circuit. Each positive trigger closes the GCS, and each negative trigger opens it. Because of this, we get the square-wave output shown. The GCS is useful in counter, digital circuits, and other applications in which a negative trigger is available for turnoff.

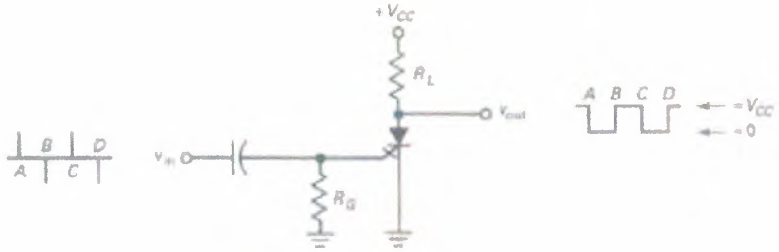


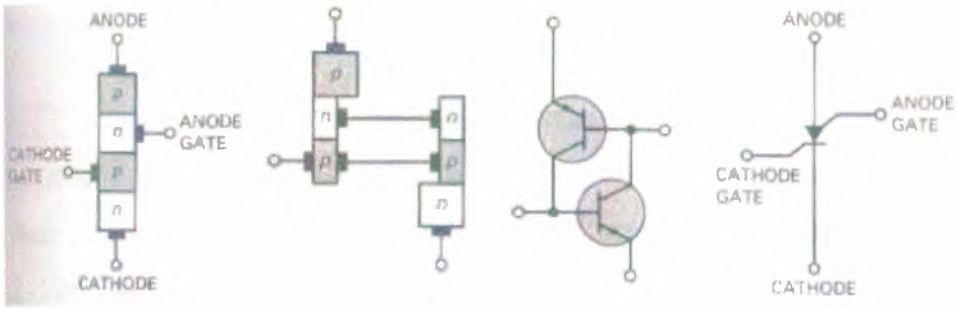
Figure 3.10 GCS circuit

3.3.3. Silicon Controlled Switch

Figure 3-11a shows the doped regions of a silicon controlled switch (SCS).

Now an external lead is connected to each doled region. Visualize the device separated into two halves (Fig. 3-11b). Therefore, it's equivalent to a latch with access to both bases (Fig. 3-11c). A forward-bias trigger on either base will close the SCS. Likewise, a reverse-bias trigger on either base will open the device.

Figure 3-11d shows the schematic symbol for a SCS. The lower gate is called the cathode gate; the upper gate is the anode gate. The SCS is a low-power device compared with the SCR. It handles currents in milli-amperes rather than amperes.



(a) (b) (c) (d)

Figure 3.11 Silicon controlled switch.

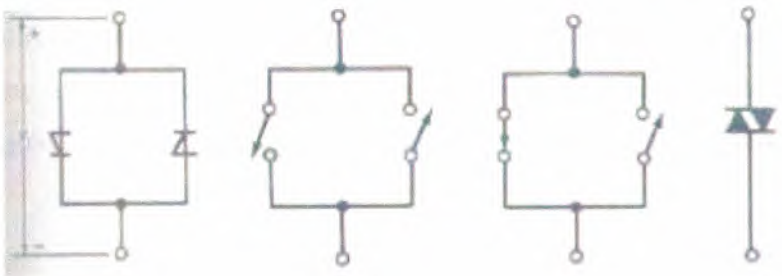
3.4. BIDCIRECTIONAL THYRISTROS

Up until now, all devices have been unidirectional; current was in only one direction. This section discuses bidirectional thyristors-devices in which the current can flow in either direction.

3.4.1. Dias

The diac run have latch current in either direction. The equivalent circuit of a diac is a pair of four-layer diodes in parallel, as shown in Fig. 3-12a, ideally the same as the latches in Fig. 3-12b The diac is nonconducting until the voltage across it tries to exceed the breakover
voltage in either direction.

For instance, if v has the clarity indicated in Fig. 15-1a, the left diode conducts when v tries to exceed the breakover voltage. In this case, the left latch closes, as shown in Fig. 3-12c. However, if the polarity of v is opposite to that of Fig. 3-12a, the result would be that the right latch closes when v tries to exceed the breakover voltage.



(a) (b) (c) (d)

Figure 3.12 Diac

Once the diac is conductible the only way to open it is by low-current drop out. This means that you must reduce the current below the rated holding current of the device. Figure 2-12d shows the schematic symbol for a disc.

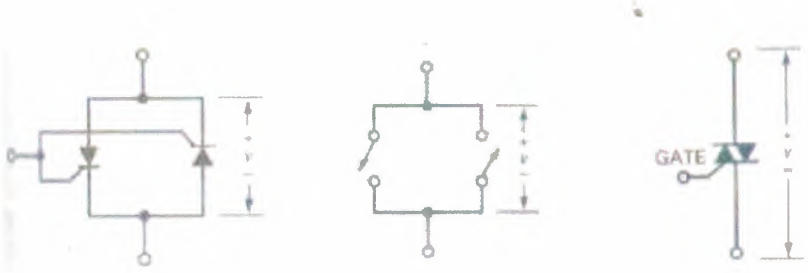


Figure 3.13 Triac,(a) (b) (c)

3.4.2. Triac

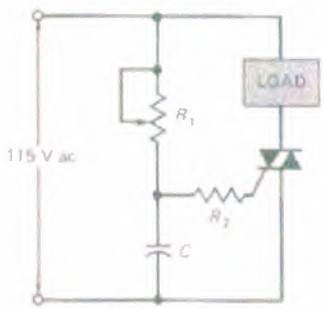
The triac arts like two SCRS in parallel (Fig. -13a), equivalent to the two latches of Fig.3-13b. Because of this, the triac can control current The breakover voltage is usually high, so that the

normal way to turn on a triac is by applying a forward-bias trigger.

Datasheets list the trigger voltage and trigger current needed to turn on a triac. If p has the clarity shown in Fig. 3-13a, we have to apply a positive trigger; this closes the left latch. When p has opposite polarity, a negative trigger is needed; it will close the right latch. Figure 3-13c is the schematic symbol for a triac.

Figure 3-14a shows a triac circuit that can be used to control the current through a heavy load. In this circuit, resistance R_1 and capacitance C shift the phase angle of the gate signal. Because of this phase shift, the gate voltage lags the line voltage by an angle between 0 and 90°. You can see these ideas in Fig. 15-18b and c. The line voltage has a phase angle

of 0°, while the capacitor voltage lags the line voltage. When the capacitor voltage is large enough to supply the trigger current, the triac conducts. Once on, the triac continues to conduct until the line voltage returns to zero.



(a)

Figure 3.14 (a)

The shaded portion of each half cycle shows you when the triac is conducting. Because R_1 is variable, the phase angle of the capacitor voltage can be changed. This allows us to control the shaded portions of the line voltage. In other words, we can control the average load currently Control like this is useful in industrial heating, lighting, and other heavy power applications.

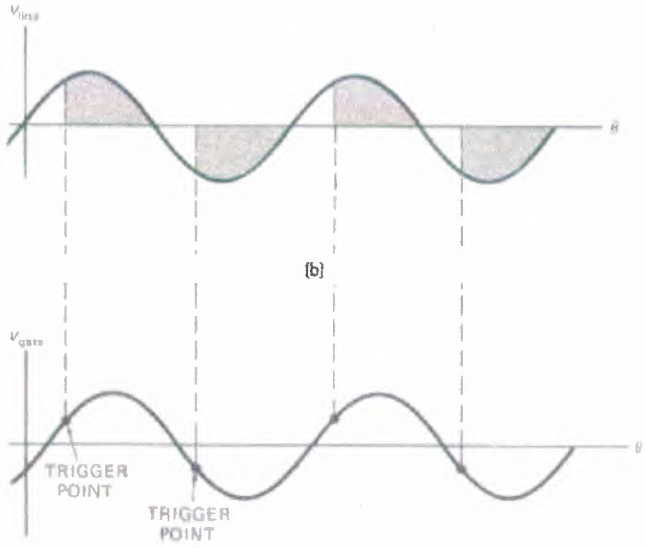


Figure 3.14 (b) and (c) Triac circuit and waveforms.

3.5. The Unijunction Transistor

The unijunction transistor (UJT) has two doped regions with three external leads (Fig. 3-15a). It has one emitter and two bases. The emitter is heavily doped, having many holes. The *n* region, however, is lightly doled. For this reason, the resistance between the bases is relatively high, typically 5 to 10 k ohm when the emitter is open. We call this the interbase resistance, symbolized by R_{bb}.

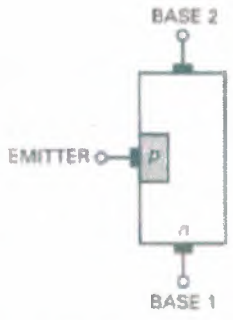


Figure 3.15 (a) structure.

3.5.1. Intrinsic Standoff Ratio

Figure 3-15b shows the equivalent circuit of a UJT. The emitter diode drives the junction of two internal resistances R_1 and R_8. When the emitter diode is nonconducting, R_{BB} is the sum of R_1 and R_2. When a supply voltage is between the two bases, as shown in Fig. 3-15c, the voltage across R_1 is given by

$$V1 = \frac{R1}{R1 + R2}(V) = \frac{R1}{R_{BB}}(V)$$

or

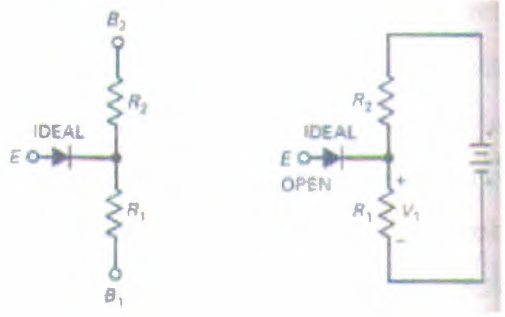
where

$$V1 = \eta V \qquad (3\text{-}3)$$

$$\eta = \frac{R1}{R_{BB}}$$

(The Greek letter (η) is pronounced eta as the *a* in face and *a* as the*a* in about.).
The quantity m is called the intrinsic standoff ratio, which is nothing more than the voltage-divider factor. The typical range of η is from 0.5 to 0.8. For instance, a 2N2646 has an m of 0.65. If this UJT is used in Fig. 3-15c with a supply voltage of 10 V then

$$V1 = \eta V = 0.65(10\ V) = 6.5\ V$$



(b) (c)

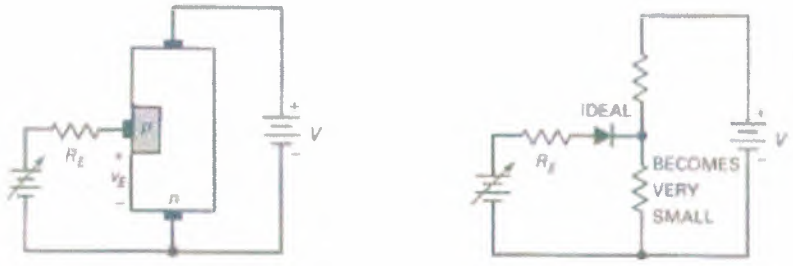
Figure 3.15 (b) equivalent circuit (c) standoff voltage

In Fig. 3-15c, V_1 is called the intrinsic standoff voltage because it keeps the emitter diode reverse-biased for all emitter voltages less than V_1. If V_1 equals 6.5 V, then ideally we have to apply slightly more than 6.5 V to the emitter to turn on the emitter diode.

3.5.2. How a UJT Works

In Fig. 3-16a, imagine that the emitter supply voltage is turned down to zero. Then the intrinsic standoff voltage reverse-biases the emitter diode. When we increase the emitter

supply voltage, V_E increases until it is slightly greater than V_1 . This turns on the emitter diode. since the p region is heavily doped compared with the *n* region, holes are injected into the lower half of the UJT. The tight doping of the n region gives these holes a long lifetime. These holes create a conducting path between the emitter and the lower base. The hooding of the lower half of the UJT with holes drastically lowers Resistance R_1 (Fig.3.16). Because R_1 is suddenly much lower in value, V_E suddenly drops to a low value, and the emitter current increases.



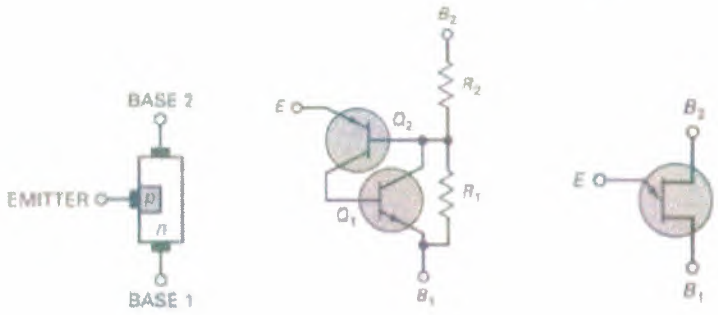
(a) (b)

Figure 3.16 (a) UJA circuit; (b) R_1 approaches zero after emitter diode turns on.

3.5.3. Latch Equivalent Circuit

One way to remember how the UJT of Fig. 3-17a works is by relating it to the latch of fig.3-17b.With a positive voltage from B_2 to B_1 , a standoff voltage V_1 appears across R_1 This keeps the emitter diode of Q2 reverse-biased as long as the emitter input voltage is less than the standoff voltage. When the emitter input voltage is slightly greater than the standoff voltage, however, Q2 turns on and positive feedback takes over. This drives both transistors into saturation, ideally shorting the emitter and the lower base.

Figure 3-17c is the schematic symbol for a UJT. The emitter arrow reminds us of the upper emitter in a latch. When the emitter voltage exceeds the standoff voltage, the latch between the emitter and the lower abase closes. Ideally, you can visualize a short between *E* and a $B_{1.To}$ asecond approximation, a low voltage called the emitter saturation $V_{E(sat)}$ appears between E and B_1.



(a) (b) (c)

Figure 3.17 (a) UJT: Structure; (b) Latch equivalent circuit ; (c) Schematic symbol.

The latch stays closed as long as the latch current (emitter current) is greater than the holding current. Data sheets specify a valley current Iv, which is equivalent to holding current. For instance, a 2N2646 has an Iv of 6 mA; to hold the latch closed, the emitter current must be greater than 6 mA.

3.6. MORE THTRISTOR APPLICATIONS

Earlier, we discussed the different kinds of thyristors including four-layer diodes, SCRs, diacs, tiac, etc. The thyristor is such an unusual control device that it can be used in a11 kinds of ways. Thyrfstors have become increasingly popular for controlling ac power to resistive and inductive loads, such as motors, solenoids, and heating elements. Compared with competing devices like relays, thyristors offer lower cost and better reliability. This section discusses some applications of thyristors to give you an idea of the variety of ways in which they can be used.

3.6.1. Overvoltage Detector

Figure 3-18 shows a circuit known as an overvoltage detector. Here is how it works: The four-layer diode has a breakover voltage of 10 V. As long as the power supply puts out 9 V, the four-layer diode is open and the lamp is dark. But if something goes wrong with the power supply and its voltage rises above 10 V, then the four-layer diode breaks over

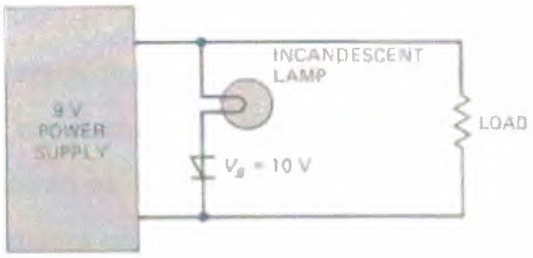


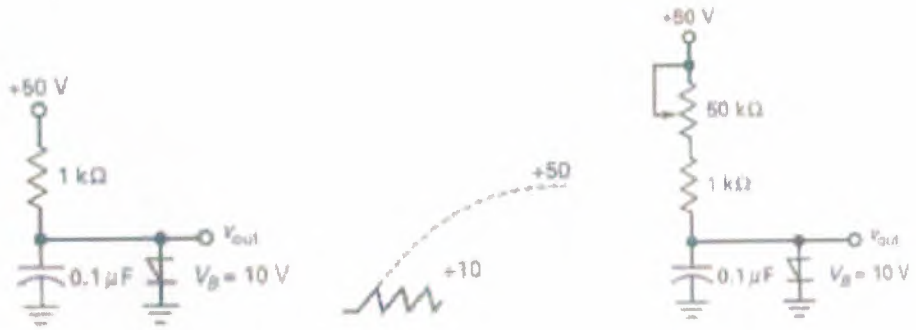
Figure 3.18 Overvoltage detector.

and the lamp comes on. Even if the supply should return to 9 V, the diode remains latched as a faxed indication of the overvoltage that has occurred. The only way to make the lamp go out is to turn off the supply.

3.6.2. Sawtooth Generator

Figure 3-19a shows a sawtooth generator. If the four-layer diode were not in the circuit, the capacitor would charge exponentially, and its voltage would follow the dashed curve of Fig. 3-19b. But the four-layer diode is in the circuit. Therefore, as soon as the capacitor voltage reaches 10 V, the diode breaks over and the latch closes. This discharges the capacitor, producing the flyback (sudden decrease) of capacitor voltage. At some point on the fatback, the current drops below the holding current, and the four-layer diode opens. The next cycle then begins.

Figure 3-19a is an example of a relaxation oscillator, a circuit whose output depends on the charging and discharging of a capacitor (or inductor). If we increase the RC time constant, then the capacitor takes longer to charge to 10 V and the frequency of the sawtooth wave is lower. For instance, with the potentiometer of Fig. 3-19c we can get a 50:1range in frequency.



(a) (b) (c)

Figure 3.19 Sawtooth generator

3.6.3. SCR Crowbar

Because the knee of the zener diode is curved rather than sharp, the basic SCR crowbar discussed earlier has a *sop turn-on.* this crowbar circuit can be improved by adding some voltage gain as shown an Fig. 3.20. the transistor provides voltage gain which produces a much sharper turn on. When the voltage across R4 exceeds approximately 0.7 v the SCR turns on. An ordinary diode is included for temperature compensation of the transistor's base-emitter diode. The trigger adjust allows us to set the trip mint of the circuit, typically around 10 to 15 percent above the normal voltage.

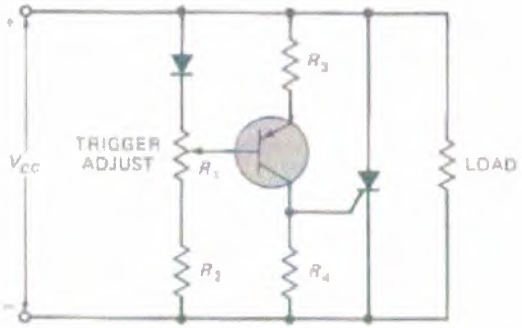


Figure 3.20 SCR crowbar.

Figure 3-21 shows an even better solution. The triangular box is an IC called a comparator. This IC produces avary large voltage gain typically 100,000as or more. the input to this IC is between the plus and minus input terminals. Because of its large voltage gain, the IC can detect the slightest overvoltage. The zener diode produces 10 V, which goes to the minus (put of the comparator. The trigger adjust produces slightly less than 10 V for the plus input. As a result, the

input Voltage to the compactor is negative. The output of the comparator is also negative, which cannot trigger the SCR. If the supply voltage tries

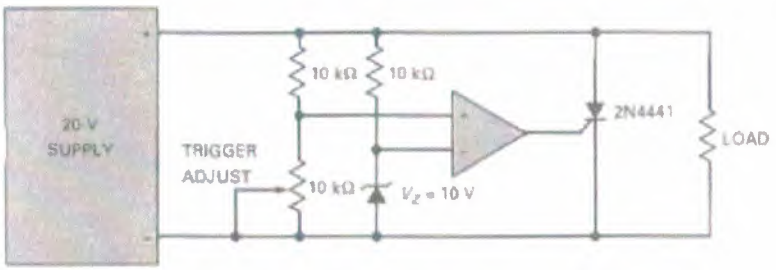


Figure 3.21 Another SCR crowbar

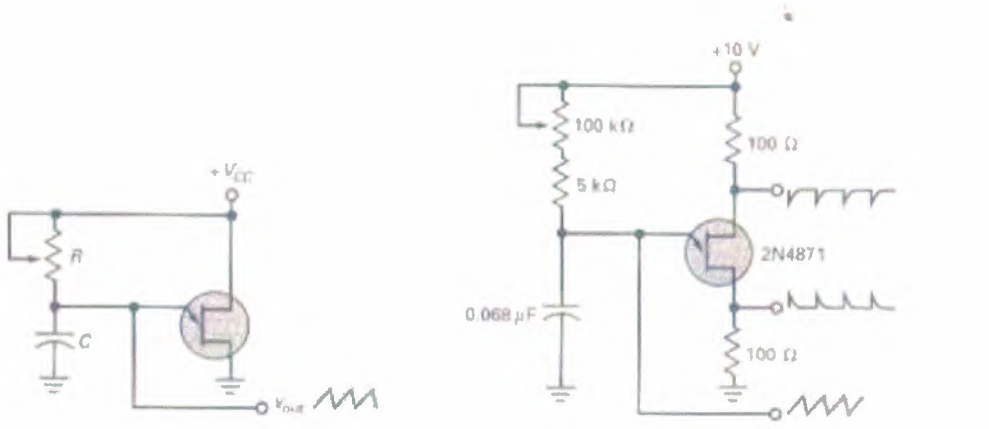
to rise above 20V, the plus input of the comparator becomes greater than 10 V. Since the input voltage is positive, tile output of the comparator becomes positive and drives the SCR into conduction. This rapidly shuts down the supply by crowbarring the load terminals.

The simplest solution when you need a crowbar is to use an IC crowbar as shown in Fig. 3-22. An IC crowbar is an integrated circuit with a zener diode for detection, transistors for voltage gain, and an SCR for crowbarring. The popular RCA SK9345 series is an example of what is commercially available. The SK9345 protects power supplies of + 5 V, the 5K9346 protects + 12 V, and the SK9347 protects + 15 V. For instance, if an SK9345 is used in Fig. 15-28, it will protect the load for a nominal supply voltage of + 5 V. The data sheet of an SK9345 indicates that it fares at + 6.6 V with a tolerance of $\pm$ 0.2 V.

Figure 3.22 IC crowbar

3.6.4. UJR Relaxation Oscillator

Figure 3-23a shows a UJT relaxation oscillator. The action is similar to that of the four-layer diode relaxation oscillator. The capacitor charges toward Vcc, but as soon as its voltage exceeds the standoff voltage, the UJT closes. This discharges the capacitor until low-current drop out occurs. As soon as the UJT opens, the next cycle begins. As a result, we get a sawtooth output.



(a) (b)

Figure 3.23 UJT circuits : (a) Sawtooth generator, (b) Sawtooth trigger output

If we add a small resistor to each base circuit, we can get three useful outputs: sawteeth waves, positive triggers, and negative triggers, as shown in Fig. 3-23b. The triggers appear during the fatback of the sawtooth because the UJT conducts heavily at this time. With the values of Fig. 3-23b, the frequency can be adjusted between 50 Hz and 1 kHz (approximately).

3.6.5. Automobile Ignition

Sharp trigger pulses out of a UJT relaxation oscillator can be used to trigger an SCR. For instance, Fig. 3-24 shows part of an automobile ignition system. With the distributor points open, the capacitor charges exponentially toward + 12 V. As soon as the capacitor voltage exceeds the intrinsic standoff voltage, the UJT conducts heavily through the primary winding. The secondary voltage then triggers the SCR. When the SCR latches shut, the positive end of the output capacitor is suddenly founded. As the output capacitor discharges through the ignition coil, a high-voltage pulse drives one of the spark plugs. When the mints close, the circuit resets itself in preparation for the next cycle.

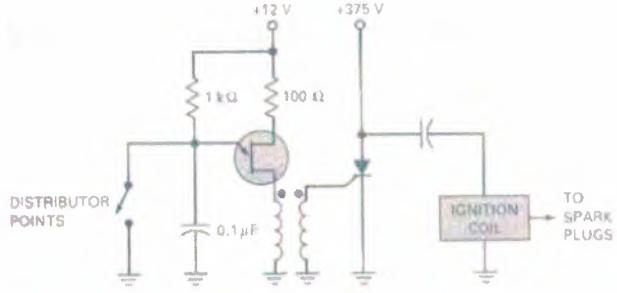


Figure 3.24 UJT trigger SCR to produce spark for automobile ignition.

3.6.6. Optocoupler Control

Figure 3-25 is an example of optocoupler control. When an input pulse turns on the LED (D_4), its light activates the photo-SCR. In turn, this produces a trigger voltage for the main SCR (D2). In this way, we get isolated control of the positive half cycles of line voltage. An ordinary diode D_1 is needed to protect the SCR from inductive kickback and transients that may occur during the reverse half cycle.

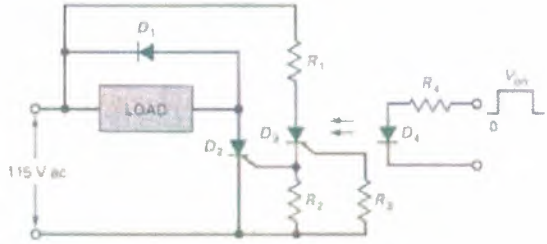


Figure 3.25 Operator control of SCR

3.6.7. Diac-Triggered SCR

In Fig. 3-26, the full-wave output from a bridge rectifier drives a SCR that is controlled by a disc and an RC charging circuit. By adjusting R_1,we can change the time constant and control the mint at which the diac fires. Circuits like these can easily control several hundred watts of power to a lamp, heater, or other load. A four-layer diode could be used instead of a diac.

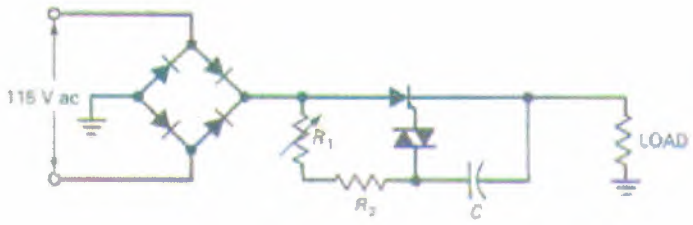


Figure 3.26 Controlling the conduction angle of a SCR.

3.7. PROJECT: MODIFICATION OF THE THYRISTOR GATE CONTROL SYSTEM OF THE PS MAIN MAGNET POWER SUPPLY

3.7.1. Introduction

The PS Main Magnet Power Supply (MPS) is a large twelve-pulse controlled-rectifier, designed to deliver 6.4kA DC witht a maximum output voltage of 9 kV approximately.

It involves two series-connected 12-pulse thyristorized converters, supplying the bending magnets in a symmetrical topology as depicted in Figure 1. The 6.6kV mains for the thyristorized power converters is obtained through two transformer stations from a 42MVA alternator, which is driven by a 6MW synchronous motor. A filter stage between the power converter and the load reduces the output peak-to-peak voltage ripple to the allowed limits.

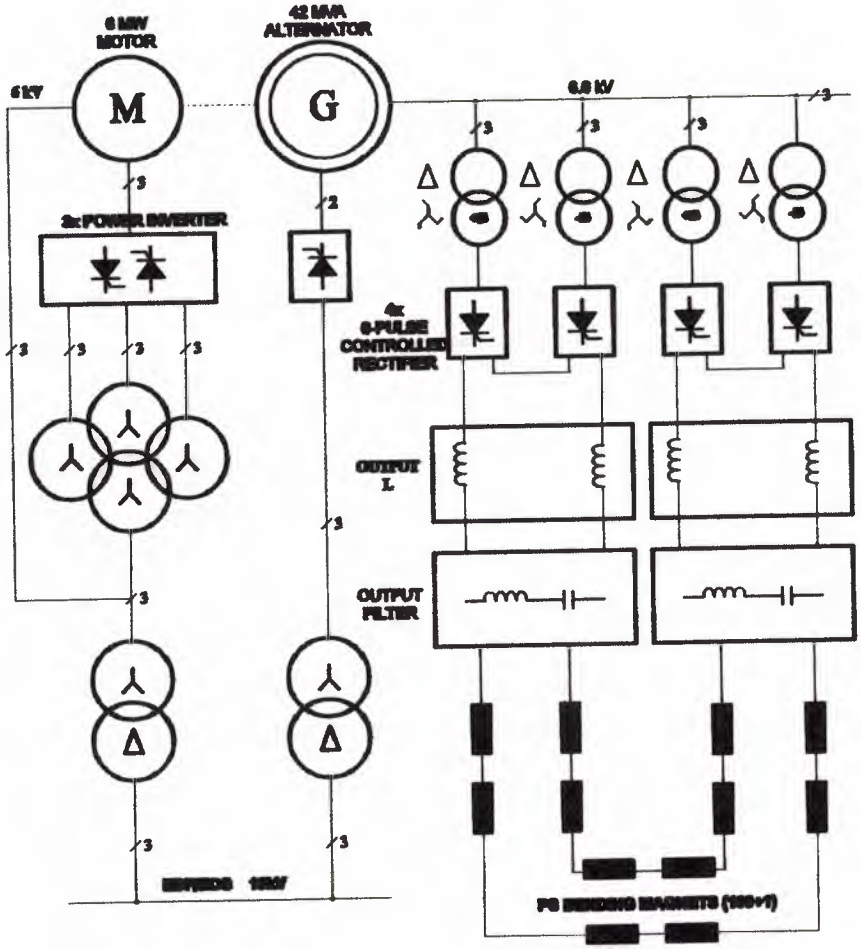


Figure 3.27 Overview of the PS Main Power Supply

The most severe constraints on the MPS arise from the need for a precision and time-response repeatability better than 50 ppm in the tenths of megawatt output power range. Hence, every element in the system becomes extremely critical. Besides hundreds of subtle issues affecting the overall precision, ranging from the geometric symmetry of the physical layout to the tight tolerances of the power transformers, the converter's performance mainly relies on:

a)-The motor-alternator assembly open loop dynamics.

b)-The motor's speed / power control system.

c)-The alternator's voltage control system.

d)-The power converter, which involves:

d.1)-The converter's topology.

d.2)-The output filter.

d.3)-The load.

e)-The control system of the power converter.

f)-The reference input.

From a control point of view, it is clear that there are strong cross-interactions between any of the sub-systems, a) through e), previously cited. For instance, I)-the proper tuning of the multi-resonant output filter depends on the alternator's speed; II)-the load time-constant influences the bandwidth of the control system of the power converter; III)-the motor's speed is affected by the alternator's load.

In this report, a short discussion on the control system of the power converter is firstly presented. Some possible improvements to this system are suggested. In the following paragraphs, the relevance of the thyristor gate controller (TGC) as a part of the power conversion plant and the currently used TGC fixture are briefly discussed. Finally, a different approach to develop an improved TGC, which accounts for the observed disadvantages of the existing one, is proposed.

3.7.2. Overview of the Control System of the Power Converter

The objective of this paragraph is to introduce the control architecture of the power converter in order to set the basis for further discussion. To this end, the control system of the power converter will be considered by itself, as if there were no interaction with the different control systems (i.e.: the motor's speed/power controller and the alternator's voltage controller). The global analysis of the whole as one multiple input-output system, though advisable, is out of scope and does not add any useful information in what the TGC concerns.

The control scheme for the power converter is shown in Figure 3.28.

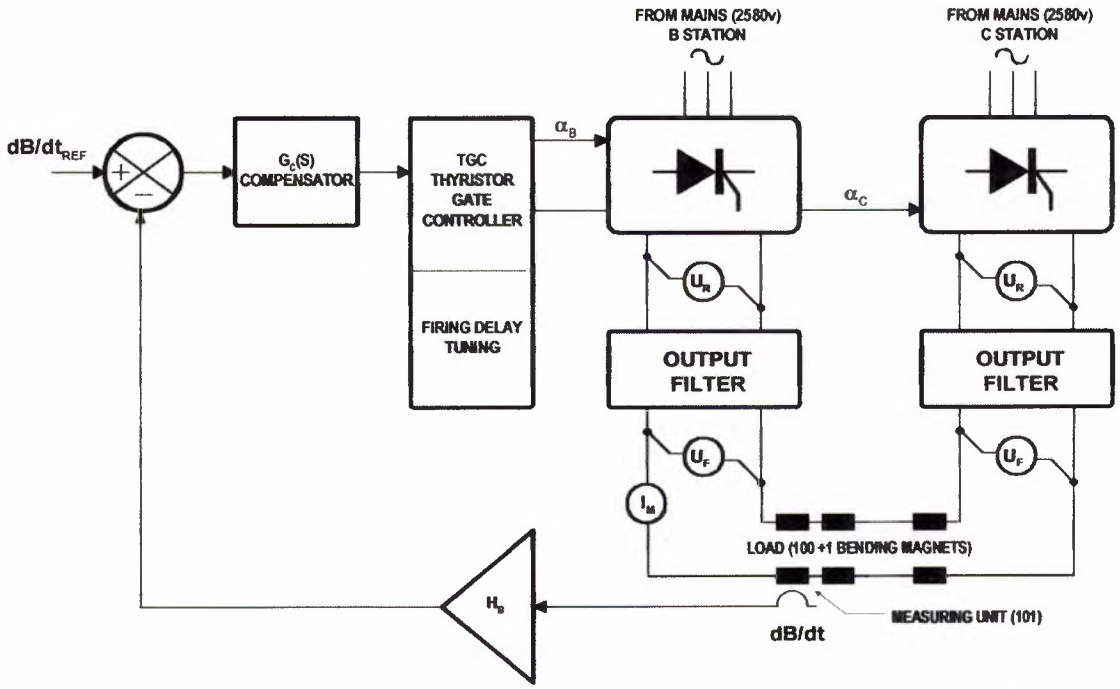


Figure 3.29 Simplified control block diagram for the Power Converter

The isocenter's magnetic field density **B** is the very fundamental physical magnitude on the bending magnets because it mainly defines the trajectory and stability of the particle beam. So, the servosystem managing the power converter should be devoted to control this variable. Owing to technological problems, a fast and accurate enough magnetic field transducer is not available, yet. Hence, several approaches were developed in the past to obtain a useful feedback signal as close as possible to **B** in a single loop topology. Firstly the filtered output voltage U_F was used, then the output current and finally the d|**B**|/dt, which is in use at present.

The time response and accuracy of the power converter under d|**B**|/dt control is roughly given by the reference signal and the feedback path, as in every SISO system. However, two aspects related to both signals should be remarked:

a)-The reference input from the MCR is actually digital but, as far as the controller is analog, a pair of 16-bit DAC converter are used outside the loop.

b)-The analog feedback signal comes from a pick-up coil mounted on a reference magnet (# 101), built exactly the same way than the one hundred PS's bending magnets. All the magnets are series-connected, such that the same current drives also the reference magnet.

Having a digital reference for d|**B**|/dt, it is reasonable to think of transforming the analog controller into a digital one. This would lead to a most accurate system from the reference point of view. On the other hand, a digital reference also imposes a digital feedback involving an A to D conversion on the measured d|**B**|/dt signal, which could degrade the closed loop performance. An A/D converter in the loop (in this case in the feedback path) adds a staircase-like non-linearity with the corresponding limit-cycling control behavior due to signal quantization. According to the required precision for the power supply, a fast and linear 18-bit A/D converter should be necessary. Although, taking into account the problems to develop such an accurate converter in order not to degrade the loop performance, the digital option provides several improvements to the control system. For instance, high reproducibility, no aging or thermal drifts on the internal parameters, capability to implement non-linear controllers, flexibility to make changes at no extra cost, high reliability and low component count.

A further improvement on the system could consist of the addition of an inner loop to control the rectified voltage U_R. This technique is frequently found on different thyristorized power supplies at PS and provides mainly the following benefits: a)-Linearization of the power converter; b)-Rejection to disturbances from the mains (motor-alternator assembly), low frequency voltage sags and 50Hz-related components.

To implement a digital inner loop around the rectified voltage U_R it is necessary to split the control signals at the TGC level, because of the balanced topology of the power converter. The TGC acts as a kind of modulator, translating the dimensionless digital magnitude (or a voltage in the analog case) to a selected firing event with a precise phase lag respect to the mains' phase. More basic details about several types of TGC's can be found on the attached material and in the following section.

Finally, it is important to remark that the most important source of disturbances on the converter is the fact of being supplied by a weak mains. That is, a generator set that:

a)-Has a relatively high output impedance.

b)-Its output frequency/phase time response depends strongly on the ratio of the delivered electric energy to the total kinetic energy on the axis.

c)-Has a limited electric power capacity related to the load, which leads to severe stator voltage transients during longer than expected, despite the excitation control. (Figure 3 and 4)

Note that:

Regarding the control system, it is suggested to:

1. Add a digital inner loop on U_R to reduce disturbances.
2. Replace the analog control system by a digital one.
3. Substitute the currently used TGC by a more precise digital TGC.

3.7.3. The TGC (Thyristor Gate Control) Subsystem

As stated above, the TGC subsystem can be regarded as a type of modulator, because it translates a digital dimensionless magnitude into a precise delay for periodical firing events. Much of the converter's performance relies on the TGC's precision. There are several hardware strategies to implement a TGC whose descriptions may be easily found elsewhere in the literature but, for the sake of clearness, only the currently used approach will be discussed.

3.7.4. Current approach for the TGC

At present, the MPS employs the thirty-years-old TGC from Brown Boveri Co.. It is based on an elementary operating principle that can be understood with the aid of Figure 3.29 .

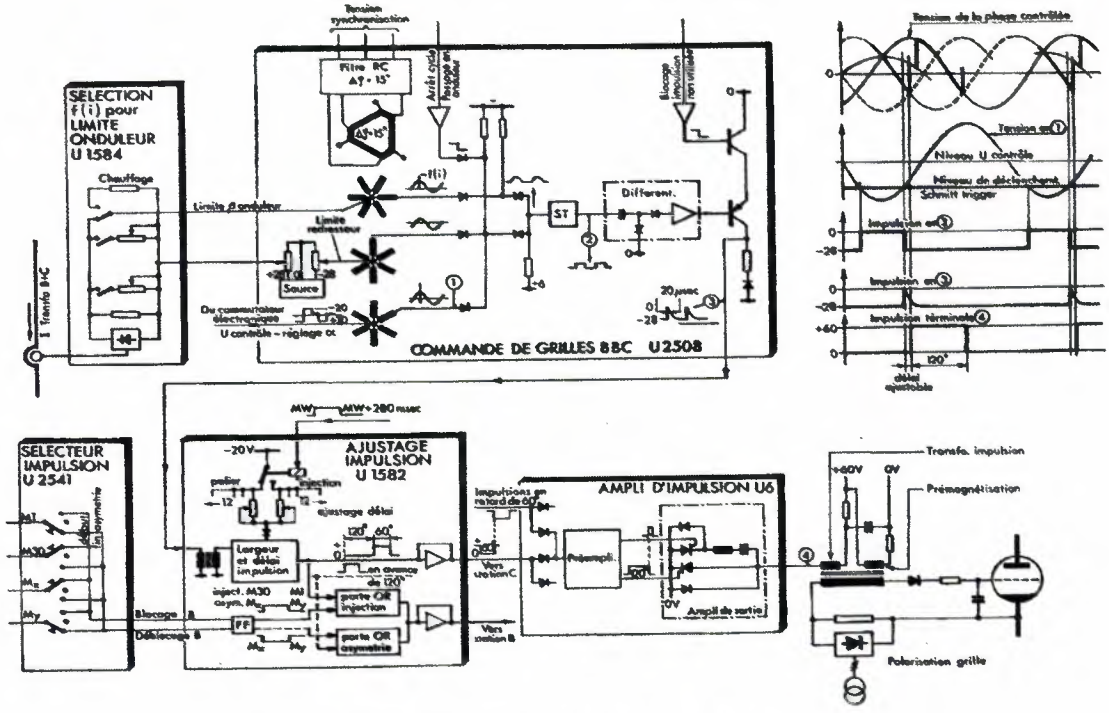


Fig. 87 Schéma bloc de la commande de grilles

Figure 3.29 Block diagram of the BBC's Thyristor gate controller

From Figure3.30 it can be seen that the input variable to the TGC is the neutral-to-ground unbalancing voltage of a zig-zag wounded measuring transformer. The input voltage shifts the transformer's sinusoidal output voltage adding a slowly changing value and following, a schmitt-trigger compares the later signal to zero within a given hysteresis. A monostable circuit provides a time-variable event at the falling edge, accordingly. Before reaching the thyristor stages, the triggering pulses successively passes by a manual delay tuning, by a pulse-stretching circuit, by an optocoupler, by a pulse amplifier, by an optic fiber driver and finally by a capacitor-discharge gating circuit.

In order to compensate for voltage asymmetries on the mains and for uneven firing delays, which would lead to an increase in the subharmonic content otherwise, a fine delay-tuning fixture was devised. The adjustment of the delay for each thyristor is performed at two output current levels, during low and high-energy flat tops.

3.7.5. Advantages of the BBC Thyristor gate controller

a)-There is no need for additional synchronism with the mains.

b)-It has a fast time response.

c)-To some extent, voltage sags on the alternator's output are instantaneously compensated for.

d)-Possibility of manual tuning of each firing delay to reduce subharmonics.

3.7.6. Disadvantages of the BBC Thyristor gate controller

a)-Non-linearity.

b)-Low precision, aging and thermal dependence.

c)-High component count and complexity.

d)-High uncertainty on firing events:

e)-Asymmetric operation of both stations is not possible.

f)-A firing jitter of +/- 3.5□S at the flat top of the highest energy cycle was measured. (Figures 7 and 8).

g)-As the mains frequency changes, a variable delay is produced by the use of an RC filter (Figure 5) introducing a phase shift of 15°at 50Hz.

h)-Thermal drift on the RC input filter lead to differences on the firing angle □ for a constant input voltage.

I)-Asymmetries on the RC input filter can increase the 300Hz subharmonic component of the output ripple.

j)-The firing pulses are not necessarily equally spaced, depending on the phase-voltage degree of symmetry.

k)-A distorted mains affects its operation.

There are some interesting aspects related to the system's input voltage waveforms that must be also taken into account to develop a high-performance TGC. The first point concerns thyristor's overlapping, which severely distorts the alternator's output particularly at high output current as can be seen in Figure 9. From the waveform, it can be understood that if this signal is used unfiltered to determine the firing event -as in the case of BBC's TGC- some unpredictable loss of precision may result. Even if the disturbance on the mains is created by the very TGC and it appears right after the delivery of the gating pulse, it takes some time for the generator to recover from this transient overload. Pending the overlap, the delay for the next pulse in the sequence is being prepared using the distorted sinus. Under a different approach, a TGC based on a tight synchronism with the mains phase, would require processing resources in order to get rid of the distortion without adding any frequency-dependent phase lag.

The second interesting aspect to consider is that both, the amplitude of the harmonic components of output ripple as well as its total RMS value, are strongly affected by the overlap angle. Figure 10 helps to notice how the 600Hz fundamental decreases meanwhile the 1200Hz second harmonic increases on the rectified voltage U_R, as the current rises.

The third subject related to the performance of the existing TGC in the system is the presence of current-dependent triggering delays.

3.7.7. The New TGC for the PS Main Power Supply Project

This project deals with the development of a new Thyristor Gate Control for the controlled rectifier of the MPS. As a reference on this matter, previous works in devising high-performance digital TGC's can be cited (Ref [2]). The proposition for this project is reflected on the physical block diagram shown in Figure 12. More information will shortly be provided in the form of a functional block diagram.

The block diagram of Figure 12 shows a flexible hardware topology, suitable for this project. The block marked Master Delay Generator is embedded in an FPGA from Xilinx, using almost the same approach than that described in [2] but duplicated in order to allow a separated triggering control for stations B and C. The DSP core has to:

a)-Run the filtering algorithm on the synch variables.

b)-Manage memory data transfer, acquisition events and I/O signals (A/D and D/A)

c)-Provide asymmetric firing for both stations in order to reduce voltage ripple on U_R.

d)-Set the firing limits on □, according to the parameters provided through the front-end G64 PCB.

e)-Set the self calibrating mode for the 16-bit A/D converters.

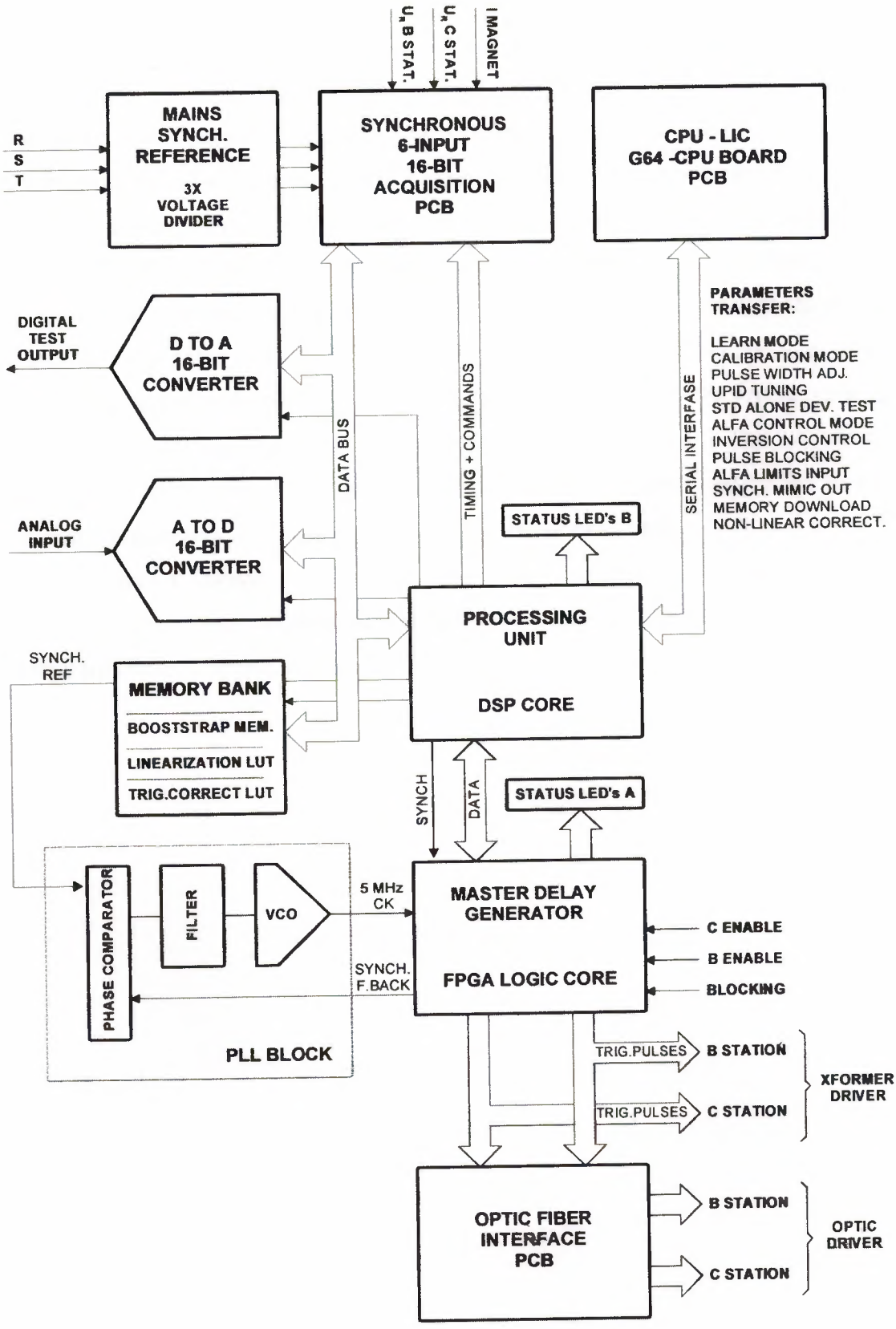
f)-Generate a test mode function to adjust the firing angles.

g)-Run the UPID algorithm for the voltage loop.

h)-Manage the serial communication with the front-end controller.

i)-Deliver the synch. train pulses to the PLL.

Figure 2.30 New TGC project Block Diagr


U_R B STAT.
U_R C STAT.
I MAGNET
R
S
T
MAINS SYNCH. REFERENCE
3X VOLTAGE DIVIDER
SYNCHRONOUS 6-INPUT 16-BIT ACQUISITION PCB
CPU - LIC G64 -CPU BOARD PCB
PARAMETERS TRANSFER:
LEARN MODE
CALIBRATION MODE
PULSE WIDTH ADJ.
UPID TUNING
STD ALONE DEV. TEST
ALFA CONTROL MODE
INVERSION CONTROL
PULSE BLOCKING
ALFA LIMITS INPUT
SYNCH. MIMIC OUT
MEMORY DOWNLOAD
NON-LINEAR CORRECT.
SERIAL INTERFASE
DIGITAL TEST OUTPUT
D TO A 16-BIT CONVERTER
DATA BUS
TIMING + COMMANDS
ANALOG INPUT
A TO D 16-BIT CONVERTER
STATUS LED's B
PROCESSING UNIT
DSP CORE
SYNCH. REF
MEMORY BANK
BOOSTSTRAP MEM.
LINEARIZATION LUT
TRIG.CORRECT LUT
SYNCH
DATA
STATUS LED's A
PHASE COMPARATOR
FILTER
VCO
5 MHz CK
SYNCH. F.BACK
PLL BLOCK
MASTER DELAY GENERATOR
FPGA LOGIC CORE
C ENABLE
B ENABLE
BLOCKING
TRIG.PULSES
B STATION
TRIG.PULSES
C STATION
XFORMER DRIVER
OPTIC FIBER INTERFACE PCB
B STATION
C STATION
OPTIC DRIVER

The system takes the synchronism from the mains, through the existing 1kVA reference transformer. A filtering algorithm on the input synch signals is necessary in order to get rid of the strong amplitude disturbances without a frequency-dependent phase shift. A 16-bit wide digital word is sent to the master delay generator, which produces the firing events to the corresponding thyristors with a delay according to this input. The memory bank contains also a look-up table to compensate for the converter's non-linear transfer function. The maximum and minimum alpha values are downloaded from the front-end.

There is a possibility to perform asymmetric triggering of stations B and C in order to reduce the output peak-to-peak ripple. The system also allows –in the first approach- the individual manual correction of the triggering events to +/-1°. This procedure is expected to be performed only once at start-up for two different current flat tops. The data for subharmonic compensation is stored in the memory bank.

As an additional feature, it will also possible to operate in U_R closed-loop mode. Both feedback signals are synchronically sampled by means of the acquisition PCB. The UPID parameters are introduced also through the front-end.

CONCLUSION

After reading the technical study, of lamp chaser circuits design using power electronics components, we could be able to understand the real importance of power electronics and its validity and applicability to the most vital and essential electronics projects, as we have noticed in the 12volt lamp chaser circuit.

Also we could understand by the brief explanations to describe the basic construction of a JFET, and draw a diagram showing how it is normally biased. The term field effect is related to the depletion layers around each *p* region. The junctions between each *p* region and the *n* regions have depletion layers because free electrons diffuse from the *n* regions into the *p* regions, and we could understand that the thyristor is a semiconductor device that contains three or more junctions, and that has current voltage characteristics. The term has most often been to silicon controlled rectifiers, but also applies to other npnp devices.

Finally and through the power electronics technique we could have constructed a D.C. lamp chaser circuit that, a number of lights are arranged so that they turn on sequentially, with present time delay between each operation (lamp control circuit) , until they finally on together.

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