NEAR EAST UNIVERSITY

Faculty of Engineering

Department of Electrical and Electronic Engineering

DTMF RECEIVER CIRCUIT

Graduation Project
EE - 400

Student: Mehmet Dağaştı (990071)

Supervisor: Asst. Prof. Dr. Kadri Büründcük

Nicosia 2007

ACKNOWLEDGMENTS

First of all I want to represent all my thanks to Asst. Prof. Dr. Kadri Büründcük who was supervisor of my project. He guided me with his wide experiences, knowledge and patience. He supported and corrected me in each phase of my project. With his knowledge I over come some difficulties during my project and I believe these knowledge's and experiences will help me in my future.

Special thanks to Dr. Özgür Cemal Özerdem for his kindly help during my education life.

I want to thanks Dr. Kaan Uyar to help me about digital logic part of my project.

I also want to represent my thanks to SAHA Elektronik. They helped me to find necessary components for my project.

Finally I also want to thank to my fiancée, all my family especially to my parents. They always with me and help me during my education.

ABSTRACT

Nowadays every household have to work to gain money and live more comfortable so they spend more time for their works, waiting for heater, washing machine and for other equipments loose time. Those reasons bring automation for houses. Automations generally uses timer bases systems but sometimes these systems doesn't satisfy people's need and wireless controllers are not reliable and also has a range. In this project telephone lines are used as a carrier so there is no range limit for controlling. This project designed for remote house appliances controlling with using DTMF signals. The circuit can control Heater, Central heating unit, Microwave, Air-condition, Washing machine, Dishwasher, Home security system, Oven and Outdoor lamps.

TABLE OF CONTENTS

INTRODUCTION

The purpose of this project is to provide information on the operation and application of DTMF (dual tone multi frequency) Receivers. The CM 8870pi integrated DTMF receiver will be discussed in detail and its use illustrated in the application example.

More than 25 years ago the need for improved method for transferring dialling information through the telephone network was recognised. The traditional method, dial pulse signalling, was not only slow, suffering severe distortion over long wire loops, but required a DC path through the communications channel.

A signalling scheme was developed utilizing voice frequency tones and implemented as a very reliable alternative to pulse dialling. This scheme is known as DTMF.

The DTMF (Dual Tone Multi Frequency) is a tone composed of two different frequencies. It is basically used for communication.

In this project DTMF is used for controlling nine different appliances, switching them on or off. The DTMF signals on telephone instrument are used as control signals. The digit '0' in DTMF mode is used to toggle between the appliance mode and normal telephone operation mode. Thus the telephone can be used to switch on or switch off the appliances also while being used for normal conversation.

The chapter 1 introduce DTMF and explains idea of DTMF. Why use of DTMF necessary and advantages of it explained in this chapter.

The chapter 2 presents information and use of DTMF generator & decoder ICs (integrated circuits)

The chapter 3 represents DTMF controlled home appliances circuit. How to control home appliances with using DTMF decoders and problem occurred while wiring circuit.

CHAPTER 1: DTMF

1.1 What is DTMF?

DTMF signal is one that consists of only the sum of two pure sinusoids at valid frequencies. Those are frequencies one from high tone group and one from low tone group. Table 1.1 shows both high and low tone group. DTMF standards specify 50ms tone and 50ms space duration. Busy signal 480 Hz 620 Hz ,Dial tone 350 Hz 440 Hz, Ring-back tone (US) 440 Hz 480 Hz.

Table 1.1 High & Low DTMF tone groups [Ref.4]

Low tones group

High tones group

Tones	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

Phone systems used a system known as pulse (DP in the USA) or loop disconnect (LD) Signaling to dial numbers, which works by rapidly disconnecting and connecting the calling party's phone line, like flicking a light switch on and off. The repeated connection and disconnection, as the dial spins, Sounds like a series of clicks. The exchange equipment counts those clicks or dial pulses to determine the called number.

LD range was restricted by telegraphic distortion and other technical problems, and placing calls over longer distances required either operator assistance (operators used an earlier kind of multi-frequency dial) or the provision of subscriber trunk dialling equipment.

DTMF was developed at Bell Labs in order to allow dialing signals to dial long-distance numbers, potentially over nonwire links such as microwave links or satellites. For a few non crossbar offices, encoder/decoders were added that would convert the older pulse signals into DTMF tones and play them down the line to the remote end office. At the

remote site another encoder/decoder could decode the tones and perform pulse dialing, for example for Strowger switches. It was as if you were connected directly to that end office, yet the signaling would work over any sort of link. This idea of using the existing network for signaling as well as the message is known as in-band signaling. It was clear even in the late 1950s when DTMF was being developed the future of switching lay in electronic switches, as opposed to the electromechanical crossbar systems then in use either switching system could use either dial system, but DTMF promised shorter holding times, which was more important in the larger and more complex registers used in crossbar systems. In this case pulse dialling made no sense at any point in the circuit, and plans were made to roll DTMF out to end users as soon as possible.

Tests of the system occurred in the early 1960s, where DTMF became known as Touch Tone. Though Touch Tone phones were already in use in a few places, they were vigorously promoted at the 1964 New York World's Fair. The Touch Tone system also introduced a standardized keypad layout.

1.2 Why Two Tones?

Why are two tones used instead of just one? A dual tone design requires fewer tone detectors in the dial register of the central office than a single tone design would. A dual tone design also reduces the sensitivity requirement of the receiver which allows it to recognize tone distortion caused by abnormal conditions such as line noise on a local loop.

DTMF tones must be sounded at least 40 ms in order for the register at the central office to recognize the tones with a 60 ms pause between digits. (33% faster than rotary dial, which takes an average of 1.5s per digit to dial) The use of two frequencies is also removes the chance of deducting voice or noise as a tone.

1.3 DTMF Generating and Generator Chips

The DTMF generator circuit is straight forward to construct. Only 3 of the MT 5089's 4 column pins (3, 4, and 5) and all 4 row pins (11 to 14) were used. Thus it uses only 12 of the 16 touch tones. In figure 1.3.1 you'll note the "/" in front of column and row pin labels (e.g. /C1).

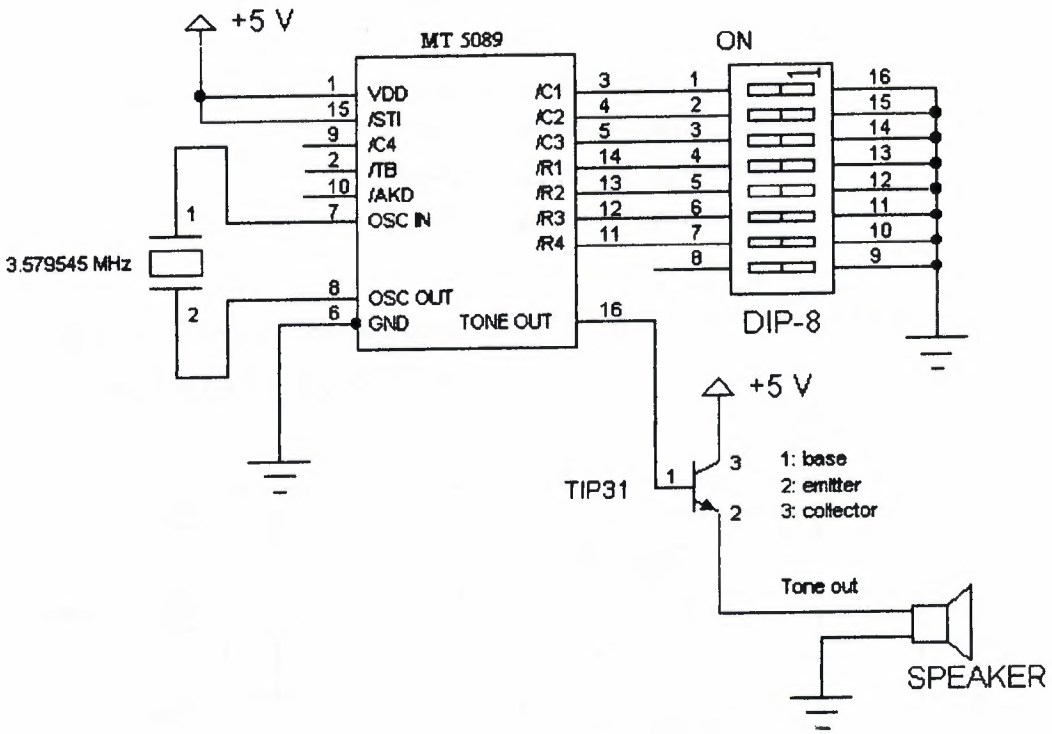


Figure 1.3.1 Simple DTMF tone generator IC

This means that these pins are active low. In other words, a pin is enabled when it is grounded.

When the circuit is powered on, these pins normally high (+5V), C1-C3 and R1-R4 are wired to an 8-position DIP switch. In a single-package this DIP contains 8 single-pole-single-throw (SPST) switches. You slide a DIP position to open or close its switch. When closed that particular switch connects its associated column or row pin to ground and makes it active. Table 1.3.1 shows the DIP positions that will activate the tone associated with the key. The numbers in bold and parenthesis are your desired key tone. Thus if you wanted to dial a "0", you would slide only positions 2 and 7 on the DIP switch.

Table 1.3.1 Dip switch positions

(1) DIP: 1+4	(2) DIP: 2+4	(3) DIP: 3+4
(4) DIP: 1+5	(5) DIP: 2+5	(6) DIP: 3+5
(7) DIP: 1+6	(8) DIP: 2+6	(9) DIP: 3+6
(*) DIP: 1+7	(0) DIP: 2+7	(#) DIP: 3+7

Figure 1.3.2 shows the block diagram of MT 5089 Touch Tone Generator and table 1.3.2 shows the characteristics of MT 5089.

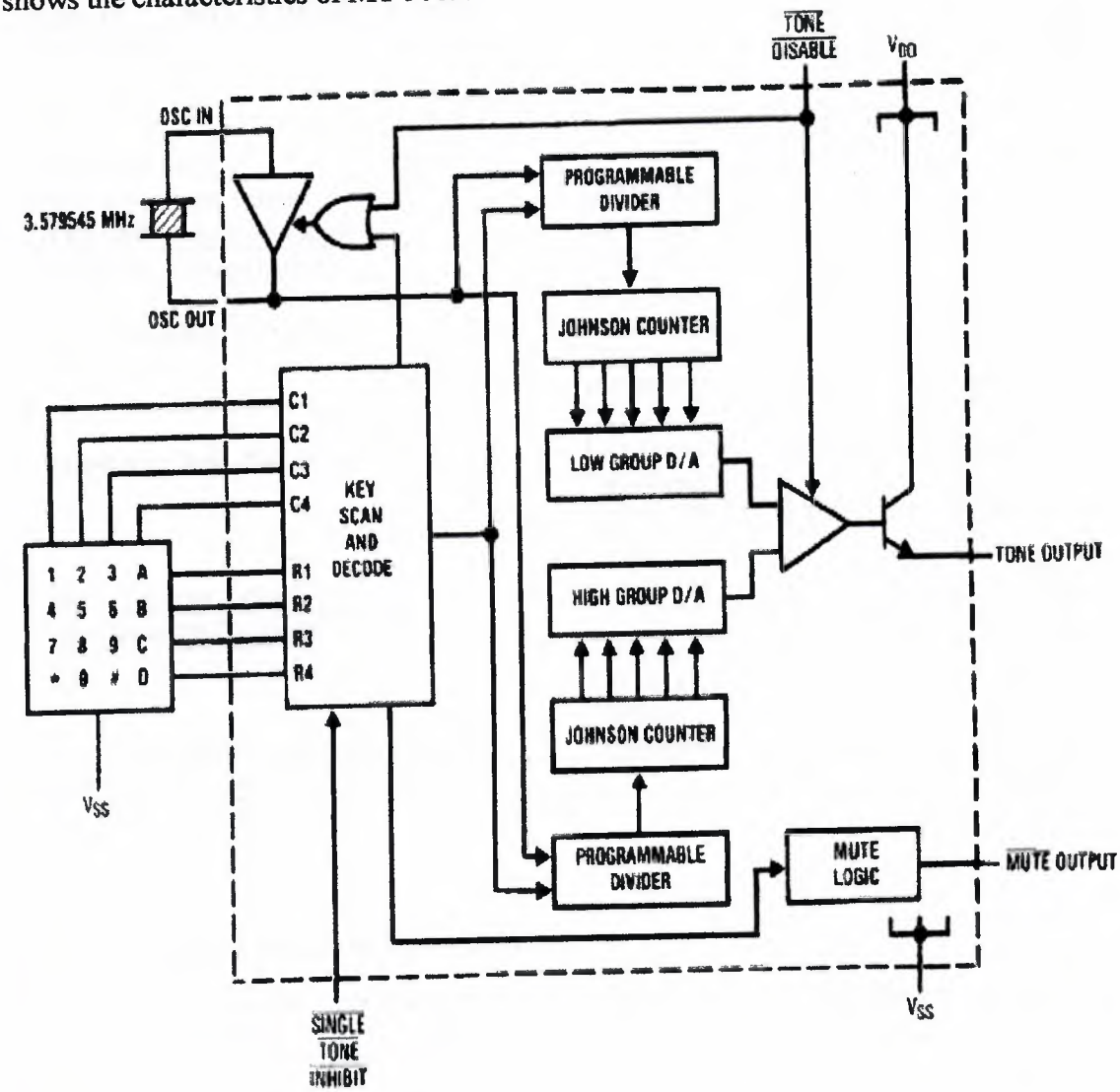


Figure 1.3.2 Block diagram of MT 5089 tone generator IC

Table 1.3.2 Characteristics of MT 5089

Parameter	Conditions	Min	Type	Max	Units
Minimum Supply Voltage for key sense and MUTE Logic Functions		2			V
Minimum Operating Voltage for generating tones		3.5			V
Operating Current Idle Generating Tones	Mute open RL=∞ VDD=3.5V		2 11	2.5 2.5	mA mA
Input Resistors COLUMN and ROW(Pull-up) SINGLE TONE INHIBIT(Pull-Down) TONE DISABLE(Pull-Up)		25 120	 50		kΩ kΩ
Input Low Level				0.2 VDD	V
Input High Level		0.8 VDD			V
MUTE OUT Sink Current (COLUMN and ROW Active)	VDD=3.5V VO=0.5V	0.4			mA mA
MUTE Out Leakage Current	VO=VDD		1		mA
Output Amplitude Low Group	RL=240Ω VDD=3.5V RL=240Ω VDD=10V	190 510	250 700	340 880	mVrms mVrms
Output Amplitude High Group	RL=240Ω VDD=3.5 V RL=240Ω VDD=10V	270 735	340 955	470 1265	mVrms mVrms
Mean Output DC Offset	VDD=3.5V VDD=10V		1.3 4.6		V V
High Group Pre-Emphasis		2.2	2.7	3.2	dB
Dual Tone/Total Harmonic Distortion Ratio	VDD=4V, RL=240Ω 1MHz Bandwidth		-23	-22	dB
Start-Up Time (to90% Amplitude)			3	5	ms

1.4 DTMF Decoding and Decoder Chip

Early DTMF decoders (receivers) utilized banks of band pass filters making them somewhat cumbersome and expensive to implement. This generally restricted their application to central offices (telephone exchanges).

The first generation receiver typically LC filters, active filters and/or phase loop techniques to receive and decode DTMF tones. Initial functions were commonly, phone number decoders and toll call restrictors. A DTMF receiver is also frequently used as a building block in a tone-to-pulse converter which allows Touch-Tone dialling access to mechanical step-by-step and crossbar exchanges.

The introduction of MOS/LSI digital techniques brought about the second generation of tone receiver development. These devices were used to digitally decode the two discrete tones that result from decomposition of the composite signal. Two analog band pass filters were used to perform the decomposition. Totally self-contained receivers implemented in thick film hybrid technology depicted the start of third generation devices. Typically, they also used analog active filters to band split the composite signal and MOS digital devices to decode the tones.

The development of silicon-implemented switched capacitor sampled filters marked the birth of the fourth and current generation of DTMF receiver technology. Initially single chip band pass filters were combined with currently available decoders enabling a two chip receiver design. A further advance in integration has merged both functions onto a single chip allowing DTMF receivers to be realized in minimal space at a low cost. The second and third generation technologies saw a tendency to shift complexity away from the analog circuitry towards the digital LSI circuitry in order to reduce the complexity of analog filters and their inherent problems.

Now that the filters themselves can be implemented in silicon, the distribution of complexity becomes more a function of performance and silicon real estate.

The CM 8870pi is a state of the art single chip DTMF receiver incorporating switched capacitor filter technology and an advanced digital counting/averaging algorithm for period measurement. It's the product of CALIFORNIA MICRO DEVICES Company. The block diagram (figure 1.4.1) illustrates the internal workings of this device.

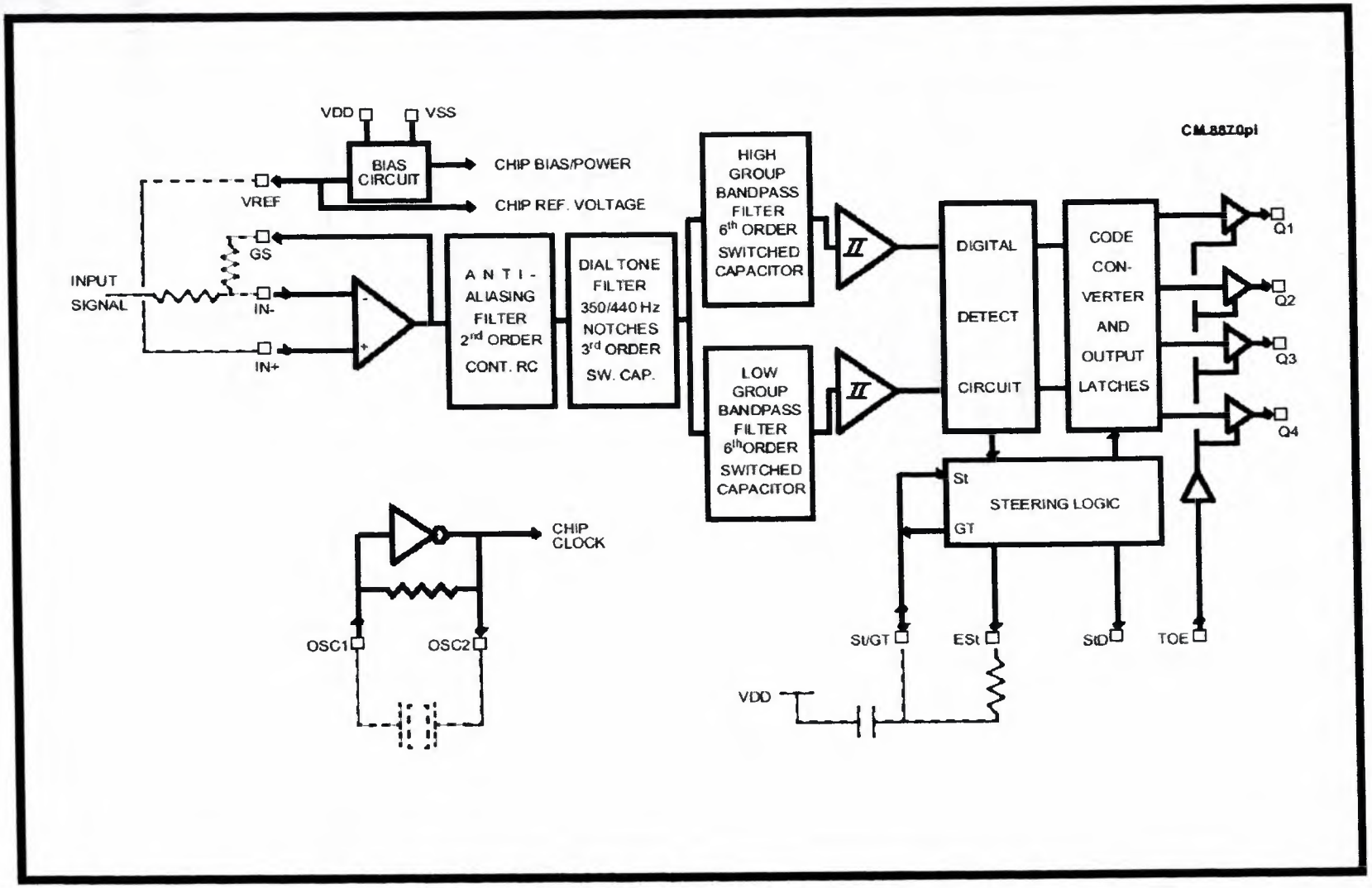


Figure 1.4.1 Block diagram of CM 8870pi DTMF decoder IC

To aid design flexibility, the DTMF input signal is first buffered by an input op-amp which allows adjustment of gain and choice of input configuration. The input stage is followed by a low pass continuous RC active filter which performs an antialiasing function.

Dial tone at 350 and 440Hz is then rejected by a third order switched capacitor notch filter. The signal, still in its composite form, is then split into its individual high and low frequency components by two sixth order switched capacitor and pass filters. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator. The two resulting rectangular waves are applied to digital circuitry where a counting algorithm measures and averages their periods. An accurate reference clock is derived from an inexpensive external 3.58MHz colour burst crystal. The timing diagram figure 1.4.2 illustrates the sequence of events which follow digital detection of a DTMF tone pair.

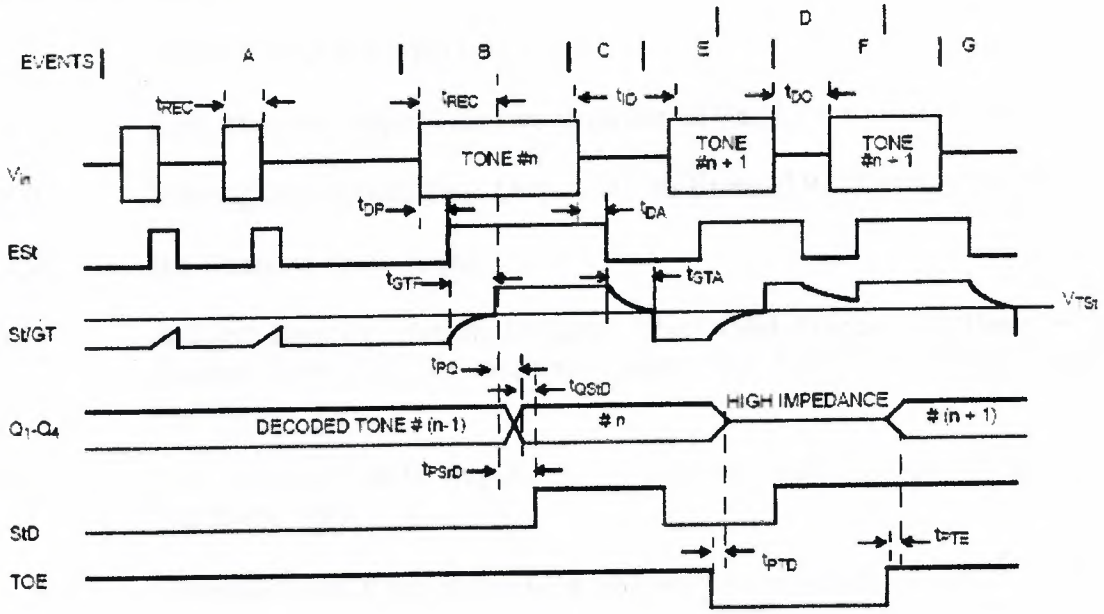


Figure 1.4.2 Sequence of events when call established

Explanation of Events

A) Tone Bursts Detected, Tone Duration Invalid Outputs Not Updated

B) Tone #n Detected. Tone Duration Valid. Tone Decoded and Latched in Outputs

C) End of Tone #n Detected. Tone Absent Duration Valid. Outputs Remain Latched Until Next Valid Tone

D) Outputs Switched to High Impedance State

E) Tone #n + 1 Detected. Tone Duration Valid Tone Decoded and Latched in Outputs (currently high impedance)

F) Acceptable Dropout of Tone #n + 1. Tone Absent Duration Invalid. Outputs Remain Latched.

G) End of Tone #n + 1 Detected. Tone Absent Duration Valid. Outputs Remain Latched Until Next Valid Tone.

Explanation of Symbols

V_{in}	DTMF Composite Input Signal
ESt	Early Steering Output Indicates Detection of Valid Tone Frequencies
ST/GT	Steering Input/Guard Time Output. Drives External RC Timing Circuit.
Q1-Q4	Bit Decoded Tone Output
StD	Delayed Steering Output. Indicates That Valid Frequencies Have Been Present/Absent For The Required Guard Time Thus Constituting a Valid Signal.
TOE	Tone Output Enable (input). A Low Level Shifts Q1-Q4 to Its High Impedance State.
t_{REC}	Maximum DTMF Signal Duration Not Detected as Valid.
t_{REC}	Minimum DTMF Signal Duration Required For Valid Recognition
t_{ID}	Maximum Time Between Valid DTMF Signals.
t_{DO}	Maximum Allowable Drop Out During Valid DTMF Signals
t_{DP}	Time to Detect The Presence of Valid DTMF Signals.
t_{DA}	Time to Detect the Absence of Valid DTMF Signals.

t_{GTP} Guard Time Tone Present.

t_{GTA} Guard Time Tone Absent.

Upon recognition of a valid frequency from each tone group the Early Steering (ESt) output is raised. The time required to detect the presence of two valid tones, t_{DP}, is a function of the decode algorithm, the tone frequency and the previous state of the decode logic. ESt indicates that two tones of proper frequency have been detected and initiates an RC timing circuit.

If both tones are present for the minimum guard time, t_{GTP}, which is determined by the external RC network, the DTMF signal is decoded and the resulting data (Table 1.4.1) is latched in the output register. The Delayed Steering (StD) output is raised and indicates that new data is available. The time required to receive a valid DTMF signal, t_{REC} , is equal to the sum of t_{DP} and t_{GTP}.

Table 1.4.1 DTMF signals and resulting outputs [Ref. 20]

f_{LOW}	f_{HIGH}	KEY	TOE	Q1	Q2	Q3	Q4
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	0	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1209	0	1	1	1	1	0
941	1336	*	1	1	1	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	0	0	1
770	1633	B	1	1	0	1	0
852	1633	C	1	1	0	1	1
941	1633	D	1	0	0	0	0
-	-	ANY	0	Z	Z	Z	Z

A simplified circuit diagram (figure 1.4.3) illustrates how the IC's steering circuit drives the external RC network to generate guard times.

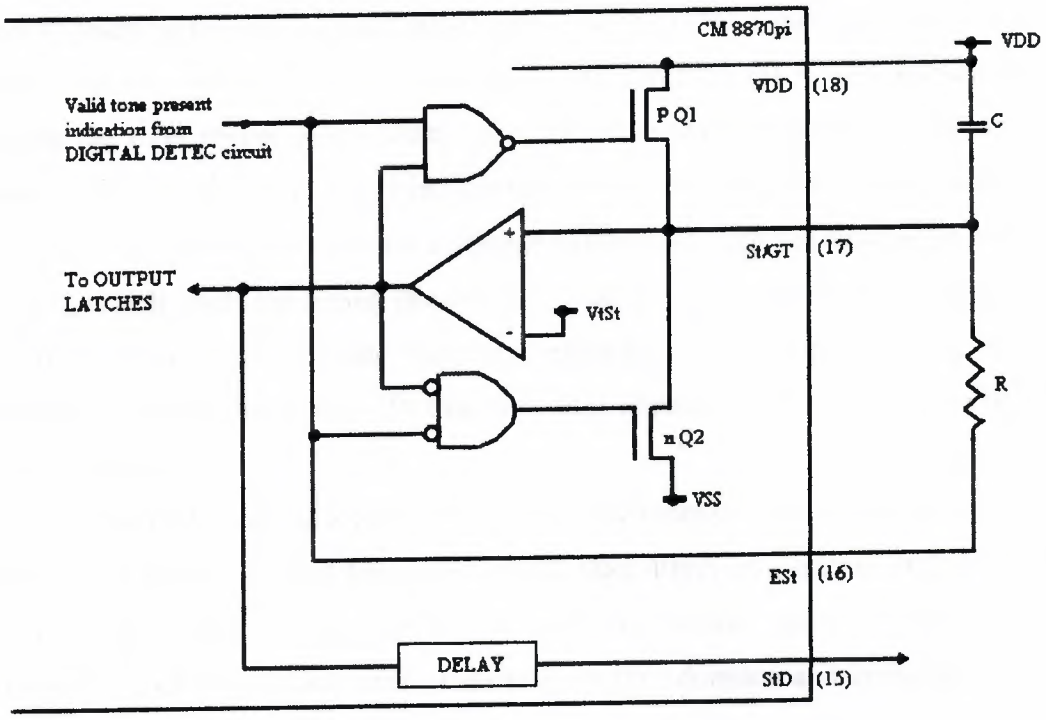


Figure 1.4.3 Guard time RC network driver diagram

Pin 17, St/GT (Steering/Guard Time), is a bidirectional signal pin which controls StD, the output latches, and resets the timing circuit.

When St/GT is in its input mode (St Function) both Q1 and Q2 are turned off and the voltage level at St/GT is compared to the steering threshold voltage V_{TSt}. A transition from below to above V_{TSt} will switch the comparator's output from low to high strobing new data into the output latches, and raising the StD output. As long as an input level above V_{TSt} is maintained StD will remain high indicating the presence of a valid DTMF signal. Initially, when no valid tone-pairs are present, capacitor C is fully charged applying a low voltage to St/GT. This causes a low at the comparator's output and since ESt is also low, Q2 turns on ensuring that C is completely charged. In this condition St/GT is in its output

mode (GT function). When a valid tone pair is received ESt is raised turning off Q2 which puts St/GT in its high impedance input mode and allows C to discharge through R.

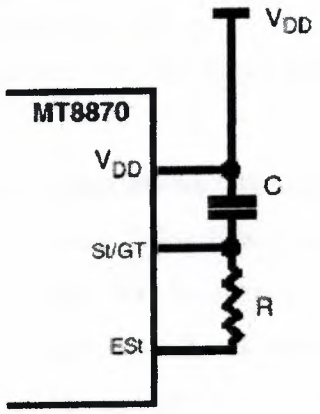
If this condition persists for the tone-present guard time, t_{GTP}, the voltage at St/GT rises above V_{TSt} raising StD which indicates reception of a valid DTMF signal.

If the tone pair drops out before the duration of t_{GTP}, ESt is lowered turning on Q2 which charges C resetting the tone-present guard time. Once a DTMF signal is recognized as valid both ESt and the comparator output are high. This turns on Q1 which discharges C and initializes the tone absent guard time, t_{GTA}. After the DTMF signal is removed, ESt is lowered, Q1 turns off placing St/GT in its input mode and C begins to charge through R.

If the same valid tone-pair does not reappear before t_{GTA} then the voltage at St/GT falls below V_{TSt} which resets the timing circuit via Q2 and prepares the device to receive another signal. If the same valid tone-pair reappears before t_{GTA}, ESt is raised turning on Q1 and discharging C which resets t_{GTA}. In this case StD remains high and the tone dropout is disregarded as noise.

To provide good reliability in a typical telephony environment, a DTMF receiver should be designed to recognize a valid tone-pair greater than 40mS in duration and, to accept as successive digits, tone pairs that are greater than 40mS apart. However in other environments, such as two-way radio, the optimum tone duration and intra-digit times may differ due to noise considerations.

By adding an extra resistor and steering diode (Fig.1.4.4.b, c) t_{GTP} and t_{GTA} can be set to

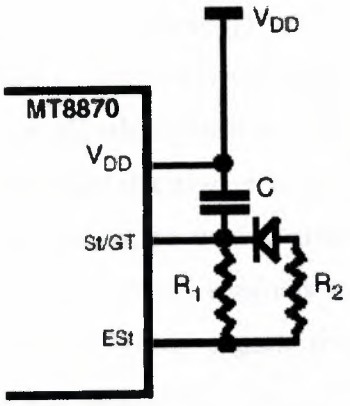


$[t_{GTP} = t_{GTA}]$

$t_{GTP} = (RC)\ \ln(V_{DD} / V_{TSt})$

$t_{GTA} = (RC)\ \ln(V_{DD} / [V_{DD} - V_{TSt}])$

Figure 1.4.4.a
Tone present and absent guard times equal



$[t_{GTP} < t_{GTA}]$

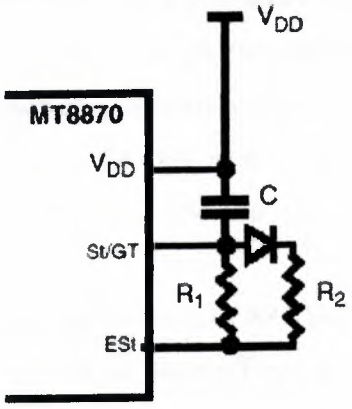
$t_{GTP} = (R_PC) \ln(V_{DD} / V_{TSt})$

$R_P = R_1R_2 (R_1+R_2)$

$t_{GTA} = (R_1C) \ln(V_{DD} / [V_{DD} - V_{TSt}])$

Figure 1.4.4.b

Tone present less than tone absent guard time



$[t_{GTP} > t_{GTA}]$

$t_{GTP} = (R_1C) \ln(V_{DD} / V_{TSt})$

$t_{GTA} = (R_PC) \ln(V_{DD}/[V_{DD} - V_{TSt}])$

$R_P = R_1R_2 / (R_1+R_2)$

Figure 1.4.4.c

Tone present greater than tone absent guard time

Guard time adjustment allows tailoring of noise immunity and talk-off performance to meet specific system needs. Talk-off is a measure of errors that occur when the receiver falsely detects a tone pair due to speech or background noise simulating a DTMF signal. Increasing t_{GTP} improves talk off performance since it reduces the probability that speech will maintain DTMF simulation long enough to be considered valid.

The trade-off here is decreased noise immunity because dropout (longer than t_{DA}) due to noise pulses will restart t_{GTP}. Therefore, for noisy environments, t_{GTP} should be decreased. The signal absent guard time, t_{GTA}, determines the minimum time allowed between successive DTMF signals.

A dropout shorter than t_{GTA} will be considered noise and will not register as successive valid tone detection. This guard against multiple reception of single character. Therefore, lengthening t_{GTA} will increase noise immunity and tolerance to the presence of an unwanted third tone at the expense of decreasing the maximum signalling rate. The intricacies of the digital detection algorithm have a significant impact on the overall receiver performance. It is here that the initial decision is made to accept the signal as valid or reject it as speech or noise. Trade-offs must be made between eliminating talk off errors and eliminating the effects of unwanted third tone signals and noise. These are mutually conflicting events.

On one hand valid DTMF signals present in noise must be recognized which requires relaxation of the detection criteria. On the there hand, relaxing the detection criteria increases the probability of receiving "hits" due to talk off errors. Many considerations must be taken into account in evaluating criteria for noise rejection.

In the telephony environment two sources of noise are predominant. These are, third tone interference, which generally comes from dial tone harmonics, and band-limited white noise. In the CM 8870pi a complex digital averaging algorithm provides excellent immunity to voice, third tone and noise signals which prevail in a typical voice bandwidth channel.

The algorithm used in the CM 8870pi combines the digital decoders with improvements resulting from years of practical use within the telephone environment. The algorithm has evolved through a combination of statistical calculations and empirical "tweaks" to result in the realization of an extremely reliable decoder.

CHAPTER 2: REAL LIFE APPLICATIONS

2.1 Basic DTMF Receiver Applications

The list below shows some applications which are performed by using DTMF receiver ICs

- Home remote control
- Remote data entry from any Touch-Tone keypad
- Credit card verification and inquiry
- Salesman order entry
- Catalogue store (stock/price returned via voice synthesis)
- Stock broker buy/sell/inquire -using stock exchange listing mnemonics
- Answering machine message retrieval
- Automatic switchboard extension forwarding

2.2 DTMF Controlled Applications

a) Home Applications

A household DTMF remote control system with an optional data port can boast a variety of conveniences (figure 2.2.1). Remote ON/OFF control may be given to electric appliances such as a slow cooker, exterior lighting and garage heater.

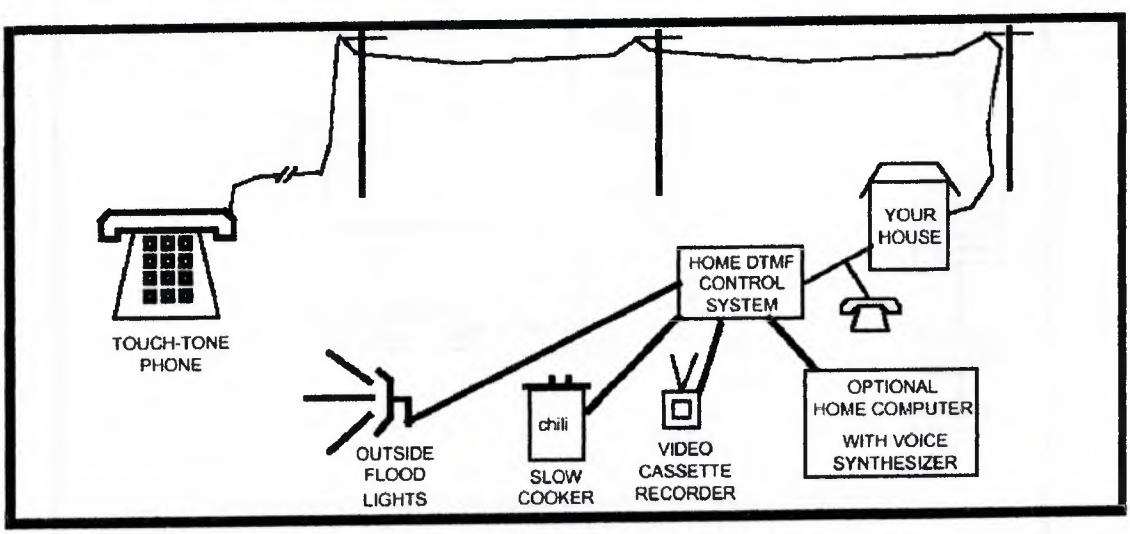


Figure 2.2.1 DTMF controlled home appliances [Ref. 3]

An electro-mechanical solenoid operated valve allows remote control of a garden sprinkler. Video buffs could interface to their VCR remote control inputs and record T.V. shows with a few keystrokes of their friend's telephone. This would enhance the function of timers which are currently available on most VCR's. Schedule changes or unexpected broadcasts could be captured from any remote location featuring a Touch-Tone™ phone.

Security systems could be controlled and a microphone could be switched in for remote audio monitoring.

Interfacing a home computer to the data port makes an excellent family message centre. At the remote end messages are entered from a telephone keypad. The computer responds with voice messages generated by a speech synthesizer. In the home, messages to be left are entered via the computer keyboard. Messages to be read may be displayed on the computer monitor or "played back" through the speech synthesizer.

A simple block diagram shows how this scheme may be implemented for a home DTMF control system (figure 2.2.2).

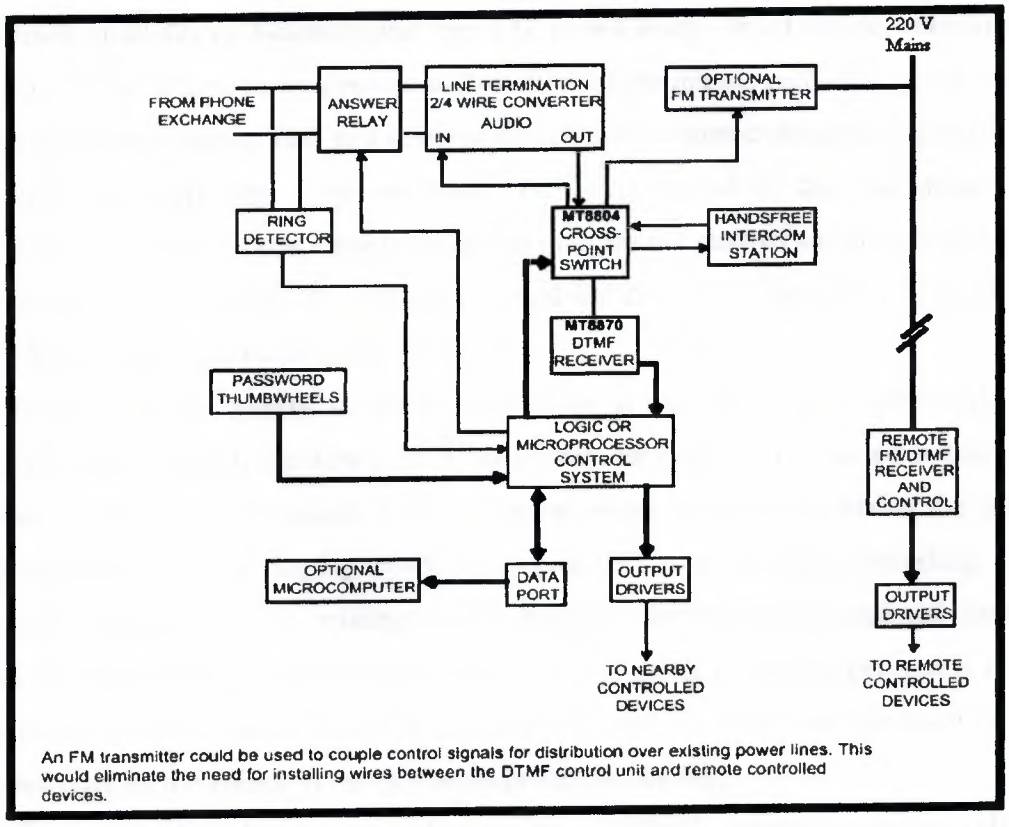


Figure 2.2.2 DTMF controlled home appliances with computerized configuration

A ringing voltage detector signals the microprocessor of an incoming call. The microprocessor, after the prescribed number of rings, closes the answer relay engaging the proper terminating impedance. A two-to-four wire converter splits bidirectional audio from the balanced telephone line into separate single ended transmit and receive paths. Receive audio is then switched to the DTMF receiver through the cross point switch. Upon receiving a valid DTMF signal, the microprocessor is alerted by the rising edge of StD. The microprocessor then checks for a valid password sequence and decodes subsequent commands.

A command can be entered to put the system into remote-control mode. In this case the cross point switch is configured to route DTMF signals into the FM-over-mains transmitter as well as the system tone receiver. Forwarding of control signals is accomplished by applying an FM carrier to the power line. This eliminates the need to string control wires haphazardly about the house.

The appropriate device is selected by its unique DTMF I.D. code. The microcomputer keeps track of all device locations and their I.D. codes since it must decide when to supply function outputs to the nearby devices and when to let the remote receivers handle the data. Subsequent data is transmitted to a selected device until a reset command is entered. Upon receiving any DTMF signal, answer back tones are returned by the microprocessor to acknowledge valid or invalid operations and to indicate the state of an interrogated device. For example, a low to high tone transition could indicate that a particular device is on, a high to low transition indicating the off state.

A command could be entered to put the system in an external mode which would allow communications through the data port. A host computer could be connected to this port to broaden the scope of the system. The resident microprocessor unit contains the software and hardware to control ringing verification, password and command decoding, answer back tone generation, audio routing, output function latches and an optional data port. Output drivers buffer the latches and switch relays or SCRs to control peripheral devices. An infinite variety of devices could be controlled by such a system, the spectrum of which is limited only by the ability to provide appropriate interfacing.

This system could also be the heart of a DTMF intercom system allowing intercommunication, "phone-patching", and remote control from varied household

locations. This type of system concept is, of course, anything but limited to home use. Many applications can provide conveniences to consumers, salespeople and executives. For example, a merchant could verify credit card accounts quickly utilizing only a telephone keypad for data entry (figure 2.2.3). Each credit card company could reserve one or more telephone lines to provide this function, reducing the human effort required. The receiving end system would be required to answer the call, provide a short answer back tone or message, receive and decode the credit card account number, verify it, verify the owner's name and give a go/no-go authorization. This return data could easily be provided with the aid of a voice synthesizer. An auto-dialler containing appropriate phone numbers could be installed at the merchant end as an added time saver.

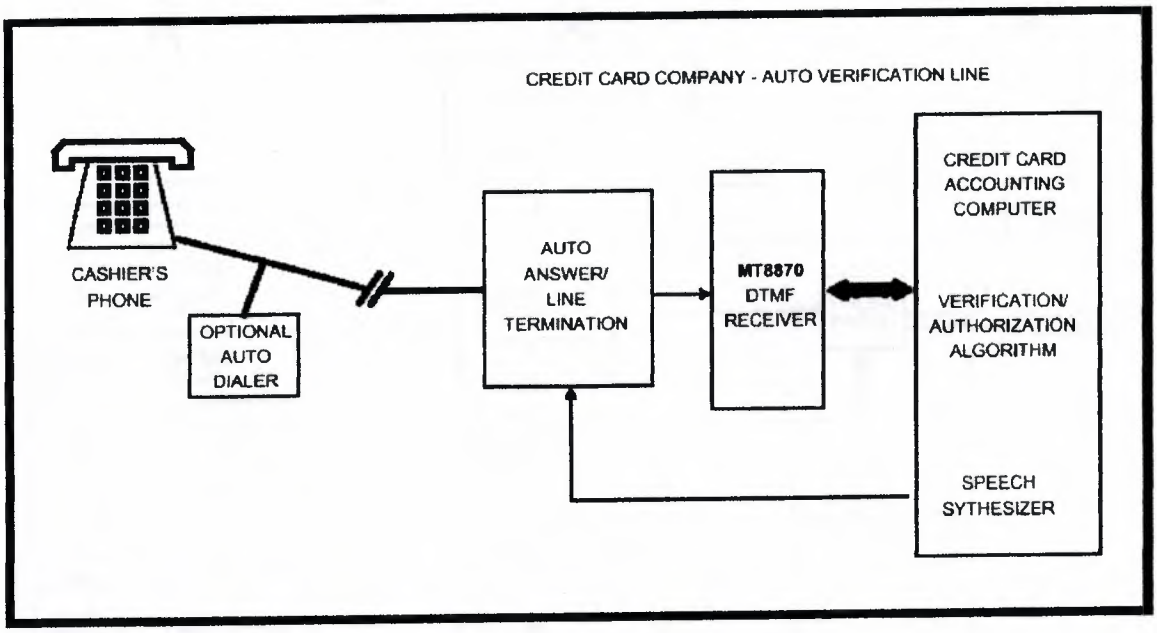


Figure 2.2.3 Credit card verification by using DTMF

b) DTMF in Mobile Radio Applications

DTMF signaling plays an important role in distributed communications systems, such as multi-user mobile radio (figure 2.2.4). It is a "natural" in the two-way radio environment since it slips neatly into the center of the voice spectrum, has excellent noise immunity and highly integrated methods of implementation are currently available. It is also directly compatible with telephone signaling, simplifying automatic phone patch systems.

Several emergency medical service networks currently use DTMF signals to control radio repeaters. Functions are, typically, mobile identification, selection of appropriate repeater links, selection of repeater frequencies, reading of repeater status, and for completing automatic phone patch links. If available in a system of this type, audio from a long distance communications link (microwave, satellite, etc.) could be switched, via commands from the user's DTMF keypad, into the local repeater.

This would offer the mobile user a variety of paths for communication without the assistance of a human operator.

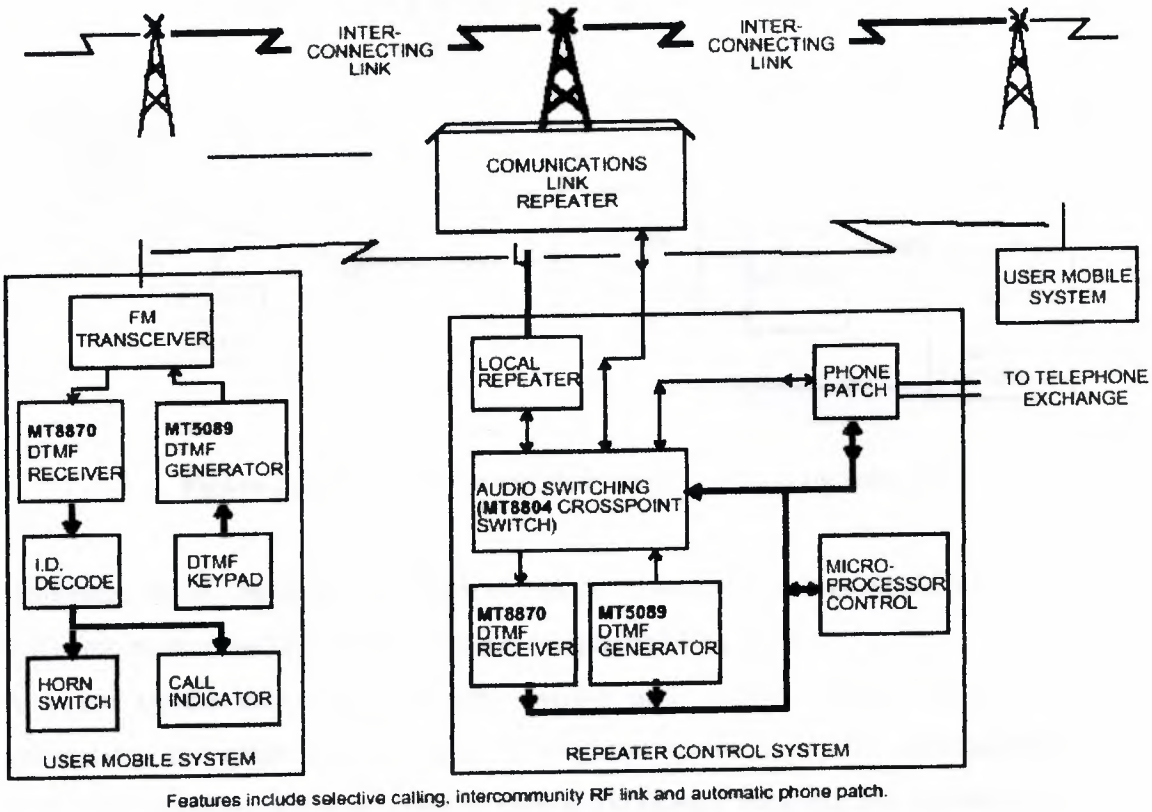


Figure 2.2.4 DTMF controlled FM communication

With a similar arrangement, a travelling salesman could access price, delivery and customer status, enter or delete merchandise orders and retrieve messages all from the comfort of the customer's office (figure 2.2.5.a). A department store could provide shop-by-phone service to its customers using telephone keypad data entry (figure 2.2.5.b).

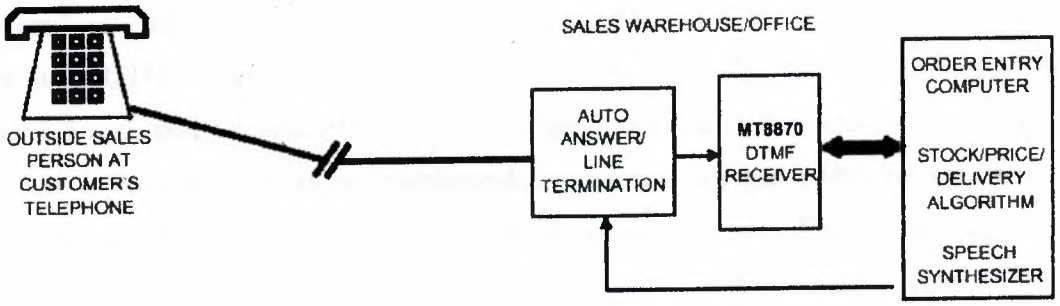


Figure 2.2.5.a DTMF controlled access to sales office

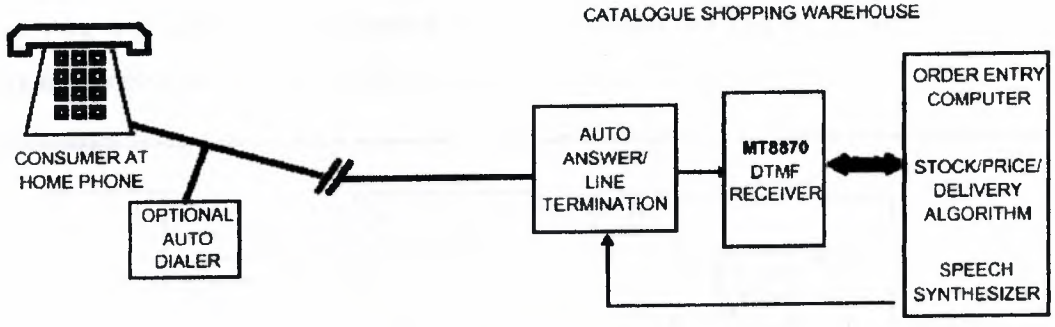


Figure 2.2.5.b DTMF controlled access to shopping warehouse

Brokerage firms, utilizing the stock exchange mnemonic listings could provide trading price information and buy/sell service via telephone keypad entry.

A voice synthesizer could provide opening and current trading price, volume of transactions and other pertinent data. A telephone answering system manufacturer could apply this technique, allowing users to access and change outgoing and incoming messages from a Touch-Tone phone. A PBX manufacturer could offer a feature that relieves the switchboard attendant from unnecessary interaction.

A call could be answered automatically and a recording may reply Thank you for calling XYZ. Please dial the extension you wish to contact or zero for the switchboard". If the caller knows the called party's extension in advance it is not necessary to wait for the switchboard attendant to forward the call. The attendant could be notified to intervene if

there is no action by the caller say, ten seconds after the recording ends. This provides a similar function to a "Direct Inward Dialling"(DID) trunk but without the additional overhead incurred with renting a block of phone numbers as in the DID case.

Now that a DTMF receiver is so easy and inexpensive to implement there are many simple dedicated uses that become attractive. A useful home and office application for DTMF receivers is in a self-contained telephone-line-powered toll call restrictor similar to the block diagram in figure 2.3.5.a. This could be installed in an individual telephone or at the incoming main termination depending on which phone or phones are to be restricted. While disallowing visitors from making unauthorized long distance calls, the owner may still desire access to toll dialling.

This could be provided by adding a logic circuit that disables the toll restrictor upon receiving a predetermined sequence of DTMF characters (figure 2.3.6). In this case, the user must enter his password before dialling a long distance number.

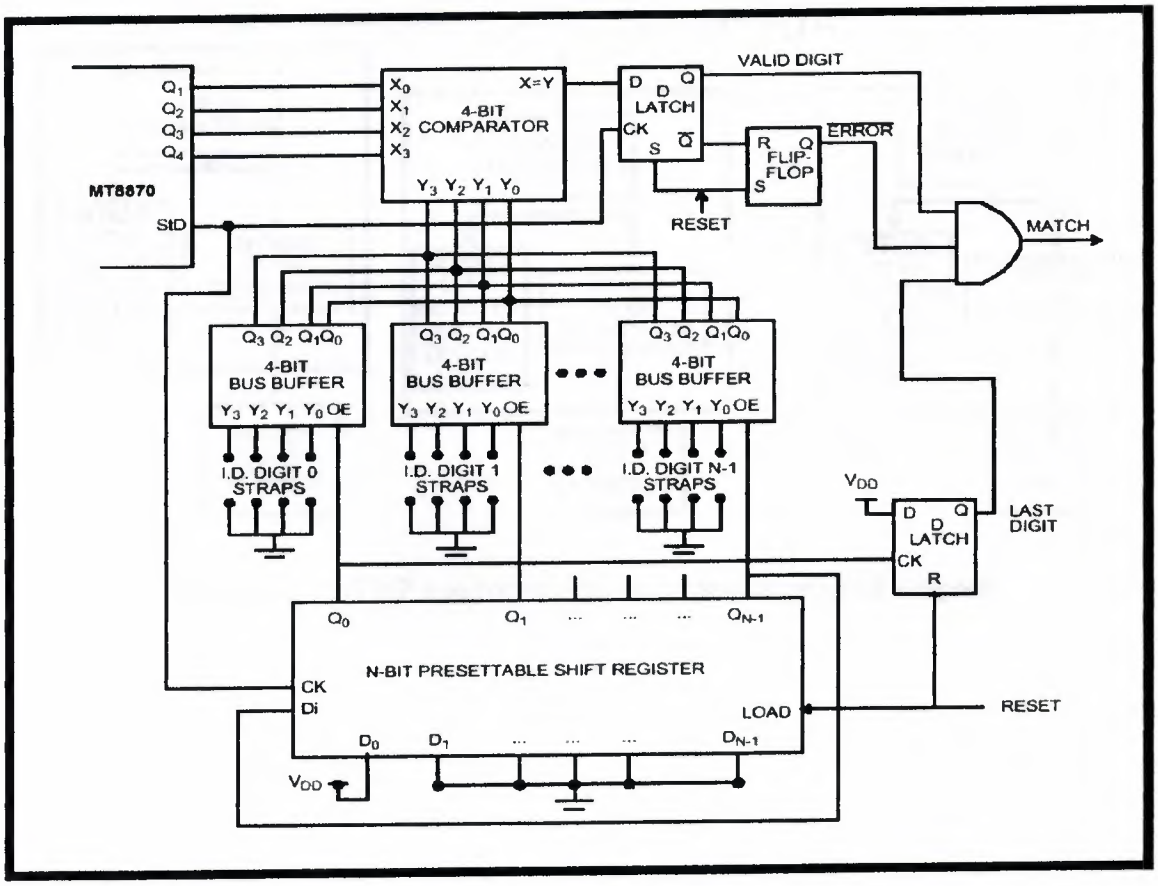


Figure 2.2.6 Security circuit for DTMF controlled applications

c) DTMF Controlled Data Communication

There is a vast array of potential applications for DTMF signalling using the existing telephone network. Considering that there are millions of ready-made data sets installed in convenient locations (i.e. the Touch Tone telephone) remote control and data entry may be performed by users without requiring them to carry around bulky data modems.

Figure 2.2.7 shows DTMF controlled data communication block diagram. In this block diagram MT 8870 is used which has same properties of CM 8870pi. MT 8870 is the product of ZARLINK Semiconductor.

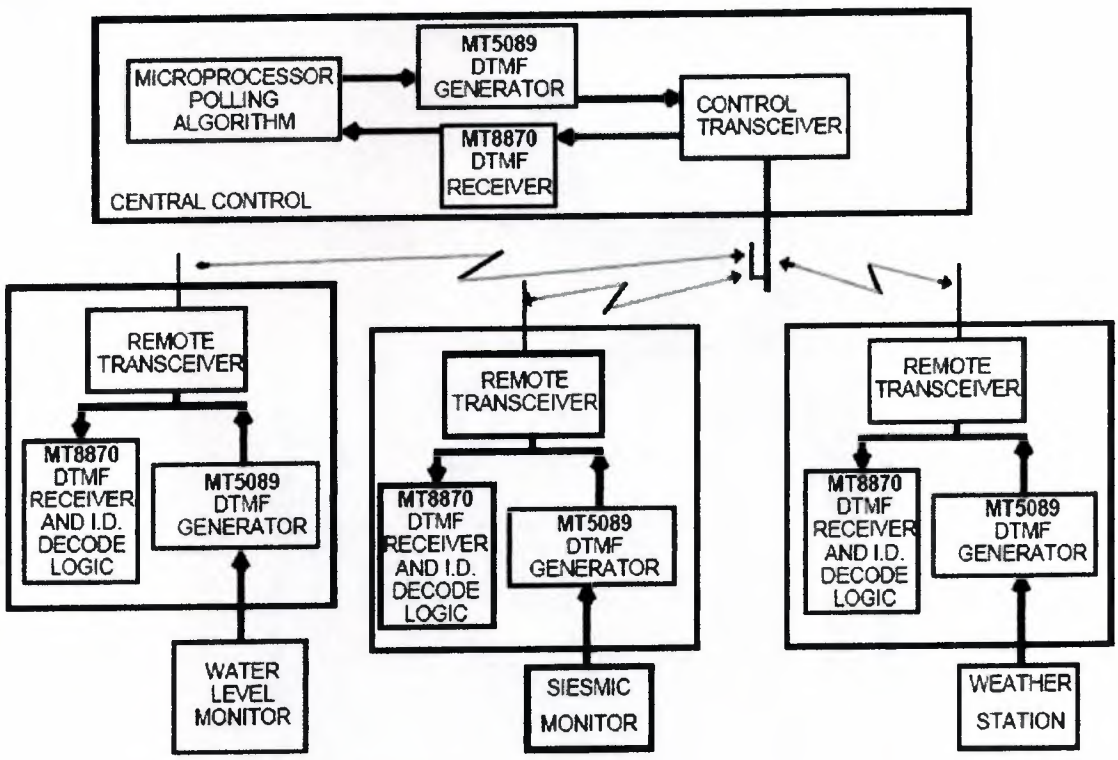


Figure 2.2.7 DTMF controlled data communication block diagram

CHAPTER 3: DTMF RECEIVER PROJECT

3.1 Project Circuit

This project is about DTMF receivers. Here the receiver circuit enables users to switching 'on' and 'off' of appliances through telephone lines. It can be used to switch appliances from any distance, overcoming the limited range of infrared and radio remote controls The circuit uses IC CM 8870 (DTMF-to-BCD converter), DM 74LS154 (4-to-16-line demultiplexer), and five FT 4013 (D flip-flop) ICs and three CD 4049 NOT gate ICs. The pictures of project are given on figure 3.1.a and b, scheme is given on figure 3.2

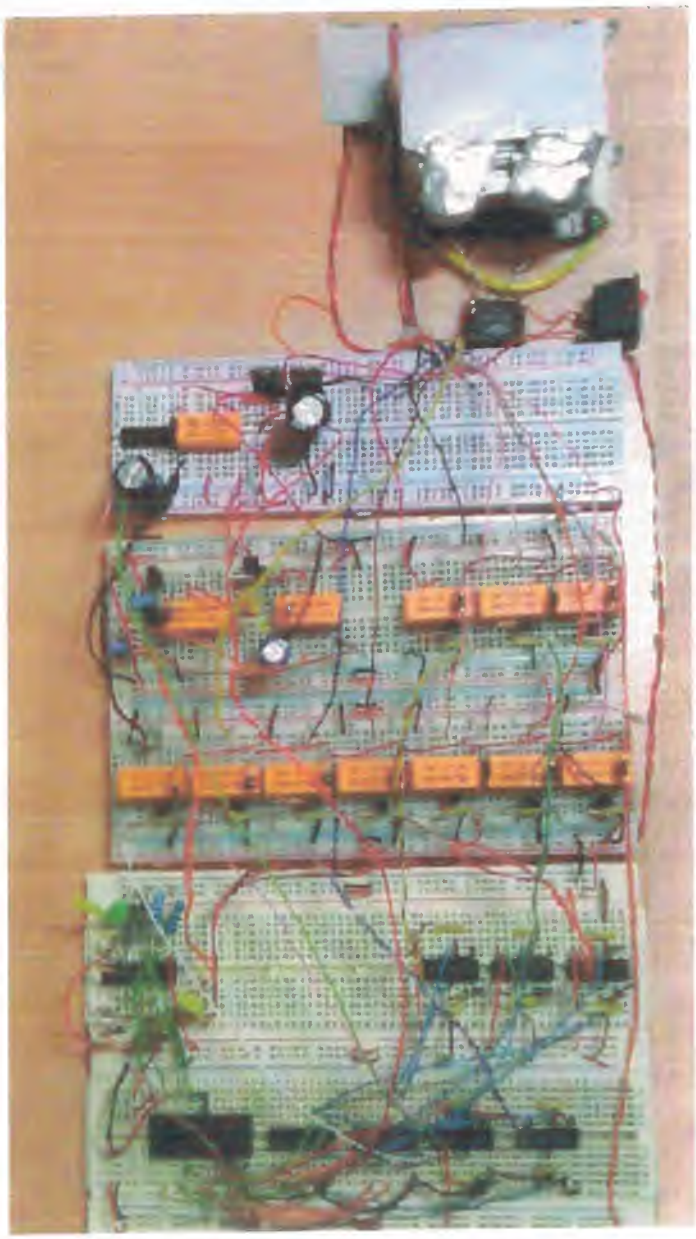


Figure 3.1.a DTMF receiver circuit

Figure 3.1.b Controlled appliances

The pictures shown on figure 3.1.b simulates DTMF controlled home appliances which are outdoor lamps, central heating unit, security system, oven, microwave, dishwasher, heater, air-conditioner and washing machine.

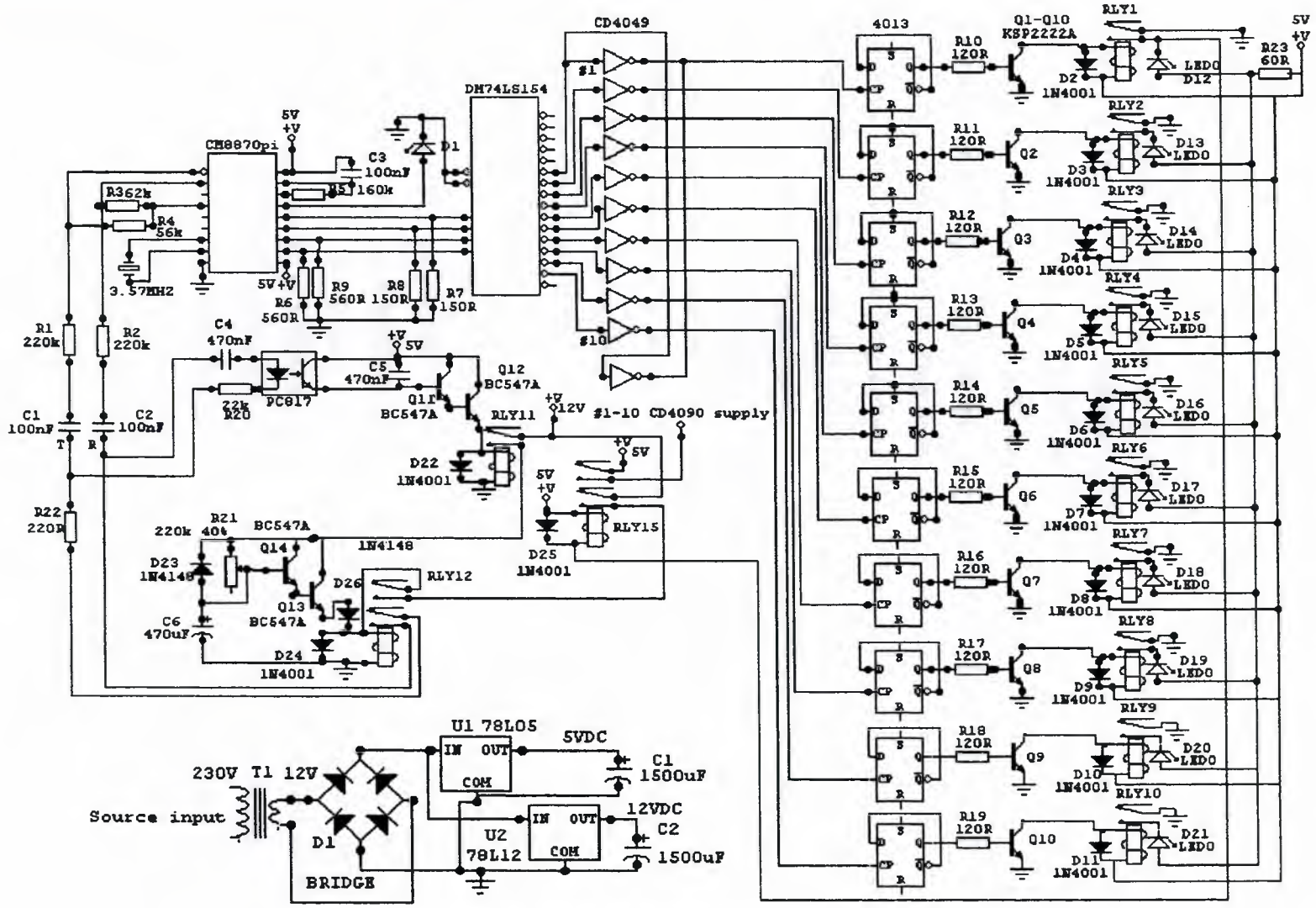


Figure 3.1.2 DTMF controlled home appliances circuit

3.2 Working Principle of Circuit

The circuit has 4 parts which are Power supply, Ring detect & auto answer, Decoding and Controlling part.

The Power supply part; this part simply composed of one 230 to 12VAC Transformer which has bridge rectifier connected to its output and two regulator ICs LM7812 and LM7805; LM7812 is 12VDC regulator which supplies timer's voltage and LM7805 is 5VDC regulator which supplies all IC's and relay's voltage. To prevent voltage oscillation at the output of regulators 1500uF 25V capacitors are placed.

Ring deduct & auto answer part; as the name implies Ring deduct & auto answer part has two main parts, one of them is Ring deduct and the other one is turn on timer based auto answer part. Lets look how Ring deduction done. Once the call established to the circuit (after hearing ring-back tone), the telephone line signal feeds PC 817 opto-coupler via C4 and R20, when the opto-coupler has driven the 5V supply voltage on its collector flows to its emitter and feeds RLY11 with an Darlington connected transistors (Q11 & Q12). Here the tricky part is C5, it is used to prevent sharp voltage degreasing so that the relay will not turn off between two rings, as we know the ring signal is not continuous. When RLY11 has driven its N/O contacts close and energize RLY12. RLY12's N/O contacts drives timer with 12VDC and timer starts.

The working principle of timer is simply RC circuit and a Darlington connected transistors. The auto answer time can be adjusted with R21 (variable resistor). After timer circuit answered phone RLY12 connects 220ohm resistor (R22) in parallel to telephone line. That resistor removes the ring signal from telephone line. The other N/O contact of RLY12 feeds itself over RLY15's N/O contacts. At the beginning RLY15 is off mode and RLY12 can't get any voltage over RLY15. How to feed RLY15 so that, RLY12 can feed itself over it, otherwise in a short time RLY12 turns off and removes R22 from network and circuit will close the line(off hook mode), to solve this problem and also to prevent unwanted interference to the circuit separate NOT gate placed that is always active. The 10^{th} output of DM74LS154 which is active when key zero is preset from telephone's keypad connected to NOT gate and the output of this gate drives RLY11 and it drives RLY15

When this relay activated, RLY12 can feed itself over RLY15 and RLY12 also energize other NOT gates so the user can interference to the appliances.

If key zero doesn't press within 4 second (this time is related with RLY11 and C6) the circuit will close line and waits for new call.

The decoding process is made by CM8870pi IC this IC is used with some passive components to decode DTMF signals. The output of CM8870pi is 4 bit binary which is given on chapter 1 at table 1.4.1.

DM74LS154 is 4 to 16 bit demultiplexer; it converts 4 bit BCD to 16 separate output, to able to use all of those outputs we have to use Hexadecimal telephone device that has 16 key on it 0-9,#,* and A-D. The normal daily used telephones has only keys 0-9, # and * so if we have internal telephone centre # and * have another function. # is call waiting and * is flash because of this in this project, these conditions taken into account and only 0-9 keys are used.

Zero is used to toggle between appliances and normal phone conversation 1-9 is used to control appliances because of that reasons only 10 of DM74LS154's outputs are necessary. To make those outputs suitable with use D-type flip flops, NOT gates have to placed at the output of DM74LS154, two of CD4049 that has 6 separate NOT gate inside of it is enough to solve this problem. The outputs of these IC's are connected to CD4013's input. Each IC has 2 D-type fillip flop inside of it so 5 of that ICs are enough to control appliances.

These flip lops changes their states when its input is HI so if the input always HI it stays at same position. If we want to change its output we have to drive it with a pulse (0,5V). This force the user to press any other key before pressing key zero to activate it because key zero is used to toggle between normal conversation and appliance controlling mode. Key zero is also used to deactivate the circuit and exit.

Assume user has call the circuit and it answered after adjusted time and user pressed zero key on the telephone keypad and made some changes (turn on or off some appliances) then to exit from this mode he or she has to press zero key again to remove supply voltage of CD4049 #1-10 and turn off them also to close line.

The last decoded key was zero and only 10^{th} output of DM74LS154 was low so when user calls again and presses zero to enable circuit, the output of both CM 8870pi and DM74LS154 remains same. It means that the input of D-type flip flop also remains same so it will not update output, because of this reason the user must press any other key except from zero then press zero so the output of all three IC's will update and circuit will be

enable to control appliances. If zero is not pressed before closing the telephone line the circuit will not close the line and stays in safe mode until someone resets it.

3.3 Problems Occurred While Design Circuit

While wiring this project I faced with lots of problems one and the most important of them was decoding problem. Second problem was how to design a circuit that able to answer telephone line and answering wait time must be adjustable.

The first scheme shown on figure 3.3.1 was wired first and decoding of tones couldn't accomplish.

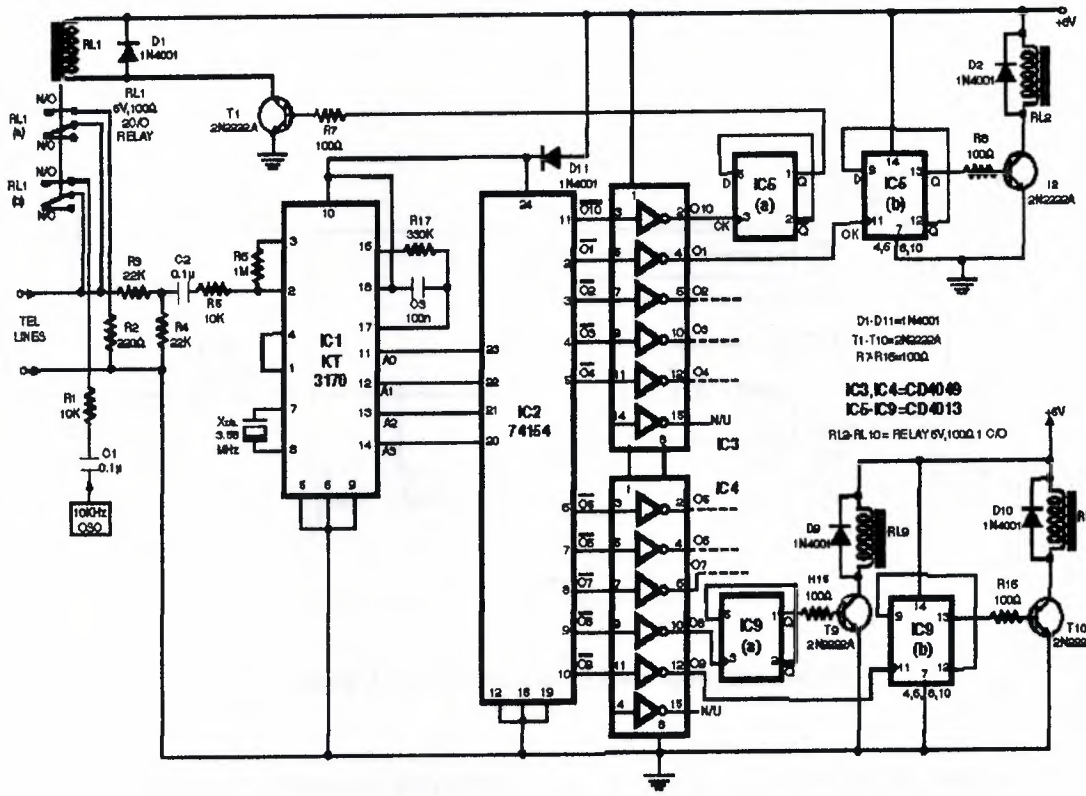


Figure 3.3.1 The first wired unsuccessful circuit [Ref.8]

The first circuit diagram was use only one input of CM 8870pi's internal op-amp and it has also gain select resistor connected between GS and -IN. When the circuit has been wired and tested, tones weren't decoded .Each time when supply voltage was applied; the outputs of CM 8870pi went to Hi and remain same. The CM 8870pi couldn't decode the input

DTMF signals and update the outputs. The IC has been changed first to check if it is working or not and seen that it is ok so something was wrong in that schematic because nothing was changed when IC replaced. Some more research has been make abut that IC and got more input combinations also understood that the tone present and tone absent time has very important role in this circuit, most of the circuits found related with this project uses 100nf capacitor and resistor around 200kohm for tone absent and tone present time adjustment. 300kohm variable resistor has placed to find out when circuit accept tones and decode theme but it didn't work again. Than circuit diagram has been changed with another one witch is use both inputs of op-amp. Figure 3.3.2 show second wired circuit to decode DTMF tones.

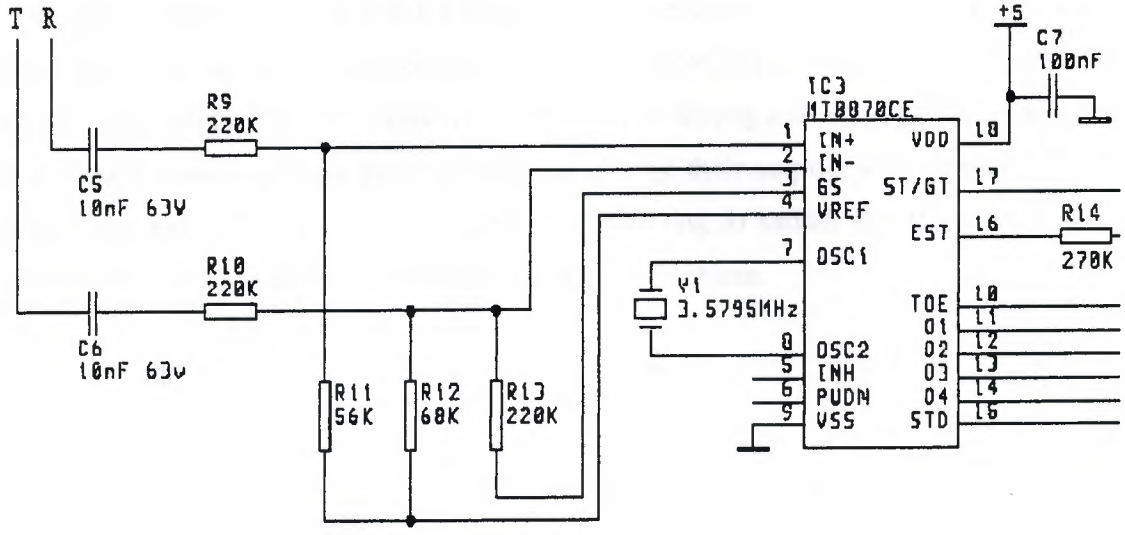


Figure 3.3.2 Two input DTMF decoder circuit

At the beginning this schematic also didn't work properly, only first input could be decoded and the others couldn't be decoded. R14 and C7 have changed to adjust tone present and tone absent times but this attempt didn't have success. Line input resistors were change with smaller value resistors but nothing changed until the value of gain select resistor increased this time first tone could be decode second and the other couldn't. By removing the gain select resistor IC has start to decode input DTMF signals.

What was the reason that gain select resistor has to be removed so the IC could decode all

of the codes successfully; The reason was HI input signal it was high enough also has noise with it that only first DTMF signal could decode and there IC was locked and accepts other signals as the first signal and newer update the output. High values of gain select resistor tried like 2 Mohm but experiments showed that no need to gain select resistor because IC was working very successfully and gives reliable outputs.

After solving decoding problem the auto answer problem and timer problem occurred, because figure 3.3.2 design with using microprocessor that can solve all these problems with an program but in this project no need to use microprocessor. These problems can be solved with using logic. An opto-coupler is used as a ring detector with some passive components and for the auto answer wait timing a turn on type timer placed these two small and simple circuits enough to solve problems for ring deduct and timing.

The last problem occurred was disabling circuit so that other people can't interference to the circuit. To solve this problem something has to be happened that controlling part of circuit disabled. D-Type flip flops are the heart of switching action if I kill them this means that if their supply voltages gone nothing can change their outputs without supply voltage. Something has to be used like independent controlling to switch flip flops on & off. As chapter 3.2 implies a separate NOT gate solved this problem.

CONCLUSION

For the control engineering reliability is very important and also for remote controlling range limits has important role. DTMF controlling circuit overcomes all of these problems while designing this circuit those problems held to accounted and developed.

The circuit has to able to answer telephone line, waits for key zero, if not pressed by remote user to able to control appliances, it has to close the line. Those specifications need ring deduction, timer and separate controlling for key zero. Combination of those parts makes the circuit to control nine different appliances with decoding DTMF tones.

For the future work this type circuits can be improved and equip with microprocessor so that more functions and more secure controlling systems can establish.

REFERENCES

[1] Elektronik Devre Uygulamalari II,Eyüp Ersan Sülün,Muzaffer Aslan, Abdülkadir Çakir (2002)

[2] Dijital Elektronik,Yilmaz Çamur (1992)

[3] http://www.bobblick.com/techref/projects/tonedec/tonedec.html

[4] http://www.tech-faq.com/dtmf-tone-frequencies.shtml

[5] http://www.ece.utexas.edu/~mason/codesign/dtmf.html

[6] http://en.wikipedia.org/wiki/Dual-tone_multi-frequency

[7] http://www.electronic-circuits-

[8] http://www.diagrams.com/remotecontrolsimages/remotecontrolsckt5.shtml

[9] http://www.boondog.com/tutorials/dtmf/dtmf.htm

[10] http://www.dattalo.com/technical/theory/dtmf.html

[11] http://www.thisisarecording.com/sounds14.shtml

[12] http://www.catauto.com/pdf/cp_4.pdf

[13] http://www.dialabc.com/sound/detect/faq.html

[14] http://www.ece.utexas.edu/~mason/codesign/DTMF_Performance.html

[15] http://www.pspilot.de/pppdtmf/pppdtmf.html

[16] http://www.hw-server.com/docs/dtmfb.html

[17] http://en.wikipedia.org/wiki/Dual-tone_multi-frequency

[18] http://www.hackcanada.com/blackcrawl/elctrnic/dtmf-faq.txt

[19] http://margo.student.utwente.nl/el/phone/dtmf.htm#DTMF_003

[20] http://www.datasheetcatalog.com

[21] http://www.datasheetarchive.com

[22] http://www.datasheets.org.uk

[23] http://www.fairchildsemi.com

APPENDIX (Datasheets)

Datasheet of CM 8870pi

CMOS Integrated DTMF Receiver

Features

- Full DTMF receiver
- Less than 35mW power consumption
- Industrial temperature range
- Uses quartz crystal or ceramic resonators
- Adjustable acquisition and release times
- 18-pin DIP, 18-pin DIP EIAJ, 18-pin SOIC, 20-pin PLCC
- **CM8870C**
  - — Power down mode
  - — Inhibit mode
  - — Buffered OSC3 output (PLCC package only)
- CM8870C is fully compatible with CM8870 for 18-pin devices by grounding pins 5 and 6

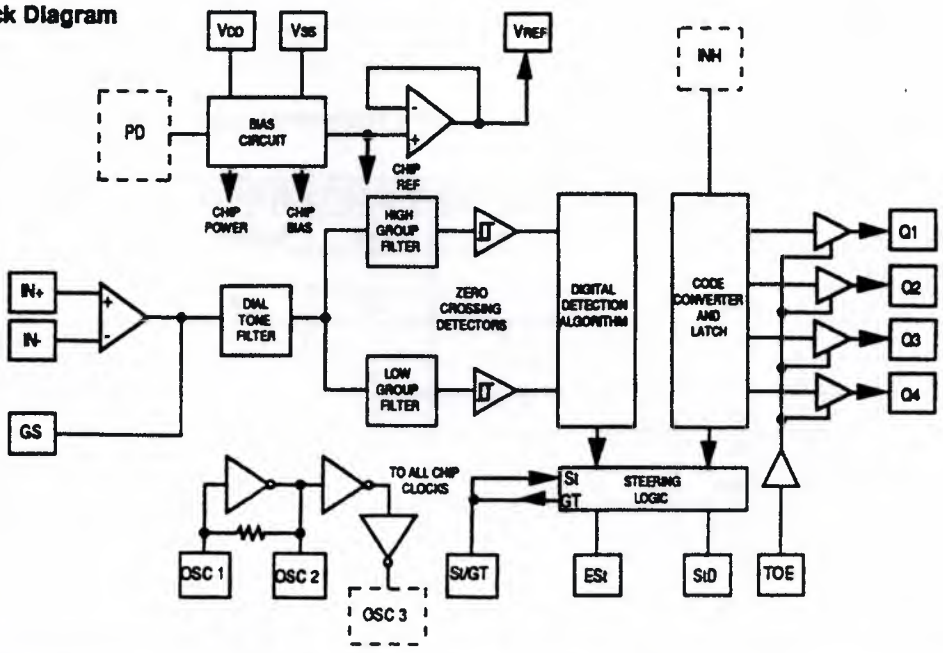
Applications

- PABX
- Central office
- Mobile radio
- Remote control
- Remote data entry
- Call limiting
- Telephone answering systems
- Paging systems

Product Description

The CAMD CM8870/70C provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC package. The CM8870/70C is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW, max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The CM8870/70C decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. This DTMF receiver minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal or ceramic resonator as an external component.

Block Diagram



C1550900

Absolute Maximum Ratings: (Note 1)

ABSOLUTE MAXIMUM RATINGS		
Parameter	**Symbol**	**Value**
Power Supply Voltage (V_{DD}-V_{SS})	V_{DD}	6.0V Max
Voltage on any Pin	Vdc	V_{SS}-0.3V to V_{DD}+0.3V
Current on any Pin	I_{DD}	10mA Max
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	T_S	-65°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5.0V ± 5%, T_A = -40°C to +85°C unless otherwise noted.

DC CHARACTERISTICS							
Parameter		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Operating Supply Voltage		V_{DD}	4.75		5.25	V	
Operating Supply Current		I_{DD}		3.0	7.0	mA	
Standby Supply Current		I_{DDQ}			25	µA	PD=V_{DD}
Power Consumption		P_O		15	35	mW	f=3.579 MHz; V_{DD}=5.0V
Low Level Input Voltage		V_{IL}			1.5	V	V_{DD}=5.0V
High Level Input Voltage		V_{IH}	3.5			V	V_{DD}=5.0V
Input Leakage Current		I_{IH}/I_{IL}		0.1		µA	V_{IN} = V_{SS} = V_{DD} (Note 1)
Pull Up (Source) Current on TOE		I_{so}		6.5	20	µA	TOE=0V, V_{DD}=5.0V
Input Impedance, (IN+, IN-)		R_{IN}	8	10		MΩ	@ 1KHz
Steering Threshold Voltage		V_{Tst}	2.2		2.5	V	V_{DD} = 5.0V
Low Level Output Voltage		V_{OL}			0.03	V	V_{DD} = 5.0V, No Load
High Level Output Voltage		V_{OH}	4.97			V	V_{DD} = 5.0V, No Load
Output Low (Sink) Current		I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4V
Output High (Source) Current		I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
Output Voltage	V_{REF}	V_{REF}	2.4		2.7	V	V_{DD} = 5.0V, No Load
Output Resistance	V_{REF}	R_{OR}		10		KΩ	

Operating Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5.0V ± 5%, T_A = -40°C to +85°C unless otherwise noted.

Gain Setting Amplifier

OPERATING CHARACTERISTICS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input Leakage Current	I_{IN}			±100	nA	V_{SS} < V_{IN} < V_{DD}
Input Resistance	R_{IN}	10			MΩ	
Input Offset Voltage	V_{OS}			±25	mV	
Power Supply Rejection	PSRR	50			dB	1KHz (Note 12)
Common Mode Rejection	CMRR	40			dB	-3.0V < VI_N < 3.0V
DC Open Loop Voltage Gain	A_{VOL}	32			dB	
Open Loop Unity Gain Bandwidth	fc	0.3			MHz	
Output Voltage Swing	V_O	4.0			V_{P-P}	R_L ≥ 100KW to V_{SS}
Maximum Capacitive Load (GS)	C_L			100	pF	
Maximum Resistive Load (GS)	R_L			50	KΩ	
Common Mode Range (No Load)	Vcm	2.5			V_{P-P}	No Load

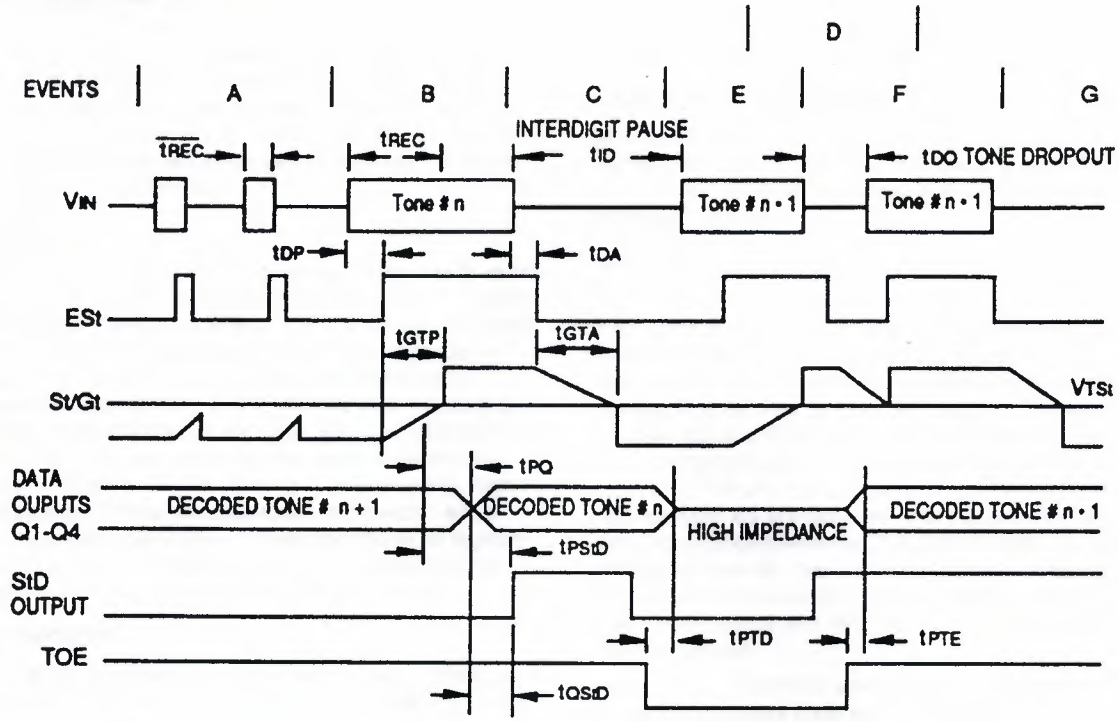
AC Characteristics: All voltages referenced to V_{SS}, V_{DD}=5.0V ±5%, T_A=-40°C to +85°C, f_{CLK}=3.579545 MHz using test circuit (Fig. 1) unless otherwise noted.

AC CHARACTERISTICS							
Parameter		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Valid Input Signal Levels (each tone of composite signal)			-29		+1	dBm	1,2,3,4,5,8
			27.5		869	mV_{RMS}	
Positive Twist Accept					10	dB	2,3,4,8
Negative Twist Accept					10	dB	
Freq. Deviation Accept Limit					1.5%±2Hz	Nom.	2,3,5,8,10
Freq. Deviation Reject Limit			±3.5%			Nom.	2,3,5
Third Tone Tolerance				-16		dB	2,3,4,5,8,9,13,14
Noise Tolerance				-12		dB	2,3,4,5,6,8,9
Dial Tone Tolerance				+22		dB	2,3,4,5,7,8,9
Tone Present Detection Time		t_{DP}	5	8	14	mS	Refer to Timing Diagram
Tone Absent Detection Time		t_{DA}	0.5	3	8.5	mS	
Min Tone Duration Accept		t_{REC}			40	mS	(User Adjustable) Times shown are obtained with circuit in Fig. 1)
Max Tone Duration Reject		t_{REC}	20			mS	
Min. Interdigit Pause Accept		t_{ID}			40	mS	
Max. Interdigit Pause Reject		t_{DO}	20			µS	
Propagation Delay (St to Q)		t_{PQ}		6	11	µS	TOE = V_{DD}
Propagation Delay (St to StD)		t_{PSt_D}		9	16	µS	
Output Data Set Up (Q to StD)		t_{QSt_D}		3.4		µS	
Propagation Delay (TOE to Q)	Enable	t_{PTE}		50		nS	R_L = 10KΩ C_L = 50pF
	Disable	t_{PTD}		300		nS	
Crystal/Clock Frequency		f_{CLK}	3.5759	3.5795	3.5831	MHz	
Clock Output (OSC 2)	Capacitive Load	C_{LO}			30	pF	

Notes:

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE.
12. External voltage source used to bias V_{REF}.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.

Timing Diagram



Explanation of Events

A) Tone bursts detected, tone duration invalid, outputs not updated.
B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.
C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
D) Outputs switched to high impedance state.
E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

V_{IN} DTMF composite input signal.
ESt Early Steering Output. Indicates detection of valid tone frequencies.
St/GT Steering input/guard time output. Drives external RC timing circuit.
Q1-Q4 4-bit decoded tone output.
StD Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
TOE Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
t_{REC} Maximum DTMF signal duration not detected as valid.
t_{REC} Minimum DTMF signal duration required for valid recognition.
t_{ID} Minimum time between valid DTMF signals.
t_{DO} Maximum allowable drop-out during valid DTMF signal.
t_{DP} Time to detect the presence of valid DTMF signals.
t_{DA} Time to detect the absence of valid DTMF signals.
t_{GTP} Guard time, tone present.
t_{GTA} Guard time, tone absent.

Functional Description

The CAMD CM8870/70C DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP, SOIC, or 20-pin PLCC package configuration. The CM8870/70C's internal architecture consists of a bandsplit filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The CM8870/70C decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by E_{St}. A logic high on ESt causes V_C (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives VC to V_{DD}. GT continues to drive high as long as ESt remains high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$t_{REC} = t_{DP} + t_{GTP}$

$t_{GTP} \approx 0.67\ RC$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guardtimes for tone-present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the CM8870/70C provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1, with the op-amp connected for unity gain and VREF biasing the input at ½ V_{DD}. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.

Clock Circuit

The internal clock circuit is completed with the addition of a standard television color burst crystal or ceramic resonator having a resonant frequency of 3.579545 MHz. The CM8870C in a PLCC package has a buffered oscillator output (OSC3) that can be used to drive clock inputs of other devices such as a microprocessor or other CM887X's as shown in Figure 7. Multiple CM8870/70Cs can be connected as shown in figure 8 such that only one crystal or resonator is required.

Pin Function Table

PIN FUNCTION		
Name	**Description**	
IN+	Non-inverting Input	Connection to the front-end differential amplifier
IN-	Inverting Input	
GS	Gain Select	Gives access to output of front-end differential amplifier for connection of feedback resistor.
V_{REF}	Reference voltage output (nominally $V_{DD}/2$). May be used to bias the inputs at mid-rail.	
INH	Inhibits detection of tones represents keys A, B, C, and D	
OSC3	Digital buffered oscillator output.	
PD	Power Down	Logic high powers down the device and inhibits the oscillator.
OSC1	Clock Input	3.579545 MHz crystal connected between these pins completes internal oscillator.
OSC2	Clock Output	
V_{SS}	Negative power supply (normally connected to OV).	
TOE	Three-state output enable (input). Logic high enables the outputs Q_1-Q_4. Internal pull-up.	
Q_1 Q_2 Q_3 Q_4	Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2).	
StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V_{TSt}.	
ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
St/Gt	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected a St causes the device to register the detected tone pair . The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Fig. 2)	
V_{DD}	Positive power supply.	
IC	Internal Connection.	Must be tied to V_{SS} (for 8870 configuration only)

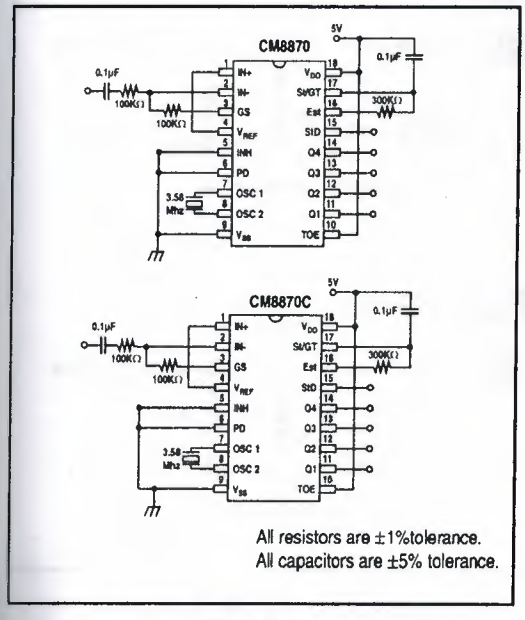


Figure 1.
Single Ended Input Configuration

F_{LOW}	F_{HIGH}	KEY	TOW	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1209	0	H	1	0	1	0
941	1336	·	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z
L = logic Low, H = Logic High, Z = High Impedance							

Figure 2.
Functional Diode Table

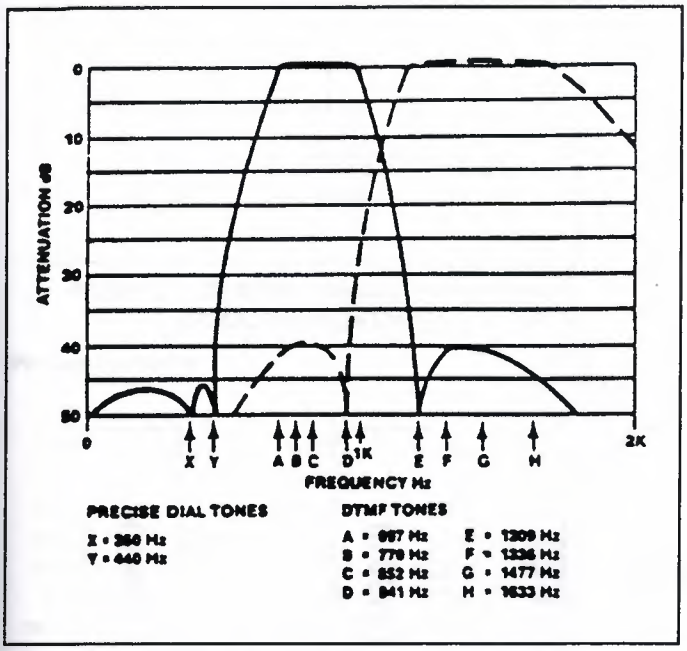


Figure 3. Typical Filter Characteristic

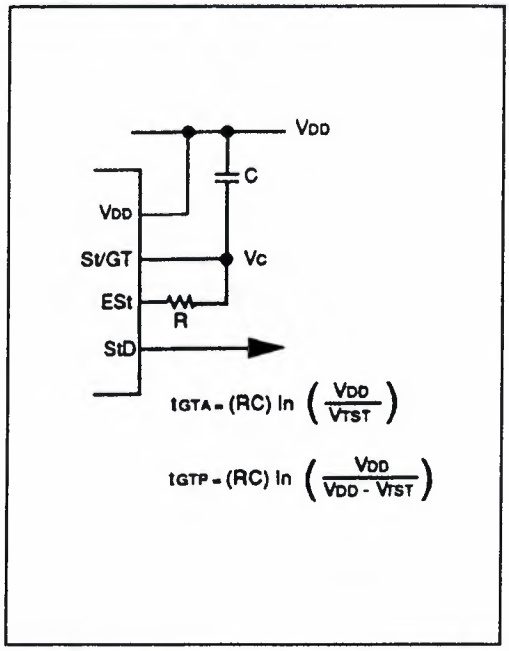


Figure 4. Basic Steering Circuit

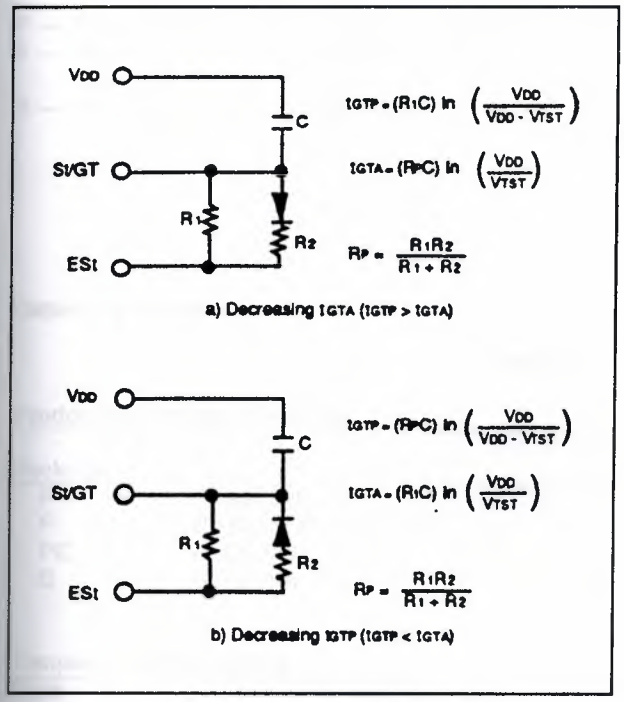


Figure 5. Guard Time Adjustment

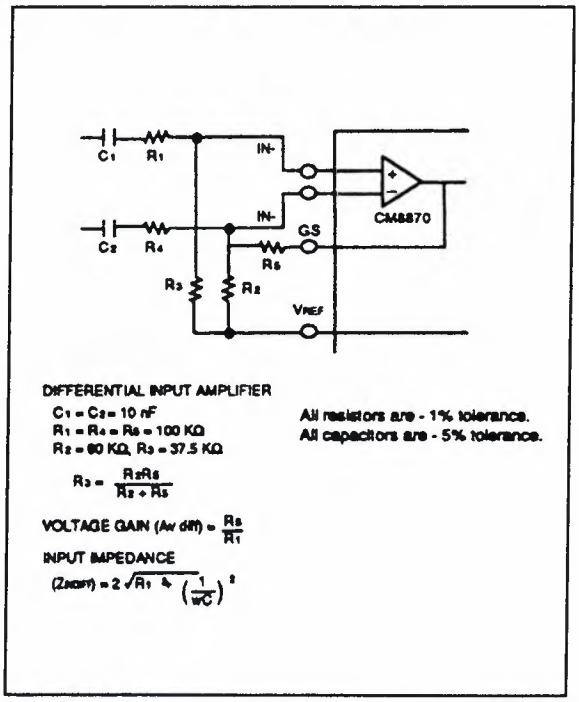


Figure 6. Differential Input Configuration

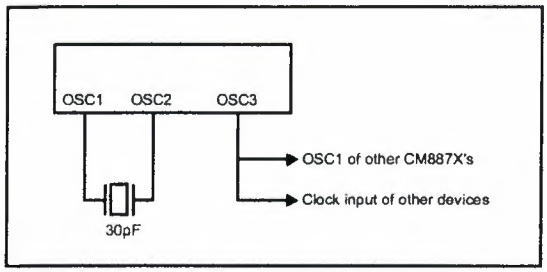


Figure 7. CM8870C Crystal Connection (PLCC Package Only)

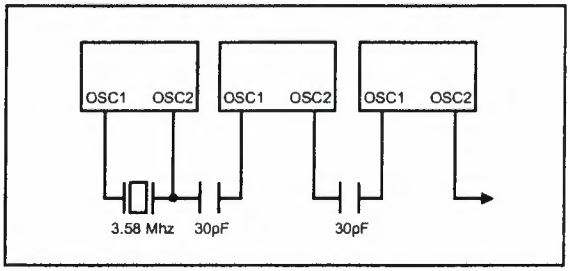
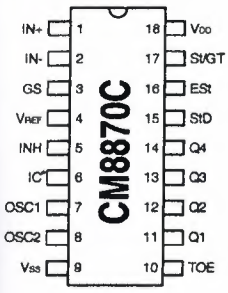
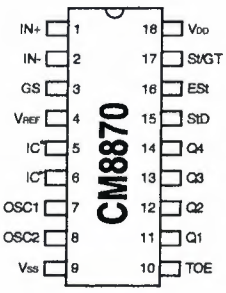


Figure 8. CM8870/70C Crystal Connection

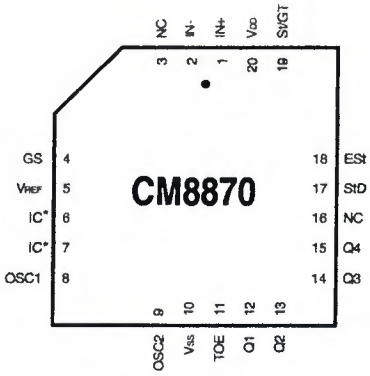
Pin Assignments



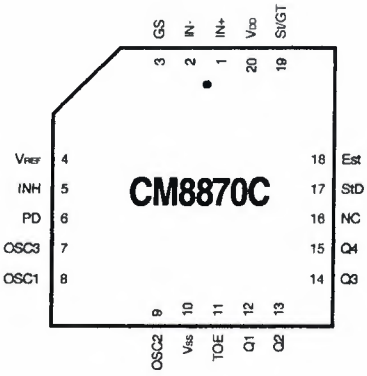
P — Plastic DIP (18)
F — Plastic SOP EIAJ (18)
S — SOIC (18)



P — Plastic DIP (18)
F — Plastic SOP EIAJ (18)
S — SOIC (18)



PE — PLCC (20)
* — Connect To VSS



PE — PLCC (20)

Ordering Information

Example: CM8870 / CM8870C — P — I

Product Identification Number

Package

P	—	Plastic DIP (18)
F	—	Plastic SOP EIAJ (18)
PE	—	PLCC (20)
S	—	SOIC (18)

Temperature/Processing

None	—	0°C to +70°C, ±5% P.S. Tol.
I	—	-40°C to +85°C, ±5% P.S. Tol.

Datasheet of DM74LS154

National Semiconductor

June 1989

54154/DM54154/DM74154
4-Line to 16-Line Decoders/Demultiplexers

General Description

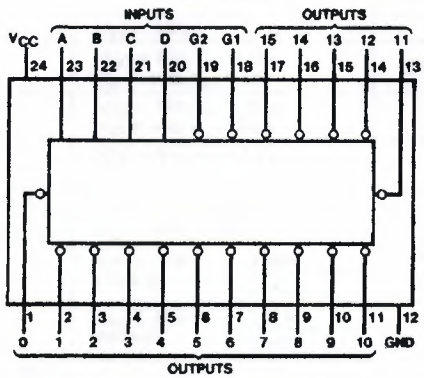
Each or these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  3 levels of logic 19 ns
  Strobe 18 ns
- Typical power dissipation 170 mW
- Alternate Military/Aerospace device (54154) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6548–1

Order Number 54154DMQB, 54154FMQB, DM54154J or DM74154N
See NS Package Number J24A, N24A or W24C

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54154			DM74154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	49	mA
			DM74		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

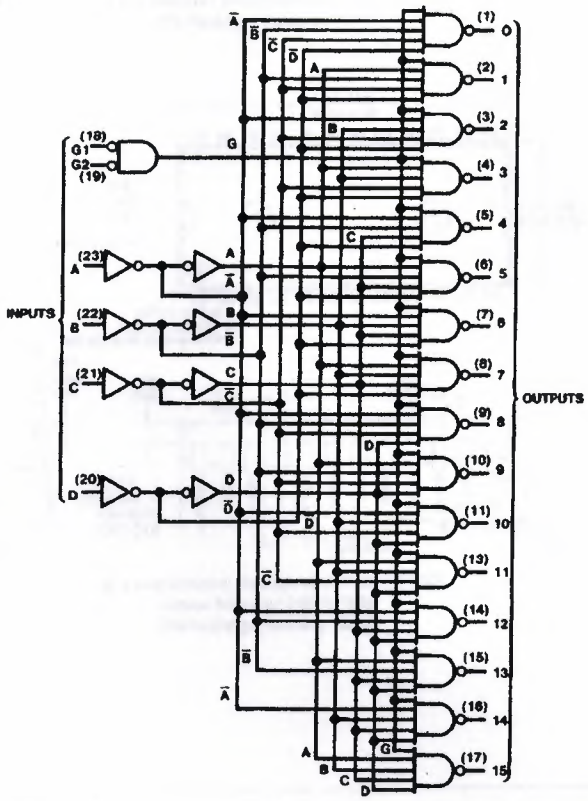
Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		27	ns

Function Table

Inputs						Outputs													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

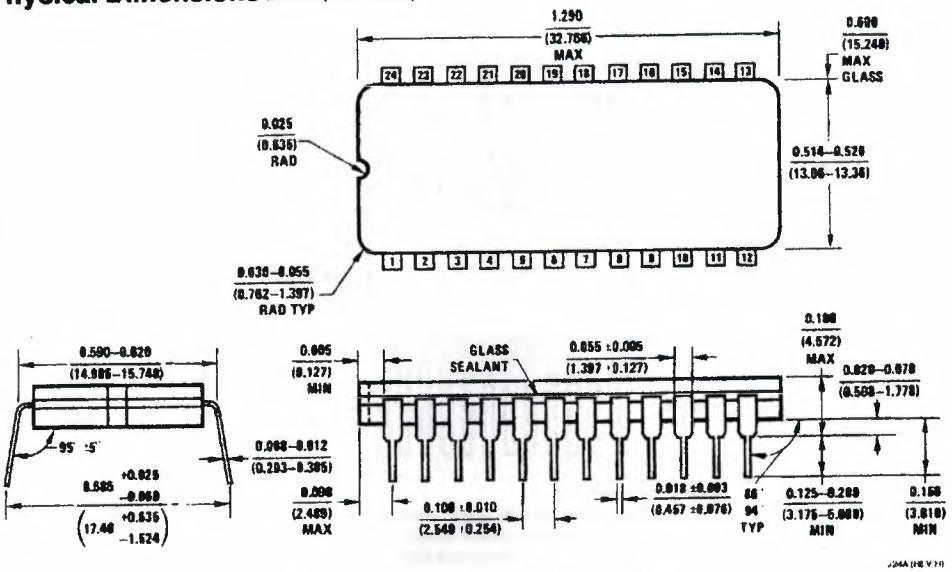
H = High Level, L = Low Level, X = Don't Care

Logic Diagram

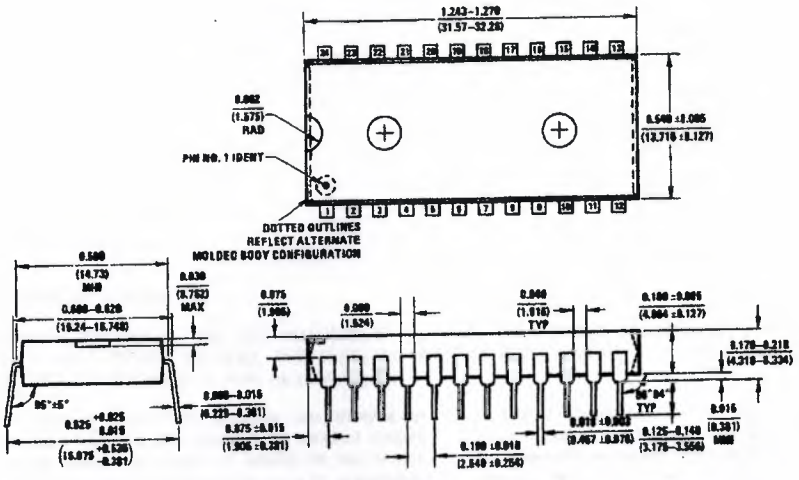


TL/F/6548–2

Physical Dimensions inches (millimeters)

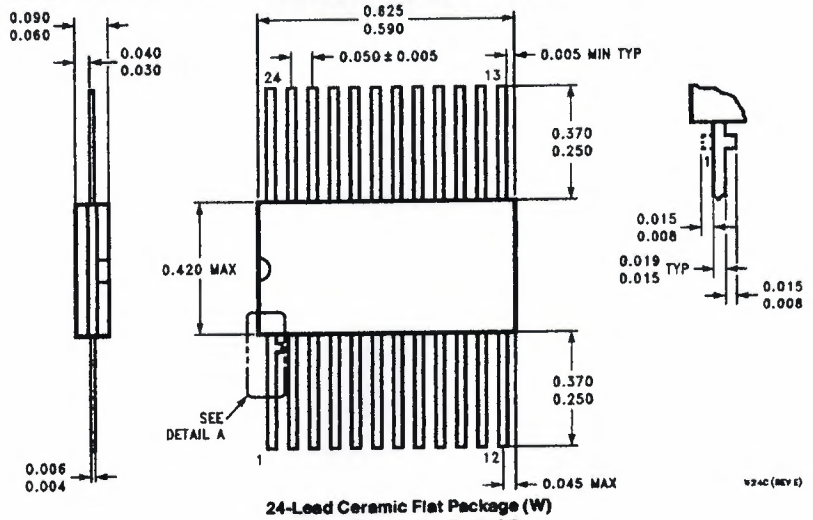


24-Lead Ceramic Dual-In-Line Package (J)
Order Number 54154DMQB or DM54154J
NS Package Number J24A



24-Lead Molded Dual-In-Line Package (N)
Order Number DM74154N
NS Package Number N24A

Physical Dimensions inches (millimeters) (Continued)



24-Lead Ceramic Flat Package (W)
Order Number 54154FMQB
NS Package Number W24C

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nec.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

Datasheet of CD4049UB

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS046A

August 1998 - Revised May 1999

CMOS Hex Buffer/Converters

The CD4049UB and CD4050B devices are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC} = 5V, $V_{OL} \leq 0.4V$, and $I_{OL} \geq 3.3mA$.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

Features

- CD4049UB Inverting
- CD4050B Non-Inverting
- High Sink Current for Driving 2 TTL Loads
- High-To-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-To-Low Logic Level Converter

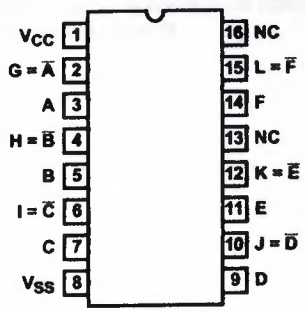
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD4049UBE	-55 to 125	16 Ld PDIP	E16.3
CD4050BE	-55 to 125	16 Ld PDIP	E16.3
CD4049UBF	-55 to 125	16 Ld CERDIP	F16.3
CD4050BF	-55 to 125	16 Ld CERDIP	F16.3
CD4050BM	-55 to 125	16 Ld SOIC	M16.3

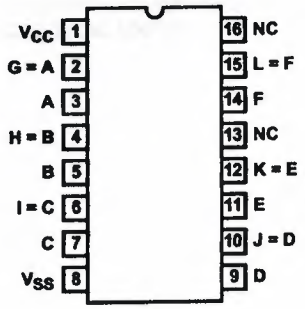
NOTE: Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office o customer service for ordering information.

Pinouts

CD4049UB (PDIP, CERDIP)
TOP VIEW

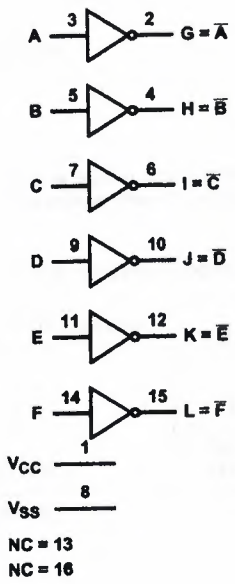


CD4050B (PDIP, CERDIP, SOIC)
TOP VIEW

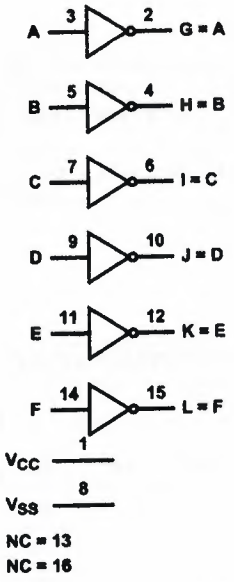


Functional Block Diagrams

CD4049UB



CD4050B



Schematic Diagrams

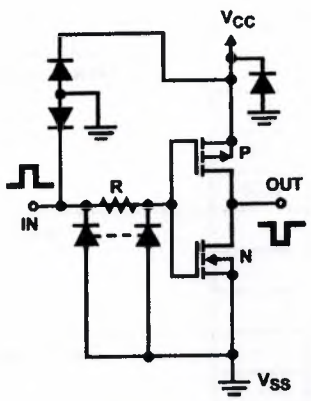


FIGURE 1A. SCHEMATIC DIAGRAM OF CD4049UB, 1 OF 6 IDENTICAL UNITS

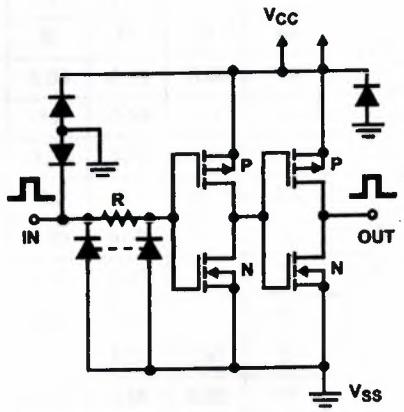


FIGURE 1B. SCHEMATIC DIAGRAM OF CD4050B, 1 OF 6 IDENTICAL UNITS

Absolute Maximum Ratings

Supply Voltage (V+ to V-) . . . . . -0.5V to 20V
DC Input Current, Any One Input . . . . . ±10mA

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W
PDIP Package	90	N/A
CERDIP Package	130	55
SOIC Package	100	N/A

Maximum Junction Temperature (Plastic Package) . . . . . 150°
Maximum Storage Temperature Range . . . . . -65°C to 150°
Maximum Lead Temperature (Soldering 10s) . . . . . 265°
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of th device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Quiescent Device Current I_{DD} (Max)	-	0,5	5	1	1	30	30	-	0.02	1	µA
	-	0,10	10	2	2	60	60	-	0.02	2	µA
	-	0,15	15	4	4	120	120	-	0.02	4	µA
	-	0,20	20	20	20	600	600	-	0.04	20	µA
Output Low (Sink) Current I_{OL} (Min)	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	-	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	-	mA
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	-	mA
	1.5	0,15	15	26	25	20	18	24	48	-	mA
Output High (Source) Current I_{OH} (Min)	4.6	0,5	5	-0.81	-0.73	-0.58	-0.48	-0.65	-1.2	-	mA
	2.5	0,5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	-	mA
	9.5	0,10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0	-	mA
	13.5	0,15	15	-5.2	-4.8	-3.5	-3.1	-4.3	-8.0	-	mA
Out Voltage Low Level V_{OL} (Max)	-	0,5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,15	5	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage High Level V_{OH} (Min)	-	0,5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0,10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0,15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, V_{IL} (Max) CD4049UB	4.5	-	5	1	1	1	1	-	-	1	V
	9	-	10	2	2	2	2	-	-	2	V
	13.5	-	15	2.5	2.5	2.5	2.5	-	-	2.5	V
Input Low Voltage, V_{IL} (Max) CD4050B	0.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1	-	10	3	3	3	3	-	-	3	V
	1.5	-	15	4	4	4	4	-	-	4	V
Input High Voltage, V_{IH} Min CD4049UB	0.5	-	5	4	4	4	4	4	-	-	V
	1	-	10	8	8	8	8	8	-	-	V
	1.5	-	15	12.5	12.5	12.5	12.5	12.5	-	-	V

DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Input High Voltage, V_{IH} Min CD4050B	4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	9	-	10	7	7	7	7	7	-	-	V
	13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I_{IN} Max	-	0,18	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	µA

AC Electrical Specifications $T_A = 25°C$, Input t_r, $t_f = 20ns$, $C_L = 50pF$, $R_L = 200kΩ$

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V_{IN}	V_{CC}	TYP	MAX	
Propagation Delay Time Low to High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	ns
	10	5	45	90	ns
	15	15	25	50	ns
	15	5	45	90	ns
Propagation Delay Time Low to High, t_{PLH} CD4050B	5	5	70	140	ns
	10	10	40	80	ns
	10	5	45	90	ns
	15	15	30	60	ns
	15	5	40	80	ns
Propagation Delay Time High to Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	ns
	10	5	15	30	ns
	15	15	15	30	ns
	15	5	10	20	ns
Propagation Delay Time High to Low, t_{PHL} CD4050B	5	5	55	110	ns
	10	10	22	55	ns
	10	5	50	100	ns
	15	15	15	30	ns
	15	5	50	100	ns
Transition Time, Low to High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	ns
	15	15	30	60	ns
Transition Time, High to Low, t_{THL}	5	5	30	60	ns
	10	10	20	40	ns
	15	15	15	30	ns
Input Capacitance, C_{IN} CD4049UB	-	-	15	22.5	pF
Input Capacitance, C_{IN} CD4050B	-	-	5	7.5	pF

Typical Performance Curves

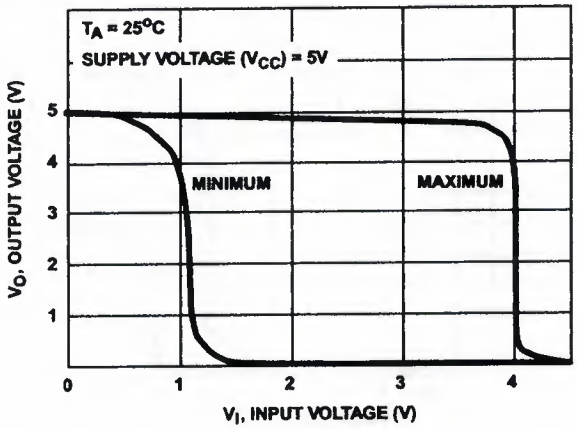


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4049UB

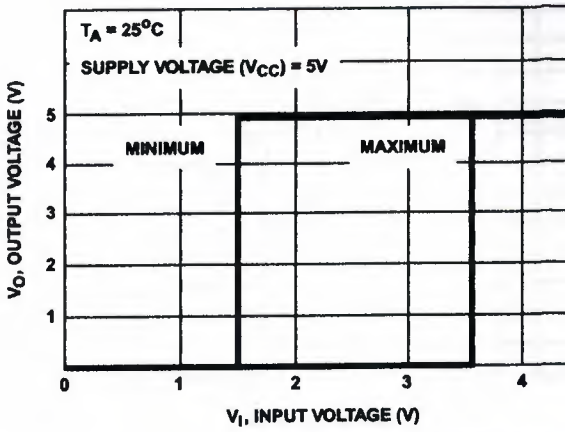


FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4050B

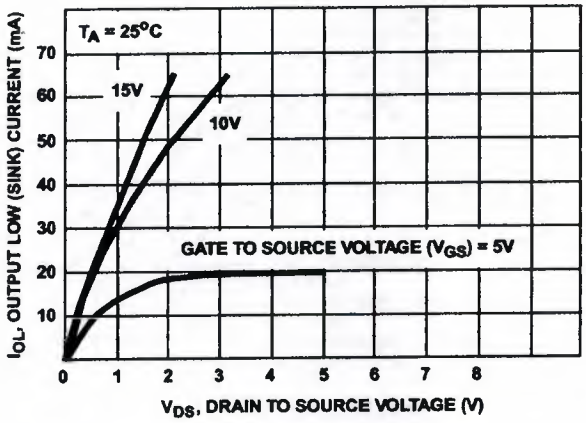


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

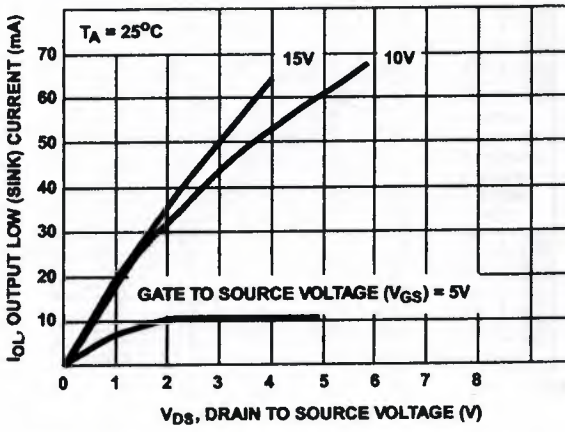


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT DRA CHARACTERISTICS

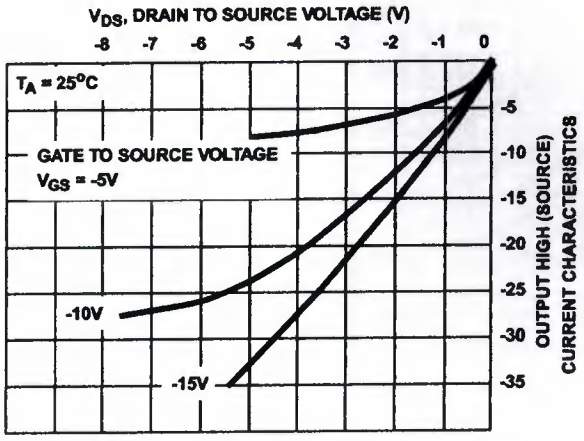


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

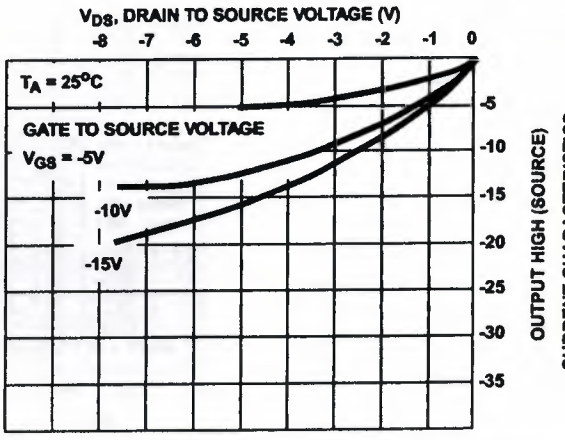


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Curves (Continued)

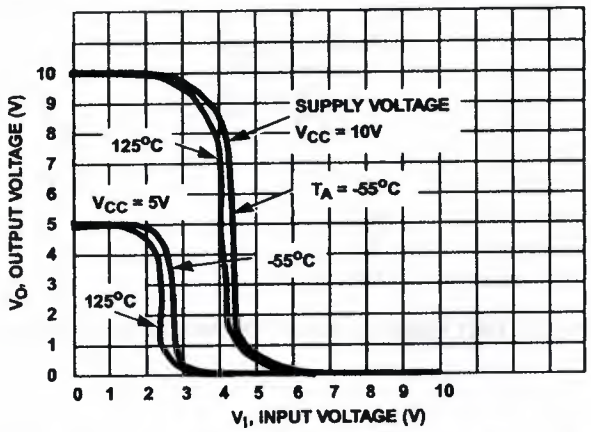


FIGURE 8. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4049UB

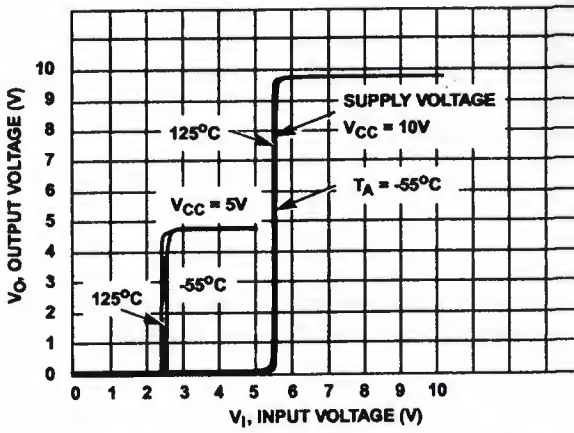


FIGURE 9. TYPICAL VOLTAGE TRANSFER CHARACTERISTIC AS A FUNCTION OF TEMPERATURE FOR CD4050

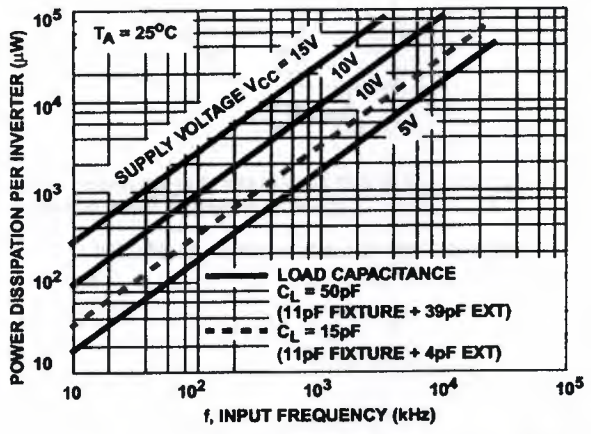


FIGURE 10. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

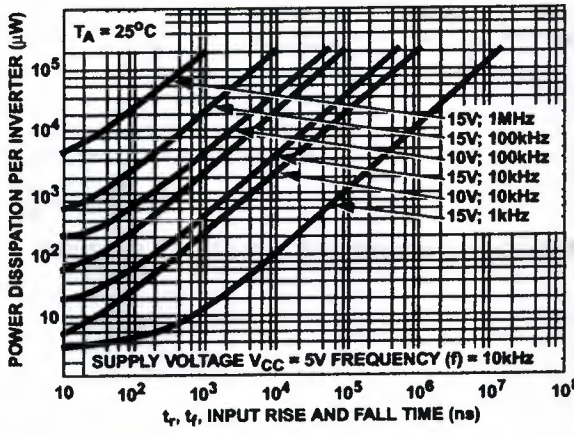


FIGURE 11. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4049U

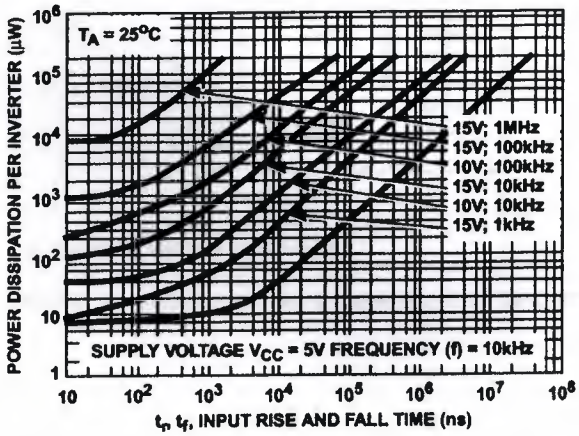


FIGURE 12. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4050B

Test Circuits

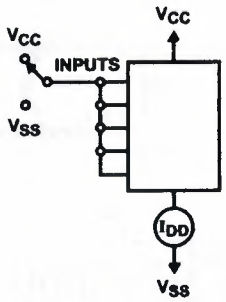
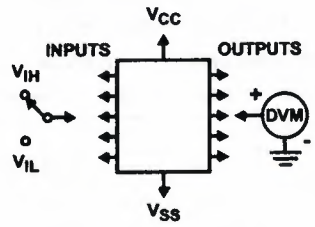
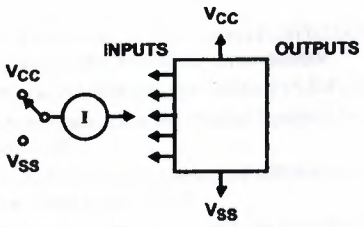


FIGURE 13. QUIESCENT DEVICE CURRENT TEST CIRCUIT



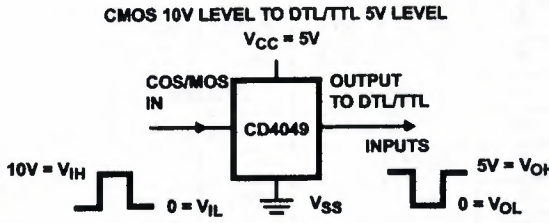
NOTE: Test any one input with other inputs at V_{CC} or V_{SS}.

FIGURE 14. INPUT VOLTAGE TEST CIRCUIT



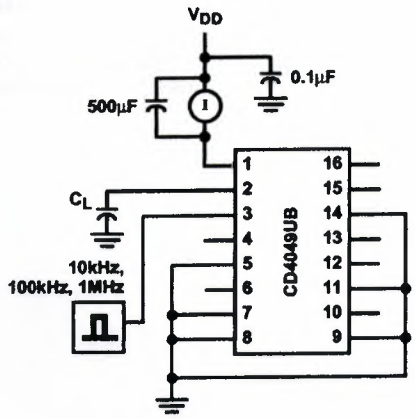
NOTE: Measure inputs sequentially, to both V_{CC} and V_{SS} connect all unused inputs to either V_{CC} or V_{SS}.

FIGURE 15. INPUT CURRENT TEST CIRCUIT



In Terminal - 3, 5, 7, 9, 11, or 14
Out Terminal - 2, 4, 6, 10, 12 or 15
V_{CC} Terminal - 1
V_{SS} Terminal - 8

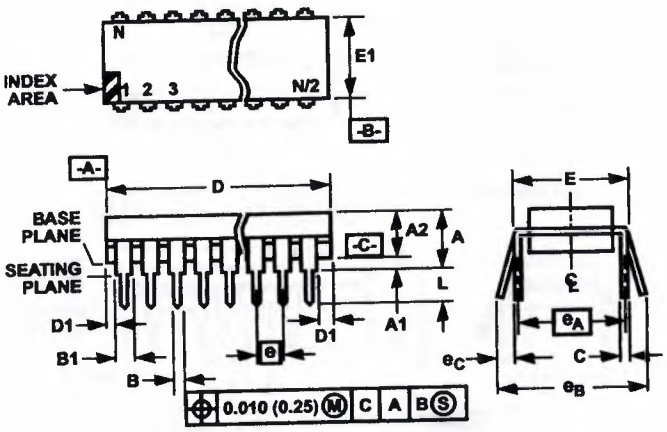
FIGURE 16. LOGIC LEVEL CONVERSION APPLICATION



C_L INCLUDES FIXTURE CAPACITANCE

FIGURE 17. DYNAMIC POWER DISSIPATION TEST CIRCUITS

Dual-In-Line Plastic Packages (PDIP)



NOTES:

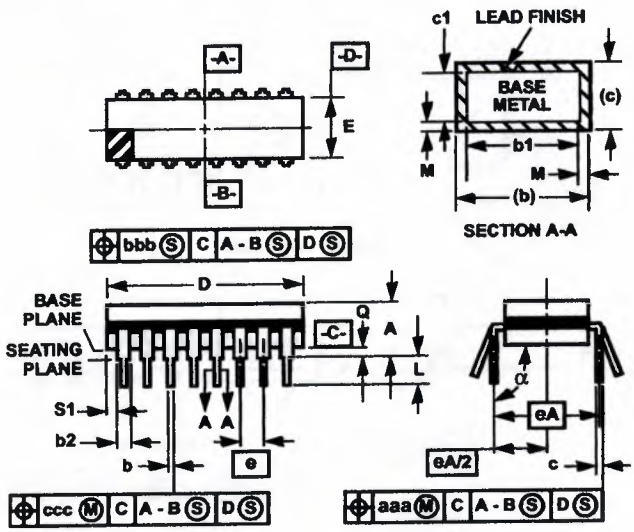
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/9

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



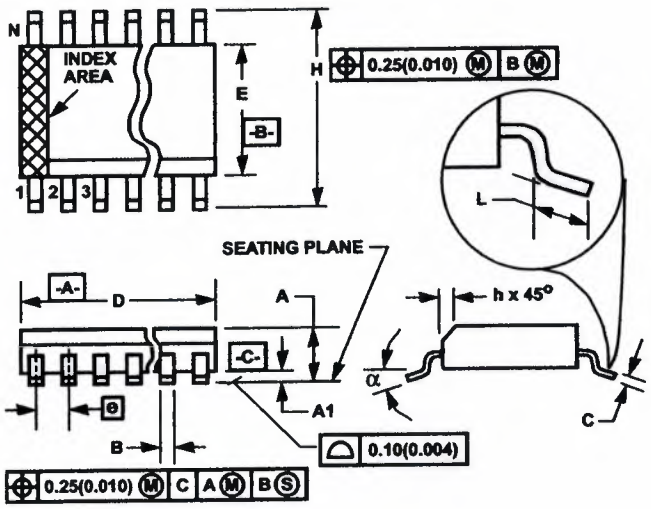
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAG

SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/

Datasheet of CD4013BC

FAIRCHILD
SEMICONDUCTOR™

CD4013BC
Dual D-Type Flip-Flop

General Description

The CD4013B dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL: fan out of 2 driving 74L
  compatibility: or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

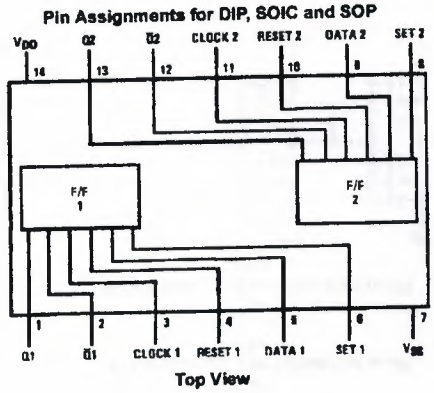
Ordering Code:

Order Number	Package Number	Package Description
CD4013BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
CD4013BCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4013BCN	N14A	14-Lead Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC and SOP



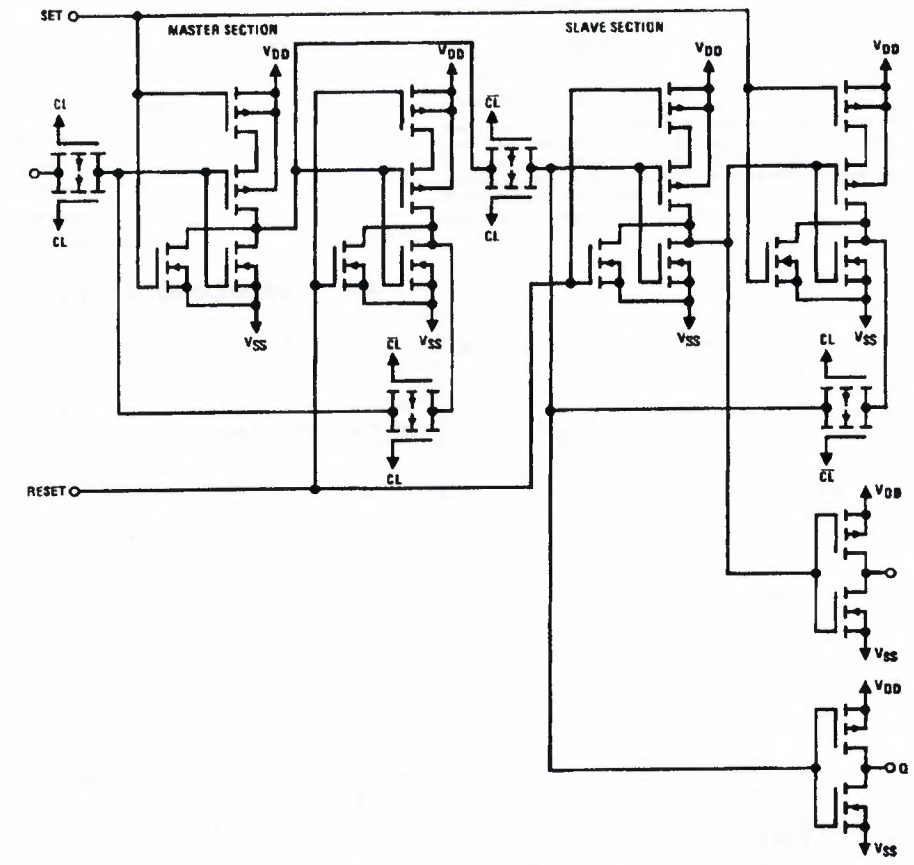
Top View

Truth Table

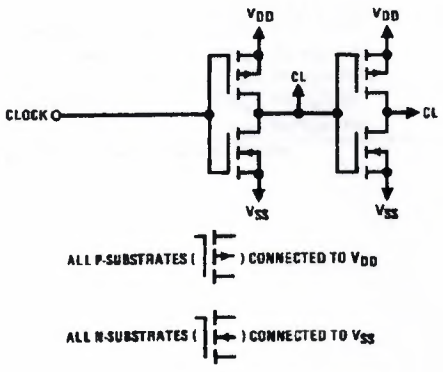
CL (Note 1)	D	R	S	Q	$\overline{Q}$
⌐	0	0	0	0	1
⌐	1	0	0	1	0
⌐	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

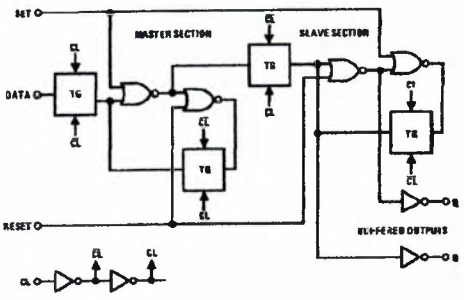
No Change
x = Don't Care Case
Note 1: Level Change

Schematic Diagrams



Logic Diagram





Absolute Maximum Ratings (Note 2)

(Note 3)

DC Supply Voltage (V_{DD})	−0.5 V_{DC} to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 V_{DC} to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 3)

DC Supply Voltage (V_{DD})	+3 V_{DC} to +15 V_{DC}
Input Voltage (V_{IN})	0 V_{DC} to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8.0			8.0		60	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16.0			16.0		120	µA
V_{OL}	LOW Level Output Voltage	$\|I_O\|$ < 1.0 µA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	$\|I_O\|$ < 1.0 µA								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1.0 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1.0 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

Note 4: I_{OH} and I_{OL} are measured one output at a time.

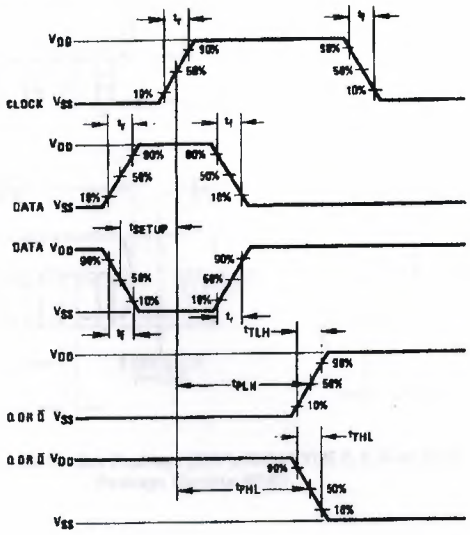
AC Electrical Characteristics (Note 5)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, unless otherwise noted

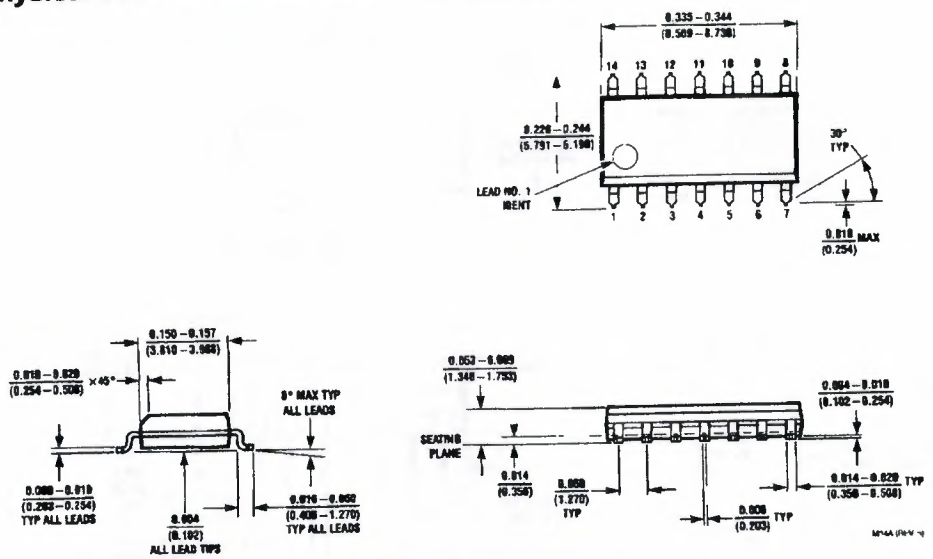
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			15	µs
		$V_{DD} = 10V$			10	µs
		$V_{DD} = 15V$			5	µs
t_{SU}	Minimum Set-Up Time	$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		15	30	ns
		$V_{DD} = 15V$		12	25	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.5	5		MHz
		$V_{DD} = 10V$	6.2	12.5		MHz
		$V_{DD} = 15V$	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

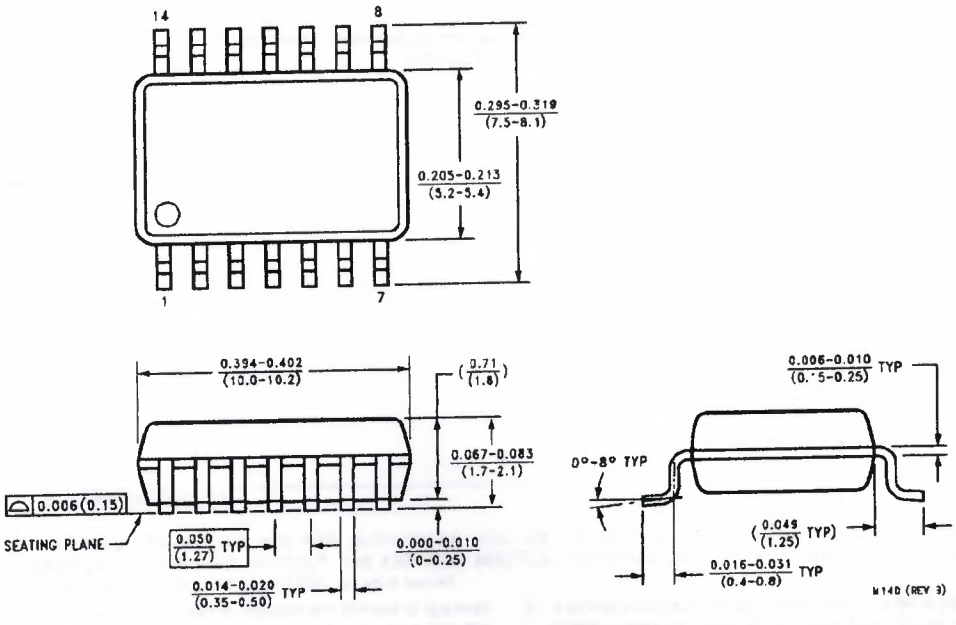
Switching Time Waveforms



Physical Dimensions inches (millimeters) unless otherwise noted

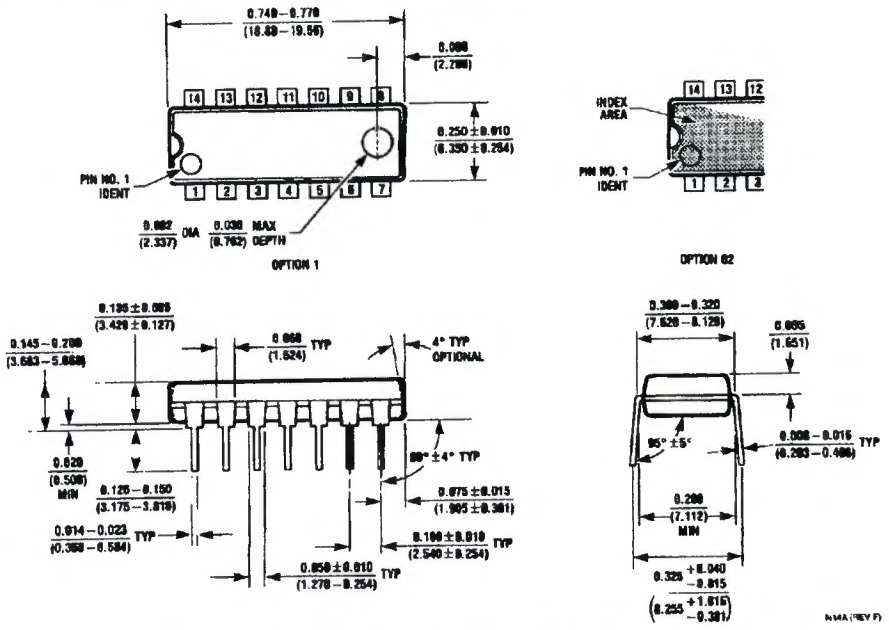


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

Datasheet of PC817

PC817 Series

High Density Mounting Type Photocoupler

● Lead forming type (I type) and taping reel type (P type) are also available. (**PC817I/PC817P**)
●● TÜV (VDE0884) approved type is also available as an option.

■ Features

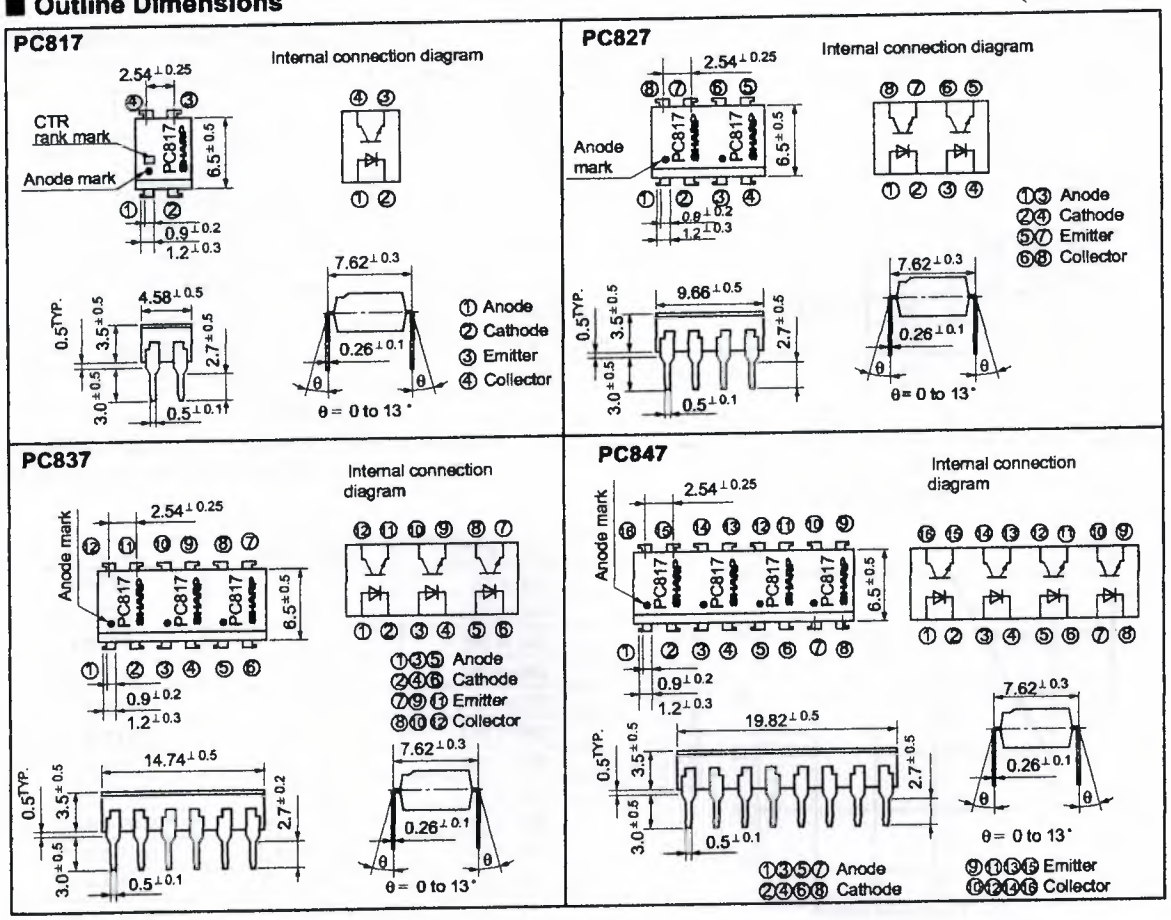
1. Current transfer ratio
   (CTR: MIN. 50% at I_F = 5mA, V_{CE}=5V)
2. High isolation voltage between input and output (V_{iso}: 5 000V $_{rms}$)
3. Compact dual-in-line package
   PC817 : 1-channel type
   PC827 : 2-channel type
   PC837 : 3-channel type
   PC847 : 4-channel type
4. Recognized by UL, file No. E64380

■ Applications

1. Computer terminals
2. System appliances, measuring instruments
3. Registers, copiers, automatic vending machines
4. Electric home appliances, such as fan heaters, etc.
5. Signal transmission between circuits of different potentials and impedances

■ Outline Dimensions

(Unit : mm)



■ Absolute Maximum Ratings (Ta= 25°C)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	*1Peak forward current	I_{FM}	1	A
	Reverse voltage	V_R	6	V
	Power dissipation	P	70	mW
Output	Collector-emitter voltage	V_{CEO}	35	V
	Emitter-collector voltage	V_{ECO}	6	V
	Collector current	I_C	50	mA
	Collector power dissipation	P_C	150	mW
Total power dissipation		P_{tot}	200	mW
*2Isolation voltage		V_{iso}	5 000	V_{rms}
Operating temperature		T_{opr}	- 30 to + 100	°C
Storage temperature		T_{stg}	- 55 to + 125	°C
*3Soldering temperature		T_{sol}	260	°C

*1 Pulse width<=100μs, Duty ratio : 0.001
*2 40 to 60% RH, AC for 1 minute
*3 For 10 seconds

■ Electro-optical Characteristics (Ta= 25°C)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage		V_F	I_F = 20mA	-	1.2	1.4	V
	Peak forward voltage		V_{FM}	I_{FM} = 0.5A	-	-	3.0	V
	Reverse current		I_R	V_R = 4V	-	-	10	μA
	Terminal capacitance		C_t	V= 0, f= 1kHz	-	30	250	pF
Output	Collector dark current		I_{CEO}	V_{CE} = 20V	-	-	10^{-7}	A
Transfer characteristics	*4Current transfer ratio		CTR	I_F = 5mA, V_{CE} = 5V	50	-	600	%
	Collector-emitter saturation voltage		$V_{CE(sat)}$	I_F = 20mA, I_C = 1mA	-	0.1	0.2	V
	Isolation resistance		R_{ISO}	DC500V, 40 to 60% RH	5×10^{10}	10^{11}	-	Ω
	Floating capacitance		C_f	V= 0, f= 1MHz	-	0.6	1.0	pF
	Cut-off frequency		f_c	V_{CE}= 5V, I_C= 2mA, R_L= 100Ω, - 3dB	-	80	-	kHz
	Response time	Rise time	t_r	V_{CE}= 2V, I_C= 2mA, R_L= 100Ω	-	4	18	μs
		Fall time	t_f		-	3	18	μs

*4 Classification table of current transfer ratio is shown below.

Model No.	Rank mark	CTR (%)
PC817A	A	80 to 160
PC817B	B	130 to 260
PC817C	C	200 to 400
PC817D	D	300 to 600
PC8●7AB	A or B	80 to 260
PC8●7BC	B or C	130 to 400
PC8●7CD	C or D	200 to 600
PC8●7AC	A, B or C	80 to 400
PC8●7BD	B, C or D	130 to 600
PC8●7AD	A, B, C or D	80 to 600
PC8●7	A, B, C, D or No mark	50 to 600

● : 1 or 2 or 3 or 4

Fig. 1 Forward Current vs. Ambient Temperature

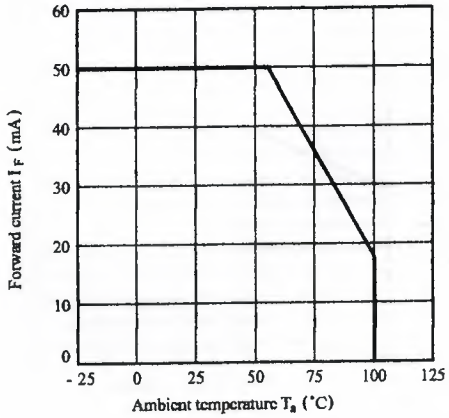


Fig. 2 Collector Power Dissipation vs. Ambient Temperature

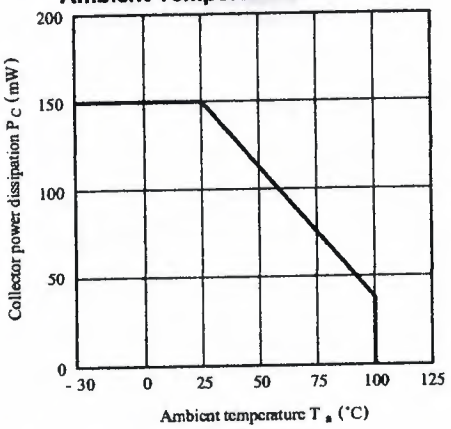


Fig. 3 Peak Forward Current vs. Duty Ratio

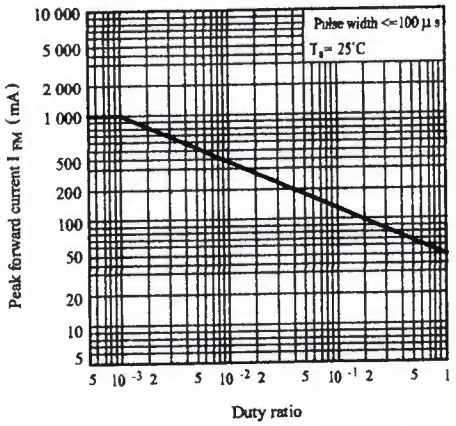


Fig. 4 Current Transfer Ratio vs. Forward Current

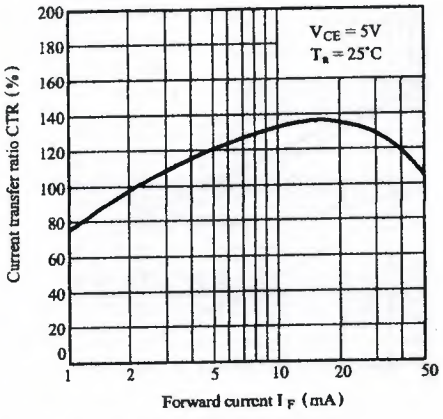


Fig. 5 Forward Current vs. Forward Voltage

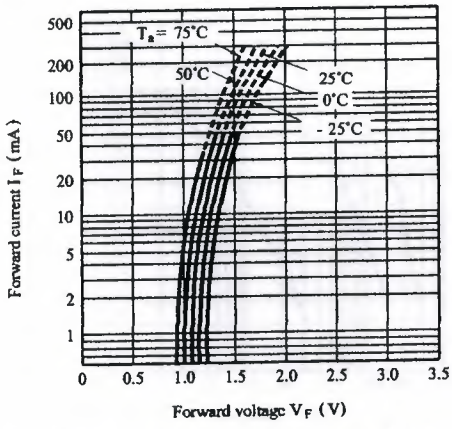


Fig. 6 Collector Current vs. Collector-emitter Voltage

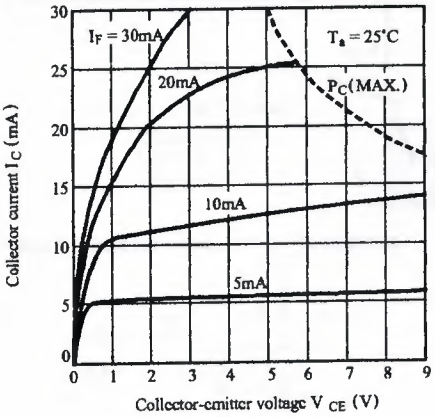


Fig. 7 Relative Current Transfer Ratio vs. Ambient Temperature

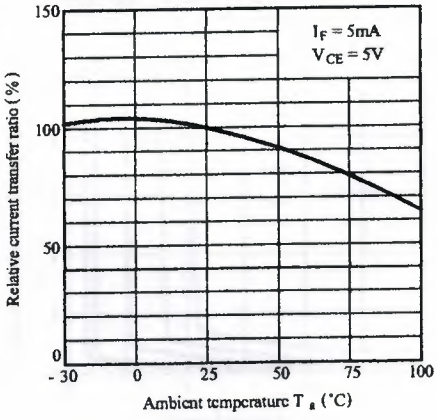


Fig. 8 Collector-emitter Saturation Voltage vs. Ambient Temperature

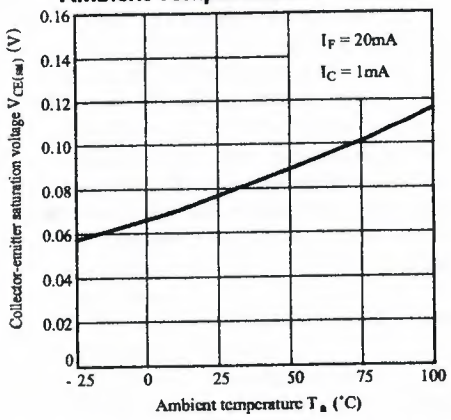


Fig. 9 Collector Dark Current vs. Ambient Temperature

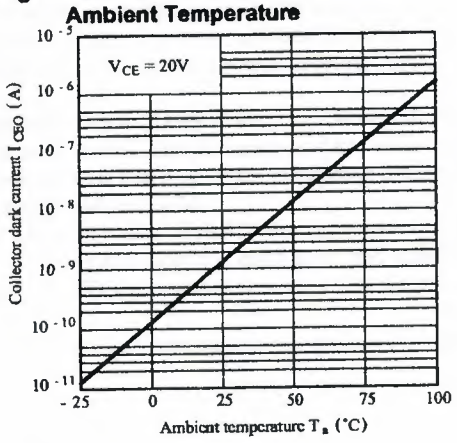


Fig.10 Response Time vs. Load Resistance

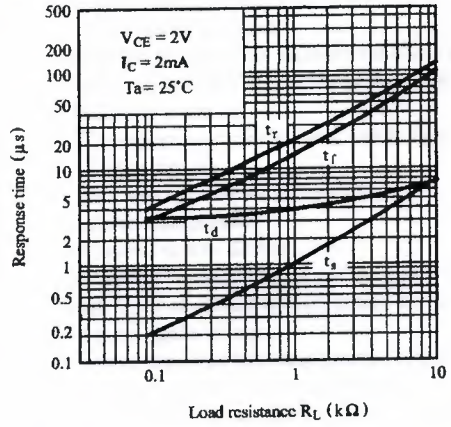
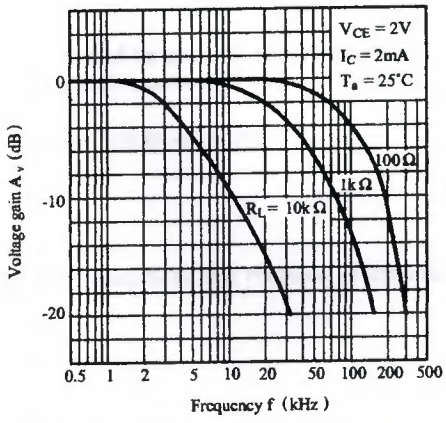
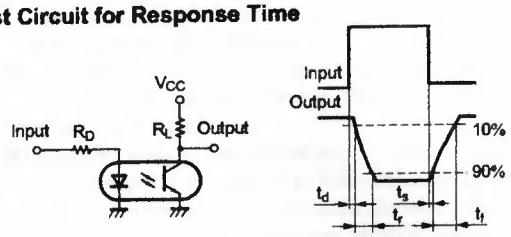


Fig.11 Frequency Response



Test Circuit for Response Time



Test Circuit for Frepuency Response

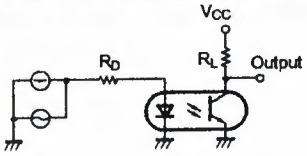
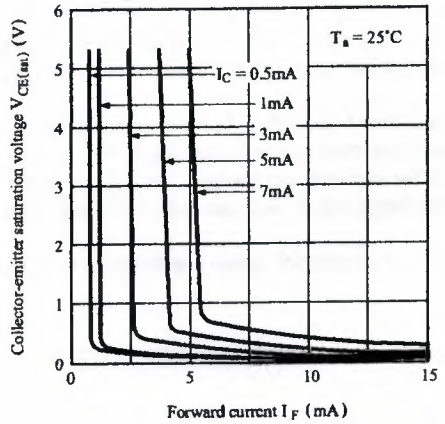


Fig.12 Collector-emitter Saturation Voltage vs. Forward Current



● Please refer to the chapter "Precautions for Use"

NOTICE

- The circuit application examples in this publication are provided to explain representative applications of SHARP devices and are not intended to guarantee any circuit design or license any intellectual property rights. SHARP takes no responsibility for any problems related to any intellectual property right of a third party resulting from the use of SHARP's devices.
- Contact SHARP in order to obtain the latest device specification sheets before using any SHARP device. SHARP reserves the right to make changes in the specifications, characteristics, data, materials, structure, and other contents described herein at any time without notice in order to improve design or reliability. Manufacturing locations are also subject to change without notice.
- Observe the following points when using any devices in this publication. SHARP takes no responsibility for damage caused by improper use of the devices which does not meet the conditions and absolute maximum ratings to be used specified in the relevant specification sheet nor meet the following conditions:

(i) The devices in this publication are designed for use in general electronic equipment designs such as:
- Personal computers
- Office automation equipment
- Telecommunication equipment [terminal]
- Test and measurement equipment
- Industrial control
- Audio visual equipment
- Consumer electronics

(ii) Measures such as fail-safe function and redundant design should be taken to ensure reliability and safety when SHARP devices are used for or in connection with equipment that requires higher reliability such as:
- Transportation control and safety equipment (i.e., aircraft, trains, automobiles, etc.)
- Traffic signals
- Gas leakage sensor breakers
- Alarm equipment
- Various safety devices, etc.

(iii) SHARP devices shall not be used for or in connection with equipment that requires an extremely high level of reliability and safety such as:
- Space applications
- Telecommunication equipment [trunk lines]
- Nuclear power control equipment
- Medical and other life support equipment (e.g., scuba).

- Contact a SHARP representative in advance when intending to use SHARP devices for any "specific" applications other than those recommended by SHARP or when it is unclear which category mentioned above controls the intended use.
- If the SHARP devices listed in this publication fall within the scope of strategic products described in the Foreign Exchange and Foreign Trade Control Law of Japan, it is necessary to obtain approval to export such SHARP devices.
-
- Contact and consult with a SHARP representative if there are any questions about the contents of this publication.

Datasheet of LM7812

FAIRCHILD SEMICONDUCTOR®

May 2006

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C to +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

Block Diagram

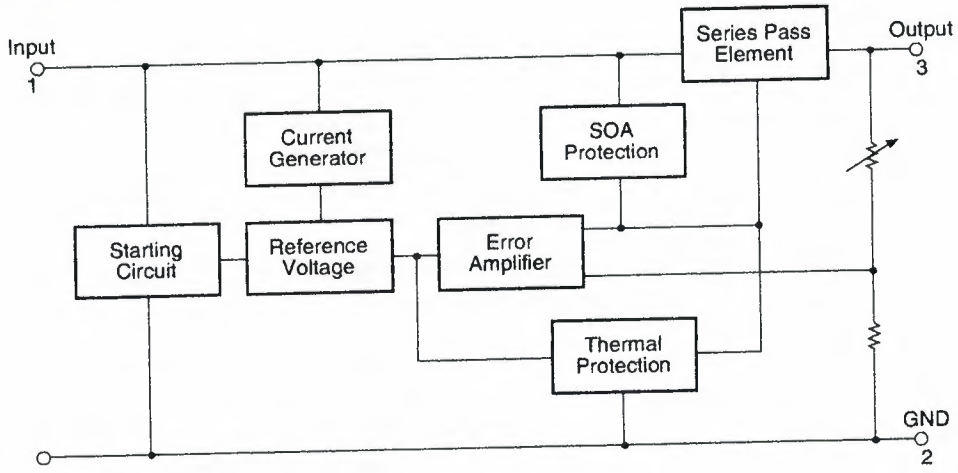


Figure 1.

Pin Assignment

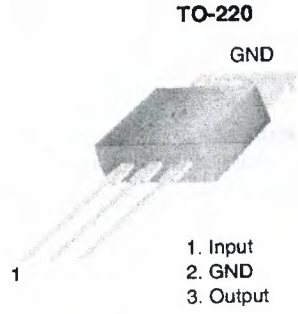


Figure 2.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5V to 18V	35	V
		V_O = 24V	40	V
$R_{\theta JC}$	Thermal Resistance Junction-Cases (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics (LM7812) (Continued)

Refer to the test circuits. -40°C < T_J < 125°C, I_O = 500mA, V_I = 19V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		11.5	12.0	12.5	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 14.5V to 27V		11.4	12.0	12.6	
Regline	Line Regulation(11)	T_J = +25°C	V_I = 14.5V to 30V	–	10.0	240	mV
			V_I = 16V to 22V	–	3.0	120	
Regload	Load Regulation(11)	T_J = +25°C	I_O = 5mA to 1.5A	–	11.0	240	mV
			I_O = 250mA to 750mA	–	5.0	120	
I_Q	Quiescent Current	T_J = +25°C		–	5.1	8.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	0.1	0.5	mA
		V_I = 14.5V to 30V		–	0.5	1.0	
$\Delta V_O/\Delta T$	Output Voltage Drift(12)	I_O = 5mA		–	-1.0	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	76.0	–	µV/V_O
RR	Ripple Rejection(12)	f = 120Hz, V_I = 15V to 25V		55.0	71.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance(12)	f = 1kHz		–	18.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	230	–	mA
I_{PK}	Peak Current(12)	T_J = +25°C		–	2.2	–	A

Notes:

11. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.
12. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7812A) (Continued)

Refer to the test circuits. $0°C < T_J < 125°C$, $I_O = 1A$, $V_I = 19V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_O	Output Voltage	$T_J = +25°C$		11.75	12.0	12.25	V
		$I_O = 5mA$ to $1A$, $P_O \leq 15W$, $V_I = 14.8V$ to $27V$		11.5	12.0	12.5	
Regline	Line Regulation[29]	$V_I = 14.8V$ to $30V$, $I_O = 500mA$		–	10.0	120	mV
		$V_I = 16V$ to $22V$		–	4.0	120	
		$T_J = +25°C$	$V_I = 14.5V$ to $27V$	–	10.0	120	
			$V_I = 16V$ to $22V$	–	3.0	60.0	
Regload	Load Regulation[29]	$T_J = +25°C$, $I_O = 5mA$ to $1.5A$		–	12.0	100	mV
		$I_O = 5mA$ to $1A$		–	12.0	100	
		$I_O = 250mA$ to $750mA$		–	5.0	50.0	
I_Q	Quiescent Current	$T_J = +25°C$		–	5.1	6.0	mA
ΔI_Q	Quiescent Current Change	$I_O = 5mA$ to $1A$		–	–	0.5	mA
		$V_I = 14V$ to $27V$, $I_O = 500mA$		–	–	0.8	
		$V_I = 15V$ to $30V$, $T_J = +25°C$		–	–	0.8	
$\Delta V_O/\Delta T$	Output Voltage Drift[30]	$I_O = 5mA$		–	-1.0	–	mV/°C
V_N	Output Noise Voltage	$f = 10Hz$ to $100kHz$, $T_A = +25°C$		–	10.0	–	$\mu V/V_O$
RR	Ripple Rejection[30]	$f = 120Hz$, $I_O = 500mA$, $V_I = 14V$ to $24V$		–	60.0	–	dB
V_{DROP}	Dropout Voltage	$I_O = 1A$, $T_J = +25°C$		–	2.0	–	V
r_O	Output Resistance[30]	$f = 1kHz$		–	18.0	–	mΩ
I_{SC}	Short Circuit Current	$V_I = 35V$, $T_A = +25°C$		–	250	–	mA
I_{PK}	Peak Current[30]	$T_J = +25°C$		–	2.2	–	A

Note:

29. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

30. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

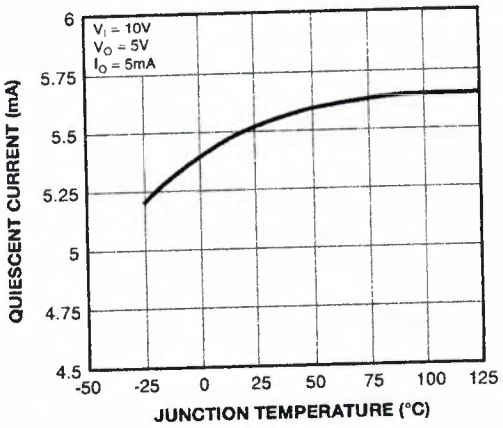


Figure 3. Quiescent Current

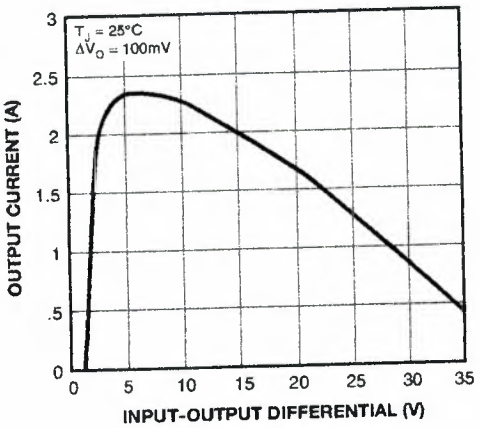


Figure 4. Peak Output Current

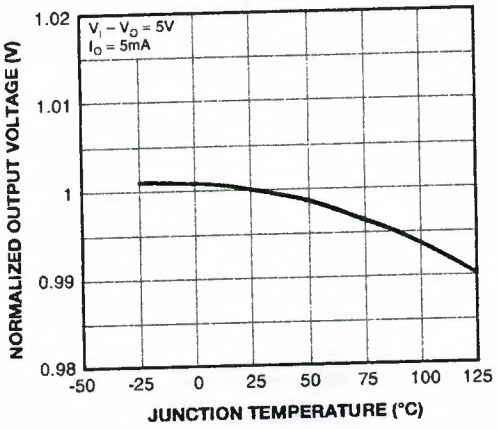


Figure 5. Output Voltage

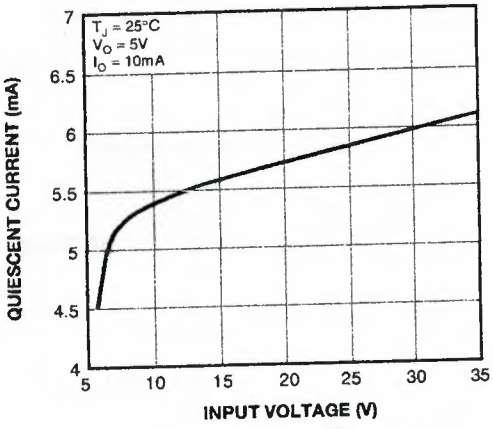


Figure 6. Quiescent Current

Typical Applications

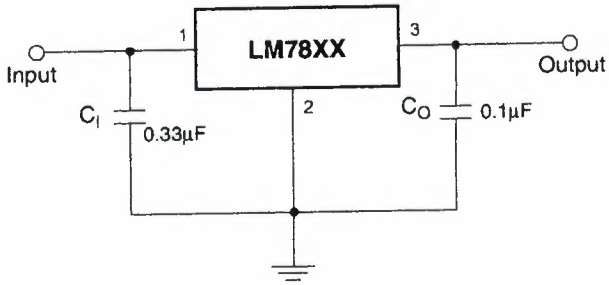


Figure 7. DC Parameters

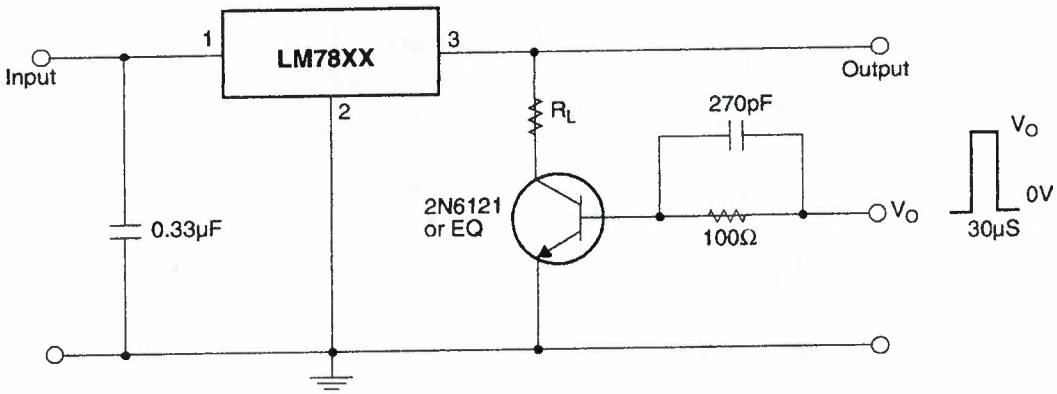


Figure 8. Load Regulation

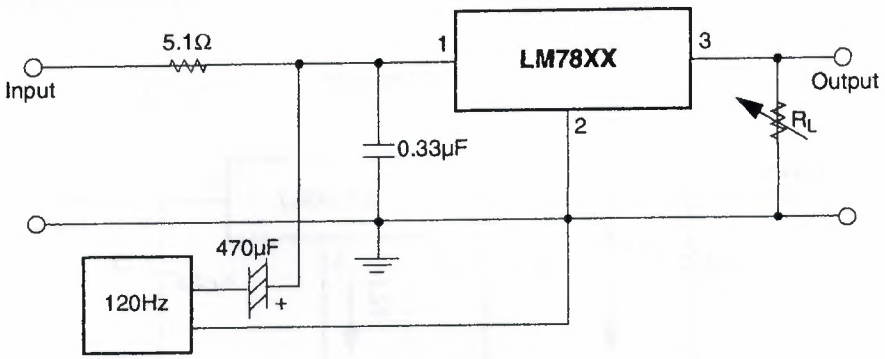


Figure 9. Ripple Rejection

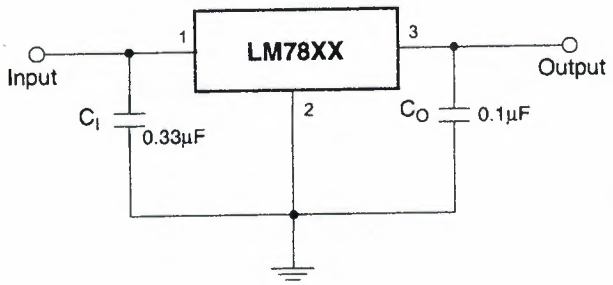
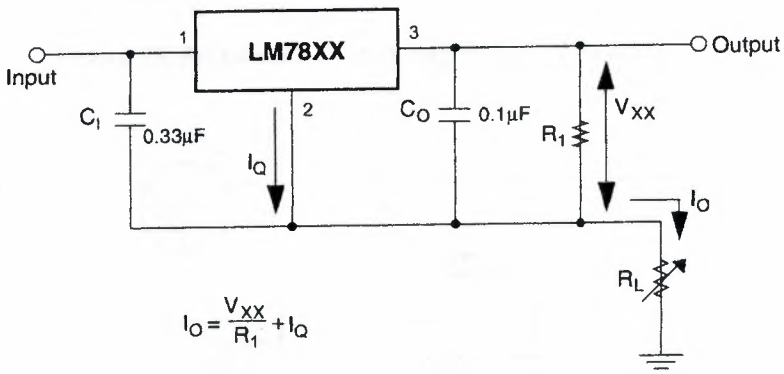


Figure 10. Fixed Output Regulator



Notes:

1. To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
2. C_I is required if regulator is located an appreciable distance from power supply filter.
3. C_O improves stability and transient response.

Figure 11.

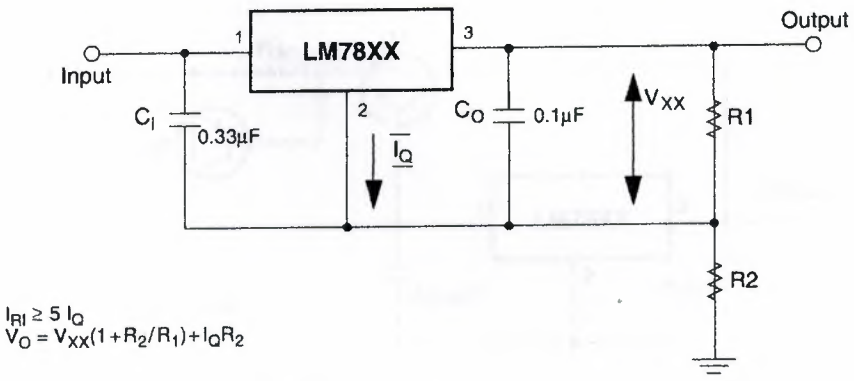


Figure 12. Circuit for Increasing Output Voltage

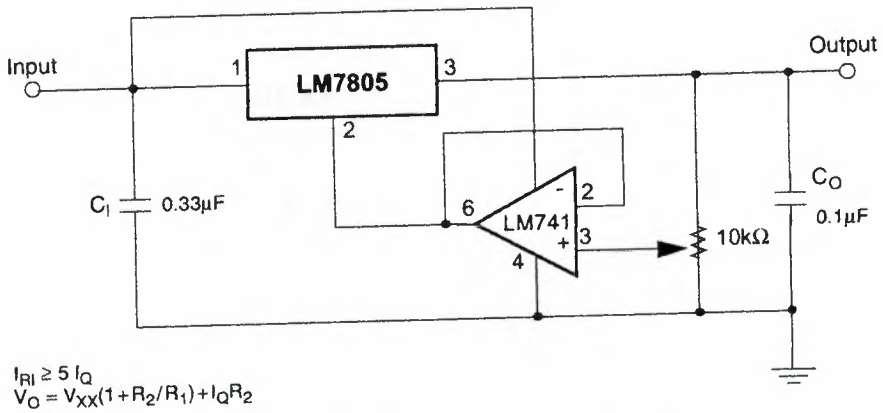


Figure 13. Adjustable Output Regulator (7V to 30V)

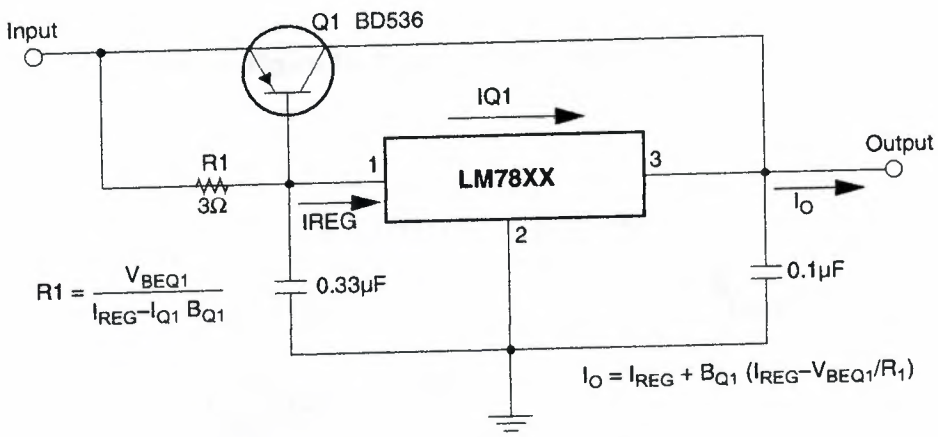


Figure 14. High Current Voltage Regulator

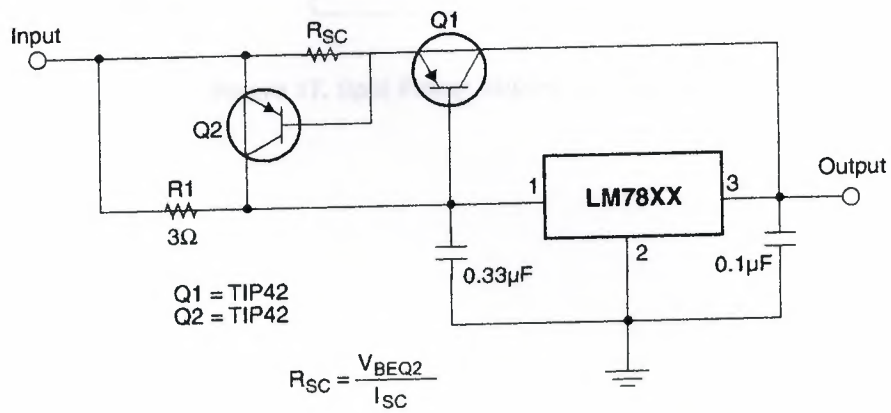


Figure 15. High Output Current with Short Circuit Protection

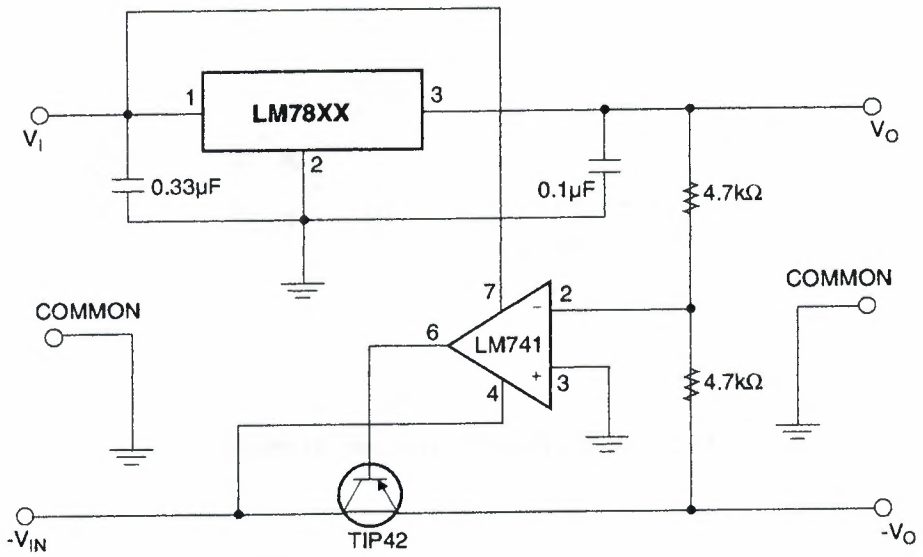


Figure 16. Tracking Voltage Regulator

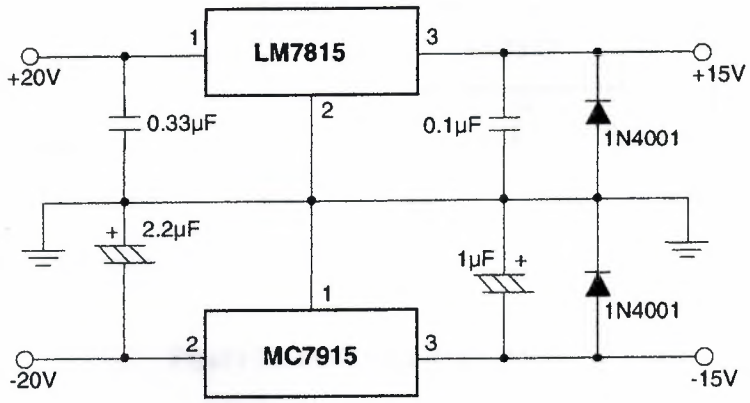


Figure 17. Split Power Supply (±15V – 1A)

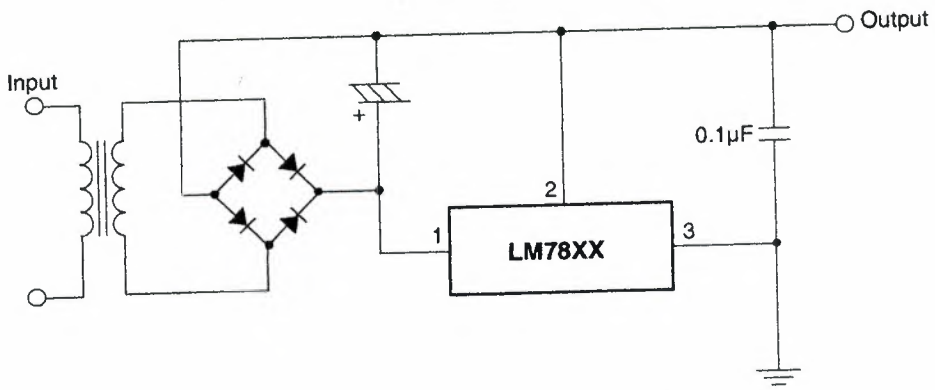


Figure 18. Negative Output Voltage Circuit

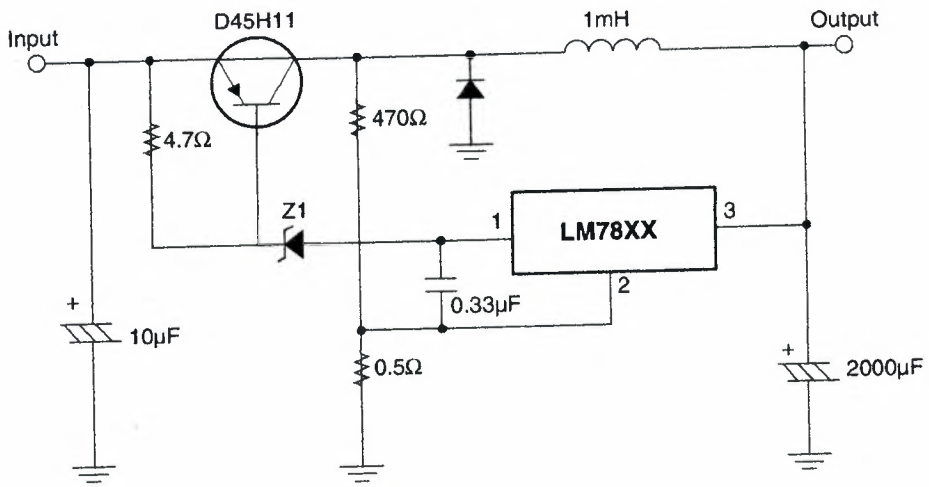


Figure 19. Switching Regulator

Datasheet of LM7805

FAIRCHILD
SEMICONDUCTOR®

May 2006

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C to +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

Block Diagram

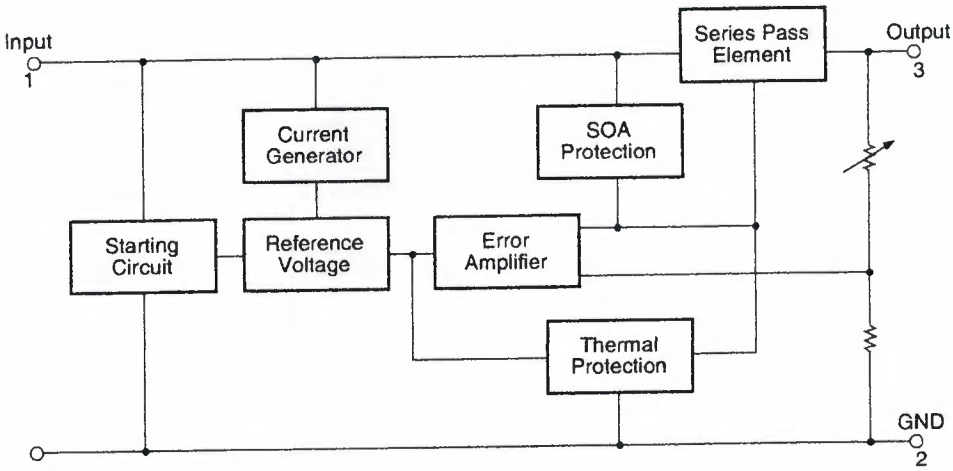


Figure 1.

Pin Assignment

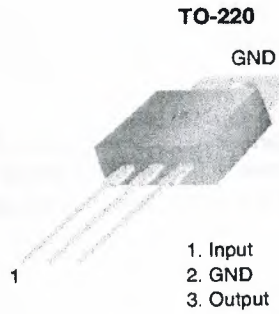


Figure 2.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5V to 18V	35	V
		V_O = 24V	40	V
$R_{\theta JC}$	Thermal Resistance Junction-Cases (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics (LM7805)

Refer to the test circuits. -40°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I = 0.1µF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.8	5.0	5.2	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 7V to 20V		4.75	5.0	5.25	
Regline	Line Regulation(1)	T_J = +25°C	V_O = 7V to 25V	–	4.0	100	mV
			V_I = 8V to 12V	–	1.6	50.0	
Regload	Load Regulation(1)	T_J = +25°C	I_O = 5mA to 1.5A	–	9.0	100	mV
			I_O = 250mA to 750mA	–	4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	8.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	0.03	0.5	mA
		V_I = 7V to 25V		–	0.3	1.3	
$\Delta V_O/\Delta T$	Output Voltage Drift(2)	I_O = 5mA		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	42.0	–	µV/V_O
RR	Ripple Rejection(2)	f = 120Hz, V_O = 8V to 18V		62.0	73.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance(2)	f = 1kHz		–	15.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	230	–	mA
I_{PK}	Peak Current(2)	T_J = +25°C		–	2.2	–	A

Notes:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.
2. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7805A) (Continued)

Refer to the test circuits. $0°C < T_J < 125°C$, $I_O = 1A$, $V_I = 10V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	$T_J = +25°C$		4.9	5.0	5.1	V
		$I_O = 5mA$ to $1A$, $P_O \leq 15W$, $V_I = 7.5V$ to $20V$		4.8	5.0	5.2	
Regline	Line Regulation[19]	$V_I = 7.5V$ to $25V$, $I_O = 500mA$		–	5.0	50.0	mV
		$V_I = 8V$ to $12V$		–	3.0	50.0	
		$T_J = +25°C$	$V_I = 7.3V$ to $20V$	–	5.0	50.0	
			$V_I = 8V$ to $12V$	–	1.5	25.0	
Regload	Load Regulation[19]	$T_J = +25°C$, $I_O = 5mA$ to $1.5A$		–	9.0	100	mV
		$I_O = 5mA$ to $1A$		–	9.0	100	
		$I_O = 250mA$ to $750mA$		–	4.0	50.0	
I_Q	Quiescent Current	$T_J = +25°C$		–	5.0	6.0	mA
ΔI_Q	Quiescent Current Change	$I_O = 5mA$ to $1A$		–	–	0.5	mA
		$V_I = 8V$ to $25V$, $I_O = 500mA$		–	–	0.8	
		$V_I = 7.5V$ to $20V$, $T_J = +25°C$		–	–	0.8	
$\Delta V_O/\Delta T$	Output Voltage Drift[20]	$I_O = 5mA$		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	$f = 10Hz$ to $100kHz$, $T_A = +25°C$		–	10.0	–	$\mu V/V_O$
RR	Ripple Rejection[20]	$f = 120Hz$, $I_O = 500mA$, $V_I = 8V$ to $18V$		–	68.0	–	dB
V_{DROP}	Dropout Voltage	$I_O = 1A$, $T_J = +25°C$		–	2.0	–	V
r_O	Output Resistance[20]	$f = 1kHz$		–	17.0	–	mΩ
I_{SC}	Short Circuit Current	$V_I = 35V$, $T_A = +25°C$		–	250	–	mA
I_{PK}	Peak Current[20]	$T_J = +25°C$		–	2.2	–	A

Notes:

19. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.
20. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

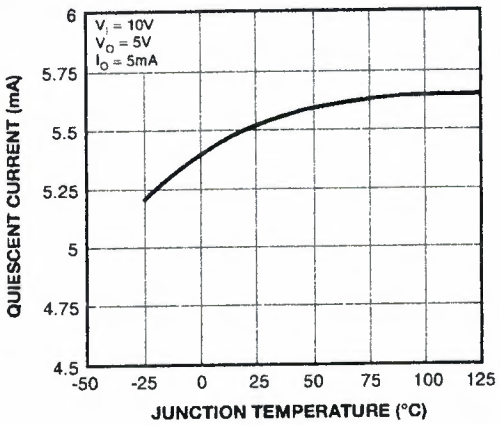


Figure 3. Quiescent Current

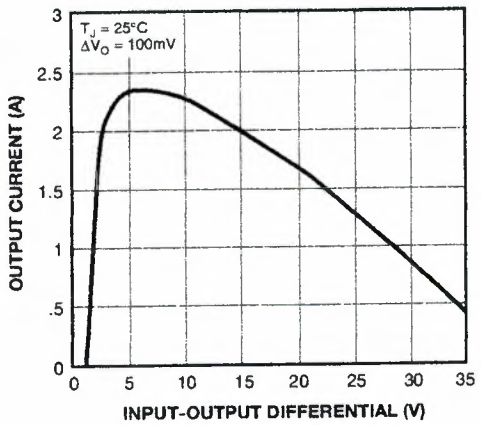


Figure 4. Peak Output Current

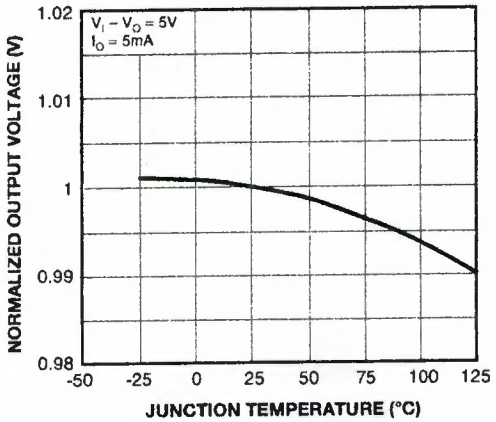


Figure 5. Output Voltage

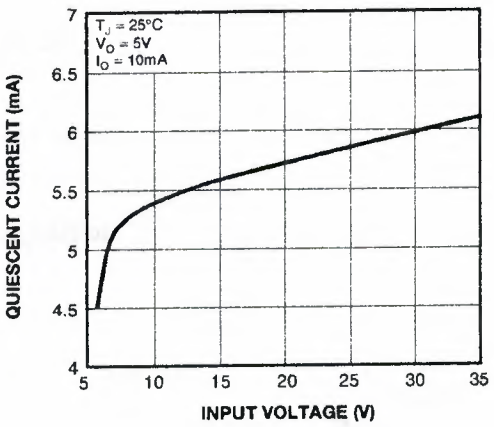


Figure 6. Quiescent Current

Typical Applications

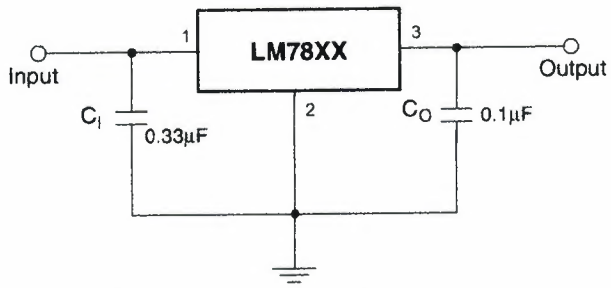


Figure 7. DC Parameters

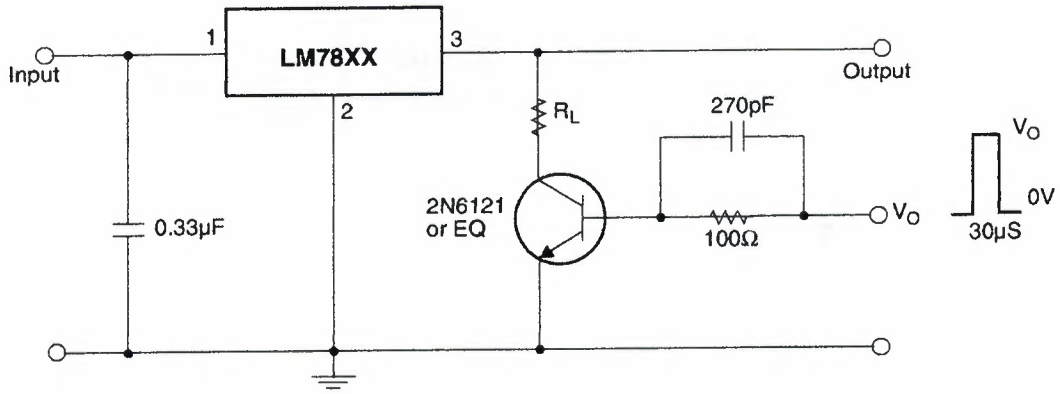


Figure 8. Load Regulation

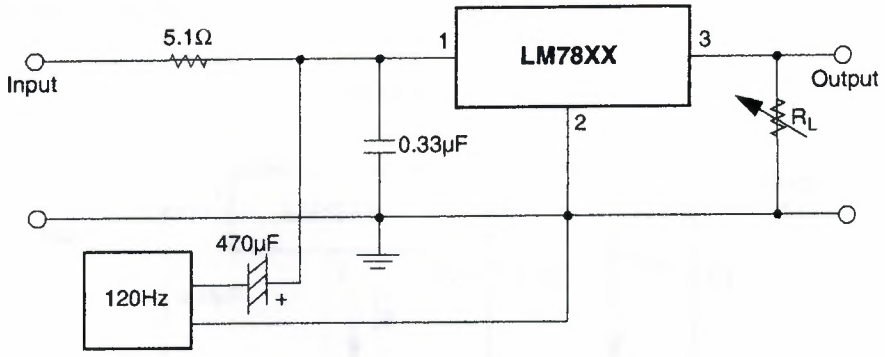


Figure 9. Ripple Rejection

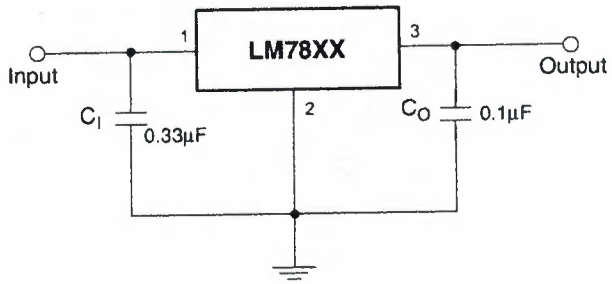
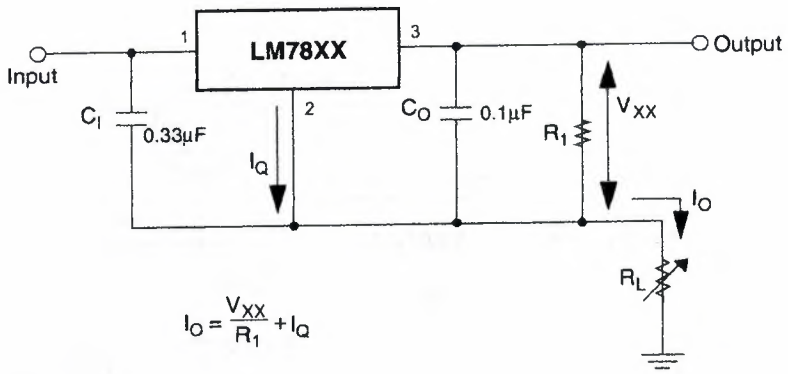


Figure 10. Fixed Output Regulator



Notes:

1. To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
2. C_I is required if regulator is located an appreciable distance from power supply filter.
3. C_O improves stability and transient response.

Figure 11.

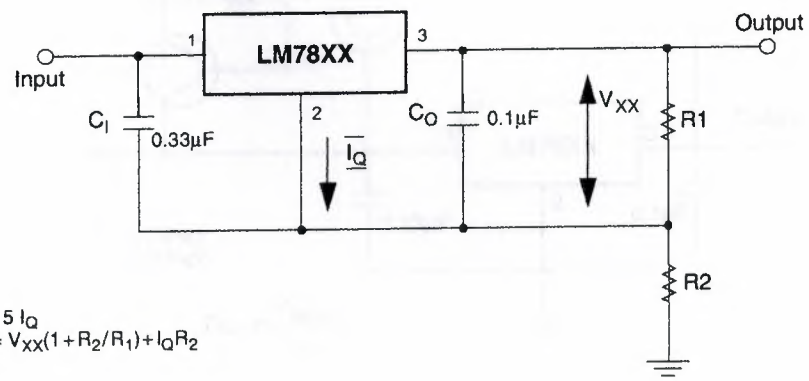


Figure 12. Circuit for Increasing Output Voltage

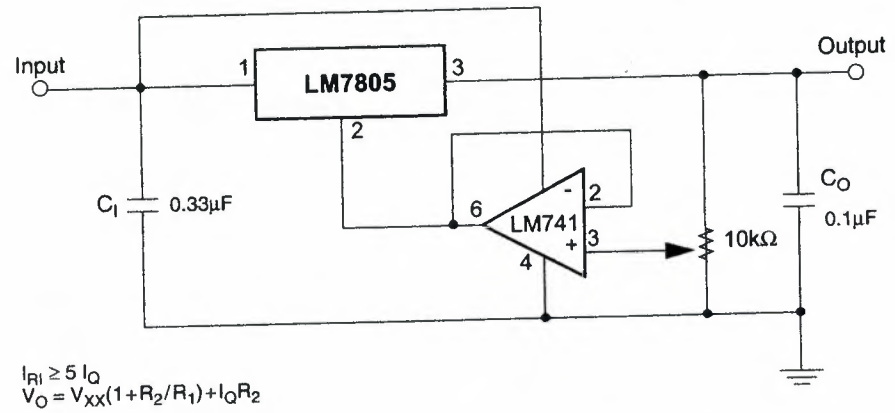


Figure 13. Adjustable Output Regulator (7V to 30V)

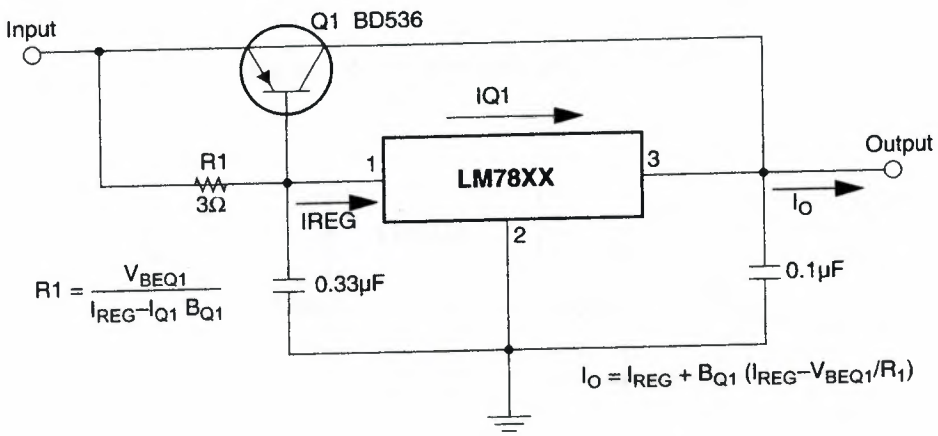


Figure 14. High Current Voltage Regulator

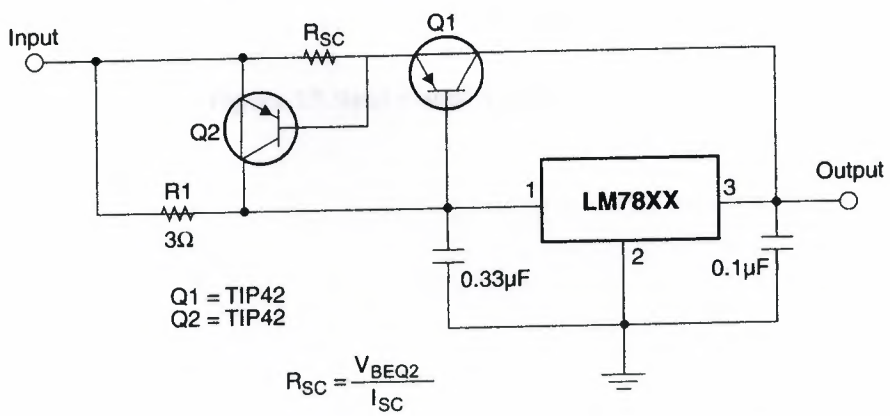


Figure 15. High Output Current with Short Circuit Protection

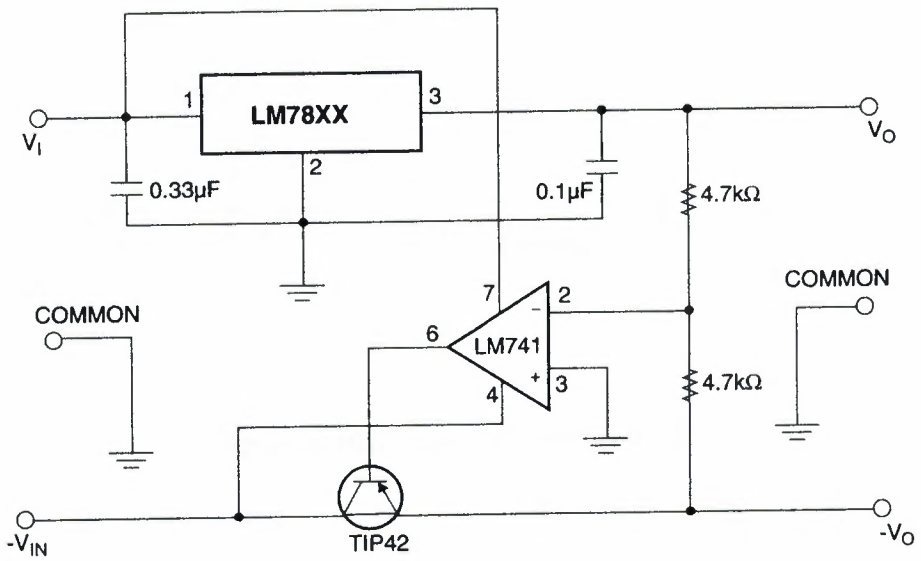


Figure 16. Tracking Voltage Regulator

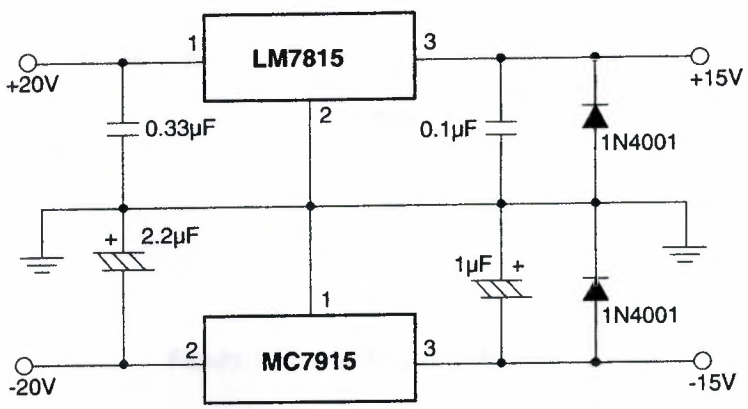


Figure 17. Split Power Supply (±15V – 1A)

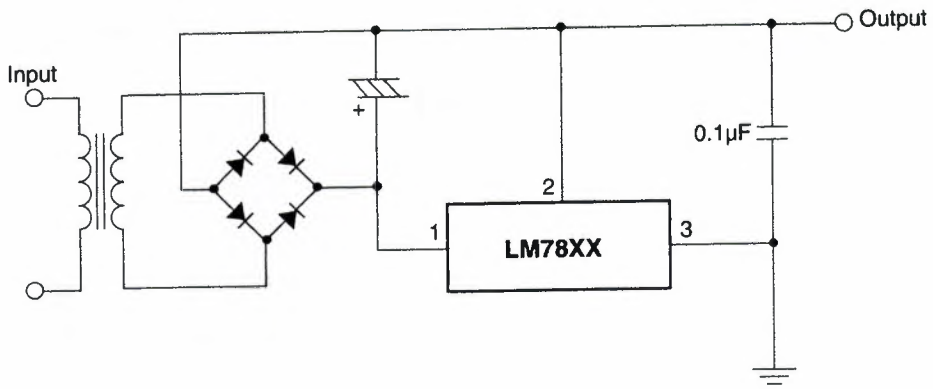


Figure 18. Negative Output Voltage Circuit

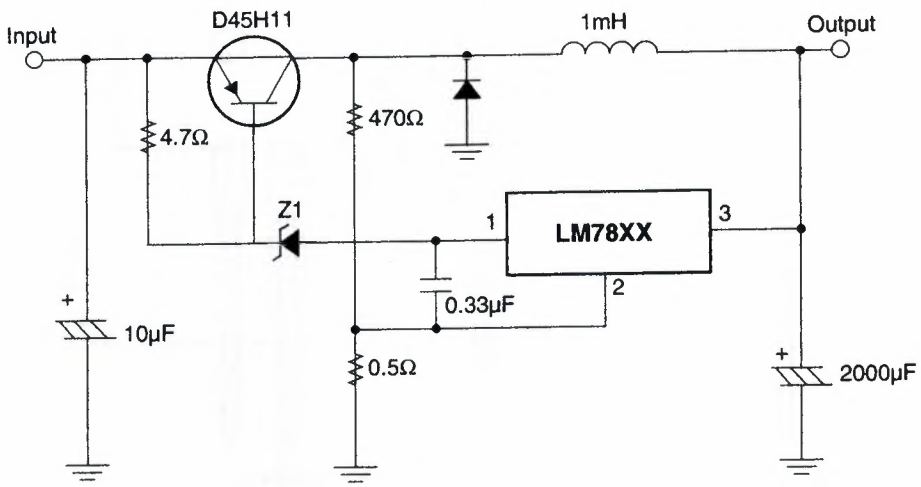
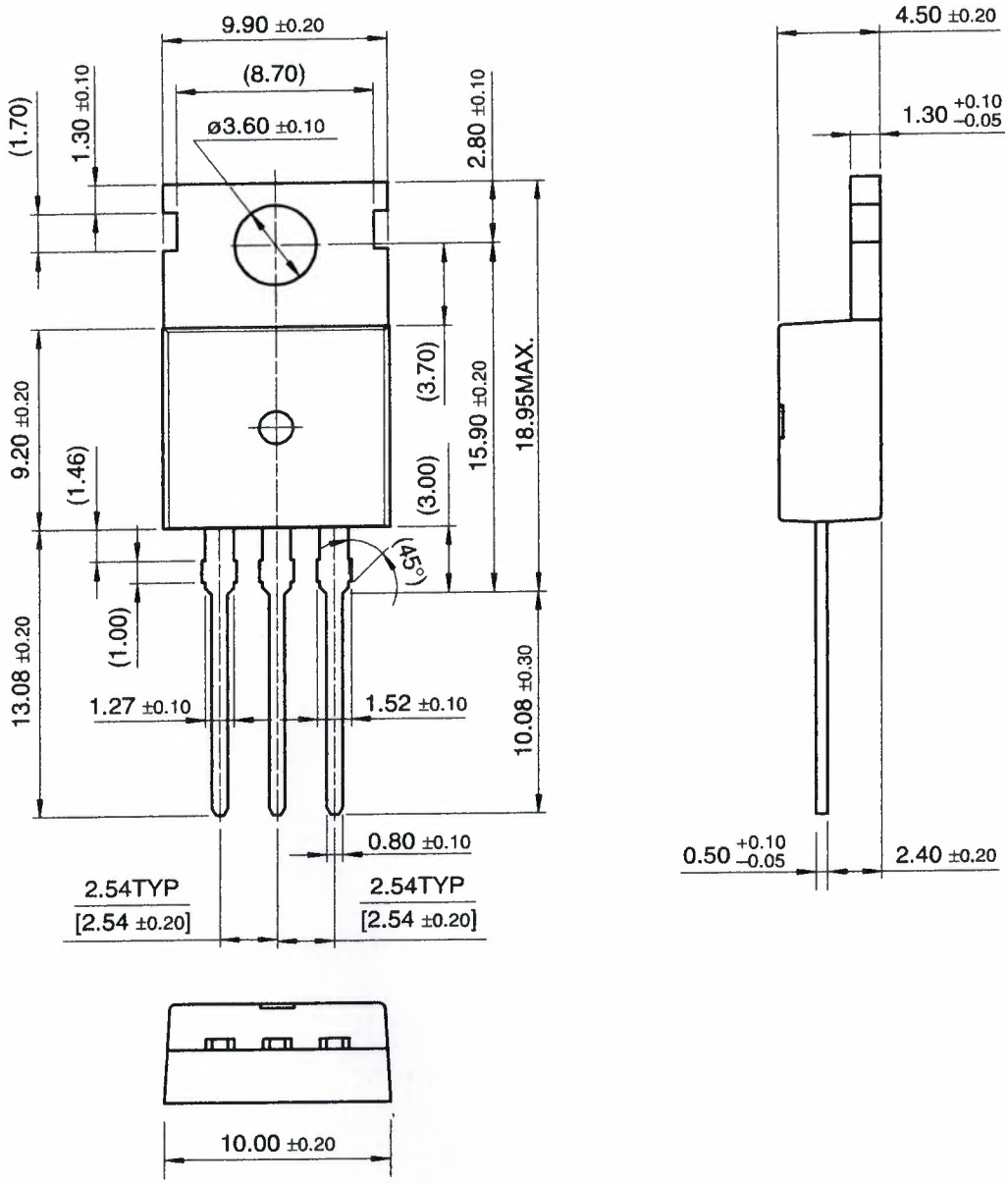


Figure 19. Switching Regulator

Mechanical Dimensions

Dimensions in millimeters

TO-220



Datasheet of KPS2222A

FAIRCHILD
SEMICONDUCTOR®

KSP2222A

General Purpose Transistor

- Collector-Emitter Voltage: V_{CEO}= 40V
- Collector Power Dissipation: P_C (max)=625mW
- Refer KSP2222 for graphs

TO-92

1

1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	75	V
V_{CEO}	Collector-Emitter Voltage	40	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current	600	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

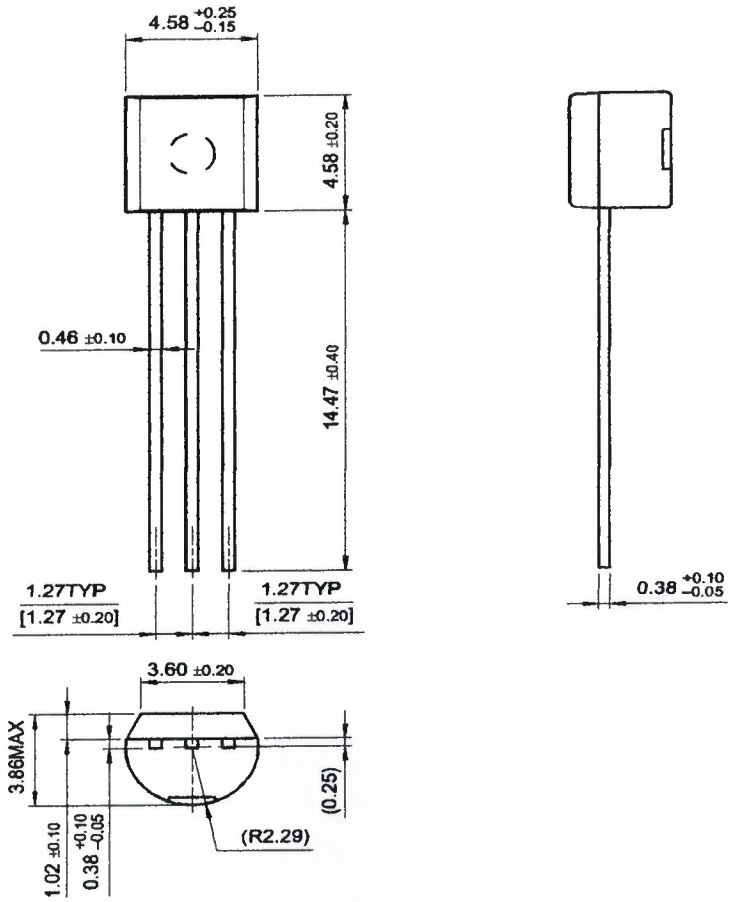
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=10μA, I_E=0	75			V
BV_{CEO}	Collector Emitter Breakdown Voltage	I_C=10mA, I_B=0	40			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=10μA, I_C=0	6			V
I_{CBO}	Collector Cut-off Current	V_{CB}=60V, I_E=0			0.01	μA
I_{EBO}	Emitter Cut-off Current	V_{EB}=3V, I_C=0			10	nA
h_{FE}	DC Current Gain	I_C=0.1mA, V_{CE}=10V V_{CE}=10V, I_C=1mA V_{CE}=10V, I_C=10mA V_{CE}=10V, *I_C=150mA V_{CE}=10V, *I_C=500mA	35 50 75 100 40		 300 	
V_{CE} (sat)	* Collector-Emitter Saturation Voltage	I_C=150mA, I_B=15mA I_C=500mA, I_B=50mA			0.3 1	V V
V_{BE} (sat)	* Base-Emitter Saturation Voltage	I_C=150mA, I_B=15mA I_C=500mA, I_B=50mA		0.6	1.2 2	V V
f_T	Current Gain Bandwidth Product	V_{CE}=20V, I_C=20mA f=100MHz	300			MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz			8	pF
t_{ON}	Turn On Time	V_{CC}=30V, I_C=150mA I_{B1}=15mA, V_{BE}(off)=0.5V			35	ns
t_{OFF}	Turn Off Time	V_{CC}=30V, I_C=150mA I_{B1}=I_{B2}=15mA			285	ns
NF	Noise Figure	I_C=100μA, V_{CE}=10V R_S=1KΩ, f=1KHz			4	dB

* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%
* Also available as and PN2222A

Rev. A1, June 2001

Package Demensions

TO-92



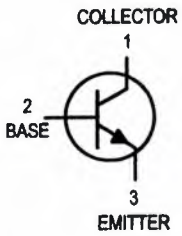
Dimensions in Millimeters

Rev. A1, June 2001

Datasheet of BC547

Amplifier Transistors
NPN Silicon

BC546, B
BC547, A, B, C
BC548, A, B, C



CASE 29–04, STYLE 17
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	BC 546	BC 547	BC 548	Unit
Collector–Emitter Voltage	V_{CEO}	65	45	30	Vdc
Collector–Base Voltage	V_{CBO}	80	50	30	Vdc
Emitter–Base Voltage	V_{EBO}	6.0			Vdc
Collector Current — Continuous	I_C	100			mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12			Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)	BC546 BC547 BC548	$V_{(BR)CEO}$	65 45 30	— — —	— — —	V
Collector–Base Breakdown Voltage (I_C = 100 µAdc)	BC546 BC547 BC548	$V_{(BR)CBO}$	80 50 30	— — —	— — —	V
Emitter–Base Breakdown Voltage (I_E = 10 µA, I_C = 0)	BC546 BC547 BC548	$V_{(BR)EBO}$	6.0 6.0 6.0	— — —	— — —	V
Collector Cutoff Current (V_{CE} = 70 V, V_{BE} = 0) (V_{CE} = 50 V, V_{BE} = 0) (V_{CE} = 35 V, V_{BE} = 0) (V_{CE} = 30 V, T_A = 125°C)	 BC546 BC547 BC548 BC546/547/548	I_{CES}	 — — — —	 0.2 0.2 0.2 —	 15 15 15 4.0	 nA µA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = 10 μA, V_{CE} = 5.0 V)	BC547A/548A		—	90	—	
	BC546B/547B/548B		—	150	—	
	BC548C		—	270	—	
(I_C = 2.0 mA, V_{CE} = 5.0 V)	BC546		110	—	450	
	BC547		110	—	800	
	BC548		110	—	800	
	BC547A/548A		110	180	220	
	BC546B/547B/548B		200	290	450	
	BC547C/BC548C		420	520	800	
(I_C = 100 mA, V_{CE} = 5.0 V)	BC547A/548A		—	120	—	
	BC546B/547B/548B		—	180	—	
	BC548C		—	300	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 10 mA, I_B = 0.5 mA)			—	0.09	0.25	
(I_C = 100 mA, I_B = 5.0 mA)			—	0.2	0.6	
(I_C = 10 mA, I_B = See Note 1)			—	0.3	0.6	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$	—	0.7	—	V
(I_C = 10 mA, I_B = 0.5 mA)						
Base–Emitter On Voltage		$V_{BE(on)}$				V
(I_C = 2.0 mA, V_{CE} = 5.0 V)			0.55	—	0.7	
(I_C = 10 mA, V_{CE} = 5.0 V)			—	—	0.77	
SMALL–SIGNAL CHARACTERISTICS						
Current–Gain — Bandwidth Product		f_T				MHz
(I_C = 10 mA, V_{CE} = 5.0 V, f = 100 MHz)	BC546		150	300	—	
	BC547		150	300	—	
	BC548		150	300	—	
Output Capacitance		C_{obo}	—	1.7	4.5	pF
(V_{CB} = 10 V, I_C = 0, f = 1.0 MHz)						
Input Capacitance		C_{ibo}	—	10	—	pF
(V_{EB} = 0.5 V, I_C = 0, f = 1.0 MHz)						
Small–Signal Current Gain		h_{fe}				—
(I_C = 2.0 mA, V_{CE} = 5.0 V, f = 1.0 kHz)	BC546		125	—	500	
	BC547/548		125	—	900	
	BC547A/548A		125	220	260	
	BC546B/547B/548B		240	330	500	
	BC547C/548C		450	600	900	
Noise Figure		NF				dB
(I_C = 0.2 mA, V_{CE} = 5.0 V, R_S = 2 kΩ,	BC546		—	2.0	10	
f = 1.0 kHz, Δf = 200 Hz)	BC547		—	2.0	10	
	BC548		—	2.0	10	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1.0 V.

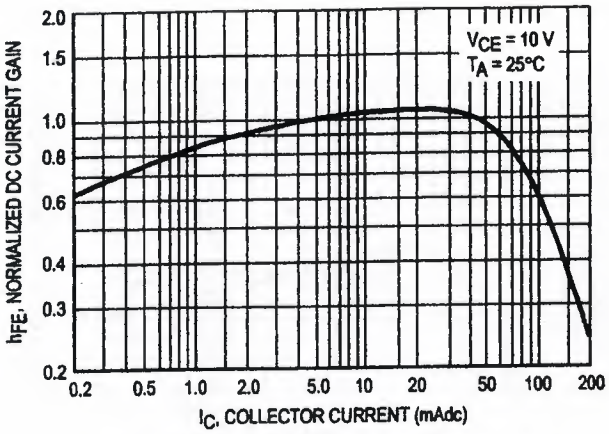


Figure 1. Normalized DC Current Gain

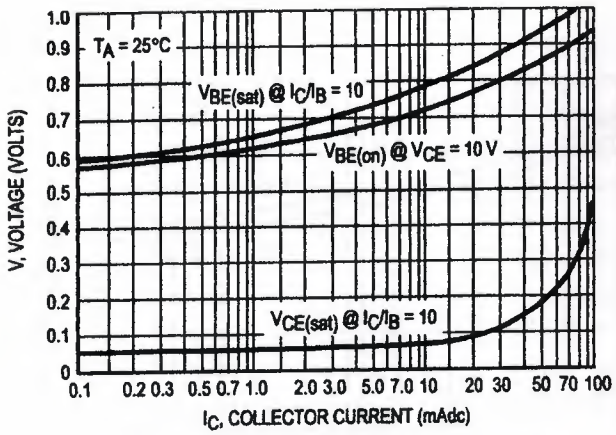


Figure 2. "Saturation" and "On" Voltages

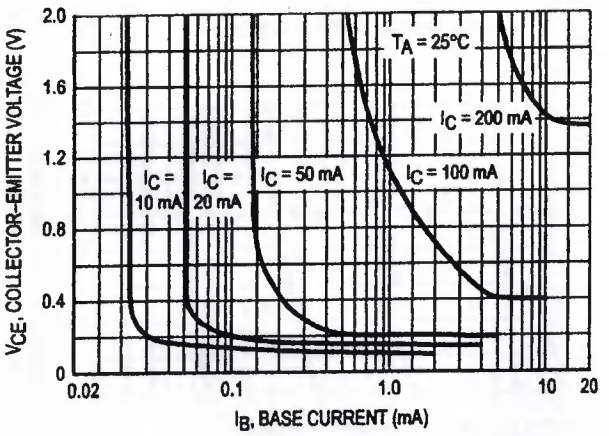


Figure 3. Collector Saturation Region

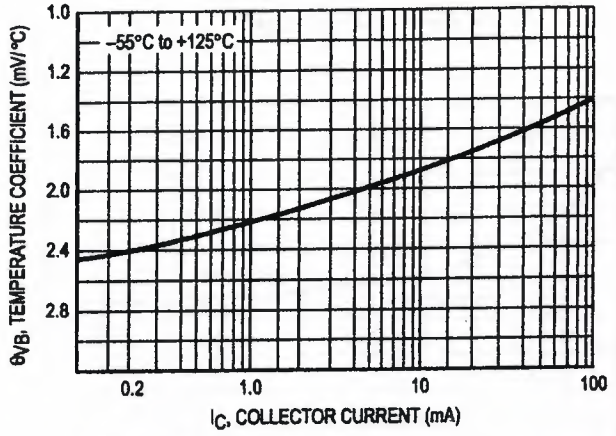


Figure 4. Base–Emitter Temperature Coefficient

BC547/BC548

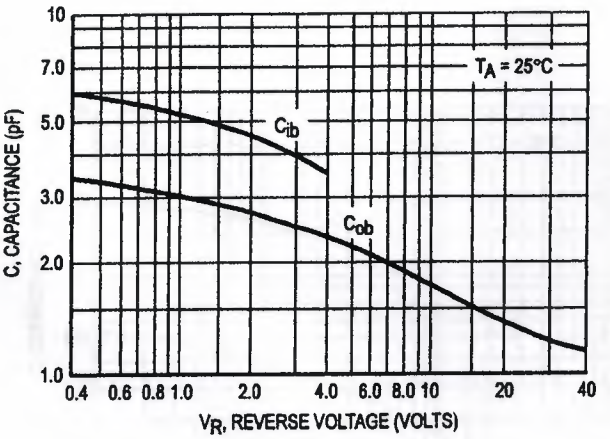


Figure 5. Capacitances

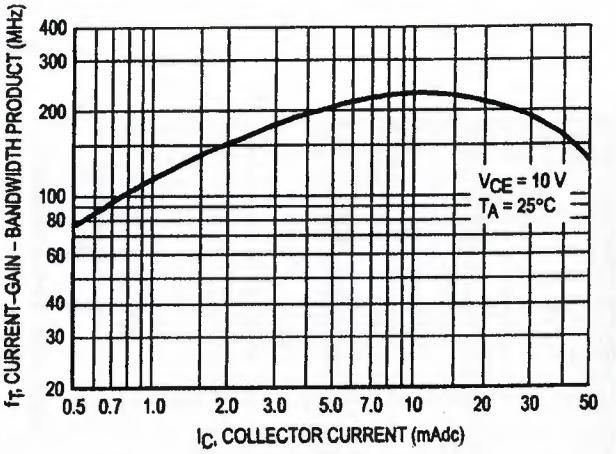


Figure 6. Current–Gain – Bandwidth Product

BC547/BC548

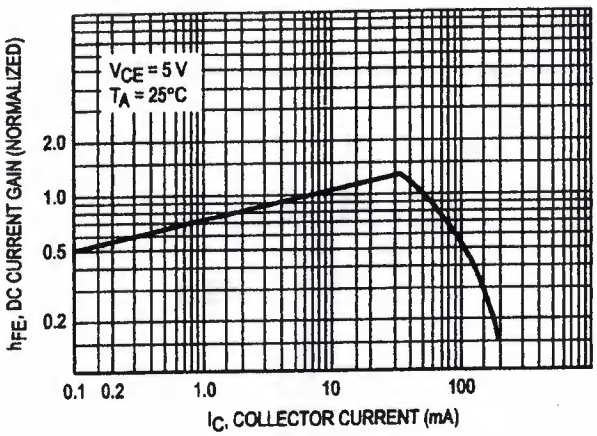


Figure 7. DC Current Gain

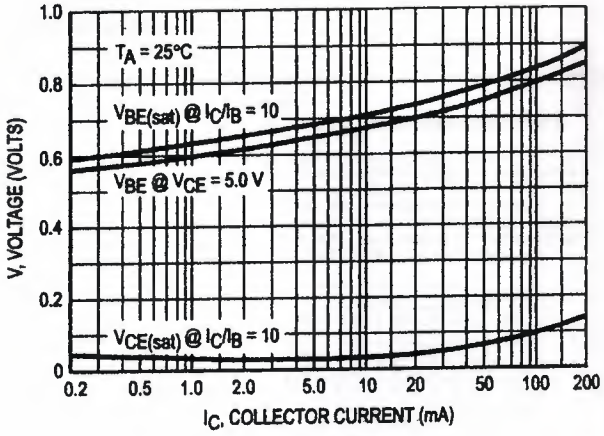


Figure 8. "On" Voltage

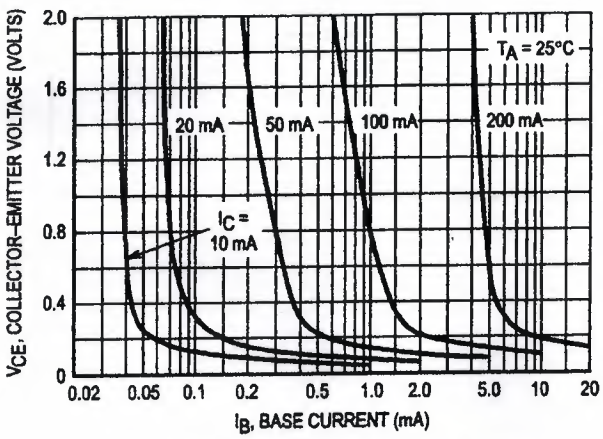


Figure 9. Collector Saturation Region

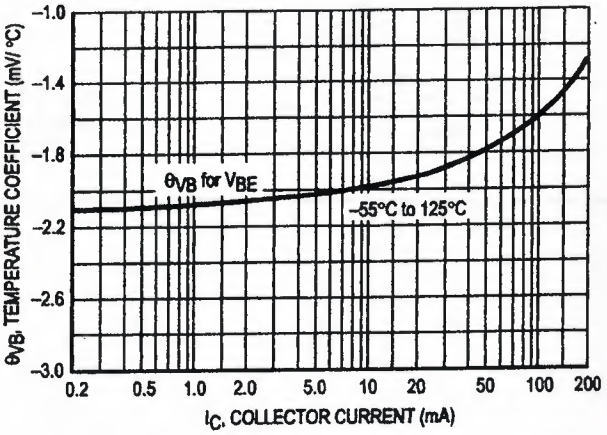


Figure 10. Base–Emitter Temperature Coefficient

BC546

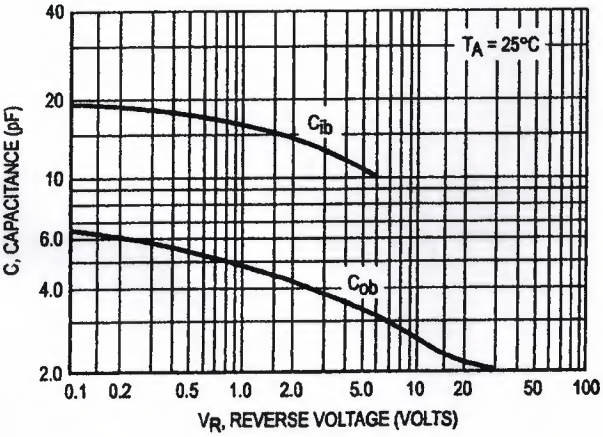


Figure 11. Capacitance

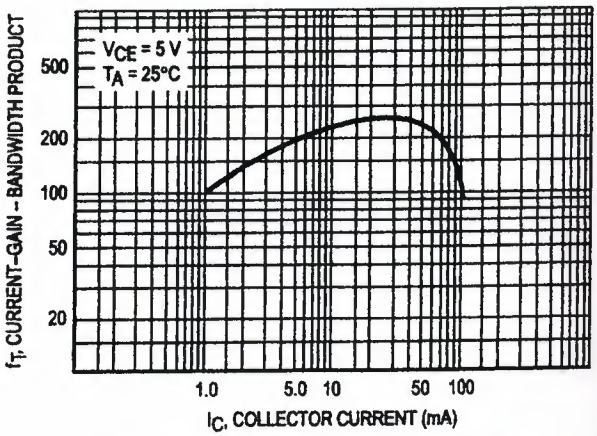
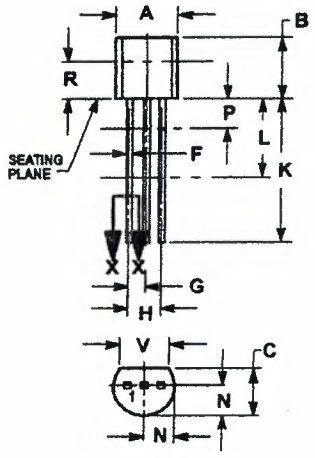
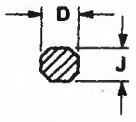


Figure 12. Current–Gain – Bandwidth Product

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER