# NEAR EAST UNIVERSITY

## Faculty of Engineering

## Department of Electrical and Electronic Engineering

# TELEREMOTE CONTROL WITH PLC

**Graduation Project**
**EE – 400**

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# ASTRACT

In this study, a system of teleremote circuit via telephone lines. For building up the system minimum needs are Programmable Logic Controller (PLC), active telephone line, and teleremote control circuit.

The teleremote control circuit enables us to control some appliances: on the other hand the programmable logic controller (PLC) is controlled by teleremote control circuit. Therefore if there is a telephone line the control of the appliances can be any where.

The circuit described here can be used to switch up to nine appliances (corresponding to the digits 1 through 9 of the telephone key-pad). The DTMF signals on the telephone instrument are used as control signals. The digit '0' in DTMF mode is used to toggle between the appliance mode and normal telephone operation mode. Thus the telephone can be used to switch on or switch off the appliances via Programmable Logic Controller (PLC) and driven relays.

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# INTRODUCTION

The rapid developments in electronics have unstopply revolutionized the tele-communication and internet technology in recent years and have become a part of daily life, bringing in everything from Pampers to programmable logic devices. The rising usage of internet has been complemented with developments in communication technology.

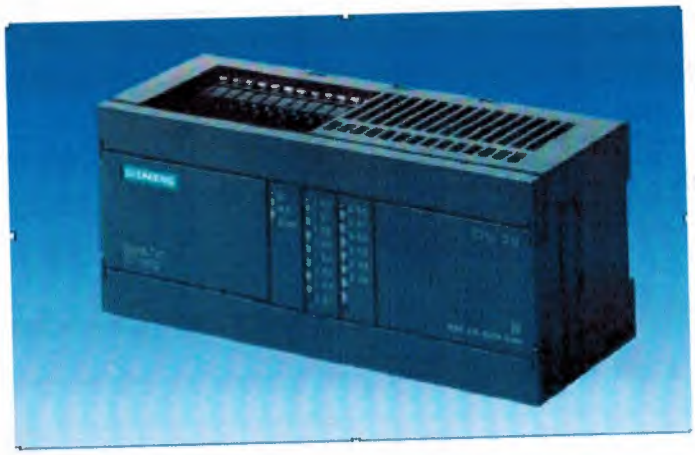


**Figure 1.**Siemens S7 CPU212 PLC

Moreover, Telecommunication technologies start to invade the home to carry phone signals and comfort of telecommunication systems. These rapid developments show that internet based and telecommunication systems have had a huge role in home and business solutions nowadays and will have more in future.

Telecommunication technology allows companies to overcome many of the physical constraints that often prevent them from doing business in distant markets, which means that an a commerce market is fundamentally global (Choi and Whinston.1999).

By using the telephone code of lines are sent to telephone and control the equipment via PLC. Its possible doing the processes wherever you are.

The functional as follows:

- Calling of the destination number then destination number will answer automatically.

- By pressing numbers the control circuit will sent the information received from telephone lines to PLC for performing the processes.

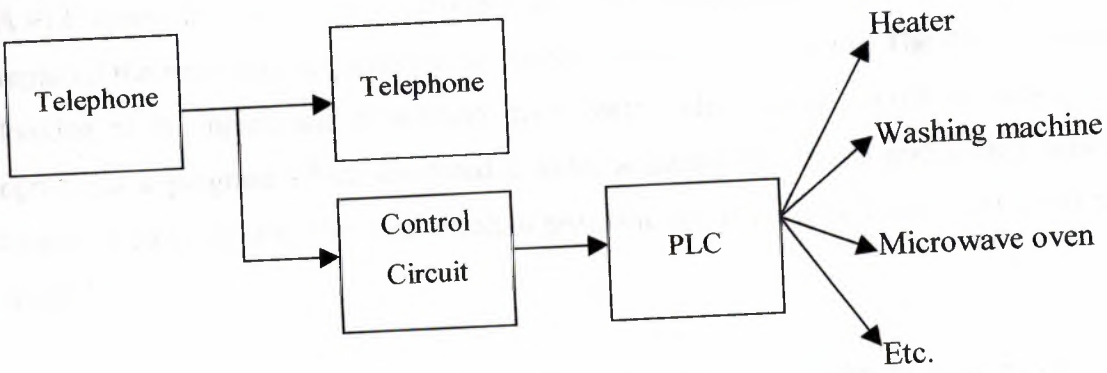



**Figure 2.** Architecture

# 1. INTRODUCING THE PLC

## 1.1 What is PLC ?

A PLC (programmable logic controller) is a small industrial computer which originally replaced the necessary sequential relay circuits for machine control. The PLC works by looking at its inputs and depending upon their state, turning on/off its outputs. It contained a program which executed a loop, scanning the inputs and taking actions based on these inputs. The user enters a program, usually via software, that gives the desired results.

PLCs are used in many "real world" applications. If there is industry present, chances are good that there is a PLC present. If you are involved in machining, packaging, material handling, automated assembly or countless other industries you are probably already using them. If you are not, you are wasting money and time. Almost any application that needs some type of electrical control has a need for a PLC.

A PLC, basically consists of two elements:

I. the central processing unit
II. the input/output system

### *I. The Central Processing Unit*

The central processing unit (CPU) is the part of a programmable controller that retrieves, decodes, stores, and processes information. It also executes the control program stored in the PLC's memory. In essence, the CPU is the "brains" of a programmable controller. It functions much the same way the CPU of a regular computer does, except that it uses special instructions and coding to perform its functions.

The CPU has three parts:

I. the processor
II. the memory system
III. the power supply

The processor is the section of the CPU that codes, decodes, and computes data. The memory system is the section of the CPU that stores both the control program and data from the equipment connected to the PLC. The power supply is the section that provides the PLC with the voltage and current it needs to operate.

### *II. The Input/Output System*

The input/output (I/O) system is the section of a PLC to which all of the field devices are connected. If the CPU can be thought of as the brains of a PLC, then the I/O system can be thought of as the arms and legs. The I/O system is what actually physically carries out the control commands from the program stored in the PLC's memory.
The I/O system consists of two main parts:

I. the rack
II. I/O modules

The rack is an enclosure with slots in it that is connected to the CPU. I/O modules are devices with connection terminals to which the field devices are wired. Together, the rack and the I/O modules form the interface between the field devices and the PLC. When set up properly, Each I/O module is both securely wired to its corresponding field devices and securely installed in a slot in the rack. This creates the physical connection between the field equipment and the PLC. In some small PLC's, the rack and the I/O modules come prepackaged as one unit

## 1.2 Inputs And Outputs

All of the field devices connected to a PLC can be classified in one of two categories:

I. inputs
II. outputs

Inputs are devices that supply a signal/data to a PLC. Typical examples of inputs are push buttons, switches, and measurement de-vices. Basically an input device tells the PLC, "Hey, something's happening out here…you need to check this out to see how it affects the control program.

Outputs are devices that await a signal/data from the PLC to perform their control functions. Lights, horns, motors, and valves are all good examples of output devices. These devices stay put, minding their own business, until the PLC says, "You need to turn on now" or "You'd better open up your valve a little more," etc.

There are two basic types of input and output devices:

I. discrete
II. analog

Discrete devices are inputs and outputs that have only two states: on and off. As a result, they send/receive simple signals to from a PLC. These signals consist of only 1's and 0's. A 1 means that the device is on and a 0 means that the device is off.

Analog devices are inputs and outputs that can have an infinite number of states. These devices can not only be on and off, but they can also be barely on, almost totally on, not quite off, etc. These devices send receive complex signals to from a PLC. Their communications consist of a variety of signals, not just 1's and 0's. Because different input and output devices send different kinds of signals, they sometimes have a hard time communicating with the PLC. While PLC's are powerful devices, they can't always speak the "language" of every device connected to them. That's where the I/O modules we talked about earlier come in. The modules act as "translators" between the field devices and the PLC. They ensure that the PLC and the field devices all get the information they need in a language that they can understand.

### *1.3 Control Programs*

We talked a little bit earlier about the control program. The control program is a software program in the PLC's memory. It's what puts the control in a programmable controller. The user or the system designer is usually the one who develops the control program. The control program is made up of things called instructions. Instructions are, in essence, little computer codes that make the inputs and outputs do what you want in order to get the result you need. There are all different kinds of instructions and they can make a PLC do just about anything (add and subtract data, time and count events,

compare information, etc.). All you have to do is program the instructions in the proper order and make sure that they are telling the right devices what to do and voila!...you have a PLC-controlled system. And remember, changing the system is a snap. If you want the system to act differently, just change the instructions in the control program. Different PLC's offer different kinds of instructions. That's part of what makes each type of PLC unique.

However, all PLCs use two basic types of instructions:

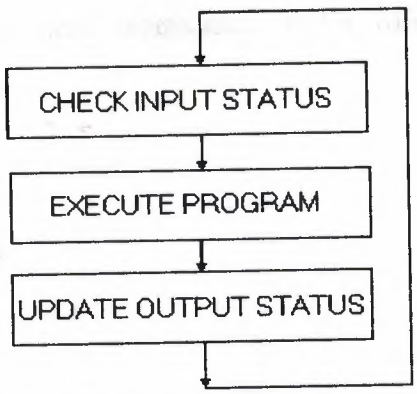
I. contacts
II. coils

Contacts are instructions that refer to the input conditions to the control program that is, to the information supplied by the input field devices. Each contact in the control program monitors a certain field device. The contact waits for the input to do something in particular (e.g., turn on, turn off, etc. this all depends on what type of contact it is). Then, the contact tells the PLC's control program, "The input device just did what it's supposed to do. You'd better check to see if this is supposed to affect any of the output devices."

Coils are instructions that refer to the outputs of the control program that is, to what each particular output device is supposed to do in the system. Like a contact, each coil also monitors a certain field device. However, unlike a contact, which monitors the field device and then tells the PLC what to do, a coil monitors the PLC control program and then tells the field device what to do. It tells the output device, "Hey, the PLC just told me that the switch turned on. That means that you're supposed to turn on now. So let's go!" In PLC talk, this three-step process of monitoring the inputs, executing the PLC control program, and changing the status of the

### 1.4 How PLC Work?

A PLC works by continually scanning a program. We can think of this scan cycle as consisting of 3 important steps. There are typically more than 3 but we can focus on the important parts and not worry about the others. Typically the others are checking the system and updating the current internal counter and timer values.




Step 1-CHECK INPUT STATUS-First the PLC takes a look at each input to determine if it is on or off. In other words, is the sensor connected to the first input on? How about the second input? How about the third... It records this data into its memory to be used during the next step.

Step 2-EXECUTE PROGRAM-Next the PLC executes your program one in struction at a time. Maybe your program said that if the first input was on then it should turn on the first output. Since it already knows which inputs are on/off from the previous step it will be able to decide whether the first output should be turned on based on the state of the first input. It will store the execution results for use later during the next step.

Step 3-UPDATE OUTPUT STATUS-Finally the PLC updates the status of the outputs. It updates the outputs based on which inputs were on during the first step and the results of executing your program during the second step.

### *1.5 Why Use PLC's ?*

The software advantage provided by programmable controllers is tremendous. In fact, it is one of the most important features of PLCs. Software makes changes in the control system easy and cheap. If you want a device in a PLC system to behave differently or to control a different process element, all you have to do is change the control program. In a traditional system, making this type of change would involve physically changing the wiring between the devices, a costly and time-consuming endeavor. In addition to the

programming flexibility we just mentioned, PLCs offer other advantages over traditional control systems.

These advantages include:

- high reliability
- small space requirements
- computing capabilities
- reduced costs
- ability to withstand harsh environments
- expandability

### 1.6 Capabilities of the S7-212 CPUs

The S7-200 family includes a wide variety of CPUs. This variety provides a range of features to aid in designing a cost-effective automation solution. Table 2 provides a summary of the major features of each S7-212 CPU.

## Table 2

## CPU 212 DC power supply, DC inputs, DC outputs

**Order Number: 6ES7 212–1AA01–0XB0**

| General Features | |
|---|---|
| Physical size (L x W x D) | 160 x 80 x 62 mm (6.3 x 3.15 x 2.44 in.) |
| Weight | 0.3 kg (0.7 lbs.) |
| Power dissipation | 5 W at 1.75 A load |
| User program size/storage | 512 words/EEPROM |
| User data size/storage<br>Data retention | 512 words/RAM<br>50 hr typical<br>(8 hr minimum at 40° C) |
| Local I/O[1] | 8 inputs/6 outputs |
| Maximum number of expansion modules | 2 |
| Digital I/O supported | 64 inputs/64 outputs |
| Analog I/O supported | 16 inputs/16 outputs |
| Boolean execution speed | 1.2 µs/instruction |
| Internal memory bits | 128 |
| Timers | 64 timers |
| Counters | 64 counters |
| High-speed counters | 1 software (2 KHz max.) |
| Analog adjustments | 1 |
| Standards compliance | UL 508 CSA C22.2 142<br>FM Class I, Division 2<br>VDE 0160 compliant<br>CE compliant |

| Output Points | | |
|---|---|---|
| Output type | Sourcing transistor | |
| Voltage range | 20.4 VDC to 28.8 VDC | |
| Maximum load current | 0 to 40° C | 55° C[2] |
| Per single point | 0.75 A | 0.50 A |
| Per 2 adjacent points | 1.00 A | 0.75 A |
| All points total | 2.25 A | 1.75 A |
| Inductive load clamping | (per common) | |
| Single pulse | 2A L/R = 10 ms<br>1A L/R = 100 ms | |
| Repetitive | 1 W energy dissipation<br>(1/2 LI$^2$ x switch rate < 1 W) | |
| Leakage current | 100 µA | |

| Output Points (continued) | |
|---|---|
| Switching delay | 25 µs ON, 120 µs OFF |
| Surge current | 4 A, 100 ms |
| Voltage drop | 1.8 V maximum at maximum current |
| Optical isolation | 500 VAC, 1 min |
| Short circuit protection | None |

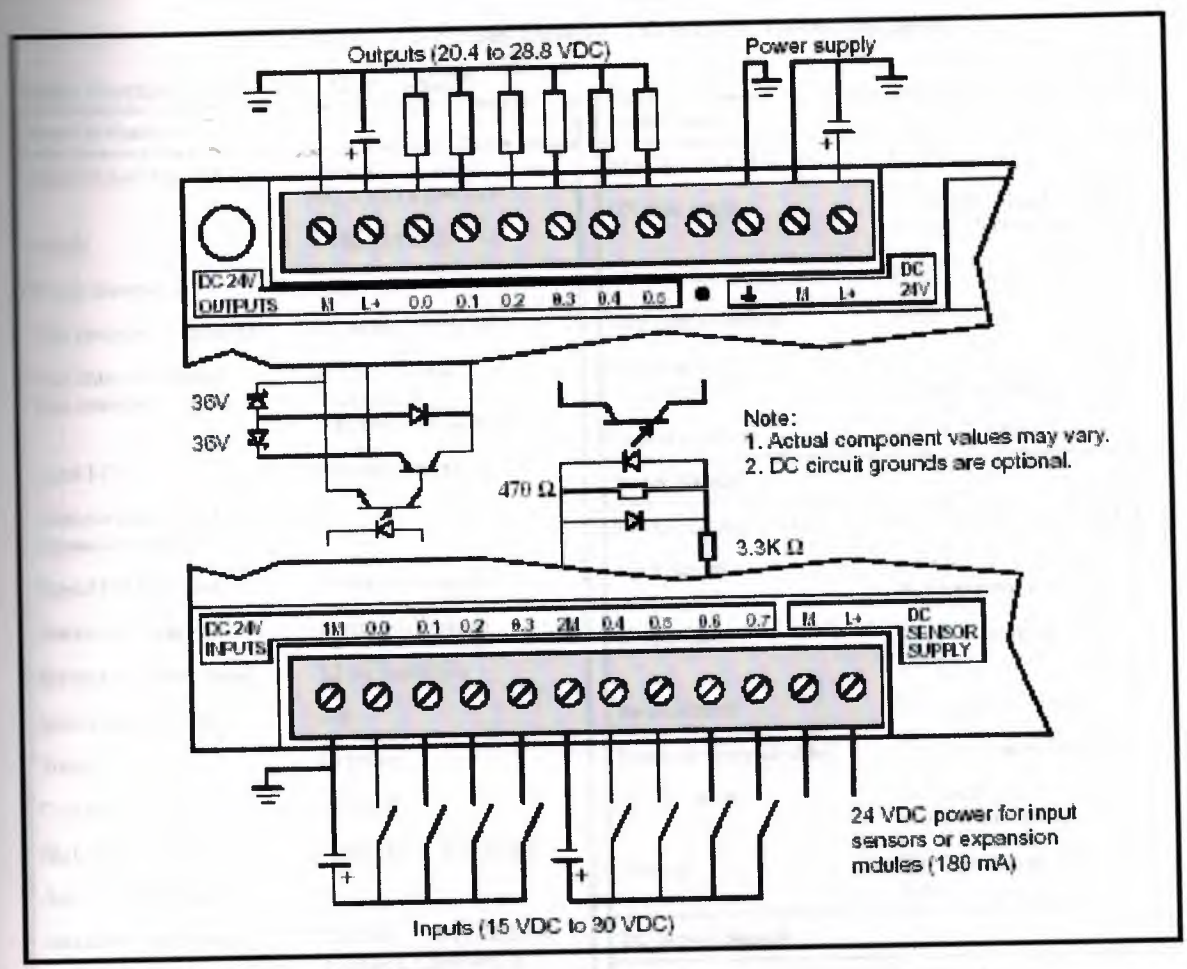
| Input Points | |
|---|---|
| Input type (IEC 1131–2) | Type 1 sinking |
| ON state range | 15–30 VDC, 4 mA minimum<br>35 VDC, 500 ms surge |
| ON state nominal | 24 VDC, 7 mA |
| OFF state maximum | 5 VDC, 1 mA |
| Response time<br>I0.0 to I0.7 | <br>0.3 ms maximum |
| Optical isolation | 500 VAC, 1 min |

| Power Supply | |
|---|---|
| Voltage range | 20.4 to 28.8 VDC |
| Input current | 60 mA typical, CPU only<br>500 mA maximum load |
| UL/CSA rating | 50 VA |
| Holdup time | 10 ms minimum from 24 VDC |
| Inrush current | 10 A peak at 28.8 VDC |
| Fusing (non-replaceable) | 1 A, 125 V, slow blow |
| 5 VDC current | 260 mA for CPU<br>340 mA for expansion I/O |
| Isolated | No |

| DC Sensor Supply | |
|---|---|
| Voltage range | 16.4 to 28.8 VDC |
| Ripple/noise (< 10MHz) | Same as supplied voltage |
| 24 VDC available current<br>Short-circuit current limit | 180 mA<br>< 600 mA |
| Isolated | No |

1 The CPU reserves 8 process-image input and 8 process-image output image register points for local I/O.

2 Linear derate 40 to 55° C. Vertical mount derate 10° C.




**Connector Terminal Identification for CPU 212 DC/DC/DC**

## CPU 212 AC Power Supply, DC Inputs, Relay Outputs

**Order Number: 6ES7 212–1BA01–0XB0**

| General Features | |
|---|---|
| Physical size (L x W x D) | 160 x 80 x 62 mm<br>(6.3 x 3.15 x 2.44 in.) |
| Weight | 0.4 kg (0.9 lbs.) |
| Power dissipation | 6 W |
| User program size/storage | 512 words/EEPROM |
| User data size/storage<br>Data retention | 512 words/RAM<br>50 hr typical<br>(8 hr minimum at 40° C) |
| Local I/O[1] | 8 inputs/6 outputs |
| Maximum number of expansion modules | 2 |
| Digital I/O supported | 64 inputs/64 outputs |
| Analog I/O supported | 16 inputs/16 outputs |
| Boolean execution speed | 1.2 µs/instruction |
| Internal memory bits | 128 |
| Timers | 64 timers |
| Counters | 64 counters |
| High-speed counters | 1 software (2 KHz max.) |
| Analog adjustments | 1 |
| Standards compliance | UL 508 CSA C22.2 142<br>FM Class I, Division 2<br>VDE 0160 compliant<br>CE compliant |

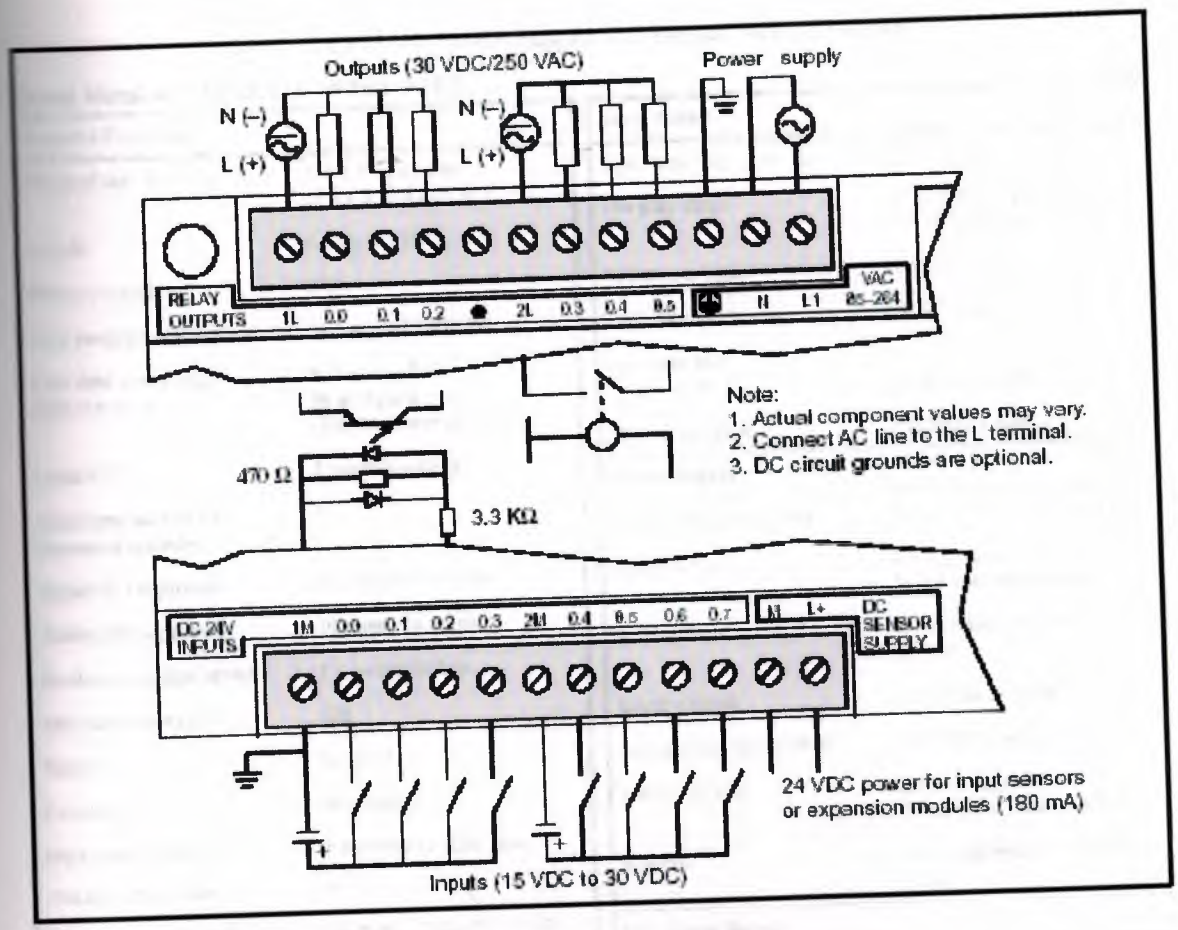
| Output Points | |
|---|---|
| Output type | Relay, dry contact |
| Voltage range | 5 to 30 VDC/250 VAC |
| Maximum load current | 2 A/point, 6 A/common |
| Overcurrent surge | 7 A with contacts closed |
| Isolation resistance | 100 MΩ minimum (new) |
| Switching delay | 10 ms maximum |
| Lifetime | 10,000,000 mechanical<br>100,000 with rated load |
| Contact resistance | 200 mΩ maximum (new) |
| Isolation<br>coil to contact<br>contact to contact<br>(between open contacts) | <br>1500 VAC, 1 min<br>750 VAC, 1 min |
| Short circuit protection | None |

| Input Points | |
|---|---|
| Input type (IEC 1131–2) | Type 1 sinking |
| ON state range | 15–30 VDC, 4 mA minimum<br>35 VDC, 500 ms surge |
| ON state nominal | 24 VDC, 7 mA |
| OFF state maximum | 5 VDC, 1 mA |
| Response time<br>10.0 to 10.7 | <br>0.3 ms maximum |
| Optical isolation | 500 VAC, 1 min |

| Power Supply | |
|---|---|
| Voltage/frequency range | 85 to 264 VAC at 47 to 63 Hz |
| Input current | 4 VA typical, CPU only<br>50 VA maximum load |
| Holdup time | 20 ms minimum from<br>110 VAC |
| Inrush current | 20 A peak at 264 VAC |
| Fusing (non-replaceable) | 2 A, 250 V, slow blow |
| 5 VDC current | 260 mA for CPU<br>340 mA for expansion I/O |
| Isolated | Yes, Transformer, 1500 VAC,<br>1 min |

| DC Sensor Supply | |
|---|---|
| Voltage range | 20.4 to 28.8 VDC |
| Ripple/noise (< 10MHz) | 1 V peak-to-peak maximum |
| 24 VDC available current<br>Short circuit current limit | 180 mA<br>< 600 mA |
| Isolated | No |

1 The CPU reserves 8 process-image input and 8 process-image output image register points for local I/O.




**Connector Terminal Identification for CPU 212 AC/DC/Relay**

## 24 VAC CPU 212 Power Supply, DC Inputs, Relay Outputs

**Order Number: 6ES7 212–1FA01–0XB0**

| General Features | |
|---|---|
| Physical size (L x W x D) | 160 x 80 x 62 mm (6.3 x 3.15 x 2.44 in.) |
| Weight | 0.4 kg (0.9 lbs.) |
| Power dissipation | 6 W |
| User program size/storage | 512 words/EEPROM |
| User data size/storage<br>Data retention | 512 words/RAM<br>50 hr typical<br>(8 hr minimum at 40° C) |
| Local I/O[1] | 8 inputs/6 outputs |
| Maximum number of expansion modules | 2 |
| Digital I/O supported | 64 inputs/64 outputs |
| Analog I/O supported | 16 inputs/16 outputs |
| Boolean execution speed | 1.2 µs/instruction |
| Internal memory bits | 128 |
| Timers | 64 timers |
| Counters | 64 counters |
| High-speed counters | 1 software (2 KHz max.) |
| Analog adjustments | 1 |
| Standards compliance | UL 508 CSA C22.2 142<br>FM Class I, Division 2<br>VDE 0160 compliant<br>CE compliant |

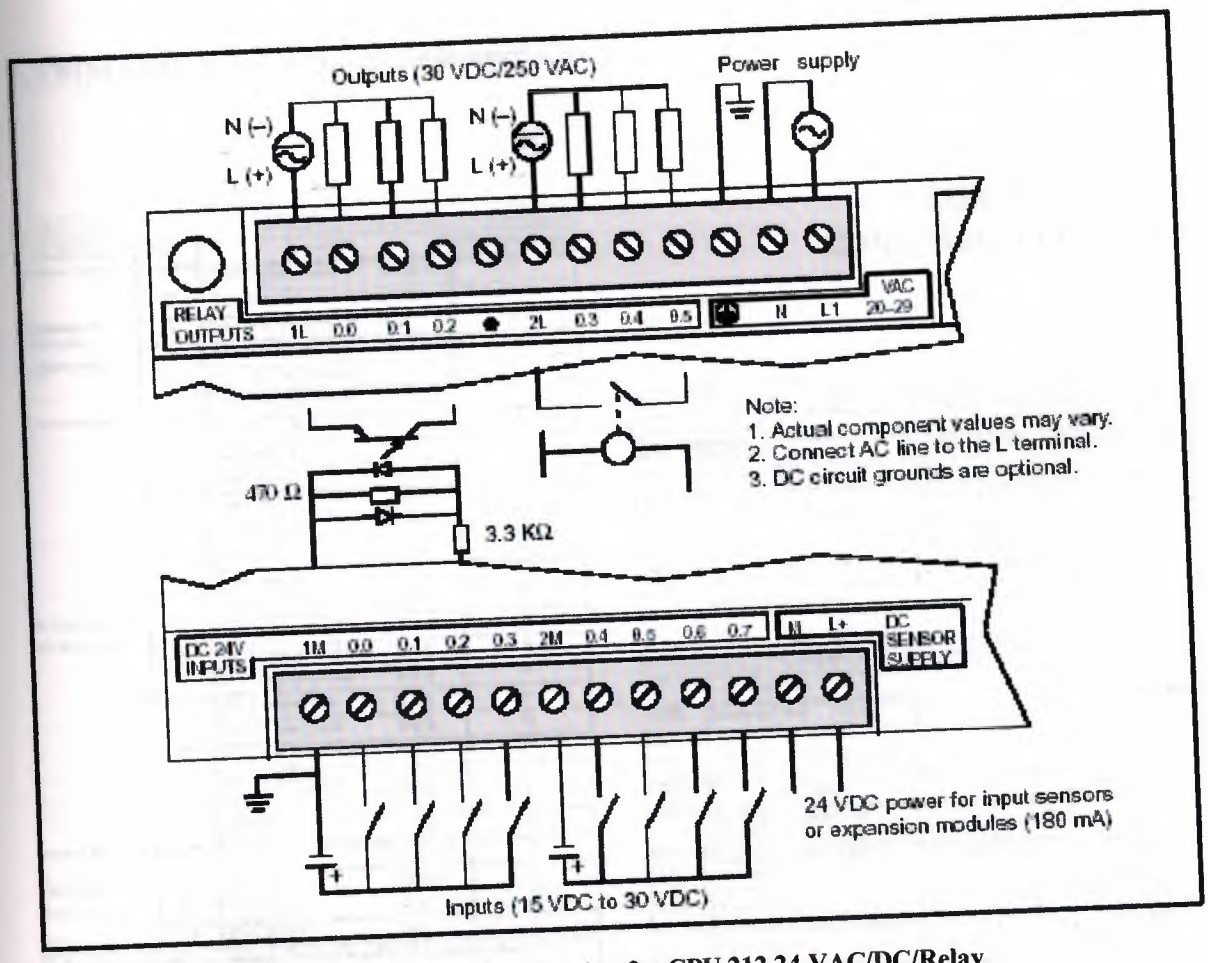
| Output Points | |
|---|---|
| Output type | Relay, dry contact |
| Voltage range | 5 to 30 VDC/250 VAC |
| Maximum load current | 2 A /point, 6 A /common |
| Overcurrent surge | 7 A with contacts closed |
| Isolation resistance | 100 MΩ minimum (new) |
| Switching delay | 10 ms maximum |
| Lifetime | 10,000,000 mechanical<br>100,000 with rated load |
| Contact resistance | 200 mΩ maximum (new) |
| Isolation<br>coil to contact<br>contact to contact<br>(between open contacts) | <br>1500 VAC, 1 min<br>750 VAC, 1 min |
| Short circuit protection | None |

| Input Points | |
|---|---|
| Input type (IEC 1131–2) | Type 1 sinking |
| ON state range | 15–30 VDC, 4 mA minimum<br>35 VDC, 500 ms surge |
| ON state nominal | 24 VDC, 7 mA |
| OFF state maximum | 5 VDC, 1 mA |
| Response time<br>I0.0 to I0.7 | <br>0.3 ms maximum |
| Optical isolation | 500 VAC, 1 min |

| Power Supply | |
|---|---|
| Voltage/frequency range | 20 to 29 VAC at 47 to 63 Hz |
| Input current | 4 VA typical, CPU only<br>50 VA maximum load |
| Holdup time | 20 ms minimum from 24 VAC |
| Inrush current | 20 A peak at 29 VAC |
| Fusing (non-replaceable) | 2 A, 250 V, slow blow |
| 5 VDC current | 260 mA for CPU<br>340 mA for expansion I/O |
| Isolated | Yes, Transformer, 500 VAC, 1 min |

| DC Sensor Supply | |
|---|---|
| Voltage range | 20.4 to 28.8 VDC |
| Ripple/noise (< 10MHz) | 1 V peak-to-peak maximum |
| 24 VDC available current<br>Short circuit current limit | 180 mA<br>< 600 mA |
| Isolated | No |

1 The CPU reserves 8 process-image input and 8 process-image output image register points for local I/O.




**Connector Terminal Identification for CPU 212 24 VAC/DC/Relay**

# SIMATIC S7-200
# Quick Reference Card

| Interrupts | | | |
|---|---|---|---|
| Priority Group | Event | Description | Priority in Group |
| Communication interrupts (highest priority) | 8 | Port 0: Receive character | 0 |
| | 9 | Port 0: Transmit | 0 |
| | 23 | Port 0: Receive message | 0 |
| | 24 | Port 1: Receive message | 1 |
| | 25 | Port 1: Receive character | 1 |
| | 26 | Port 1: Transmit complete | 1 |
| I/O interrupt: Middle priority | 0 | Rising edge, I0.0* | 0 |
| | 2 | Rising edge, I0.1 | 1 |
| | 4 | Rising edge, I0.2 | 2 |
| | 6 | Rising edge, I0.3 | 3 |
| | 1 | Falling edge, I0.0* | 4 |
| | 3 | Falling edge, I0.1 | 5 |
| | 5 | Falling edge, I0.2 | 6 |
| | 7 | Falling edge, I0.3 | 7 |
| | 12 | HSC0 = preset value* | 0 |
| | 13 | HSC1 = preset value | 8 |
| | 14 | HSC1 direction change | 9 |
| | 15 | HSC1 external reset | 10 |
| | 16 | HSC2 = preset value | 11 |
| | 17 | HSC2 direction change | 12 |
| | 18 | HSC2 external reset | 13 |
| | 19 | PLS0 | 14 |
| | 20 | PLS1 | 15 |
| Timed interrupts: Lowest priority | 10 | Timed 0 | 0 |
| | 11 | Timed 1 | 1 |
| | 21 | T32 = preset | 2 |
| | 22 | T96 = preset | 3 |

* If event 12 is attached to an interrupt, then event 0 and event 1 cannot be attached to interrupts.

CPU 212 CPU 214 CPU 215 CPU 216

| Special Memory Bits | | | |
|---|---|---|---|
| SM0.0 | Always On | SM1.0 | Result of operation = 0 |
| SM0.1 | First Scan | SM1.1 | Overflow or illegal value |
| SM0.2 | Retentive data loss | SM1.2 | Negative result |
| SM0.3 | Power up | SM1.3 | Division by 0 |
| SM0.4 | 30 s off / 30 s on | SM1.4 | Table full |
| SM0.5 | 0.5 s off / 0.5 s on | SM1.5 | Table empty |
| SM0.6 | Off 1 scan / on 1 scan | SM1.6 | BCD to binary conversion error |
| SM0.7 | Switch in RUN position | SM1.7 | ASCII to hex conversion error |

| High-Speed Counter Modes | | | | | |
|---|---|---|---|---|---|
| Counter | | Inputs | | | |
| HSC0 | Maximum 2 kHz | I0.0 | | | |
| HSC1 | 7 kHz 20 kHz | I0.6 | I0.7 | I1.0 | I1.1 |
| HSC2 | 7 kHz 20 kHz | I1.2 | I1.3 | I1.4 | I1.5 |
| Mode | Description | Clock | | Reset | Start |
| 0 to 2 | Single phase with internal direction | Up/Down: 0, 1, 2 | | 1, 2 | 2 |
| 3 to 5 | Single phase with external direction | Up/Down: 3, 4, 5 | Direction: 3, 4, 5 | 4, 5 | 5 |
| 6 to 8 | Two phase | Up: 6, 7, 8 | Down: 6, 7, 8 | 7, 8 | 8 |
| 9 to 11 | Quadrature A/B | A: 9, 10, 11 | B: 9, 10, 11 | 10, 11 | 11 |

CPU 212 CPU 214 CPU 215 CPU 216

| Description | Range Limit | | | | Accessible as... | | | |
|---|---|---|---|---|---|---|---|---|
| | 212 | 214 | 215 | 216 | Bit | Byte | Word | DWord |
| User Program Size | 512 W | 2048 W | 4096 W | 4096 W | | | | |
| User Data Size | 512 W | 2048 W | 2560 W | 2560 W | | | | |
| Variable memory | 0-1023 | 0-4095 | 0-5119 | 0-5119 | Vx.y | VBx | VWx | VDx |
| Input Image Register | 0.7 | 0.7 | 0.7 | 0.7 | Ix.y | IBx | IWx | IDx |
| Output Image Register | 0.7 | 0.7 | 0.7 | 0.7 | Qx.y | QBx | QWx | QDx |
| Analog Inputs | 0-30 | 0-30 | 0-30 | 0-30 | | | AIWx | |
| Analog Outputs | 0-30 | 0-30 | 0-30 | 0-30 | | | AQWx | |
| Bit Memory | 0-15 | 0-31 | 0-31 | 0-31 | Mx.y | MBx | MWx | MDx |
| Special Memory | 0-85 | 0-85 | 0-194 | 0-194 | SMx.y | SMBx | SMWx | SMDx |
| Retentive Timers 1 ms | 0 | 0,64 | 0,64 | 0,64 | Tx | | Tx | |
| Retentive Timers 10 ms | 1-4 | 1-4, 65-68 | 1-4, 65-68 | 1-4, 65-68 | Tx | | Tx | |
| Retentive Timers 100 ms | 5-31 | 5-31, 69-95 | 5-31, 69-95 | 5-31, 69-95 | Tx | | Tx | |
| On Delay Timers 1 ms | 32 | 32, 96 | 32, 96 | 32, 96 | Tx | | Tx | |
| On Delay Timers 10 ms | 33-36 | 33-36, 97-100 | 33-36, 97-100 | 33-36, 97-100 | Tx | | Tx | |
| On Delay Timers 100 ms | 37-63 | 37-63, 101-127 | 37-63, 101-255 | 37-63, 101-255 | Tx | | Tx | |
| Counters | 0-63 | 0-127 | 0-255 | 0-255 | Cx | | Cx | |
| High Speed Counter | 0 | 0-2 | 0-2 | 0-2 | | | | HCx |
| Accumulators | 0-3 | 0-3 | 0-3 | 0-3 | | ACx | ACx | ACx |
| Sequence Control Relay (SCR) | 0-7 | 0-15 | 0-31 | 0-31 | Sx.y | SBx | SWx | SDx |
| Jumps/Labels | 0-63 | 0-255 | 0-255 | 0-255 | | | | |
| Call Subroutine | 0-15 | 0-63 | 0-63 | 0-63 | | | | |
| Interrupt Routines | 0-31 | 0-127 | 0-127 | 0-127 | | | | |
| Interrupt Events | 0,1,8-10, 12 | 0-23 | 0-23 | 0-26 | | | | |
| PID Loops | N/A | N/A | 0-7 | 0-7 | | | | |
| Ports | Port 0 | Port 0 | Port 0, DP Port | Port 0, Port 1 | | | | |

## Boolean Instructions

| | | |
|---|---|---|
| LD | N | Load |
| LDI | N | Load Immediate |
| LDN | N | Load Not |
| LDNI | N | Load Not Immediate |
| A | N | AND |
| AI | N | AND Immediate |
| AN | N | AND Not |
| ANI | N | AND Not Immediate |
| O | N | OR |
| OI | N | OR Immediate |
| ON | N | OR Not |
| ONI | N | OR Not Immediate |
| LDB= | N1, N2 | Load result of Byte Compare N1 (=, >=, or <=) N2 |
| LDB> | N1, N2 | |
| LDB< | N1, N2 | |
| AB= | N1, N2 | AND result of Byte Compare N1 (=, >=, or <=) N2 |
| AB> | N1, N2 | |
| AB< | N1, N2 | |
| OB= | N1, N2 | OR result of Byte Compare N1 (=, >=, or <=) N2 |
| OB> | N1, N2 | |
| OB< | N1, N2 | |
| LDW= | N1, N2 | Load result of Word Compare N1 (=, >=, or <=) N2 |
| LDW> | N1, N2 | |
| LDW< | N1, N2 | |
| AW= | N1, N2 | AND result of Word Compare N1 (=, >=, or <=) N2 |
| AW> | N1, N2 | |
| AW< | N1, N2 | |
| OW= | N1, N2 | OR result of Word Compare N1 (=, >=, or <=) N2 |
| OW> | N1, N2 | |
| OW< | N1, N2 | |
| LDD= | N1, N2 | Load result of DWord Compare N1 (=, >=, or <=) N2 |
| LDD> | N1, N2 | |
| LDD< | N1, N2 | |
| AD= | N1, N2 | AND result of DWord Compare N1 (=, >=, or <=) N2 |
| AD> | N1, N2 | |
| AD< | N1, N2 | |
| OD= | N1, N2 | OR result of DWord Compare N1 (=, >=, or <=) N2 |
| OD> | N1, N2 | |
| OD< | N1, N2 | |
| LDR= | N1, N2 | Load result of Real Compare N1 (=, >=, or <=) N2 |
| LDR> | N1, N2 | |
| LDR< | N1, N2 | |
| AR= | N1, N2 | AND result of Real Compare N1 (=, >=, or <=) N2 |
| AR> | N1, N2 | |
| AR< | N1, N2 | |
| OR= | N1, N2 | OR result of Real Compare N1 (=, >=, or <=) N2 |
| OR> | N1, N2 | |
| OR< | N1, N2 | |
| NOT | | Stack Negation |
| EU | | Detection of Rising Edge |
| ED | | Detection of Falling Edge |
| = | N | Assign Value |
| =I | N | Assign Value Immediate |
| S | S_BIT, N | Set bit Range |
| R | S_BIT, N | Reset bit Range |
| SI | S_BIT, N | Set bit Range Immediate |
| RI | S_BIT, N | Reset bit Range Immediate |

## Math, Increment, and Decrement instructions

| | | |
|---|---|---|
| +I | IN1, OUT | Add Integer, DWord or Real IN1+OUT=OUT |
| +D | IN1, OUT | |
| +R | IN1, OUT | |
| -I | IN1, OUT | Subtract Integer, DWord, or Real OUT-IN1=OUT |
| -D | IN1, OUT | |
| -R | IN1, OUT | |
| MUL | IN1, OUT | Multiply Integer or Real IN1 * OUT = OUT |
| *R | IN1, OUT | |
| DIV | IN1, OUT | Divide Integer or Real OUT / IN1 = OUT |
| /R | IN1, OUT | |
| SQRT | IN, OUT | Square Root |
| INCB | OUT | Increment Byte, Word or DWord |
| INCW | OUT | |
| INCD | OUT | |
| DECB | OUT | Decrement Byte, Word, or DWord |
| DECW | OUT | |
| DECD | OUT | |
| PID | Table, Loop | PID Loop |

## Timer and Counter Instructions

| | | |
|---|---|---|
| TON | Txxx, PT | On Delay Timer |
| TONR | Txxx, PT | Retentive On Delay Timer |
| CTU | Cxxx, PV | Count Up |
| CTUD | Cxxx, PV | Count Up/Down |

## Real Time Clock Instructions

| | | |
|---|---|---|
| TODR | T | Read Time of Day clock |
| TODW | T | Write Time of Day clock |

## Program Control Instructions

| | | |
|---|---|---|
| END | | Conditional End of Program |
| MEND | | Main Program End of Program |
| STOP | | Transition to STOP Mode |
| WDR | | Watchdog Reset (300 ms) |
| JMP | N | Jump to defined Label |
| LBL | N | Define a Label to Jump to |
| CALL | N | Call a Subroutine |
| SBR | N | Define a Subroutine to be Called |
| CRET | | Conditional Return from SBR |
| RET | | Unconditional Return from SBR |
| FOR | Index, Initial, Final | For/Next Loop |
| NEXT | | |
| LSCR | N | Load, Transition, and End Sequence Control Relay Segment |
| SCRT | N | |
| SCRE | | |

## Move, Shift, Rotate, and Fill Instructions

| | | |
|---|---|---|
| MOVB | IN, OUT | Move Byte, Word, DWord, Real |
| MOVW | IN, OUT | |
| MOVD | IN, OUT | |
| MOVR | IN, OUT | |
| BMB | IN, OUT, N | Block Move Byte, Word DWord |
| BMW | IN, OUT, N | |
| BMD | IN, OUT, N | |
| SWAP | IN | Swap Bytes |
| SHRB | Data, S_bit, N | Shift Register Bit |
| SRB | OUT, N | Shift Right Byte, Word, DWord |
| SRW | OUT, N | |
| SRD | OUT, N | |
| SLB | OUT, N | Shift Left Byte, Word, DWord |
| SLW | OUT, N | |
| SLD | OUT, N | |
| RRB | OUT, N | Rotate Right Byte, Word, DWord |
| RRW | OUT, N | |
| RRD | OUT, N | |
| RLB | OUT, N | Rotate Left Byte, Word, DWord |
| RLW | OUT, N | |
| RLD | OUT, N | |
| FILL | IN, OUT, N | Fill memory space with pattern |

## Logic Operations

| | | |
|---|---|---|
| ALD | | And for combinations |
| OLD | | Or for combinations |
| LPS | | Logic Push (stack control) |
| LRD | | Logic Read (stack control) |
| LPP | | Logic Pop (stack control) |
| ANDB | IN1, OUT | Logical And of Byte, Word, and DWord |
| ANDW | IN1, OUT | |
| ANDD | IN1, OUT | |
| ORB | IN1, OUT | Logical Or of Byte, Word, and DWord |
| ORW | IN1, OUT | |
| ORD | IN1, OUT | |
| XORB | IN1, OUT | Logical XOr of Byte, Word, and DWord |
| XORW | IN1, OUT | |
| XORD | IN1, OUT | |
| INVB | OUT | Invert Byte, Word and DWord (1's complement) |
| INVW | OUT | |
| INVD | OUT | |

## Table, Find, and Conversion Instructions

| | | |
|---|---|---|
| ATT | Data, Table | Add data to table |
| LIFO | Table, Data | Get data from table |
| FIFO | Table, Data | |
| FND= | Scr, Pattrn, Indx | Find data value in table that matches comparison |
| FND<> | Scr, Pattrn, Indx | |
| FND< | Scr, Pattrn, Indx | |
| FND> | Scr, Pattrn, Indx | |
| BCDI | OUT | Convert BCD to Integer |
| IBCD | OUT | Convert Integer to BCD |
| DTR | IN, OUT | Convert DWord to Real |
| TRUNC | IN, OUT | Convert Real to DWord |
| ATH | IN, OUT, LEN | Convert ASCII to HEX |
| HTA | IN, OUT, LEN | Convert HEX to ASCII |
| DECO | IN, OUT | Decode |
| ENCO | IN, OUT | Encode |
| SEG | IN, OUT | Generate 7-segment pattern |

## Interrupt

| | | |
|---|---|---|
| INT | N | Beginning of Interrupt routine |
| CRETI | | Conditional Return from Interrupt |
| RETI | | Return from Interrupt |
| ENI | | Enable Interrupts |
| DISI | | Disable Interrupts |
| ATCH | INT, EVENT | Attach Interrupt routine to event |
| DTCH | EVENT | Detach event |

## Communication

| | | |
|---|---|---|
| XMT | TABLE, PORT | Freeport transmission |
| RCV | TABLE, PORT | Freeport receive message |
| NETR | TABLE,PORT | Network Read |
| NETW | TABLE,PORT | Network Write |

## High Speed Instructions

| | | |
|---|---|---|
| HDEF | HSC, Mode | Define High Speed Counter mode |
| HSC | N | Activate High Speed Counter |
| PLS | X | Pulse Output |

Instructions are valid for the individual S7-200 PLCs as marked according to the following key:

- 214, 215, and 216 only
- 215 and 216 only

If not marked, the instructions are valid for all S7-200 PLCs.

# 2.ELECTRONIC CIRCUIT DEVICES

## 2.1.DIODE

### 2.1.1.PN Junction

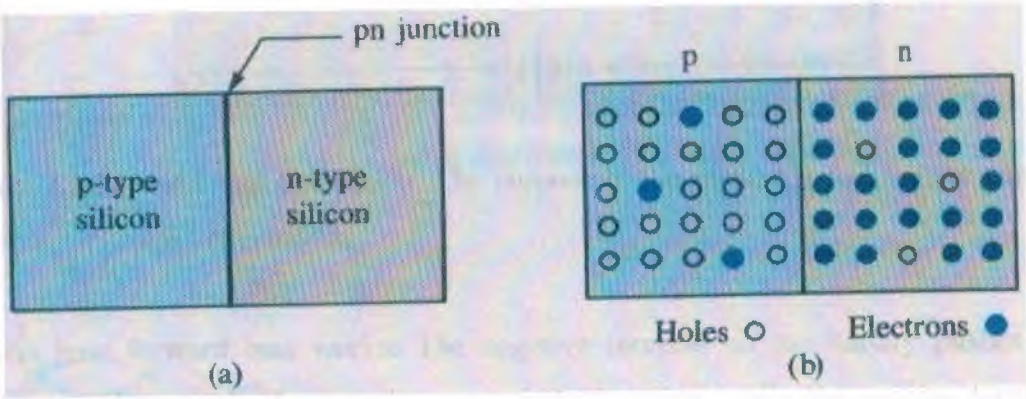



**Figure 2.1** Basic pn structure at the instant of junction formation. Both majority and minoriy carriers are shown.

Figure 2.1(a) shows a pn junction formed between the two regions when a piece of silicon is doped so that half is n-type and the other half is p-type. This basic structure forms a semiconductor diode. The n region has many free electrons (majority carriers ) and only a few thermally generated holes (minority carriers). The p region has many holes (majority carriers) and only a few thermally generated free electrons (minority carriers). This is shown in Figure 2.1(b). The pn junction is fundamental to the operation of diodes, transistors, and other solid state devices .

### 2.1.2. Forward Bias

The term bias in electronics refers to a fixed dc voltage that sets the operating conditions for a semiconductor device. Forward bias is the condition that permits current across a pn junction. Figure 2.2 shows a dc voltage connected in a direction to forward-bias the diode. Notice that the negative terminal of the battery is connected to n region ( called cathode ), and the positive terminal is connected to the p region ( called the anode ).

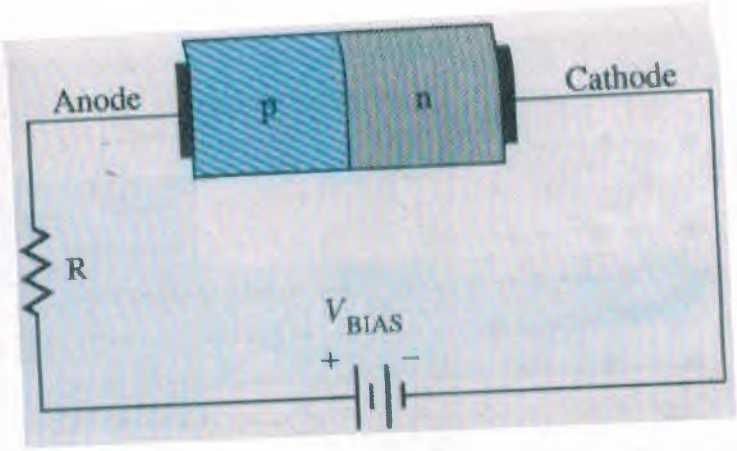



**Figure 2.2** Forward-bias connection. The purpose of the resistor is to limit the current to prevent damage to the diode.

This is how forward bias works: The negative terminal of the battery pushes the conduction electrons in the n region toward the junction, while the positive terminal pushes the holes in the p region also toward the junction. ( Recall that like charges repel each other.) When it overcomes the barrier potential, the external bias voltage source provides the n-region electrons with enough energy to penetrate the depletion layer and cross the junction, where they combine with the p-region holes. As electrons leave the n-region, more folw in from the negative terminal of the battery. So, current through the n-region is the movement of the conduction electrons (majority carriers) toward the junction.

When the conduction electrons enter the p region and combine with holes, they become valence electrons. They then move as valence electrons from hole to hole toward the positive anode connection. The movement of these valence electrons essentially creates a movement of holes in the opposite direction as we our learned earlier. So, current in the p region is the movement of holes ( majority carriers ) toward the junction. Figure 2.3 illustrated electron flow in a forward-biased diode.

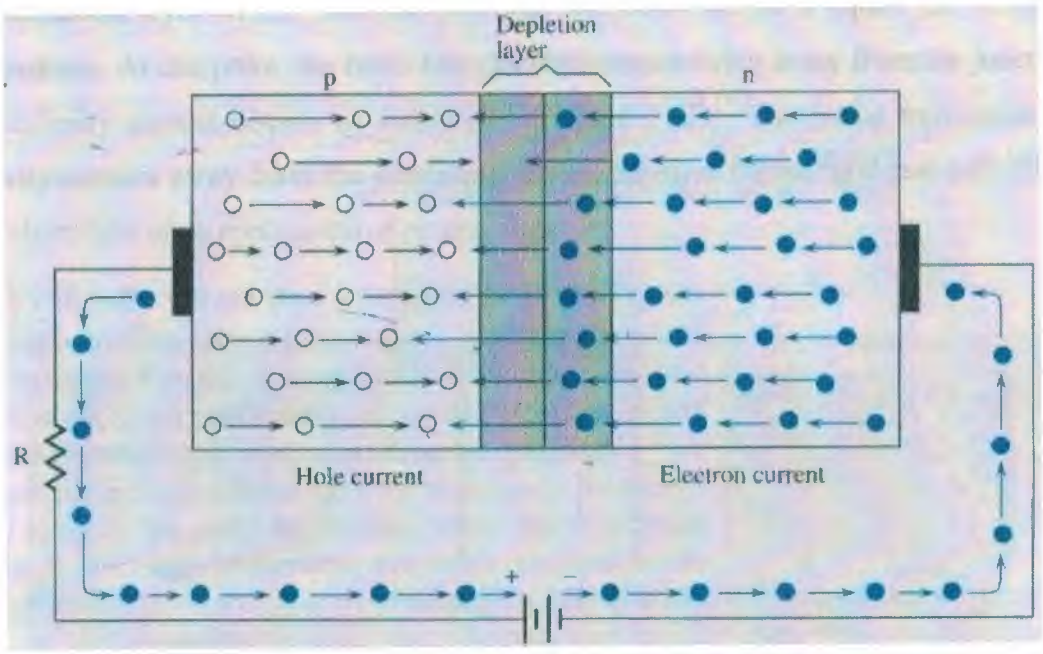



**Figure 2.3** Electron flow in a pn junction diode.

### 2.1.3.Reverse Bias

Reverse bias isthe condition that pervents cuurent across the pn junction. Figure 2.4. shows a dc voltage source connected to reverse-bias the diode. Notice that the negative terminal of the battery is connected to the p region, and the positive terminal is connected to the n region. The negative terminal of the battery attracts holes in the p region away from the pn junction, wihle the positive terminal also attracts electrons away from the junction. As electrons and holes move away from the junction, the depletion layer widens; more positive ions are ceated in the n region, and more negative ions are created in the p region, as shown in Figure 2.5.

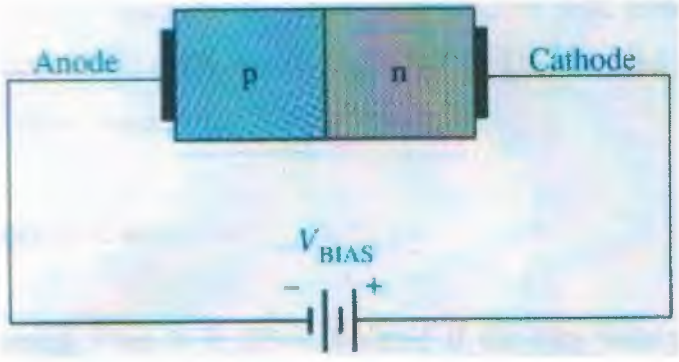



**Figure 2.4** Reverse bias connection.

The deplation layer widens until the potential difference across it equals the external bias voltage. At this point, the holes and electrons stop moving away from the junction and majority current ceases, as indicated in Figure 2.5(b). The initial movement of majority carriers away from the junction is called transient current and last only for a very short time upon application of reverse bias.

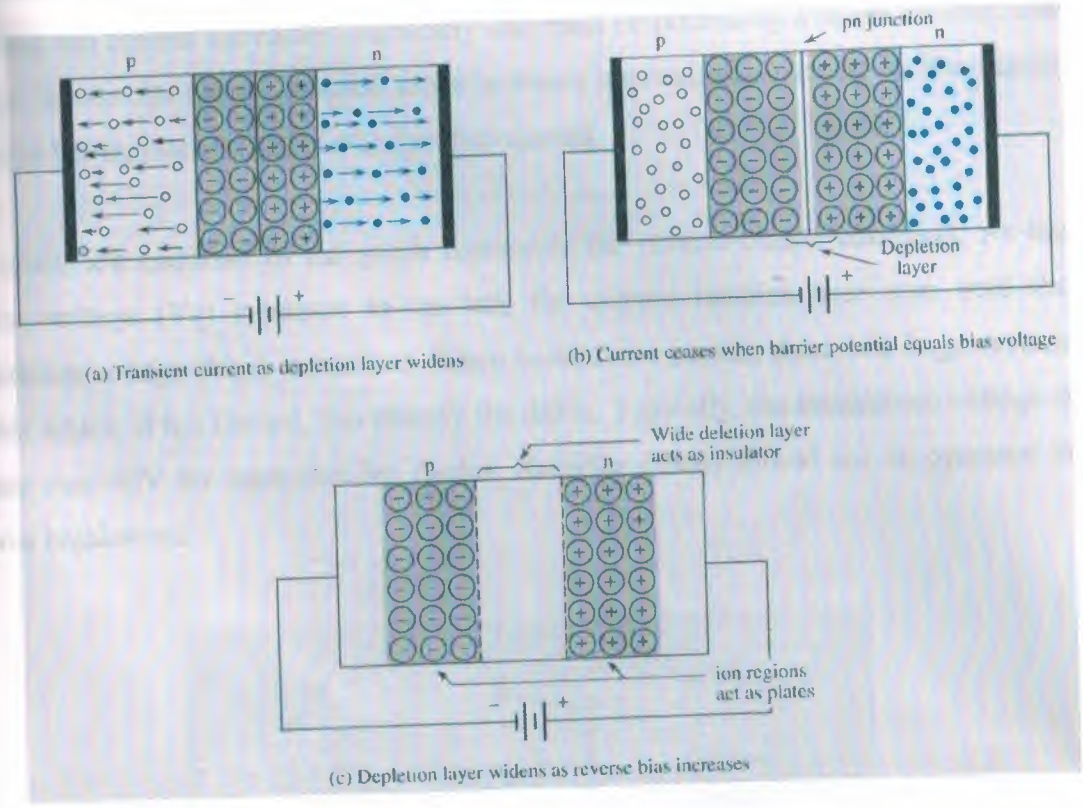



**Figure 2.5** Reverse bias.

When the diode is reverse-biased, the depletion layer effectively acts as an insulator between the layers of oppositely charged ions. This effectively forms a capacitor, is illustrated in Figure 2.5(c). Since the deplation layer widens with increased reverse-biased voltage, the capacitance decreases and vice versa. This internal capacitance is called deplation-layer capacitance.

### 2.1.4.Diode Characteristic Curve

A diode conducts current when it is forward-biased if the bias voltage exceeds the barrier potential, and the diode prevents current when it is reverse-biased at less than the

breakdown voltage. Figure 2.6 shows a diode characteristic curve, which is a graph of diode current versus voltage. The upper right quadrant of the graph represents the forward-biased condition. As we can see, there is essentialy no forward current ($I_f$) for forward voltages ($V_f$) below the barrier potential. As the forward voltage approaches the value of the barrier potential (typically 0.7V for the silicon and the 0.3V for germanium), the current begins to increase. Once the forward voltage reaches the barrier potential, the current insreaeses drastically and must be limited by a series resistor. The voltage across the forward-biased diode remains approximately equal to the barrier potential but increases slightly with forward current.

The tower left quadrant of the graph represents the reverse-biased condition. As the reverse voltage ($V_R$) increases to the left, the current remains near zero until the breakdown voltage ($V_{BR}$) is reached. When breakdown occurs, there is a large reverse current which, if not limited, can destroy the diode. Typically, the breakdown voltage is greater than 50V for most rectifier diodes. Rectifier diodes should not be operated in reverse breakdown.

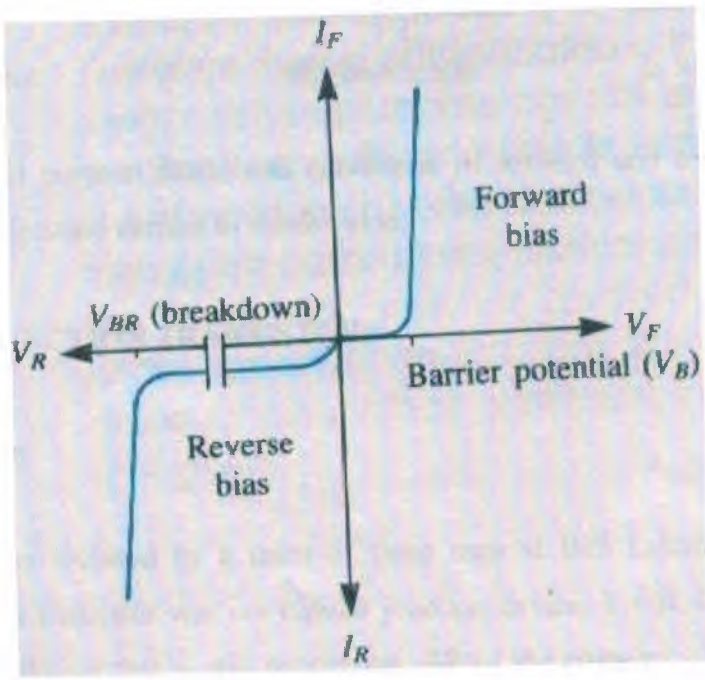



**Figure 2.6** Diode characteristic curve

### 2.1.5 Diode Symbol

Figure 2.7(a) is the standart symbol for a general-purpose diode. The arrow points in the direction of conventional current. The two terminals of the diode are the anode and cathode. When the anode is positive with respect to the cathode, the diode is forward biased and current is from anode to cathode, as shown in Figure 2.7(b). If there is any question about terminal polarities, always check the manufacturer's data book. Remember that when the diode is forward-biased, the barrier potential $V_B$ always appears between anode and cathode, as indicated in the figure. When the anode is negative with respect to the cathode, the diode is reverse-biased, as shown in Figure 2.7(c). The bias battery voltage is designated $V_{BB}$ and is not the same as the barrier potential.

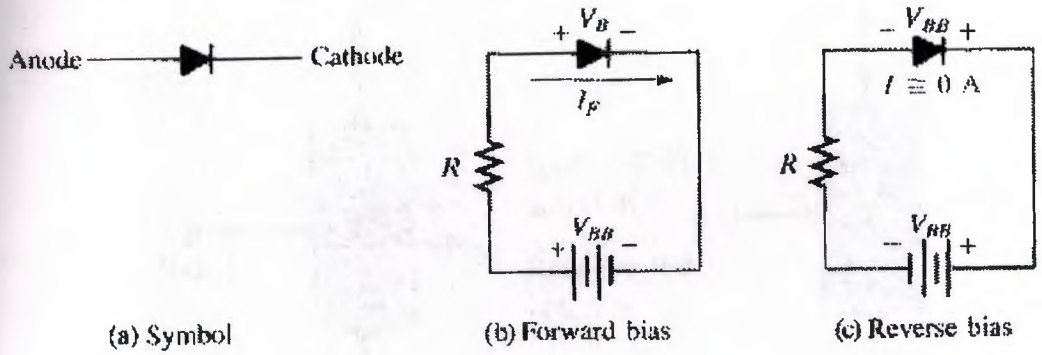



**Figure 2.7** Gneral purpose diode and conditions of forward and reverse bias. The resistor limits the forward current to a safe value.

## 2.2.BİPOLAR JUNCTION TRANSISTORS

### 2.2.1.Introduction

The transistor was invested by a team of three men at Bell Laboraturies in 1947. Although this first transistor was not bipolar junction device, it was the begining of a technological revolution that is still continuing. All of the complex electronic devices and systems today are an outgrowth of early developments in semiconductor transistors.

There are two basic types of transistors the bipolar junction transistor (BJT), and the field effect transistor (FET). The BJT is used in two broad areas as a linear amplifier to boost or amplify an electrical signal and as an electronic switch.

### 2.2.2.Transistor Construction

The bipolar junction transistor (BJT) is constructed with three doped semiconductor regions seperated by two pn junctions. The three regions are called **emitter**, **base**, and **collector**. The two types of bipolar transistor are shown in Figure 2.8. One type consists of two n regions seperated by n region (pnp).

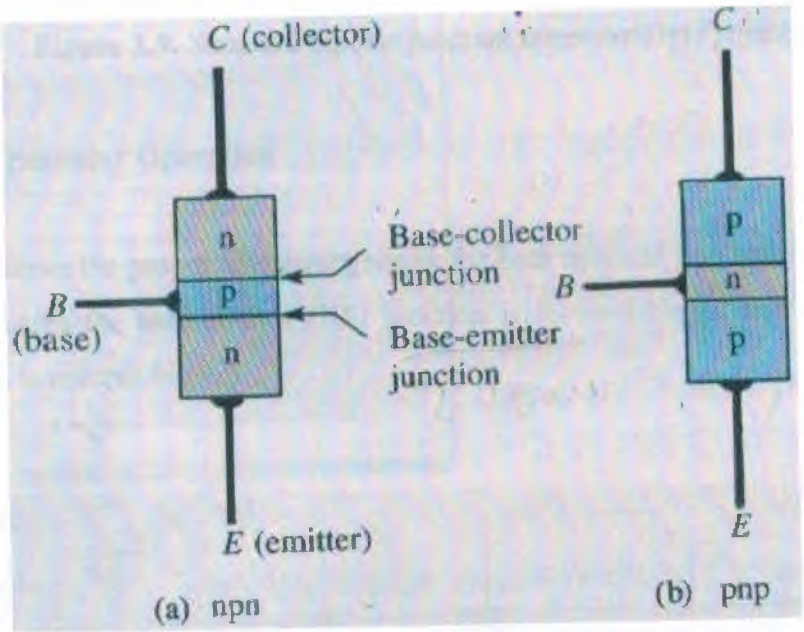



**Figure 2.8.** Basic bipolar transistor construction.

The pn junction joining the base region and the emitter region is called the base-emitter junction. The junction joining the base region and the collector region is called base-collector junction, as indicated in Figure 2.8(a). A wire lead connects to each of the three regions, as shown. These leads are labeled E, B, and C for emitter, base, and collector, respectively.

The base region is lightly doped and very narrow compared to the heavily doped emitter and collector regions. Figure 2.9 shows the shematic symbols for the npn and pnp

bipolar transistors. The term bipolar refers to the use of both holes and electrons as carriers in the transistor structure.

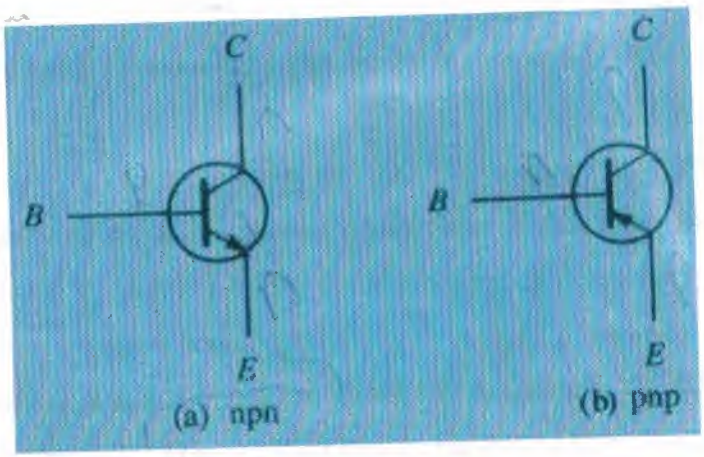



**Figure 2.9.** Standard bipolar junction transistor (BJT) symbols.

### 2.2.3.Basic Transistor Operation

Figure 2.10 shows the proper bias arrangement for both npn and pnp transistors. Notice that in both cases the base-emitter (BE) junction is forward-biased and the collector (BC) junction is reverse-biased.

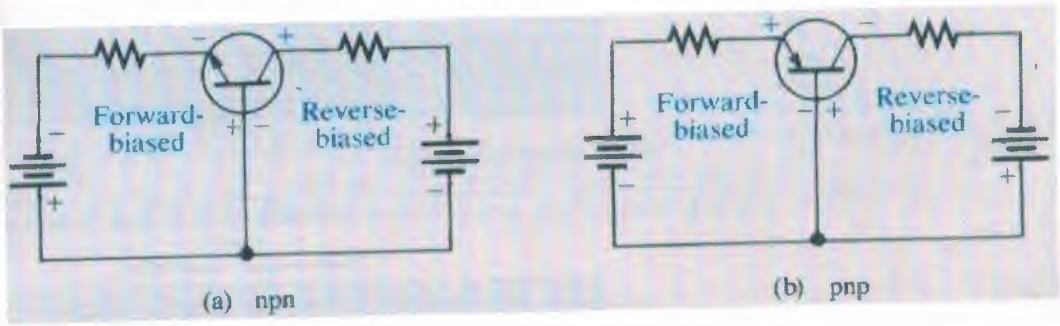



**Figure 2.10.** Forward-reverse bias of a bipolar transistor.

Now, let's examine what happens inside the transistor when it is forward-reverse biased. The forward bias from base emitter narrows the BE depletion layer, and the reverse bias from the base- collector widens the BC depletion layer, as depicted in Figure 2.11(a). The n type emitter region is teeming with conduction-band (free) electrons that easily diffuse across the forward-biased BE juntion in to the p type base region, just as in a forward-biased diode. The base region is lightly doped and very

narrow so that it has a very limited numöber of holes. Thus, only a small percentage of all electrons flowing across the BE junction can combine with the available holes. These relatively few recombined electrons flow out of the base lead as valence electrons, forming the small base current $I_B$, as shown in Figure 2.11(b).

Most of electrons flowing from the emitter into the narrow base region do not recombine and diffuse into the BC depletion layer. Once in this layer they are pulled across the reverse-biased BC juntion by the depletion layer field set up by the force of attraction between the positive and negative ions. Actually, we can think of the electrons are being pulled across the reverse-biased BC junction by the attraction of the positive ions on the other side. This is illustrated in Figure 2.11(c). The electrons now move through the collector region, out through the collector lead, and into the positive terminal of the external dc source. This forms the collector current, $I_C$, as shown. The amount of collector current depends directly on the amount of base current and is essentially independent the dc collector voltage.

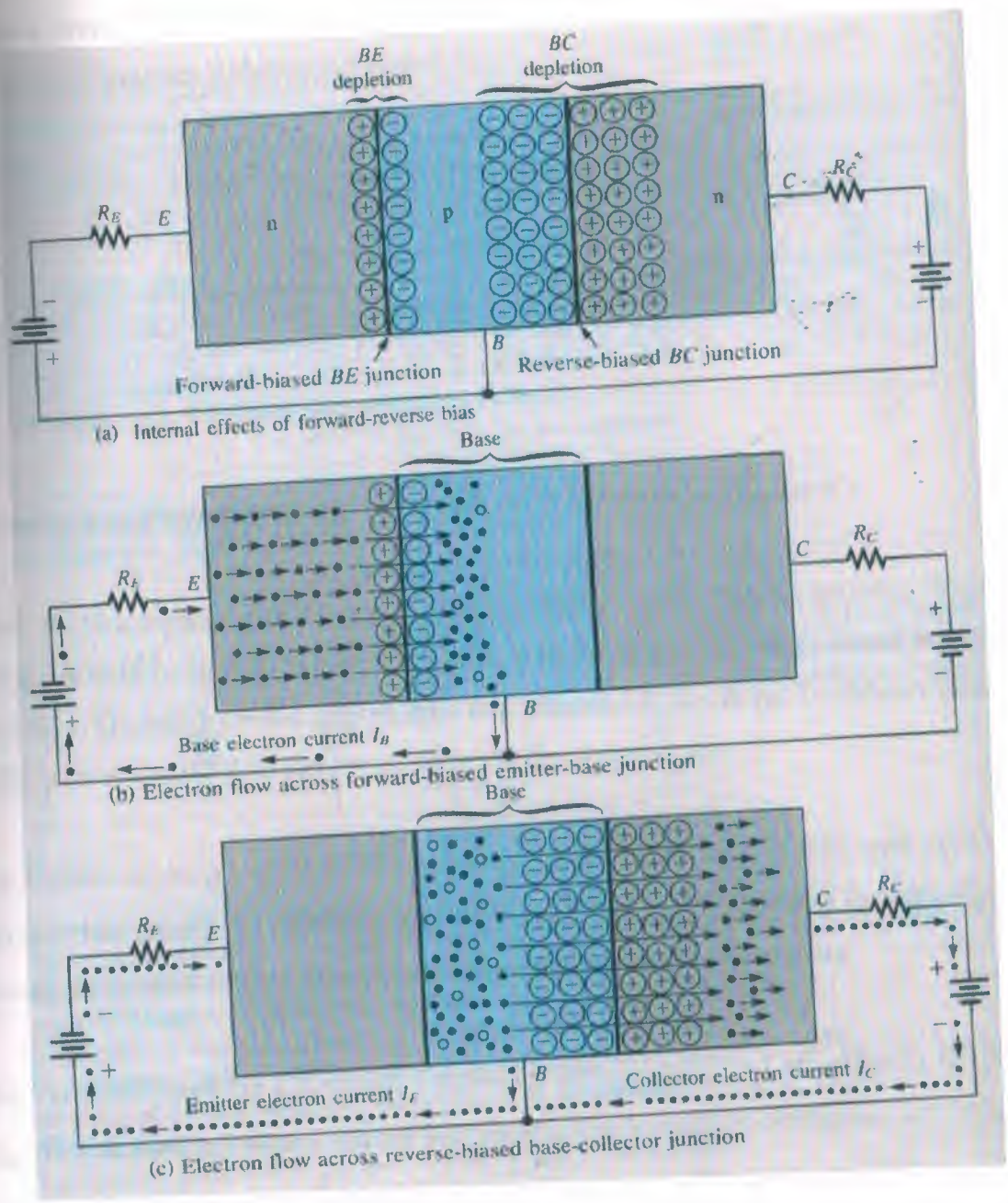



**Figure 2.11.** Illustration of BJT action. The base region is very narrow, but it is shown wider here for clarity.

## 2.3.SYNCHRONOUS UP/DOWN COUNTERS ICs

Four-bit synchronous binary counters are available in a single integreted-circuit (IC) package. The popular synchronous IC counters are the 74192 and 74193. They both have some features that were not available on the ripple counter ICs. The can count up or down and can be preset to any count that we desire. The 74192 is a BCD decade

up/down counter and the 74193 is a 4-bit binary up/down counter. The logic symbol used for both counters is shown in Figure 2.12.

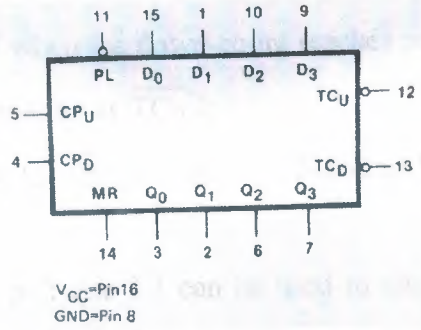



**Figure 2.12** Logic symbol for the 74192 and 74193 synchronous counter ICs.

There are two separate clock inputs: $C_{PU}$ for counting up and $C_{PD}$ for counting down. One colck must be held HIGH while counting with the other. The binary output is taken from $Q_0$ to $Q_3$, which are the outputs from four internal J-K flip-flops. The Master Reset (MR) is an active-HIGH Reset for resetting the Q outputs to zero.

The counter can be preset by placing any binary value on the parallel data inputs ($D_0$ to $D_3$) and then driving the Prallel Load ($\overline{PL}$) line LOW. The parallel load operation will change the counter outputs regardless of the conditions of the clock inputs.

The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down ($\overline{TC_D}$) are normally HIGH. The $\overline{TC_U}$ is used to indicate that the maximum count is reached and the count is about to recycle to zero (carry condition). The $\overline{TC_U}$ line goes LOW for the 74193 when the count reaches 15 and the clock ($C_{PU}$) goes HIGH to LOW. $TC_U$ remains LOW until $C_{PU}$ returns HIGH. This LOW pulse at $\overline{TC_U}$ can be used as a clock input to the next-higher-order stage of a multistage counter.

The $\overline{TC_U}$ output for the 74192 is similar except that is goes LOW at 9 and a LOW $C_{PU}$. The Boolean equations for $\overline{TC_U}$, therefore, are as follows:

$$\text{LOW at } \overline{TC_U} = Q_0Q_1Q_2Q_3\overline{CpU} \quad (74193)$$

$$\text{LOW at } \overline{TC_U} = Q_0Q_3\overline{CpU} \quad (74192)$$

The Terminal Count Down ($\overline{TC_D}$) is used to indicate that the minimum count is reached and the count is about the recycle to the maximum (15 to 9) count ( borrow condition ). Therefore, $\overline{TC_D}$ goes LOW when the down-count reaches zero and the input clock ($C_{pD}$) goes LOW. The Boolen Equation at $\overline{TC_D}$ is

LOW at $\overline{TC_D} = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}\ \overline{CpD}$ ( 74192 and 74193 )

The function table shown in Table 2.1 can be used to show the four operating modes (Reset, Load, Count Up, and Count Down ) of the 74192 / 74193

**Table 2.1** Function Table for the 74192 / 74193 Synchronous Counter Ics.

| Operating mode | Inputs | | | | | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $MR$ | $\overline{PL}$ | $C_{pU}$ | $C_{pD}$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $\overline{TC_U}$ | $\overline{TC_D}$ |
| Reset | H | × | × | L | × | × | × | × | L | L | L | L | H | L |
| | H | × | × | H | × | × | × | × | L | L | L | L | H | H |
| Parallel Load | L | L | × | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | × | H | L | L | L | L | L | L | L | L | H | H |
| | L | L | L | × | H | H | H | H | H | H | H | H | L | H |
| | L | L | H | × | H | H | H | H | H | H | H | H | H | H |
| Count Up | L | H | ↑ | H | × | × | × | × | Count up | | | | H | H |
| Count Down | L | H | H | ↑ | × | × | × | × | Count down | | | | H | H |

• H = HIGH voltage level; L = LOW voltage level; × = don't care; ↑ = LOW-to-HIGH clock transition.

## 2.4.NOT GATE (INVERTER)

The inverter is used to complement or invert a digital signal. It has a single input and single output. If HIGH level (1) comes in, it produces a LOW level (0) output. If a LOW level ( 0 ) comes in , it produces a HIGH level ( 1 ) output. The

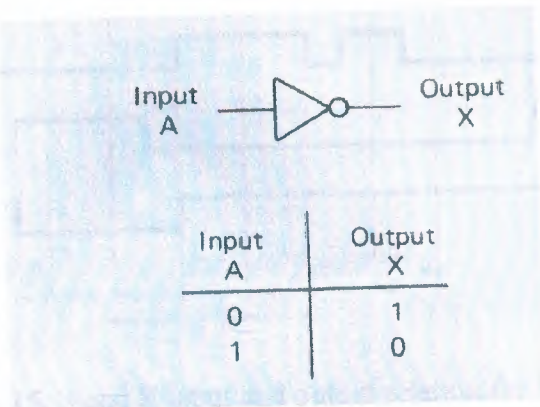



**Figure 2.13**. Inverter symbol and truth table.

symbol and truth table for the inverter gate are shown in Figure 2.13.

The operation of the inverter is very simple and can be illustrated further by studying the timing diagram of Figure 2.14. The timing diagram graphically show us the operation of the inverter. When the input is HIGH, the output is LOW, and when the input is LOW, the output is HIGH. The output wave form is therefore the exact complement of the input.

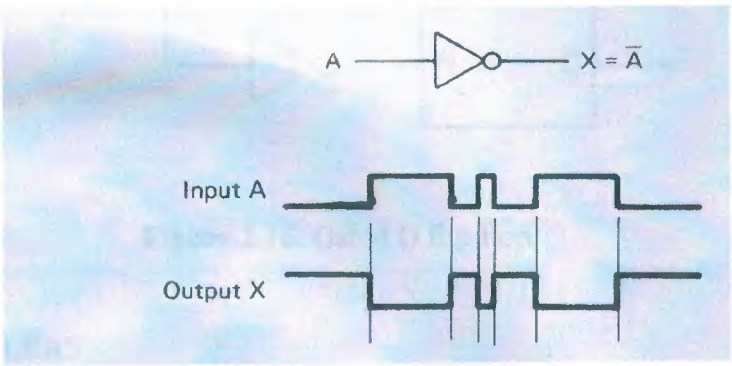



**Figure 2.14.** Timing analysis of an inverter gate.

The Boolen equation for an inverter is written $X = \overline{A}$ (X = NOT A). The bar overthe A is an inversion bar, used to signify the complement.

## 2.5. D TYPE FLIP-FLOP (Data flip-flop)

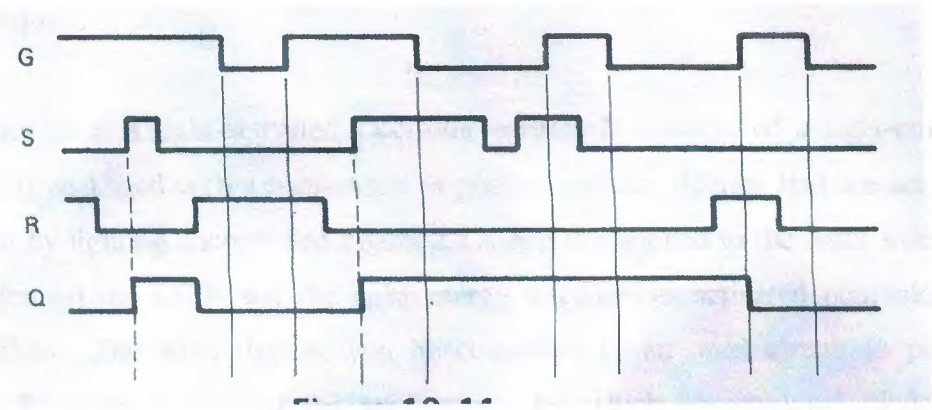



**Figure 2.15.** S and R input and output relation for D flip flop.

It can be formed from the gated S-R flip-flop by the adddition of an inverter. In Figure 2.16 we can see that S and R will be complements of each other, and S is connected to a single line labeled D (Data). The operation is such that Q will be the same as D, while G is HIGH and Q will remain "latched" in whatever state it was in before the HIGH-to-LOW transition on G.

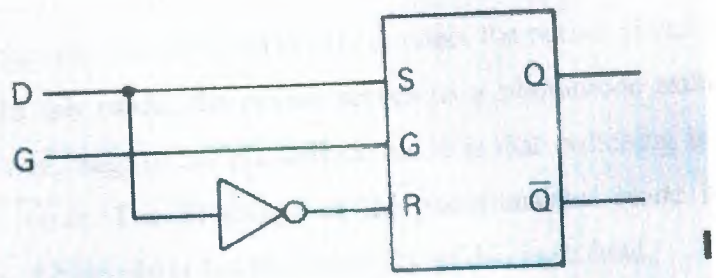



**Figure 2.16.** Gated D flip flop.

## 2.6.OPTOCOUPLERS

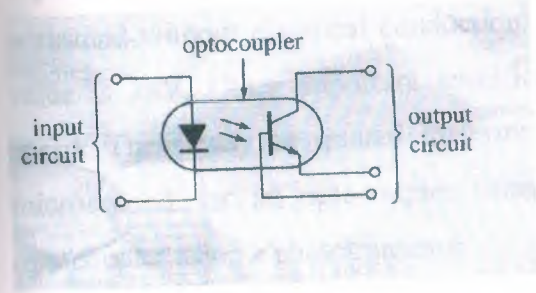



**Figure 2.17.** An optocoupler consists of an LED packaged with a photodiode or phototransistor

An optocoupler is a light-activated electronic switch. It consists of a light-emitting diode (LED) packaged with a *photodiode* or *phototransistor,* devices that are activated (turned on) by lighting energy. See Figure 2.17. A pulse applied to the input side turns on (illuminates) the LED, and the light energy it generates activated photodiode or phototransistor. The latter devices can be connected to an open circuit to perform switching functions in any of the applications for which conventional diodes and transistors are used. The principal use of optocouplers is to interface circuits where good electrical isolation is required. Since there is no physical contact between the input

circuit and output circuit, each can have a seperate ground, or referance. Because of this ability to isolate circuits, optocouplers are also called optoisolators.

The output circuit in Figure 2.17 contains phototransistors. In some commercially available units, the base is not an externally accessible terminal, since the only collector and emitter are neccessay to serve as switch terminals. In other units, the base terminal is accessible so that the user can have optionally connect the output circuit between the base and collector. In this mode, the device serves as a photodiode rather than as a phototransistor. The advantage of the photodiode mode is that switching is much faster than phototransistor mode. The advantage of the phootransistor mode is that, as in conventional devices, the transistor has the capability of driving a load.

The current tansfer ratio (CTR) of an optocoupler is the ratio of output current to input current. Depending on device design and application, it may range from 0.1 or less to several hundred. Optocoupler specifications usually include electrical isolation, expressed as a voltage. This voltage is the input-output voltage that the device can withstand without electrical cunduction occuring between input and output. A typical value is 2kV. Other important specifications of an optocoupler relate to switching speed. These may be quoted in terms of rise and fall times. Typical value are 1 microsecond for an optocoupler using a photodiode and 5 microseconds for an optocoupler using a phototransistor.

## 2.7. INTERFACING RELAYS AND SOLENOIDS

A relay is mechanical switch or set of switches that are pened or closed by a magnetic field generated when electrical current is passed through a coil. See Figure 2.18. In the context of a relay, the switches are called contacts. When no current passes through the coil, it is said to be deenergized, the contacts are in their ''normal'' state: normally open or normally closed. When the coil is energized, the contacts switch to the opposite state. Like optocouplers, relays provide electrical isolation between an input circuit (the coil) and output circuits, the circuits connected to the contact. They are used to drive heavy loads. A relatively small voltage applied to the coil circuit opens and closes heavy-duty contacts that can switch high voltages and currents. A very common application of relay is to start oand stop and electrical motor. A solenoid is similar to a relay

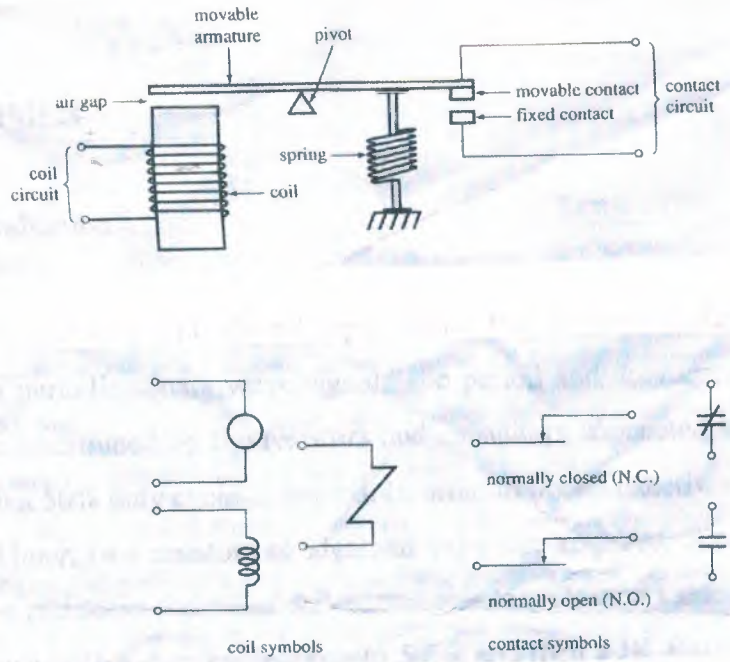



**Figure 2.18.** The electromechanical relay.

except in stead of opening and closing switches when its coil energized, it opens or closes a mechanical value. Solenoids are used the control flow of liquits and gases. Relays and solenoids are both very slow in comparison to electronic switching speeds, so they are used only when the load is to be switched in or out of a circuit for long intervals of time. An example of such a load is the fan motor in an air conditioning system.

Figure 2.19 shows a circuit used to drive a relay coil. One of the problems with driving a relay is that a very large voltage spike appears across the coil terminals.

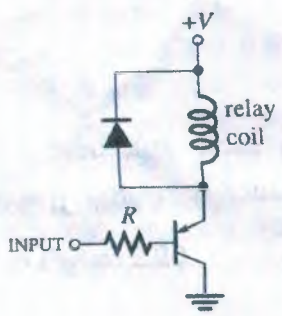



**Figure 2.19.** A relay-driver cicuit.

## 2.8. 555 TIMER

### 2.8.1.Introduction

The 555 Timer is a TTL digital logic circuit that is used in the controller circuit to produce a periodic square wave signal. The period and duty cycle of the square wave signal are determined by the resistors and capacitors connected to the timer. A square wave with a 50% duty cycle is desired. In order to obtain exactly a 50% duty cycle from the 555 Timer, two resistors of identical value are required. Since it is impractical to obtain two resistors of identical value, two resistors close in value are used to generate a square wave with a duty cycle close to 50%, and then a JK flip flop is used to create a square wave with a duty cycle of exactly 50%. The frequency of the square wave produced by the JK flip flop is 1/2 the frequency of the output of the 555 timer.

### 2.8.2.Time Delay Circuit

555 IC is used for monostable and also for astable. For astable and monostable the time constant can be adjusted between microseconds and a few hours. Since it works with 5V and 18V we can adopted to all type of circuits. An also it feeds 200mA, bulbs, relays, and some components which are like bulbs and relays can be drived directly. When the output of IC is high the IC spends 10mA by itself, and when the output reaches the zero volt it uses 1mA of 200mA.

In my circuit it is used as monostable oscillator.

## 2.9. DEMULTIPLEXERS

Demultiplexing is the opposite procedure from multiplexing. We can think of demultiplexer as a data distributor. It takes a single input data value and routes it to one of several outputs, as illustrated in Figure 2.20.

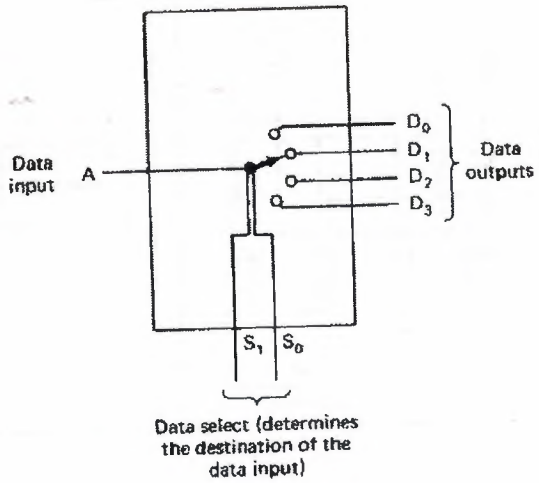



**Figure 2.20.** Functional diagram of a four-line demultiplexer.

Integrated-circuit demultiplexers come in several configurations of inputs/outputs. There are two types which is one of the 74139 dual four-line demultiplexer and other one is 74154 16-line demultiplexer.

The logig diagram and logic symbol for the 74139 are given in Figure 2.21. Notice that the 74139 is divided into two equal sections. By looking at the logic diagram, we will see that the schematic is the same as that of a 2-line-to-4-line decoder. Decoders and demultiplexers are the same, except with a decoder we hold the E enable line LOW and enter a code at the $A_0A_1$ inputs. As a demultiplexer, the $A_0A_1$ inputs are used to select the destination of input data. The input data are brought in via the E line. The 74138 3-line-to-8-line decoder.

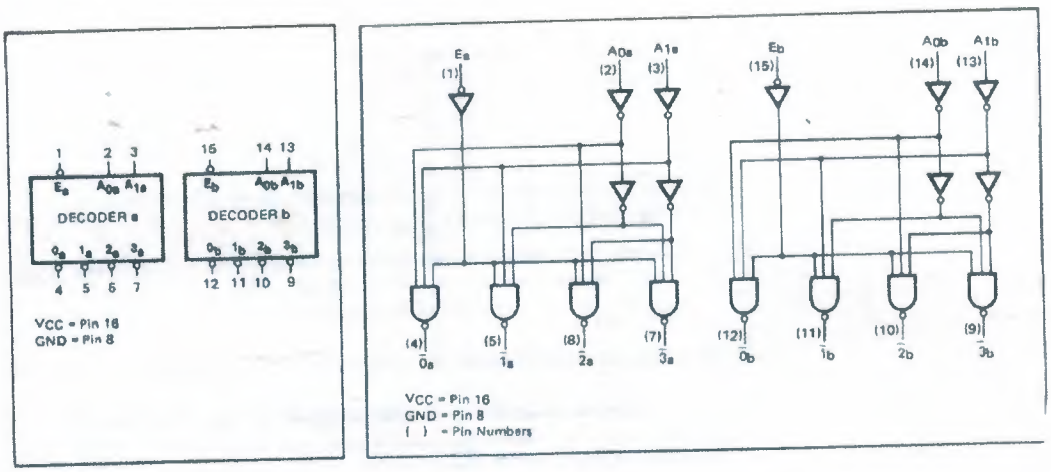



**Figure 2.21.** The 74139 dual 4-line demultiplexer: (a) logic symbol; (b) logic diagram.

To use the 74139 as a demultiplexer to route some input data signal to, let's say, the 2a output, the connections shown in Figure 2.22 would be made. In the figure the destination 2a selected by making $A_{1a} = 1$, $A_{0a} = 0$. The input signal is brought into the enable line ($E_a$). When $E_a$ goes LOW the selected output line goes LOW; when $E_a$ goes high, the selected output line goes HIGH.

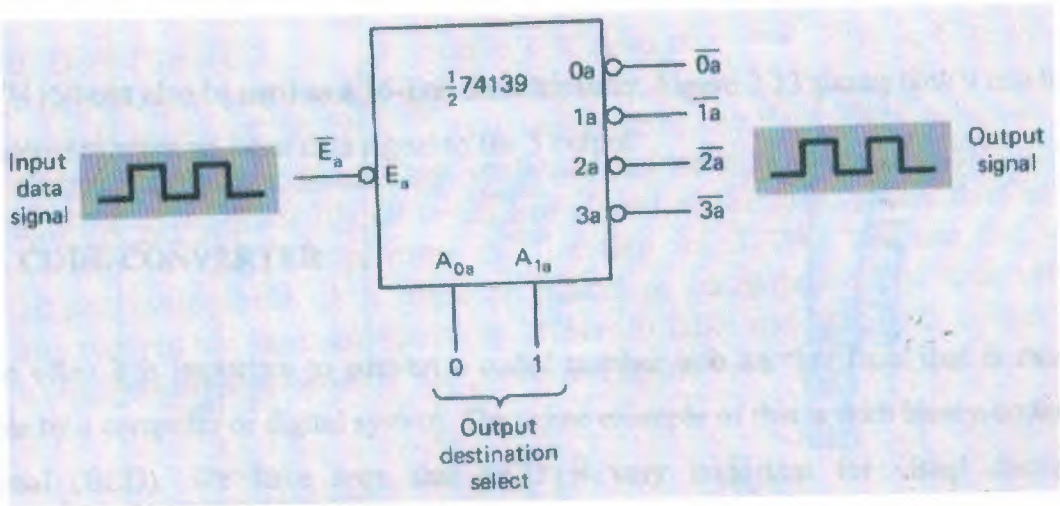



**Figure 2.22.** Connections to route an input data signal to the $2_a$ output of a 74139 demultiplexer.

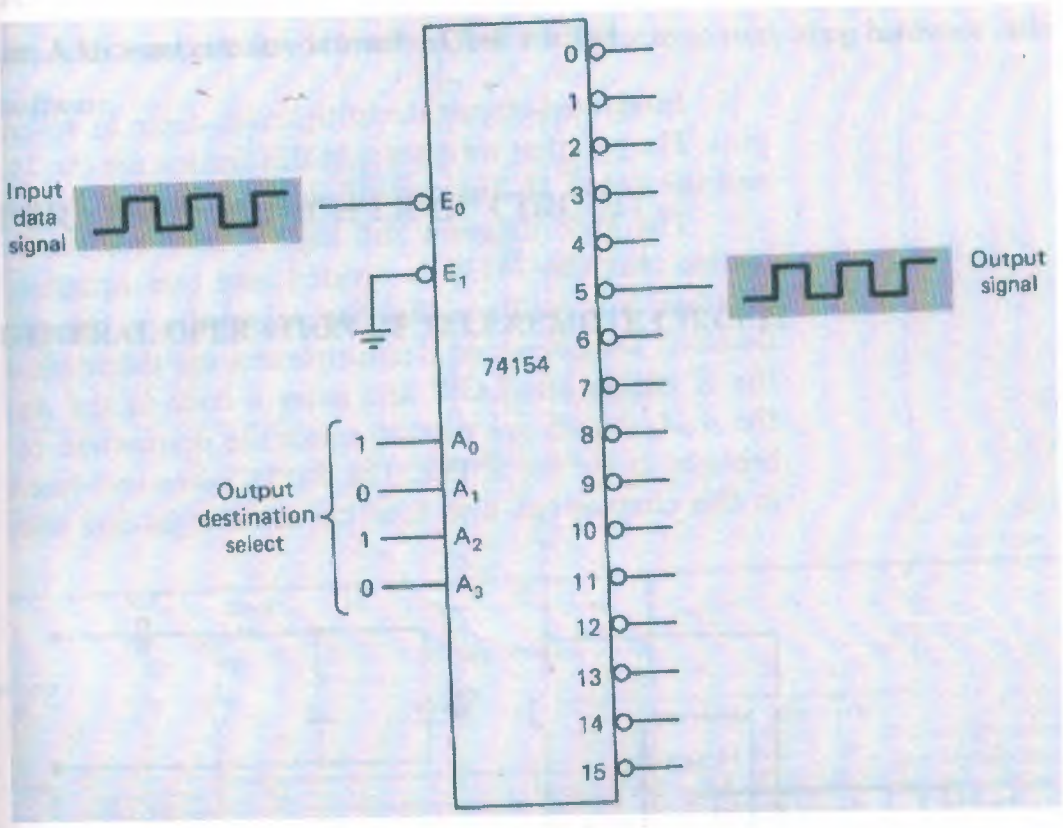



**Figure 2.23.** The 74154 demultiplexer connections to route an input signal to the 5 output.

The 74154 can also be used as a 16-line demultiplexer. Figure 2.23 shows how it can be connected to route an input data signal to the 5 output.

## 2.10. CODE CONVERTER

Quite often it is important to convert a coded number info another from that is more usable by a computer or digital system. The prime example of this is with binary-coded-decimal (BCD). We have seen that BCD is very important for visual display communication between a computer and human begins. But BCD is very difficult to deal with arithmetically. Algorithms, or procedures, have been developed for conversion of BCD to binary by computer programs (software) so that the computer will be able to perform all arithmetic operations in binary.

Another way to convert BCD to binary, the hardware approach, is with MSI integrated circuits. Additional circuitry is involved, but it is faster to convert using hardware rather than software.

# 3.OPERATION PRINCIPLE OF CIRCUIT

## 3.1. GENERAL OPERATION OF TELEREMOTE CIRCUIT

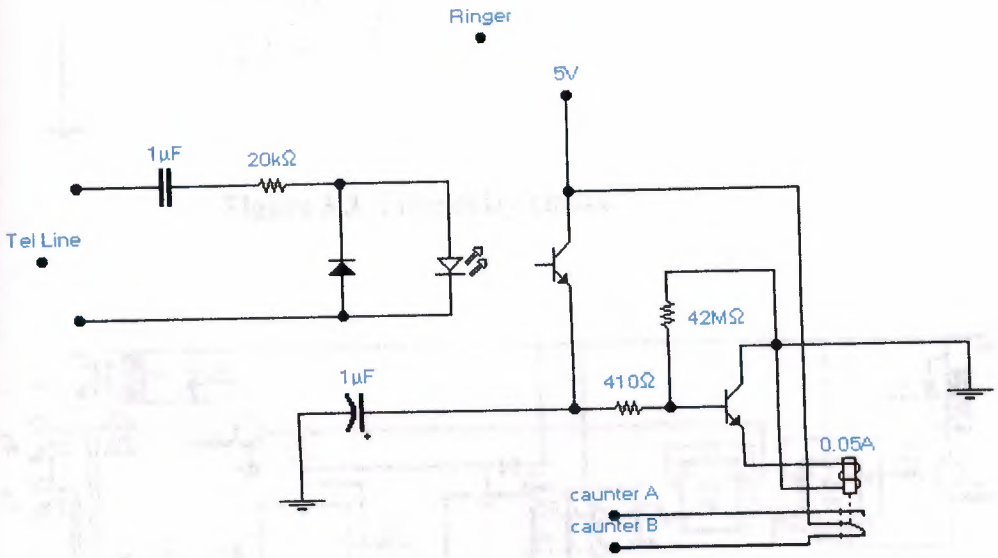



**Figure 3.1.** Receiver circuit

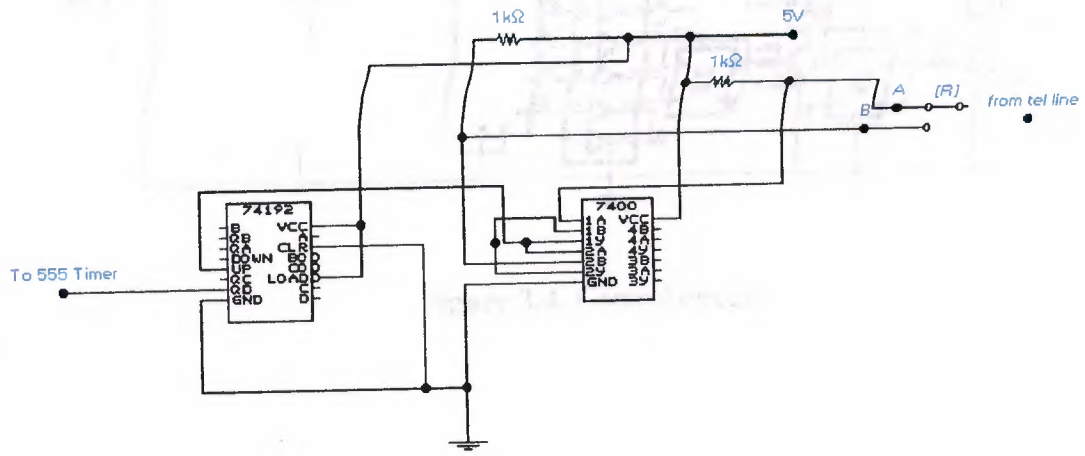



**Figure 3.2.** Counter circuit.

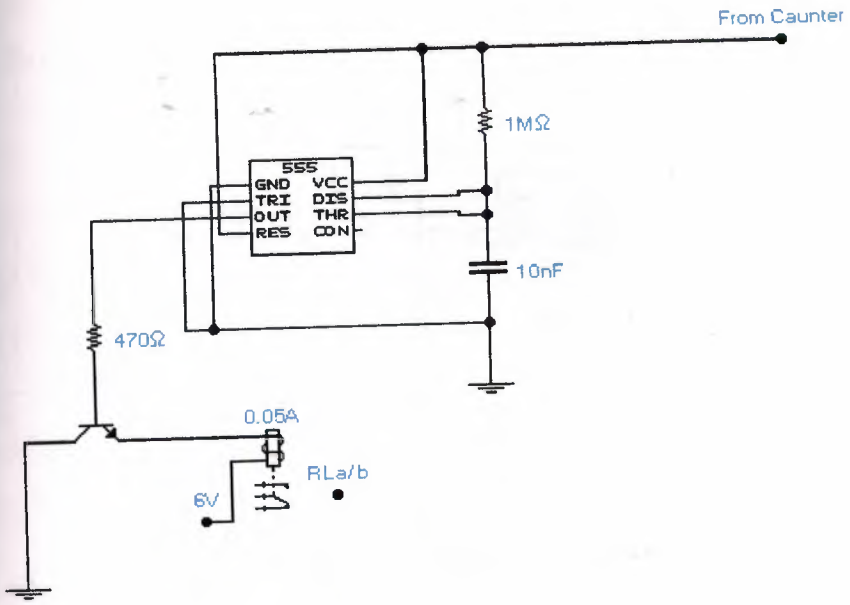



**Figure 3.3.** Time delay circuit.

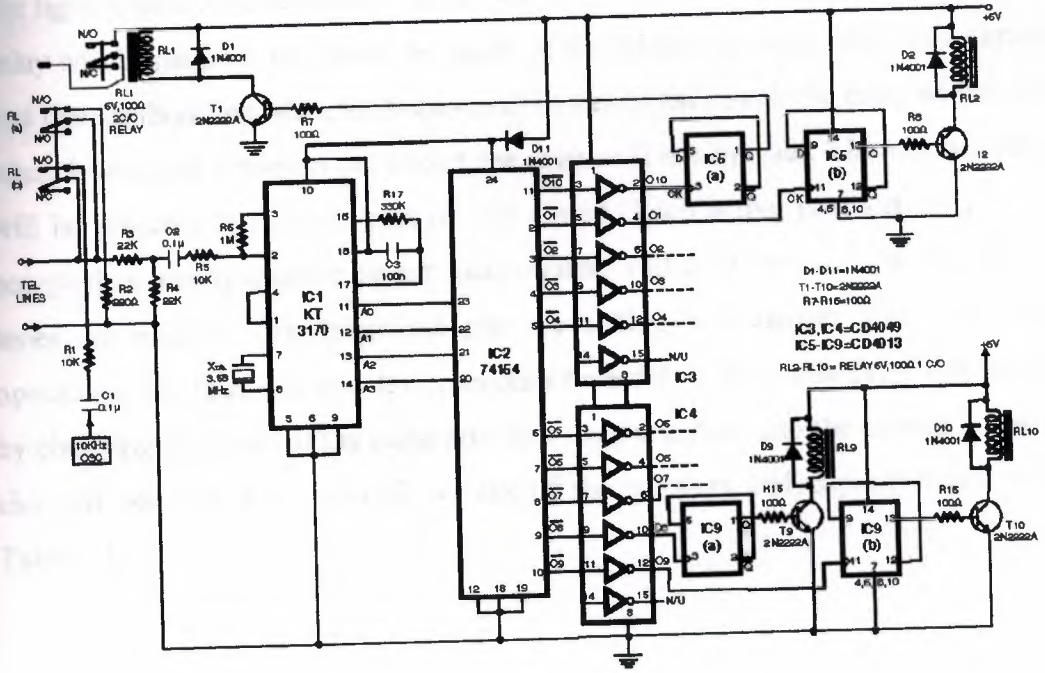



**Figure 3.4.** Control circuit.

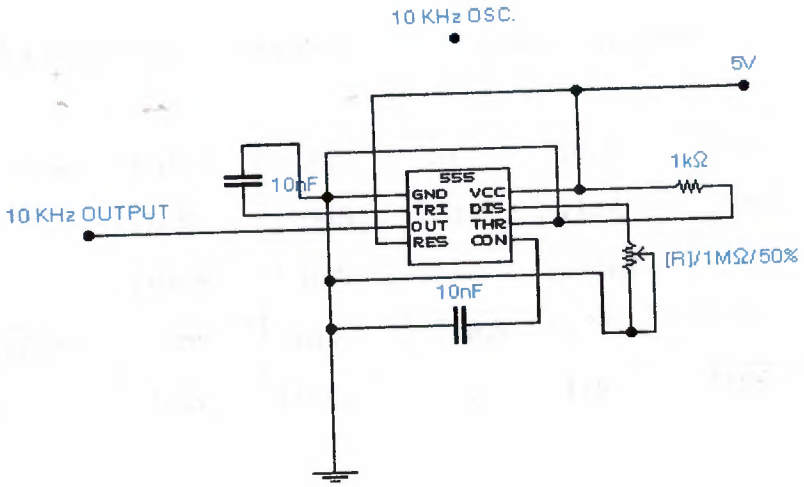



**Figure 3.5.** Oscillator Circuit

When the DTMF is send to the optocoupler part of the circuit the light emitting diode will emitte lights. The light emitted will be detected by the phototransistor will convert the light source to an electrical signal the TR1 will be driven and then the coil of the relay will be magnetized. Since the signal of the telephone line is high for a certain time and then of therefore when the high signal comes to the circuit the relay will operate but when low signal comes to the circuit the relay will not operate. This on and off period will be detected by counter part of that circuit. Each active position of relay will be accepted as one by counter circuit. And counter will count up to eight. When the eight tones are reached. The telephone you are calling will answer you. And after this operations the timer will set eleven seconds time delay. This time delay can be adjusted by changing the value of the capacitors and resistors. And also the counter value can be changed between some specific values of the resistors and capacitors are shown in Table 3.1.

**Table 3.1** Resistors and capacitors value of monostable timer.

| | 0.001μF | 0.01μF | 0.1μF | 1μF | 10μF | 100μF | 1000μF |
|---|---|---|---|---|---|---|---|
| 1kΩ | — | 11μS | 110μS | 1.1mS | 11mS | 110mS | 1.1S |
| 10kΩ | 11μS | 110μS | 1.1mS | 11mS | 110mS | 1.1S | 11S |
| 100kΩ | 110μS | 1.1mS | 11mS | 110mS | 1.1S | 11S | 110S |
| 1MΩ | 1.1mS | 11mS | 110mS | 1.1S | 11S | 110S | 1100S |

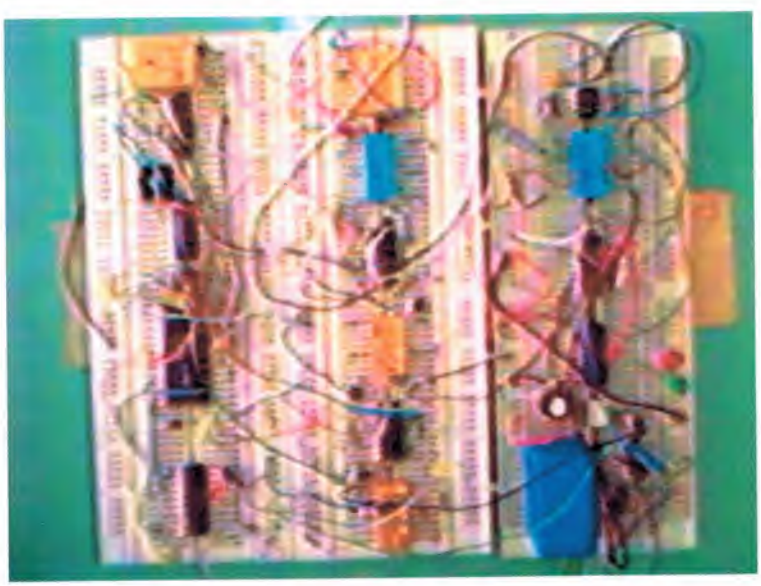
This eleven seconds time will let you do your operation. In this stituation, operations shoul be finished in limited time which is eleven seconds. When the zero button is pressed after operation, the operation will be finished. Or after counter counts eight if you zero button is pressed the system will give you unlimited time to perform your operation and again by pressing zero button, the operation will be finished.

## 3.2. OPERATIN OF THE CONTROL CIRCUIT

The circuit uses IC MT8870 (DTMF to BCD converter), 74154 (4-to-16-line Demultiplexer), and five CD4013 (D flip flop) ICs. The working of the circuit is as follows.

Once a call is established (after hearing ring-back tone), dial "0" in DTMF mode. IC1 decodes this as '1010', which is further demultiplexed by IC2 as output 010 (at pin 11) of IC2 (74154). The active low output of IC2, after inversion by an inverter gate of IC3 *(CD4049), becomes logic 1. This is used to toggle flip-flop-1 (F/F-1) and relay RL1 is* energised. Relay RL1 has two changeover contacts, RL1(a) and RL1(b). The energised RL1(a) contacts provide a 220-ohm loop across the telephone line while RL1(b) contacts inject a 10kHz tone on the line, which indicates to the caller that appliance mode has been selected. The 220-ohm loop on telephone line disconnects the ringer from the telephone line in the exchange. The line is now connected for appliance mode of operation.

If digit '0' is not dialed (in DTMF) after establishing the call, the ring continues and the telephone can be used for normal conversation. After selection of the appliance mode of operation, if digit '1' is dialed, it is decoded by IC1 and its output is '0001'. This BCD code is then multiplexed by 4-to-16-line demultiplexer IC2 whose corresponding output, after inversion by a CD4049 inverter gate, goes to logic 1 state. This pulse toggles the corresponding flip-flop to alternate state. The flip-flop output is used to drive a relay (RL2) which can switch on or switch off the appliance connected through its contacts. By dialing other digits in a similar way, other appliances can also be switched 'on' or 'off'. Once the switching operation is over, the 220-ohm loop resistance and 10kHz tone needs to be removed from the telephone line. To achieve this, digit '0' (in DTMF mode) is dialed again to toggle flip-flop-1 to de-energise relay RL1, which terminates the loop on line and the 10kHz tone is also disconnected. The telephone line is thus again set free to receive normal calls. This circuit is to be connected in parallel to the telephone instrument.



# 4. OPERATION OF PLC

## 4.1. LADDER DIAGRAM & STATEMENT LIST

**Network 1**

When press the button one, I 0.0 input will operated and heater (Q 0.0) is operated as timer count as.

**Network 2**

When I 0.0 is active, counter (C0) count one and when press the button seven,it will be reset.

**Network 3**

After the counter (C0) count one, timer (T36) will counted thirty sec.

**Network 4**

When press the button two (three times), I 0.4 input will active and heater (Q 0.4) would be operated as timer count as.

**Network 5**

When I 0.4 is active, the counter (C1) count two and it will be reset when press the button seven.

**Network 6**

After counter (C1) count, timer (T38) count sixty sec.

**Network 7**

When we press the button eight, I 0.1 input is active and washing machine (Q 0.1) will operate.

**Network 8**

When the button nine was pressed, I 0.2 input will active and microwave oven (Q 0.2) would operated as timer count as.

**Network 9**

When I 0.2 is active, counter (C2) counts one.And it will reset with button seven.

**Network 10**

When counter (C2) counts one, timer (T39) will count thirty sec.

**Network 11**

When the button five was pressed (three times), I 0.3 input would be active and microwave oven (Q 0.5) will operate as timer count as.

**Network 12**

When I 0.3 is operate, counter (C3) will count two and when pressing the button seven, it will be reset.

**Network 13**

After counter (C3) counted, the timer would count sixty sec.

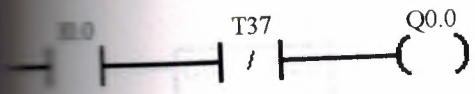
**Network 14**

The operation will finish.

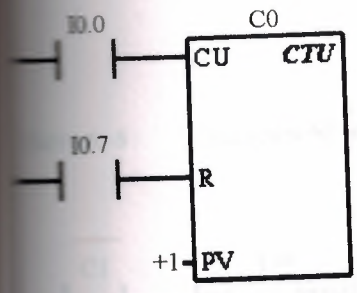
PROGRAM TITLE COMMENTS

Press F1 for help and example program

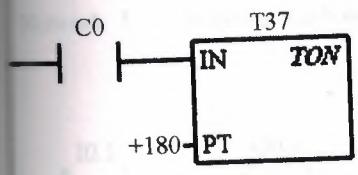
Network 1 Heater operation for 30 sec.



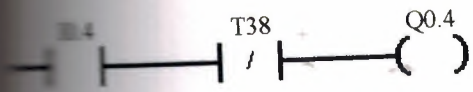

Network 2 Counter count 1



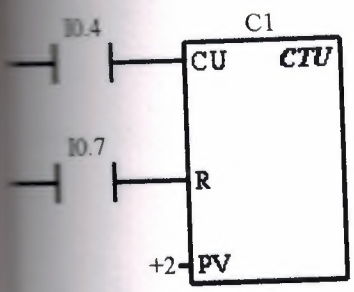

Network 3 Timer count 30 sec.



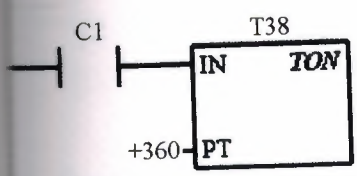
Network 4 Heater operation for 60 sec.




Network 5 Counter count 2.

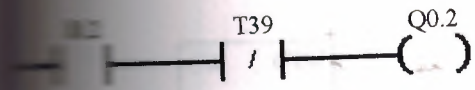



Network 6 Timer count 60 sec.

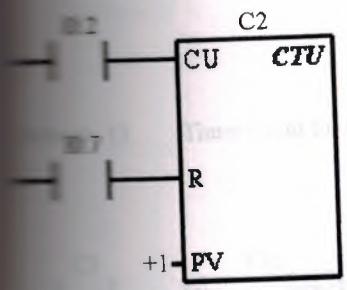



Network 7 Washing machine operation

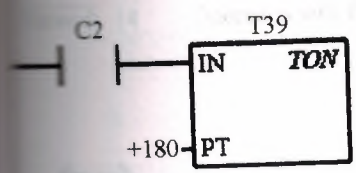
Microwave oven operation for 30 sec.



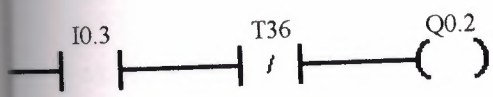

Counter count 1.



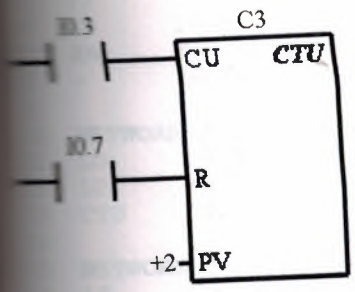

Timer count 30 sec.



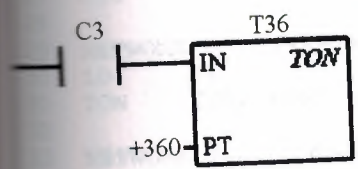

Microwave oven operation for 60 sec.



Network 12 Counter count 2.




Network 13 Timer count for 60 sec.




Network 14 Operation will finish.

(END)

```
NETWORK 1    //Heater operation for 30 sec.

LD      I0.0
AN      T37
=       Q0.0

NETWORK 2    //Counter count 1
LD      I0.0
LD      I0.7
CTU     C0, +1

NETWORK 3    //Timer count 30 sec.
LD      C0
TON     T37, +180

NETWORK 4    //Heater operation for 60 sec.
LD      I0.4
AN      T38
=       Q0.4

NETWORK 5    //Counter count 2.
LD      I0.4
LD      I0.7
CTU     C1, +2

NETWORK 6    //Timer count 60 sec.
LD      C1
TON     T38, +360

NETWORK 7    //Washing machine operation
LD      I0.1
=       Q0.1

NETWORK 8    //Microwave oven operation for 30 sec.
LD      I0.2
AN      T39
=       Q0.2

NETWORK 9    //Counter count 1.
LD      I0.2
LD      I0.7
CTU     C2, +1

NETWORK 10   //Timer count 30 sec.
LD      C2
TON     T39, +180

NETWORK 11   //Microwave oven operation for 60 sec.
LD      I0.3
AN      T36
=       Q0.2

NETWORK 12   //Counter count 2.
LD      I0.3
LD      I0.7
CTU     C3, +2

NETWORK 13   //Timer count for 60 sec.
LD      C3
TON     T36, +360

NETWORK 14   //Operation will finish.
MEND
```

# CONCLUSION

The aim of the study is showing that any process can be managed remotely with easy. Need for remote managing could appear in health-critical or dangerous conditions, being far away job, etc. It could be extremely useful for managers to check or administer.

In fact, a production unit may have a PLC or other types of control device on their processes, so that they may not need this part of job. In this case, if some computers make the data collection and control the process with telephone lines.

In our study, since the telephone lines are live, the processes are controlled in seconds easily. Of course if the destination number is in local area, only dialling will be faster therefore the process will be faster.

In practice, after answering the telephone the tele-secretary will be activated and direct the user by its voice commans.

Our study enables user perform processes twice for safety the password may be set. As human life is busy or be far away from their houses and factories. The remote control becomes very important, since most of equipments are controlled by telephone line.

FAIRCHILD SEMICONDUCTOR®

# 1N4001 - 1N4007

## Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

## General Purpose Rectifiers

### Absolute Maximum Ratings*

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Value | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | 4001 | 4002 | 4003 | 4004 | 4005 | 4006 | 4007 | |
| $V_{RRM}$ | Peak Repetitive Reverse Voltage | 50 | 100 | 200 | 400 | 600 | 800 | 1000 | V |
| $I_{F(AV)}$ | Average Rectified Forward Current .375 " lead length @ $T_A$ = 75°C | 1.0 | | | | | | | A |
| $I_{FSM}$ | Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave | 30 | | | | | | | A |
| $T_{stg}$ | Storage Temperature Range | -55 to +175 | | | | | | | °C |
| $T_J$ | Operating Junction Temperature | -55 to +175 | | | | | | | °C |

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

### Thermal Characteristics

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $P_D$ | Power Dissipation | 3.0 | W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 50 | °C/W |

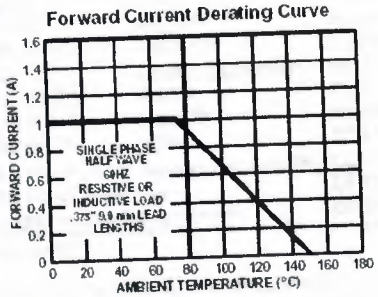
### Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

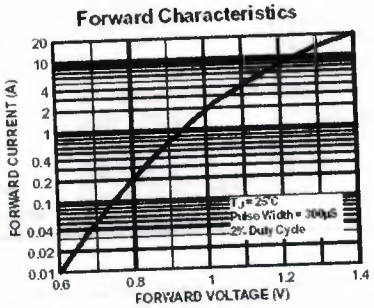
| Symbol | Parameter | Device | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | 4001 | 4002 | 4003 | 4004 | 4005 | 4006 | 4007 | |
| $V_F$ | Forward Voltage @ 1.0 A | 1.1 | | | | | | | V |
| $I_R$ | Maximum Full Load Reverse Current, Full Cycle $T_A$ = 75°C | 30 | | | | | | | µA |
| $I_R$ | Reverse Current @ rated $V_R$ $T_A$ = 25°C | 5.0 | | | | | | | µA |
| | $T_A$ = 100°C | 500 | | | | | | | µA |
| $C_T$ | Total Capacitance $V_R$ = 4.0 V, f = 1.0 MHz | 15 | | | | | | | pF |

## Typical Characteristics

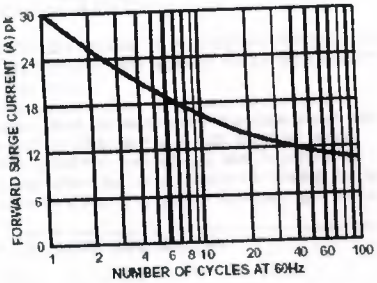
### Forward Current Derating Curve



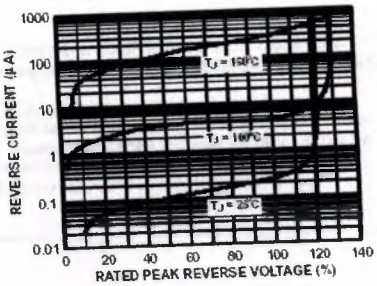

### Forward Characteristics




### Non-Repetitive Surge Current




### Reverse Characteristics



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Across the board. Around the world.™
The Power Franchise™
ProgrammableActive Droop™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |

Rev. I2

FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised March 2002

# CD4013BC
# Dual D-Type Flip-Flop

## General Description

The CD4013B dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

## Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 $V_{DD}$ (typ.)
- Low power TTL: fan out of 2 driving 74L
  compatibility: or 1 driving 74LS

## Applications

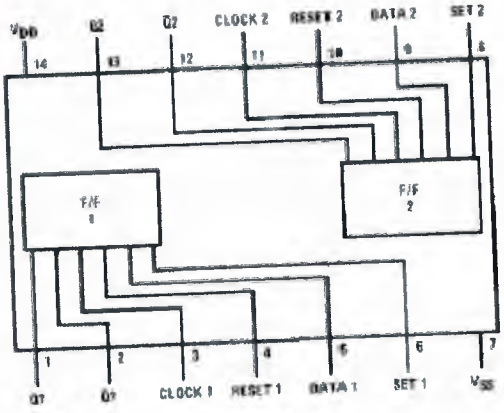
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| CD4013BCM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4013BCSJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| CD4013BCN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




Top View

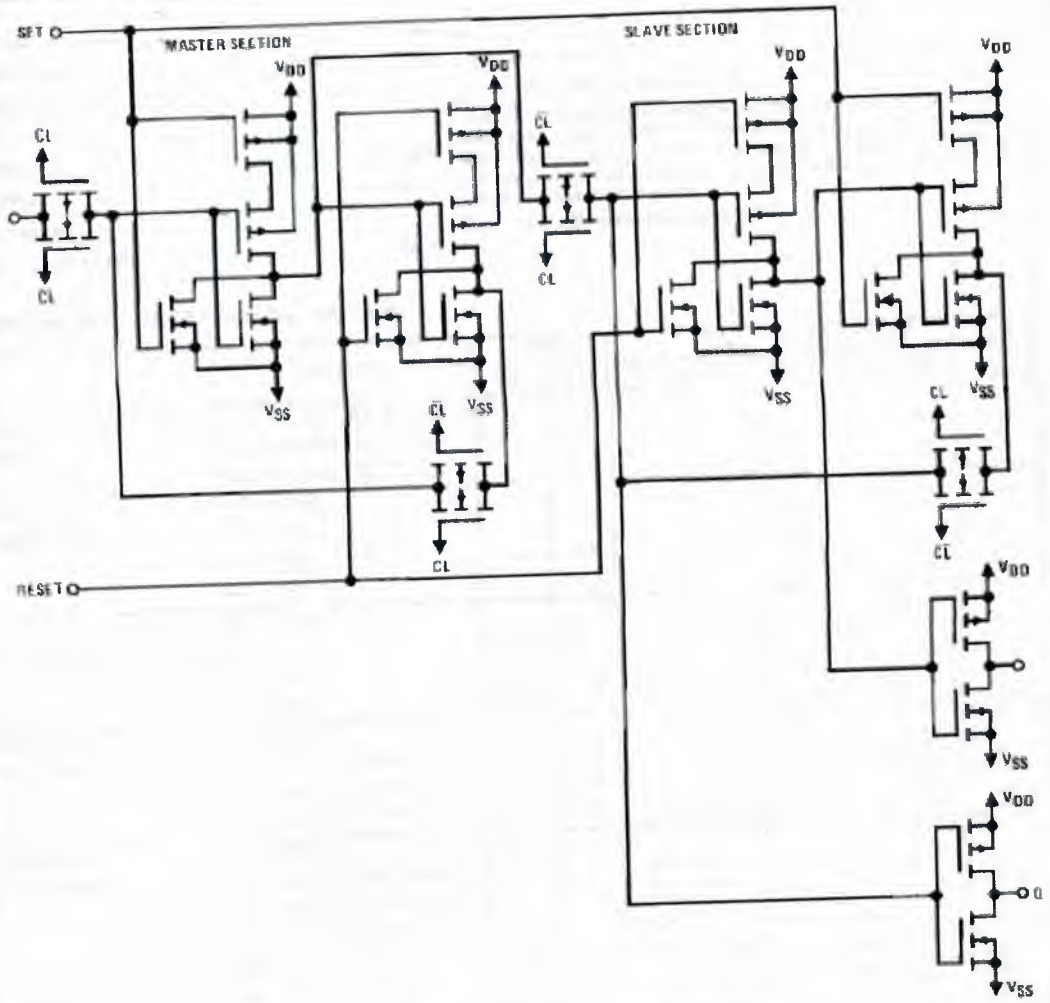
## Truth Table

| CL (Note 1) | D | R | S | Q | $\overline{Q}$ |
|---|---|---|---|---|---|
| ↗ | 0 | 0 | 0 | 0 | 1 |
| ↗ | 1 | 0 | 0 | 1 | 0 |
| ↘ | x | 0 | 0 | Q | $\overline{Q}$ |
| x | x | 1 | 0 | 0 | 1 |
| x | x | 0 | 1 | 1 | 0 |
| x | x | 1 | 1 | 1 | 1 |

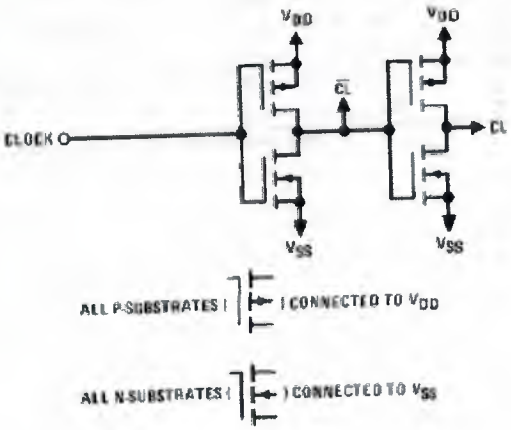
No Change
x = Don't Care Case
Note 1: Level Change

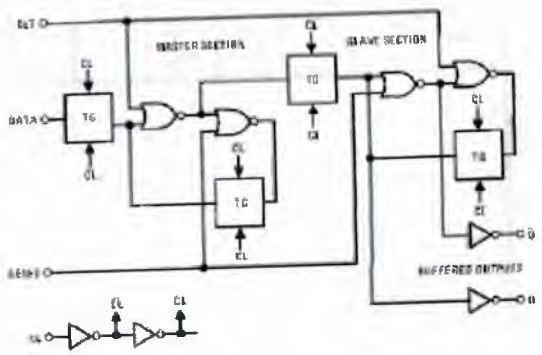
 DS005946

## Schematic Diagrams




## Logic Diagram



## Absolute Maximum Ratings (Note 2)

(Note 3)

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | −0.5 $V_{DC}$ to +18 $V_{DC}$ |
| Input Voltage ($V_{IN}$) | −0.5 $V_{DC}$ to $V_{DD}$ +0.5 $V_{DC}$ |
| Storage Temperature Range ($T_S$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |

## Recommended Operating Conditions (Note 3)

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | +3 $V_{DC}$ to +15 $V_{DC}$ |
| Input Voltage ($V_{IN}$) | 0 $V_{DC}$ to $V_{DD}$ $V_{DC}$ |
| Operating Temperature Range ($T_A$) | −55°C to +125°C |

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 3: $V_{SS}$ = 0V unless otherwise specified.

## DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | −55°C | | +25°C | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}$ = 5V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 1.0 | | | 1.0 | | 30 | µA |
| | | $V_{DD}$ = 10V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 2.0 | | | 2.0 | | 60 | |
| | | $V_{DD}$ = 15V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 4.0 | | | 4.0 | | 120 | |
| $V_{OL}$ | LOW Level Output Voltage | $\|I_O\|$ < 1.0 µA | | | | | | | | V |
| | | $V_{DD}$ = 5V | | 0.05 | | | 0.05 | | 0.05 | |
| | | $V_{DD}$ = 10V | | 0.05 | | | 0.05 | | 0.05 | |
| | | $V_{DD}$ = 15V | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{OH}$ | HIGH Level Output Voltage | $\|I_O\|$ < 1.0 µA | | | | | | | | V |
| | | $V_{DD}$ = 5V | 4.95 | | 4.95 | | | 4.95 | | |
| | | $V_{DD}$ = 10V | 9.95 | | 9.95 | | | 9.95 | | |
| | | $V_{DD}$ = 15V | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{IL}$ | LOW Level Input Voltage | $\|I_O\|$ < 1.0 µA | | | | | | | | V |
| | | $V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V | | 1.5 | | | 1.5 | | 1.5 | |
| | | $V_{DD}$ = 10V, $V_O$ = 1.0V or 9.0V | | 3.0 | | | 3.0 | | 3.0 | |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V | | 4.0 | | | 4.0 | | 4.0 | |
| $V_{IH}$ | HIGH Level Input Voltage | $\|I_O\|$ < 1.0 µA | | | | | | | | V |
| | | $V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V | 3.5 | | 3.5 | | | 3.5 | | |
| | | $V_{DD}$ = 10V, $V_O$ = 1.0V or 9.0V | 7.0 | | 7.0 | | | 7.0 | | |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V | 11.0 | | 11.0 | | | 11.0 | | |
| $I_{OL}$ | LOW Level Output Current (Note 4) | $V_{DD}$ = 5V, $V_O$ = 0.4V | 0.64 | | 0.51 | 0.88 | | 0.36 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 0.5V | 1.6 | | 1.3 | 2.25 | | 0.9 | | |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 4.2 | | 3.4 | 8.8 | | 2.4 | | |
| $I_{OH}$ | HIGH Level Output Current (Note 4) | $V_{DD}$ = 5V, $V_O$ = 4.6V | −0.64 | | −0.51 | −0.88 | | −0.36 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 9.5V | −1.6 | | −1.3 | −2.25 | | −0.9 | | |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | −4.2 | | −3.4 | −8.8 | | −2.4 | | |
| $I_{IN}$ | Input Current | $V_{DD}$ = 15V, $V_{IN}$ = 0V | | −0.1 | | $-10^{-5}$ | −0.1 | | −1.0 | µA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = 15V | | 0.1 | | $10^{-5}$ | 0.1 | | 1.0 | |

Note 4: $I_{OH}$ and $I_{OL}$ are measured one output at a time.

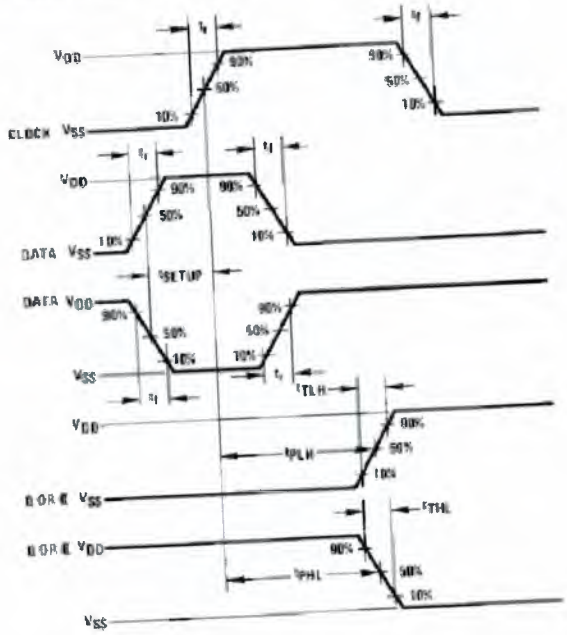
## AC Electrical Characteristics (Note 5)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, unless otherwise noted

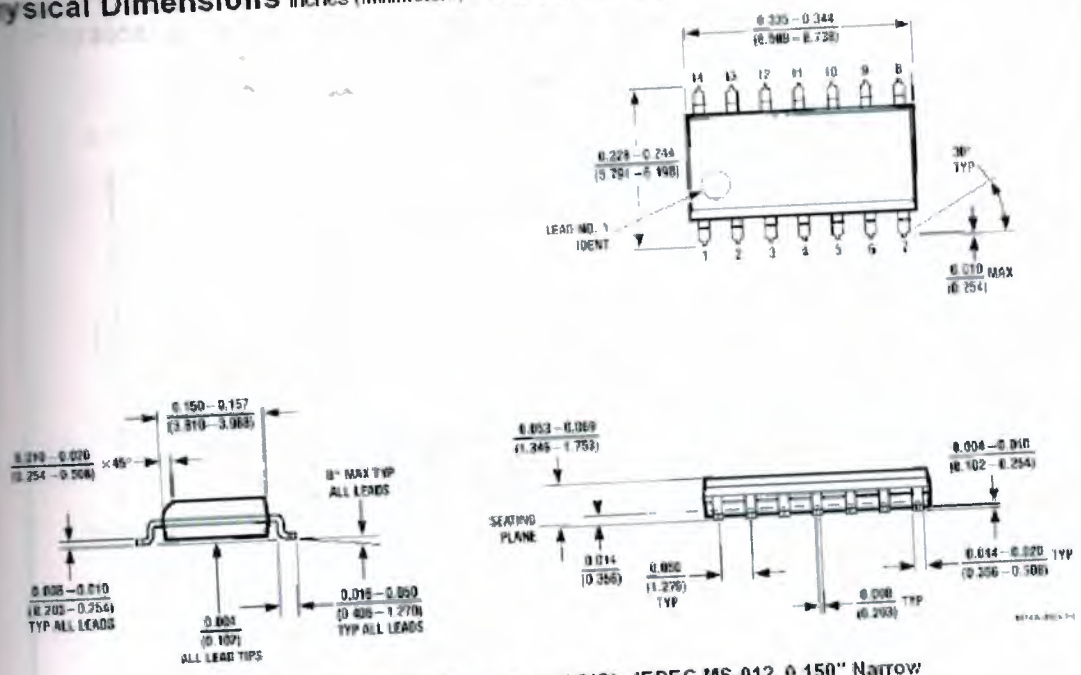
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CLOCK OPERATION** | | | | | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | $V_{DD} = 5V$ | | 200 | 350 | ns |
| | | $V_{DD} = 10V$ | | 80 | 160 | |
| | | $V_{DD} = 15V$ | | 65 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | $V_{DD} = 5V$ | | 100 | 200 | ns |
| | | $V_{DD} = 10V$ | | 50 | 100 | |
| | | $V_{DD} = 15V$ | | 40 | 80 | |
| $t_{WL}$, $t_{WH}$ | Minimum Clock Pulse Width | $V_{DD} = 5V$ | | 100 | 200 | ns |
| | | $V_{DD} = 10V$ | | 40 | 80 | |
| | | $V_{DD} = 15V$ | | 32 | 65 | |
| $t_{RCL}$, $t_{FCL}$ | Maximum Clock Rise and Fall Time | $V_{DD} = 5V$ | | | 15 | μs |
| | | $V_{DD} = 10V$ | | | 10 | |
| | | $V_{DD} = 15V$ | | | 5 | |
| $t_{SU}$ | Minimum Set-Up Time | $V_{DD} = 5V$ | | 20 | 40 | ns |
| | | $V_{DD} = 10V$ | | 15 | 30 | |
| | | $V_{DD} = 15V$ | | 12 | 25 | |
| $f_{CL}$ | Maximum Clock Frequency | $V_{DD} = 5V$ | 2.5 | 5 | | MHz |
| | | $V_{DD} = 10V$ | 6.2 | 12.5 | | |
| | | $V_{DD} = 15V$ | 7.6 | 15.5 | | |
| **SET AND RESET OPERATION** | | | | | | |
| $t_{PHL(R)}$, $t_{PLH(S)}$ | Propagation Delay Time | $V_{DD} = 5V$ | | 150 | 300 | ns |
| | | $V_{DD} = 10V$ | | 65 | 130 | |
| | | $V_{DD} = 15V$ | | 45 | 90 | |
| $t_{WH(R)}$, $t_{WH(S)}$ | Minimum Set and Reset Pulse Width | $V_{DD} = 5V$ | | 90 | 180 | ns |
| | | $V_{DD} = 10V$ | | 40 | 80 | |
| | | $V_{DD} = 15V$ | | 25 | 50 | |
| $C_{IN}$ | Average Input Capacitance | Any Input | | 5 | 7.5 | pF |

Note 5: AC Parameters are guaranteed by DC correlated testing.

## Switching Time Waveforms

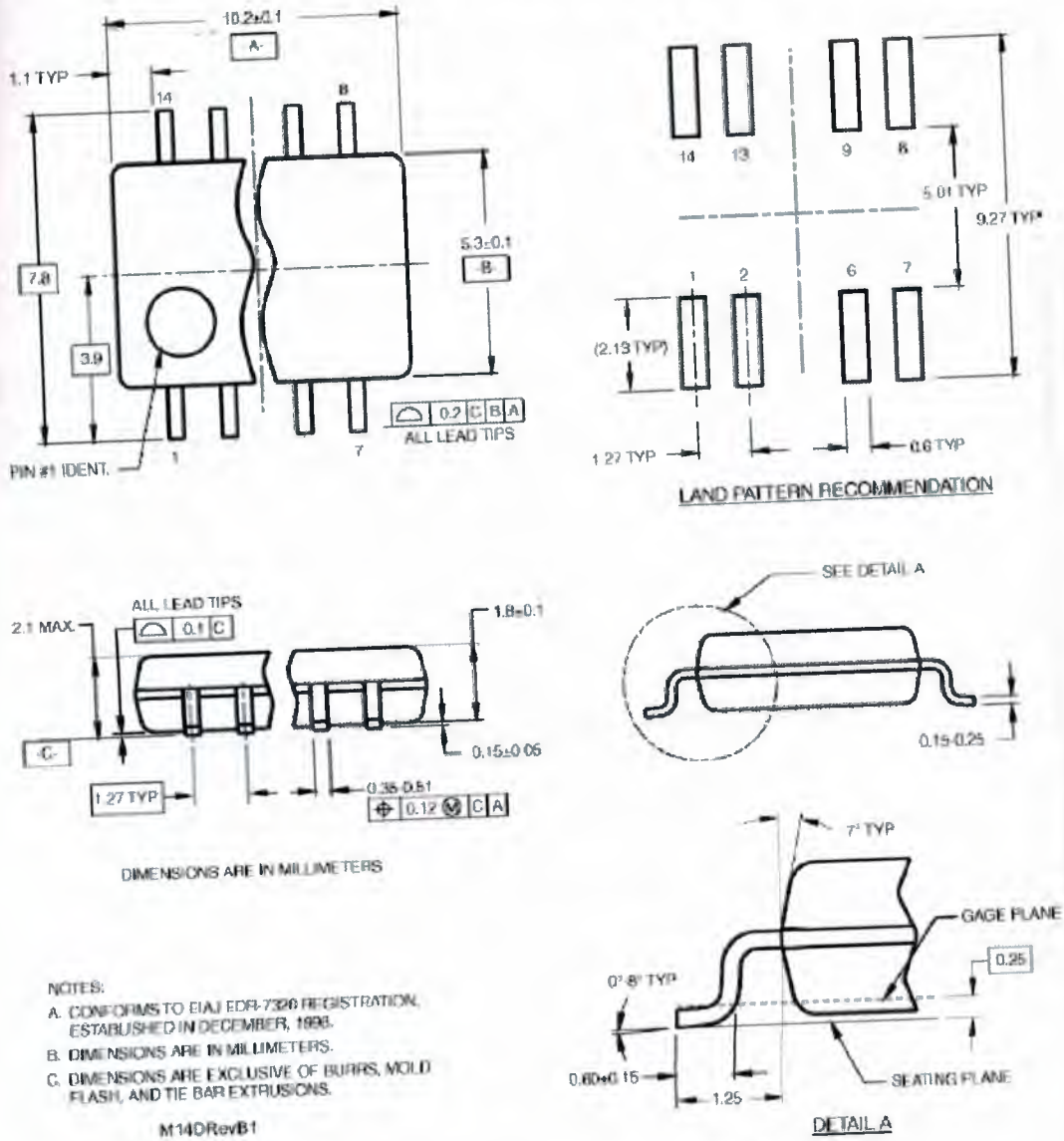


## Physical Dimensions inches (millimeters) unless otherwise noted




14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

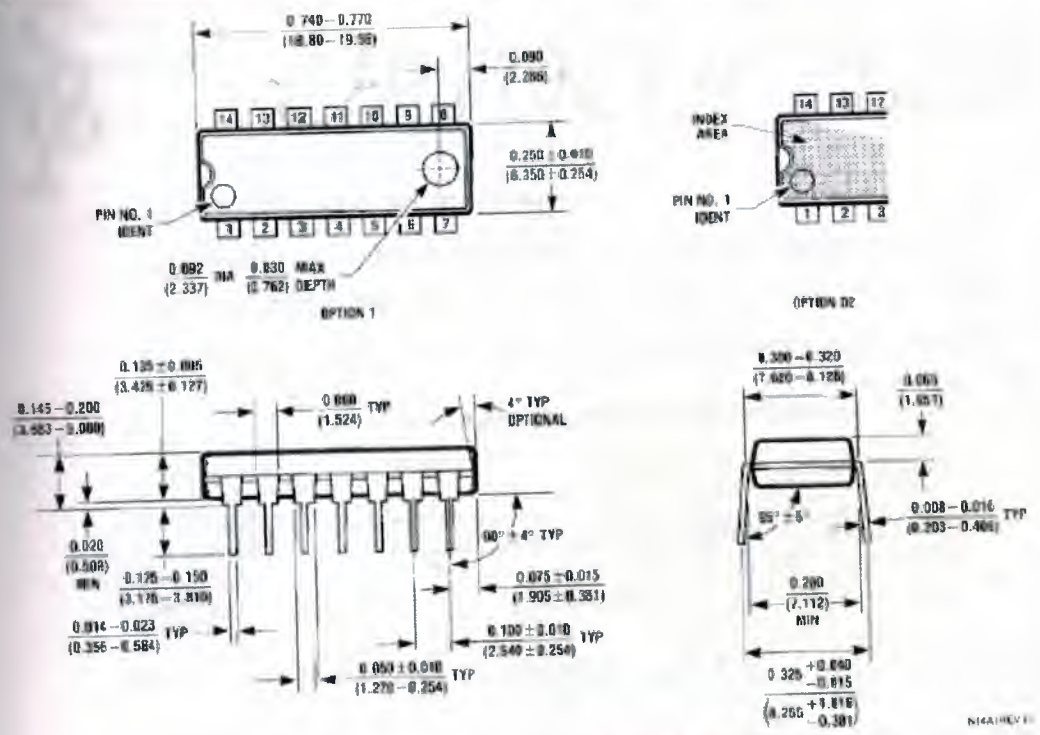
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N14A**

# SMALL OUTLINE PACKAGE OPTOCOUPLERS

Size does matter, but bigger isn't always better.

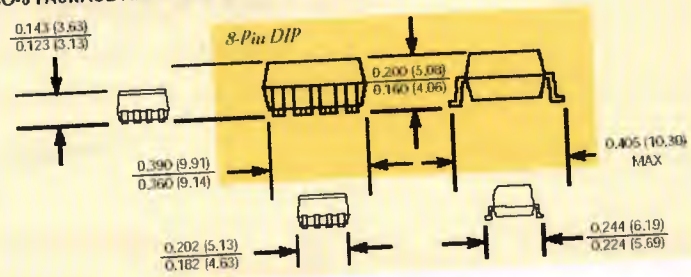
Portable and compact devices require optocouplers that deliver the performance of a standard 4- or 8-pin dual inline package (DIP), but occupy only a fraction of the space.

Fairchild Semiconductor's small outline package (SOP) optocouplers meet that need.

All dimensions are in inches (millimeters)

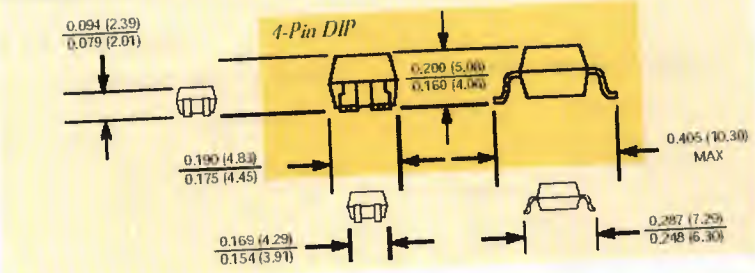
*SO-8 Package*

**AN SO-8 PACKAGE HAS A 69% SMALLER FOOTPRINT THAN AN 8-PIN DIP**



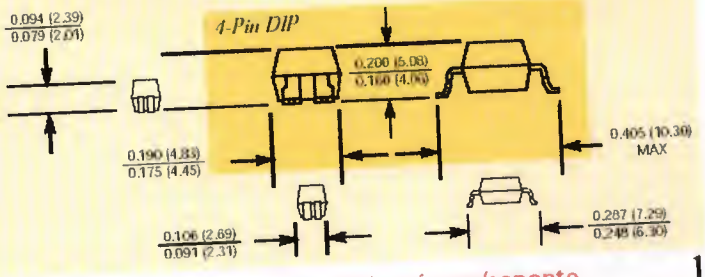

*Full-Pitch Mini-Flat Package*

**A FULL-PITCH MINI-FLAT PACKAGE HAS A 37% SMALLER FOOTPRINT THAN A 4-PIN DIP**




*Half-Pitch Mini-Flat Package*

**A HALF-PITCH MINI-FLAT PACKAGE HAS A 61% SMALLER FOOTPRINT THAN A 4-PIN DIP**

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For more information, including data sheets, go to www.fairchildsemi.com/sopopto

## *SO-8 Package Optocouplers*

High-Speed (1 Mbit/s ) Transistor Output, GaAsP Input Optocoupler
High-Speed (10 Mbit/s ) Logic Gate Output, GaAsP Input Optocoupler
High-Gain (>300% CTR) Split Darlington Output, GaAsP Input Optocoupler
Phototransistor Output, GaAs Input Optocoupler
Photodarlington Output, GaAs Input Optocoupler
Transistor Output, AC GaAs Input Optocoupler
Dual-Channel Phototransistor Output, GaAs Input Optocoupler
Dual-Channel Photodarlington Output, GaAs Input Optocoupler

## *Full- and Half-Pitch Mini-Flat Package Optocouplers*

Phototransistor Output, GaAs Input Optocoupler
Phototransistor Output, AC GaAs Input Optocoupler

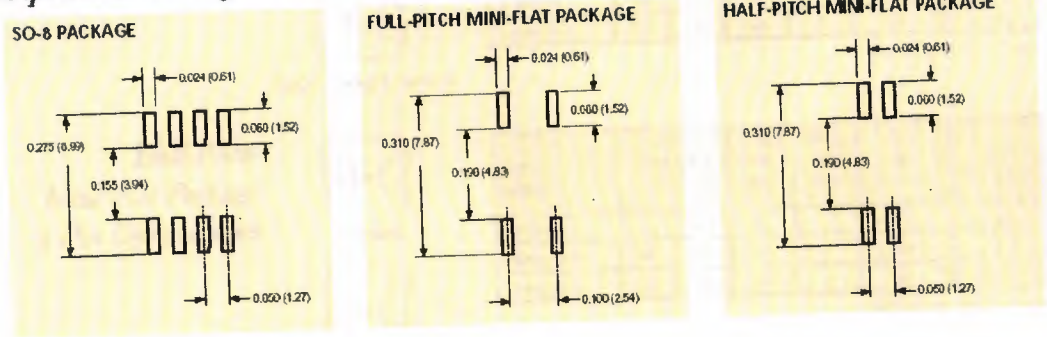
## *Safety Regulatory Agency Approvals*

BSI, CSA and UL certified.

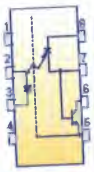
## *Tape and Reel Ordering Information*

Option R1 – 500 devices per reel, 7 inch (178 mm) reel diameter
Option R2 – 2,500 devices per reel, 13 inch (330 mm) reel diameter

## *Footprint Drawings for PCB Layout*



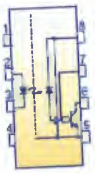
## *SO-8 Package High Speed Transistor Output Optocouplers*



*Base not connected for HCPL-0452

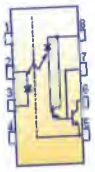
| Part Number | CTR @ 16 mA $I_F$ (%) min | CTR @ 16 mA $I_F$ (%) max | $V_{OL}$ (V) max | $I_{CC}$ (µA) max | $T_{PHL}/T_{PLH}$ (µs) max | $V_{ISO}$ AC [RMS] |
|---|---|---|---|---|---|---|
| HCPL-0452* | 19 | 50 | 0.4 | 200 | 0.8/0.8 | 2.5 kV |
| HCPL-0500 | 7 | 50 | 0.4 | 200 | 1.5/1.5 | 2.5 kV |
| HCPL-0501 | 19 | 50 | 0.4 | 200 | 0.8/0.8 | 2.5 kV |

## *SO-8 Package High Speed Logic Gate Optocouplers*



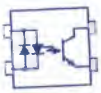
| Part Number | $I_{FT}$ (mA) max | $V_{OL}$ (V) max | $CM_H/CM_L$ (KV/µs) min | $I_{CC}$ (mA) max | $T_{PHL}/T_{PLH}$ (ns) max | $V_{ISO}$ AC [RMS] |
|---|---|---|---|---|---|---|
| HCPL-0600 | 5 | 0.6 | — | 13 | 75/75 | 2.5 kV |
| HCPL-0601 | 5 | 0.6 | 5 | 13 | 75/75 | 2.5 kV |

## *SO-8 Package High Gain Split Darlington Optocouplers*



| Part Number | CTR @ 1.6 mA $I_F$ (%) min | CTR @ 1.6 mA $I_F$ (%) max | $V_{OL}$ (V) max | $I_{OH}$ (µA) max | $T_{PHL}/T_{PLH}$ (µs) max | $V_{ISO}$ AC [RMS] |
|---|---|---|---|---|---|---|
| HCPL-0700 | 300 | 2600 | 0.4 | 250 | 10/35 | 2.5 kV |
| HCPL-0701 | 500 | 2600 | 0.4 | 100 | 25/60 | 2.5 kV |

## *Full-Pitch Mini-Flat Package 4-Pin Optocouplers*



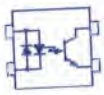
HMAA2705

HMA121, HMA124, HMA2701

| Part Number | CTR @ 5 mA $I_F$ (%) min | CTR @ 5 mA $I_F$ (%) max | $BV_{CEO}$ (V) min | $BV_{ECO}$ (V) min | $t_R/t_F$ (µs) typical | $V_{ISO}$ AC [RMS] |
|---|---|---|---|---|---|---|
| HMA121 | 50 | 600 | 80 | 7 | 3/3 | 3.75 kV |
| HMA124 | 100 | 1200 | 80 | 7 | 3/3 | 3.75 kV |
| HMA2701 | 50 | 300 | 40 | 7 | 3/3 | 3.75 kV |
| HMAA2705 | 50* | 300* | 40 | 7 | 3/3 | 3.75 kV |

*CTR measured at $I_F$ = ±5 mA

## *Half-Pitch Mini-Flat Package 4-Pin Optocouplers*



HMHAA280

HMHA281, HMHA2801

| Part Number | CTR @ 5 mA $I_F$ (%) min | CTR @ 5 mA $I_F$ (%) max | $BV_{CEO}$ (V) min | $BV_{ECO}$ (V) min | $t_R/t_F$ (µs) typical | $V_{ISO}$ AC [RMS] |
|---|---|---|---|---|---|---|
| HMHA281 | 50 | 600 | 80 | 7 | 3/3 | 2.5 kV |
| HMHAA280 | 50* | 600* | 80 | 7 | 3/3 | 2.5 kV |
| HMHA2801 | 80 | 600 | 80 | 7 | 3/3 | 2.5 kV |

*CTR measured at $I_F$ = ±5 mA

## *SO-8 Package*
## *Phototransistor Output*
## *GaAs Input*
## *Optocouplers*

| Part Number | CTR* 10 mA $I_F$ (%) min | CTR* 10 mA $I_F$ (%) max | $BV_{CEO}$ (V) min | $BV_{ECO}$ (V) min | $t_{ON}/t_{OFF}$ (µs) typical | $V_{ISO}$ AC (RMS) |
|---|---|---|---|---|---|---|
| MOC205 | 40 | 80 | 70 | 7 | 3.0/2.8 | 3.0 kV |
| MOC206 | 63 | 125 | 70 | 7 | 3.0/2.8 | 3.0 kV |
| MOC207 | 100 | 200 | 70 | 7 | 3.0/2.8 | 3.0 kV |
| MOC208 | 40 | 125 | 70 | 7 | 3.0/2.8 | 3.0 kV |
| MOC211 | 20 | — | 30 | 7 | 7.5/5.7 | 3.0 kV |
| MOC212 | 50 | — | 30 | 7 | 7.5/5.7 | 3.0 kV |
| MOC213 | 100 | — | 30 | 7 | 7.5/5.7 | 3.0 kV |
| MOC215 | 20* | — | 30 | 7 | 7.5/5.7 | 3.0 kV |
| MOC216 | 50* | — | 30 | 7 | 7.5/5.7 | 3.0 kV |
| MOC217 | 100* | — | 30 | 7 | 7.5/5.7 | 3.0 kV |

*CTR measured at $I_F$ = 1 mA

## *SO-8 Package*
## *Photodarlington Output*
## *GaAs Input*
## *Optocoupler*

| Part Number | CTR* 1 mA $I_F$ (%) min | CTR* 1 mA $I_F$ (%) max | $BV_{CEO}$ (V) min | $BV_{ECO}$ (V) min | $t_{ON}/t_{OFF}$ (µs) typical | $V_{ISO}$ AC (RMS) |
|---|---|---|---|---|---|---|
| MOC223 | 500 | — | 30 | 7 | 3.5/95.0 | 3.0 kV |

## *SO-8 Package*
## *Transistor Output*
## *AC Input*
## *Optocoupler*

| Part Number | CTR* ±10 mA $I_F$ (%) min | CTR* ±10 mA $I_F$ (%) max | $BV_{CEO}$ (V) min | $BV_{ECO}$ (V) min | $t_{ON}/t_{OFF}$ (µs) typical | $V_{ISO}$ AC (RMS) |
|---|---|---|---|---|---|---|
| MOC256 | 20 | — | 30 | 5 | — | 3.0 kV |

## *SO-8 Package*
## *Dual Channel*
## *Phototransistor Output*
## *GaAs Input*
## *Optocouplers*

| Part Number | CTR* 10 mA $I_F$ (%) min | CTR* 10 mA $I_F$ (%) max | $BV_{CEO}$ (V) min | $BV_{ECO}$ (V) min | $t_{ON}/t_{OFF}$ (µs) typical | $V_{ISO}$ AC (RMS) |
|---|---|---|---|---|---|---|
| MOCD207 | 100 | 200 | 70 | 7 | 3.0/2.8 | 3.0 kV |
| MOCD208 | 40 | 125 | 70 | 7 | 3.0/2.8 | 3.0 kV |
| MOCD211 | 20 | — | 30 | 7 | 7.5/5.7 | 3.0 kV |
| MOCD213 | 100 | — | 30 | 7 | 3.0/2.8 | 3.0 kV |
| MOCD217 | 100* | — | 30 | 7 | 7.5/5.7 | 3.0 kV |

*CTR measured at $I_F$ = 1 mA

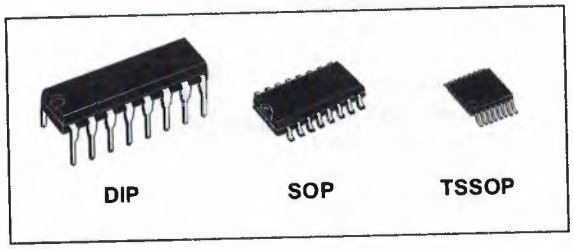
## *SO-8 Package*
## *Dual Channel*
## *Photodarlington Output*
## *GaAs Input*
## *Optocoupler*

| Part Number | CTR* 1 mA $I_F$ (%) min | CTR* 1 mA $I_F$ (%) max | $BV_{CEO}$ (V) min | $BV_{ECO}$ (V) min | $t_{ON}/t_{OFF}$ (µs) typical | $V_{ISO}$ AC (RMS) |
|---|---|---|---|---|---|---|
| MOCD223 | 500 | — | 30 | 7 | 3.5/95.0 | 3.0 kV |

# M74HC192

## SYNCHRONOUS UP/DOWN DECADE COUNTER

- HIGH SPEED :
  $f_{MAX}$ = 55 MHz (TYP.) at $V_{CC}$ = 6V
- LOW POWER DISSIPATION:
  $I_{CC}$ =4μA(MAX.) at $T_A$=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % $V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  $V_{CC}$ (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 192



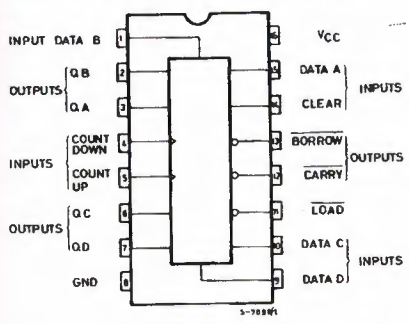

**ORDER CODES**

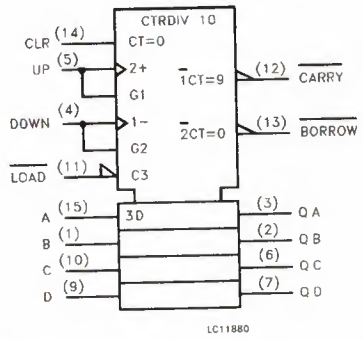
| PACKAGE | TUBE | T & R |
|---|---|---|
| DIP | M74HC192B1R | |
| SOP | M74HC192M1R | M74HC192RM13TR |
| TSSOP | | M74HC192TTR |

### DESCRIPTION

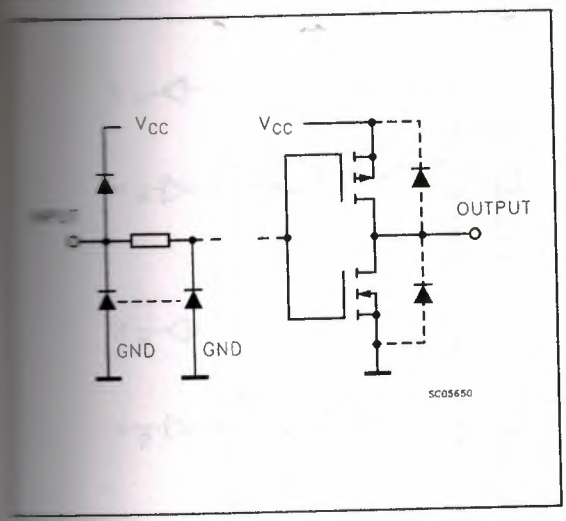
The M74HC192 is an high speed CMOS SYNCRONOUS UP/DOWN DECADE COUNTERS fabricated with silicon gate $C^2MOS$ technology.
The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to low independently of either COUNT input. Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counters overflows. The counter can be cascaded by connection the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



## INPUT AND OUTPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

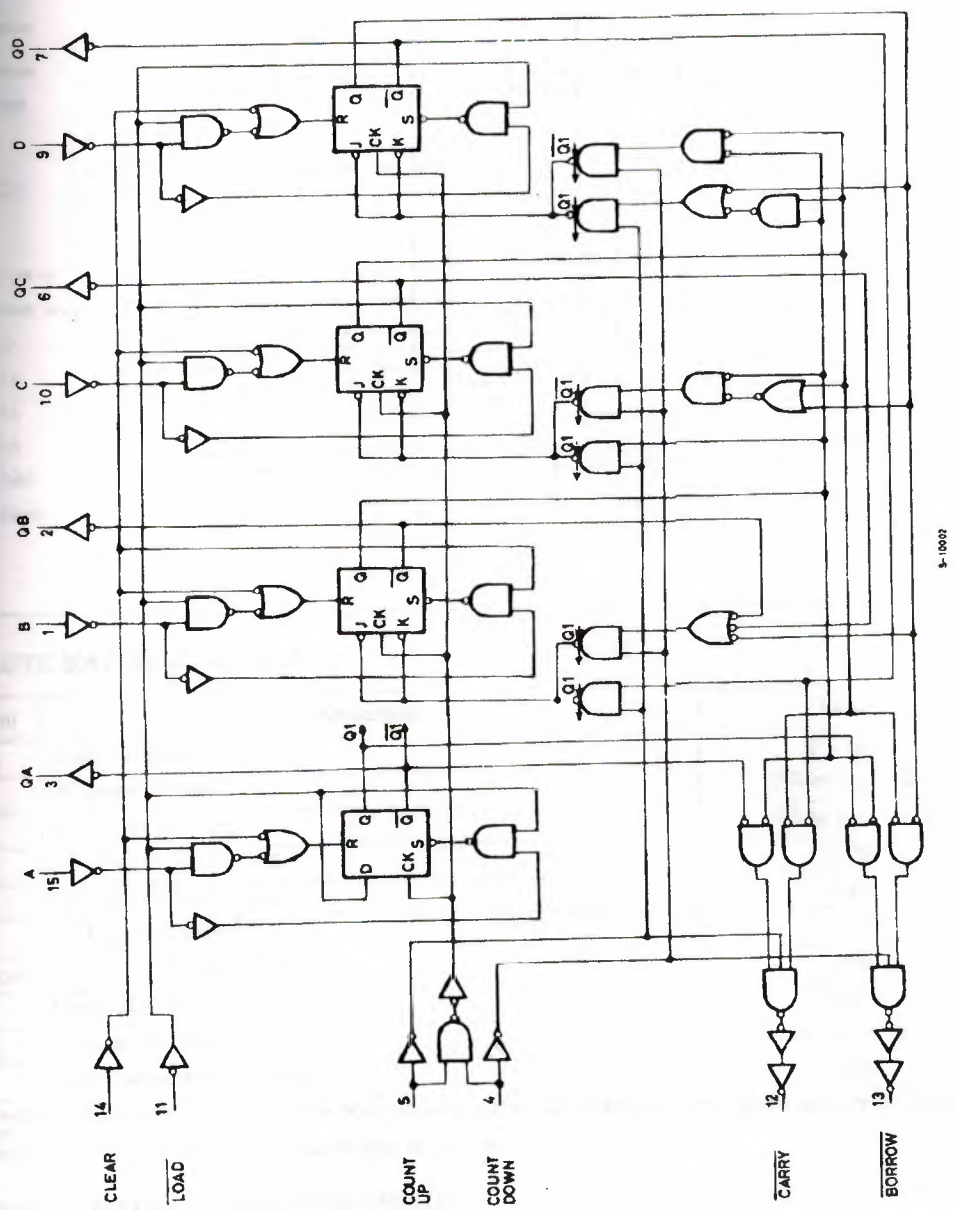
| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 3, 2, 6, 7 | QA to QD | Flip-Flop Outputs |
| 4 | COUNT DOWN | Count Down Clock Input |
| 5 | COUNT UP | Count Up Clock Input |
| 11 | $\overline{\text{LOAD}}$ | Asynchronous Parallel Load Input (Active LOW) |
| 12 | $\overline{\text{CARRY}}$ | Count Up (Carry) Output (Active LOW) |
| 13 | $\overline{\text{BORROW}}$ | Count Down (Borrow) Output (Active LOW) |
| 14 | CLEAR | Asynchronous Reset Input (Active High) |
| 15, 1, 10, 9 | A to D | Data Inputs |
| 8 | GND | Ground (0V) |
| 16 | Vcc | Positive Supply Voltage |

## TRUTH TABLE

| COUNT UP | COUNT DOWN | $\overline{\text{LOAD}}$ | CLEAR | FUNCTION |
|---|---|---|---|---|
| ⎍ | H | H | L | COUNT UP |
| ⎎ | H | H | L | NO COUNT |
| H | ⎍ | H | L | COUNT DOWN |
| H | ⎎ | H | L | NO COUNT |
| X | X | L | L | PRESET |
| X | X | X | H | RESET |

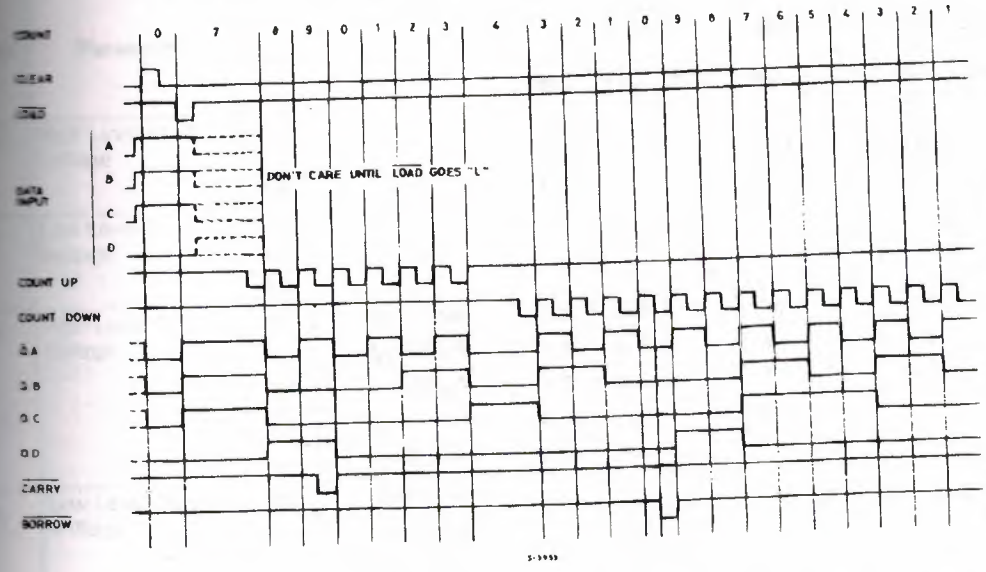
X : Don't Care

## LOGIC DIAGRAM




This logic diagram has not be used to estimate propagation delays

## TIMING CHART




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 to +7 | V |
| $V_I$ | DC Input Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Current | ± 25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 50 | mA |
| $P_D$ | Power Dissipation | 500(*) | mW |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2 to 6 | V |
| $V_I$ | Input Voltage | | 0 to $V_{CC}$ | V |
| $V_O$ | Output Voltage | | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating Temperature | | -55 to 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 2.0V | 0 to 1000 | ns |
| | | $V_{CC}$ = 4.5V | 0 to 500 | ns |
| | | $V_{CC}$ = 6.0V | 0 to 400 | ns |

## DC SPECIFICATIONS

| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | $V_{CC}$ (V) | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | 1.5 | | V |
| | | 4.5 | | 3.15 | | | 3.15 | | 3.15 | | |
| | | 6.0 | | 4.2 | | | 4.2 | | 4.2 | | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | | 0.5 | V |
| | | 4.5 | | | | 1.35 | | 1.35 | | 1.35 | |
| | | 6.0 | | | | 1.8 | | 1.8 | | 1.8 | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $I_O$=-20 µA | 1.9 | 2.0 | | 1.9 | | 1.9 | | V |
| | | 4.5 | $I_O$=-20 µA | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | 6.0 | $I_O$=-20 µA | 5.9 | 6.0 | | 5.9 | | 5.9 | | |
| | | 4.5 | $I_O$=-4.0 mA | 4.18 | 4.31 | | 4.13 | | 4.10 | | |
| | | 6.0 | $I_O$=-5.2 mA | 5.68 | 5.8 | | 5.63 | | 5.60 | | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $I_O$=20 µA | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | 4.5 | $I_O$=20 µA | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 6.0 | $I_O$=20 µA | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 | $I_O$=4.0 mA | | 0.17 | 0.26 | | 0.33 | | 0.40 | |
| | | 6.0 | $I_O$=5.2 mA | | 0.18 | 0.26 | | 0.33 | | 0.40 | |
| $I_I$ | Input Leakage Current | 6.0 | $V_I$ = $V_{CC}$ or GND | | | ± 0.1 | | ± 1 | | ± 1 | µA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_I$ = $V_{CC}$ or GND | | | 4 | | 40 | | 80 | µA |

**ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6ns)

| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 2.0 | | | 30 | 75 | | 95 | | 110 | ns |
| | | 4.5 | | | 8 | 15 | | 19 | | 22 | |
| | | 6.0 | | | 7 | 13 | | 16 | | 19 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (COUNT UP, DOWN - Q) | 2.0 | | | 65 | 190 | | 240 | | 285 | ns |
| | | 4.5 | | | 20 | 38 | | 48 | | 57 | |
| | | 6.0 | | | 16 | 32 | | 41 | | 48 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (COUNT UP - $\overline{CARRY}$) | 2.0 | | | 40 | 130 | | 165 | | 195 | ns |
| | | 4.5 | | | 13 | 26 | | 33 | | 39 | |
| | | 6.0 | | | 11 | 22 | | 28 | | 33 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (COUNT DOWN - $\overline{BORROW}$) | 2.0 | | | 40 | 130 | | 165 | | 195 | ns |
| | | 4.5 | | | 13 | 26 | | 33 | | 39 | |
| | | 6.0 | | | 11 | 22 | | 28 | | 33 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (LOAD - Q) | 2.0 | | | 85 | 220 | | 275 | | 330 | ns |
| | | 4.5 | | | 25 | 44 | | 55 | | 66 | |
| | | 6.0 | | | 20 | 37 | | 47 | | 56 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (LOAD - $\overline{CARRY}$) | 2.0 | | | 110 | 250 | | 315 | | 375 | ns |
| | | 4.5 | | | 30 | 50 | | 63 | | 75 | |
| | | 6.0 | | | 25 | 43 | | 54 | | 64 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (LOAD - $\overline{BORROW}$) | 2.0 | | | 110 | 250 | | 315 | | 375 | ns |
| | | 4.5 | | | 31 | 50 | | 63 | | 75 | |
| | | 6.0 | | | 25 | 43 | | 54 | | 64 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (DATA - Q) | 2.0 | | | 80 | 190 | | 240 | | 285 | ns |
| | | 4.5 | | | 25 | 38 | | 48 | | 57 | |
| | | 6.0 | | | 20 | 32 | | 41 | | 48 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (DATA - $\overline{CARRY}$) | 2.0 | | | 120 | 250 | | 315 | | 375 | ns |
| | | 4.5 | | | 34 | 50 | | 63 | | 75 | |
| | | 6.0 | | | 28 | 43 | | 54 | | 64 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (DATA - $\overline{BORROW}$) | 2.0 | | | 110 | 250 | | 315 | | 375 | ns |
| | | 4.5 | | | 30 | 50 | | 63 | | 75 | |
| | | 6.0 | | | 25 | 43 | | 54 | | 64 | |
| $t_{PHL}$ | Propagation Delay Time (CLEAR -Q) | 2.0 | | | 100 | 225 | | 280 | | 340 | ns |
| | | 4.5 | | | 30 | 45 | | 56 | | 68 | |
| | | 6.0 | | | 25 | 38 | | 48 | | 58 | |
| $t_{PLH}$ | Propagation Delay Time (CLEAR -CARRY) | 2.0 | | | 120 | 250 | | 315 | | 375 | ns |
| | | 4.5 | | | 35 | 50 | | 63 | | 75 | |
| | | 6.0 | | | 29 | 43 | | 54 | | 64 | |
| $t_{PHL}$ | Propagation Delay Time (CLEAR - $\overline{BORROW}$) | 2.0 | | | 120 | 250 | | 315 | | 375 | ns |
| | | 4.5 | | | 35 | 50 | | 63 | | 75 | |
| | | 6.0 | | | 29 | 43 | | 54 | | 64 | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.0 | | 5 | 12 | | 4 | | 3.4 | | MHz |
| | | 4.5 | | 25 | 48 | | 20 | | 17 | | |
| | | 6.0 | | 30 | 55 | | 24 | | 20 | | |

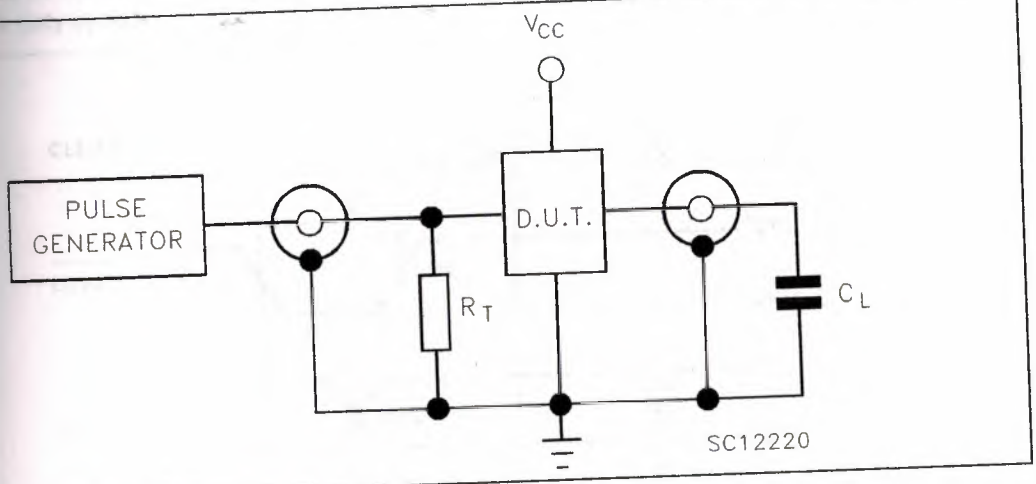
| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | $V_{CC}$ (V) | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| | Minimum Pulse Width (COUNT UP/ DOWN) | 2.0 | | | 34 | 100 | | 125 | | 150 | ns |
| | | 4.5 | | | 9 | 20 | | 25 | | 30 | |
| | | 6.0 | | | 7 | 17 | | 21 | | 26 | |
| | Minimum Pulse Width (LOAD) | 2.0 | | | 34 | 75 | | 95 | | 110 | ns |
| | | 4.5 | | | 9 | 15 | | 19 | | 22 | |
| | | 6.0 | | | 7 | 13 | | 16 | | 19 | |
| | Minimum Pulse Width (CLEAR) | 2.0 | | | 40 | 100 | | 125 | | 150 | ns |
| | | 4.5 | | | 12 | 20 | | 25 | | 30 | |
| | | 6.0 | | | 10 | 17 | | 21 | | 26 | |
| | Minimum Set-up Time(DATA -LOAD) | 2.0 | | | 30 | 75 | | 95 | | 110 | ns |
| | | 4.5 | | | 9 | 15 | | 19 | | 22 | |
| | | 6.0 | | | 7 | 13 | | 16 | | 19 | |
| | Minimum Hold Time | 2.0 | | | | 0 | | 0 | | 0 | ns |
| | | 4.5 | | | | 0 | | 0 | | 0 | |
| | | 6.0 | | | | 0 | | 0 | | 0 | |
| | Minimum Removal Time (LOAD) | 2.0 | | | 6 | 50 | | 65 | | 75 | ns |
| | | 4.5 | | | 2 | 10 | | 13 | | 15 | |
| | | 6.0 | | | 2 | 9 | | 11 | | 13 | |
| | Minimum Removal Time (CLEAR) | 2.0 | | | 14 | 50 | | 65 | | 75 | ns |
| | | 4.5 | | | 4 | 10 | | 13 | | 15 | |
| | | 6.0 | | | 3 | 9 | | 11 | | 13 | |

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | $V_{CC}$ (V) | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $C_{IN}$ | Input Capacitance | 5.0 | | | 5 | 10 | | 10 | | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (note 1) | 5.0 | | | 68 | | | | | | pF |

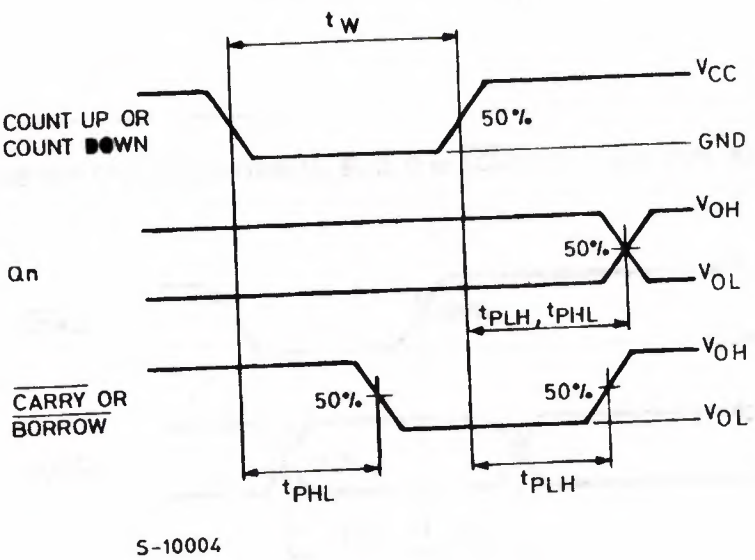
1) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT

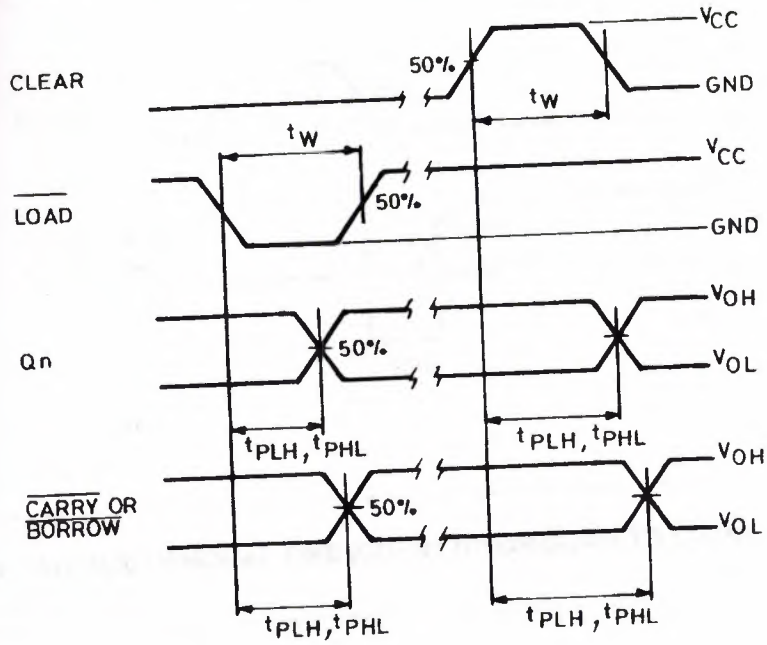



$C_L$ =50pF or equivalent (includes jig and probe capacitance)
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)

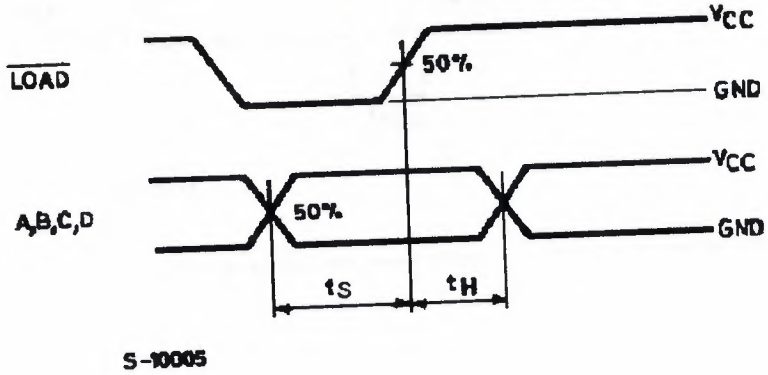
**WAVEFORM 1 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (COUNT UP AND DOWN)**
(f=1MHz; 50% duty cycle)



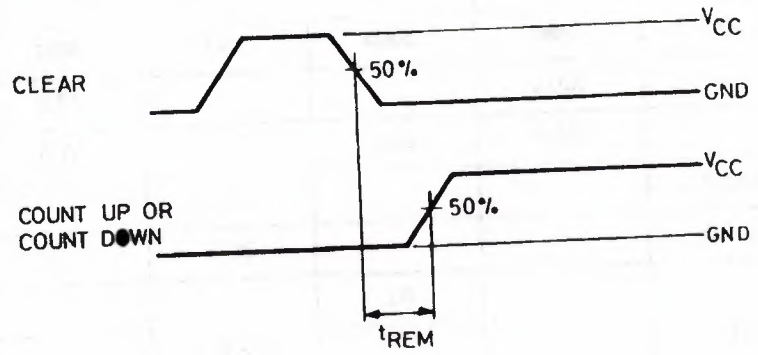
**WAVEFORM 2 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (CLEAR, $\overline{LOAD}$)**
(f=1MHz; 50% duty cycle)



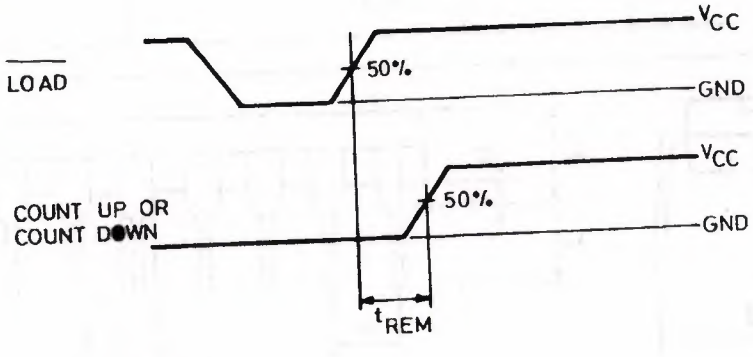

**WAVEFORM 3 : SETUP AND HOLD TIME (A, B, C, D to $\overline{LOAD}$)** (f=1MHz; 50% duty cycle)



**WAVEFORM 4: MINIMUM REMOVAL TIME (COUNT UP OR DOWN TO CLEAR)**
(f=1MHz; 50% duty cycle)

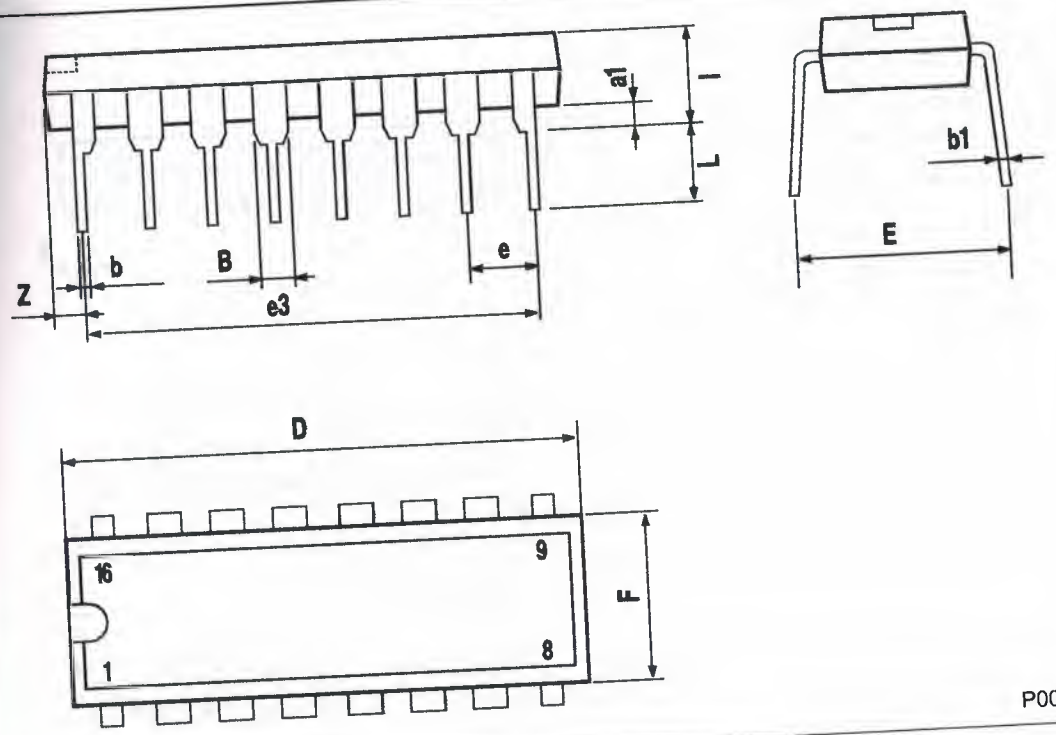



**WAVEFORM 5 : MINIMUM REMOVAL TIME (COUNT UP OR DOWN TO $\overline{LOAD}$)**
(f=1MHz; 50% duty cycle)



## Plastic DIP-16 (0.25) MECHANICAL DATA

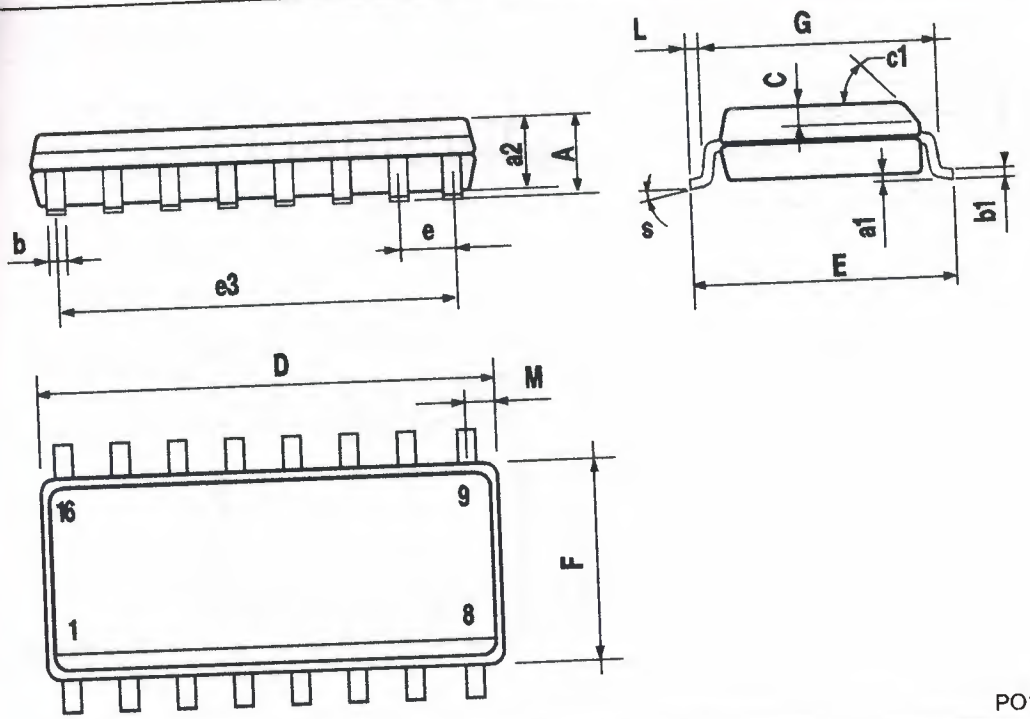
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |




P001C

## SO-16 MECHANICAL DATA

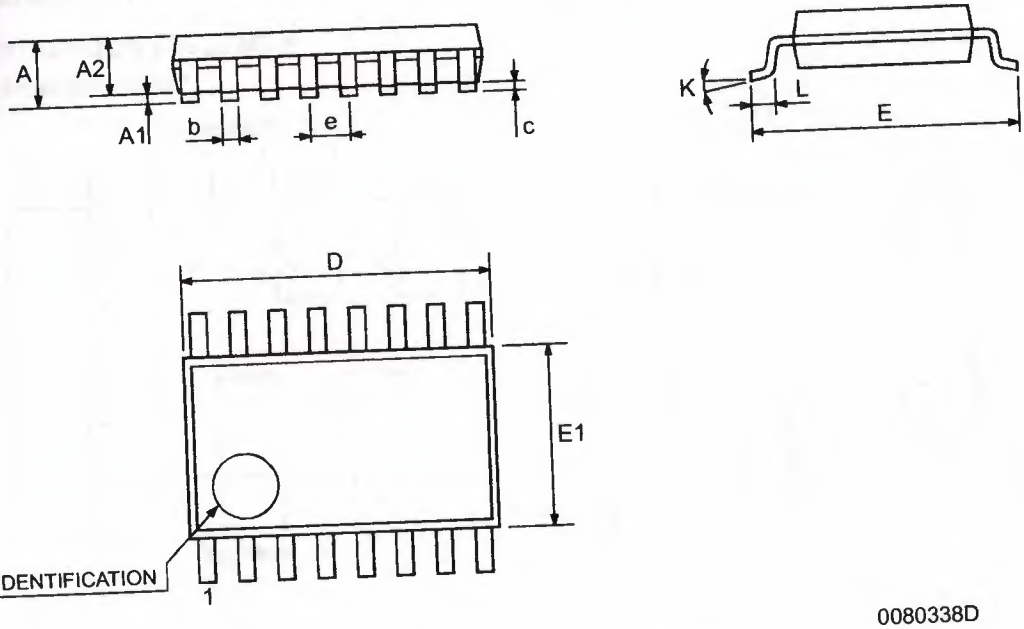
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.2 | 0.003 | | 0.007 |
| a2 | | | 1.65 | | | 0.064 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |




PO13H

## TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



FAIRCHILD SEMICONDUCTOR™

October 1987
Revised April 2002

# CD4049UBC • CD4050BC
# Hex Inverting Buffer • Hex Non-Inverting Buffer

## General Description

The CD4049UBC and CD4050BC hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage ($V_{DD}$). The input signal high level ($V_{IH}$) can exceed the $V_{DD}$ supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at $V_{DD}$ = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

## Features

- Wide supply voltage range: 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than $V_{DD}$

## Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS HIGH-to-LOW logic level converter

## Ordering Code:

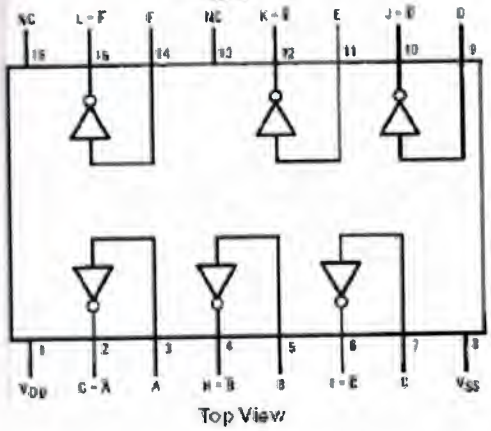
| Order Number | Package Number | Package Description |
|---|---|---|
| CD4049UBCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4049UBCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| CD4050BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4050BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagrams

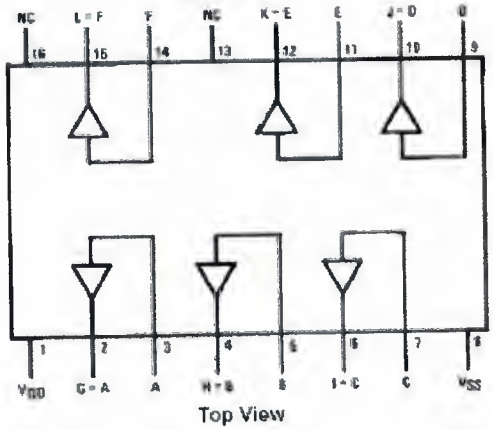
Pin Assignments for DIP

CD4049UBC




Top View

CD4050BC

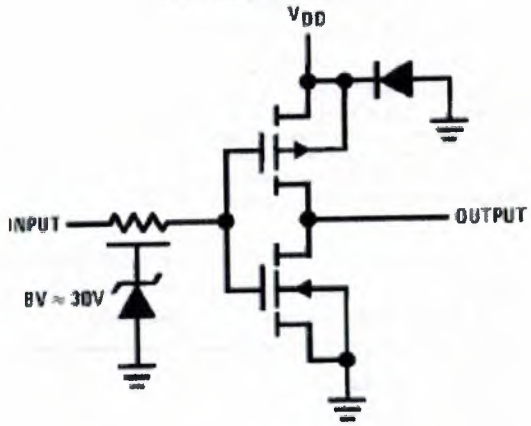



Top View

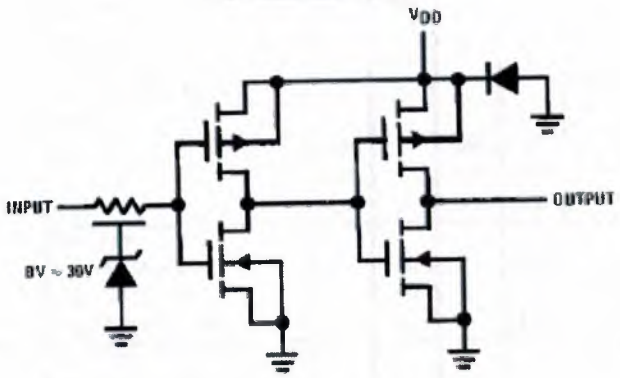
 

## Schematic Diagrams

CD4049UBC
1 of 6 Identical Units




CD4050BC
1 of 6 Identical Units



## Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | −0.5V to +18V |
| Input Voltage ($V_{IN}$) | −0.5V to +18V |
| Voltage at Any Output Pin ($V_{OUT}$) | −0.5V to $V_{DD}$ + 0.5V |
| Storage Temperature Range ($T_S$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |

## Recommended Operating Conditions (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | 3V to 15V |
| Input Voltage ($V_{IN}$) | 0V to 15V |
| Voltage at Any Output Pin ($V_{OUT}$) | 0 to $V_{DD}$ |
| Operating Temperature Range ($T_A$) | |
| CD4049UBC, CD4050BC | −55°C to +125°C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS}$ = 0V unless otherwise specified.

## DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | −55°C | | +25°C | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}$ = 5V | | 1.0 | | 0.01 | 1.0 | | 30 | µA |
| | | $V_{DD}$ = 10V | | 2.0 | | 0.01 | 2.0 | | 60 | |
| | | $V_{DD}$ = 15V | | 4.0 | | 0.03 | 4.0 | | 120 | |
| $V_{OL}$ | LOW Level Output Voltage | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V, $\|I_O\|$ < 1 µA | | | | | | | | |
| | | $V_{DD}$ = 5V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 10V | | 0.05 | | 0 | 0.05 | | 0.05 | |
| | | $V_{DD}$ = 15V | | 0.05 | | 0 | 0.05 | | 0.05 | |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V, $\|I_O\|$ < 1 µA | | | | | | | | |
| | | $V_{DD}$ = 5V | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD}$ = 10V | 9.95 | | 9.95 | 10 | | 9.95 | | |
| | | $V_{DD}$ = 15V | 14.95 | | 14.95 | 15 | | 14.95 | | |
| $V_{IL}$ | LOW Level Input Voltage (CD4050BC Only) | $\|I_O\|$ < 1 µA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 0.5V | | 1.5 | | 2.25 | 1.5 | | 1.5 | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1V | | 3.0 | | 4.5 | 3.0 | | 3.0 | |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | | 4.0 | | 6.75 | 4.0 | | 4.0 | |
| $V_{IL}$ | LOW Level Input Voltage (CD4049UBC Only) | $\|I_O\|$ < 1 µA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 4.5V | | 1.0 | | 1.5 | 1.0 | | 1.0 | V |
| | | $V_{DD}$ = 10V, $V_O$ = 9V | | 2.0 | | 2.5 | 2.0 | | 2.0 | |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | | 3.0 | | 3.5 | 3.0 | | 3.0 | |
| $V_{IH}$ | HIGH Level Input Voltage (CD4050BC Only) | $\|I_O\|$ < 1 µA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 4.5V | 3.5 | | 3.5 | 2.75 | | 3.5 | | V |
| | | $V_{DD}$ = 10V, $V_O$ = 9V | 7.0 | | 7.0 | 5.5 | | 7.0 | | |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | 11.0 | | 11.0 | 8.25 | | 11.0 | | |
| $V_{IH}$ | HIGH Level Input Voltage (CD4049UBC Only) | $\|I_O\|$ < 1 µA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 0.5V | 4.0 | | 4.0 | 3.5 | | 4.0 | | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1V | 8.0 | | 8.0 | 7.5 | | 8.0 | | |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 12.0 | | 12.0 | 11.5 | | 12.0 | | |
| $I_{OL}$ | LOW Level Output Current (Note 4) | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 0.4V | 5.6 | | 4.6 | 5 | | 3.2 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 0.5V | 12 | | 9.8 | 12 | | 6.8 | | |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 35 | | 29 | 40 | | 20 | | |
| $I_{OH}$ | HIGH Level Output Current (Note 4) | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 4.6V | −1.3 | | −1.1 | −1.6 | | −0.72 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 9.5V | −2.6 | | −2.2 | −3.6 | | −1.5 | | |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | −8.0 | | −7.2 | −12 | | −5 | | |
| $I_{IN}$ | Input Current | $V_{DD}$ = 15V, $V_{IN}$ = 0V | | −0.1 | | $-10^{-5}$ | −0.1 | | −1.0 | µA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = 15V | | 0.1 | | $10^{-5}$ | 0.1 | | 1.0 | |

Note 3: $V_{SS}$ = 0V unless otherwise specified.

## DC Electrical Characteristics (Continued)

Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. $I_{OL}$ and $I_{OH}$ are tested one output at a time.

## AC Electrical Characteristics (Note 5)

CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level | $V_{DD} = 5V$ | | 30 | 65 | ns |
| | | $V_{DD} = 10V$ | | 20 | 40 | |
| | | $V_{DD} = 15V$ | | 15 | 30 | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level | $V_{DD} = 5V$ | | 45 | 85 | ns |
| | | $V_{DD} = 10V$ | | 25 | 45 | |
| | | $V_{DD} = 15V$ | | 20 | 35 | |
| $t_{THL}$ | Transition Time HIGH-to-LOW Level | $V_{DD} = 5V$ | | 30 | 60 | ns |
| | | $V_{DD} = 10V$ | | 20 | 40 | |
| | | $V_{DD} = 15V$ | | 15 | 30 | |
| $t_{TLH}$ | Transition Time LOW-to-HIGH Level | $V_{DD} = 5V$ | | 60 | 120 | ns |
| | | $V_{DD} = 10V$ | | 30 | 55 | |
| | | $V_{DD} = 15V$ | | 25 | 45 | |
| $C_{IN}$ | Input Capacitance | Any Input | | 15 | 22.5 | pF |

Note 5: AC Parameters are guaranteed by DC correlated testing.

## AC Electrical Characteristics (Note 6)

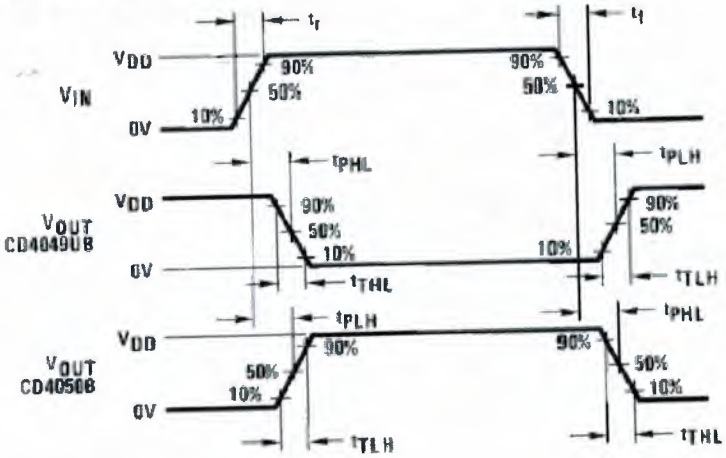
CD4050BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level | $V_{DD} = 5V$ | | 60 | 110 | ns |
| | | $V_{DD} = 10V$ | | 25 | 55 | |
| | | $V_{DD} = 15V$ | | 20 | 30 | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level | $V_{DD} = 5V$ | | 60 | 120 | ns |
| | | $V_{DD} = 10V$ | | 30 | 55 | |
| | | $V_{DD} = 15V$ | | 25 | 45 | |
| $t_{THL}$ | Transition Time HIGH-to-LOW Level | $V_{DD} = 5V$ | | 30 | 60 | ns |
| | | $V_{DD} = 10V$ | | 20 | 40 | |
| | | $V_{DD} = 15V$ | | 15 | 30 | |
| $t_{TLH}$ | Transition Time LOW-to-HIGH Level | $V_{DD} = 5V$ | | 60 | 120 | ns |
| | | $V_{DD} = 10V$ | | 30 | 55 | |
| | | $V_{DD} = 15V$ | | 25 | 45 | |
| $C_{IN}$ | Input Capacitance | Any Input | | 5 | 7.5 | pF |

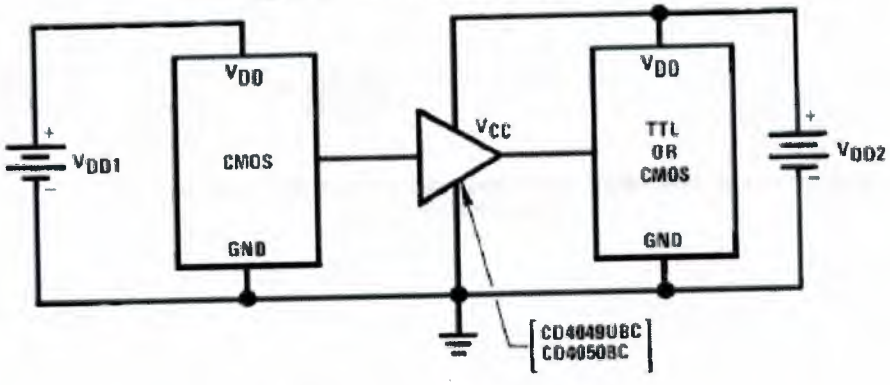
Note 6: AC Parameters are guaranteed by DC correlated testing.

## Switching Time Waveforms




## Typical Applications

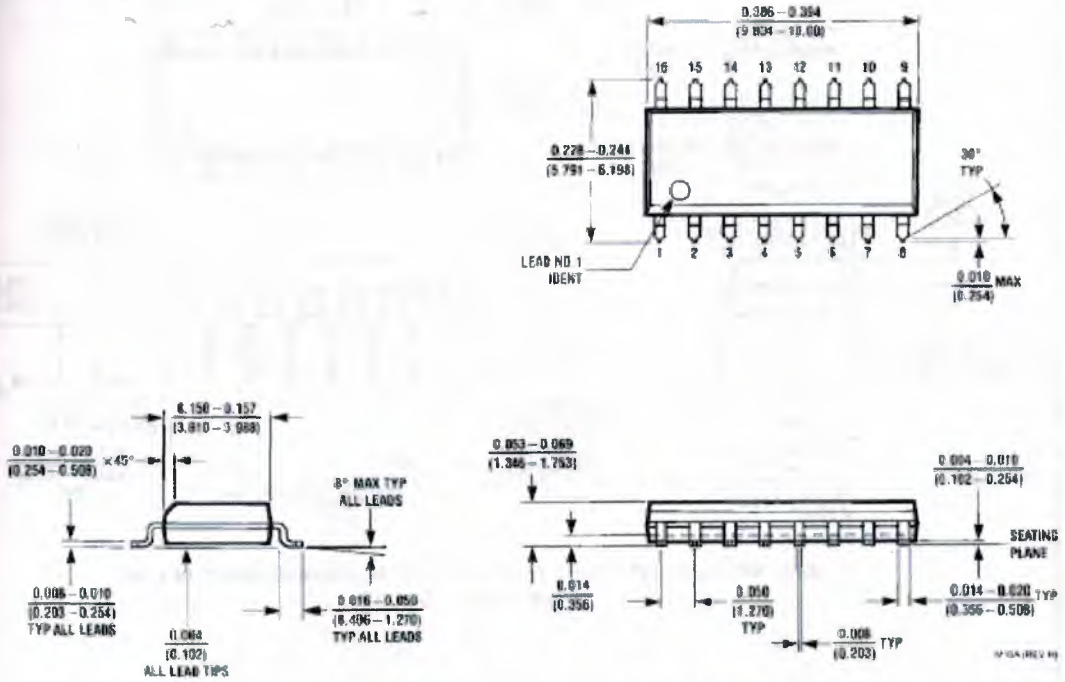
CMOS to TTL or CMOS at a Lower $V_{DD}$




$V_{DD1} \geq V_{DD2}$

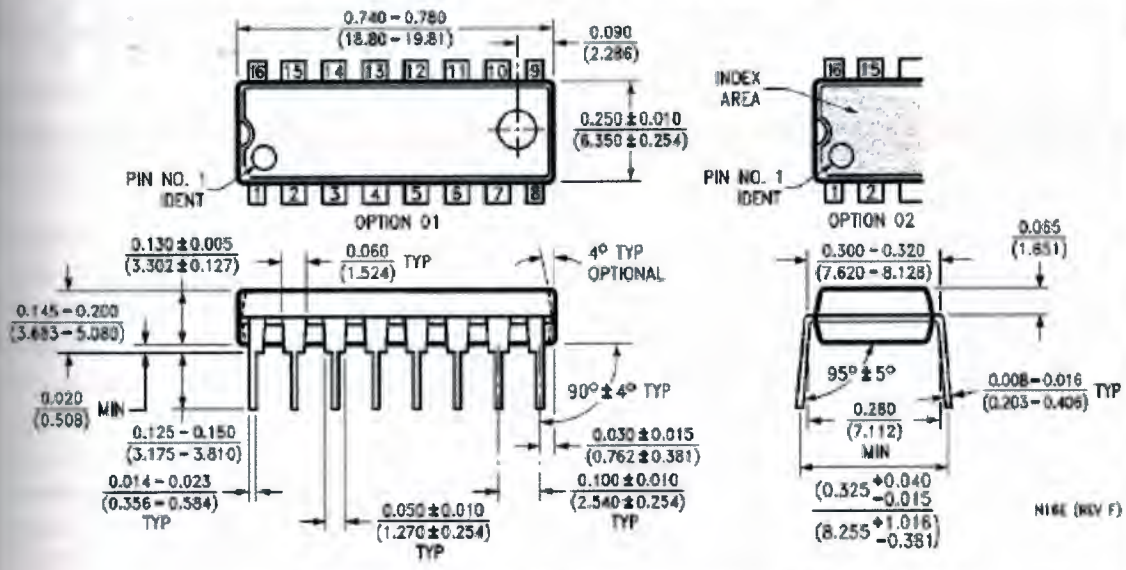
In the case of the CD4049UBC the output drive capability increases with increasing input voltage.
E.g., If $V_{DD1}$ = 10V the CD4049UBC could drive 4 TTL loads.

## Physical Dimensions inches (millimeters) unless otherwise noted




16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**

# ISO²-CMOS MT8870D/MT8870D-1
## Integrated DTMF Receiver

ISSUE 5 March 1997

### Features
- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

### Applications
- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

**Ordering Information**

| | |
|---|---|
| MT8870DE/DE-1 | 18 Pin Plastic DIP |
| MT8870DS/DS-1 | 18 Pin SOIC |
| MT8870DN/DN-1 | 20 Pin SSOP |

**-40 °C to +85 °C**

### Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

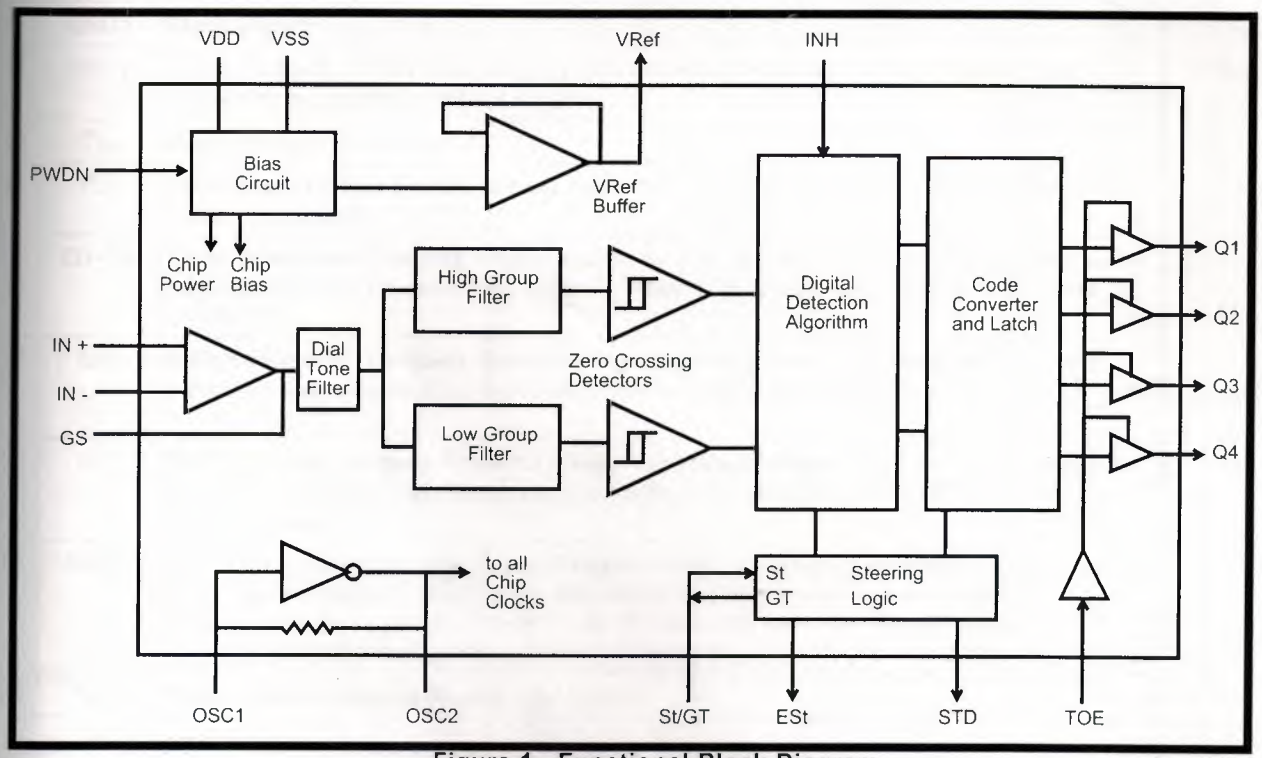



**Figure 1 - Functional Block Diagram**

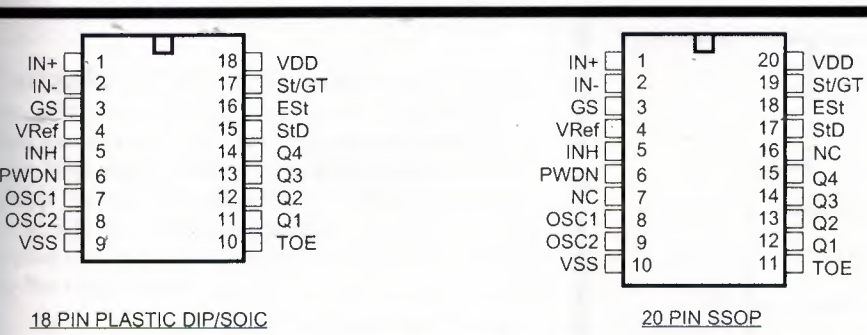



**Figure 2 - Pin Connections**

## Pin Description

| Pin # 18 | Pin # 20 | Name | Description |
|---|---|---|---|
| 1 | 1 | IN+ | **Non-Inverting Op-Amp (Input).** |
| 2 | 2 | IN- | **Inverting Op-Amp (Input).** |
| 3 | 3 | GS | **Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor. |
| 4 | 4 | $V_{Ref}$ | **Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10). |
| 5 | 5 | INH | **Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down. |
| 6 | 6 | PWDN | **Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down. |
| 7 | 8 | OSC1 | **Clock (Input).** |
| 8 | 9 | OSC2 | **Clock (Output).** A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit. |
| 9 | 10 | $V_{SS}$ | **Ground (Input).** 0V typical. |
| 10 | 11 | TOE | **Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally. |
| 11-14 | 12-15 | Q1-Q4 | **Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance. |
| 15 | 17 | StD | **Delayed Steering (Output).**Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below $V_{TSt}$. |
| 16 | 18 | ESt | **Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low. |
| 17 | 19 | St/GT | **Steering Input/Guard time (Output) Bidirectional.** A voltage greater than $V_{TSt}$ detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than $V_{TSt}$ frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St. |
| 18 | 20 | $V_{DD}$ | **Positive power supply (Input).** +5V typical. |
| | 7, 16 | NC | No Connection. |

## Functional Description

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

### Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

### Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while

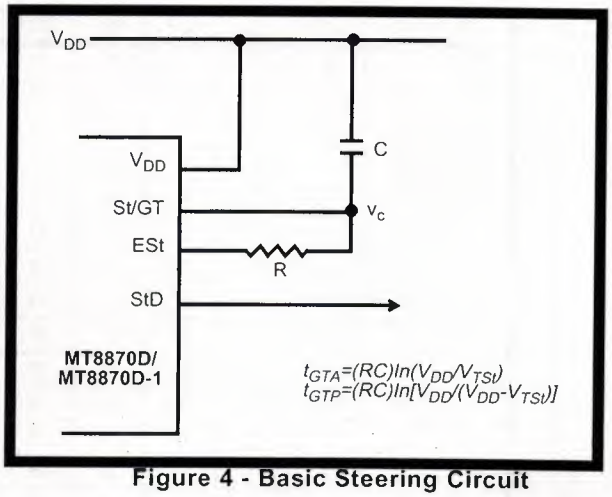



**Figure 4 - Basic Steering Circuit**

providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

### Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes $v_c$ (see Figure 4) to rise as the capacitor discharges. Provided signal

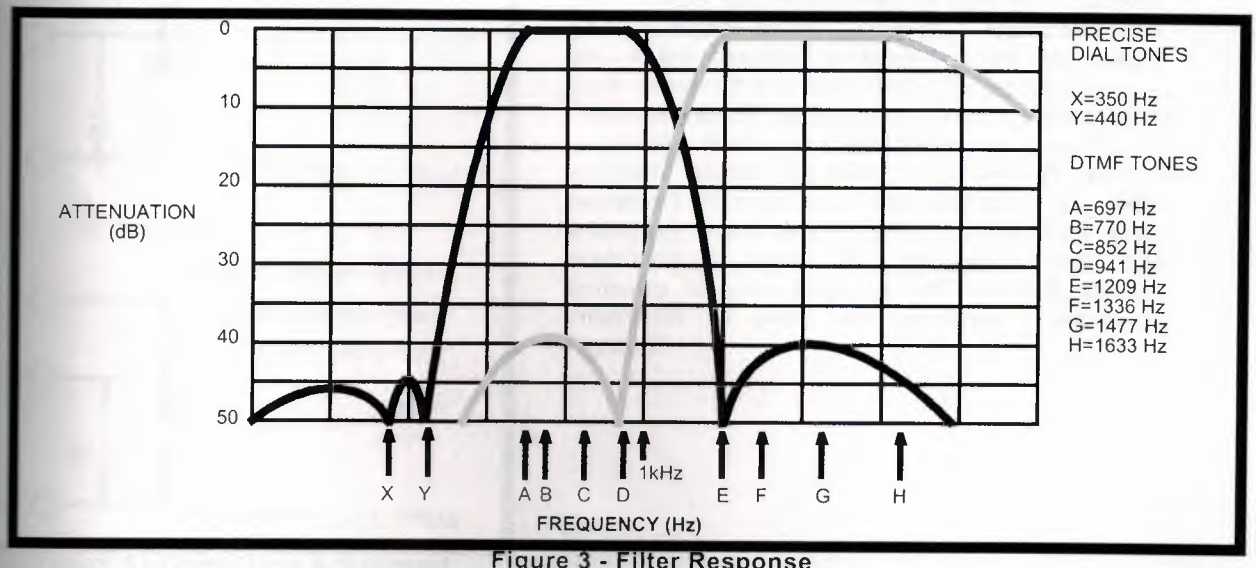



**Figure 3 - Filter Response**

is maintained (ESt remains high) for the period ($t_{GTP}$), $v_c$ reaches the threshold of the steering logic to register the tone pair, setting its corresponding 4-bit code (see Table 1) in the output latch. At this point the GT output is disabled and drives $v_c$ to $V_{DD}$. GT continues to drive high as long as ESt remains high. Finally, after a guard delay to allow the output latch to settle, the internal steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to optimize performance to meet a wide variety of system requirements.

### Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 4 is applicable. Component values are chosen according to the formula:

$$t_{REC}=t_{DP}+t_{GTP}$$
$$t_{ID}=t_{DA}+t_{GTA}$$

The value of $t_{DP}$ is a device parameter (see Figure 7) and $t_{REC}$ is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer.

| Digit | TOE | INH | ESt | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ |
|---|---|---|---|---|---|---|---|
| ANY | L | X | H | Z | Z | Z | Z |
| 1 | H | X | H | 0 | 0 | 0 | 1 |
| 2 | H | X | H | 0 | 0 | 1 | 0 |
| 3 | H | X | H | 0 | 0 | 1 | 1 |
| 4 | H | X | H | 0 | 1 | 0 | 0 |
| 5 | H | X | H | 0 | 1 | 0 | 1 |
| 6 | H | X | H | 0 | 1 | 1 | 0 |
| 7 | H | X | H | 0 | 1 | 1 | 1 |
| 8 | H | X | H | 1 | 0 | 0 | 0 |
| 9 | H | X | H | 1 | 0 | 0 | 1 |
| 0 | H | X | H | 1 | 0 | 1 | 0 |
| * | H | X | H | 1 | 0 | 1 | 1 |
| # | H | X | H | 1 | 1 | 0 | 0 |
| A | H | L | H | 1 | 1 | 0 | 1 |
| B | H | L | H | 1 | 1 | 1 | 0 |
| C | H | L | H | 1 | 1 | 1 | 1 |
| D | H | L | H | 0 | 0 | 0 | 0 |
| A | H | H | L | undetected, the output code will remain the same as the previous detected code | | | |
| B | H | H | L | | | | |
| C | H | H | L | | | | |
| D | H | H | L | | | | |

**Table 1. Functional Decode Table**

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

Different steering arrangements may be used to select independently the guard times for tone present ($t_{GTP}$) and tone absent ($t_{GTA}$). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing $t_{REC}$ improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short $t_{REC}$ with a long $t_{DO}$ would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

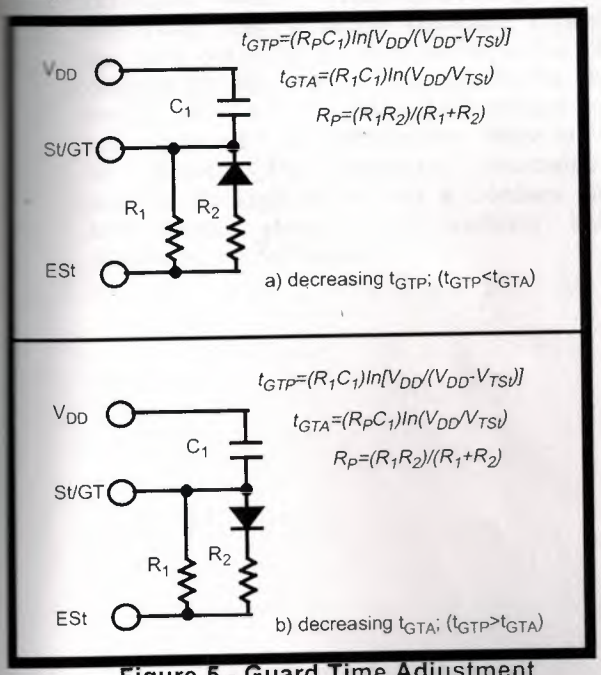



**Figure 5 - Guard Time Adjustment**

### Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

### Differential Input Configuration

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a bias source ($V_{Ref}$) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and $V_{Ref}$ biasing the input at $^1/_2V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor $R_5$.

### Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several MT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

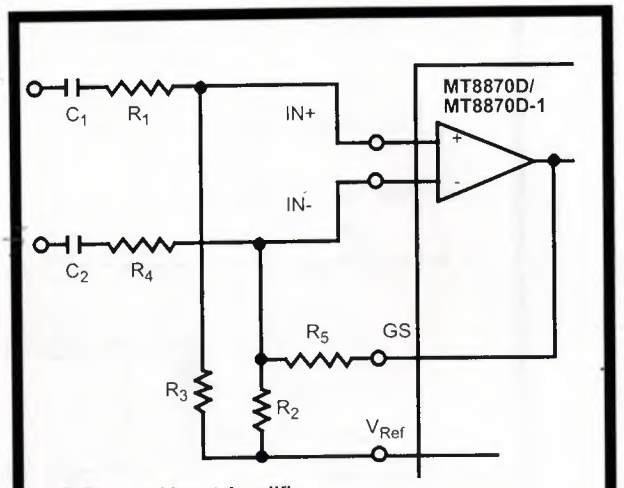



**Figure 6 - Differential Input Configuration**

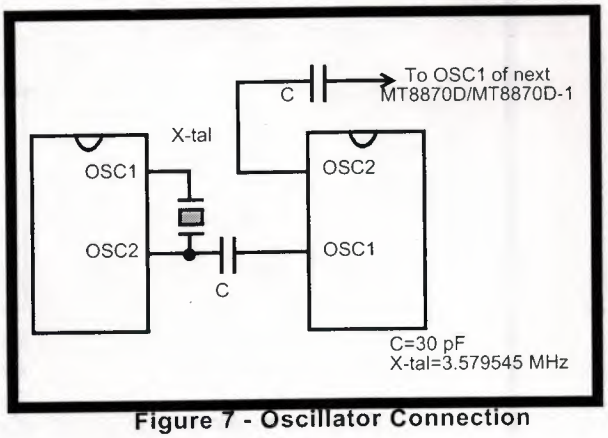



**Figure 7 - Oscillator Connection**

| Parameter | Unit | Resonator |
|---|---|---|
| R1 | Ohms | 10.752 |
| L1 | mH | .432 |
| C1 | pF | 4.984 |
| C0 | pF | 37.915 |
| Qm | - | 896.37 |
| Δf | % | ±0.2% |

**Table 2. Recommended Resonator Specifications**

Note: Qm=quality factor of RLC model, i.e., $1/2\Pi fR1C1$.

## ications

### SYSTEM FOR BRITISH TELECOM
### 1151

shown in Fig. 9 illustrates the use of D-1 device in a typical receiver system. BT defines the input signals less than -34 dBm as operate level. This condition can be attained a suitable values of $R_1$ and $R_2$ to 3 dB attenuation, such that -34 dBm input will correspond to -37 dBm at the gain setting of MT8870D-1. As shown in the diagram, the ent values of $R_3$ and $C_2$ are the guard time ments when the total component tolerance is . For better performance, it is recommended to the non-symmetric guard time circuit in Fig. 8.

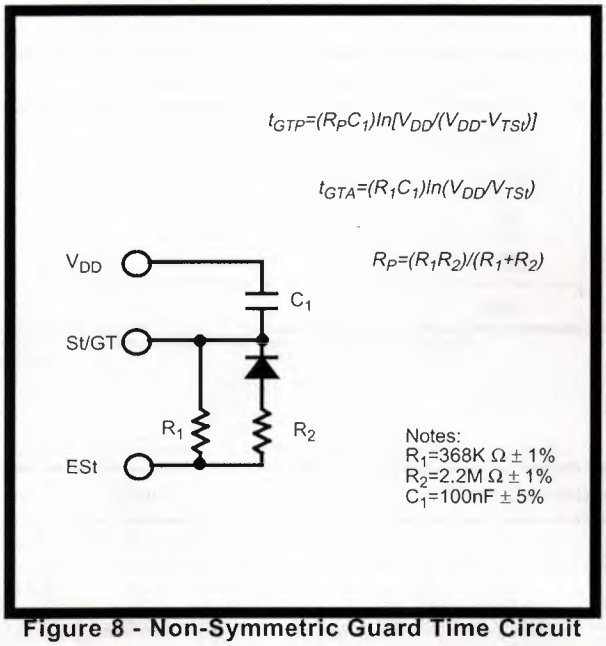



**Figure 8 - Non-Symmetric Guard Time Circuit**

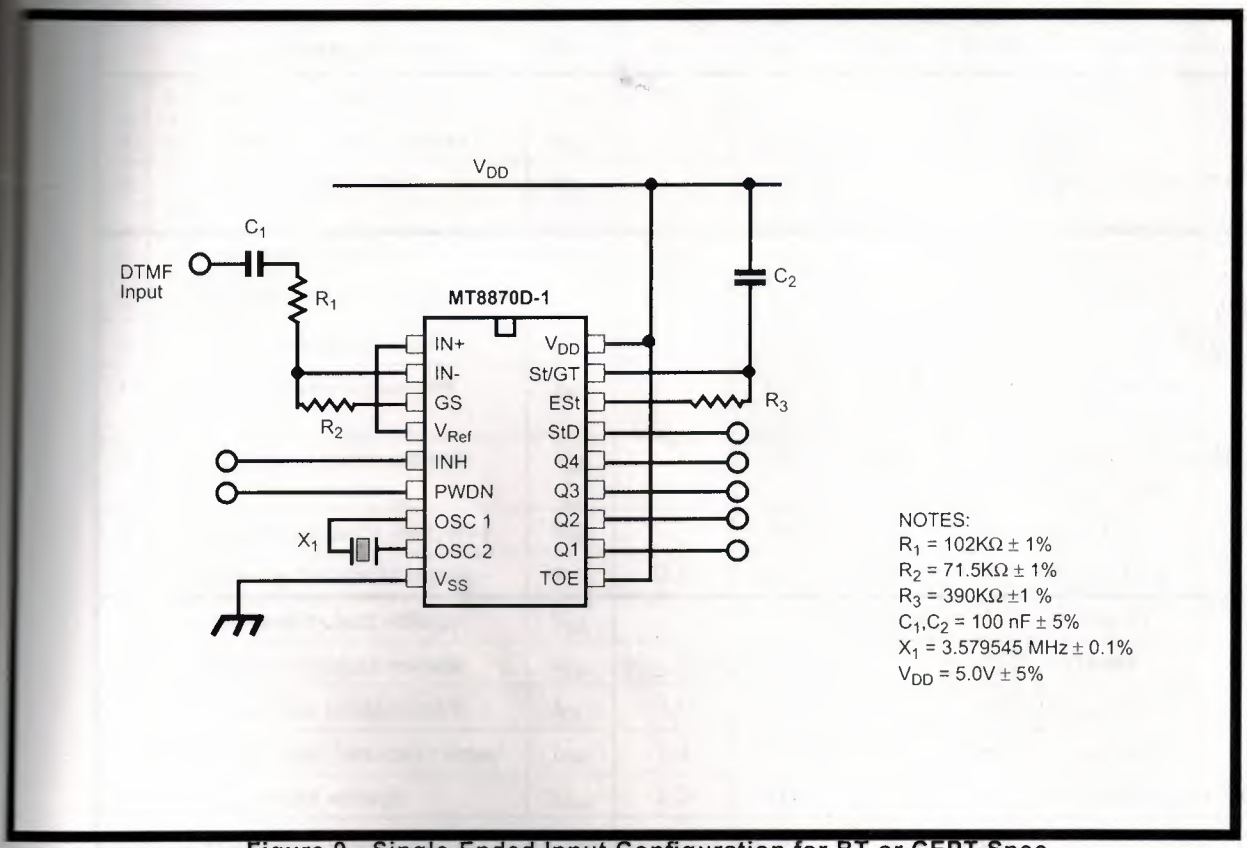



**Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec**

## Absolute Maximum Ratings†

| | Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| 1 | DC Power Supply Voltage | $V_{DD}$ | | 7 | V |
| 2 | Voltage on any pin | $V_I$ | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| 3 | Current at any pin (other than supply) | $I_I$ | | 10 | mA |
| 4 | Storage temperature | $T_{STG}$ | -65 | +150 | °C |
| 5 | Package power dissipation | $P_D$ | | 500 | mW |

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C. All leads soldered to board.

## Recommended Operating Conditions - Voltages are with respect to ground ($V_{SS}$) unless otherwise stated.

| | Parameter | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | DC Power Supply Voltage | $V_{DD}$ | 4.75 | 5.0 | 5.25 | V | |
| 2 | Operating Temperature | $T_O$ | -40 | | +85 | °C | |
| 3 | Crystal/Clock Frequency | fc | | 3.579545 | | MHz | |
| 4 | Crystal/Clock Freq.Tolerance | Δfc | | ±0.1 | | % | |

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

## DC Electrical Characteristics - $V_{DD}$=5.0V± 5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C, unless otherwise stated.

| | | Characteristics | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| 1 | SUPPLY | Standby supply current | $I_{DDQ}$ | | 10 | 25 | µA | PWDN=$V_{DD}$ |
| 2 | | Operating supply current | $I_{DD}$ | | 3.0 | 9.0 | mA | |
| 3 | | Power consumption | $P_O$ | | 15 | | mW | fc=3.579545 MHz |
| 4 | INPUTS | High level input | $V_{IH}$ | 3.5 | | | V | $V_{DD}$=5.0V |
| 5 | | Low level input voltage | $V_{IL}$ | | | 1.5 | V | $V_{DD}$=5.0V |
| 6 | | Input leakage current | $I_{IH}/I_{IL}$ | | 0.1 | | µA | $V_{IN}$=$V_{SS}$ or $V_{DD}$ |
| 7 | | Pull up (source) current | $I_{SO}$ | | 7.5 | 20 | µA | TOE (pin 10)=0, $V_{DD}$=5.0V |
| 8 | | Pull down (sink) current | $I_{SI}$ | | 15 | 45 | µA | INH=5.0V, PWDN=5.0V, $V_{DD}$=5.0V |
| 9 | | Input impedance (IN+, IN-) | $R_{IN}$ | | 10 | | MΩ | @ 1 kHz |
| 10 | | Steering threshold voltage | $V_{TSt}$ | 2.2 | 2.4 | 2.5 | V | $V_{DD}$ = 5.0V |
| 11 | OUTPUTS | Low level output voltage | $V_{OL}$ | | | $V_{SS}$+0.03 | V | No load |
| 12 | | High level output voltage | $V_{OH}$ | $V_{DD}$-0.03 | | | V | No load |
| 13 | | Output low (sink) current | $I_{OL}$ | 1.0 | 2.5 | | mA | $V_{OUT}$=0.4 V |
| 14 | | Output high (source) current | $I_{OH}$ | 0.4 | 0.8 | | mA | $V_{OUT}$=4.6 V |
| 15 | | $V_{Ref}$ output voltage | $V_{Ref}$ | 2.3 | 2.5 | 2.7 | V | No load, $V_{DD}$ = 5.0V |
| 16 | | $V_{Ref}$ output resistance | $R_{OR}$ | | 1 | | kΩ | |

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

## Operating Characteristics - $V_{DD}$=5.0V±5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C ,unless otherwise stated.

### Gain Setting Amplifier

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Input leakage current | $I_{IN}$ | | | 100 | nA | $V_{SS} \le V_{IN} \le V_{DD}$ |
| 2 | Input resistance | $R_{IN}$ | 10 | | | MΩ | |
| 3 | Input offset voltage | $V_{OS}$ | | | 25 | mV | |
| 4 | Power supply rejection | PSRR | 50 | | | dB | 1 kHz |
| 5 | Common mode rejection | CMRR | 40 | | | dB | 0.75 V ≤ $V_{IN}$ ≤ 4.25 V biased at $V_{Ref}$ =2.5 V |
| 6 | DC open loop voltage gain | $A_{VOL}$ | 32 | | | dB | |
| 7 | Unity gain bandwidth | $f_C$ | 0.30 | | | MHz | |
| 8 | Output voltage swing | $V_O$ | 4.0 | | | $V_{pp}$ | Load ≥ 100 kΩ to $V_{SS}$ @ GS |
| 9 | Maximum capacitive load (GS) | $C_L$ | | | 100 | pF | |
| 10 | Resistive load (GS) | $R_L$ | | | 50 | kΩ | |
| 11 | Common mode range | $V_{CM}$ | 2.5 | | | $V_{pp}$ | No Load |

## MT8870D AC Electrical Characteristics - $V_{DD}$=5.0V ±5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C , using Test Circuit shown in Figure 10.

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Notes* |
|---|---|---|---|---|---|---|---|
| 1 | Valid input signal levels (each tone of composite signal) | | -29 | | +1 | dBm | 1,2,3,5,6,9 |
| | | | 27.5 | | 869 | $mV_{RMS}$ | 1,2,3,5,6,9 |
| 2 | Negative twist accept | | | | 8 | dB | 2,3,6,9,12 |
| 3 | Positive twist accept | | | | 8 | dB | 2,3,6,9,12 |
| 4 | Frequency deviation accept | | ±1.5% ± 2 Hz | | | | 2,3,5,9 |
| 5 | Frequency deviation reject | | ±3.5% | | | | 2,3,5,9 |
| 6 | Third tone tolerance | | | -16 | | dB | 2,3,4,5,9,10 |
| 7 | Noise tolerance | | | -12 | | dB | 2,3,4,5,7,9,10 |
| 8 | Dial tone tolerance | | | +22 | | dB | 2,3,4,5,8,9,11 |

‡Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz ) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

## MT8870D-1 AC Electrical Characteristics

- $V_{DD}$=5.0V±5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C , using Test Circuit shown in Figure 10.

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Notes* |
|---|---|---|---|---|---|---|---|
| 1 | Valid input signal levels (each tone of composite signal) | | -31 | | +1 | dBm | Tested at $V_{DD}$=5.0V 1,2,3,5,6,9 |
| | | | 21.8 | | 869 | $mV_{RMS}$ | |
| 2 | Input Signal Level Reject | | -37 | | | dBm | Tested at $V_{DD}$=5.0V 1,2,3,5,6,9 |
| | | | 10.9 | | | $mV_{RMS}$ | |
| 3 | Negative twist accept | | | | 8 | dB | 2,3,6,9,13 |
| 4 | Positive twist accept | | | | 8 | dB | 2,3,6,9,13 |
| 5 | Frequency deviation accept | | ±1.5%± 2 Hz | | | | 2,3,5,9 |
| 6 | Frequency deviation reject | | ±3.5% | | | | 2,3,5,9 |
| 7 | Third zone tolerance | | | -18.5 | | dB | 2,3,4,5,9,12 |
| 8 | Noise tolerance | | | -12 | | dB | 2,3,4,5,7,9,10 |
| 9 | Dial tone tolerance | | | +22 | | dB | 2,3,4,5,8,9,11 |

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz ) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
13. Guaranteed by design and characterization.

## AC Electrical Characteristics - $V_{DD}$=5.0V±5%, $V_{SS}$=0V, -40°C ≤ To ≤ +85°C , using Test Circuit shown in Figure 10.

| | | Characteristics | Sym | Min | Typ‡ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 1 | TIMING | Tone present detect time | $t_{DP}$ | 5 | 11 | 14 | ms | Note 1 |
| 2 | | Tone absent detect time | $t_{DA}$ | 0.5 | 4 | 8.5 | ms | Note 1 |
| 3 | | Tone duration accept | $t_{REC}$ | | | 40 | ms | Note 2 |
| 4 | | Tone duration reject | $t_{\overline{REC}}$ | 20 | | | ms | Note 2 |
| 5 | | Interdigit pause accept | $t_{ID}$ | | | 40 | ms | Note 2 |
| 6 | | Interdigit pause reject | $t_{DO}$ | 20 | | | ms | Note 2 |
| 7 | OUTPUTS | Propagation delay (St to Q) | $t_{PQ}$ | | 8 | 11 | µs | TOE=$V_{DD}$ |
| 8 | | Propagation delay (St to StD) | $t_{PStD}$ | | 12 | 16 | µs | TOE=$V_{DD}$ |
| 9 | | Output data set up (Q to StD) | $t_{QStD}$ | | 3.4 | | µs | TOE=$V_{DD}$ |
| 10 | | Propagation delay (TOE to Q ENABLE) | $t_{PTE}$ | | 50 | | ns | load of 10 kΩ, 50 pF |
| 11 | | Propagation delay (TOE to Q DISABLE) | $t_{PTD}$ | | 300 | | ns | load of 10 kΩ, 50 pF |
| 12 | PDWN | Power-up time | $t_{PU}$ | | 30 | | ms | Note 3 |
| 13 | | Power-down time | $t_{PD}$ | | 20 | | ms | |
| 14 | CLOCK | Crystal/clock frequency | $f_C$ | 3.5759 | 3.5795 | 3.5831 | MHz | |
| 15 | | Clock input rise time | $t_{LHCL}$ | | | 110 | ns | Ext. clock |
| 16 | | Clock input fall time | $t_{HLCL}$ | | | 110 | ns | Ext. clock |
| 17 | | Clock input duty cycle | $DC_{CL}$ | 40 | 50 | 60 | % | Ext. clock |
| 18 | | Capacitive load (OSC2) | $C_{LO}$ | | | 30 | pF | |

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

NOTES:
1. Used for guard-time calculation purposes only.
2. These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
3. With valid tone present at input, $t_{PU}$ equals time from PDWN going low until ESt going high.

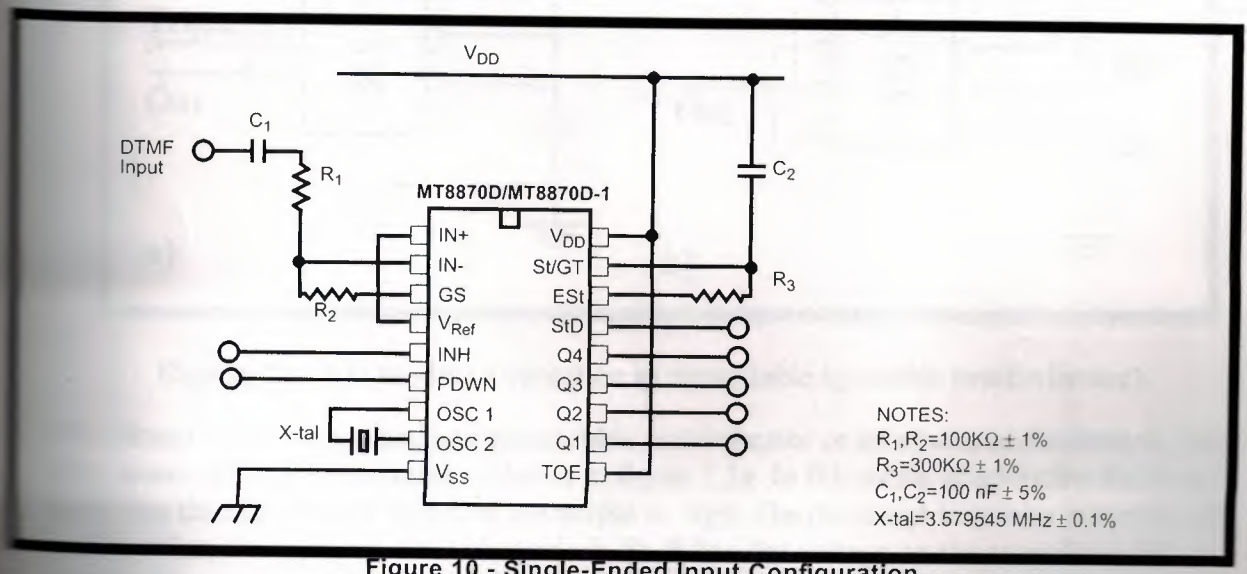



**Figure 10 - Single-Ended Input Configuration**

# The 555 timer

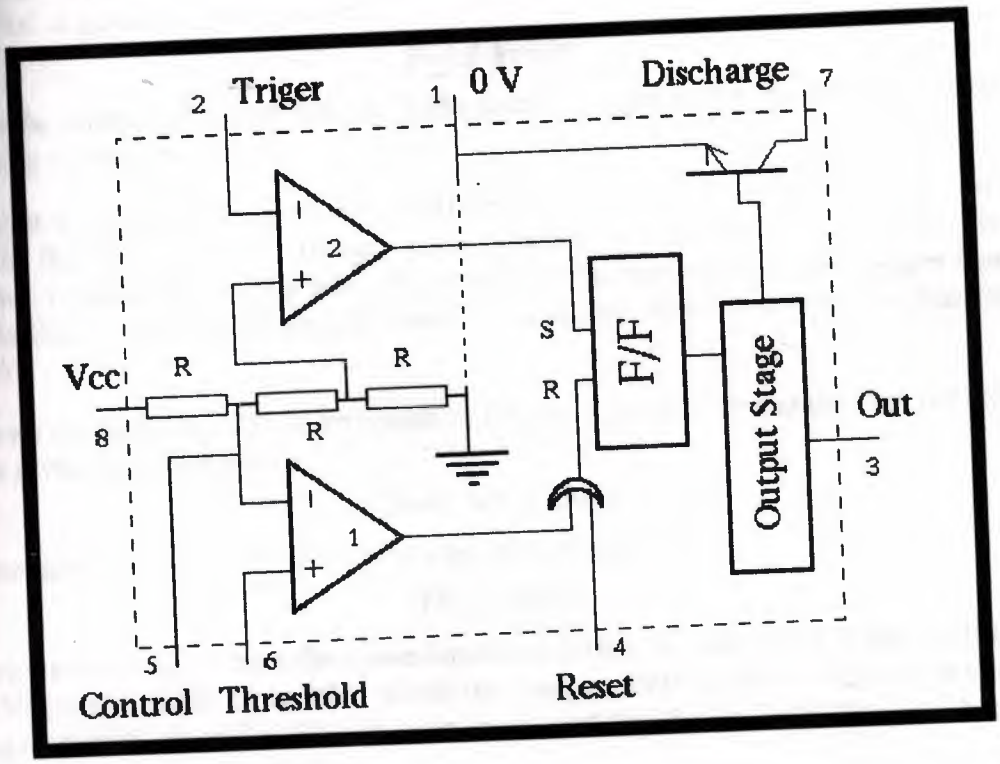



**Figure:** The 555 internal circuit

The 555 circuit is consisted by two comparators, one ohmic ladder one flip-flop and a discharging transistor, as it is shown in figure 1.1.

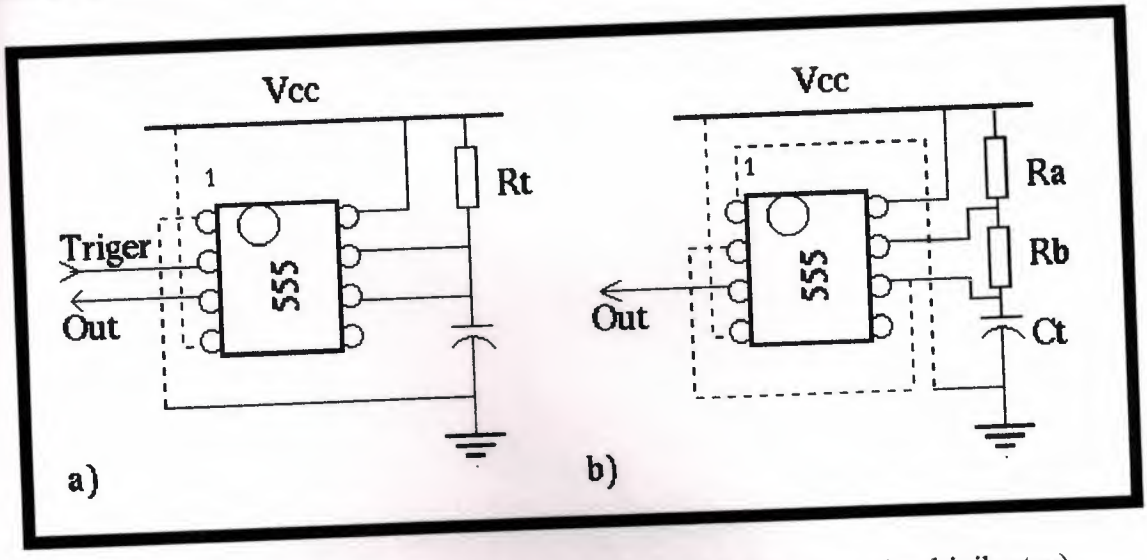



**Figure:** The 555 modes of operation a) monostable b) astable (multivibrator).

This circuit can be connected as a monostable multivibrator or an astable multivibrator. The 555, connected as a monostable is shown in figure 1.1a. In this mode of operation the *trigger* input sets the flip flop which drives the output to *high*. The discharge transistor is turned off and therefore the capacitor *Ct* is charged via *Rt*. When the voltage on the capacitor ( *Ct*) reaches the control voltage, which is defined by the three resistor voltage divider ( *Vcont=2/3*

Ver ), the flip-flop is resetted. This turns the discharge transistor on, which discharge the capacitor. Thereafter the circuit can be charged again by a new pulse at the *trigger* input. The timed period is given by the equation:

$$T=1.1\ Rt*Ct$$

Were $T$ is the output pulse *high* period, $Ct$ the charging capacitance measured in Farads and $Rt$ the charging resistor in Ohms.

If the circuit is connected as an astable multivibrator (figure 1.1b), the comparator 2 of figure 1.1 sets the flip-flop, when the voltage on the capacitor $Ct$ falls below $1/3Vcc$, while the comparator 1 resets the flip-flop when the voltage on the capacitor becomes bigger than $2/3Vcc$. In this case the discharging transistor is turned *on*, which discharge the time capacitor $Ct$ via $Rb$.

This allows the use of the 555 as an oscillator (figure 1.1b) The time at the *high* (or charging) period is given by the equation:

$$Th=0.7(Ra+Rb)Ct$$

While the time for the low period is given by the equation:

$$Tl=0.7\ Rb*Ct$$

The obvious observation from the above equations is that the duty cycle of the oscillator is always bigger than 50%. Or in other words the charging time is always bigger that the discharging period, since $Ra+Rb>Rb$ taken in account that $Ra>0$. Yet if Ra>>Rb then a 50% duty cycle can be approximated.

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