University of Salford
Department of Electrical and Electronics

COMMUNICATION LINK BETWEEN TWO ROBATS AND A CENTRAL COMPUTER BY MEANS OF INRARED RADIATION

** A WIRELESS LAN APPROACH **

PROJECT SUMMERY

By

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ABSTRACT

Traditionally,robotic research has concentrated on the development of single robot devices which use increasingly sophisticated hardware and software to achieve move complex tasks.At Salford,we have adopted an alternative approach wher the single sophisticated device is replaced by a number of technically simpler robots which concentrate and co-operate to acheive a complex task.

This approach has a number of advantages,including the ability to have different robots with different capabilities and fault tolerance due to redundancy.

My project is a subsidiary of one of research areas in Salford,Co-operant Mobile Robot for Advanced Manufacturing and Material Handling Applications.The researchers,in Salford have investigated the nature of co-operation,particularly learning from the insect world where the sosial insects such as bees,ants and terminates.The researchers have also developed a powerfull control architecture to implement co-operation,based on behaviours.

Some of the advantages of a cominication link between robots to co-operate is given in introduction.

ACKNOWLEDGEMENT.

It is imposible to state all the scholars who contribute this project,but I would like to thank to Dr.Barns for his encouragement and the administration of Salford University for creating such a motivating development center.

INTRODUCTION

1.

1.1 OFFLINE CONTROL

The majority of robat control comands are created online using a teach pendant to drive the robat through a sequence of positions where various fanctions are programmed to perform the operations desired.In contrast,offline programming is performed without direct involment of the robat.there are several well established reasons for using offline control:

(a)the robat is non-productive during the manual teaching phase.

(b)online teaching is both tedious and time consuming particularly for complex operations.

(c)the danger of damage to an expensive component may be significant during the teaching phase.

(d)online teaching sets the attitude of the robat tool "by eye" which may be inadequate for cetain applications such as drilling and assembly tasks.

(e)in small batch manufacture,online teach methods may occupy a significant proportion of the total production of the total production run time.

1.2 ADVANTAGES OF INFRA-RED RADIATION IN COMMUNICATION

The advantages of IR radiation over systems employing other forms of electromagnetic radiation lies primarily in:

1-Their directivity,which means greater antenna gain with smaller antenna size in return means less required transmittion power.

2-The hugeness of the available spectrum and the wide bandwith that is thereby available for transmission.

1.3 DATA COMMUNICATION.

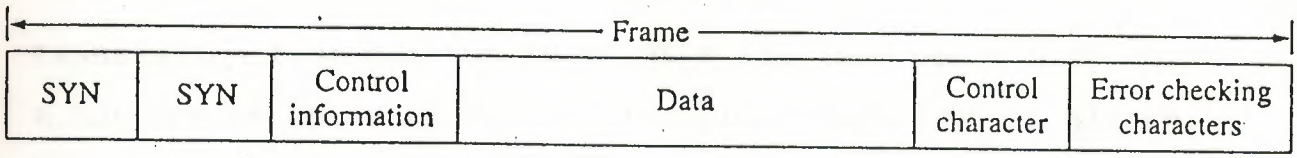
Data communication is the process of sharing or exchanging encoded information between two or more pieces of equipment.The term encoded information means that data is transfered as a sequence of electrical signal.Encoded data can be sent in either analog or digital form.In this project it is in the form of digital.

1.4 SERIAL AND PARALLEL TRANSMISSION

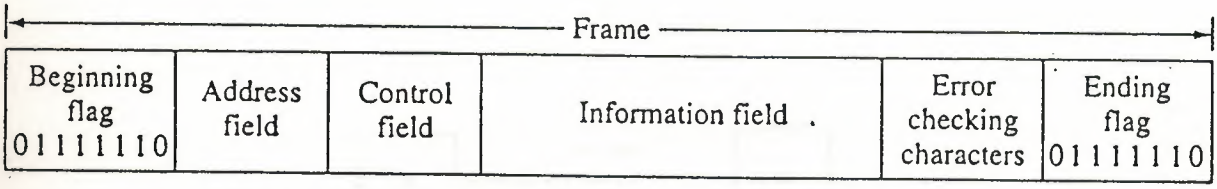
Data may be transferred either by serial transmission over a single line or by parallel transmission over many lines.In serial transmission,binary data is sent down a single wire 1 bit at a time.In parallel transmission,each bit has its own wire and all the data is sent at the same time.As expected,parallel transission is faster because all bits are sent at once.Therefore parallel transmission is used within the computer for the functions such as transferring data between the CPU and memory,between the CPU and I/O chips,and between memory and I/O chips.The primary concern of this project is serial rather then parallel.

1.5 ASYNCHRONOUS TRANSMISSION

Asynhronous means that a character may be transmitted at any time.Asynchronous transmission is used primarily for slow speed (less than 19200 bits per second) and inexpensive data equipment such as CRT terminals,printers,and ploters.It is a popular method of sending data because the logic circuitry is simple,thus reducing the cost.It also allows for variable burst of data;that is,the time between characters does not have to be equal.



(a)



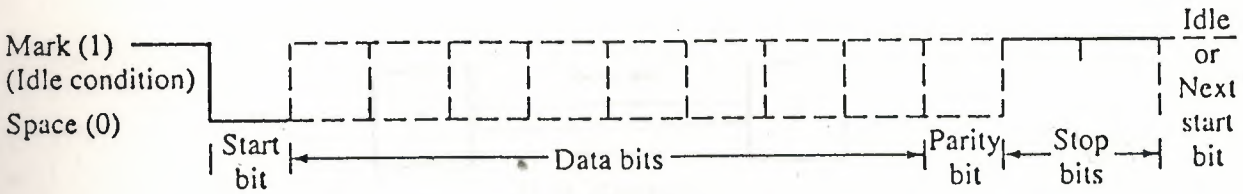


Figure 1.1 Transission Formats (a) Synchronous (b) Asynchronous.

1.6 COMMUNICATION MODES

There are three types of communication modes:SIMPLEX,HALF-DUPLEX,and FULL-DUPLEX.In simplex transmission,data always flows in the same direction direction.Half-duplex communication permits transission from point A to point B and from point B to point A,but not at the same time.Full-duplex communication allows transmission from A to B and from B to A simultaneously.Fig 1.1 depicts the modes of communication.

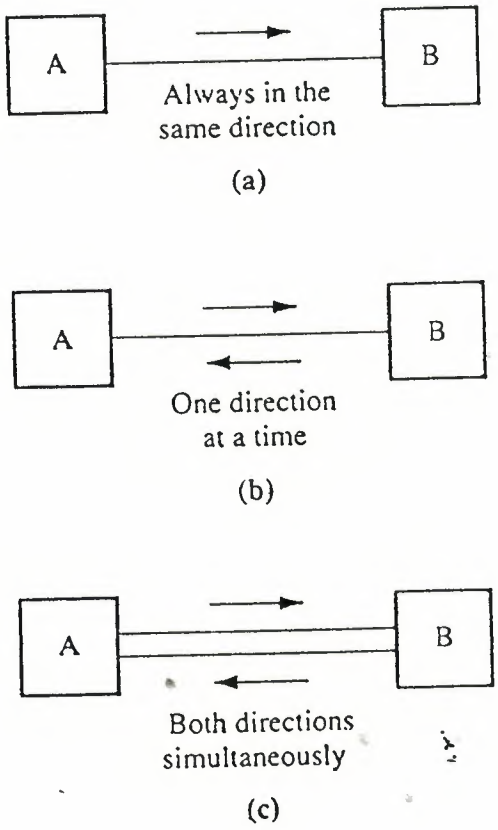


Fig 1.2 Types of Modes:(a) Simplex;(b) Half-duplex; (c) Full-duplex

1.7 SUMMERY OF BASIC CONCEPTS IN THIS PROJECT.

1.In serial I/O communication,a word is transmitted one bit at a time over a single line by converting a parallel word into a stream of serial bits.On the other hand,a word is received by converting a stream of bits into a parallel word.

2.Serial data communication can be either syncronous or asynchronous mode for low speed data communication.

3.The MPU identifies a serial peripheral through a decoded address and an appropriate control signal.Data transfer can be implemented using such methods as polling and interrupt.

DEVELOPMENT CONSIDERATIONS

2.

2.DEVELOPMENT CONSIDERATIONS.

2.1 MICROPROCESSOR

There is a wide range of criteria to be considered;

(a) Speed

(b) Cost

(c) Memory addresing capability

(d) Interrupt structure

(e) I/O structure

(f) Word size

2.2 HARDWARE/SOFTWARE TRADEOFF

For same aspects of an application there is a choise of realising functions in either hardware or software.The choise between a hardware or software implementation for a function is on several issues:

2.2.1 SPEED

A software solution may be too slow,with the processor capability available.In general,dedicated hardware can be expected to respond more quicly than a stored program device like a microprocessor.

2.2.2 COST.

The possible expense of a more powerfull processor and additional memory to support a software solution must be compared againest the cost of any additional hardware.The question of cost over a production

run must be considered.If it is a matter of software development cost against hardware cos,then the former is non-recurring whereas the latter rises with the number of systems produced.

2.2.3 RELIABILITY.

A hardware solution for a particular function may be less prone to incorrect operation since it only performs the one function whereas the processor is performing many functions which interract with one another.Certainly,the reliabilty of hardware is better understood and is therefore easier to predict,than the reliability of software.

2.3 CHOISE OF LEVEL OF LANGUAGE

The choise of level of language at which the application code can be developed rests between:

(a) High level language

(b) Assembly language

(c) Microcode

The relative merits of each of these are discussed below.

2.3.1 HIGH LEVEL LANGUAGE.

The advantages which accure from working with a high level language include:

1- The easy of writing code in the form of near-English statements.

2- The easy of reading code in near-English.

3- The housekeeping of memory usage and other system detailes which are carried out automatically.

4- Higher productivity than is the case for lower level coding.

The disadvantages of the high level languages for control applications include:

1- Lower efficiency:compiler generated machine code is usually significantly less efficient than hand generated code,both in terms of speed and size.However,it should be noted that as larger applications are considered,their increased complexity swamps the assembly programmer in detail so that the code becomes less efficient.

2- Poor hardware interface:few high level languages offer the ability to interact closely with the hardware.

2.3.2 ASSEMBLY LANGUAGE

As it was stated above,if the program gets larger assembly language is not recommended.

2.3.3 MICROCODE.

Although access to the microcode level is more widespread than it is used to be,the large overheads in writing at this level will rule it out as a serious possibility.

2.4 BANDWITH CONSIDERATIONS

As shown in figure 2.1 sharp digital signals require a tremendous amount of frequency spectrum (bandwith).Since transmission channels have limited bandwith,it is very important important to choose the appropiate signaling format.

During the design of the system I consider the following:

(1) The minimum possible bandwith required for a given pulse rate

(2) How pulses can be shaped to minimize the bandwith and distortion of the data pulses.

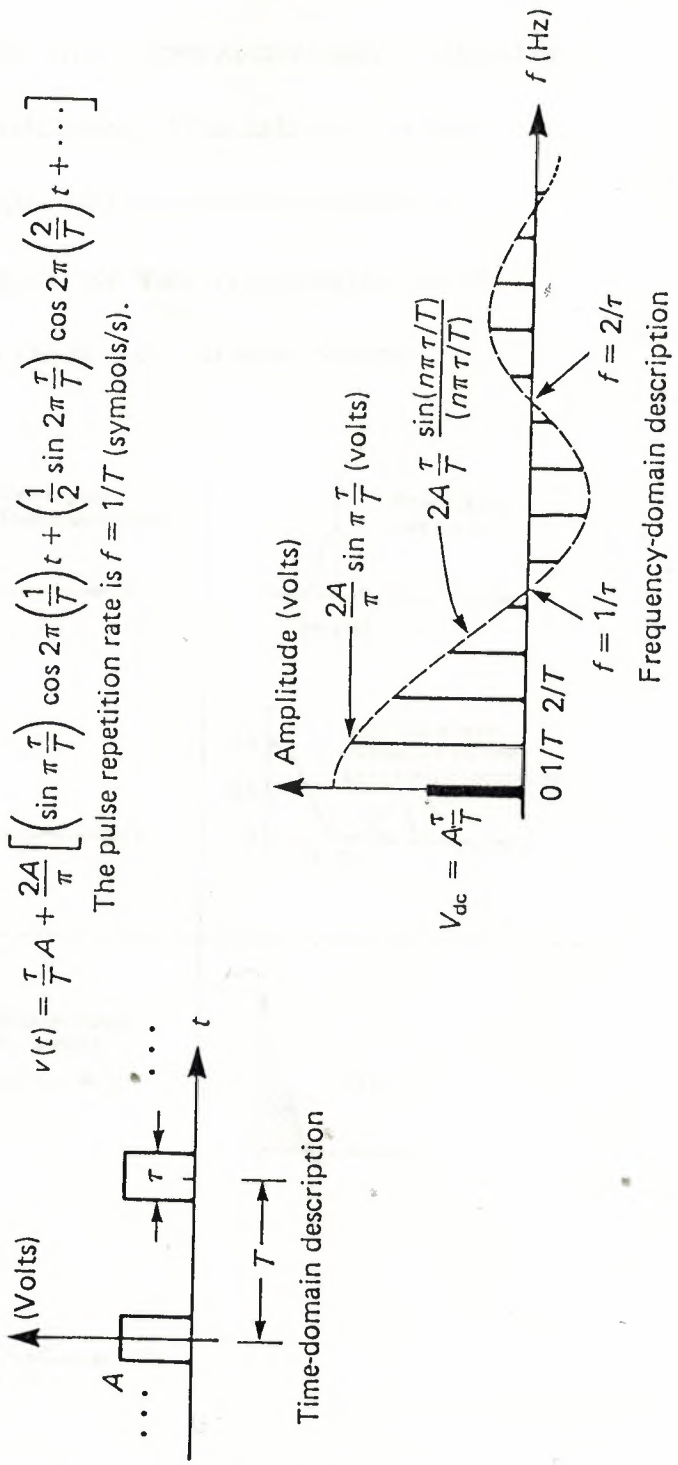


Figure 2.1 Time and Frequency description of a rectangular pulse train.

2.5 PULSE SHAPING FOR MINIMAZING BANDWITH AND PULSE DISTORTION.

Figure 2.2 shows pulses and the first lobe,and indicates how power is more concentrated for some pulse shapes as compered to others.For a channel with a bandwith wide enough to include the first lobe, transmitting raised-cosine pulses will result in the reception of more power with less pulse distortion than for rectangular pulses. In spite of this fact Nonreturn to zero format was choosen.

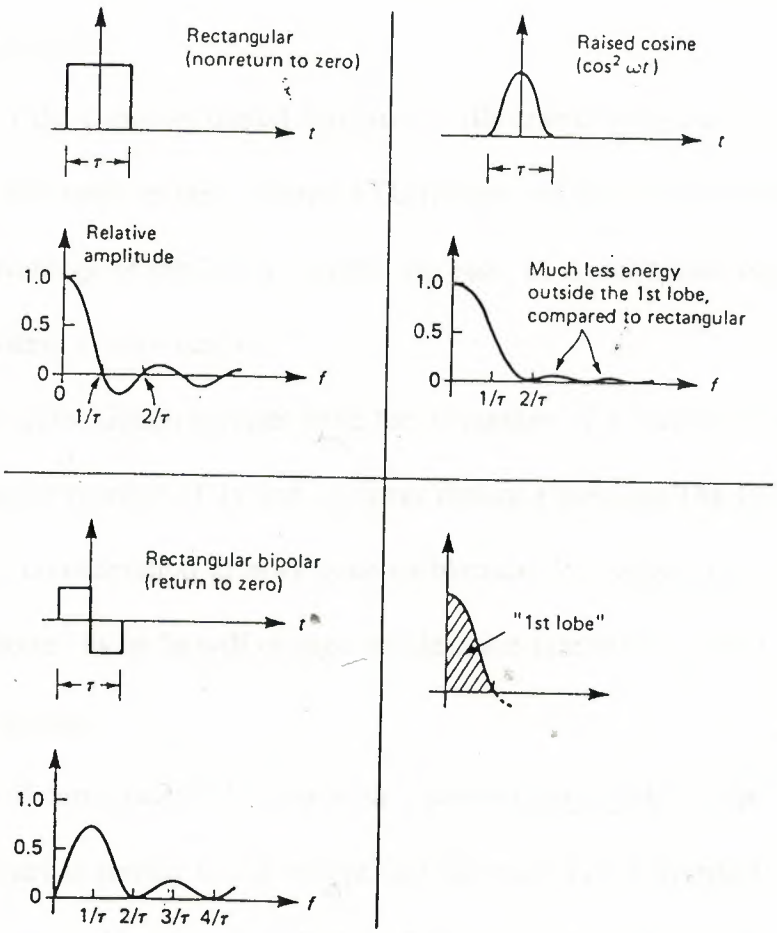


Figure 2.2 Frequency spectra for three different digital transmission

2.6 DIGITAL TRANSMISSION FORMATS.

Most digital data is generated by computers and terminals that usually operate internally on a parallel TTl-level signal format.TTl levels are 0 to .8 V for a logic 0 and 2 to 5 V for a logic 1 input level.Also output current levels are typically less than 16 mA.

Transmitting binary computer data over distances greater than a few a few meters requires circuitry other than TTL because capacitance and line resistance will limit the frequency response and distort the pulses. In addition it is often undesirable or impossible to transmit the dc component of typical TTl signals.

Some of the common digital formats are illustrated in figure 2.3.The NRZ signal is the same as the common TTL format and NRZ-B is a bipolar version.

The advantage of the RZ is that the increase in signal transitions will help in system synhronization.

Bipolar transmission formats have the advantage of a zero dc component assuming an equal number of 1s and 0s occur during a message.The DC component is an important consideration in nosy systems because dc changes due to short burst of continuous 1s or 0s will change the desicion threshold and can result in more errors.

The AMI format,called bipolar with a percent duty cycle by the telephone industry,is similar to RZ except that alternate 1s are inverted. The dc component is less than for RZ,the minimum bandwith is less than for RZ biphase.An additional advantage of AMI is that, by depecting violations of the alternate-one rule,transmission errors can be detected.

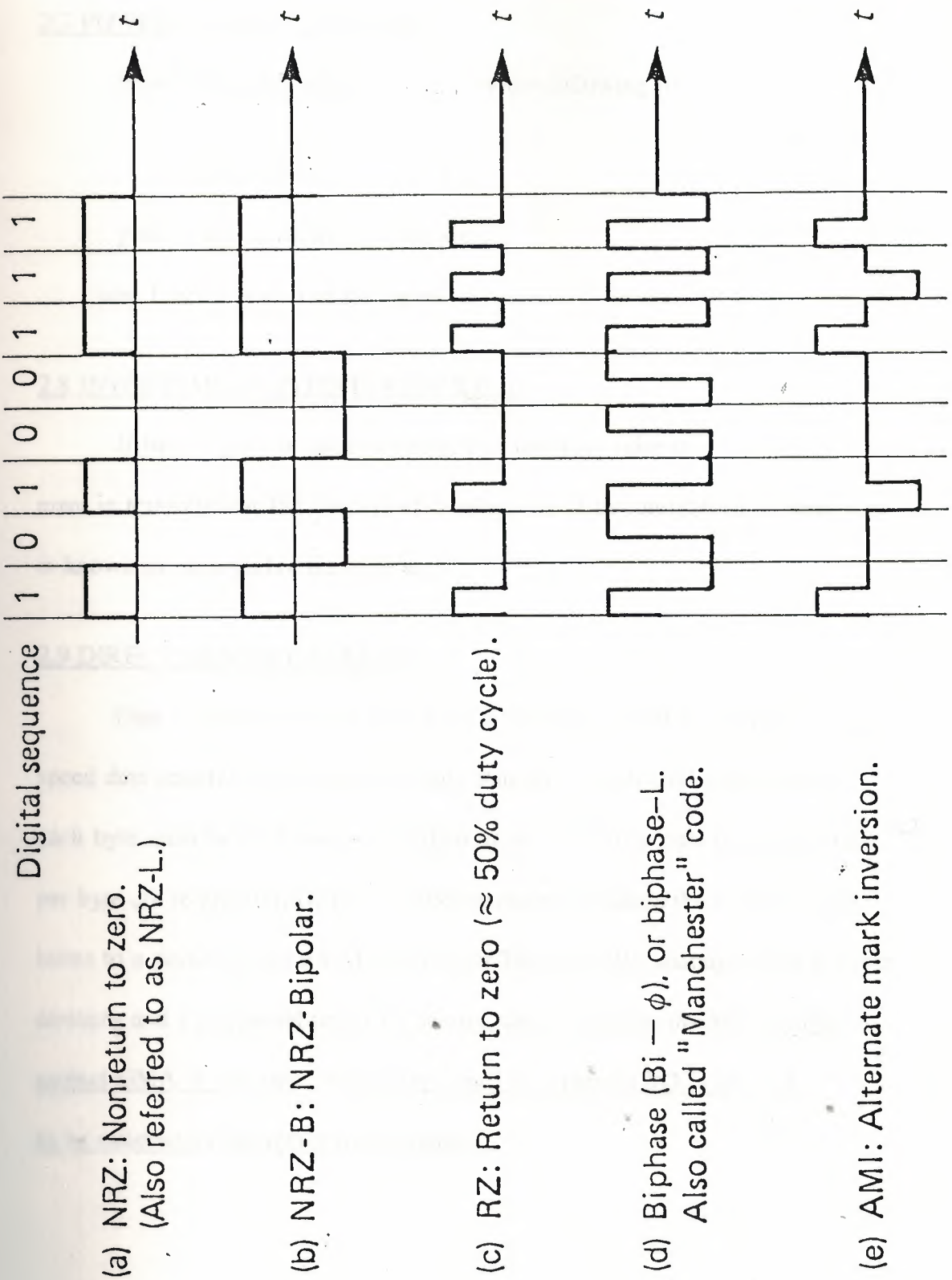


Figure 2.3 A few digital formats.

2.7 POWER IN DIGITAL SIGNALS

Power in digital signals is given by the following formula:

$$P = (t/T)\ V.V/R \qquad 2.1$$

given that t is duration of the signal

and T is the period of the signal

2.8 INTERSYMBOL INTERFERENCE (ISI)

If two neighbour pulses overlap this will give raise to error in transmission.The process of overlapping of two neighbour pulses is known as intersymbol interference.

2.9 DIRECT MEMORY ACCESS.

Direct Memory Access (DMA) is a commonly used technique for high speed data transfer.In interrupt I/O, data transfer is relatively slow because each byte must be read and then written to its destination;thus two instruction per byte are required.In DMA, the microprocessor releases the control of the buses to a decice called a DMA controller.The controller manages data between memory and a peripheral under its control, thus bypassing the MPU.In this project DMA is not used because the speed of inperrupt I/O is deemed to be satisfactory for remot robot control.

3 MICROPROCESSOR BASED COMMUNICATION

3.1 INTERFACING.

Interface has a broad range of meanings in the computer world:it can refer to the hardware or software aspects of connecting together anything from large-scale system components down to indivi diual chips.This section considers the hardware interfaces requ'ired between internal system buses and the outside world.Two significant points in interfacing are;

3.1.1 MATCHING OF ELECTRICAL REQUIRMENTS.

The interface must be able to match the electrical requirments of the internal system bus on one side and the requirments of the external devices on the other.

3.1.2 MATCHING OF TIMING REQUIRMENTS.

The interface has to match speed with the internal system bus on one side and accommodate the timing requirments of the outside world devices on the other.

3.2 ACCESSING THE I/O INTERFACE.

Two approches to I/O bus organisation are examined here:

(a) Memory mapped I/O

(b) Isolated I/O

3.2.1 MEMORY MAPPED I/O.

In this scheme,the I/O interface chips are connected to the system address and data buses in exactly the same way as a memory chip.The advantages of this approach are listed below.

(a) Since each I/O chip requires typically no more then 16 locations,the address space of even an 8-bit processor at 64K bytes is so large that there is no real restriction on the number of I/O chips that can be addressed.

(b) No additional buses or control signals are required

because those provided for the memory can be shared.

(c) The number of machine code instruction in a processor's instruction set is limited.Since no machine codes are required to handle I/O seperately,the instruction set can be enriched in other areas.In addition,usually very comprehensive range of instructions available to access memory can also be used for I/O operations.

A disadvantage of this approach is that the I/O chips encroach on the overall address space available for memory.However,since individual I/O chips use very few locations,this does not usually constitute a serious problem.

This scheme is widely used and is application to all microprocessors.

3.3 ASYNCRONOUS TRANSMISSION.

Asynchronous transmission is used for low-speed,inexpensive data equipment.Asynchronous transmission begins when the line is brought from mark to space.This first bit is called the start bit.the start bit is immediately followed by the data bits.Depending to the application,there are between 5 and 8 data bits.A parity bit is usually used.Figure 2.1 illustrates the character format.

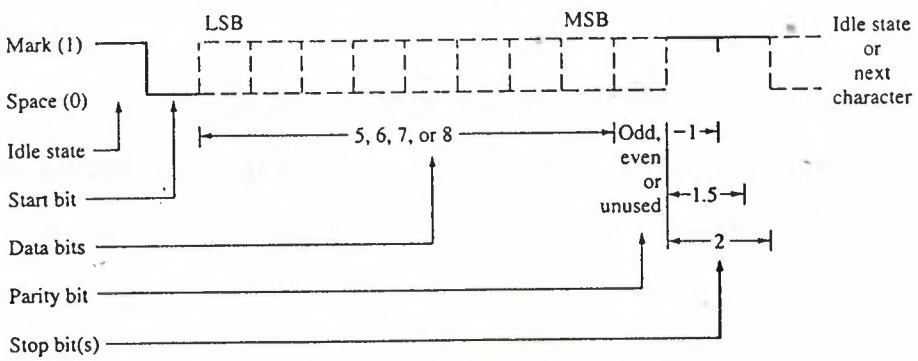


Figure 2.1 Character Format for Asynhcronous Communication

3.3.1 START BIT

When data is not being tranmitted,the communication line is said to be in the idle or mark state.When a character is going to be sent,the transmitter brings the line to a logic 0 for 1 bit time,the start bit.It is this bit that is used by the receiver to resynchronize its receiving circuitry.the asynchronous receiver is designed to detect the transition from logic 1 to logic 0.Since noise is a problem on a communication line,receivers are designed to sample the line several times before recognizing the beginning of the data bits.

3.3.2 DATA BITS.

Data bits follow the start bit.The least significant bit of the data follows the start bit.The data bits contain the information to be tranmitted and received.Same transmitters and receivers are designed for 5,6,7 or 8 bits.

3.3.3 PARITY BIT.

Parity is a method of error detection.A parity bit is an optional bit that follows the data bits.If parity is used,there are two types,even or odd.In this project parity bits will not be used because there reliability in IR communication links is not believed to be sufficient.

3.3.4 STOP BIT.

Following the data bits and the parity bit (if used),the transmitter sends a stop bit or bits.These bits are logic 1s and indicate the end of the character.The duration of the stop bits generated by UART.

3.3.5 BIT RATE.

The time to transmit (or receive) a bit is known as bit

time or bit interval.The reciprocal of the bit time is known as bit rate.In equation form,this is expressed as

$$\text{Bit rate} = 1/tb \qquad (2.3)$$

where tb is the bit rate.

INFRA-RED IN FREE SPACE COMMUNICATION

4.

4. INFRA-RED RADIATION IN COMMUNICATION

4.1 INFORMATION THEORY ASPECT.

A detailed mathematical and geometrical development by Shannon has resulted in the general expression of channel capacity for the classical electromagnetic case of

$$R_{(P=N)} = B \log\left(\frac{N}{P_0}\right), \qquad (4.1)$$

A derivation of channel capacity with consideration of quantum effects has been recently accomplished.The results are valid for systems in which only a single transmission mode of the field is utilized,such as in coaxial cable and waveguides.This condition exists whenever the field polarization distribution over any plane perpendicular to the direction of propagation can be considered in variant.This condition can be considered typical of a long-range infra-red communication system.The entropy per mode for white noise was determined to be

$$H = \log(1 + \bar{m}) + \bar{m} \log\left(1 + \frac{1}{\bar{m}}\right), \qquad (4.2)$$

where m is the avarage number of photons in a mode.The energy per mode E is then hfm.In bandwith B,from the quantum mechanical considerations,B modes per second are present:then the incident power is given by

$$P = \bar{E}B = hf\bar{m}B. \tag{4.3}$$

By substituting for m in equation 4.2 we obtain

$$H = \log\left(1 + \frac{P}{hfB}\right) + \frac{P}{hfB}\log\left(1 + \frac{hfB}{P}\right). \tag{4.4}$$

The information or entropy rate will then be given by

$$= B\log\left(1 + \frac{P}{hfB}\right) + \frac{P}{hf}\log\left(1 + \frac{hfB}{P}\right). \tag{4.5}$$

And the upper limit of information capacity

$$C = B\log\left(1 + \frac{S}{N + hfB}\right) + \frac{S+N}{hf}\log\left(1 + \frac{hfB}{S+N}\right) - \frac{N}{hf}\log\left(1 + \frac{hfB}{N}\right). \tag{4.6}$$

4.2 SEMICONDUCTOR IR COMPONENTS.

In a pure semiconductur material the number of electrons and and holes must be always be equal and this number can be changed by changing the temperature.There is another way of changing the electron and hole populations and that is by doping the semiconducture with atoms whose valences differ from thet of the host material.

One of the most fundamental of electronic devices involves

forming a junction between p and n materials.Such a device acts as a diode,i.e a device that will pass current in one direction but not in the other.Even more interesting from my point of view is that when a current is flowing through the junction it may emit radiation.

Suppose we imagine making a junction by simply placing pieces of n and p material in physical contact.Because there are more electrons in the conduction band og the end material than there are in the conduction band of the p material,electrons tend to flow from the n to the p conduction band.Similarly holes flow from the p to the n valance band.Because the electrons and holes carry charge,this flow causes the two sides of the junction to become electrically charged.The n side becomes positively charged ,the p side negatively charged.The resulting charge seperation produces an elecrtic field which opposes the diffusive flow and eventually an equilibrium situation is reached when there is no net charge flow.The charge builed up causes an energy level barrier of height ev to appear at the interface as shown in figure 4.1 where V is known as the contact or diffusion potential.

We know consider what happens when an external potential is applied.Suppose the p material is made negative and the n material positive;in this case the external potential adds to the internal potential,and the total internal potential barrier at the interface becomes larger.It is know more difficult for electrons in the n material to surmount this barrier,and in addition there are few electrons about in the p material to travel from the p to the n side of the junction.Fig 4.2(a)

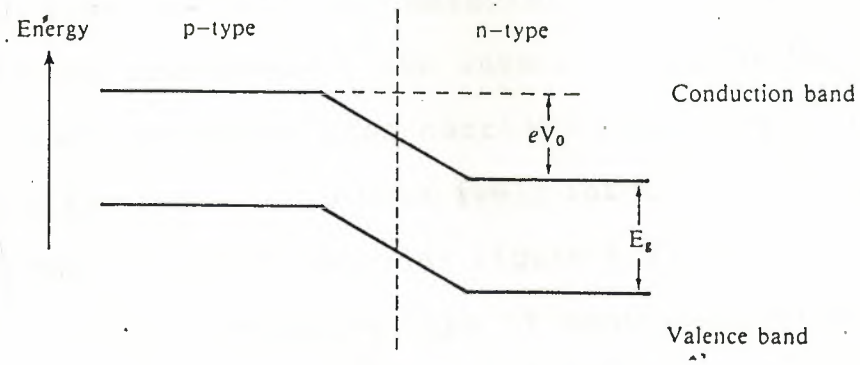


Figure 4.1 Energy level barrier created when a p-n junction is formed.

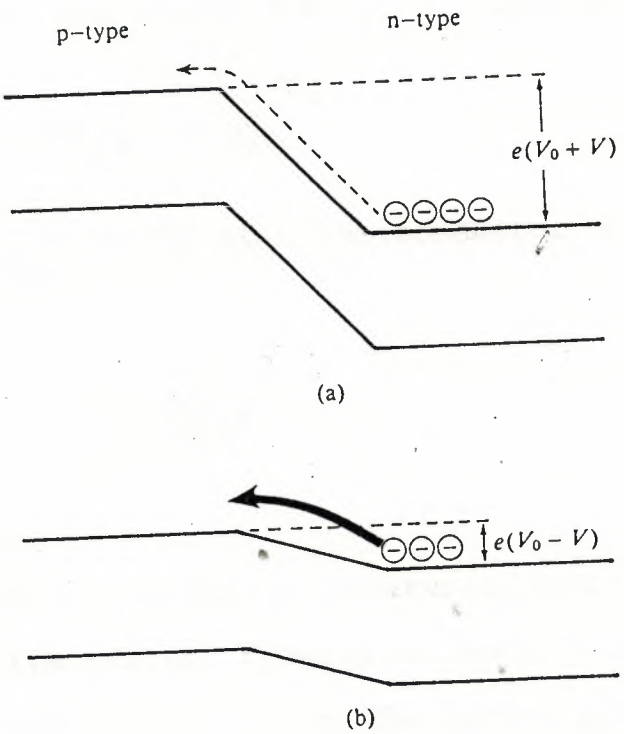


Figure 4.2 The barrier height at a p-n junction when (a) reverse bias (b) forward bias of magnitude V is applied.

The result is a small current which conventionally is taken as flowing from the n to the p material.In contrast to this,when the polarities are reversed the internal barrier height is reduced making it easier tfor carriers to surmount the barrier,and the result is a relatively large conventional current flow from the p to the n material figure 4.2(b).The junction may be made either from a single type of semiconductor material (forming a homojunction) or from different types (when a heterojunction is formed).

If an electron makes a radiative transition from the bottom of the conduction band (energy Ec) to the top of the valance (energy Ev) then the wavelength of the light emitted is given by

$$\frac{hc}{\lambda} = E_c - E_v = E_g. \qquad (4.7)$$

The reflectance (R) of a semiconductor-air interface by using the formula

$$R = \left(\frac{n-1}{n+1}\right)^2 \qquad (4.8)$$

The amount of population inversion, and hence gain is determined by the current flowing.At low current any population inversion achieved is offset by the losses present and lasing does not occur.Any radiation generated is due to spontaneous emission (as in a LED) which increases linearly with the drive current.Beyond a critical current (the treshold current),however lasing commences and radiative output then increases vary rapidly with increasing current,as shown in figure 4.3

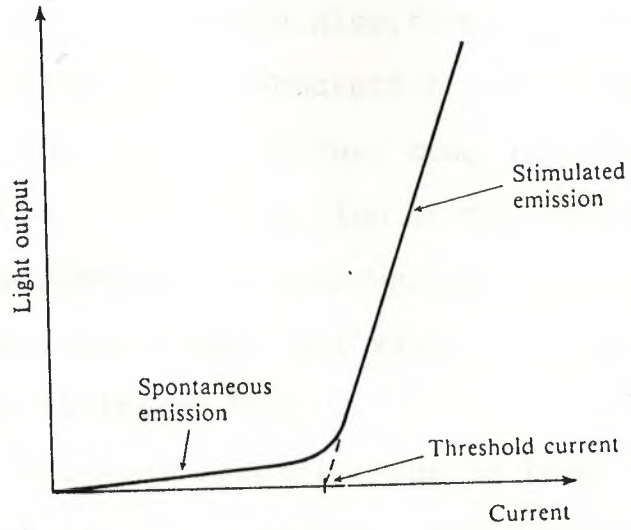


Fig 4.3 Light output-current characteristic of an ideal semiconductor IR emiter.

A major difficulty with homojunction lasers is that there is little to stop the radiation from spreading out sideways from the gain region suffering loss instead of gain.For this reason homojunction lasers can usually omly be operated in pulsed mode and with current densities of the order of 400 Amm-2 or higher.

In this project I am using laser based on GaAs as the active region emit radiation of 0.94 micrometer.

4.3 ATMOSPHERE AS A TRANSMISSION MEDIUM.

The gases present in greatest abundance in the earth's atmosphere are nitrogen,oxjgen,water vapour,carbon dioxide,methane,nitrous oxide,carbon monoxide and ozone.The two gases present in the highest concentrations,N2 and O2,absorb almost exclusively in the far ultraviolet.

In practice,it is difficult to determine the exact path loss through the atmosphere.There are number of complications.For example,in many wavelength intervals the absorbtion coefficient

is not independent of wavelength.Hence a different transmittance is present for each wavelength.Also,temperature and total pressure will influence the absorption coefficient,thereby modifying the transmittance.Another complication is that the absorption coefficient is a function of the concentration of the gases that will absorb.Absorber concentration,total pressure,and pressure,and temperature will all vary as a function of geography,season,altitude.

The actual value of transmittance is best determined experimentally if we can do so for a given path.However,there have been sufficient data collected by various sources for different conditions that one can by judicious and logical use of the data approximate the transmittance with reasonable accuracy.

4.4 GENERAL TRANSMITTANCE CURVES AND TABLES.

The general atmospheric transmittance curve as a function of wavelength is presented in figure 4.4.In table 4.1 water vapour transmission coefficients are listed for differet windows (wavelength intervals) of figure 4.5

If the atmospheric path loss is assumed to be composed of two major factors,loss due to scattering and loss due to absorbtion,then we can calculate the over-all transmittance by determining the transmittance for absorbtion and the transmittance for scattering at the desired frequency.

The formula for transmittance when considering scattering is:

$$T_r(h, \theta) = e^{-h/L(h)} \sec \theta. \qquad (4.9)$$

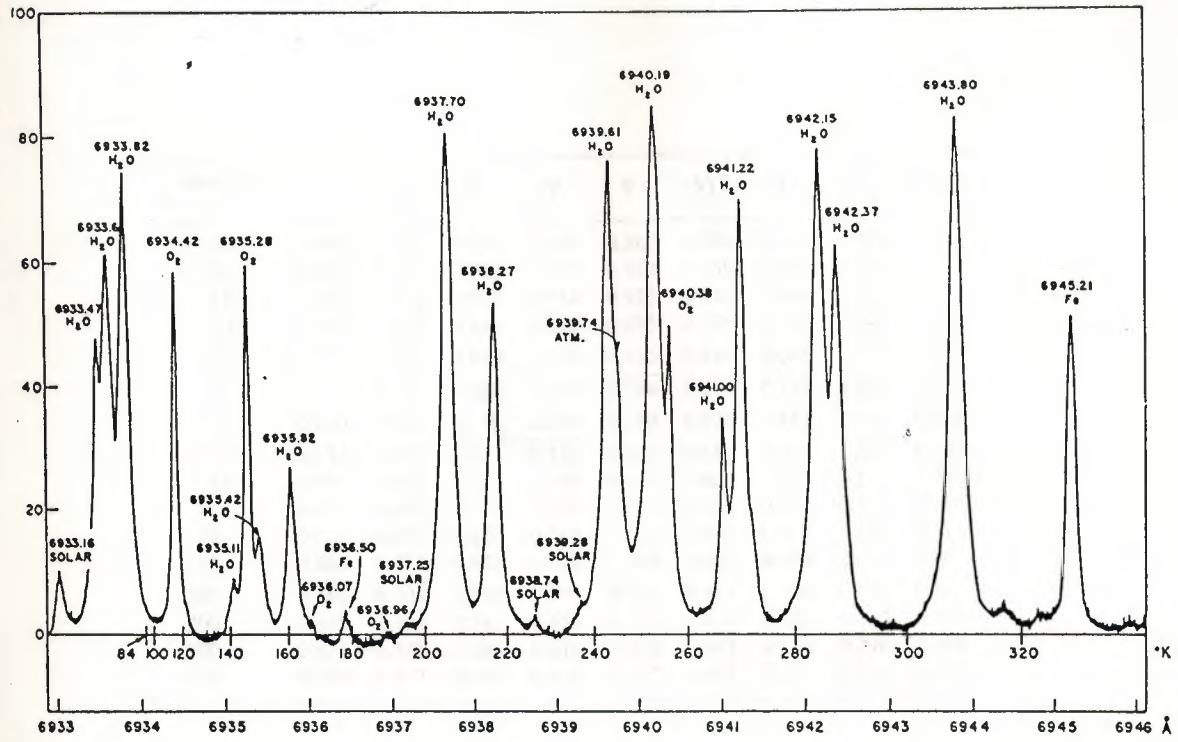


Figure 4.4 Atmospheric absorption at the laser frequency

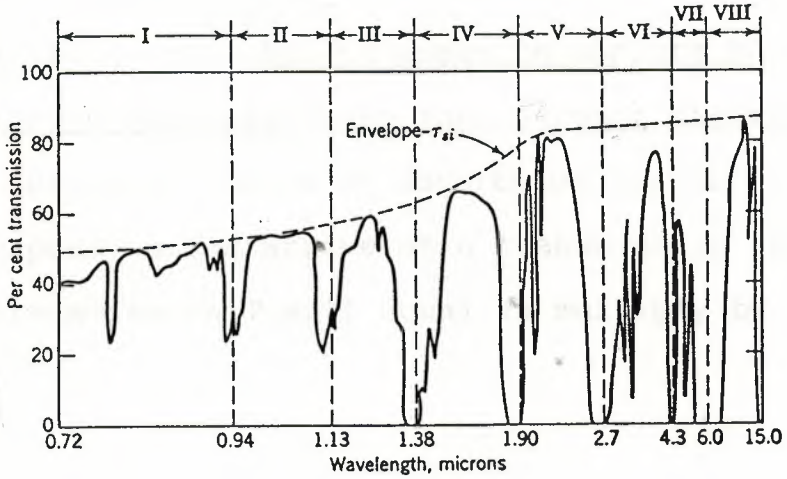


Figure 4.5 General atmospheric transmittance curve versus wavelength.

Table 4.1 Water vapour transmission coefficients

w Window	I	II	III	IV	V	VI	VII	VIII	I-VIII
0.01	0.997	0.996	0.987	0.979	0.965	0.964	0.915	0.942	0.978
0.02	0.996	0.995	0.982	0.970	0.950	0.949	0.879	0.918	0.969
0.05	0.993	0.992	0.971	0.954	0.925	0.920	0.816	0.875	0.951
0.1	0.990	0.988	0.959	0.935	0.895	0.889	0.749	0.828	0.932
0.2	0.987	0.984	0.940	0.910	0.855	0.846	0.665	0.765	0.907
0.5	0.979	0.975	0.912	0.861	0.784	0.776	0.557	0.685	0.866
1.0	0.970	0.965	0.878	0.810	0.730	0.726	0.487	0.629	0.831
2.0	0.954	0.950	0.830	0.750	0.680	0.680	0.426	0.578	0.793
5.0	0.934	0.922	0.763	0.680	0.618	0.623	0.351	0.517	0.744
10	0.908	0.892	0.715	0.630	0.576	0.584	0.313	0.475	0.706
20	0.874	0.850	0.670	0.582	0.536	0.546	0.274	0.437	0.666
50	0.806	0.774	0.622	0.526	0.488	0.502	0.229	0.390	0.609
100	0.746	0.704	0.576	0.488	0.454	0.469	0.201	0.359	0.562
200	0.688	0.642	0.541	0.452	0.422	0.436	0.175	0.330	0.519
500	0.623	0.568	0.496	0.410	0.384	0.403	0.147	0.296	0.469
1000	0.580	0.517	0.465	0.378	0.357	0.377	0.128	0.272	0.435

where V is the visual range in kilometers, R is the range in kilometers and $q=.5V^{1/2}$. But in order to compute the realistic tranmittance, we must also take into account absorbtion. Using the curves or tables of absorbtion for different amounts of water vapour, we can arrive at a transmission factor Ta. The complete transmission T will equal Ta multiply by Ts.

BACKGROUND ENERGY CONSIDERATIONS
5.

5. BACKGROUND ENERGY CONSIDERATIONS

The limitation on the sensetivity is often the result of the background energy that is incident at the receiver.By incident background energy,I mean non-signal photons that arrive at the and are within the spectral acceptance band of the receiver.

There are many cases where the background consists of different sources.

5.1 NATURAL BACKGROUND SOURCES.

The effective background of some different natural sources are listed in Table 5.1

Table 5.1 Typical values of luminane for various natual sources.

Source	Luminance, foot-lamberts
Sun, as observed from Earth's surface at meridian	4.7×10^8
Moon, bright spot, as observed from Earth's surface	730
Clear blue sky	2300
Lightning flash	2×10^{10}

5.2 SKY BACKGROUND.

Above the earth's atmosphere,the radiation from the sun is substantially constant in both quality and quantity.Figure 5.1 shows relative spectral distribution of energy in the sunlight above the earth's atmosphere.On a clear day,solar radiation is

scattered selectively in its passage through the earth's atmosphere.This selective scattering causes the sky to be blue,and causes the radiation of short wavelengths to be correspondingly reduced in intensity in the unscattered beam.

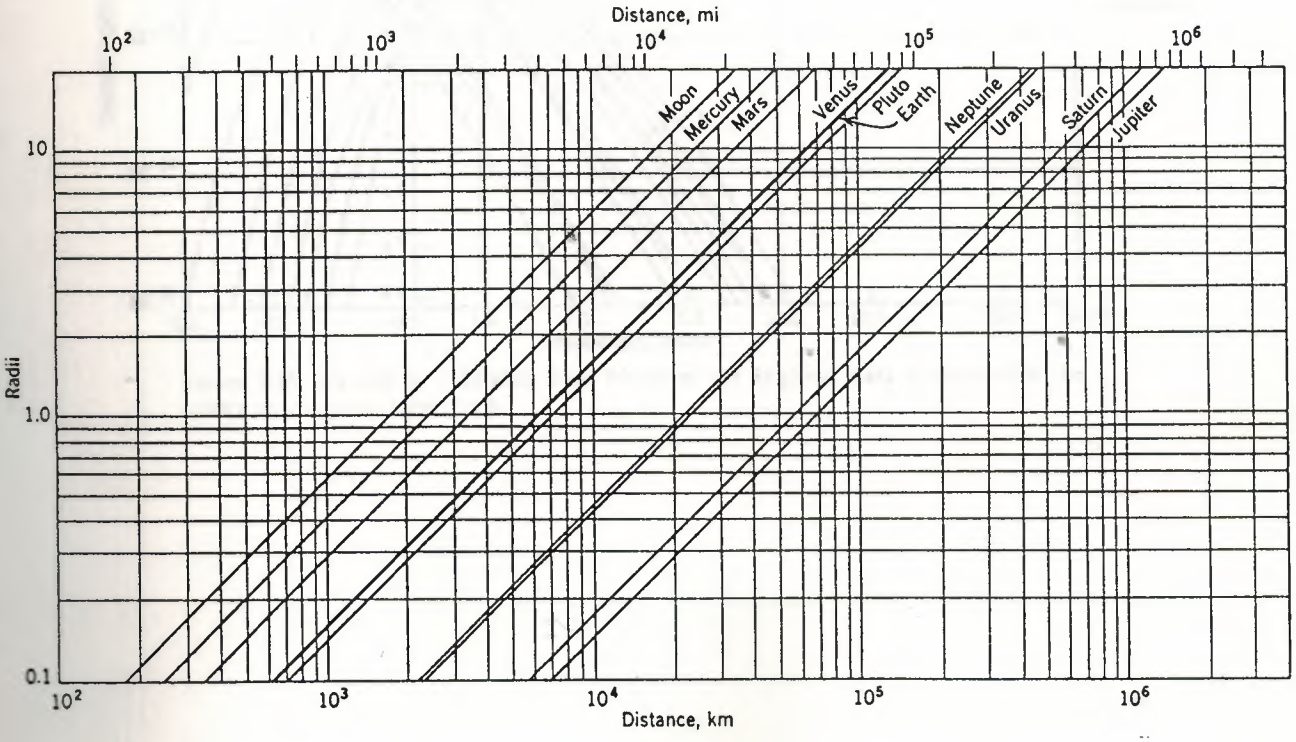
5.3 STAR BACKGROUND.

The background light from stars has been determined by astronomers over a long period of time.The measurment unit traditionally used is the stellar magnitude,which is defined as

$$M=-2.5\log(I/Io) \qquad (5.1)$$

where I is the effective irradiance in watts/cm2 and Io is some standard irradiance.The visual magnitude of various stars with which I am concered is given in Table 5.2.

Table 5.2 Visual magnitude of various stars.



The irradiance of various stars has been calculated from there visual magnitude and effective temperature.The results are shown in figure 5.1 with the watts/cm2 (spectral power density) shown as a function of wavelength.

Figure 5.1 calculated irradiance from fifteen of the brightest stars.

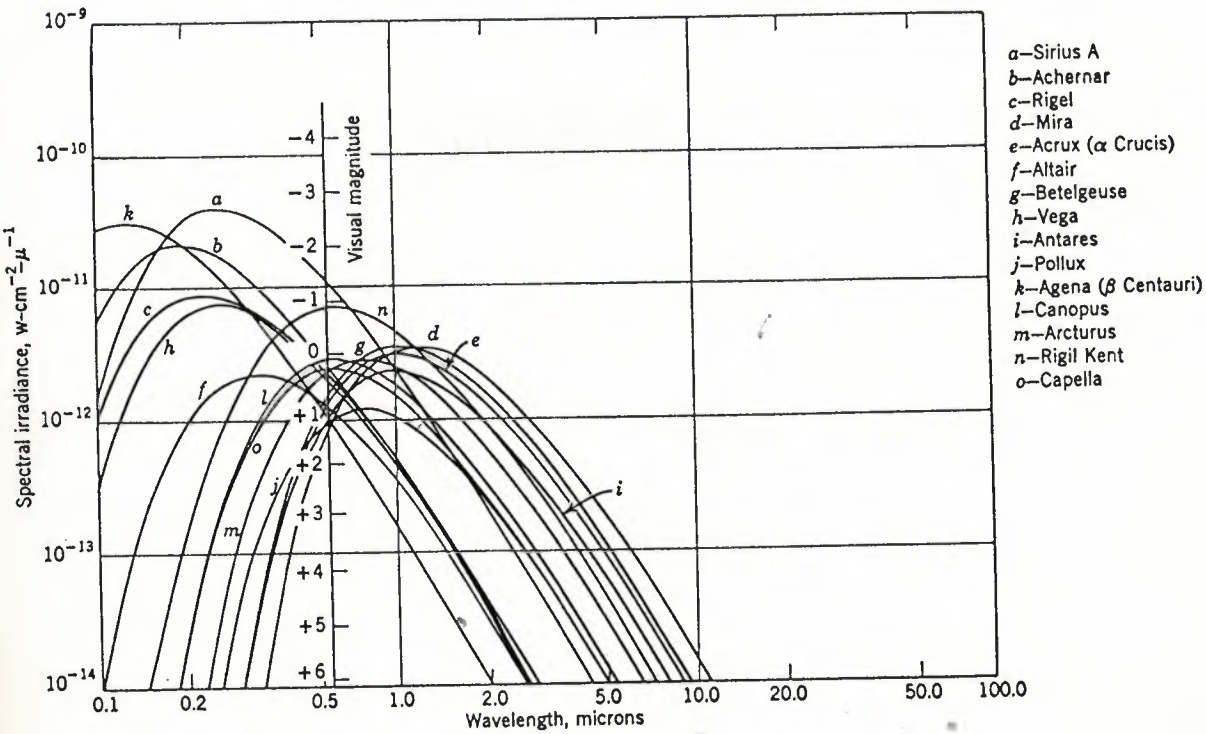


Figure 7-25 Calculated irradiance from fifteen of the brightest stars (from outside the earth's atmosphere) (from [7-6]).

HARDWARE
6.

6. HARDWARE.

This part is related to hardware interfacing as it applies to the IBM PC.

6.1 MICROPROCESSOR BUSES.

The 8088 is intended to be used in a three-bus system, figure 6.1 depicts this. The address bus provides an address to memory and I/O devices. The data bus provides a pathway along which data can flow between the microprocessor and the memory, or I/O devices. The control bus provides control signals that control the flow of information along the data bus.

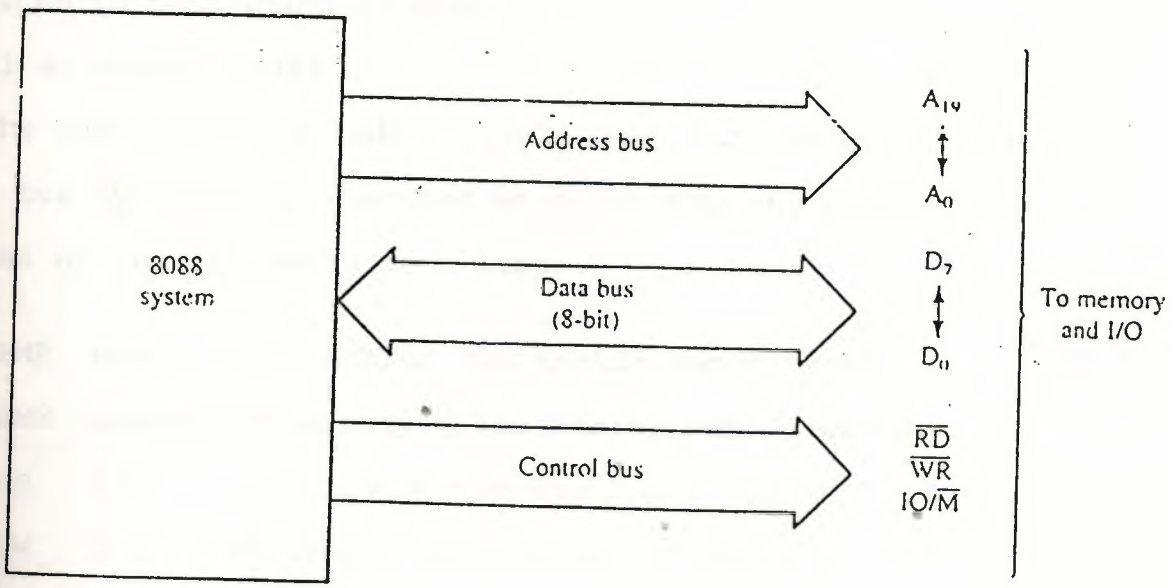


Figure 6.1 Microprocessor Buses.

The address bus contains 20 address lines connected to two logical address spaces,the memory address space and the I/O address space.All 20 lines are active during a memory bus cycle,implying a memory address range from 00000H to 0FFFFFH (1 mega byte).Only 16 lines are active during an I/O bus cycle,which limits the I/O (port) address space to range 0000H-0FFFFH(64k bytes).In the IBM PC only lower 10 of these 16 lines decoded during an I/O instruction,thus limiting the port space to the range 0000H-03FFh (1k byte).(Any memory referance instruction causes a memory bus cycle,whereas only IN and OUT instructions cause I/O bus cycle)

The data bus is an eight bit,bidirectional pathway connected to devices in both address space. It is connected to I/O devices as well as memory chips.

The control bus includes signals that correspond to the type of the bus cycle being executed.At a minimum,the control bus contains of the following four lines:

MEMR memory read,active low during memory read.

MEMW memory write,active low during memory write.

IOR I/O read,active low during I/O read.

IOW I/O write,active low during I/O write.

The MEMR,MEMR lines are connected to the memory chips, and the IOR,IOW are connected to the I/O devices.During microprocessor-controlled bus cycles,only one of these lines will be active. Figure 6.2 depicts the 8088 pinout.

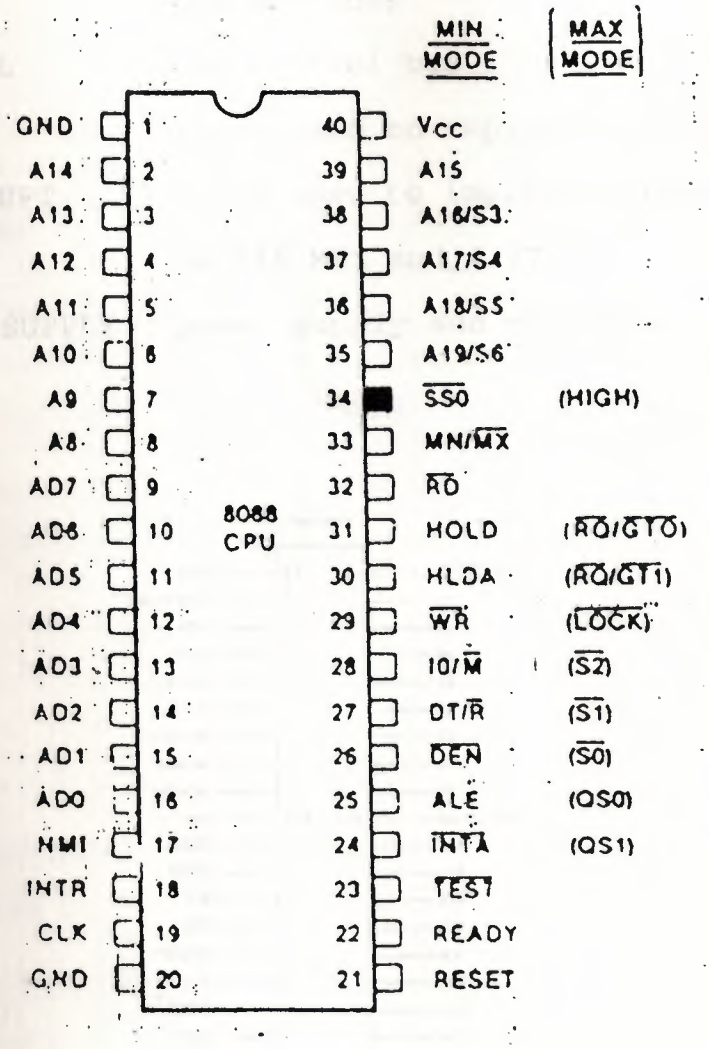


Figure 6.2 8088 pinout.

2 THE I/O CHANNEL.

The I/O channel is a set of 62 lines connected to five card-
ge connectors on the system board.Nonsystem hardware is added
the pc by simply plugging cards into I/O channel.Because of
s central role in hardware interfacing,I will keep the I/O
annel in focus throughout the rest of the desertation.

The I/O channel lines can be classified by the function they
erform:

ADDRESS	the address bus
DATA	the data bus
CONTROL	the control bus
DMA	lines used to impliment DMA functions
INTERRUPT	lines used to impliment interrupt functions
ClOCK	14.318 MHz and 4.77 MHz
POWER SUPPLY	power supply and ground

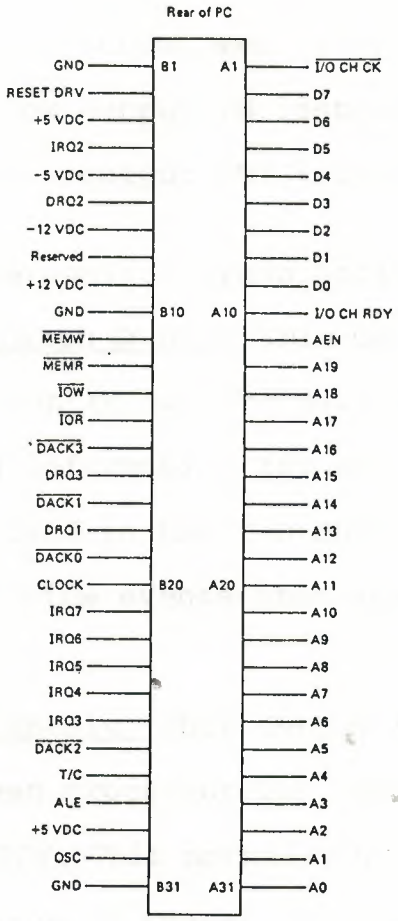


Figure 6.3 I/O Channel

Address: Output lines A0-A19 from the address bus.The 74Ls373 demultiplexing chip drives these lines as well as the system board address bus.

Data: Lines D0-D7 from the bidirectional data bus.The data bus is driven by the 74ls245 bidirectional buffer.

Control: In addition to the usual control lines, there are several unrelated lines in this group.First we have the following control lines,which come directly from the 8288 bus controller:

MEMR active-low,output,memory read

MEMW active-low,output,memory write

IOR active-low,output,IN instruction

IOW active-low,output,OUT instruction

Other lines in the control group include the following:

ALE-Address Latch Enable. This output signal comes directly from the 8288 bus controller.The main function of this signal is to provide timing information for the 74ls373 demulteplexing latch.ALE can be used in the I/O channel to find the beginning of a bus cycle-to time events that must be synchronized to bus cycle.

AEN-Address Enable. This output signal allows us to distinguish between processor bus cycle and DMA bus cycle.

I/O Channel RDY. This normally high input line can be pulled low by a slow device to insert processor wait-states.

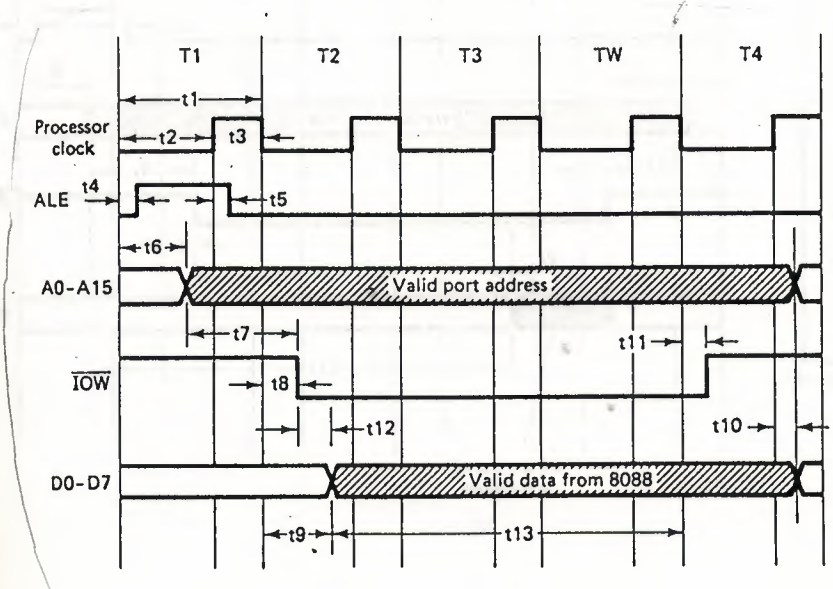
I/O Channel Check. This normal high input line is pulled low to indicate a memory or I/O device parity error.

Reset DRV. This output signal is active-high during power-on and can be used to reset or initialize I/O devices.

6.3 I/O CHANNEL AND PROCESSOR INITIATED BUS CYCLES

Designing an interface for an I/O or memory device requires a detailed understanding of bus cycles.Control signals that typically enable or strobe the I/O or memory devices must meet the timing requirments of the devices.

Figure 6.4 shows a typical memory-write bus cycle.The figure is simplified version of the timing of diagram found in the Intel Microsystem Components Handbook.At the top of the figure,we find the processor clock.The memory-write bus cycle consists of four clock periods,labeled T1,T2,T3,and T4.At the begining of the bus cycle,during T1,ALE goes high,enabling the 74LS373 demultiplexing latch.Shortly thereafter,the address becomes valid,propagating through the 74LS373 to the system and I/O channel address bus.



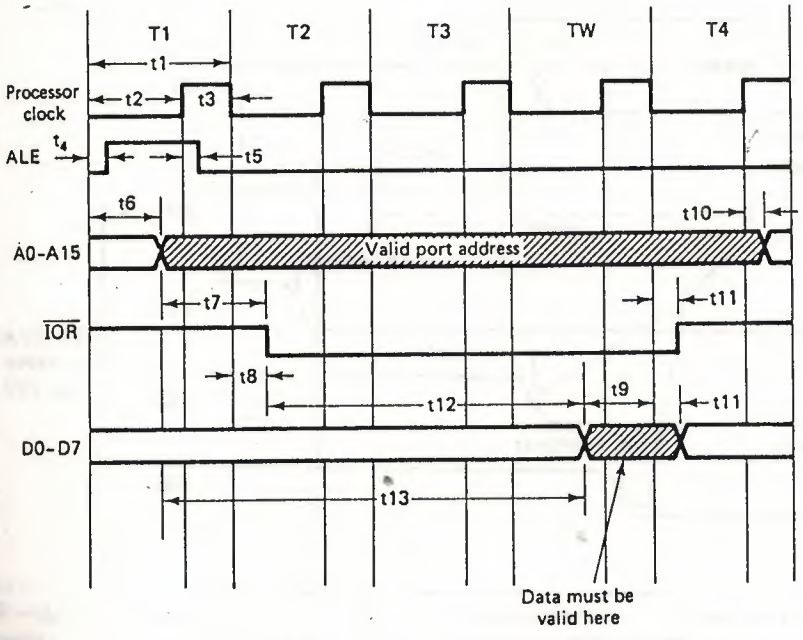
Symbol	Max.	Min.
t1	–	209.5
t2	–	124.5
t3	–	71.8
t4	15	–
t5	15	–
t6	128	16
t7	–	91.5
t8	35	10
t9	122	14
t10	–	10
t11	35	10
t12	112	–
t13	–	506.5

*All times are in nanoseconds

Figure 6.4 Memory-Write bus Cycle

Near the end of T1,ALE falls,causing the 74LS373 to latch the address for the rest of the bus cycle.During T2,MEMW goes low,followed by valid data on the bus.MEMW goes high at the beginning of T4 when both the address and data are still valid. The rising edge of MEMW is often used to strobe data into memory.

The memory-read bus cycle in figure 6.5 shows a similar pattern.T1 is essentially the same as for a memory-write bus cycle.The falling edge of MEMR is typically used to enable the device being read.The device responds with the valid data that is strobed into the processor at the beginning of T4.



Symbol	Max.	Min.
t1	–	209.5
t2	–	124.5
t3	–	71.8
t4	15	–
t5	15	–
t6	128	16
t7	–	91.5
t8	35	10
t9	–	42
t10	35	10
t11	–	10
t12	–	551.5
t13	–	668

*All times are in nanoseconds

Figure 6.5 Memory Read cycle.

The I/O bus cycles are similar to the memory bus cycles except for the automatic insertion of one wait-state by system board logic.Figures 6.6 and 6.7 shows that the I/O bus cycles have one added clock period,TW (t-Wait).The insertion of wait state approximately 210 ns to the time available to I/O device.

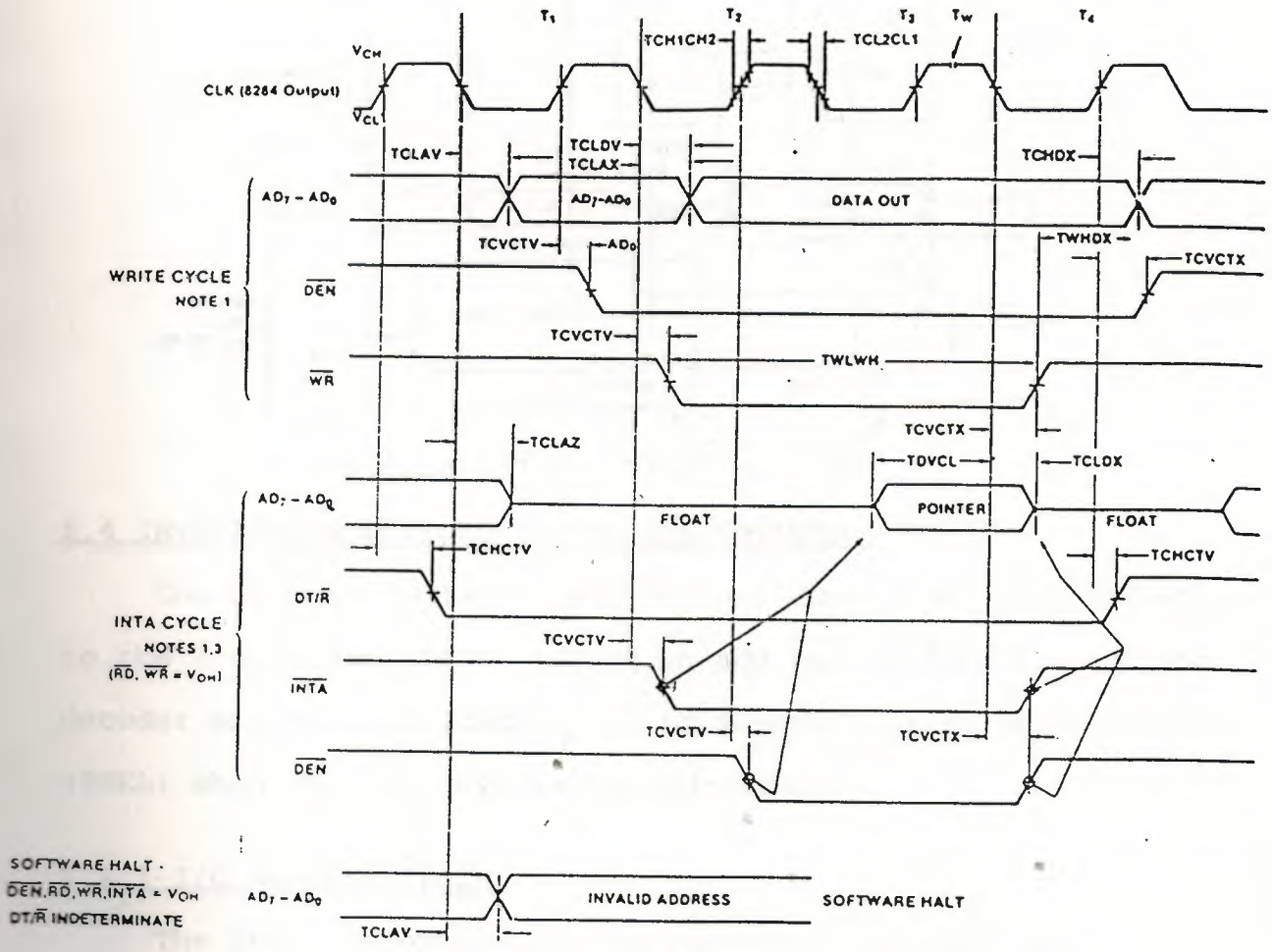


Figure 6.6 I/O Write Bus Cycle.

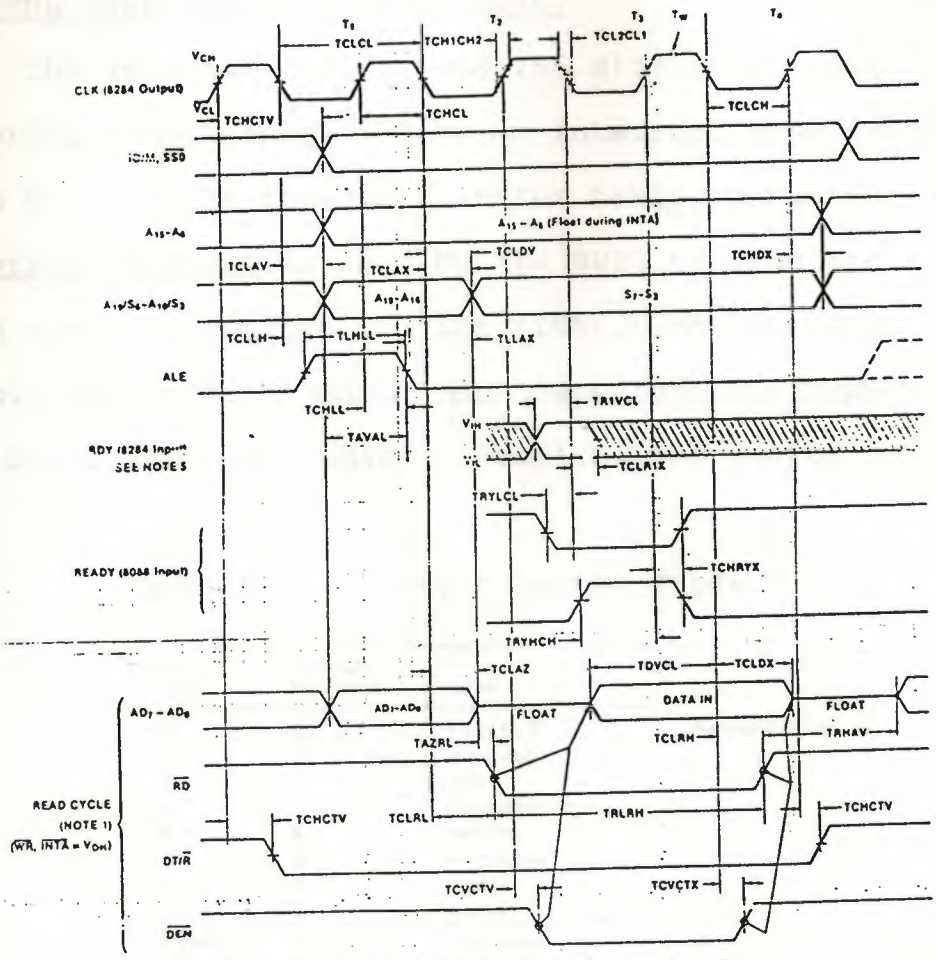


Figure 6.7 I/O Read Bus Cycle.

6.4 INTERFACING DEVICES TO THE I/O CHANNEL.

One of first tasks to be performed when interfacing a device to the I/O channel is to design an address decoder.The address decoder monitors the address bus to generate a port select signal (PSEL) when the I/O devices is addressed.

6.4.1 I/O ADDRESS SPACE.

The 8088 microprocessor is capable of addressing 64K different ports via 16 address lines.However, the IBM PC system board decodes (recognizes) only the lower 10 address lines,restricting the number of available ports to 1024.The lower half of the 1024 ports arereserved for the system board itself,and the upper half is dedicated to the I/O channel.Many

6.5 THE 8088 INTERRUPT STRUCTURE.

The 8088 can field up to 256 different types of interrupts,each specified by an interrupt type number ranging from 0 to 255.An interrapt vector table,containing up to 256 interrupt vectors,is used by the 8088 to find the location of each specific service routine (ISR).Each inperrupt vector is a double-word pointer containing the offset and segment address of the associated ISR.Table 6.1 depicts the vector table.

Table 6.1 Interrupt Vector Table.

Interrupt type	Interrupt type (hex)	Name	
0	0	divide by 0	Address 00000H
1	1	single step	
2	2	NMI	
3	3	breakpoint	
4	4	overflow	
5	5	print screen	
6	6	unused	
7	7	unused	
8 IRQ0	8	time of day	8259A interrupt lines
9 IRQ1	9	keyboard	
10 IRQ2	A	unused	
11 IRQ3	B	COM2	
12 IRQ4	C	COM1	
13 IRQ5	D	unused	
14 IRQ6	E	diskette	
15 IRQ7	F	LPT1	
16	10	video I/O	BIOS entry points
17	11	equipment	
18	12	memory	
19	13	disk I/O	
20	14	serial I/O	
21	15	cassette	
22	16	keyboard I/O	
23	17	printer	
24	18	resident BASIC	
25	19	bootstrap	
26	1A	time of day	
27	1B	keyboard break	User-supplied routines
28	1C	timer tick	
29	1D	video install	
30	1E	disk install	
31	1F	video graphics	
32	20	DOS program terminate	DOS and BASIC interrupts
33	21	DOS function call	
34	22	DOS terminate address	
35	23	DOS fatal error	
36	24	DOS Ctrl Brk exit	
37	25	DOS absolute disk read	
38	26	DOS absolute disk write	
39-63	27-3F	DOS reserved	
64-95	40-5F	reserved	
96-103	60-67	reserved for user	
104-127	68-7F	available	
128-133	80-85	reserved for BASIC	
134-240	86-F0	reserved for BASIC	
241-255	F1-FF	not used	Address 003FFH

The table begins at the address 0000:0000 and is 1K byte in length (256 vectors, four bytes per vector). Note the order of the offset and the segment values. A useful rule to remember is that intel processors always store the least significant part of multibyte data in the low memory address, that is ,least=low.

When the interrupt occurs, the current CS, IP, and the flag word are pushed onto the stack(in that order). IP and CS are than loaded from the interrupt vector table, and the interrupt enable flag(IF) and the trap-single step-flag (TF) are cleared. Thus the ISR is entered with interrupts and single-step disabled. External inperrupts can be reenabled during the ISR with the STI (set interrupt enable flag) instruction. The ISR must not change any registers. If it does, the interrupted program will most likely produce errors.

6.5.1 EXTERNAL INTERRUPTS.

The 8088 has two pins that can be used to signal an interrupt. The NMI (nonmaskable interrupt) is positive edge-triggered and is normally used to signal "catastrophic" events like power failures. The IBM PC usesNMI to respond to three different interrupt sources-system board parity error, I/O CH CK, and an interrupt 8087 interrupt.

6.5.2 INTERNAL INTERRUPTS.

All internal interrupts have a higher piority than any external interrupt

6.6 EXTERNAL CONNECTIONS OF A UART.

A typical external pin assignments for internal block diagram of a UART is shown in figure below:

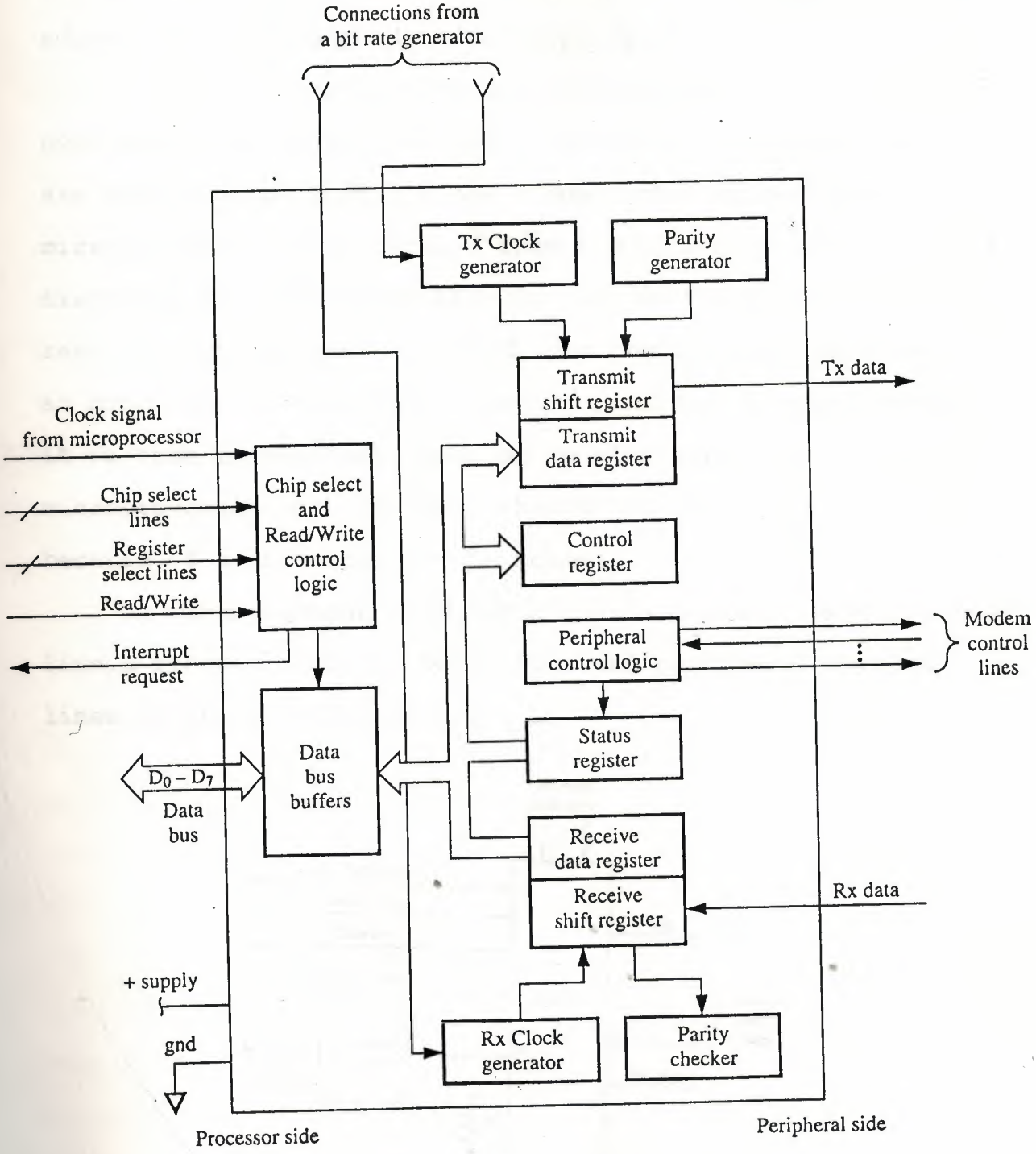


Figure 6.9 Typical External Pin Assignments for Internal Block Diagram of a UART.

The UART has chip select or chip enable pins that are used by microprocessor to select the device,that is,to enable the data bus buffers.These pins are connected to the microprocessor's address lines through decoder chips,as shown in figure 7.0.

Data is transferred between the microprocessor and a UART over an 8-bit bidirectional data bus.All of these data transfers are synchronized form a clock signal that drives the microprocessor or is derived from the microprocessor internal circuitry.The read-write line is used by the microprocessor to read or write data to the UART over the data bus.UART has also an interrupt request (IRQ) line to signal the microprocessor that it is time to send more data or receive data or to signal the microprocessor that the data should not be sent or received because of a situation at the modem.

On the peripheral side,UARTs have a transmit data (Tx Data) line,a receive data (Rx Data) line,and peripheral control lines,as shown in figure 6.9

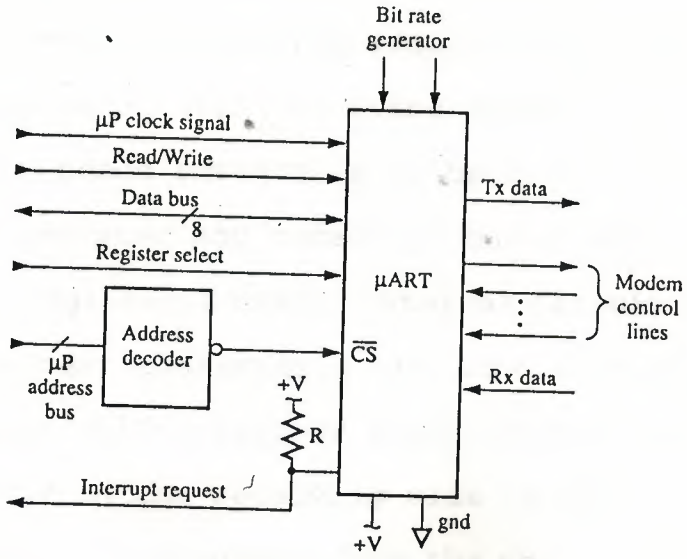


Figure 7.0 Typical Wiring Connections for a UART

Serial data is transmitted and received on the Tx data and Rx Data lines,respectively.Thus,a UART receives parallel from the microprocessor over the data bus and transmit it serially on the Tx Data line.Similarly,a UART receives a serial data on the Rx Data line and transfers it to the microprocessor in a parallel format over the data bus.Hence,the basic function of a UART is as a paallel-to-serial and serial-to-parallel converter.To transmit serial data,UART automatically insert the start,parity(in this projet there is no),and stop bits before transmitting the serially.After a UART receives a character on the Rx Data line,it "strips away"the start,parity,and stop bits before the microprocessor reads the data.

The rate at which data is transmitted and received is set by an external clock signal.In same UARTs an external crystal can be connected directly to the device.

6.7 INTERNAL BLOCK DIAGRAM OF A UART.

The registers associated with transmission of serial data are the transmit shift register and transmit data register.The recieve shift register and the receive data register are the registers associated with receiving serial data.The microprocessor sends characters to be transmitted only to the trasmit data register and receives characters only from the receive shift register.A UART's internal circuitry automatically transfers the next character to be sent from the transmit data to the transmit shift register whenever the shift register is empty.Similarly,on the receiving side ,a UART automatically transfers received characters from the shift register to the data register when the data register is empty.

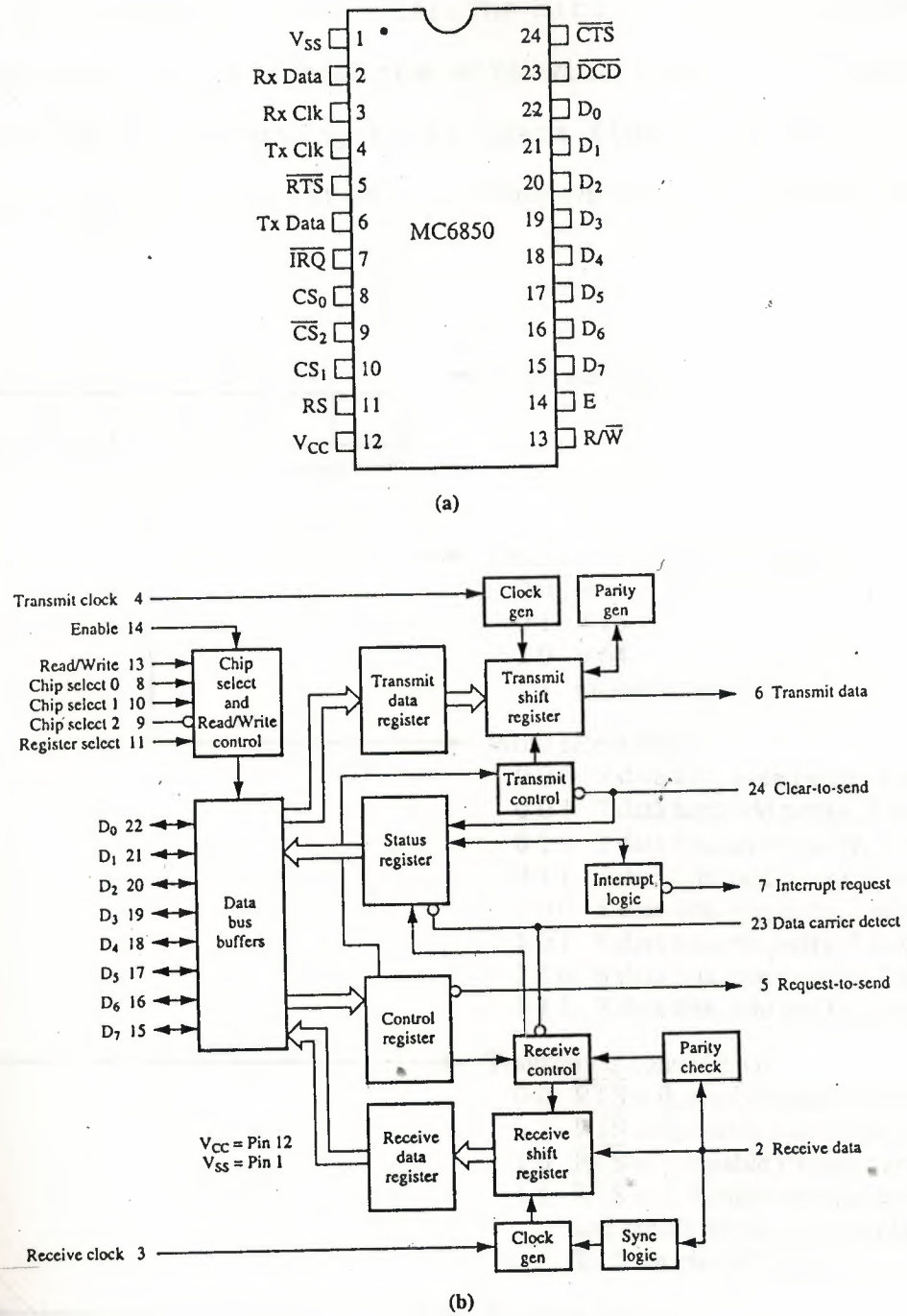


Figure 7.1 The MC6850 ACIA Pin Assignments in (a) and Internal Block Diagram as given in (b)

6.9 ACIA's CONTROL REGISTER.

Like other UART devices,Motorola's ACIA's control register is an 8- bit write only register.The binary pattern written into this register programs how the ACIA will operate for both transmitting and receiving serial data figure 7.2 shows how the bits of the control register are grouped and the function of each group.

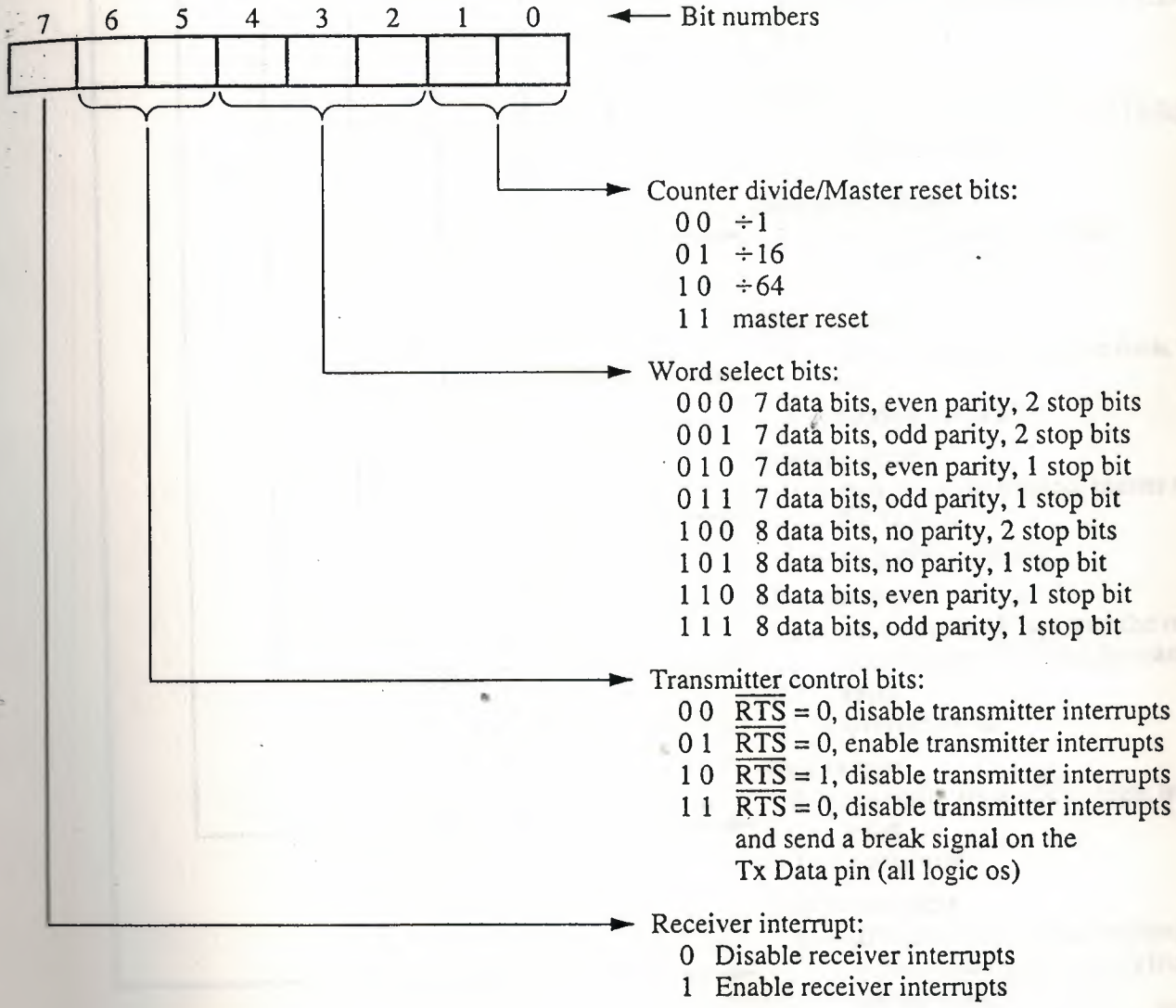


Figure 7.2 The Format for the MC6850 Control Register.

6.A ACIA's STATUS REGISTER.

The status register is a "record keeper" of conditions that have occured at the UART.As shown in Figure 7.3,the status register for an ACIA is an 8-bit read only register.Each bit of the register indicates the status of a different function.

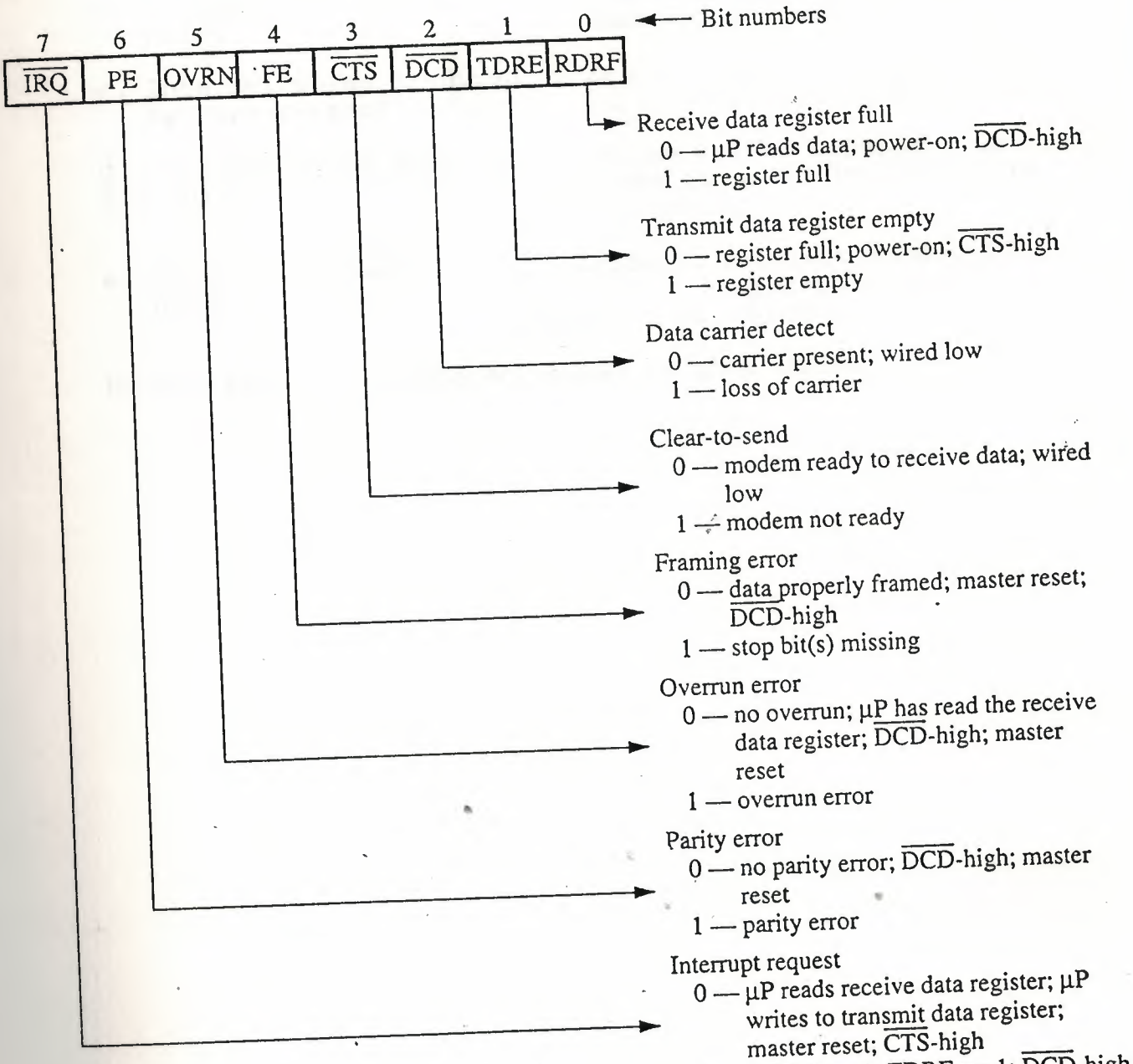


Figure 7.3 Format for the MC6850 ACIA's Status Register.

7.B NOISE

Table 6.2 Noise sources "controbuting" this project.

NOISE	PRODUCED BY
a. Noise in signal (quantum noise)	Statical fluctuation of signal power
b. Background radiation noise	Statistical fluctuations of background radiation.
c. Internal noise produced by dark current	Statistical fluctuations of internally generated current
d. Internal noise such as 1/f noise	Noise values dependent on devices owing to imperfections of detector.
e. Thermal (Johnson) noise	Noise in receiver produced by noise temperature of r-f portion of receiver.

Noises a,b,c are different types of shot noise.

SOFTWARE
7.

7.SOFTWARE.

7.1 SEND AND WAIT PROCEDURE.

Stop-and-wait has been used primarily for half duplex operations.After transmitting a frame the transmitter waits for a reply before sending another frame.

7.2 CORRECTION BY RETRANSMISSION.

Error correction by coding does not generally reduce the error rate sufficient to satisfy the requirments of data processing equipment.Also,these codes have a correction capability which is always less than their detection capability.Because of this,most transmission systems must use a more effective means of correcting errors than those which are based on correcting codes.It should be capable of use either alone or in conjuction with an error correcting code.As it is possible to design codes which provide an excellent probability of error detection,the most frequently used method of correction in data transmission consists of coding the data and performing error detection at the destination station.The latter returns a short positive acknowledgement (ACK) to the transmitting station if it does not detect any error in the message and a negative acknowledgement (NAK) if it does.Figure 7.1 depicts the scenario. When a trasmitting station receives a positive acknowlegement,it can continue with the transmission of the following message.Otherwise if it receives a negative acknowlegement,it deduces that the massage that it has just sent has beeb subject to errors and it repeats the transmission.

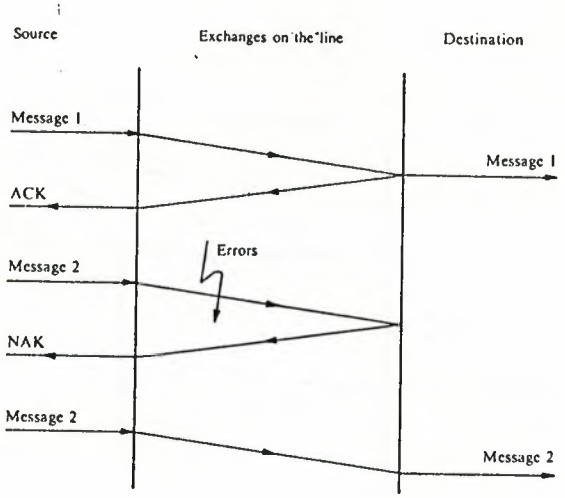


Figure 7.1 Error correction by retransmission

The system of correction by retransmission is simple in princeple but its realization poses problems;in particular it is necessary to avoid duplication of messages when the acknowledgement messages themselves suffer errors or are lost.

7.2 DETECTION OF LOST MESSAGES.

In some cases,disturbances in the transmission channel are such that the message is never received at the destionation,either because of a catastrophic breakdown of equipment or simply because the noise temporarily reaches to a level such that the receiver is incapable of recognizing the beginning of the message.In this case, the receiver cannot detect a transmission fault since it does not know that the message has been sent.In order to recover from this kind of situations,timers are used.The timer is set to a guard time t1 slightly greater than the transfer time of the message and corresponding acknowledgement.

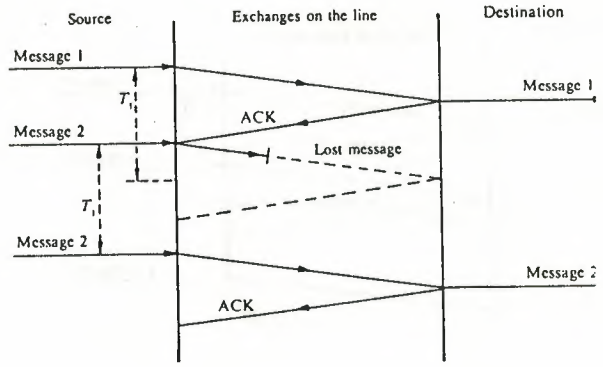


Figure 7.2 The use of timers in the protocol

If the transmitter has not received an acknowledgement after time T1, it deduces that the message or the acknowledgement has been lost and it repeats transmission of the same message.Figure 7.2 depicts detection of lost message by time up method.

The most serious question which occures with timers concerns the interpretation which must be given to non-reception of the acknowledgement with the window time T1 defined by the timer.If it is the ACK which has been lost,the receiver wrongly deduces that the message has been lost and retransmits it which causes a duplication of this message.It is therefore necessary to take precautions against the risk of duplication which can be achieved by a system of numbering of messages (0 or 1).

7.3 OPTIMUM MESSAGE LENGTH.

In practice, messages are divided into a useful part consisting of M bits of text and a supervisory part which contains R bits.The R supervisory bits serve bits serve to

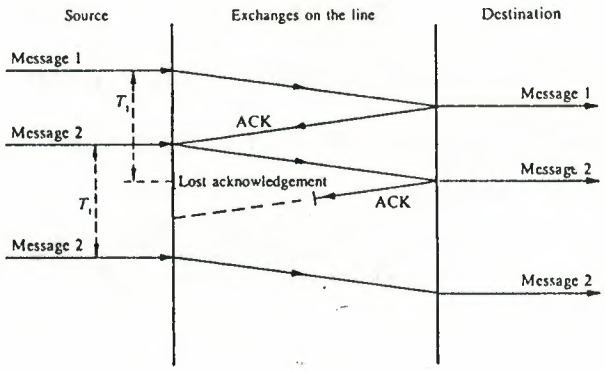


Figure 7.3 Duplication of messages produced by the loss of an acknowlegment.

delimit the message,monitor errors and also to specify the nature of the message,its origin and its destionation.Hence the message contains N=M+R.If transmission errors occur,the probability Pm that a message error is give by

(7.1)

in the case where bit errors are independent and the bit error probability Pb is very small.When a message is in error,with a probability Pm,it is retransmitted again with an error probability Pm and so on until it is retransmitted without error with a probability of 1-Pm.If all the errors are detected,the mean delay Tr between two succesive successfully transmitted messages becomes:

(7.2)

$$\bar{T}_R = \sum_{i=1}^{\infty} i T_R (1 - P_M) P_M^{i-1}$$

with little math,it takes the form;

$$\bar{T}_R = \frac{T_R}{1-p_M} = \frac{T_R}{(1-p_B)^n} \qquad (7.3)$$

The effective data rate D,expressed in bits per second, corresponds to the transmission of M bits by the message.Hence;

$$D = \frac{m}{T_R} = \frac{m(1-p_B)^n}{T_R} = \frac{mC(1-p_B)^{m+r}}{m+r+n_1+CT_P} \qquad (7.4)$$

The optimum length of messages,which corresponds to the maximum rate can be obtained by finding the value of M which makes dD/dM equal to zero,hence;

$$\frac{\partial D}{\partial m} = \frac{C(1-p_B)^{m+r}}{(m+r+n_1+CT_P)^2}[m(m+r+n_1+CT_P)\mathrm{Ln}(1-p_B)+(r+n_1+CT_P)] \qquad (7.5)$$

By putting a=r+n1+CTp

$$\frac{\partial D}{\partial m} = \frac{C(1-p_B)^{m+r}}{(m+a)^2}[m(m+a)\mathrm{Ln}(1-p_B)+a] \qquad (7.6)$$

The derivation is zero for

$$m = \frac{1}{2}\left[-a+\sqrt{a^2-\frac{4a}{\mathrm{Ln}(1-p_B)}}\right] \qquad (7.7)$$

which enables the maximum useful rate for a given error probability to be determined by substitution of 7.7 into 7.4

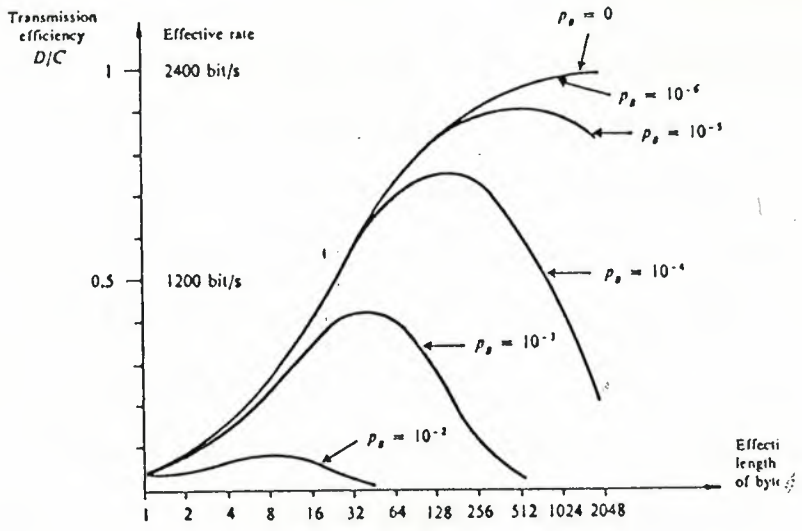


Figure 7.4 transmission efficiency versus bit error probability for send and wait procedure.

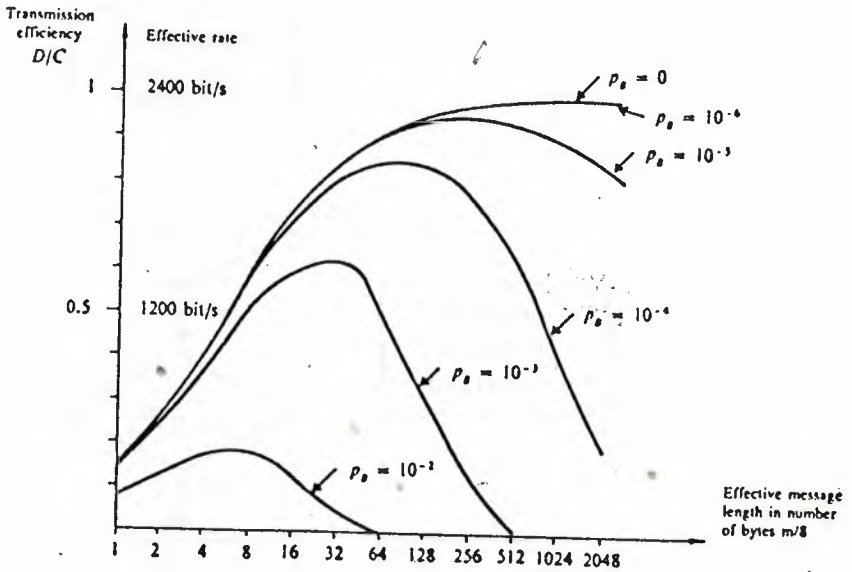


Figure 7.5 Transmission efficiency as a function of bit error probability for send and wait precedure.

7.5 TRANSMIT ROUTINE.

Figure 7.7 shows a flow chart enables microprocessor of IBM PC to determine if the transmit data register is empty so that another character may be sent to it.As seen from figure 7.7, the microprocessor reads the status register to check the TDRE bit.If this bit is logic one,the microprocessor will move the next character from memory buffer location to the transmit data register.If the TDRE bit is a logic 0,CTS bit must be checked to be sure the ACIA has not received a signal from a modem indicating no further transmission at this time.

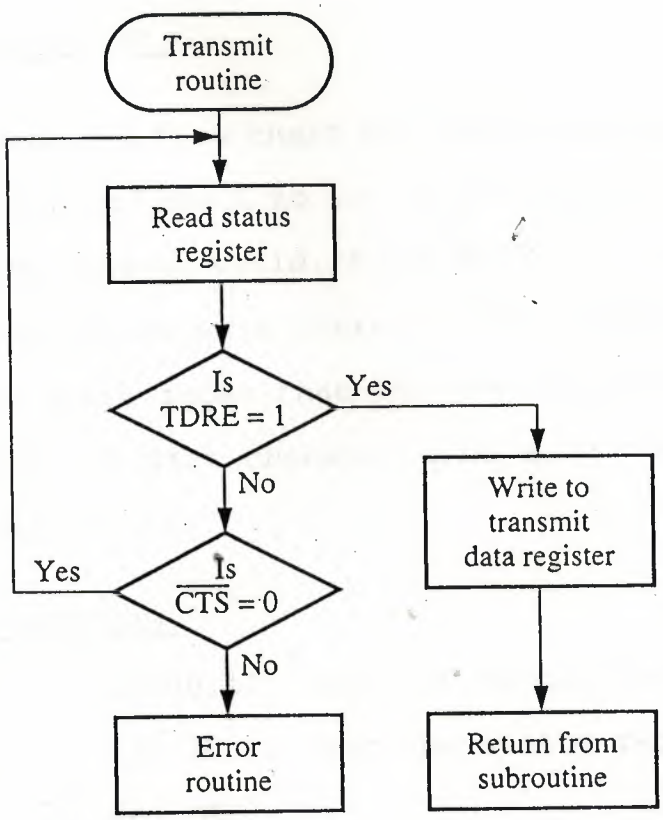


Figure 7.7 Flowchart illustrating the steps involved for the microprocessor to write a character to the ACIA's transmit data register.

7.6 THE TRANSMISSION PROGRAM.

```
        LEA       $2000,A1        load memory buffer address
READST: MOVE.B    $10040,D0       read the status register
        LSR       #02,D0          shift TDRE bit into C flag.
        BCS       TXDATA          test the TDRE bit;if C=1
                                  branch to TXDATA.
        LSR       #02,D0          Shift CTS bit into C flag
        BCC       READST          test CTS bit;if C=0,
                                  branch to READST.
TXDATA: MOVE.B    (A1)+$10042     move the next character to
                                  ACIA.
        RTS                       return from the subroutine.
```

7.7 THE RECEIVE ROUTINE.

Figure 7.8 shows a flow chart for IBM PC microprocessor read the status register and check to out if the receive data register is full and if the data is valid.If the RDRF bit is a logic 0,the DCD bit is checked to be sure there has not been a loss of carrier.The flow chart shows that the framing error,overrun parity error bits are firt checked to be sure the receive data register holds valid data.

7.8 THE RECEIVE PROGRAM.

```
        LEA       $2500,A2  load the memory buffer address
READSR: MOVE.B    $10040,D0 read the status register.
        LSR       #01,D0
        BSC       FEBIT     if C=1,branch to check FE bit
        LSR       #02,D0    shift DCD bit into C flag
```

7.5 TRANSMIT ROUTINE.

Figure 7.7 shows a flow chart enables microprocessor of IBM PC to determine if the transmit data register is empty so that another character may be sent to it.As seen from figure 7.7, the microprocessor reads the status register to check the TDRE bit.If this bit is logic one,the microprocessor will move the next character from memory buffer location to the transmit data register.If the TDRE bit is a logic 0,CTS bit must be checked to be sure the ACIA has not received a signal from a modem indicating no further transmission at this time.

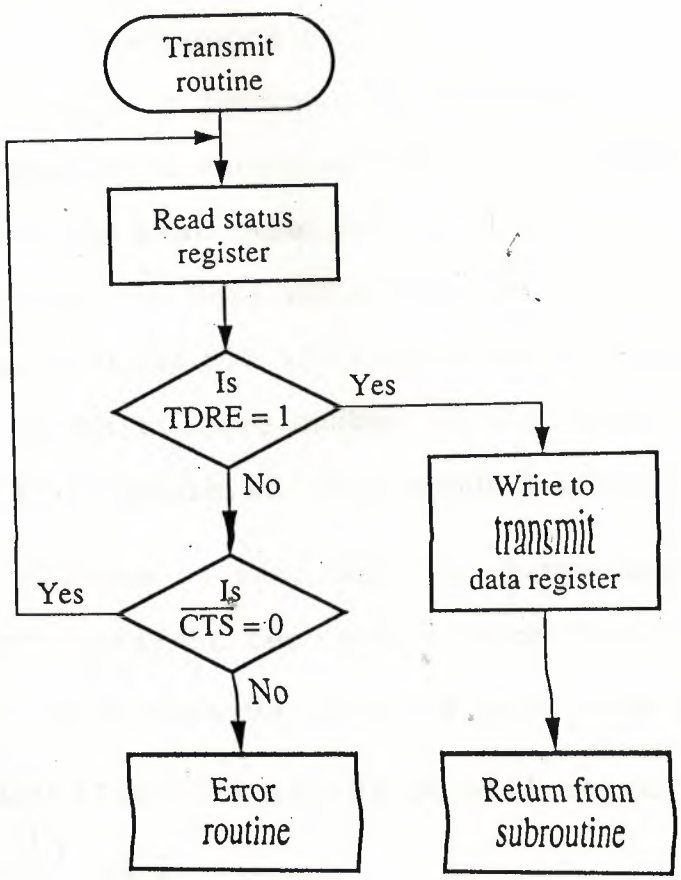


Figure 7.7 Flowchart illustrating the steps involved for the microprocessor to write a character to the ACIA's transmit data register.

7.9 ABOUT THE PASCAL PROGRAM.

To accomplish communication link 1 have developed the flow diagram in previos page.From now on 1 will refer it STOP-AND WAIT AUTOMATIC REPEAT REQUEST (ARQ) protocol.The protocol basically consists of having one station send a frame bearing a sequence number of 0 or 1 to the other station.This data frame will contain in addition to other information a packet of actual data.The transmitting end has an input buffer where this data frame and being transmitted over the data link.Even after transmission of the data that are in end 1's input buffer,those data are kept in the data frame containing that particular data packet has been received successfully.

The latter condition (successful reception of a data frame 0 or 1) is indicated by having the end 2 station send the frame sequence number of the last received valid frame back to the end 1 station as part of the next data frame being sent from 2 to 1.This is done by setting the ack number in this frame (the one going from 2 to 1) to the seq number of the last valid frame received from 1.For example,if end 1 sends a frame with seq=0 to end 2,it is not allowed to send out its frame seq=1(containing a new data packet) until it receives a frame from end 2 bearing an ack=0.If 1 doesn't receive this ack back from 2 within a certain specified timeout interval,it will retransmit the original frame to end 2

7.10 THE PASCAL PROGRAM.

```
type Event=(Valid Frame Arrives,error,Timeout);
```

```
prosedure Sample;
var event:Event
  s,r:Frame
  expseq:Sequence Number
  buffer:Massage
begin
  s.seq:=0
  expseq:=0
  s.ack:=1
  get from host(buffer);
  s.data:=buffer;
  repeat
     send Frame(s);
     reset and Start Timer;
     wait(event);
     if event=Valid Frame Arrives then
       begin
          get Frame(r);
          if r.seq=expseq then
            begin
               send to Host(r.data);
               s.ack:=expseq;
               increment(expseq);
            end
          if r.ack=s.seq then
           begin
          increment(s.seq);
          get from Host(buffer);
```

```
            s.data:=buffer;
        end;
      end;
    until Forever
  end;Sample
```

7.11 PETRI-NET DIAGRAM.

In this diagram the individual stations and the line are each assigned to different areas of the diagram,and each circle shows only the state of one of the three entities (end 1,end 2,or the other line).The state of the entire state is than denoted by placing a TOKEN in one of the circles in each of the three diagram areas.The transition between states are shown by heavy bars.A given transition is allowed to occur whenever all the circles connected to the input side of a bar possess a token.After the transition takes place the new state is indicated by placing a token in all the circles which are connected to the output side of the bar.Normally some of the tokens do not move during most of the state transition which takes place.the number of inputs to a bar does not have to be equal to the number of outputs.

7.12 THE EFFICIENCY OF PROTOCOL.

To discuss different efficiencies more easily,I will first define some algebraic representations:

D = the number of actual data bits in a frame

H = the number of "overhead" bits in the frame

F = D+H = the total number of bits in the frame

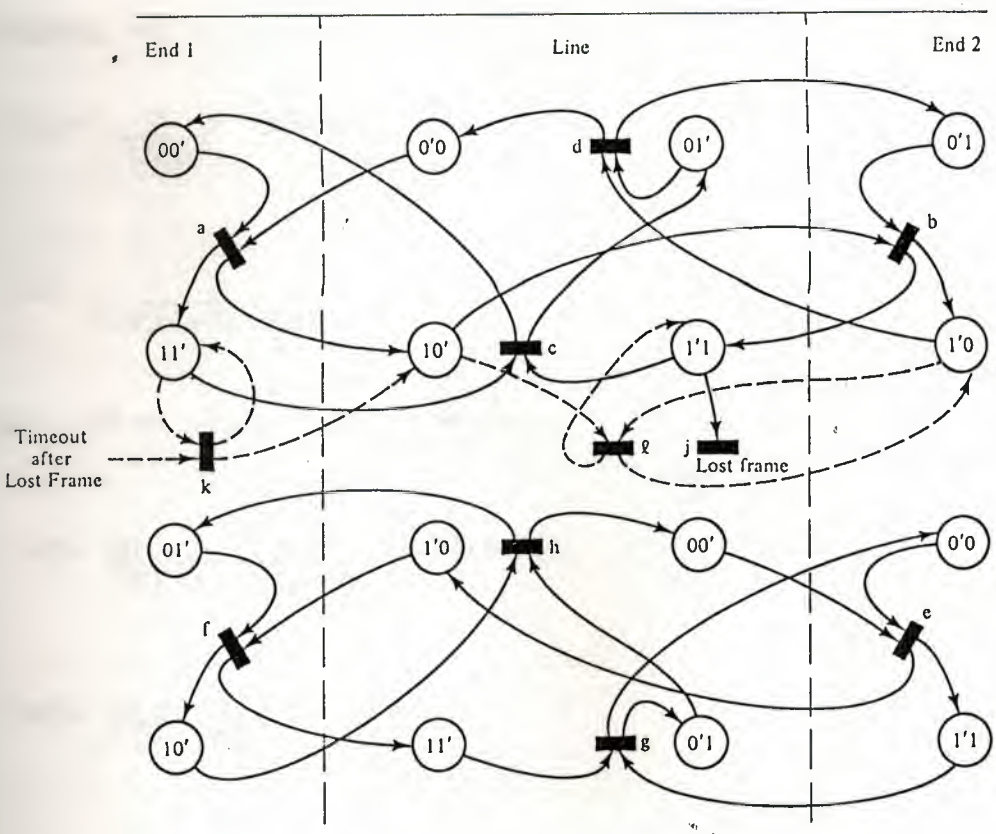


Figure 7.11 The petri-net diagram of the protocol

C = the channel transmission capacity in bits per second

Tav = the average time needed to get a undamaged frame through the link

Tf = the time required to transmit the data frame

Tp = the one way transmission propagation time

Tx = the turnround time at one station

Tc = time required to transmit a control frame

BER = the bit error rate.

PDF = the probability of a frame being damaged

Nch = the channel efficiency in percent

Ntr = the transmission efficiency in percent

Npr = the "protocol" efficiency

By using these symbols, what is normally termed as channel efficiency is ;

$$Nch = \left(\frac{D}{CTav}\right)(100)\% \qquad 7.8$$

Or

$$Nch = \frac{D}{C(F/C+Tp+Tx)}(100)\% \qquad 7.9$$

Or quit often this is written as;

$$Nch = \left(\frac{D}{F}\right)\left(\frac{F}{F+C(Tp+Tx)}\right)(100)\% \qquad 7.10$$

$$Nch = \left(\frac{Ntr}{100}\right)\left(\frac{Npr}{100}\right)(100)\% \qquad 7.11$$

The time required to transmit a frame and get it acknowledge would be;

$$Tav = \left(\frac{F}{C}\right)+(2Tp)+(2Tx)+TOS+Tc \qquad 7.12$$

where TOS is the waiting time before transmitting the ACK control frame from the receiving end. Thus,

$$Npr = \frac{F}{F+C(2Tp+2Tx+TOS+Tc)}(100)\% \qquad 7.13$$

the probability of a data frame being damaged during transmission is;

$$PDF = \sum_{k=1}^{F}\left(\frac{F!}{k!(F-k)!}\right)BER^{k}(1-BER)^{F-k} \qquad 7.14$$

$$\doteq F \times BER \text{ when BER is small}$$

The probability that the frame will not be damaged is ;

$$1-PDF=(1-F\ BER) \qquad 7.15$$

The avarage number of tries to get a valid frame through the data link is then given by;

$$= \sum_{k=1}^{\infty} k(PDF)^{k-1}(1 - PDF) \qquad 7.16$$

$$= \frac{1}{1 - PDF}$$

The time needed to transmit frames which get damaged and then wait until timeout occurs before trying again is equal to (F/C) plus TOR.The time requred to transmit an undamaged frame and get a reply back is equal to (F/C) + Tp + Tx .Thus,

$$Tav=(kav-1)(F/C + TOR) + (F/C + Tp + Tx) \qquad 7.17$$

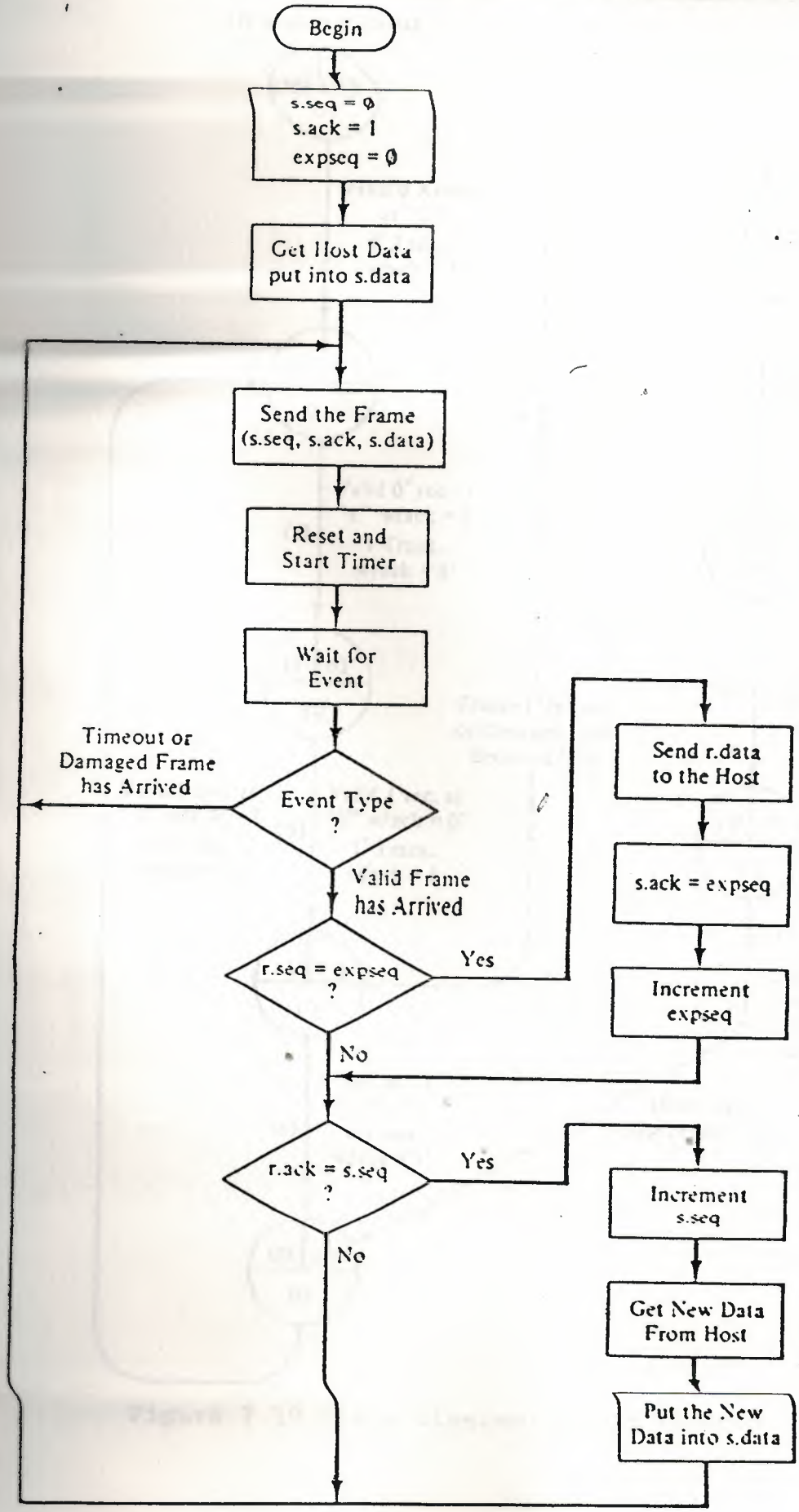
Combining this with the expression for kav we get

$$Tav=\frac{(F/C) + (PDF)(TOR) + (1 - PDF)(Tp+Tx)}{1-PDF} \qquad 7.18$$

which gives;

$$Npr=\frac{F(1-PDF)(100)\%}{C((F/C) + (PDF)(TOR) + (1-PDF)(Tp + Tx))} \qquad 7.19$$

$$=\frac{F(1-PDF)(100)\%}{F + C((PDF)(TOR) + (1-PDF)(Tp + Tx))} \qquad 7.20$$


Begin
s.seq = 0
s.ack = 1
expseq = 0
Get Host Data
put into s.data
Send the Frame
(s.seq, s.ack, s.data)
Reset and
Start Timer
Wait for
Event
Timeout or
Damaged Frame
has Arrived
Event Type
?
Valid Frame
has Arrived
r.seq = expseq
?
Yes
Send r.data
to the Host
s.ack = expseq
Increment
expseq
No
r.ack = s.seq
?
Yes
Increment
s.seq
Get New Data
From Host
Put the New
Data into s.data
No

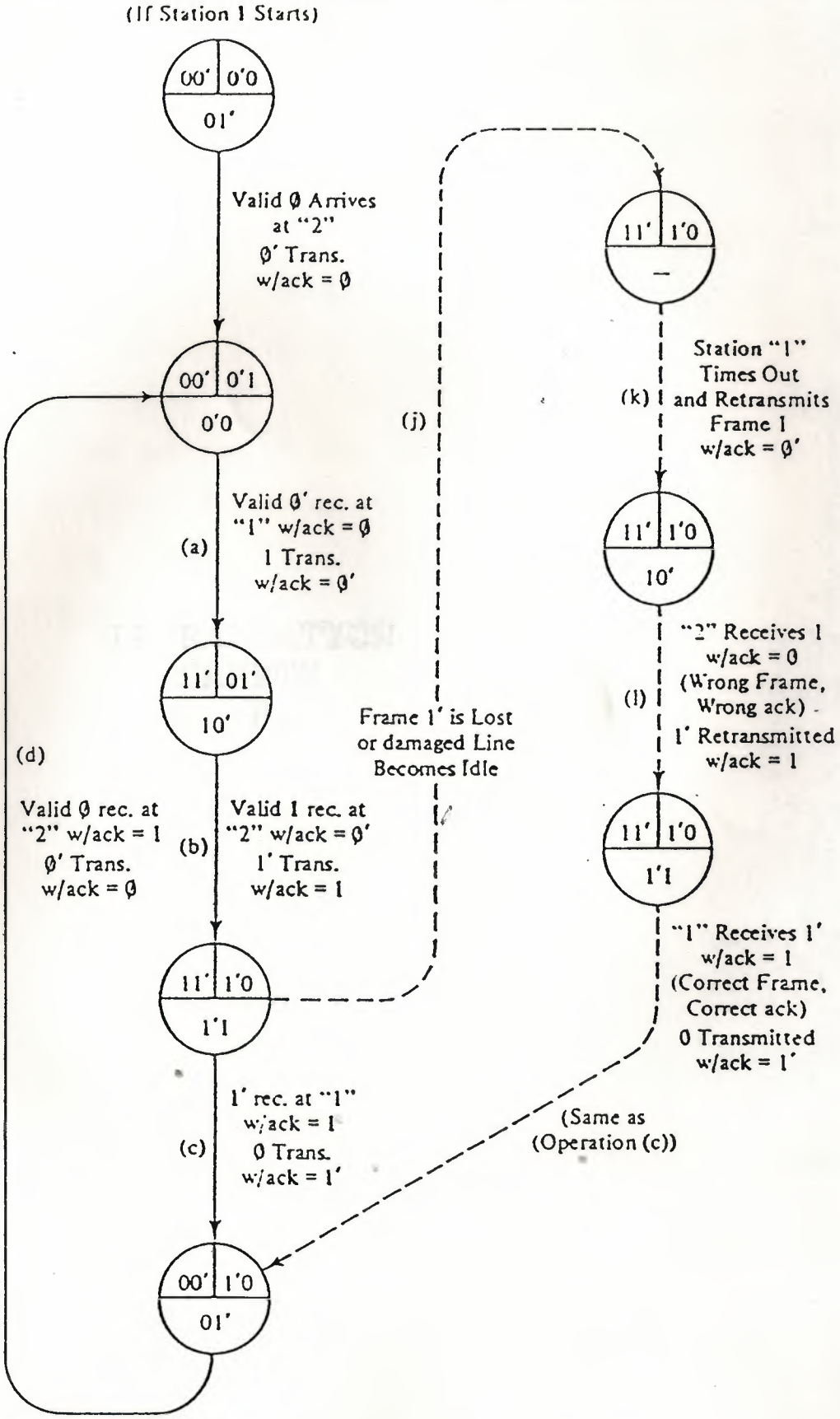


Figure 7.10 State Diagram of the Protocol.

IR RADIATION SAFETY

8.

8. IR RADIATION SAFETY.

Most practical IR emitters emit radiation that is potentially hazardous.The degree of the hazard is related to the output characteristics of the IR,the way in which it is used and the experience of the operator.

The primary event causing damage is the absorption of the radiation by the biological tissues.

In general terms,skin can tolorate a great deal more exposure than can the eye.The hazards are wavelength dependent,being more pronounced for ultraviolent radiation.

In the case of posibility of risk AMERICAN STANDARDS FOR THE SAFE USE OF LASERS # Z136 should be consulted.