GENERALIZED MULTICELL SWITCHED INDUCTOR AND SWITCHED-CAPACITOR Z-SOURCE INVERTERS

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

By FATMA MUFTAH SLLAMI

In Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name: Fatma Muftah Sllami Signature: Date:

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ABSTRACT

Power conditioning units such as inverters are required for a variety of application in both industrial and non-industrial applications. In industrial application of inverters, areas such as flexible AC power transmission systems or distributed power systems, charging of electric vehicles, control of ac motors with variable functionality, distinctive power producers. The most common type of industrial based inverter with high applications is the voltage or current source inverters also known as VSI or CSI. Although VSI and CSI has provided relief when it comes to power conditioning, they are bedeviled with numerous drawbacks such as output buck functionality, susceptibility to effects of EMIs due to lack of shoot through protection, increased losses when boost functionality are desired at the output. The above problems are solved by the introductions of the impedance source inverter (ZSI). The generalized impedance source inverter topologies (SL and SC) have been introduced to increase the voltage and current gains of the conventional impedance topologies. Simulation results are produced using PSCAD software to validate the boosting functions of the generalized topologies. Comparative analysis of generalized SL and three other inverter topologies (TL, Trans ZSI and Cascaded) is investigated.

Keywords: Voltage source inverter; current source inverter; switched inductor; switched capacitor; tapped inductor; trans ZSI and cascaded.

ÖZET

Inverterler gibi güç düzenleyici üniteler, hem sanayisel hem sanayi dışı uygulamalarda gereklidir. Inverterlerin endüstriyel uygulamaları, AC güç iletimi sistemleri veya dağıtılmış güç sistemleri, şarj edilen elektrikli arabalar, çeşitli işlevsellikle alternatif akım motorlarının kontrolü, ayırt edici güç üreticilerini içermektedir. En yaygın sanayisel alan inverterları, VSI veya CSI olarak bilinen voltaj veya akım kaynağı inverterlarıdır. VSI ve CSI'lerin çok rahatlama sağlamasına rağmen, sıra güç düzenlemeye gelince, çıkış (output) buck işlevselliği, koruma sırasında fışkın azlığı kaynaklı EMI etkilerine duyarlılık, itiş işlemi verimde istendiğinde artan hasarlar gibi birçok sorun çıkarıyorlar. Yukarıdaki sorunlar direnç kaynağı inverteri tanıtımı tarafından giderilmiştir (ZSI). Genelleştirilmiş direnç kaynağı inverter topolojileri (SL ve SC), klasik direnç topolojilerinin voltaj ve akım kazançlarını arttırmak için uygulamaya konmuştur. Simulasyon sonuçları, genelleştirilmiş topolojilerin itme işleminin geçerliliğini denetleme amacıyla PSCAD yazılımı kullanılarak elde edilmiştir. Genelleştirilmiş SL ve diğer üç inverter topolojilerinin (TL, Trans ZSI ve Kaskat) karşılaştırmalı analizi incelenmiştir.

Anahtar kelimeler: Gerilim kaynağı inverteri; akım kaynağı inverteri; kurmalı indüktör; kurmalı kapasitör; dişli indüktör; trans ZSI ve Kaskat.

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LIST OF ABBREVIATIONS

DC	Direct Current
AC	Alternating Current
VSI	Voltage Source Inverter
CSI	Current Source Inverter
ZSI	Impedance Source Network
BZSI	Bidirectional Impedance Source Network
IZSI	Improved Z Source Inverter
PV	Photovoltaic Systems
HPZSI	High Performance Impedance Source Network
EMI	Electromagnetic Interference
FLZSI	Four Leg Z Source Inverter
DuZSI	Dual Z Source Inverter
NPZSI	Neutral Point Z Source Inverter
ZSID	Z Source Inverter Diode
ZSIS	Z Source Inverter Switch
QZSI	Quasi-Z-Source Inverter
SLQZSI	Switched Inductor Quasi-Z-Source Inverter
DGC	Doubly Grounded Circuits
HFTI	High Frequency Transformer Isolation
PWM	Pulse Width Modulation
СВ	Circuit Breakers
UC	Ultra-Capacitor
CFSI	Current Fed Switched Inverter
KVL	Kirchhoff Voltage Low
RL	Resistive-Inductive

CHAPTER 1 INTRODUCTION

1.1 Overview

The importance of power inversion using inverter devices is becoming an integral part of power systems such as distributed generations, flexible ac transmissions, adjustable industrial drives, power conditioners and integration of renewable energy into grid systems. The function of dc-ac inverter is not only to change dc voltage into ac voltage but also perform necessary power conditioning to give suitable voltage and frequency with good quality waveforms devoid of harmonic contents. Basically the topology of the inverter determines the magnitude of the output to a corresponding frequency. The conventional voltage source inverter also known as voltage fed inverter and the current source inverter or current fed inverter are the bedrocks for the development of dc-ac inverter. They are very useful in industrial and non-commercial applications but they are composed of a number of drawbacks which has led to the development of other inverter topologies such Z source inverters.

The disadvantages of voltage source inverter (VSI) which hinders it efficient applications in power systems are; VSI operates as a buck converter; the generated output voltage is smaller than the input voltage hence the voltage transfer ratio is limited, short circuit faults will cause damage to inverter components such diodes and switches; immunity to noises generated by electromagnetic interferences are not possible. However, the size of VSI is small and compact, the output voltage waveform is independent of the type of load. The current source inverter (CSI) on the hand has the following drawbacks; functions as a boost inverter, when applied to light loads the CSI performance is unsteady, in other to step-up or step-down the input or output voltage more converters are required. However some advantages of CSI are; for commutation purposes the use of thyristor is uncomplicated. Both VSI and CSI have increased cost when high boosting functionality is required, efficiency is reduced by the introduction of buck-boost converters, size and weight also increases hence will not be suitable for applications where these factors are of great importance.

The introduction of Z source inverter has solved most of the limitations of VSI and CSI but has also introduced a couple of limitations which are being overcome by continuous research and further development of the conventional impedance source network (ZSI). ZSI is composed of symmetrical passive components connected in the shape of the letter X. Two capacitors and two inductors constitute the passive components which connected together forms the impedance network. One of the main advantages of the conventional ZSI is the buck-boost functionality which makes it possible to have infinity magnitude of output voltage; theoretically this is idea is possible but not practically hence other topologies of ZSI have been introduced to provide higher boosting options and to reduce the defects of the conventional ZSI.

1.2 Thesis Problem

The past decade has seen rapid development of the conventional Z source inverter in the areas of application, control, modulation, component type and size, circuit modeling and boosting capabilities. The gains or boosting capabilities of conventional ZSI is infinite theoretically only, in practical applications, factors like minimized spectral conduct and high component stress limits the voltage gain capabilities.

Trade-off in the duty ratios of modulation and shoot through state are partial causes of voltage gain limitations of the conventional ZSI. To improve these gains several topologies of ZS have been proposed, some examples are switches inductor and switched capacitors topologies, Trans Z source topologies, quasi Z source topologies, and tapped inductor topologies.

Although all these topologies have high boosting capabilities, their advantages can be traced to the disadvantages of the previous topologies they tried to enhance. Some researchers seek to have reduced components with average boosting factors; some seek higher boosting factors regardless of the component count.

1.3 The aim of Thesis

The aim of this thesis to simulate switched inductor and switched capacitor based impedance source inverters in the *generalized* form. The generalized switched inductor topology will increase the boosting factor which is a limitation of the switched inductor topology. Also the boosting factor of the generalized switched capacitor will presented using current source impedance network inverter. Comparison between the generalized and not-generalized topologies will be presented based on simulation results.

1.4 The Importance of Thesis

The importance of power inversion using inverter devices is becoming an integral part of power systems such as distributed generations, flexible ac transmissions, adjustable industrial drives, power conditioners and integration of renewable energy into grid systems. Basically power conversion devices have become integral part of human society and responsible for the efficient and smooth running of the following of sectors of human society; aviation, telecommunication, education, transportation and power generation stations.

Generalized switched inductor and switched capacitor topologies will increase the boosting factor of any inverter topology that it's applied to; this will maximize the inverter output power resulting in the efficient application of power source such renewable energy.

1.5 Limitation of Study

This research was carried out with extreme caution taking into consideration all necessary precautions for both theoretical and simulation of projects as required of a graduate student but definitely some drawbacks or limitations will be encountered. The absence of well-equipped laboratory prevents us from producing experimental results; also the simulation results are limited to the mathematical modeling used for the software design.

1.6 Overview of the Thesis

The structure of this thesis is as follows:

Chapter 1: Introduction. This chapter is made of introduction, Thesis Problem, The aim of Thesis, The important of Thesis and overview of the thesis.

Chapter 2: Literature Review of Z Source Inverters

Chapter 3: Proposed Topology and Simulation Results

Chapter 4: Conclusion and Future Works

CHAPTER 2 Z SOURCE INVERTERS

2.1 Introduction

The impedance network or Z-source converters have recently caught the attention of researchers and power electronic industry players because of its enough advantages over other converters. As such the aim of my research is review academic papers on Z source inverters or converters over the last two decades; this will be achieved by the selection of 50 journal and conference papers, reviewing the various topologies, applications and control methods. This will enable me to fully understand the extent of usage of the Z source inverter (ZSI).

2.2 Z Source Inverter

The ZSI which was proposed in 2003 by (Peng, F. Z. 2003) is a power electronic converter which is mostly applied in dc – ac power conversion; it has exciting characteristics such as single stage power inversion and the buck-boost properties. The ZSI is composed of four passive components of two capacitors and two inductors designed in X structure which constitutes the impedance structure or source. The impedance structure is placed in-between the source and the main converter body hence forming the impedance source inverter. Figure 1 shows the basic ZSI topology which uses the shoot through state to increase the voltage gain or increase the magnitude of the source voltage; this advantage of the ZSI over other power electronic converters increases its scope of operation and reliability, produces single stage of power conversion (dc-ac), it has reduced cost, provides high efficiency, its size or volume is also reduced and has least component count. The application of ZSI in emerging energy sources such wind farms, photovoltaic systems, mini hydropower system and other current power electronic conversion systems such as hybrid and electric cars is propitious (Peng, F. Z. 2003)



Figure 2.1: Basic ZSI structure (Peng, F. Z. 2003).

The applications of ZSI is not limited to only dc-ac conversion but can also be applied to the following types of conversion; ac-dc, dc-dc, and ac-ac. Also the impedance network of ZSI can be placed in any converter topology where the source is either VSI or CSI where the output of the converter has multilevel waveform functionality. There are several limitations of the conventional voltage source converter or current source converters such as; application of extra converter for buck-boost functions thereby increasing the cost of the system, volume of the system also increases considerably, efficiency is adversely affected because double stage conversion increases system losses. Turning on all switches on the same phase or leg will lead to short circuit or a condition called shoot-through which leads to destruction of the converter. The conventional VSI or CSI have poor immunity to electromagnetic interference (EMI) which is one of the major causes of unintentional gating of switches. Several topologies have been developed after the basic ZSI of Figure 2.1 was presented in 2003 because of a number of drawbacks of the basic ZSI structure; there was very large inrush current during beginning of converter operation, the power flow was unidirectional due to the diode, suitable for semi heavy-load applications, the source current flow is discontinuous, higher capacitor voltage in impedance network, secluded source and inverter dc rail (Ellabban, O., & Abu-Rub, H. 2016).

2.3 Z Source Topologies

To solve the drawbacks of the basic ZSI structure, the following topology were designed; the bidirectional ZSI topology was designed by replacing the diode with bidirectional switch, BZSI structure is suitable for photovoltaic systems since PV panels cannot store energy. The switch operates throughout the regenerative phase just as the diode will in the inverter phase. The BZSI topology allows bidirectional power flow or exchange between the source (dc) and the load (ac).

The advantages of the BZSI over ZSI negate the cost of the switch (Shen, M., & Peng, F. Z. 2008). The HPZSI (high performance ZSI) (Ding, X., et al. 2007; Ellabban, O.et al. 2009) was designed for wide range of load applications; the inductor in the impedance structure of this topology is much smaller than ZSI hence voltage drop of the dc link is eliminated, the impedance structure is simplified both in design and control methodology, the addition of bidirectional switch and a capacitor to ZSI yields HPZSI (Shen, M., & Peng, F. Z. 2008). The IZSI; improved Z source inverter has the merits of ZSI plus eliminating inrush current and reducing voltage stress on the capacitors. IZSI if acquired from ZSI by changing the position of the diode and the H-bridge and also reversing the connection of the impedance network and the H-bridge (Tang, Y., et al. 2009; Yu, K., et al. 2010). Figure 2.3 shows various topologies of the improved ZSI structure such IZSI, QRSSZSI, SZSI and HPIZSI.



Figure 2.2: ZSI topologies a) ZSI b) Bidirectional ZSI (c) High performance ZSI (Peng, F. Z. 2003; Shen, M., & Peng, F. Z. 2008; Ding. X., et al. 2007).



Figure 2.3: Various improved Z source topologies (Tang, Y., et al. 2009; Yu, K., et al. 2010). Another topology called the four-wire ZSI or ZWZSI has numerous literatures, (Khlebnikov, A. S., & Kharitonov, S. A. 2008) presented a FWZSI system which was an improvement of the HPZSI topology; two bidirectional switches and two capacitors are used, the neutral point is between two capacitors and the other bidirectional switch is placed in the negative current path. A different procedure to obtain the four leg structure in (dos Santos, E. C., Muniz, J. H. G., & Da Silva, E. R. C, 2010) is by adding extra phase or leg to obtain four leg Z source inverter; FLZSI. The DuZSI known as the dual Z source inverter is obtained by adding another H-bridge to the FWZSI, its advantage includes the quality of the output voltage is greatly improved the current stress on the components is reduced but its drawback is an increase in the number of switches (Khlebnikov, A. S., Kharitonov et a , 2011) hence increased losses. The last type of topology is the neutral point Z source inverter NPZSI (Bachurin, P. A., Makarov, 2013) where the passive components are increased and a neutral point introduced in the impedance network. The various four wire topologies enumerated above is shown in Figure 2.4.



Figure 2.4: The neutral point Z source topologies (Bachurin, P. A., Makarov, 2013).

To reduce or eliminate leakage current in the PV based three phase transformerless Z source inverter, a new topology called Z source inverter diode ZSID was presented in [Bradaschia, F, 2011; Erginer, V., & Sarul, M. H. 2013). The function of the second diode is to isolate the photovoltaic system's terminals from the H-bridge in the shoot through state hence preventing the flow of leakage current in the structure. Z source inverter switch –ZSIS provides the impetus of system stability for any scope of modulation index (Ferraz, P. E, 2011). Two topologies of quasi Z source inverter are presented in (Anderson, J., & Peng, F. Z. ,2008) with continuous and discontinuous current flow properties. These topologies have numerous benefits when compared to ZSI; common mode noise of the network is reduced due to dc source and the combined earthing of the source, the components of impedance network has lower ratings. The input diode can be changed with bidirectional switch to obtain the bidirectional quasi-Z source inverter (Guo, F et al, 2013). Figure 2.5. Show the QZSI topologies; (a) with non-continuous current input and (b) steady current flow.



Figure 2.5: Quasi Z source inverters (Anderson, J., & Peng, F. Z., 2008).

There are other topologies of ZSI which boost the voltage gain probability of the inverter and these types of topologies are referred to as extended improved topologies. The topologies are achieved by substituting the inductor or inductors in the basic QZSI or ZSI with switched inductor network to produce switched inductor quasi-Z source inverter or switched inductor Z source inverter. This method can be applied to other improved ZSI topologies. The advantage of adding the switched inductor network is a sharp increase in the boosting ability which produces solidity of structure, increased power density, better relationship between modulation index and voltage gain. The switched inductor Z source inverter together with switched inductor improved Z source inverter is shown in Figure 2.6.



Figure 2.6: Switched inductor Z source inverter topologies (Guo, F et al, 2013).

Combination of the switched inductor circuit together with quasi Z source inverter yield the switched inductor quasi-Z-source inverter - SLQZSI topology as shown in Figure 2.7. The switched inductor circuit can be combined with switched capacitor to produce switched-capacitor-inductor circuit as shown in Fig. 7c. Also an active switched can be incorporated in the design to produce active switched capacitor as in Figure 2.7d.(Ismeil, M., Orabi et al, 2014; Nguyen, M. K et al, 2011). The advantages of the above topologies the better efficiency it produces and far better boosting capabilities (Deng, K. et al, 2014; Li, L., & Tang, Y, 2014).



Figure 2.7: SLQZSI Topologies. (Ismeil, M., Orabi e al, 2014).

Other QZSI topologies combining the switched inductor or capacitor technology with other inverter properties creates the inverters in Figure 2.8. Where a) input current is rippled, b) has a steady source current and c) combines the extended topology with switched inductor topology.



Figure 2.8: Switched inductor topologies (Deng, K. et al, 2014).

Table I shows a comparison of the various topologies presented above based on the number of components in impedance network, whether it has steady source current flow, inrush current during startup, whether it has joint earthing and the boost factor equation.

Topologies	ZSI	SLZSI	SLIZSI	SLQZSI	ISLQZSI
Components count	2-L 2-C 1-D	4-L 2-C 7-D	4-L 2-C 7-D	3-L 2-C 4-D	3-L 3-C 3-D
Steady input current	No	No	No	Yes	Yes
Inrush Current	Yes	Yes	No	No	No
Joint Earthing	No	No	No	Yes	Yes
Boost Factor	$\begin{array}{c} (1/1 - 2 \ D0) \\ 0 \leq D0 \geq 0.5 \end{array}$	(1+Do/1 - 3D0) $0 \le D0 \ge 1/3$	(1+Do/1 - 3D0) $0 \le D0 \ge 1/3$	(1+Do/1 - 2D0 - D02) $0 \le D0 \ge 1/3$	(2/1-3D0) $0 \le D0 \ge 1/3$
Topologies	SCLQZSI	ASC/SL-ZSI	RSLQZSI	CSLQZSI	ESLQZSI
Components count	1-L, 1-CL 3-C 3-D	2-L 1-C 5-D, 1-S	4-L 2-C 7-D	4-L 2-C 7-D	4-L 4-C 4-D, 1-S
Steady input current	Yes	Yes – rippled	Yes – rippled	Yes	Yes
Inrush Current	No	No	No	No	No
Joint Earthing	Yes	No	Yes	Yes	Yes
Boost Factor	$\begin{array}{c} (3/1-4 \ D0) \\ 0 \leq D0 \geq \frac{1}{4} \end{array}$	(1+D0/1 - 3D0) $0 \le D0 \ge 1/3$	(1+D0/1 - 3D0) $0 \le D0 \ge 1/3$	(1/1 - 3D0) $0 \le D0 \ge 1/3$	$ \begin{bmatrix} 2/(1-3D0)(1-D0)] \\ 0 < D0 > 1/3 \end{bmatrix} $

Table 2.1: Comparison of selected Z source inverter topologies

Note: 2-L means 2 inductors

1-D means 1 diode

3-C means three capacitors

2.4 ZSI Circuit Analysis

The basic Z source inverter structure as presented in Figure 3.1 comes with some drawbacks which results in the development of the various topologies presented above. Mathematical analysis of the basic ZSI produces the equations below. The corresponding circuit of the ZSI considered from the dc source input is shown in Figure 2.9.



Figure 2.9: ZSI equivalent circuit. (Shen, M., & Peng, F. Z. 2008).

The impedance circuit of the ZSI should become symmetrical for effective circuit analysis. The value of the two inductors L_1 and L_2 should be equal and the value of the two capacitors C_1 and C_2 should be the same i.e.:

$$\begin{cases} L_1 = L_2 = L \\ C_1 = C_2 = C \end{cases}$$
(2.1)

Two states of operations exist in the operation of the ZSI; the shoot-through state and non-shoot through. The two states are represented in Figure 2.10.in the shoot through phase, the period of conduction is T_0 for a switching period of T, during this period Kirchhoff's voltage and current analysis of Fig. 10a yields the equations below.

$$\begin{cases} V_L = V_C \\ V_d = 2V_C \\ V_i = 0 \end{cases}$$
(2.2)



Figure 2.10: Shoot-through phase (Yu.K et al 2010).

Again if the inverter is the non-shoot through phase for a period of T_1 for a switching period of T, Kirchhoff's voltage and current analysis of Figure 2.10a yields the equations below.

$$\begin{cases}
V_L = V_0 - V_C \\
V_d = V_0 \\
V_i = V_C - V_L = 2V_C - V_0
\end{cases}$$
(2.3)

The total period for a complete cycle is given by:

$$T = T_1 + T_o \tag{2.4}$$

The average inductor value over one switching cycle T is given (2.5) which equals to zero in steady state.

$$V_{L} = \overline{v_{L}} = \frac{T_{O} \cdot V_{C} + T_{1} \cdot (V_{O} - V_{C})}{T} = 0$$
(2.5)

The above equation can be written as

$$\frac{V_C}{V_O} = \frac{T_1}{T_1 - T_O}$$
(2.6)

The average dc voltage is given by:

$$V_{i} = \overline{v}_{l} = \frac{T_{o}.0 + T_{1}.(2V_{C} - V_{O})}{T} = \frac{T_{1}}{T_{1} - T_{O}} V_{O} = V_{C}$$
(2.7)

The maximum dc source voltage is over the H-bridge is given by:

$$\widehat{\nu}_{l} = V_{C} - v_{L} = 2V_{C} - V_{o} = \frac{T}{T_{1} - T_{o}} V_{o} = B. V_{o}$$

$$(2.8)$$

Where B is the boost factor and expressed as:

$$\mathbf{B} = = \frac{T_1}{T_1 - T_0} = \frac{1}{1 - 2\frac{T_0}{T}} \ge 1 \tag{2.9}$$

The output voltage from the inverter V_{ac} is given by (2.10) where M is the modulation index of the expression

$$V_{ac} = M \cdot \frac{\hat{v}_l}{2} \tag{2.10}$$

Substituting the boost factor into the equation gives:

$$V_{ac} = M \cdot B \cdot \frac{V_0}{2}$$
 (2.11)

The step up or step down of the output of voltage source pulse width modulation B_s is a factor which gives the inverter buck-boost functionality and it's expressed as:

$$B_S = M \cdot B = 0$$
 to infinity ∞ (2.12)

The voltage across the capacitor is given by:

$$V_{\rm C} = \frac{1 - \frac{T_o}{T}}{2\frac{T_o}{T}} V_o \tag{2.13}$$

The boost factor and modulation index together determines the magnitude of the buck-boost functionality of the inverter. The duty cycle of the non-shoot through phase and the shoot through phase determines the value of the Boost factor in (2.9).

One of the basic functions of the full or half H-bridge inverters is to solve the setback of leakage current in common-mode phase by applying appropriate control technique such as sinusoidal pulse width modulation; this to prevent the generation of common-operation voltage. Another procedure for solving the challenges of leakage current in common-mode is by applying doubly grounded circuits (DGC). Better safety, easy circuit design and reduced cost of investment are the some merits of DGC (Araújo, S. V e al, 2010; Lopez et al, 2010; Zhang, F e al, 2008) Applications of the full or half H-bridge inverters have some demerits; the full bridge requires 350V dc source input to generate ac voltage of 220/240V magnitude whiles the half bridge requires double of the full to generate the same ac voltage i.e. 700Vdc is required to generate 220/240V ac voltage (Yang, B et al, 2012).

The full bridge also has some drawback such as large inductor size in the filter, reduced efficiency and large ripple current. Transformer less DGC have been discussed in (Ahmed, T., & Mekhilef, S, 2014] where some operational challenges have discussed in view of grid connection of converters without transformers, this is to provide high quality power to customers. Some of the working challenges of such systems are; dc input current, regulation of the output current and total harmonic distortion, there are standards for determining the peak values for the above challenges provided by IEC and IEEE but vary across countries. Critical attention should be given to the direct current injection if the flow of this current through current devices, distribution transformer and power meters is to be avoided; this is to avoid malfunctioning and destruction of equipment which leads to increase cost for the service provider and consumer [Calais, M et, 2009; Bletterie, B. 2006, Blewitt, W. M et al, 2010).

The correct design of the passive components in the transformer less converters leads to better efficiency and performance with reduced cost of system and reduced system size, robustness of the system is also an added advantage. For example it's an established fact in coupled inductor based converter performance is greatly enhanced than individual inductor based converters ie with coupled inductor based converter, ripples in the output voltage and input current are eliminated or reduced hence the core-loss decreased which leads to reduction converter size because extra filters may not be required. Also coupled inductor based converter have quicker responds to load transients (Fang, Y., & Ma, X. 2010; Li, J., Stratakos et al, 2004; Berkovich, Y., & Axelrod, B, 2011; Wu, W et al, 2006; Zhu et al, 2011& Zhou et al, 2014).

To reduce the cost of the transformer less based converters and also improve the performance of such systems conventional inverters and Z source based topologies have presented in, research into the performance of these inverters when applied in renewable energy source have been investigated, most especially in photovoltaic systems (Bletterie, B, 2006; Anderson, J., & Peng, F. Z, 2008& Ahmed et al, 2013). The goal of this paper is to apply semi ZSI in single phase PV systems application as was done in (Yu et al, 2011). The semi ZSI utilizes coupled inductor properties to enhance the efficiency of the system.



Figure 2.11: Discontinuous and continuous voltage gains (Yu et al, 2011).



Figure 2.12: Discontinuous and continuous voltage gain curve (Yu et al, 2011).

AC to AC converters can be grouped into the following categories; buck converters, cuk converters, boost converters and buck-boost converters. These converters have certain disadvantages which hinder their smooth operation and performance; the output voltage of the buck topology cannot exceed the input and the input voltage of the boost topology is always smaller than the output voltage. In the buck-boost topology, the voltage stress on the components is very high and the output and input current flow is discontinuous.

The cuk converter also has high voltage stress across the components. To solve the high voltage stress, buck multilevel (Stala et al, 2009; Wilkinson et al, 2006) inverter can be used to minimize the voltage stress and also produce output voltage with superior qualities. Transformers are needed to provide isolation between these types of converter and the load which results in reduction of power density of the network, increased cost and increased size of the structure, reduced efficiency, and inrush current at startup, increase in harmonics for non-linear loads and voltage drops are caused by the impedance network of the transformer (Qian et al, 2011). Several ZSI topologies have been presented after the basic Z source inverter was proposed with varied conversion applications; the conversion areas of published works are; dc-ac known as an inverter, rectification i.e. dc-ac conversion, step up or step down conversion in dc-dc applications and cycloconverter application in ac-ac (Qian et al, 2011; Nguyen e al, 2013; Ahmed et al, 2016; Siwakoti et al, 2 2015; Ding et al, 2005& Ge e al, 2012).

The goal this paper (Ahmed et al, 2016) is to apply a single phase ac-ac ZSI having the following attributes: minimizing the inrush current, buck-boost abilities to produce very large output current, reducing the harmonic content, phase angle inversion or changing ability, enhancing the stability of the inverter (Fang et al, 2005). The improved version of ZSI known as qZSI possess all the merits of the basic z source structure but provides extra impetus of reduced capacitor voltage stress, continuous source current flow and joint ground linking the output and input (Nguyen et al, 2005).

The various ac-ac Z source with high frequency transformer isolation (HFTI) is presented, these topologies of converter retains the advantages of the non-isolation converter; minimizing the inrush current, buck-boost abilities to produce very large output current, reducing the harmonic content, phase angle inversion or changing ability, enhancing the stability of the inverter plus its own added advantages.

2.5 ZSI Cycloconverter Converters

In other to make any ZSI into ac-ac converter, bidirectional switches have to be used instead of the unidirectional switches and the H-bridge circuit replaced with bidirectional switches depending on the desired structure. Examples of ac-ac ZSI converter topologies are qZSI, ZSI, Γ-ZSI (Fang et al, 2005, Nguyen et al, 2010, Banaei et al, 2016). Figure 2.12. shows the various ZSI topologies incorporated with HFTI structure. Any ZS topology where more diodes are required are suitable for convention into ac-ac ZS converter because substituting the diode with an active switch will maximize the losses in the system and also escalate the price of the structure. The following Z source converters are suitable for HFTI applications due to least passive and active switch count; Basic ZSI, qZSI, Γ-ZSI, TqZSI and ITZSI.



Figure 2.13: HFTI ZS ac-ac converters (Fang et al, 2005).(a) Traditional ZSI(b) qZS(c) T-ZS(d) T-qZSI IT-ZS(f) Γ-ZS.

The different topologies shown Figure 2.13 are derived from the non-isolated converter types by adding the high frequency transformer isolation technology. The HFTI based converters have the same structural design with the difference the type of impedance network applied and the position of the impedance network. These components are same for each type of HFTI based converter; number of bidirectional switches, high frequency transformer, the output filter network (C_f and L_f), the primary and secondary blocking capacitors C_p and C_f respectively.

The number of bidirectional switches in the entire HFTI based converters is equal i.e. to say that each converter has 3 bidirectional switches in each case made up of switches $S_1 S_2$ and S_3 . Figure 2.14 shows the ideal pulse width modulation scheme for these converters. Between the switching period (1 - D)T, switch S_1 is switched on whiles switches S_2 and S_3 are switched off, also during switching period DT, Switches S_2 and S_3 are switched on whiles S_1 is switched off, all this occurs during one cycle of the period T. In practical system, the switching between the switches (S_2 and S_3) does not occur concurrently because of the different properties of time delay (switching on and off time) for each switch. This drawback introduces dead time which cause the formation of current and voltage spikes that can destroy or damage the semiconductor switches. Smooth commutation of these switches requires the introduction of appropriate control strategy and snubber circuit as presented in (Fang et al, 2005; Nguyen et al, 2010). However the snubber circuit introduced contains passive components; resistor and capacitor which adds extra cost to the system and minimizes the efficiency of the system.



Figure 2.14: Pulse width modulation scheme HFTI converters (Fang et al, 2005).

As in the case of all Z source inverters or converters, two modes of operations exist; shoot-through state and non-shoot through state. In the non-shoot through phase as depicted by Figure 2.15 switch S_1 switched on whiles switches S_2 and S_3 are switched off. Because switch S1 is a bidirectional

switch, it's able to conduct current in both directions i.e. from the source to the load and from the load to the source, in such a case, the source needs to have energy storage capabilities. In the shoot through phase, switches S_2 and S_3 conducts whiles S_1 is off. The shoot through phase is shown in Figure.2.16. Negative current from capacitor C_s flows through switch S_3 to fulfill the condition of charge balance.



Figure 2.15: Non shoot through phase (Fang et al, 2005).



Figure 2.16: Shoot through phase (Fang et al, 2005).

2.6 Magnetically Coupled ZSI

The history of Z source inverter topologies started with the basic Z source converter which was improved to derive the quasi Z source inverter followed other topologies which utilized passive components and active switches to boost the voltage gain. These topologies used switched capacitor, or switched inductor or a combination of the two; switched capacitor inductor network. The cascaded topologies followed having capacitor/diode assistance. The magnetically coupled topology was later introduced and its receiving a lot attention due its reduced component count,

power density is improved and boosting abilities of the converter is highly enhanced (Siwakoti et al, 2015; Siwakoti et al, 2016& Chub et al, 2016). Magnetically coupled Z source topologies can be categorized into two groups; two winding networks and three winding network, which is known as Y-source. The three winding network is relative new but hundreds of research have already been conducted to improve it. Example of such improvements is the introduction of quasi Y-source topology (Siwakoti et al, 2014). Examples of the two windings topologies are tran ZSI, ΓZSI, LCCTZSI, LCCAT, and QLCCTZSI (Qian et al, 2011; Chub et al, 2016; Loh et al, 2013, Adamowicz et al, 2011).

This project (Adamowicz et al, 2014) presents auto transformer based converter with two windings to minimize the number of turns needed to accomplish an increased output voltage but at the same time maintain a reduced component count and produce higher efficiency in the system. This is achieved by the application of auto-transformer technique which reduces the turns-ratio significantly, hence the power density is hugely boosted and the system cost is minimized. The circuit of the proposed network is shown in Figure 2.17. The circuit is made up of a diode, a switch, an inductor and two capacitors, an auto-transformer having primary and secondary turns coupled inductors (N₁L₁ and N₂L₂). The output voltage of the circuit is given by V₀ and this can be the input of say an inverter to produce ac voltage with an appreciable increase in voltage. The auto transformer based converter can be applied in varied conversion application such as dc-dc, dc-ac, ac-dc, and ac-ac.



Figure 2.17: Autotransformer Z source based converter (Adamowicz et al, 2014).

The switching frequency f_s of the circuit is given in (2.15) where T_s is the period of the switching cycle. Also the duty cycle D_c is given by (2.16) where t_{on} is turn on time and T_s is the period of the switching cycle.

$$Fs = \frac{1}{T_s}$$
(2.15)

$$Dc = \frac{t_{on}}{T_s}$$
(2.16)

Figure 2.18. Show the traditional coupled inductor circuit and the autotransformer coupled inductor circuit. The voltage gain V_g of the two networks are given by (2.17) for the conventional network and (2.18) for the autotransformer network.

$$V_{g} = \frac{V_{2}}{V_{1}} = n \tag{2.17}$$

$$V_{g} = \frac{V_{2}}{V_{1}} = N = n + 1 \tag{2.18}$$



Figure 2.18: A) Traditional coupled inductor (Adamowicz et al, 2014).

b) Autotransformer coupled inductor. (Adamowicz et al, 2014).

Two states of operation exist; shoot through and non-shoot through state, in the shoot through state, the switch is closed hence the diode is reversed biased and KVL analysis of the shoot through circuit of Figure 2.19. Gives equation (2.19).

$$V_{1} -+ V_{C2} + \frac{N_{2}}{N_{1}} V_{L1} + V_{L1} - V_{C1} = V_{L}$$
(2.19)

$$v_{L1} = V_{C1}$$
 (2.20)

Putting (19) and (20) together,

$$\mathbf{v}_{\rm L} = \mathbf{V}_1 + \mathbf{V}_{\rm C2} + \frac{N_2}{N_1} \mathbf{V}_{\rm C1} \tag{2.21}$$



Figure 2.19: Shoot through circuit (Adamowicz et al, 2014).

The non-shoot through phase is shown in Figure 2.20. Where the switch is opened hence the diode is conduction because its forward biased, again applying KVL to the non-shoot through circuit give the equations below:

$$v_L = V_1 - V_{C1}$$
 (2.22)

$$V_{C2} = +\frac{N_2}{N_1} v_{L1} + v_{L1} = 0$$
(2.23)

$$\mathbf{v}_{L1} = \frac{V_{C2}}{\frac{N_2}{N_1} + 1} \tag{2.24}$$



Figure 2.20: Non-shoot through circuit (Adamowicz et al, 2014).
			20		No. of Components	
Topologies	$G_v = V_{am} / V_I$	$0 < D_{st} < D_{\rm stmax}$	L	С	Coupled Inductor	Diode
Quasi-I'-Z-source [2]	$\left(1 - \frac{N_2}{N_2 - N_3} D_{st}\right)^{-1}$	$0 \leq D_{st} < \frac{N_2 - N_3}{N_2}$	1	2	1	1
Quasi-T-source or quasi-Trans-Z-source [2]	$\left(1-\frac{N_1}{N_3}D_{st}\right)^{-1}$	$0 \leq D_{st} < \frac{N_3}{N_1}$	1	2	1	1
Quasi LCCT-Z-source [2]	$\left[1-\left(1+\frac{N_1}{N_2}\right)D_{st}\right]^{-1}$	$0 \le D_{st} < \frac{N_2}{N_1 + N_2}$	1	2	1	1
LCCT [8] / LCCTAt [9]	$\left[1-\left(1+\frac{N_1}{N_2}\right)D_{st}\right]^{-1}$	$0 \leq D_{st} < \frac{N_2}{N_1+N_2}$	1	2	1	1
Proposed A-Source Network	$\left[1-\left(2+\frac{N_2}{N_1}\right)D_{st}\right]^{-1}$	$0 \leq D_{st} < \left[2 + \frac{N_2}{N_1}\right]^{-1}$	1	2	1	1

Table 2.2: comparison of the proposed A-Source Network with some Continuous Input Current

 Type Tow Windings MCIS Networks

Table 2.3 : Voltage and current stresses across the switch and diodes in A-source DC-DC converter

Component	Voltage Stress $V_{\rm DSM} = V_O$	Current Stress			
Switch SW		$I_{\rm DSM} = \frac{N V_O}{R_L \left[1 - (1 + N) D_{st}\right]} + \frac{N \left(V_I + V_{C1}\right)}{2 f_s L}$			
Diode D_1	$V_{\rm D1M} = N V_O$	$I_{\rm D1M} = \frac{I_O}{1 + \frac{N_1}{N_2}} + \frac{V_I + V_{C1}}{2f_s L}$			
Diode D_2	$V_{\rm D2M} = V_O$	$I_{\rm D2M} = (N+1)I_O$			

Table 2.4: Voltage and current stresses across the capacitors in A-source DC-DC converter

Component	Notation	Equation
Capacitor C_1	V_{C1}	$\frac{1-D_{st}}{1-(1+N)D_{st}}V_I$
Capacitor C_2	V_{C2}	$\frac{ND_{st}}{1 - (1 + N)D_{st}} V_I$
Capacitor C_O	V_{CO}	V_O

2.7 ZSI Review

A comprehensive review of all published Z source papers from 2003 to September 2013 is presented in (Siwakoti et al, 2016). The review covers the various improved topologies after the basic Z source topology was introduced, the type of control technique applied and the application or area of application of the Z source topology. As September 2013, a total of 1113 conference and journal papers have been published as shown in Figure 2.21. Broad categorization of the various topologies is depicted in Figure 2.22a and b. The modulation technique employed is based on the type of output voltage; ac or dc. Categorization of the modulation types is shown in Figure 2.23. It should however be noted that the type of semiconductor switches used will change when the converter topology changes.



Figure 2.21: Z source network published papers. (Siwakoti et al, 2016).



⁽a)



Figure 2.22: Z source topologies (Siwakoti et al, 2016).



Figure 2.23: Types Z source modulation techniques (Siwakoti et al, 2016).

2.8 Δ-Sources Network

Several impedance network topologies have been published which seeks to improve or increase the voltage gain and also reduce the passive components in the impedance network. Answer to this is found in the coupled inductor application in Z source structures because they offer reduced cost and weight coupled with increased voltage gain at reduced component count. A new impedance network derived from the Y source structure is presented in (Siwakoti et al, 2015), this topology is a novel (Δ -Source) one which provides least losses in the windings and also little magnetizing current hence productive application of the core material is gained resulting in reduced volume and weight (Sharifi, S., & Monfared, M, 2018) The cost of the Y source structure increases because of closed loop control is required to minimize the effects of leakage reactance (Siwakoti et al, 2015). The Δ -Source applies delta connection methodology in the connection of the three coupled inductors. Also the adverse effects of leakage inductance are greatly minimized to improve the converter performance. The circuit of the proposed impedance network; Δ -Source network is shown in Figure 2.24. The shoot through and non-shoot through circuit are shown in Figure 2.25a and b respectively.



Figure 2.24: Δ -Source network (Siwakoti et al, 2015).



Figure 2.25: a) Shoot through circuit b) Non-shoot through circuit

(Sharifi, S., & Monfared, M, 2018).

In the shoot through mode, the diode D_1 is reverse biased because switch SW allows the flow of current i.e. conducting as represented in Figure 2.25a. In this mode, the coupled inductors magnetizing inductance is charged via the capacitor C_1 hence the inductor voltage is given by

(2.25). Whiles the opposite condition occurs in the non-shoot through mode i.e. the diode D_1 is forward biased and the switch SW is in the opened condition; the capacitor is charged from the input V_{in} and coupled inductor's magnetizing inductance is released to the load, the voltage of the inductor in this mode is given by (2.26). Hence the capacitor voltage can be derived from (2.25) and (2.26) to give (2.27) by applying the volt-second balance law, d_{ST} is the duty cycle in the shoot through mode. The voltage gain of the proposed topology is given by (2.28). K_{Δ} is the transformer turns ratio which is given by (2.29). The relationship between the input voltage V_{in} and the output voltage during non-shoot through mode is given by (2.30)

$$V_{\rm L} = \frac{N_1}{N_3} V_{C1} \tag{2.25}$$

$$V_{\rm L} = \frac{N_1}{N_2} \left(V_{in} - V_{C1} \right) \tag{2.26}$$

$$V_{C1} = V_{in} \frac{N_3(1 - d_{ST})}{N_3 - N_1 d_{ST}}$$
(2.27)

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{1 - \frac{N_1}{N_3} d_{ST}} = \frac{1}{1 - K\Delta d_{ST}}$$
(2.28)

$$K_{\Delta} = \frac{N_1}{N_3} \tag{2.29}$$

$$\widehat{V_{out}} = V_{in} - V_L \tag{2.30a}$$

$$\widehat{V_{out}} = V_{in} \frac{N_1}{N_2} \left(V_{in} - V_{in} \frac{N_3 (1 - d_{ST})}{N_3 - N_1 d_{ST}} \right)$$
(2.30b)

$$\widehat{V_{out}} = V_{in} \left(\frac{N_3}{N_3 - N_1 d_{ST}} \right)$$
(2.30c)

Integration of z source topologies into residential or grid connected photovoltaic systems has increased over the years due to the elimination of double stage conversion with single stage conversion provided by z source inverters. In (Siwakoti et al, 2014) Z source inverter based residential photovoltaic system is presented which seeks to: a) convert or change direct voltage into alternating voltage, b) provide booting capabilities if PV voltage is less, c) to achieve peak power supply from photovoltaic panels. Two types of conventional inversion existed before the introduction of impedance structures; single stage inversion with a transformer and double stage

inversion without transformer but two converters; dc-dc and dc-ac were utilized. Figure 2.26 and Figure 2.27 shows the two topologies. In other to produce 220V of ac voltage, the photovoltaic systems should produce $340 - 680 V_{dc}$. These voltage ranges means increase cost and increased stress on the components however if the Z source topology is applied, the output power of the PV systems is reduced to 225 - 450 Vdc which translates to reduced component ratings hence reduced component stress and reduced cost. The proposed system has the following attributes: a) Maximum power tracking, booting abilities, one stage inversion, b) dead time is not required; c) shoot through abilities, d) reduced EMI functionality e) reduced component count f) adds the advantages of previous converter topologies. The boost control technique is applied and shown in Figure 2.28.



Figure 2.26: Single stage transformer converter system (Siwakoti et al, 2014).



Figure 2.27: Double stage converter system (Siwakoti et al, 2014).



Figure 2.28: Boost control technique. (Siwakoti et al, 2014).

The relationship between the input voltage and the output voltage of the converter is represented by (2.31), the photovoltaic panel output voltage is V_p , the maximum output voltage is V_o and the modulation index of the control technique is M. the boosting factor of the equation is represented by B and its expression is given in (2.32).

$$V_{o} = \frac{M.B.V_{p}}{2}$$
(2.31)

$$\mathbf{B} = \frac{1}{1 - 2\frac{T_0}{T}} \tag{2.32}$$

$$V_{o} = \frac{M}{2(2M-1)} V_{p}$$
(2.33)

2.9 Cascaded ZSI Topologies

In [(Das et al, 2008) a cascaded Z source topology is applied in photovoltaic systems. This topology combines the advantages of multilevel converters with the merits of impedance network to achieve efficient PV based inverter. The shoot through property enables flexibility and self-contained control of the wide range of the PV voltage output. The cascaded or series connection of the modules will together control the grid integration of the PV power; deadbeat control is applied in linking the PV power to the grid. The deadbeat technique is chosen over the PI method because of zero error tracking and possibility of using digital controller. The error is minimized or reduced to zero because at the start of each sampling time the current value is predicted by deadbeat

technique. The presented topology which is multilevel cascaded Z source inverter utilizes single stage inversion hence reduced loses, eliminates the need for transformer which means reduced cost of system, and also has boosting attributes. The multilevel functionality will provide quality output power because higher steps of output voltage are produced. The combined topologies will be have the following good attributes; high efficiency, increased performance, reliable, reduced system cost. The topology is shown in Figure 2.29. All the advantages and properties of the impedance network are applied in the analysis of this topology.



Figure 2.29: Cascaded multilevel ZSI (Das et al, 2008).

Similar cascaded multilevel structure using impedance source network for photovoltaic power generation is presented in (Ben-Brahim et al, 1991). The concept is the same but different multilevel structure is applied in this case, also quasi Z source topology is used instead of the basic Z source topology as in (Das et al, 2008) which means that all the advantages of the basic Z source topology is maintained coupled with the merits of QZSI; an example is the continuous current supply from the source. Some disadvantages of the cascaded multilevel inverter are; buck boost capabilities are missing, the dc link voltage is dependent on the PV panel output voltage which is not constant because it's dependent on weather conditions. All these demerits are solved with the application of the Q Z source inverter.

One major disadvantage which exists in the cascaded multilevel inverter and quasi Z source inverter is the voltage and current ripples of thee second (2^{nd}) harmonic. Several literatures have been published which seeks to probe and find solution to the voltage and current ripples of thee second (2^{nd}) harmonic (Sun et al, 2014; Zhou et al, 2013). The proposed structure is shown in Fig. 29. And its analysis is the combination of each module of q-Z source topology. Similar topology but with the addition of energy storage system such as battery is connected in parallel to capacitor C2 of Figure 2.30. This topology is known as energy stored qZS cascaded multilevel inverter (Gu al , 2018).



Figure 2.30: Cascaded multilevel qZSI (Ben-Brahim et al, 1991).

A unique modulation technique is presented in (Yu e al, 2011) which seek to reduce the leakage current in the common mode of a three phase ZSI applied in photovoltaic systems. One major problem in transformer less converters applied in grid integration of photovoltaic system is the limitation of common mode current. The absence of galvanic isolation in the transformer less converter connection produces leakage currents. The neutral point on the load experiences voltage fluctuations which are caused by extreme switching frequencies. Common mode voltage of extreme frequency via parasitic capacitance introduces the common mode voltage (Erginer et al, 2014; Essakiappan et al, 2011). Several techniques have been proposed to reduce the common

mode voltage; neutral point inverter, minimized common mode voltage modulation method, regular choke mode (Lopez et al, 2010; Hava et al, 2009; Cacciato et al, 1999). Several other methods have been proposed for the elimination or reduction of the common mode currents, research into the following papers will show some of the solutions such as modified odd pulse width modulation method (Cacciato et al, 2009; Bradaschia, F et al, 2011; Florescu et al, 2010& Shen t al, 2007). The common mode current in gird tied photovoltaic systems without a transformer possess great danger to the entire system. Certain standards have been put in place as a risk measure to help prevent disaster in the system; when the current get to a level which is above 0.3A, the inverter should be disconnected from the grid within 300ms (Erginer et al, 2013, Kerekes et al, 2007). The common mode voltage equation is given by (2.34) and Figure 2.31. Path of the leakage current. Modified near state pulse width modulation technique id the unique modulation method introduced by (Yu et al, 2011), the simulation results show a reduction in common mode voltage and common mode current and reduces the harmonic content of the system.



Figure 2.31: Path of leakage current (Erginer et al, 2013).

A new control method for Z source inverters is proposed in (Hou et al, 2013). This new control technique is termed as ONE-DIMENSION (ODZSI) which is derived from the single phase modulation method. A number of control methods to regulate the shoot through mode of the Z source inverters are mentioned in this literature, some example are; SVPWM, CBPWM (Sabeur et al, 2016; Shen et al, 2007& Peng et al, 2005), MBC, SBC, MCBC, MSVMBC (Shen et al, 2006; Chun et al, 2006; Ellabban et al, 2011; Rostami, H., & Khaburi, D. A, 2009). The maximum boost control method has the advantage producing peak voltage gain whiles utilizing minimum

shoot through period; this is achieved by converting the conventional zero states into shoot through modes and keeping the six active modes the same, this results in reducing the voltage stress on the semiconductor switches.

The main advantage of the proposed regulation technique is minimum time required for data processing which is very useful in digital applications; these merits are highly regarded when compared to SVPWM. The output voltage and current (power) is greatly enhanced by the proposed method (Hou et al, 2013). The proposed method is based on the principle where line to ground reference voltage is generated which is an average of the closest voltage level. Diagrams for the proposed control technique are shown in Figure 2.32.



Figure 2.32: a) Reference voltageb) flow chart

(Hou et al, 2013).

2.10 Series Z Source Inverter

Although Z source topology is a single stage converter system, the dc voltage for an inverter of the same structure is two; the source voltage into the impedance structure and the output voltage of the impedance structure known as the dc link which is also the source voltage of the converter. The ability to regulate the peak dc link voltage is crucial in reducing the voltage stress of the

components and also makes the inversion process smooth without drawbacks. A combination of two control methods; space vector PWM and feed forward have been applied in (Tran et al, 2007) to a three phase Z source inverter. Two methods to control the dc link voltage; peak dc link voltage control and Z source capacitor control have been examined in (Ding t al, 2007; Gajanayake et al, 2007& Huang et al, 2016). The Z source converter structure is greatly reduced when SVPWM technique is applied because in a period of one carrier, 6 shoot through modes can be installed which enhance the frequency of the system thus reduced sixe. The feed-forward control technique is utilized to derive a steady maximum dc link voltage. The process is simple; two values of constant maximum dc link voltage or output voltage. The feed-forward performs the task of a) whiles the feed-back performs the task of b). The advantage of the feed-forward control is the stability capabilities and quick response in transient modes. These control methods are applied to a series Z source converter shown in Figure 2.34. and the feed-forward control method is shown in Figure 2.33.



Figure 2.33: Feed-forward control method (Tran et al, 2007).



Figure 2.34: Series Z source inverter (Ding t al, 2007).

2.11 ZSI Wireless Power Transfer

Another area in literature where Z source has received enormous application is the wireless transfer of power, circuit breakers and energy storage systems. The concept and ideology are almost the same except for minor changes or differences. In (Hu et al, 2008), electric field coupling technology based capacitive power transfer is preferred to wireless power transfer technique. This technology is able to supply power to the load in the absence of galvanic connection using electric field coupling (Liu et al, 2009; Liu et al, 2010& Van Neste et al, 2014). The capacitive power transfer has the following advantages in contrast to inductive power transfer; little electrometric interference, reduced power losses, high power transfer capabilities even through metallic structures, reduced profile, wide application areas such as consumer electronics and implanted devices. Also it's applicable in high power transfers such as kW in EV charging (Liu et al, 2009; Dai et al, 2015; Dai et al, 2015& Liu et al, 2012). Figure 2.35 shows the generalized structure of the capacitive power transfer and Figure 2.36. Show the circuit of the proposed topology.



Figure 2.35: Generalized capacitive power transfer structure (Hu et al, 2008).



Figure 2.36: Proposed capacitive power transfer structure (Liu et al, 2009).

The coupling section of the structure is made up of conductive plates which are in pairs, copper or aluminum pads can be used, dielectric materials is used as insulation between the two plates. The structure has limitation of large reactive impedance which is solved by instigating capacitive coupling into the structure. A resonant tank is formed by series connection of capacitive coupling and tuning inductor (single). The structure is made up of five block; the source and two switches, inductor-capacitor-capacitor filter, the Z source network, capacitive coupling and the rectifier section plus load. The values of the capacitor and inductor in the inductor-capacitor-capacitor filter section are determined by:

$$C_{fl} = C_{f2} = C_f$$
 (2.34)

$$C_{f} = \frac{c_{f1}c_{f2}}{c_{f1} + c_{f2}} = \frac{c_{f2}}{2}$$
(2.35)

$$L_{f} = \frac{1}{\omega_{s}^{2} C_{f}} = \frac{2}{\omega_{s}^{2} C_{f2}}$$
(2.36)

A clarified structure of the proposed topology is illustrated in Figure 2.37. And the g-parameter describing the Z source structure is illustrated in Figure 2.38. The voltage and current of the terminals is given by (2.37).

$$\begin{cases} I_Z = g_{11}V_Z + g_{12}I_{AB} \\ V_{AB} = g_{21}V_Z + g_{22}I_{AB} \end{cases}$$
(2.37)



Figure 2.37: Simplified CPT diagram (Dai, J., & Ludois, D. C. 2015).



Figure 2.38: G parameters of the impedance network. (Dai, J., & Ludois, D. C. 2015).

From (2.36) the g parameters of the Z source component of the capacitive wireless power transfer are obtained by:

$$\begin{cases} g_{11} = \frac{2}{j\omega_s L_z + \frac{1}{j\omega_s C_z}} = \frac{j2\omega_s C_z}{1 - \omega_s^2 L_z C_z} \\ g_{12} = g_{21} = \frac{-j\omega_s L_z + \frac{1}{j\omega_s C_z}}{j\omega_s L_z + \frac{1}{j\omega_s C_z}} = \frac{1 + \omega_s^2 L_z C_z}{1 - \omega_s^2 L_z C_z} \\ g_{22} = \frac{2j\omega_s L_z^* \frac{1}{j\omega_s C_z}}{j\omega_s L_z + \frac{1}{j\omega_s C_z}} = \frac{2j\omega_s L_z}{1 - \omega_s^2 L_z C_z} \end{cases}$$
(2.38)

The resonant frequency and the operating frequency of the structure are given by equations (2.39) and (2.40) respectively.

$$\frac{1}{\sqrt{L_Z C_Z}} = \omega_Z \tag{2.39}$$

$$\frac{\omega_s}{\omega_z} = F \tag{2.40}$$

Therefore

$$\begin{cases} g_{11} = j\omega_s C_z \ \frac{2}{1-F^2} \\ g_{12} = g_{21} = \frac{1+F^2}{1-F^2} \\ g_{22} = j\omega L_z \frac{2}{1-F^2} \end{cases}$$
(2.41)

2.12 ZSI Circuit Breaker

Application of dc power has extended to ships due to the availability of good power conditioners such as converters. One application of these converters is the utilization of Z source inverters at medium power ranges for power protections i.e. circuit breakers (CB). Dc power is unable to naturally produce zero-junction as in the case of ac power hence circuit protective devices minimal (Iwamoto et al, 2001; Chang et al, 2013). An arc is produced in dc systems when current flow is severed and this arc is maintained by the inductance in the system so this makes turning off the system during fault mode very difficult (Cuzner et al,2009; Corzine et al, 2012). The z source inverter was envisaged to solve this problem in dc systems. Two types of z source circuit breakers have been developed so far; conventional z source circuit breaker and the series connected or chain circuit breaker (Corzine, K, 2013; Prempraneerach et al, 2013& Overstreet et al, 2014). The circuit diagrams for the two topologies of circuit breakers are shown in Figure 2.39. And Figure 2.40.



Figure 2.39: Conventional Z source circuit breaker (Corzine, K, 2013).



Figure 2.40: Series tied Z source circuit breaker (Overstreet et al, 2014).

These two topologies have a peculiar problem which is the restriction of the load current beyond the current levels at steady state; the situation where theirs is step increase of the load current the steady state current levels, the circuit breaker goes off because it considers the change as a fault. The proposed Z source circuit breaker solves this limitation above.

The proposed Z source circuit breaker solves this limitation above. Actually two designs are proposed in this paper (Chang et al, 2016). The new Z source circuit break is achieved by the inclusion of capacitive current divider which provides two lanes for the flow of current during a fault condition and changes in the load magnitude. The capacitor values are able to support changes in load current above the steady state value without tripping the breaker. The two proposed circuits are shown in Fig. 39. And Fig. 40. In Figure 2.41. The amount of current that can flow through the capacitors is limited by two resistors whiles in Figure 2.42. The same function is achieved by utilizing two inductors. The basic improvement in proposed topology is the ability to change load current magnitude without tripping the breaker and also suitability for medium voltage level applications such ships.



Figure 2.41: Resistor improved Z source circuit breaker (Chang et al, 2016).



Figure 2.42: Inductor improved Z source circuit breaker (Xia, C., & Li, X., 2015).

A different but novel Z source based circuit breaker topology is presented in (Xia, C., & Li, X., 2015) The aim of this topology is to reduce the reflected fault current which is taken from input or source and at the same time, maintaining a shared return ground lane. The disadvantage of the traditional Z source circuit breaker is the limitation of the system current to steady state current value, and the inability to protect system faults caused by small currents. The proposed topology focuses on the components size and the application of manual tripping which protects devices against persistent over-current state and rapid surges in current. This new topology is an improvement of the previous two topologies; crossed Z source and parallel connected Z source. Figure 2.43 shows the presented topology as new series connected Z source CB. In the SC-Zs-CB the fault current is produce by energy storage system rather than using the source current.



Figure 2.43: SC-Z source CB (Nag, S. S., & Mishra, S, 2014).

A new method to identify the zero crossing point of a Z source converter during the shoot through mode is presented in (Nag, S. S., & Mishra, S, 2014) for senseless brushless dc motor control. This procedure isolates zero crossing point against the speed regulation; hence the motor speed regulation is not influenced by the shoot through vector. Hence the speed of the brushless dc motor is regulated by active vectors and zero vectors. This method provides wide range of speed variations even though the points of detection and reference levels are not changed. Complementary pulse width modulation method is used to revamp the zero detection point. The drive systems of senseless brushless dc motor have safety and stability capabilities even during difficult conditions because of the application Z source inverter.

Energy storage systems have very useful function in the efficient performance of electric vehicles or hybrid electric vehicles. A hybrid energy storage system utilizing ultra-capacitor (UC) based battery is designed based on asymmetrical bidirectional Z source inverter. The diagram of the presented topology (Ismeil, M et al, 2014) is shown in Figure 2.44. The Z source inverter is considered the best topology for electric application because it's able to boost the dc power in a single stage conversions making the system efficient because loses in double stage conversion is neglected. The shoot through property of the Z source topology protects the main converter and also it has very protection from noise generated by EMI. The motor regulation, battery control and ultra-capacitor power allocation is successfully achieved by the system due to the modulation index and duty cycle of the shoot through mode. The proposed UC topology has the advantage of equal distribution of regenerative power by all equipment's, the input diode is not required which translate to reduced cost and loses.



Figure 2.44: Hybrid energy storage system. (Ismeil, M et al, 2014).

2.13 Switched Boost Inverter

A current fed switched boost inverter is proposed in (Tang et al, 2009), this inverter has the qualities or characteristics of the traditional Z source inverter with added attributes such as reduced passive component numbers, better immunity to effects of EMIs. The circuit of the proposed switched boost inverter is shown in Figure 2.45. The impedance structure is composed of two diodes (D_a , D_b), one inductor L and capacitor C, and an active switch S. the simplicity of the proposed inverter produces a compact layout. The peak gain of the switched boost occurs at 0.5 duty cycle which is similar to that of the traditional Z source e topology. The SBI is not suitable for application where very high boost factor is required because its boost factor is 1 - D time that of the conventional Z source inverter.



Figure 2.45: Switched boost inverter (Tang et al, 2009).

A new dc-ac converter is presented in (Ismeil, M e al, 2014) and this topology; called CFSI (current fed switched inverter) has the following features:

- Possess the merits of conventional Z source inverter and switched boost inverter, the gain of the new proposed topology is same as ZSI and retains the component count of SBI.
- Better immunity to effects of EMIs
- Continuous current input abilities thus suitable for renewable energy applications
- Quality output waveforms are produced because deadbeat is eliminated
- High boost can be achieved with small duty ratio

The proposed CFIS structure with its corresponding shoot through waveform is shown in Figure 2.46. A and b respectively. Comparison between CFSI, SBI and ZSI is shown in table 1.



Figure 2.46: a) CFIS circuit (Ismeil, M et al, 2014).

b) shoot through waveform (Ismeil, M et al, 2014).

Attri	butes	Boost-VSI Topology	ZSI	SBI	CFSI
No of	stages	2	1	1	1
No of passiv	ve elements	4	6	4	4
No of activ	e switches	5	4	5	5
No of passi	ve switches	5	5	6	6
Requirement	of dead-band	Yes	No	No	No
Extreme dut	ty operation	Yes	No	No	No
EMI noise	immunity	No	Yes	Yes	Yes
Input C	lurrent	Continuous	Discontinuous	Discontinuous	Continuous
Maximum invert	ter input voltage	V_	V_	(1-D)	V.
		(1-D)	(1-2D)	(1-2D) V _g	(1-2D)
Voltage Stress on switches	S	Vc	Not Applicable	Vc-Vg	Vc
	$S_1 - S_4$	Vc	Vc	Vc	Vc
	Da	Vc	Vc	V _c -V _g	Vc
	D_b	Not Applicable	Not Applicable	Vc	Vc
	$D_1 - D_4$	Vc	Vc	Vc	Vc
Capacitor	V _{cl} (or V _c)	$\frac{V_g}{(1-D)}$	$\frac{(1-D)}{(1-2D)}V_g$	$\frac{(1\text{-}D)}{(1\text{-}2D)}V_g$	$\frac{V_g}{(1-2D)}$
Voltage	V _{c2}	Not Applicable	$\frac{(1\text{-}D)}{(1\text{-}2D)}V_g$	Not Applicable	Not Applicable
Inductor Current	$I_{L1}(\text{or }I_L)$	$\frac{P}{V_g}$	$\frac{(1-D)}{(1-2D)}i_{AC}$	$\frac{(1-D)}{(1-2D)}i_{AC}$	$\frac{(1-D)}{(1-2D)}i_{AC}$
	I _{L2}	Not Applicable	$\frac{(1-D)}{(1-2D)}i_{AC}$	Not Applicable	Not Applicable
Modulati	on Index	$0 \le m \le 1$	$0 \le m \le (1-D)$	$0 \le m \le (1-D)$	$0 \le m \le (1-D)$
Total Devi	ice Rating	6*MBoost*Pout	5*MZSI*Pout	(7*M _{SBI} -2)*Pout	7*M _{CFSI} *Pout

Table 2.5: Performance Comparison of CFSI

2.14 Improved Switched Inductor ZSI

An improved switched inductor ZSI is presented in (Tang et al, 2009), the ISL/ZSI is proposed to solve the drawbacks of the conventional ZSI; high voltage stress on capacitors, limited voltage gain, high inrush current at startup and discontinuous current flow from the source. Also a higher duty cycle corresponds to reduced modulation index hence the quality of the output voltage is greatly reduced; total harmonic distortion content is increased. The boost factor and modulation index equations and expressions are respectively given by (2.42) and (2.43).

$$B = \frac{1}{1 - \frac{2T_o}{T}} = \frac{1}{1 - 2D}$$
(2.42)

$$M \le (1 - D) \tag{2.43}$$

To boost the voltage gain of the ZSI topology, several different topologies have been presented to address that drawback; switched capacitor-SC, switched inductor-SL, combination of switched capacitor and switched inductor-SC-SL, voltage lift-VL, voltage multiplier. The improved switched inductor topology was proposed because the switched inductor was unable to solve the problems of high voltage stress on components and high inrush currents (Xie et al,2009; Fathi, H., & Madadi, H, 2016). The new proposed topology ISLZSI is hybrid between SLZSI topology and IZSI topology; its circuit diagram is shown in Figure 2.47. Its equivalent circuit is shown in Figure 2.48. And the two states of operation; shoot through and non-shoot through circuit diagrams are shown in Figure 2.49 a and b respectively.



Figure 2.47: Improved SL Z source inverter. (Tang et al, 2009).



Figure 2.48: ISLZSI equivalent circuit. (Xie et al,2009).



Figure 2.49: a) Shoot through mode b) non-shoot through mode (Tang et al, 2009).



Figure 2.50: Voltage stress vs. duty cycle (Tang et al, 2009)



Figure 2.51: Boost factor vs. duty cycle (Tang et al, 2009).

The boost factor of the presented improved switched inductor impedance source inverter is given by (2.44).

$$B = \frac{1+D}{1-3D}$$
(2.44)

2.15 Enhanced Boost ZSI

A different Z source topology known as the enhanced boost ZSI is presented in in (Ge, B et al, 2013). This topology is derived from the combination of two other Z source topologies. The proposed topology EB-ZSI; produce quality output waveforms because higher modulation index (reduced duty cycle) is utilized. The boost factor is also significantly improved in the EB-ZSI, also EB-ZSI use the same value of duty ratio to produce higher boost factor than qZSI topologies, switched inductor ZSI topologies, cascaded ZSI topologies. Again when compared to qZSI topologies, switched inductor ZSI topologies, cascaded ZSI topologies EBZSI has lower voltage stress on passive components and switches. The inductor rating in EBZSI is minimal hence reduced system cost and reduced loses. The circuit of the proposed topology utilizes two impedance networks to achieve higher boosting factor and it's represented in Figure 2.52.



Figure 2.52: Enhanced boost ZSI (Ge, B et al, 2013).

The operation of EB-ZSI is similar to other impedance source topologies i.e. two states of operation exist; shoot through and non-shoot through modes. In the shoot through state (Figure 2.53), all switches on any leg of the convert are all concurrently switched on. Two diodes D_1 and D_2 are forward biased and two other diodes D_3 and D_4 are turned off because of negative current flowing across them. Also the input diode D_{in} is reversed biased because the capacitor voltage ($V_{c1} + V_{c2}$) is greater than the source voltage V_{in} , the inductors are in parallel connection with the capacitors hence are charged by them. In the non-shoot through state (Figure 2.54), diodes D_1 and D_2 are reverse biased and diodes D_3 and D_4 together with Din are forward biased. The boost B and buck-boost G factors are represented by (2.45).

$$\begin{cases} B = \frac{1}{2D^2 - 4D + 1} \\ G = M.B \end{cases}$$
(2.45)



Figure 2.53: EB-ZSI shoot through mode (Ge, B et al, 2013).



Figure 2.54: EB-ZSI non-shoot through mode (Ge, B et al, 2013).

2.16 Enhanced Boost qZSI

An enhanced boost qZSI topology is presented in (Husev et al, 2014). There are other similar topologies but the difference lies in the impedance network. This presented topology utilizes an active switch and has two less inductor/capacitor network when compared to similar topology which uses 2 switched Z source network even though it produces the same boost factor. Also the number of diodes is reduced by one and incorporates an active switch into the circuit. The efficiency is highly improved because the component stress is minimized by half thus significant reduction in the conduction losses. Figure 2.55a and 55b show the two enhanced boost qZSI. The boost factor of the proposed topology is the same as (44).



Figure 2.55: a) ESqZSI with 2 Z source network (Husev et al, 2014). b) ESqZSI with an active switch (Husev et al, 2014).

The proposed enhanced boost qZSI with an active switch is shown in Figure 2.55b. This topology is made up of the following components; an output low pass filter, two capacitors C_1 and C_2 , two inductors L_1 and L_2 and four diodes D_1 , D_2 , D_3 and D_4 . Just like other Z source networks; this topology has two states of operation; shoot through and non-shoot through. Figure 2.56 and shows the shoot through mode and non-shoot through modes. In the shoot through mode, the active switch is gated and diodes D_1 , D_2 , D_3 are not conducting because they are reverse biased but diode D_4 is forward biased. The capacitor at this stage is charged and begins to charge the inductor. Power is not transferred to the inverter/load because of the short circuit of the shoot through state. Applying KVL to Figure 2.56b yields the following expressions:

$$\begin{cases} L_1 = \frac{di_{L_1}}{dt} = V_i + V_{C1} \\ L_2 = \frac{di_{L_2}}{dt} = V_{C1} + V_{C2} \end{cases}$$
(2.46)

$$\begin{cases} i_{C1} = -i_{L1} - i_{L2} = C_1 \frac{dV_{C1}}{dt} \\ i_{C2} = -i_{L2} = C_2 \frac{dV_{C2}}{dt} \end{cases}$$
(2.47)



Figure 2.56: a) Shoot through mode b) non-shoot through mode (Husev et al, 2014).

In the non-shoot through mode, the opposite of the shoot through state phenomena occurs. The active switch and diode D_4 are turned off and diodes D_1 , D_2 , D_3 are forward biased. The capacitor is charged by the source the inductor provides power for the dc link. Applying KVL to Figure 2.56a yields the following expressions:

$$\begin{cases} L_1 = \frac{di_{L1}}{dt} = V_i - V_{C2} \\ L_2 = \frac{di_{L2}}{dt} = V_{C2} - V_{C1} \end{cases}$$
(2.48)

$$\begin{cases} i_{C1} = -i_{L2} - I_{PN_{non}} = C_1 \frac{dV_{C1}}{dt} \\ i_{C2} = i_{L1} - i_{L2} = C_2 \frac{dV_{C2}}{dt} \end{cases}$$
(2.49)

2.17 Neutral Point Clamped qZSI

Combination of neutral point clamped inverter topology and quasi Z source inverter topology is presented in (Ho, A. V., & Chun, T. W., 2018)and (Axelrod, B et al, 2008). The NPCqZSI topologies combine the advantages of the NPC and qZSI; quality output waveform with reduced harmonic content, single stage inversion, high efficiency, buck-boost capabilities, continuous drawn current at source, high immunity to EMIs, reduced component stress caused by voltage, shoot through potential. In (Ho, A. V., & Chun, T. W., 2018), a three level NPCqZSI topology is presented which has continuous current input advantage when compared to other NPCqZSI topologies. The 3L-NPCqZSI topology is derived by joining two impedance networks as shown in Figure 2.57. This technique results in the topology having wide range of source voltage application such as PV systems, continuous current input from source, heavily reduced component stress, high switching capabilities hence high quality output voltage waveforms. Analysis of the circuit is similar to qZSI analysis plus the switching pattern for the neutral point clamped inverter, the boost factor for the proposed inverter is given by (2.50).

$$B = \frac{1}{-2D_S + 1}$$
(2.50)



Figure 2.57: 3L NPCqZSI (Ho, A. V., & Chun, T. W., 2018).

In (Axelrod, B et al, 2008)., two circuits of the proposed modified quasi Z source inverter are provided, the first is a three level modified qZSI shown in Figure 2.58 and the second is cascaded 5 level modified qZSI shown in Figure 2.60. The proposed circuit is made up quasi impedance network, neutral point clamped circuit and an H bridge connected to the load. The operation of the circuit is composed of two modes; shoot through and non-shoot through.



Figure 2.58: Modified qZSI (Axelrod, B et al, 2008).

There's a neutral point located between capacitors C_1 and C_2 , this point provides two modes of operation in the shoot through mode known as the upper and lower shoot through states (Figure 2.59). In upper shoot through mode, diode D_1 is reverse biased and switches S_1 , S_2 and S_3 are gated on ad diodes D_i and D_2 are forward biased. Capacitor C_1 charges inductor L_1 and the load voltage is provided by Capacitor C_3 . In lower shoot through mode, diode D_2 is reverse biased, switches S_1 , S_3 and S_4 are gated on and diodes D_i and D_1 are forward biased. The voltage is given by capacitor C_4 and inductor L_2 is charged by capacitor C_2 .



Figure 2.59: Upper and lower shoot through mode (Axelrod, B et al, 2008).

Figure 2.60 show the five level modified quasi Z source cascaded inverter. This topology being 5level inverter means that it's a symmetrical topology, varying the voltage source each cell of the topology will produce a much higher level which will translate into quality output wave form.



Figure 2.60: 5-level Modified qZSI (Axelrod, B et al, 2008).

2.18 Comparison

This section compares the advantages and disadvantages of some selected topologies and also graphs showing the performance of the boost factor and against duty ratio are shown for the selected topologies.

Topology	Merits	Demerits
	Reduced voltage stress	Discontinuous source current input
Quasi ZSI (DCI)	Common ground	
	Continuous current input	
Quasi ZSI (CCI)	Common ground	
	Reduced voltage stress	
	• No inrush current	
	• Filters not required	• Uses 2 dc sources
Embedded ZSI	• Reduced capacitor ratings	
	• Diode blocking voltage is lower	
Bidirectional ZSI	• Current flow is bidirectional	• Increased cost due to switch

Table 2.6: Merits and Demerits comparison



Figure 2.61: Boost factor curves (Rostami, H., & Khaburi, D. A, 2009).



Figure 2.62: Boost factor and duty ratio curves (Rostami, H., & Khaburi, D. A, 2009).



Figure 2.63: Boost factor and duty ratio curves (Rostami, H., & Khaburi, D. A, 2009).



Figure 2.64: Boost factor of qZSI topologies (Rostami, H., & Khaburi, D. A, 2009).

2.19 Conclusion

Since the introduction of Z source inverters, various topologies of ZSI have been introduced which seeks to solve the drawbacks of the conventional Z source inverter. This chapter of my thesis reviewed these various topologies from the standpoint of improvements over the previous version, suitability for commercial or industrial application, circuit and mathematical analysis, boost factor improvements, reduction in number of passive and active components, continuous or discontinuous current input. This review section has broaden my knowledge about Z source inverter topologies, their application, usefulness in academic or research purpose and also providing solutions to the limitations of the conventional voltage and current source inverters.

CHAPTER 3 POWER CIRCUIT DESCRIPTION DEVELOPMENTS AND THE SIMULATION RESULTS

3.1 Introduction

The importance of power inversion using inverter devices is becoming an integral part of power systems such as distributed generations, flexible ac transmissions, adjustable industrial drives, power conditioners and integration of renewable energy into grid systems. The function of dc-ac inverter is not only to change dc voltage into ac voltage but also perform necessary power conditioning to give suitable voltage and frequency with good quality waveforms devoid of harmonic contents. Basically the topology of the inverter determines the magnitude of the output to a corresponding frequency. The conventional voltage source inverter also known as voltage fed inverter and the current source inverter or current fed inverter are the bedrocks for the development of dc-ac inverter. They are very useful in industrial and non-commercial applications but they are composed of a number of drawbacks which has led to the development of other inverter topologies such Z source inverters.

3.2 Selected Topology

The selected impedance source inverter under investigation is the switched capacitor and switched inductor in a generalized topology form. Impedance source converters have the major advantage of voltage gain boosting capabilities which are absent in the conventional voltage and current source converters. In other to increase the voltage gain capabilities in VSI or CSI, boost dc-dc topologies were connected to VSI and CSI topologies which increased the weight, losses, cost and minimized the efficiency.

The conventional Z source inverter is a combination of impedance network with either the conventional voltage source inverter or current source inverter. The impedance network is an X shaped structure made up of four passive components; two inductors and two capacitors. The passive components are symmetrical in nature; the inductors have same magnitude and the capacitors have same magnitudes. The past decade has seen rapid development of the conventional Z source inverter in the areas of application, control, modulation, component type and size, circuit

modeling and boosting capabilities. The gains or boosting capabilities of conventional ZSI is infinite theoretically only, in practical applications, factors like minimized spectral conduct and high component stress limits the voltage gain capabilities.

The generalized form of switched capacitor and switched inductor impedance source inverter is presented in this thesis, the generalized SC/SL topologies maintains the advantages of the switched capacitor and switched inductor with increased boosting capabilities when presented in the generalized form. The generalized SL topology is presented in the voltage source form whiles the generalized SC topology is presented as current source inverter.

3.3 Switched Inductor and Switched Capacitor ZSI

The switched inductor topology is obtained by making changes to the conventional Z source inverter topology; switched inductor cells are used to replace the inductor network in the conventional ZSI to obtain the switched SL topology. The first application of the switched inductor topology is the direct current to direct current converters (Peng, F. Z., 2003). The switched capacitor topology is obtained from switched inductor topology; the switched inductor cell is made up of inductors and diodes, the inductors are replaced with capacitors, the capacitors in the crossed (X) shape are replaced with inductors. The source the switched capacitor is current and its direction of flow is opposite to the voltage source the switched inductor topology. Fig. 1a and 1b are the circuits of switched inductor and switched capacitor topologies respectively.



Figure 3.1: a) Switched SL (Zhu, M et al, 2010). b) Switched SC (Peng, F. Z., 2003).

Analysis of the switched inductor and switched capacitor topologies are similar to the conventional ZSI topology, shoot through and no-shoot though modes are applicable. In the switched SL topology, the shoot through mode is achieved by concurrently turning on all switches on the same leg of the three phase bridge inverter. For example, switches SA and SA' or SB and SB' or SC and SC' will be turned on simultaneously. When this is done, diodes D2', D2, D1 and D' are forward biased hence they will conduct but diodes D3, D3', and D will not conduct because they are reverse biased. By virtue of symmetry, the passive components will have same magnitudes:

$$V_{L} = V_{L1} = V'_{L1}$$
(3.1)

$$V_{\rm C} = V_{\rm C1} = V_{\rm C2} \tag{3.2}$$

The maximum output voltage (ac) V_{ac} , maximum dc link voltage V_i , capacitor voltage V_C and inductor voltage V_L are expressed by the equations below, the equations are valid for the ranges:

$$M \le \frac{23}{20} \text{ and } d_{ST} < 0.333$$
$$V_{ac} = \frac{M (1+d_{ST})}{1-3d_{ST}} \frac{V_{dc}}{2}$$
(3.3)

$$V_{\rm C} = \frac{1 - d_{ST}}{1 - 3d_{ST}} V_{dc} \tag{3.4}$$

$$V_{i} = \frac{1 + d_{ST}}{1 + 3d_{ST}} V_{dc}$$
(3.5)

$$VL = \frac{V_{dc} - V_C}{2}$$
(3.6)

The boost factor β of the switched inductor topology is expressed by:

$$\beta = \frac{1+d_{ST}}{1-d_{ST}} \tag{3.7}$$

The switched capacitor topology is obtained from switched inductor topology; the switched inductor cell is made up of inductors and diodes, the inductors are replaced with capacitors, the capacitors in the crossed (X) shape are replaced with inductors (Siwakoti et al, 2015). Shoot through and non-shoot through analysis of the switched SC is also possible, the shoot through mode is referred to as *open circuit* and the non-shoot through mode is referred to as *non-open*
circuit. The open circuit mode is achieved by switching off all switches in inverter bridge and the following diodes are forward biased; D3, D3', and D. but the following diodes will not conduct because they are reverse biased; D2', D2, D1 and D'. in the non-open circuit analysis, the following diodes conducts because of forward biased state; D2', D2, D1 and D' whiles diodes D3, D3', and D are reverse biased. Because the switched SC is a current source inverter, the following current values needs to be determined. Capacitor current I_c , inductor current I_L , maximum output current (ac) I_{ac} , maximum dc link current I_i , and source current I_{dc} , the equations are valid for the ranges:

$$M' \le \frac{23}{20}$$
 and $d_{ST} < 0.333$
 $I_C = I_{C1} = I'_{C1}$ (3.8)

$$I_{L} = I_{L1} = I_{L2}$$
(3.9)

$$I_{\rm C} = \frac{I_{dc} - I_L}{2} \tag{3.10}$$

$$I_{ac} = \frac{M'(1+d_{oc})}{1-3d_{oc}} I_{dc}$$
(3.11)

$$I_i = \frac{1 + d_{oc}}{1 - 3d_{oc}} I_{dc}$$
(3.12)

$$I_{\rm L} = \frac{1 - d_{oc}}{1 - 3d_{oc}} I_{dc} \tag{3.13}$$

The boost factor β of the switched capacitor topology is expressed by:

$$\beta = \frac{1+d_{oc}}{1-d_{oc}} \tag{3.14}$$

3.4 Generalized Switched Inductor and Switched Capacitor

The generalized topology presented in this thesis is about the impedance network only not the whole inverter circuit, to simply put it, it's cascading of the switched impedance network for both SL and SC. The generalized switched inductor impedance source inverter is shown in Fig. 2 whiles the generalized switched capacitor impedance source inverter is shown in Fig. 3. Also it should be noted that the passive components in the X shaped are not affected in the generalized form. There's only one X shaped structure in the generalized form for both cases.



Figure 3.2: Generalized switched inductor (Li, D., et al, 2011).



Figure 3.3: Generalized switched capacitor (Li, D., et al, 2011).



Figure 3.4: Tapped inductor ZSI (Zhu, M et al, 2010).



Figure 3.5: Cascaded alternate ZSI (Li, D., et al, 2011).



Figure 3.6: Trans- ZSI (Qian, W., Peng, F. Z., & Cha, H., 2011).

The switched inductor structure of Figure 3.1a constitutes the building block for the generalized form of the switched inductor. Basically the switched inductor structure in the upper and lower arms of the inverter is the same; three diodes and two inductors on each side. But in the general form, each cell of switched inductor is made up of three diodes and one inductor as shown in Figure 3.2. Also in the general form of the switched capacitor, the each cell is made up of three diodes and one capacitor as shown in Figure 3.3. Basically the fundamental block of the generalized form has two inductors or two capacitors plus three diodes for each case; the next cell after the fundamental block is made up of one inductor or one capacitor plus three diodes each case. Shoot through and non-shoot through modes is permissible. In the shoot through mode, diodes D and D_{3n} are reversed biased hence will not conduct but diodes D_{3n-2} and D_{3n-1} are forward biased hence will conduct, the capacitor scharge the inductors via parallel connections hence inductor voltage equals to the capacitor voltage. The opposite of the shoot through mode will occur in the non-shoot through mode; diodes D and D_{3n} are forward biased hence will conduct but diodes

 D_{3n-2} and D_{3n-1} are reversed biased hence will not conduct. The inductor current feds the inverter bridge which supplies voltage to the load (ac). *N* represents the number of inductors.

$$V_{\rm C} = V_{\rm L} \tag{3.15}$$

$$V_{\rm L} = \frac{V_{dc} - V_C}{N+1}$$
(3.16)

$$v_i = \frac{1 + Nd_{ST}}{1 - (N+2)d_{ST}}$$
(3.17)

$$v_{ac} = \frac{M[1+Nd_{ST}]}{1-(N+2)d_{ST}} \frac{V_{dc}}{2}$$
(3.18)

$$V_{\rm C} = \frac{1 - d_{ST}}{1 - (N+2)d_{ST}} V_{dc} \tag{3.19}$$

The boost factor β of the generalized switched inductor topology is expressed by:

$$\beta = \frac{(1+Nd_{ST})}{[1-(N+2)d_{ST}]} \tag{3.20}$$

These equations are valid for the ranges:

$$d_{ST} < \frac{1}{N+2}, M \le \frac{23}{20}(1 - d_{ST})$$
 (3.21)

In the case of generalized switched capacitor; Figure 3.3, two states of operations exist; open circuit operation and non-open circuit operation. The open circuit state is achieved by turning off all switches in the inverter bridge, this cause forward and reverses biasing of the diodes, diodes D3n and D are forward biased whiles diodes D3n-2 and D3n-1 are reverse biased, capacitors are charged by the inductor currents. In the non-open circuit analysis, diodes D3n and D are reverse biased whiles diodes D3n-1 are forward biased. The following mathematical equations are valid for generalized SC inverter in the open and non-open circuit states.

$$i_{\rm C} = I_{\rm L} \tag{3.22}$$

$$i_{\rm C} = \frac{I_{dc} - I_L}{N+1}$$
 (3.23)

$$i_i = \frac{1 + Nd_{OC}}{1 - (N+2)d_{OC}}$$
(3.24)

$$i_{ac} = \frac{M'[1+Nd_{OC}]}{1-(N+2)d_{OC}} I_{dc}$$
(3.25)

$$I_{L} = \frac{1 - Nd_{OC}}{1 - (N+2)d_{OC}} I_{dC}$$
(3.26)

The boost factor β of the generalized switched capacitor topology is expressed by:

$$\beta = \frac{1 + Nd_{OC}}{1 - (N+2)d_{OC}} \tag{3.27}$$

The main disadvantage of the generalized switched inductor and switched capacitor topologies is the increased number of passive components, but this can be an added advantage when compared to desired boosting high gain requirements. Comparative analysis of switched inductor and switched capacitor topologies with newer versions of impedance source inverter are done to ascertain the merits and demerits of switched inductor and SC topologies. Switched inductor and switched capacitor inverters have the same results so it's prudent to use of them for the analysis and the switched inductor topology will be used for comparative analysis with other topologies of impedance source inverters. Switched inductor topology will be compared to the following topologies; TL impedance source inverter, Trans impedance network inverter and Cascaded Z source inverter.

The first comparison is with the Tapped inductor (TL) impedance source inverter (Figure 3.4). The circuit is made up of four diodes in the upper and lower limbs and two tapped inductors for the upper and lower limbs. The SL and TL impedance source inverters have the same magnitude of capacitor voltage and voltage gain. But unfortunately, TL inverter is only applicable to inverters where the source/input is voltage not current. One advantage of TL inverter over SL topology is reduced number of diodes but this minimum number of diodes comes with bigger blocking voltage much higher than SL topology. The blocking voltage equations for SL and TL topologies are given bellow, where $-v_i$, V_{D1} , and V_{D2} are the diodes voltages for diodes D, D_{3n-1} , and D_{3n} respectively for the SL topology, whiles for the TL topology, V_D , V_{D1TL} , and V_{D2TL} are the diodes voltages for diodes D, D_{TL1} , D_{TL2} and D_{TL3} , D_{TL4} respectively. From (3.28) and (3.29) it's evident that the diode blocking voltage in TL is much greater than SL topology which means that the voltage stress on the diodes are much higher and also inductor stresses are also increased.

$$\begin{cases}
-v_{i} = -\frac{1+Nd_{ST}}{1-(N+2)d_{ST}}V_{dc} \\
V_{D2} = -\frac{1-d_{ST}}{1-(N+2)d_{ST}}V_{dc} \\
VD_{1} = -\frac{d_{ST}}{1-(N+2)d_{ST}}V_{dc}
\end{cases}$$
(3.28)

$$\begin{cases}
V_D \\
V_{D1_{TL}} = \frac{V_D}{1 - (\gamma_{TL} + 2)d_{ST}} V_{dc} \\
V_{D2_{TL}} = \frac{\gamma_{TL}(1 - d_{ST})}{1 - (\gamma_{TL} + 2)d_{ST}} V_{dc}
\end{cases}$$
(3.29)

The second comparison is the Trans ZSI topology (Figure 3.6); this topology has a much lower component count when compared to SL and TL topologies. One capacitor, one diode and a coupled inductor with a transformer having a turns ratio of γ_{TZ} constitute the impedance network. The equations of the Trans ZSI topology is much explained in [3.3]. The blocking voltage capacity in the Trans ZSI topology is much higher than TL and SL topologies but it has a reduced voltage gain. A sudden rush in the instantaneous current in the Trans ZSI topology is caused by the shoot through mode due to windings voltage being low, the reduced component is a trade for transferring much higher stresses of this topology to other components in the circuit. The turns ratio in the Trans ZSI topology is much higher, also its topology is not limited to voltage source inverters only. The last comparison is the cascaded ZSI topology as shown in Figure 3.5 on page 60. SC and SL structures are able to evenly share the stresses on all components in the circuit but inter parameter difference cause difference voltage stress across the capacitors in series connection. However in the alternate cascaded topology offers better voltage/stress balance on inverter components such as diodes, capacitors and inductors. Cascaded and VSI Trans ZSI topologies have a lower voltage gain when compared to SL and SC topologies. Table 3.1 shows the comparison between the various aforementioned topologies.

	Tra	uns ZSI	SL ZSI	Tapped Inductor (TL)
Diode Voltage	$V_{D_{TZ}} = -\frac{1}{1-1}$	$\frac{\gamma_{TZ}}{(\gamma_{TZ}+1)d_{ST}}V_{dc}$	$\begin{cases} -v_{i} = -\frac{1 + Nd_{ST}}{1 - (N+2)d_{ST}}V_{dc} \\ V_{D2} = -\frac{1 - d_{ST}}{1 - (N+2)d_{ST}}V_{dc} \\ VD_{1} = -\frac{d_{ST}}{1 - (N+2)d_{ST}}V_{dc} \end{cases}$	$V_{D1_{TL}} = \frac{V_D}{1 - (\gamma_{TL} + 2)d_{ST}} V_{dc}$ $V_{D2_{TL}} = \frac{\gamma_{TL}(1 - d_{ST})}{1 - (\gamma_{TL} + 2)d_{ST}} V_{dc}$
Maximum Output voltage	$\frac{M}{1 - (\gamma_{TZ} + 1)d_{ST}} \frac{V_{dc}}{2}$		$\frac{M[1+Nd_{ST}]}{1-[N+2]d_{ST}} \frac{V_{dc}}{2}$	$\frac{M[1+\gamma_{TL}.d_{ST}]}{1-[\gamma_{TL}+2]d_{ST}}\frac{V_{dc}}{2}$
Boost Factor	$\frac{1}{1-(\gamma_{TZ}+1)d_{ST}}$		$\frac{1+Nd_{ST}}{1-(N+2)d_{ST}}$	$\frac{1+Nd_{ST}}{1-(N+2)d_{ST}}$
	Trans ZSI	Embedded	Conventional	DC –Link Embedded
Capacitor Voltage	$\frac{1-d_{ST}}{1-(\gamma_{TZ}+1)d_{ST}} V$	$\frac{1 + Nd_{ST}}{1 - (N+2)d_{ST}} \frac{V_{dc}}{2}$	$\frac{1-d_{ST}}{1-(N+2)d_{ST}} V_{dc}$	$\frac{(N+1)d_{ST}}{1-(N+2)d_{ST}}$

Table 3.1: Comparison of ZSI I topologies

3.5 Simulation Results

PSCAD software is used to simulate the impedance source inverters under investigation; cascaded topology, Tapped inductor topology, Trans ZSI topology and switched inductor topology. The input voltage is 33.5V for the impedance network connected to three phase inverter Bridge, the load is a resistive-inductive (RL) load with the following parameters R is 460hms and inductor is $5x10^{-3}$ H. Parameters for controlling the inverter are M = 0.85 and d_{ST} = 0.15.



3.5.1 Simulation Results for the Alternate Cascaded ZSI Topology

Figure 3.7: Cascaded - ZSI simulations results

Figure 3.7 shows the simulations results for the alternate cascaded Z source inverter, various components output waveforms have been illustrated. The cascaded impedance network is applied to three phase full bridge network. From Figure 3.7, the various parameters are generated; Li which is the inductor input current, two diodes voltages VD and VD2 blocking reverse voltages for the two sources and VD1 blocks reverse voltage between the two cells in the cascaded topology. Vdc is the impedance network output voltage. VL1 and VL2 are the inductor voltages.



Figure 3.8: Cascaded - ZSI simulations results

Figure 2.8 shows the second part of simulation results for the alternate cascaded Z source inverter, the output waveforms of Figure 3.8 shows results for the following parameters; i_{abc} is the ac current output of the inverter bridge, the inverter bridge output voltage across phase A and B is given by v_{ab} , the capacitor voltages are given by V_{c1} and V_{c2} . Also the inductor currents and capacitor currents are represented by i_{L1} , i_{L2} and i_{C1} , i_{C2} respectively.

The remaining simulation results for the alternate cascaded Z source inverter is illustrated in Figure 3.9 where the following parameter graphs are shown; phase voltages v_a , v_b and v_c , phase currents i_a , i_b and i_c , the impedance network output current i_{dc} , diode current i_D are all illustrated by the output waveforms.



Figure 3.9: Cascaded - ZSI simulations results

3.5.2 Simulation results for the switched inductor ZSI topology



Figure 3.10: SL - ZSI simulations results



Figure 3.11: SL - ZSI simulations results



Figure 3.12: SL - ZSI simulations results

In other to conduct an efficient comparison of the various Z source topologies under investigation similar simulation results are generated for all of them. In the case of the switched inductor topology, three figures are produced to show the simulation results, in the Figure 3.10, the waveforms of the following parameters are produced; the inductor currents i_{L1} , i_{L2} and capacitors currents i_{c1} , i_{c2} and the phase A and B output voltage v_{ab} and finally the output currents for the three phase inverter i_{abc} .

In Figure 3.11, the individual phase output waveform for the voltage and current are represented by v_a , v_b , v_c and i_a , i_b , i_c respectively. The impedance network input voltage and output voltage is given by V_i and V_{dc} respectively. Similarly the impedance network input current and output current are given by ii and i_{dc} respectively.

The source voltage blocking diode VD and the impedance network diode voltages are given by VD1 and VD2.

In Figure 3.12 the output waveform for the inductor currents i_{L1} and i_{L2} are shown, also the capacitor voltages V_{c1} and V_{c2} are represented, the inductor voltage V_L and diode voltage V_{D2} are also illustrated.



3.5.3 Simulation results for the Tapped Inductor ZSI Topology

Figure 3.13: TL - ZSI simulations results

Figure 3.13 shows the output waveform for the tapped inductor Z source inverter, similar to the simulations of the previous topologies, the following parameters are illustrated in Figure 3.13; the impedance network input voltage V_i and output voltage V_{dc} , the impedance network input current ii and output current i_{dc} , the source input blocking diode voltage V_{D_TL} , source diode current i_D , the impedance diode voltages V_{D1_TL} , V_{D2_TL} .



Figure 3.14 a: TL - ZSI simulations results



Figure 3.14 b: TL - ZSI simulations results

In Figure 3.14a, the following components output waveforms are illustrated; inductor voltage V_{L1} , the two inductor currents i_{L1} and i_{L2} , the capacitor voltages V_{c1} and V_{c2} and finally the second diode voltage V_{D2_TL} in the impedance structure. In Figure 3.14b, the following component output waveforms are illustrated; the three phase output voltage v_a , v_b and v_c , also the three phase output currents i_a , i_b and i_c , phase A and B output voltage is also shown, the three phase output current on a single graph is also shown.

3.5.4 Simulation Results for the Trans ZSI Topology



Figure 3.15 a: Trans - ZSI simulations results







Figure 3.15 c: Trans - ZSI simulations results

The output waveform of the Trans Z source inverter is segmented in four parts in Figure 3.15a to Figure 3.15d. In Figure 3.15a the output waveforms for the following components are shown; the impedance input and output voltage and current; V_i , V_{dc} and ii and i_{dc} respectively. The source diode voltage V_{D_Trans} , source diode current i_D and input current after the diode v_i .



Figure 3.15 d: Trans - ZSI simulations results

In Figure 3.15b and 15c, the three phase output voltage v_a , v_b and v_c , also the three phase output currents i_a , i_b and i_c , phase A and B output voltage is also shown, the three phase output current on a single graph is also shown. In Figure 3.15d, the impedance output current idc, inductor currents i_{L1} and i_{L2} , and capacitor current and voltage i_{c1} and v_{c1} respectively are illustrated.

3.6 Conclusion

Brief mathematical analysis of the four impedance topologies; Trans ZSI, TL ZSI, cascaded ZSI and switched inductor ZSI and simulation results have been provided for in this chapter of my thesis. From the simulation results produced, its proven that there's general improvement in the structure and output parameters of the four topologies over the traditional ZSI topology, the goal of this thesis was to show that the generalized SL topology provides better boosting or voltage when compared to conventional Z source inverter whose boosting limitation is due to low modulation ratio which cause bad spectral execution and too much stress caused by the components. Also comparing generalized SL topology to TL ZSI, alternate cascaded ZSI and Trans ZSI topologies show better boosting factor. Generalizing the SL topology provides the prospects of generalizing the other three topologies thereby improving on the various advantages or merits.

CHAPTER 4 CONCLUSION AND RECOMMENDATIONS

4.1 Conclusion

The disadvantages of voltage source inverter (VSI) which hinders it efficient applications in power systems are; VSI operates as a buck converter; the generated output voltage is smaller than the input voltage hence the voltage transfer ratio is limited, short circuit faults will cause damage to inverter components such diodes and switches; immunity to noises generated by electromagnetic interferences are not possible. However, the size of VSI is small and compact; the output voltage waveform is independent of the type of load. The current source inverter (CSI) on the hand has the following drawbacks; functions as a boost inverter, when applied to light loads the CSI performance is unsteady, in other to step-up or step-down the input or output voltage more converters are required. However some advantages of CSI are; for commutation purposes the use of thyristor is uncomplicated. Both VSI and CSI have increased cost when high boosting functionality is required, efficiency is reduced by the introduction of buck-boost converters, size and weight also increases hence will not be suitable for applications where these factors are of great importance.

The selected impedance source inverter under investigation is the switched capacitor and switched inductor in a generalized topology form. Impedance source converters have the major advantage of voltage gain boosting capabilities which are absent in the conventional voltage and current source converters. In other to increase the voltage gain capabilities in VSI or CSI, boost dc-dc topologies were connected to VSI and CSI topologies which increased the weight, losses, cost and minimized the efficiency.

The generalized form of switched capacitor and switched inductor impedance source inverters are presented in this thesis, the generalized SC/SL topologies maintains the advantages of the switched capacitor and switched inductor and introduces increased boosting capabilities when presented in the *generalized* form. The generalized SL topology is presented in the voltage source form whiles the generalized SC topology is presented as current source inverter. Simulation results for the generalized SL topology and three other inverter topologies (TL, Trans and Cascaded) are presented in chapter three. Comparative analysis these four inverter topologies shows that; switched inductor and tapped inductor topologies have higher maximum dc-link voltages than

cascaded and Trans ZSI topologies. The highest reverse blocking voltage is endured by the Trans ZSI structure. Switched inductor and cascaded topologies have the least blocking voltages. The cascaded topology has lower diode and capacitor voltage ratings hence lower rating components are applied which reduce stress and losses.

Comparative analysis of the four topologies based on stress or dc link voltage, capacitor and diode voltage, and capacitor stress have been illustrated in Fig. 7 and Fig. 8. Basically the performance of switched inductor and the other three topologies have been given in the diagrams of Fig. 7 and Fig. 8. In the case of voltage stress, switched inductor and tapped inductor topologies have minimum stress than the other two topologies; cascaded Trans ZSI. In the case of diode and capacitor voltages, the cascaded topology has better spread of stress on the components that the remaining three topologies, switched inductor topology outperformed the other two topologies; tapped inductor and Trans ZSI. When this analysis is done from the view point of total diode and voltage magnitude, the switched inductor poses the maximum total stress of diodes due to the increased number of diodes used; the two inverters with the least total diode stress are the cascaded and Trans ZSI topologies. The total stress due the capacitor voltage is however lower in switched inductor and tapped inductor topologies, the other two topologies; cascaded and Trans ZSI maximum total stress due to the capacitor voltages. The capacitor size in the Trans ZSI topology is equivalent to two capacitors in the switched inductor and tapped inductor topologies (Peng, F. Z., 2003). It's sufficient to say that the use of lower components in switched inductor and the cascaded topologies gives the merits of better spread of voltage stress and reduced losses due to conduction.

In this thesis, generalized switched inductor and switched capacitor inverters were investigated with emphasis on the switched inductor topology. The switched inductor simulation results were compared to three other inverter topologies. The results confirms superior advantages of the switched inductor in areas of voltage gain or boosting factor, reduced voltage stress and reduced capacitor ratings over the other inverter topologies. For better application of dc link voltage and reduced component stress, higher modulation index can be applied. Basically it is confirmed that the generalized switched inductor and switched capacitor topologies have much higher boosting factor than traditional ZSI and conventional SL and SC topologies.

4.2 Recommendations

For the successful progression toward to development of switched inductor and switch capacitor Z Source inverters in future, we suggest seek ways of reducing the number of components in the generalized switched inductor and switched capacitor topologies; the huge number of components especially passive components is a direct link to increase the cost and the losses of the converter.

In addition, we suggest finding some ways of including active components into the structure to increase the possibility of maximum control of the topology will be investigated . The concept of generalization can be transferred to newer ZSI topologies.

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