

**ANALYSIS AND PWM CONTROL OF SWITCHED BOOST
INVERTER**

**A THESIS SUBMITTED TO THE GRADUATE
SCHOOL OF APPLIED SCIENCES
OF
NEAR EAST UNIVERSITY**

**By
TARIQ MOHAMMED ATEEYAH MOHAMMED**

**In Partial Fulfillment of the Requirements for
the Degree of Master of Science
in
Electrical and Electronic Engineering**

NICOSIA, 2019

**TARIQ MOHAMMED ATEEYAH
MOHAMMED**

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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ABSTRACT

The Z source inverter or impedance source inverter is derived by placing an impedance network composed of inductor and capacitor with symmetrical features between the power and the inverter bridge of voltage and current source inverters. Some the distinctive attributes of the impedance source inverter when employed in power conditioning is the ability to function either as buck inverter, boost inverter or buck-boost inverter, immunity to the negative effects of EMIs, useful for renewable energy applications due to its wide peak to peak power functionality. Despite the numerous advantages of ZSI over VSI/CSI, the size, weight and cost of ZSI is of great concern and this is caused by the size of the impedance network components. The switched boost inverter topology which possesses all the advantages of the traditional impedance source inverter (ZSI) but with reduced passive component count and an increase in the number of required active components. Simulation and mathematical analysis of the switched boost inverter topology is carried out the environs of PSCAD software and results produced. Two types of PWM control techniques are utilized in the control of the SBI topology during simulation.

Keywords: Z source inverter; boost factor; switched boost inverter; PWM; buck inverter

ÖZET

Z kaynağı inverteri ya da direnç kaynak inverteri, voltaj ve akım kaynağı inverterlerinin inverter köprüsü ve gücü arasında simetrik özellikleri olan kapasitör ve endüktörden oluşan direnç ağından elde edilir. Güç düzenleyici üniteler uygulandığı zaman oluşan direnç kaynağı inverterinin önemli özelliklerinden bazıları buck inverter, boost inverter veya buck-boost inverter gibi işleyebilme yeteneği EMI'lerin olumsuz etkilerine karşı bağışıklığı ve geniş zirveden zirveye güç işlevselliğine bağlı yenilenebilir enerji uygulamaları için kullanışlı olmalarıdır. VSI/CSI'ye göre ZSI'nin birçok avantajı olmasına rağmen, ZSI'nin boyutu, ağırlığı ve fiyatı büyük bir problem ve bu direnç ağı bileşenlerinden kaynaklanmaktadır. Kurmalı boost inverter topolojisi geleneksel direnç ağı inverterinin (ZSI) tüm avantajlarını, indirgenmiş pasif bileşen ve artırılmış gerekli aktif bileşen miktarını kapsamaktadır. Kurmalı itiş inverter topolojisinin simülasyon ve matematiksel analizi PSCAD yazılımı kullanılarak yapılmıştır ve sonuçlar elde edilmiştir. PWM kontrol tekniklerinin iki türü, simülasyon süresince SBI topoloji kontrolüyle kullanılmıştır.

Anahtar kelimeler: Z kaynağı inverteri; boost Faktörü; kurmalı boost inverteri; PWM; buck inverteri

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LIST OF ABBREVIATIONS

VSI	Voltage Source Inverter
FACTS	Flexible alternating current transmission system
CSI	Current Source Inverter
ZSI	Impedance Source Network
BZSI	Bidirectional Impedance Source Network
IZSI	Improved Z Source Inverter
PV	Photovoltaic Systems
HPZSI	High Performance Impedance Source Network
EMI	Electromagnetic Interference
FLZSI	Four Leg Z Source Inverter
DuZSI	Dual Z Source Inverter
NPZSI	Neutral Point Z Source Inverter
ZSID	Z Source Inverter Diode
ZSIS	Z Source Inverter Switch
QZSI	Quasi-Z-Source Inverter
SLQZSI	Switched Inductor Quasi-Z-Source Inverter
DGC	Doubly Grounded Circuits
HFTI	High Frequency Transformer Isolation
PWM	Pulse Width Modulation
CB	Circuit Breakers
UC	Ultra-Capacitor
CFSI	Current Fed Switched Inverter
KVL	Kirchhoff Voltage Law
RL	Resistive-Inductive
SBI	Impedance Based Inverter
MC	Matrix Converters
PSC	Phase Shift Control
CIEM	Complete Inductor Energy-supplying Mode
IEM	Incomplete Inductor Energy-supplying Mode
ZPCM	Zero-crossing Input Current Mode
NPCM	Non-zero-crossing Input Current Mode
ZICM	Zero-crossing Inductor Current Mode
NICM	Non-zero-crossing Inductor Current Mode
DC	Direct Current
AC	Alternating Current

CHAPTER 1

INTRODUCTION

1.1 General Concept

The process of changing dc voltage/power to ac voltage/power is known as inversion; this process is realized by the use of principal device called an inverter. The first inverter is commonly known as the conventional 2-level inverter which is a voltage source inverter- VSI. The function of the conventional 2-level inverter is to utilize a fixed source voltage to provide changeable frequency/voltage at the inverter output for use by varied applications such as adjustable speed drive etc. inverters are classified into two groups from the input/source point of view and these categories are current source inverter CSI and voltage source inverter VSI.

A voltage source inverter is an inverter in which the source voltage (dc) amplitude is constant and it is not affected by the current of the load. Basically the output voltage is dependent on the characteristics of the inverter and the current value is dependent on the type of load. Voltage source inverters have wide areas of applications because the input is voltage source and it is suitable for many applications which require voltage source as the input. Variable or adjustable speed drives and FACTS devices are some major the major applications of voltage source inverters. Although VSI can be applied high power system, it is most suitable in medium power applications because they are able to generate output voltage with very high quality waveforms. The dc input voltage of a voltage source inverter can be any of the following; capacitor, battery, rectifier circuit source, fuel cell, PV systems etc. in the case of multilevel inverters where multiple dc source are required, a combination of the above sources can be utilized. A common type of VSI circuit is the single phase H Bridge inverter with four switches each connected with an anti-parallel diode, this switch topology allows for current flow in bi-direction and unidirectional voltage flow.

The voltage source inverter also known as voltage source converter (when used for both inversion and rectifying purposes) has wide areas of applications but it's fraught with many limitations such:

It's a buck or step down inverter that's the output voltage is always less than the input voltage unless a buck-boost converter is applied. When used as a rectifier, it's a boost rectifier circuit.

- a. Applications of buck-boost converter in VSI topology increases the cost of the unit, reduces the efficiency of the system and complicated control technique is introduced.
- b. Shoot through property is absent in VSI or CSI hence EMIs immunity is absent

c. Inductor – capacitor filter is required to reduce power systems noises.

On the other hand, the current source inverter or converter is achieved by putting a large inductor in series with the dc source. Just as in the case of voltage source inverter, the dc input voltage of a current source inverter can be any of the following; capacitor, battery, rectifier circuit source, fuel cell, PV system. Figure 1.1 and Figure 1.2 show the circuit diagram of voltage and current source inverters. These topologies are similar but have differences in the type of source voltage and the type of switches used. The difference in switch types is because in the VSI; bidirectional current flow and unidirectional voltage flow is required whilst in the CSI; bidirectional voltage flow is required and unidirectional current flow is required. In the case of CSI, several switch types can be utilized to achieve bidirectional voltage flow and unidirectional current flow, some examples of such switches are: SCR, series connection of IGBT and diode, GTO, SCR. Some limitations of CSI are:

- a. The current source inverter is a boost inverter and when applied as rectifier, it's a buck rectifier circuit.
- b. Buck dc converters are required to reduce the cost hence, cost of system and efficiency increases and reduces respectively.
- c. Open circuit on a load side is a big problem when preventive measures are not taken and reverse voltage path should be provide or blocked.

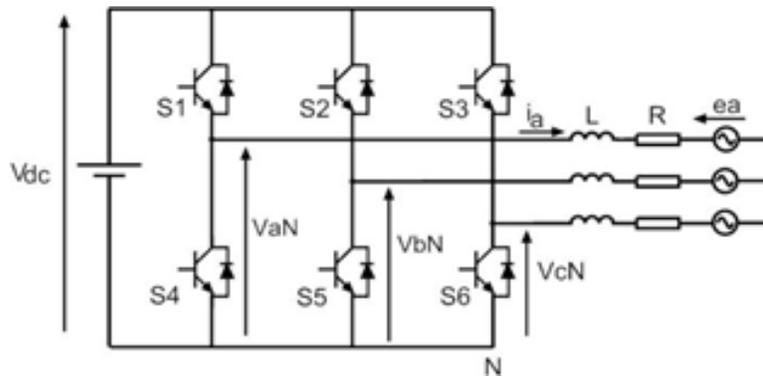


Figure 1.1: Voltage source inverter

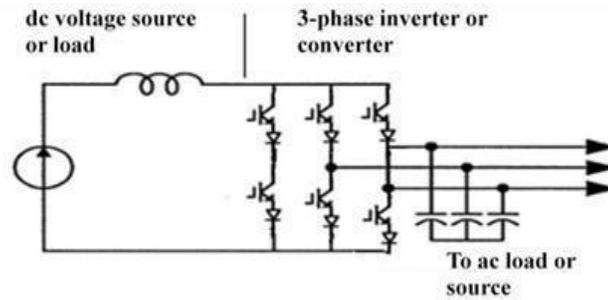


Figure 1.2: Current source inverter

1.2 Thesis Problem

Voltage source inverters and current source inverters have revolutionized power conditioning for industrial applications in varied areas of the engineering fields. Also they have contributed immensely to development of inverters most especially multilevel inverters. The quality of their output waveforms is good and they have wide range of applications. Although VSI and CSI are very useful in industrial applications, they are still bedeviled some drawbacks which when eliminated can improve their efficiency.

The major limitations of these converters have enumerated in the introduction section of this chapter. The introduction of Z source or impedance networks into VSI and CSI solves the problems of buck or boost quality depending on the topology and also shoot through property provides immunity to the effects of EMIs. The conventional Z source based inverter solves major drawbacks of VSI and CSI but they also introduce some limitations such as increased cost and size hence they are not appropriate for use in low power systems when they following factors are off great concern; cost, weight and size.

1.3 The aim of Thesis

The primary aim of this thesis is to provide solutions to the disadvantages of voltage source inverter, current source and conventional Z source based inverters in application areas where size, weight and cost are major factors for the system designing. This is achieved by introducing a novel impedance based inverter called SBI; switched Boost inverter. This inverter has the advantage of the conventional Z source inverter plus its own advantages such as reduced passive

Component count but increased active component count hence better control of the circuit. Analysis of the proposed inverter will be carried in two phases; a. steady state and b. small signal.

1.4 The importance of Thesis

It's evident that power conditioning units such as power electronic converters have come to stay are contributing immensely to development of power systems. They are used in almost every sphere of human endeavor. Some notable application areas of power electronics are: transportation, space technology, utility systems, industrial settings and home appliances.

The efficient and effective use of power electronic converters to produce good quality waveforms as desired by loads is the importance of this research. This will result in minimizing losses, increase efficiency thereby driven down the cost of power for the consumer, efficient use of power source will increase the lifespan of source and also reduce monopoly in marketing.

1.5 Limitation of study

Even though this research was conducted with outermost care, the possibilities of shortcomings and limitations are unavoidable. First the research was conducted using EMTDC/PSCAD software hence the ability to control the research is limited to the mathematical modeling of the software. Although research based simulation results have become an acceptable standard in academia, the disadvantage of not having experimental results due cost of components, proper practical knowledge and conducive laboratory cannot be ignored.

1.6 Overview of the Thesis

The structure of this thesis is as follows:

Chapter 1: Introduction. This chapter is made of introduction, Thesis Problem, The aim of Thesis, The important of Thesis and overview of the thesis.

Chapter 2: Literature Review of Z Source Inverters Chapter 3: Power Circuit Description and Simulation Results Chapter 4: Conclusion and Future Works

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The goal of this literature review is to review previously published papers on Z-Source inverters popularly known as ZSI. The review will consider the various topologies that have been developed after the introduction of the main ZSI topology, their applications and usefulness in industry when compared to other inverter topologies; the various control methodologies which are applicable to ZSI and other factors which makes the ZSI a suitable inverter for power electronics applications.

2.2 Z source inverter

The impedance structure or Z source system was basically developed to overcome the limitations associated with conventional voltage or current source converters/inverters, dc-dc converters and bidirectional and unidirectional converters. The main attraction of the impedance structure lies in its flexible source characteristics and the ability to increase output voltage from 0 to infinity theoretically. Different topologies of Z source structure have developed to increase the voltage gain or boosting factor of the converter and also limit stress imposed on the semiconductor switches while maintaining the basic structure of Z source system. These topologies are classified according to the following categories listed below and the magnetically coupled type seems promising because least number of electronic components are used and also higher voltage gain is achieved using only short ratio of duty cycle during the short-through state .

- Switched device technique.
- Cascading methodology.
- Magnetically coupled methodology.

The authors in (Xu, P., Zhang, X., Zhang, C. W., Cao, R. X., & Chang, L, 2006) studies the application of ZSI in photovoltaic systems; the disadvantages of voltage source inverters such as; random fluctuations in generated photovoltaic power means that buck or boost or a combination of the two; buck-boost converter is required for injected grid power stability which increases the cost of the system and also reduces the efficiency of the system, shoot through scheme is not applicable but dead-time control method is rather employed and this results in distorted output current waveforms. Other disadvantage reported in (Peng, F. Z., Yuan, X., Fang, X., & Qian, Z, 2003) is an output filter is required

to produce quality output power which also leads to more losses. All the problems enumerated above concerning the VSI are solved by the introduction of the ZSI topology. The Z source inverter or converter for general forms of power conversion is the utilization of an impedance network between the voltage source and the main converter circuitry. The impedance network is made up of two passive components; inductors and capacitors, other improved impedance network reduces the number of passive components and applies active component instead. In photovoltaic applications, a diode is connected in series with the panels to protect the panels from reverse current from the load because the PV panels are not energy storage systems i.e. unable to store dc voltage. The ZSI topology was developed by (Peng, F. Z., Yuan, X., Fang, X., & Qian, Z, 2003) in 2003 and after since several improved ZSI circuitry have been developed. Figure 2.1 shows the main ZSI developed by (Peng, F. Z., Yuan, X., Fang, X., & Qian, Z, 2003). The main advantage of the ZSI over other inverter topologies such as VSI or CSI is the shoot through characteristics which when controlled properly can increase or decrease the magnitude of the input voltage for both ac and dc voltages respectively. The shoot through attribute of the ZSI eliminates the need for the dead time hence the inverter output current is devoid of distortions increasing the quality of the produced power (Xu, P., Zhang, X., Zhang, C. W., Cao, R. X., & Chang, L, 2006).

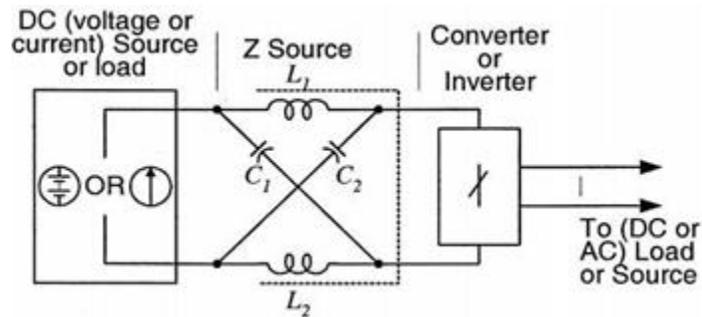


Figure 2.1: ZSI general structure

Basic analysis of ZSI when connected to PV system is done in (Xu, X. Zhang, et al, 2006) which will be grid tied at the converter output. This analysis is achieved by designing a suitable control scheme for the setup, the ZSI capacitor voltage and grid current is regulated by controlling the modulation index, the shoot through property is regulates the PV output voltage. Figure 2.2 shows the ZSI based photovoltaic system which includes the control scheme. Certain assumptions are made for the successful operation of the ZSI.

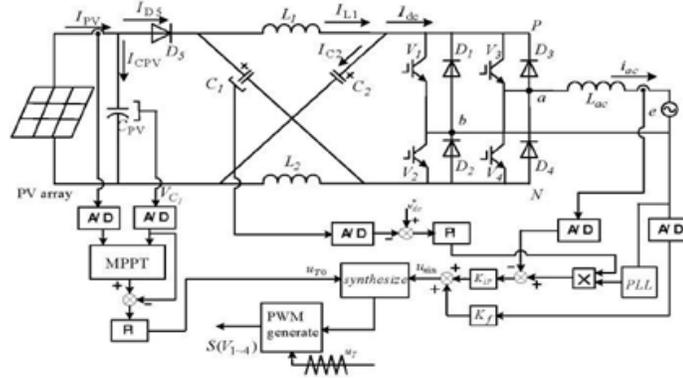


Figure 2.2: ZSI circuit and control scheme with PV

The magnitude of the two inductors L_1 and L_2 are equal and the magnitude of the two capacitors C_1 and C_2 are equal. Thus $L_1 = L_2 = L$ and $C_1 = C_2 = C$. with these assumptions made, the voltage across the inductor and capacitors are given by V_L and V_C respectively.

$$V_L = V_{L1} = V_{L2} \text{ and } V_C = V_{C1} = V_{C2} \dots \dots \dots (2.1)$$

$$V_C = \frac{1-D}{1-2D}V_d, D = \frac{T_0}{T} \dots \dots \dots (2.2)$$

$$\begin{cases} V_o = V_C = BV_d & \text{For non shoot through condition} \\ V_o = 0 & \text{For shoot through condition} \end{cases} \dots \dots \dots (2.3)$$

Two states of operations exist in the ZSI principles of operation; shoot through and non-shoot through. The circuitry of the two states of operations is shown in figure 2.3a and 2.3b. The shoot through state is shown in figure 2.3a. The following mathematical statements are valid from KVL and KCL point of view;

$$\begin{cases} V_L = V_C \\ V_d = 2V_C > V_{PV} \\ V_{PN} = 0 \end{cases} \dots \dots \dots (2.4)$$

The inverter input voltage V_{PN} which is also the impedance network output voltage is zero because switches on the same leg are put on to derive the shoot-through characteristics which results in short circuit of the inverter switches.

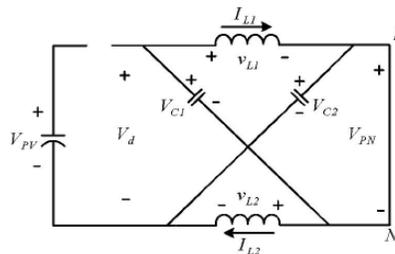


Figure 2.3 a: ZSI shoot-through state

In the shoot-through stage, diode D5 is forward biased hence the impedance network output voltage doubles as the inverter input voltage which is actually a current source input V_{PN} , again applying KVL and KCL will produce the following mathematical statements;

$$\begin{cases} V_d = V_{PV} = V_L + V_C \\ V_{PN} = V_C - V_L = 2V_C - V_{PV} \end{cases} \dots\dots\dots (2.5)$$

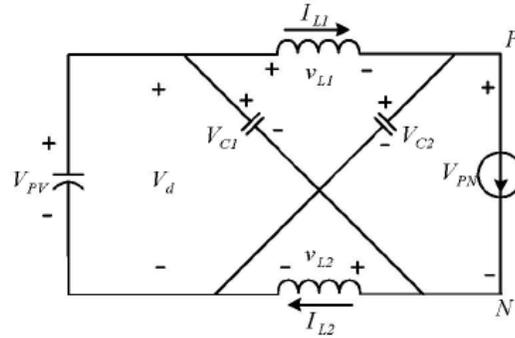


Figure 2.3 b: ZSI non shoot-through state

The capacitor voltage plays a crucial role in determining the stability and efficiency of the ZSI; the quality of the output voltage is linked to the modulation which is affected when unreasonably low capacitor voltage is applied while on the other hand semiconductor switches will be damaged when excessively high capacitor voltage is applied. These problems require the stabilization and control of the capacitor voltage which can be achieved by outer loop regulation of the capacitor voltage. Controlling the ac grid currents control the value of the capacitor voltage and this is explained by the equations below:

The power balance equation is given by (2.4) where I_{dc} and I_{ac} represent impedance network output current and grid ac current respectively. s is the Laplace operator and V_C capacitor voltage

$$V_C I_{dc} = E I_{ac} \dots\dots\dots (2.6)$$

$$I_{dc} = \frac{E}{V_C} I_{ac} \dots\dots\dots (2.7)$$

$$V_C = \frac{I_C}{sC} = \frac{I_L - I_{dc}}{sC} \dots\dots\dots (2.8)$$

2.3 Z Source Matrix Converter

Extensive commercial application of matrix converters (MC) has been very limited over the years even though comprehensive research has been conducted over the previous two decades and this can be attributed to extensive semiconductor switch count, limited voltage gain, complicated modulation strategies. To reduce the high number of switches required, the indirect matrix converter also known as sparse or ultra-sparse matrix converters were developed (Kolar, J. W et al, 2007). To improve the voltage gain capabilities of the MC, different types of topologies and control techniques have been proposed and

the ZSI conceptualization is better than the others in producing output power with superior quality and a dependable inverter/converter (Karaman, E et al, 2014). The greater numbers of research on MC have been geared towards the control techniques, developing newer topologies and PWM utilizations (Garcia-Vite, P. M et al., 2013). Nevertheless, a few ZSMC papers have been published, in (Siwakoti, Y. P., Blaabjerg, F., & Loh, P. C.2016) the idea of impedance network is applied to indirect MC where their characteristics and principles of operations are analyzed, also in (Nguyen, M. K., Lim, Y. C., & Cho, G. B. 2011) sparse MC with impedance network is applied to grid tied wind farm. The presented topology in (Karaman, E., Farasat, M., & Trzynadlowski, A. M. 2014) is derived from cascaded Z source MC and it's known as series Z source MC. The advantage of series Z source MC over cascaded Z source MC is that inrush current is limited, capacitor voltages are reduced and still maintaining the boosting factor of the latter. Figure 4a and 4b represents cascaded Z source MC and series Z source MC respectively while figure 5a and 5b shows the non-shoot through and shoot through properties of series Z source MC.

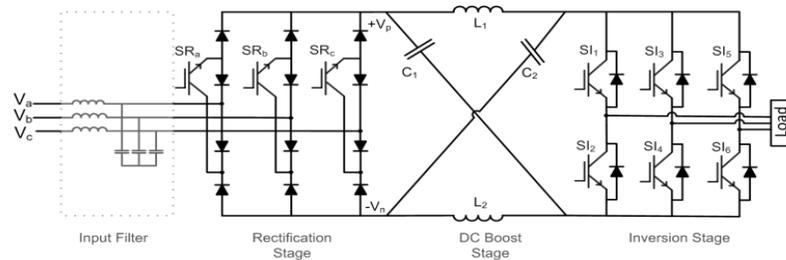


Figure 2.4 a: Z source MC

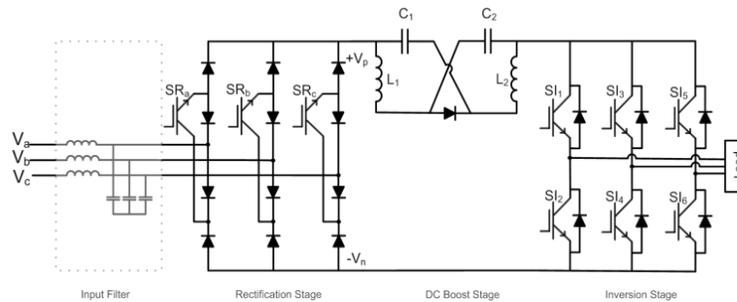


Figure 2.4 b: Series Z source MC

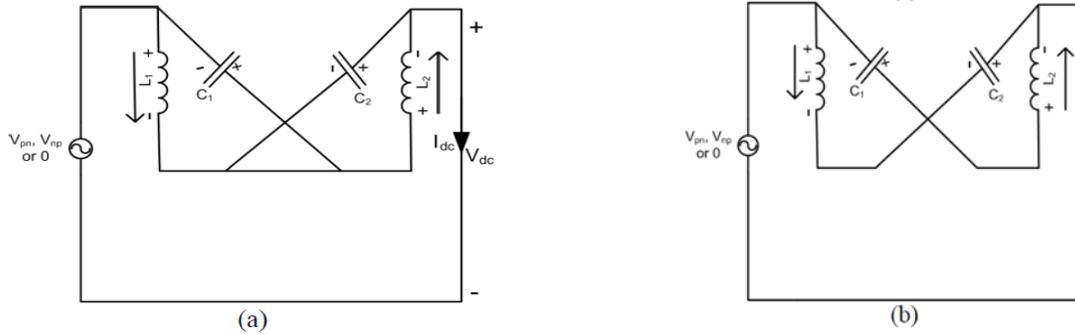


Figure 2.5: a) Series Z source MC non-shoot-through b) Series Z source MC shoot-through

The principle of operation of the above MC topology is similar to other ZSI, the difference being that a rectifier is used to change the ac source voltage into dc before being feed into the impedance network. All mathematical assumptions concerning the capacitor and inductor values remain the same. For the series Z source MC in shoot-through state, the inductor voltage is given by:

$$V_L = V_C + V_V \dots \dots \dots (2.9)$$

Where V_V is the rectifier output voltage; V_{np} , 0, V_{pn} and the inductor voltage for non-shoot through state is given by:

$$V_L = V_C \dots \dots \dots (2.10)$$

The boost factor B, for both Z source MC and Series Z source MC is given by (11) where d_{sh-th} is duty ratio for the shoot through state:

$$B = \frac{1}{1-2d_{sh-th}} \dots \dots \dots (2.11)$$

Two pulse width modulation strategies namely space vector inversion and space vector rectification are the control mechanism employed to control Z source MC and Series Z source MC. The successful realization of the Z source network employed in any inverter is heavily dependent on correct passive component selection for the impedance network. Selection of the values of inductor and capacitor are based on ripple current and ripple voltage and capacitor current respectively.

2.4 MCZS

The main objective of magnetically coupled Z source MCZS or impedance network is to utilize less number of passive components and still produce higher modulation index and boosting factor or voltage gain also MCZS components experience minor stress when compared to other topologies. Examples of MCZS topologies employing two windings only are:

- 1 Γ -Z-source LCCTZ-source
- 2 Flipped- Γ -Z-source quasi-LCCT-Z-source
- 3 T-source High-frequency transformer-isolated Z-source
- 4 *Trans-Z-source TZ-source*

The magnetically coupled based networks in which input currents are pulled continuously are better than systems which draws discontinuous input currents; examples are of such networks are presented in (Adamowicz, M., Strzelecki, R., Peng, F. Z., Guzinski, J., & Rub, H. A. 2011, August). Constraints occur when the networks are connected to fuel cells or PV system.

Different methods have been reported to smoothen the current drawn from the source current in various literatures (Liu, C., & Lai, J. S. 2007, Karaman, E et al, 2014); this is achieved by connecting extra capacitor and inductor to the circuit. The changes which are made to the various magnetically coupled Z source converters increases the stress levels of the components in the circuits but in most cases they are ignored (Siwakoti, Y. P et al, 2016). A new topology which seeks to achieve the same results of smoothing input current is realize by the addition of only a capacitor; accurate predetermined capacitance ratio of the capacitors can lead to intake of continuous source current but parasitic resistance and incorrect capacitance ratio will several affect smooth source current, during startups huge inrush current is drawn and parasitic capacitance and inductance causes oscillation at the input (Adamowicz, M et al, 2011). The problems numerated above are solved by three new types of magnetically coupled Z source converters namely:

Quasi-Y-source, Quasi- Γ -Z-source, Quasi-T-source or quasi-trans-Z-source networks

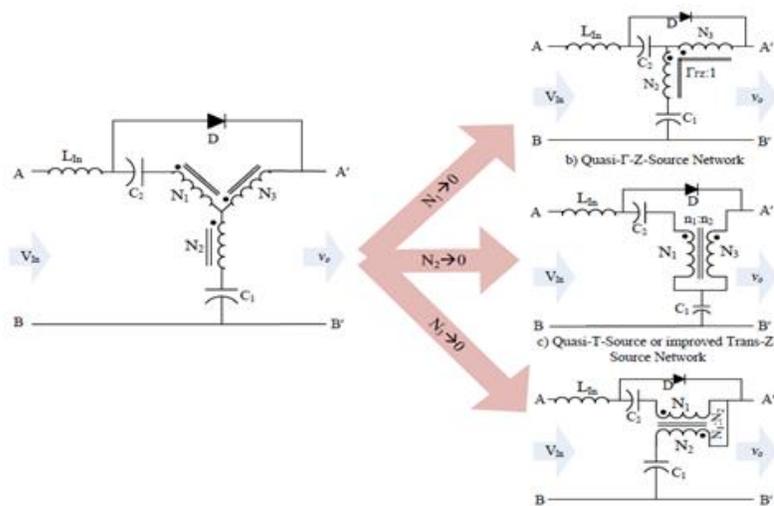


Figure 2.6: Q-Y- Source networks

2.5 Quasi ZSI

A novel quasi ZSI has been presented in (Ge, B et al, 2014) which incorporate the existing advantages of ZSI together with the proposed topology. Due to the disadvantage of double stage conversion required for conventional converters, the ZSI is chosen to overcome the cost and losses of the traditional converter. The ZSI has several advantages in PV applications such as the ability to perform under large range of PV voltage variations with limited number of components at heavily reduced cost. The quasi ZSI is an improvement of the Z source converter and has added advantages which makes suitable for photovoltaic systems applications; a) continuous current is drawn from the photovoltaic panel, extra capacitors as filters are not required b) switching ripples are reduced as c) capacitor ratings are low which means reduced cost of the system. The proposed topology in (Ge, B et al, 2014) incorporates energy storage systems such as a battery to the qZSI circuitry. Due to unreliability nature of the output power from photovoltaic structure, the energy storage systems act as buffer to solve the problems of fluctuations and intermittency. Figure 2.7 shows the previous qZSI with energy storage system and figure 2.8 shows the proposed novel structures which are both applied in PV system.

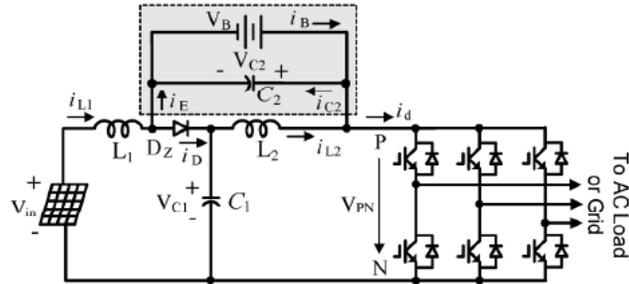


Figure 2.7: Previous ESS qZSI

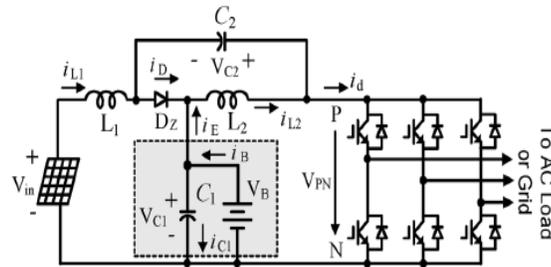


Figure 2.8: Proposed ESS qZSI

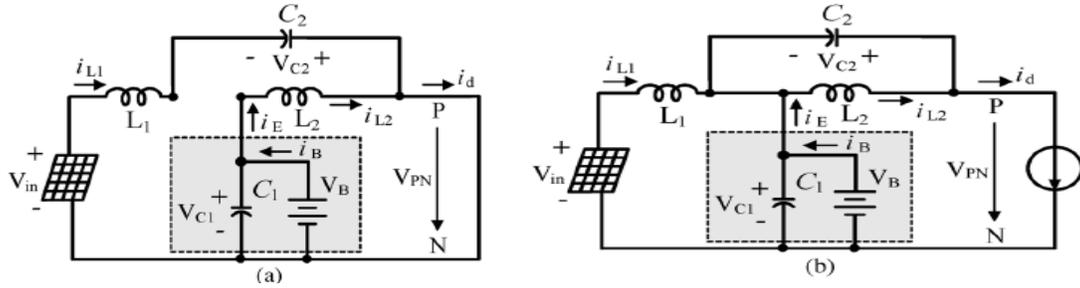


Figure 2.9: a) Shoot through state b) Non-shoot through state

The purpose of the battery in Figure 2.7 which is in parallel connection with capacitor C_2 is to balance the power of the source i.e. photovoltaic system and grid connected power. Duty ratio of the shoot through state is applied to maximize the power at the source and to manage the charging of the battery, power-flow regulation was proposed in (Sun, D et al, 2011). This methodology has demerit, which is at peak voltage there's loss of continuous voltage flow. There is discontinuous conduction mode in figure 2.7 which limits the flow of battery power hence the output of the inverter is adversely affected. The solution to this problem is presented in (Sun, D et al, 2011),(Li, F et al, 2011) where the diode is replaced with an active switch.

Figure 2.8 represents the proposed qZSI with energy storage unit and this topology has three power sources in its circuitry; the PV or input power P_V , the output or grid power P_G and the ESS power P_E , controlling two of the power sources will produce the desired power in the last source, i.e.

$$P_V - P_G + P_E = 0 \dots \dots \dots (2.12)$$

The power from the photovoltaic system is unidirectional but the power from the energy storage system is bidirectional; when its charging the power is positive and negative during discharging period. The output power is positive when the grid/load is consuming power from the inverter and negative when the load is delivering power to the energy storage unit. Just like in the case of the ZSI, two states or modes of operation are available in the ESS based qZSI system; the shoot through state and non-shoot through state. The shoot through state is derived when all switches on the same phase or leg are simultaneously put on and this results in reverse biased current flowing to the diode hence the diode goes off (non-conducting). Figure 2.9a show the shoot through state and the following equation are derived for this period.

$$C \frac{dV_{C1}}{dt} = i_B - i_{L2} \dots \dots \dots (2.13)$$

$$C \frac{dV_{C2}}{dt} = -i_{L2} \dots \dots \dots (2.14)$$

$$L \frac{di_{L1}}{dt} = V_{in} + V_{C2} \dots \dots \dots (2.15)$$

$$L \frac{di_{L2}}{dt} = V_{C1} \dots\dots\dots (2.16)$$

In the non-shoot through state, the inverter is operated just like any three phase inverter with six states which are active and conventional zero states of two. Figure 2.9b represents non-shoot through state of figure 2.8. Also the following equations are valid for the non-shoot through condition.

$$C \frac{dV_{C1}}{dt} = i_B + i_{L1} - i_d \dots\dots\dots (2.17)$$

$$C \frac{dV_{C1}}{dt} = i_{L2} - i_d \dots\dots\dots (2.18)$$

$$L \frac{di_{L1}}{dt} = V_{in} - V_{C1} \dots\dots\dots (2.19)$$

$$L \frac{di_{L1}}{dt} = - V_{C2} \dots\dots\dots (2.20)$$

In (Chen, X., Fu, Q., & Infield, D. G. 2009) a photovoltaic based ZSI power conditioning system is presented. The paper makes use of the existing basic ZSI topology to design the power condition unit because of the wide application areas that can be achieved when impedance network is used; this is a plus when compared to the traditional converter. Simulation is performed using matlab software and the results indicate that output voltage boosting and maximum power tracking is achievable with the Z source inverter. The harmonic content in the system can be reduced drastically and also used as reactive power compensation in utility where it's needed. The mathematical equations are similar to that basic Z source inverter but MPPT algorithm was introduced here for power point tracking. Shoot through and non-shoot through mythologies were also applied, Figure 2.10. Shows the harmonic contents of the current before compensation and after compensation.

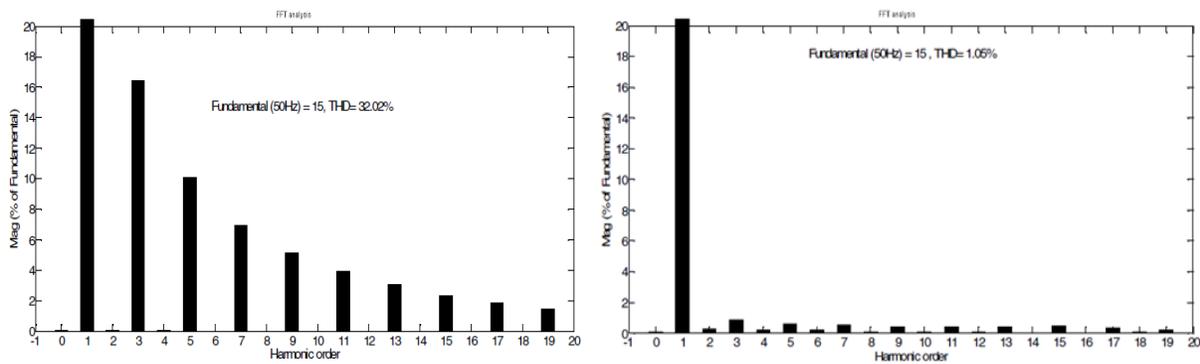


Figure 2.10: Harmonics content before and after compensation

2.6 Impedance Source Rectifier

Similarly application of Z source inverter for offshore wind farm integration to utility grids has been presented in (Shahinpour et al, 2014). In this application the Z source converter is used as rectifier since

the voltage from the wind farm is ac voltage and it's connected to High voltage direct current transmission system. Again the impedance network is composed of two inductors and two capacitors and is connected between the load and the rectifier circuit as shown in Figure 2.11. Two modes of operation exist, the shoot through and the non-shoot through. The main advantage of this structure is voltage gain boosting capabilities and the ability to provide any power factor irrespective of the load.

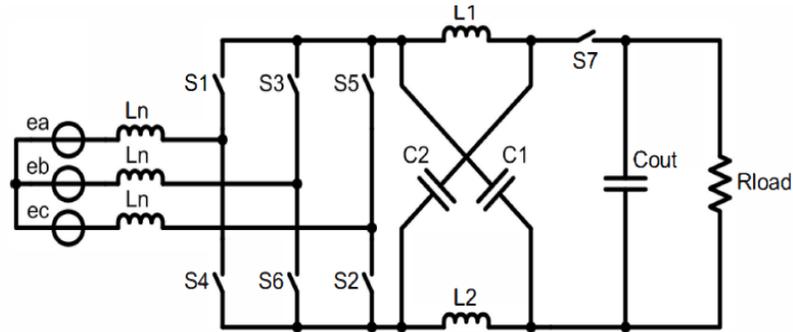


Figure 2.11: Impedance source rectifier

Three types of control techniques are presented in (Shahinpour et al, 2014), each of the three control methods are applied in simulation and the results (graph) are shown, and the three control methods are:

- [89] Simple boost control
- [90] Maximum or peak boost control
- [91] Maximum or peak constant boost control

The boost factor f and voltage gain for the above control methods in ascending are presented in the following equations:

$$B = 2M - 1, G = \frac{2B}{M} \dots \dots \dots (2.21)$$

$$B = \frac{3\sqrt{3M} - \pi}{\pi}, M = \frac{\pi(B+1)}{3\sqrt{3B}}, \dots \dots \dots (2.22)$$

2.7 Z-H Buck Converter

A new type of Z source topology is presented in (Ahmadzadeh, T et al, 2018) which is known as Z-H buck converter. This structure combines the H bridge structure with impedance network but with reduced component count in the impedance structure. Figure 2.12. Shows the Z H buck converter system. The type of switches used depends on the application type; when the converter is used as chopper, inverter or rectifier, unidirectional switches are employed and bidirectional switches used when the converter is applied as a cycloconverter. Two duty cycles mode of operations exist; $D = (0, 0.5)$ and $D = (0.5, 1)$. The main purpose of this topology is step down the input voltage to a desirable level. Two

operating states exist in the operating zone of the duty cycle D , inductor current charging state and inductor current discharging state. In the inductor (L_1 and L_2) current charging mode, two switches S_2 and S_3 are switched on to conduct, in the time period of T_0 and during the inductor (L_1 and L_2) current discharging mode switches S_1 and S_4 are switched on to conduct during T_1 period. The equivalent circuits of the two modes of operations are shown in Figure 2.13. a and b respectively. Phase shift method is used in ripple reduction (Ahmadzadeh, T., & Babaei, E. 2015)

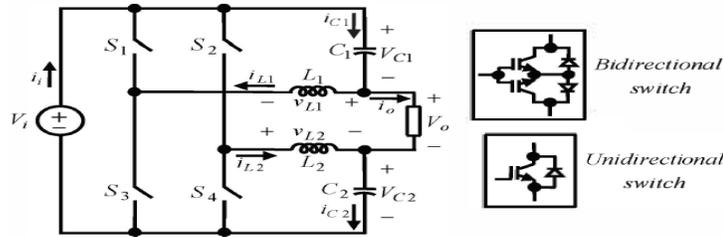


Figure 2.12: Z H buck converter

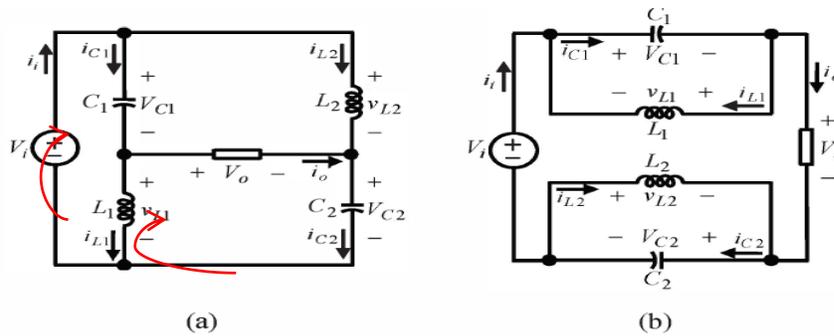


Figure 2.13: Period of operation T_0 and T_1

For the purpose of symmetry, the passive components have the same magnitude of values i.e. L_1 equals L_2 and C_1 equals C_2 . The following mathematical equations are valid for when Kirchoff's voltage law is applied to figure 2.13, first let's consider the period T_0 :

The voltage across the inductor V_L :

$$V_L = V_i - V_C \dots \dots \dots (2.23)$$

And the output voltage V_o :

$$V_o = V_i - 2V_C \dots \dots \dots (2.24)$$

Again using the symmetry analogy for the passive components and writing the Kirchoff's voltage law for T_1 period of figure 13:

The voltage across the inductor V_L :

$$V_L = - V_C \dots \dots \dots (2.25)$$

And the output voltage V_o :

$$V_o = V_i - 2V_C \dots \dots \dots (2.26)$$

Using voltage balance law, we have:

$$(V_i - V_C)T_o + (-V_C)T_1 = 0 \dots \dots \dots (2.27)$$

The average voltage across the capacitor:

$$V_C = \frac{T_o}{T_o + T_1} V_i = \frac{T_o}{T} = DV_i \dots \dots \dots (2.28)$$

$$V_C = DV_i \geq 0 \text{ for } D = (0, 0.5) \dots \dots \dots (2.29)$$

$$V_C = DV_i \geq 0 \text{ for } D = (0.5, 1) \dots \dots \dots (2.30)$$

An innovative phase shift control (PSC) method has been proposed in (Pilehvar, M. S., & Mardaneh, M., 2014), this method is applied in harmonics elimination in an impedance H bridge inverter. Although PSC is not new; a new or improved form of PSC method having four states of shoot through is proposed in this paper. The main benefit of this novel method is the elimination or reduction of harmonics concurrently, also when this new method is compared to conventional PSC as applied in H bridge inverters; this novel PSC method produces lower amplitude of low order harmonics than the conventional PSC.

2.8 ZS-HB Converter

Figure 2.14. Shows the combination of the impedance source and the H bridge inverter topology (ZS-HB converter) with the modes of operations; shoot through state and non-shoot through state.

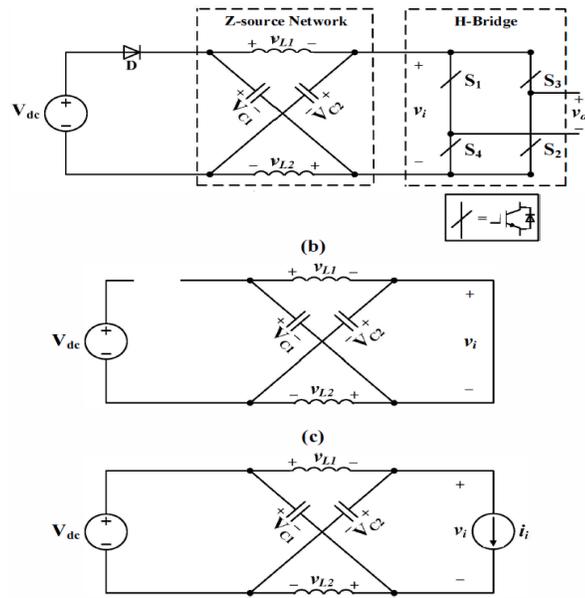


Figure 2.14: a) ZS-HB converter b) shoot through state c) non-shoot through state

Since the basic operation of the impedance source topology is well presented, I will proceed to the output

voltage of the impedance network which doubles as the input voltage of the H bridge inverter. B is known as boost factor and Dis the duty ratio.

$$V_i = 2V_C - V_{dc} = \frac{T_{SW}}{T_1 - T_0} V_{dc} = B V_{dc} \dots \dots \dots (2.31)$$

$$B = \frac{T_{SW}}{T_{nsh} - T_{sh}} = \frac{1}{1 - 2\left(\frac{T_{sh}}{T_{SW}}\right)} = \frac{1}{1 - 2D} \geq 1 \dots \dots \dots (2.32)$$

Three modes of switching patterns exist for the shoot through state; $\beta_{sh} < \alpha$, $\beta_{sh} = \alpha$, $\beta_{sh} > \alpha$, and these mode are represented in Figure 2.15a, 15b and 15c respectively.

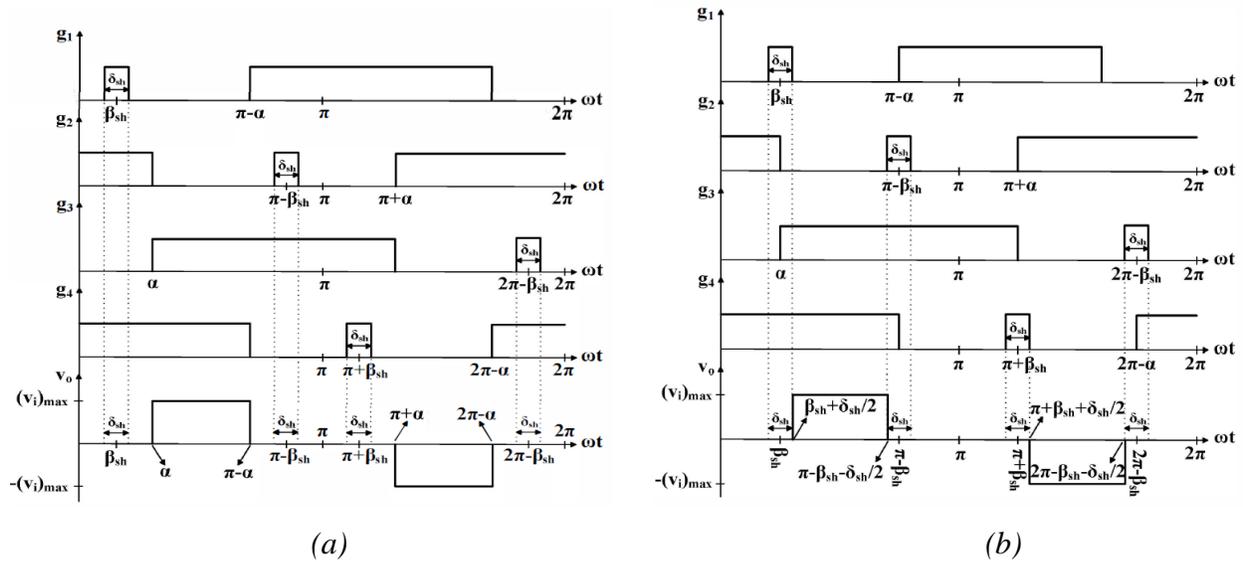


Figure 2.15: a) $\beta_{sh} < \alpha$ b) $\beta_{sh} = \alpha$,

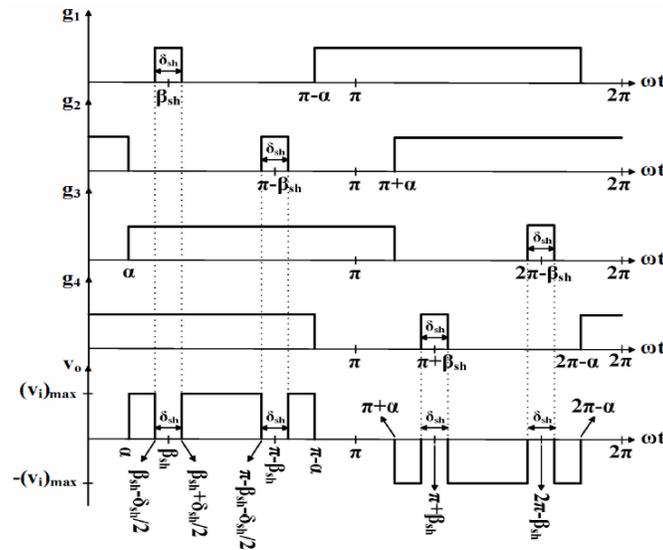
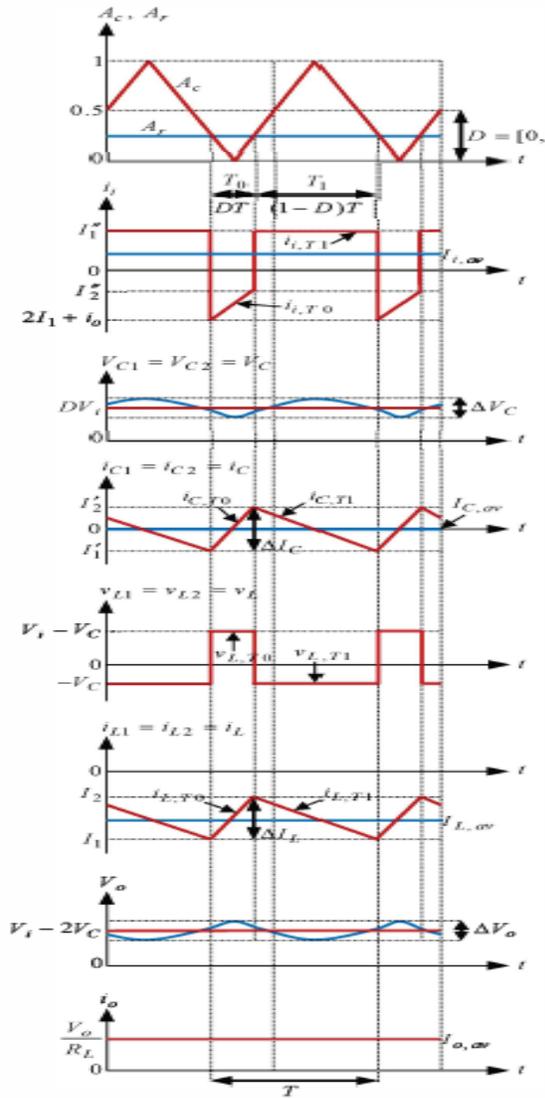
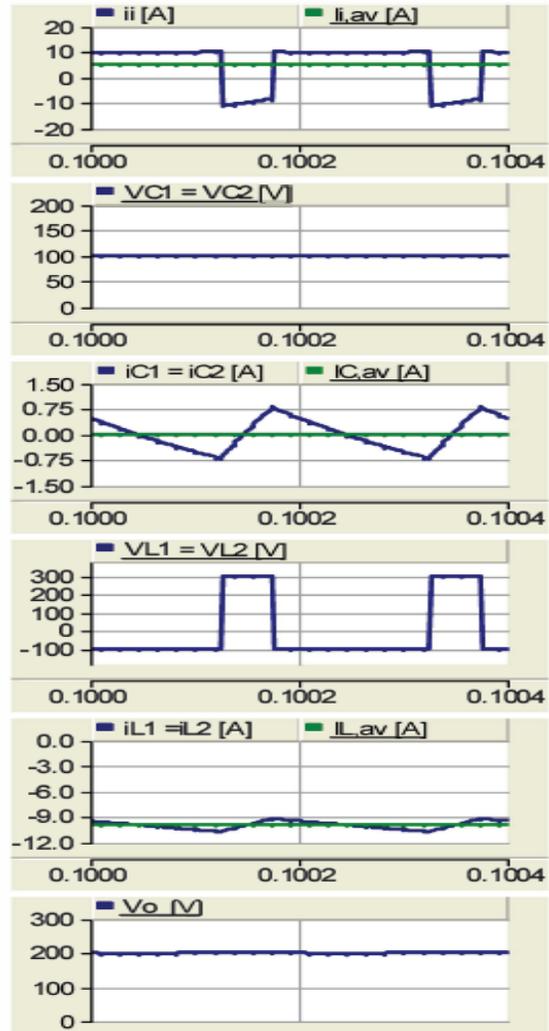


Figure 2.15: c) $\beta_{sh} > \alpha$



(a)



(b)

Figure 2.16: a) I-V waveform b) Experimental I-V waveforms

Even though Z source inverters have several advantages when compared to the traditional voltage or source inverters, their applications in industry is limited. Conventional voltage or current source inverters have much industrial application than Z source inverter. This limitation of the ZSI in industrial application can be traced to but not limited to design layout, long frequency loop dc voltage bus clamping which are investigated in (Cha, H., Li, Y., & Peng, F. Z., 2016) by adding clamping diode to the circuit to reduce the frequency loop and circuit modification by intuition. So the useful solid structure of the Z source inverter together with voltage clamping method for MCSI is simulated and experimental results produce.

2.9 Trans and Quasi Topologies

The following procedures describe how the quasi Z source inverter is obtained from the basic impedance network known as Z source inverter. Figure 2.17 shows the ZSI and Figure 2.18 shows the quasi Z source inverter. These two inverter topologies are similar but with different passive component arrangement. The qZSI is obtained from ZSI which is the foundation of all Z source topologies. Capacitor C_2 in Figure 2.17 shares the same ground with the source voltage which means that it can be moved to the top of the source as in Figure 2.18. Once that is done, inductor L_2 of Figure 2.17 is in series with the source voltage so it can be arranged as in Figure 2.18. The position of L_1 and L_2 do not matter because in the case of symmetry, the values of L_1 and L_2 are equal so is it the case of the capacitors. The main advantage of qZSI over ZSI is the continuous input current from the source because inductor L_1 is connected in series to source voltage and the simple layout of the circuit. However the voltage gain and the boost factor of ZSI and qZSI are equal and given by (2.33) and (2.34).

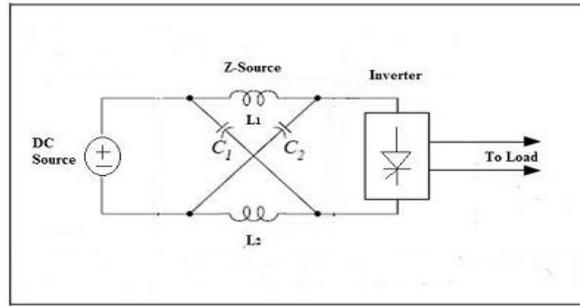


Figure 2.17: Z source inverter

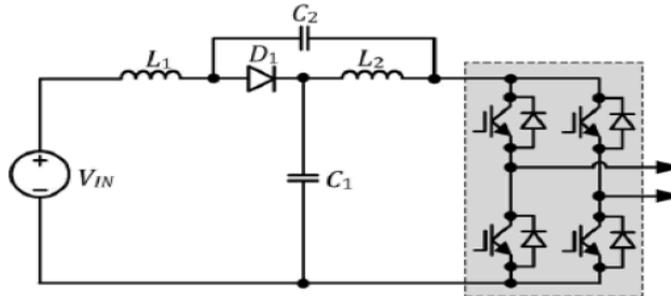


Figure 2.18: q-Z source inverter

$$G = \frac{\widehat{v}_p}{\frac{v_{in}}{2}} = MB \dots \dots \dots (2.33)$$

$$B = \frac{1}{1-2D_{sh}} \dots \dots \dots (2.34)$$

Theoretically the voltage gain capabilities of the ZSI and qZSI are infinite hence a smaller modulation index is used when very high voltage gains are required. The smaller the modulation index, the higher

the stress developed across the inverter components (Qian, W., Peng, F. Z., & Cha, H., 2011). The Trans ZSI was improved version of the qZSI to reduce the stress levels of the inverter and also increase the boost factor. In the case of the inductors, single inductors or coupled inductors can be used and the turns ratio is 1:1. The turns ratio when coupling is done between L1 and L2 is x:1 when capacitor C₂ is taken out of the circuit (Figure 2.19a) and the turns ratio changes to 1:x when C₁ capacitor is removed. The coupled inductor turns ratio is represented by x and the boost factor for the Trans Z source inverter is given by:

$$B = \frac{1}{1-(1+n)D_{sh}} \dots\dots\dots (2.35)$$

Detailed analysis of the effects of stray inductance on the performance of the inverter is explained in (Cha, H., Li, Y., & Peng, F. Z., 2016) and practical solutions given. This is mainly achieved by reducing the loop area and loop length between the dc source and the inverter bridge. One method proposed is application of two layer busbar lamination; this solves the problem caused by parasitic inductance or stray inductance. Also the number of busbar is not limited on two since 5 busbar is applicable; the other solution is the application of snubber circuits. In the improved Trans Z source inverter, a clamping diode D_c is added to the circuit to reduce the loop length and also solve the effects of stray inductance.

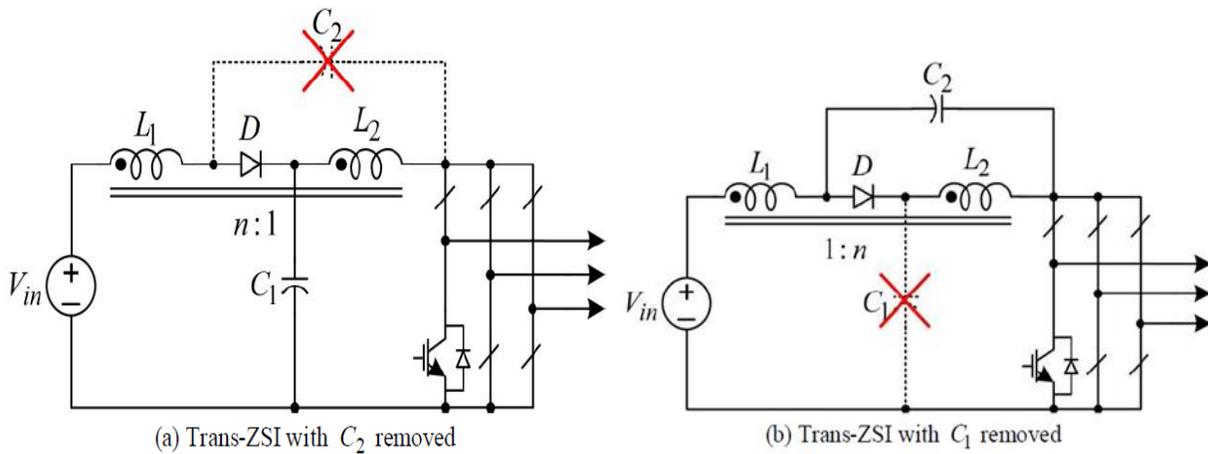


Figure 2.19: Trans Z source inverter.

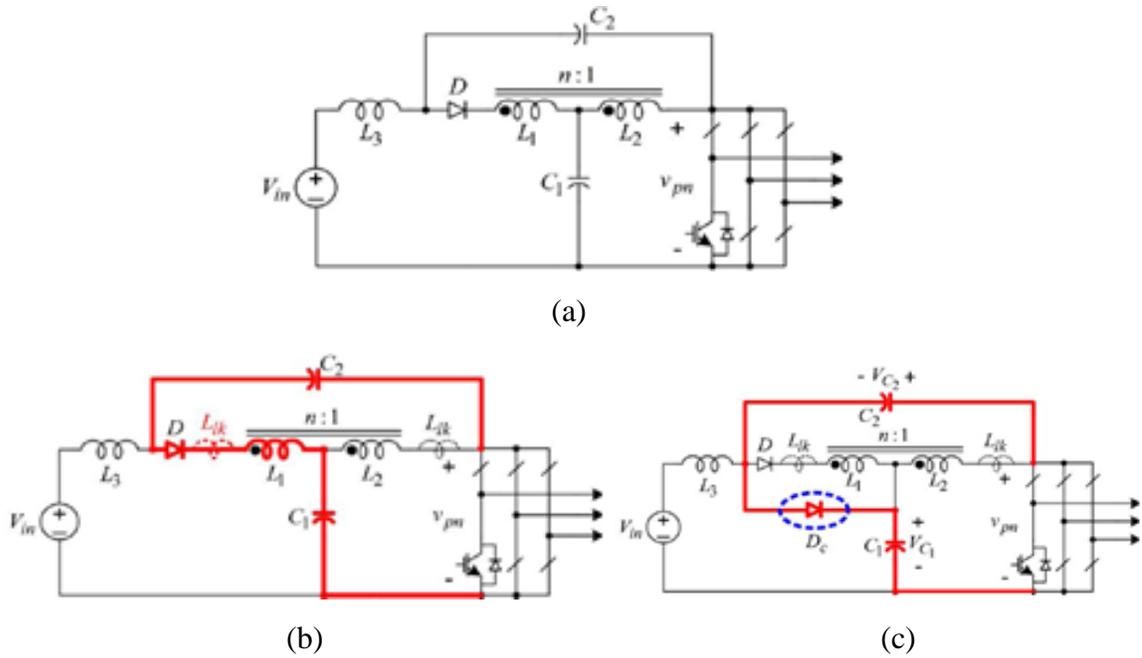


Figure 2.20: a) Improved trans. ZSI b) Improved trans. ZSI and high frequency loop
 c) high frequency loop in the improved trans. ZSI with the addition of clamp diode

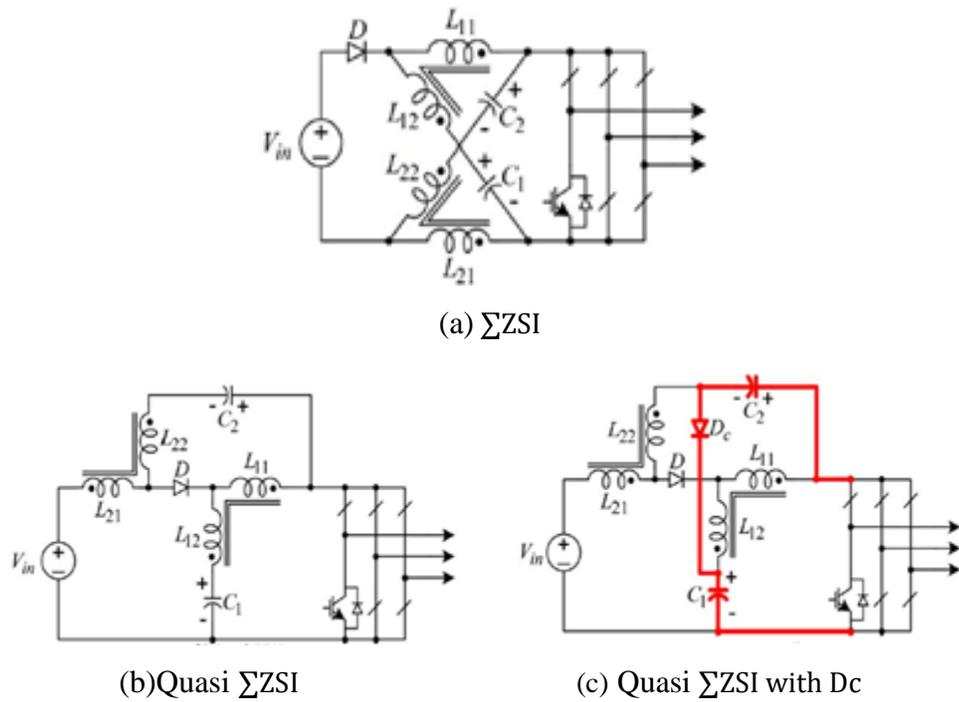
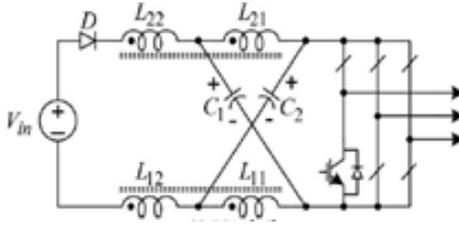
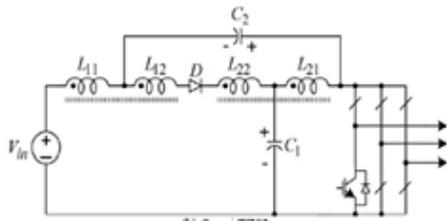


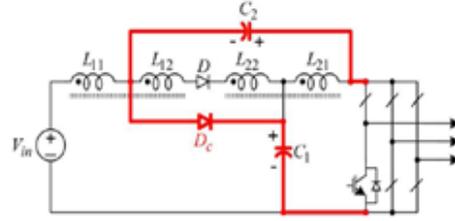
Figure 2.21: Σ ZSI and Quasi Σ ZSI



(a) TZSI ([25] S. Jiang, D. Cao, and F. Z. Peng, 2011)



(b) Quasi TZSI



(c) Quasi TZSI with Dc

Figure 2.22: TZSI and Quasi TZSI

An improvement in the basic structure of the Z source inverter was reported in (Shen, H., Zhang, B., Qiu, D., & Zhou, L., 2016) in which a common ground application was applied in Z source dc-dc converter having very high voltage gain. The introduction of renewable energy sources into power generation is an added advantage because of its positive attributes to the environment and relatively cheap when compared to conventional power generation systems. Wind and photovoltaic systems are the leaders in renewable energy system because of ease of installation and availability of smaller units for residential applications; fuel cells are gradually becoming widely available.

For better and efficient utilization of renewable energy, a good power converter is required to efficiently condition the power for standalone residential application or grid integration. Renewable energy source power generation systems have a wide range of output power because of the unreliable nature of the weather which is the ‘fuel’, hence a good power converter should be able to boost the output power regardless of the input power. Previous applications make use of double stage power conversion because a single converter does not have buck-boost capabilities.

2.10 Z Source dc-dc Converter

The conventional boost dc-dc converter has been applied widely for output power boosting and can produce infinite voltage if the duty cycle of the converter is equivalent to one. However parasitic resistance causes limitation on the peak level of the duty cycle. Theoretically the voltage gain of this converter is infinite but in practical applications it’s limited (Li, W., & He, X., 2011; Wai, R. J., & Duan, R. Y, 2005; Zhou, Y et al, 2003; Emadi, A. 2014). To overcome the limitations of this converter, several

topologies of converters have been proposed, examples are; non isolated boost dc-dc converter, non-isolated with voltage multiplier technique (Prudente, M et al, 2008; Pfitscher, L. L et al, 2014, Axelrod, B et al, 2003). Switched inductor topology (Axelrod, B et al, 2003, Tang, Y et al, 2015), switched capacitor topology (Abutbul, O e al, 2003, Luo, F. L., & Ye, H., 2004; Wu, G et al, 2015, Liang, T. J et al, 2012), cascaded topology (Walker, G. R., & Sernia, P. C., 2004).

The above so called improved topologies are too complex to operate also escalates the overall cost of the system and the system volume is also enlarged, efficiency is also reduced. The Z source network can overcome all the drawback of this converter and also render a high boosting ability with higher efficiency. An example of the impedance network coupled to a dc-dc converter (Zhang, J., & Ge, J., 2010) is shown in Figure 2.23a whiles Figure 2.23b shows the novel version of the ZS dc-dc converter. The difference between the topologies is that the diode in Figure 2.23a. is substituted to an inductor in Figure 2.23b. Detailed explanations of the merits and demerits of various improved Z source topologies have been presented in (Shen, H., Zhang, B., Qiu, D., & Zhou, L, 2016).

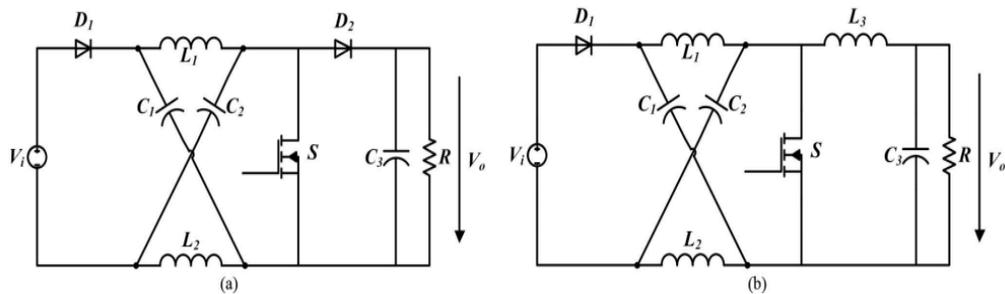


Figure 2.23: Z source dc-dc converter

The presented Z source dc-dc converter in (Shen, H et al, 2016) is shown in Figure 2.22, Figure 2.21a and Figure 2.21b shows the circuit diagram of the modes of operations; ‘zero’ state and ‘one’ state. The advantage of this dc-dc converter is the high voltage gain attributes and the common ground between the input and output sections of the converter. Slight adjustment of the load location produce the magnitude of the high voltage gain desired (Shen, H et al, 2016), other merits of the converter is the low voltage stress on the components and simple layout of the converter. The application of this converter can be in two folds; in single stage power conversion systems and double stage power conversion systems like PV systems. The application of this topology in double stage conversion system will produce highly efficient system and allow maximum power tracking (Xue, Y et al, 2004). The layout of this topology is very and it is made up of the following passive components; two inductors L_1 and L_2 , two capacitors C_1 and C_2 , and two diodes D_1 and D_2 , one switch S , a filtering capacitor C_3 and the load R . The difference between this topology and conventional converter in Figure 2.23a is the position of

the load and ground with respect to the source input, also the load and the source input are located on the same section of the impedance network of the converter and share the ground.

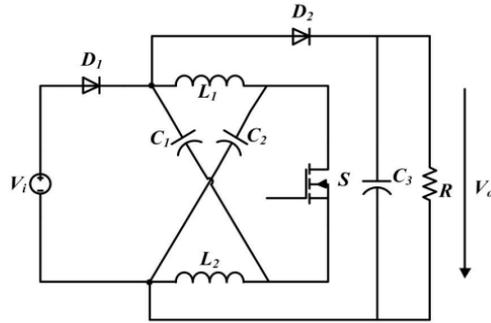


Figure 2.24: Z source dc-dc converter

The principle of operating the Z source dc-dc converter is similar to other z source converters, the symmetric conditions that exist in the basic Z source network applies to this topology as well, there's a linear increase and decrease of the capacitor voltage (v_{L1} and v_{L2}) and inductor currents (i_{L1} and i_{L2}). Hence the following conditions are valid:

$$\begin{cases} i_L = i_{L1} = i_{L2}, i_C = i_{C1} = i_{C2} \\ v_L = v_{L1} = v_{L2}, v_C = v_{C1} = v_{C2} \end{cases} \dots\dots\dots (2.36)$$

In state 0:

$$v_L = v_C = L \frac{di_L}{dt} \dots\dots\dots (2.37)$$

$$V_o = v_L + v_C = L \frac{di_L}{dt} + v_C \dots\dots\dots (2.38)$$

$$i_C = C \frac{dv_C}{dt} \approx i_L + I_o \dots\dots\dots (2.39)$$

In state 1:

$$V_i = v_L + v_L = L \frac{di_L}{dt} + v_C \dots\dots\dots (2.40)$$

$$i_i = i_C + i_L = C \frac{dv_C}{dt} + i_L \dots\dots\dots (2.41)$$

The continuous conduction mode of the converter can be categorized into two modes of operation; 0 states and 1 states. Figure 2.26 show waveform output for these modes of operation. These modes of operation occur in the dynamic state. The zero state is shown in Figure 2.26a while the one state or state one is shown by Figure 2.26b.

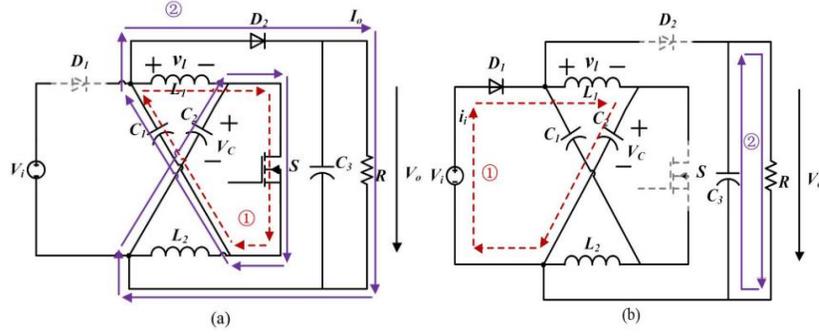


Figure 2.25: Z source dc-dc converter

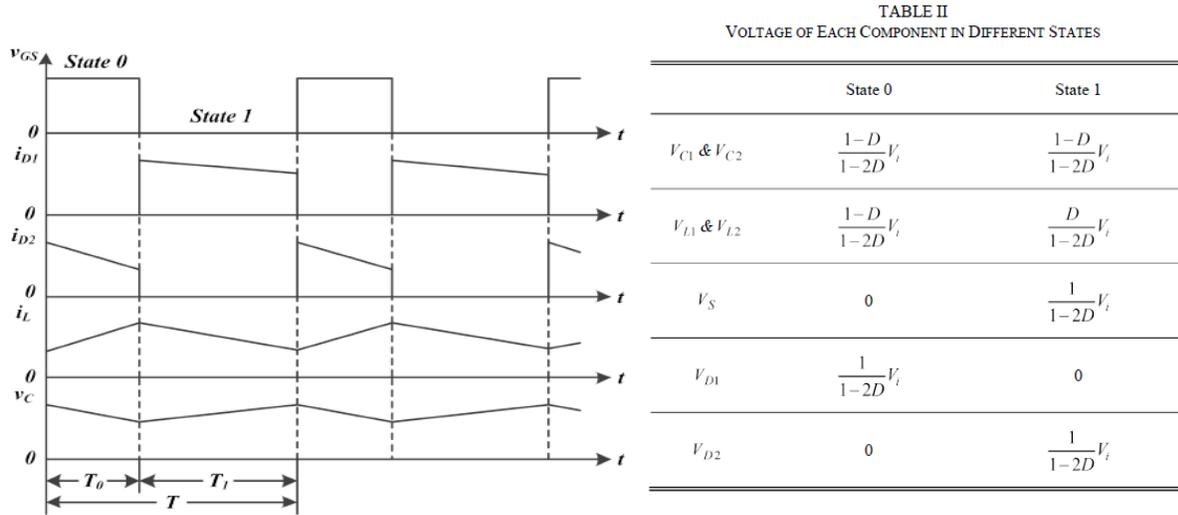


Figure 2.26: State one and zero waveform.

Table 2.1: Current of each Component in Different States

	State 0	State 1
$I_{L1} \& I_{L2}$	$\frac{2-5D+4D^2}{1-2D} I_o$	$\frac{2-5D+4D^2}{1-2D} I_o$
$I_{C1} \& I_{C2}$	$\frac{3-7D+4D^2}{1-2D} I_o$	$\frac{3D-4D^2}{1-2D} I_o$
I_S	$\frac{5-12D+8D^2}{1-2D} I_o$	0
I_{D1}	0	$\frac{2(1-D)}{1-2D} I_o$
I_{D2}	I_o	0

Table 2.2: Comparison on Number of Component

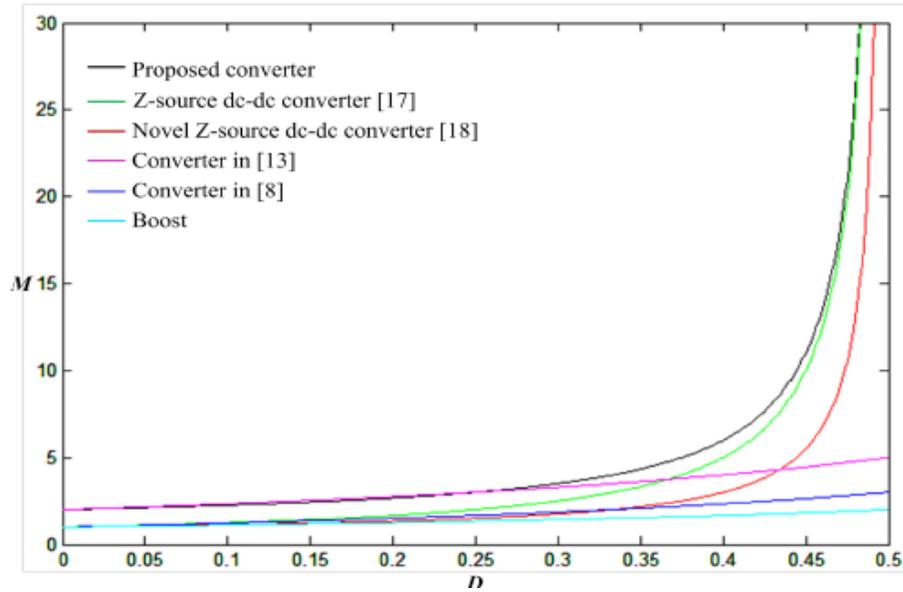
	Number of Components			
	Inductor	Capacitor	Diode	Switch
Boost	1	1	1	1
Proposed Converter	2	3	2	1
Z-source DC-DC Converter	2	3	2	1
Novel Z-source DC-DC Converter	3	3	1	1
Converter in [13]	1 coupled-inductor	4	4	1
Converter in [8]	2	1	4	1

Table 2.3: Comparison of Switch Stress

	Current Stress	Voltage Stress
Boost	I_0	U_0
Proposed Converter	$\left(D_0 + \frac{2}{D_0} - 2\right)I_0$	D_0U_0
Z-source DC-DC Converter	I_0	U_0
Novel Z-source DC-DC Converter	$(1 + D_0)I_0$	$(1 + D_0)U_0$
Converter in [13]	I_0	$\frac{2 - D_0}{3}U_0$
Converter in [8]	I_0	U_0

Table 2.4: Comparison of Diode Stress

	Current Stress	Voltage Stress
Boost	I_0	U_0
Proposed Converter	I_0	$D_0 U_0$
Z-source DC-DC Converter	I_0	U_0
Novel Z-source DC-DC Converter	I_0	$\frac{1}{1-D_0} U_0$
Converter in [13]	I_0	$\frac{1}{2+D_0} U_0$
Converter in [8]	I_0	U_0

**Figure 2.27:** Comparison of Voltage gains

A resonant Z source converter (González-Santini, N. S et al, 2016) with power factor correction is applied in wireless power transfer applications such as the charging of electric vehicle batteries. The Z source resonant converter executes output voltage regulation and power factor correction simultaneously due to impedance network in the structure of the converter. Three different on board battery charging converter is presented and compared with proposed topology. A simplified diagram of electric vehicle

charging is shown in Figure 2.28. The system utilizes online inductive power transfer principle, the electric vehicle has pickup coil located at the bottom of the car which connects wireless to the charging station to charge batteries on board the vehicle.

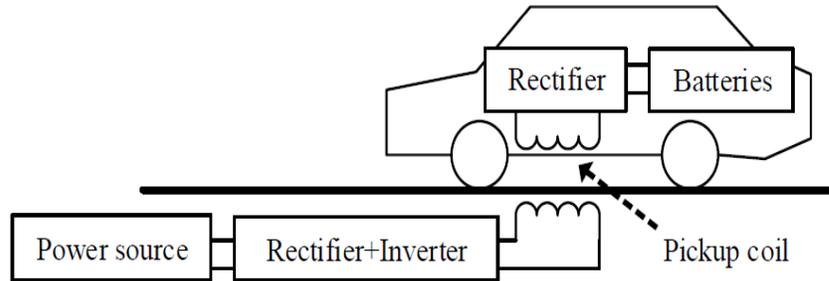


Figure 2.28: Wireless EH charging system

Figure 2.29 show the conventional on board battery charger in electric vehicles. This topology is made up of double stage power conversion i.e. ac to dc and dc to dc. From the diagram, the first stage of power conversion is a simultaneous task of changing ac to dc by means of rectification and also power factor correction. The other part is a dc to dc conversion and it's dependent on the desired dc voltage at the output.

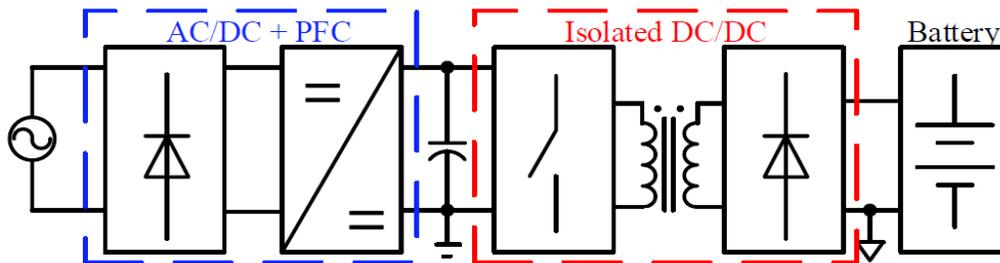


Figure 2.29: Conventional on board battery charging system

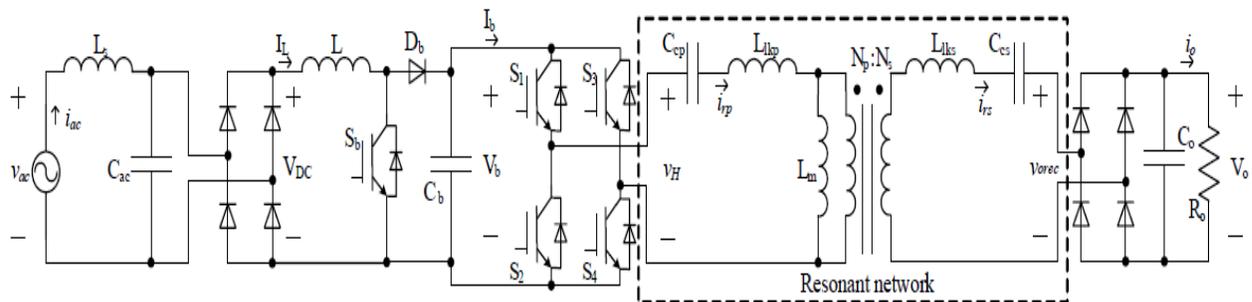


Figure 2.30: Boost converter for OBC

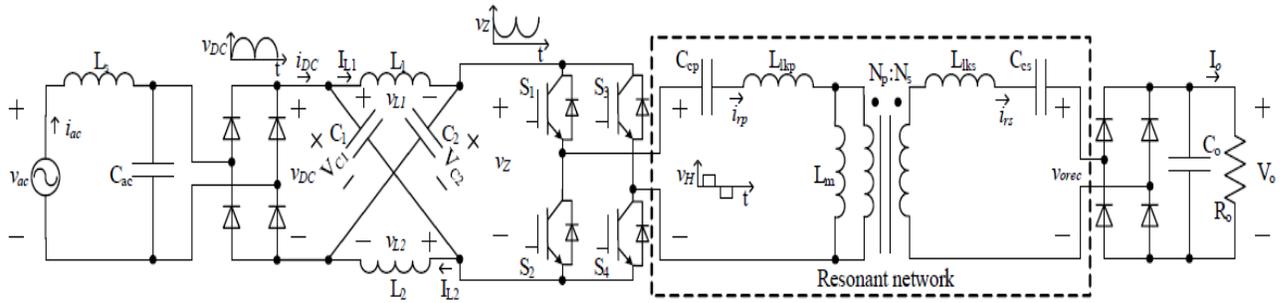


Figure 2.31: Proposed Z source resonant converter

The advantages of the traditional boost converter for on board battery charger are; low cost of the converter, power factor and power density are high, has good efficiency (Musavi, F et al, 2012). This topology is not suitable for high power applications the efficiency decreases due to the high losses incurred at the rectifier stage hence powers up to 3.5kW are suitable range for applications (Musavi, F et, 2012, Yilmaz, M., & Krein, P. T., 2013). The proposed topology has fewer semiconductor switches when compared to the boost topology but the proposed topology also has more passive components than the boost topology. The size and weight of the boost topology will be much higher due to the heat sink. There are three modes of operation state for the proposed Z source resonant converter as depicted in Figure 2.32. And the corresponding output waveforms are shown in Figure 2.33

- Active state
- Shoot through state
- Traditional zero state

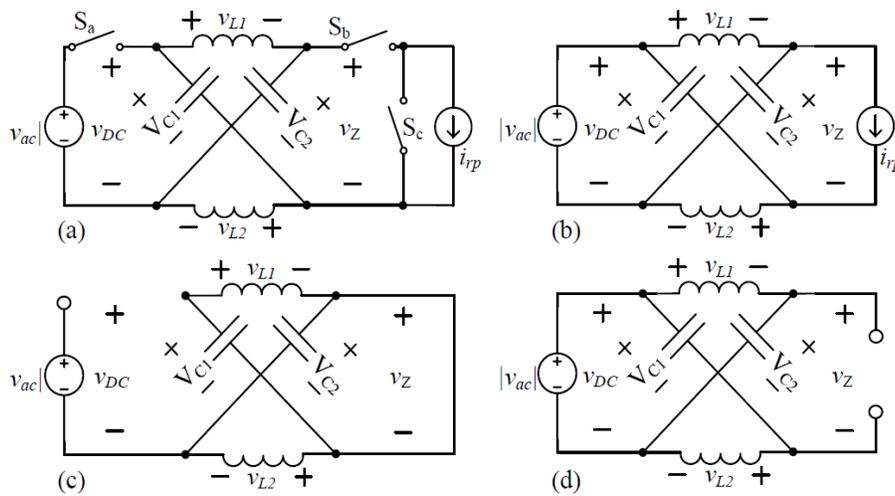


Figure 2.32: Modes of operation of ZSRC

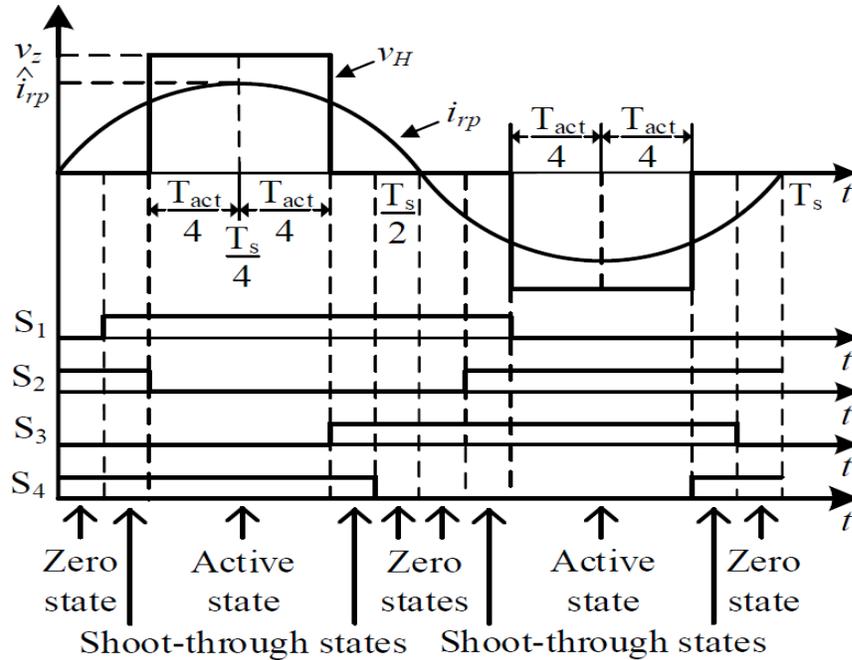


Figure 2.33: Modes of operation output waveforms

This paper (Dong, S., Zhang, Q., & Cheng, S., 2015) analysis the effects of ripples produced by the capacitor voltage and the critical inductance on bidirectional Z source inverter. Different literature areas (topology, parameters of the design, PWM control techniques) of Z source converter have been published over the and suitable application areas such as renewable energy sources; PV systems, wind energy, hybrid electric vehicles, power factor correction, motor speed control have been noted (Peng, F e al, 2007 , Lei, Q et al, 2014). Although Z source inverters have several advantages, there are a few draw backs such as large area required by capacitor and inductor which increase the overall space of the system. Conventional ZSI operates in two modes; continuous conduction mode CCM or discontinuous conduction mode DCM but that's not the case of the bidirectional Z source inverter shown in Figure 2.34. B-ZSI operates in CCM only because the bidirectional switch Sw7 enables reverse current flow from the load to the source. This paper categorizes the conduction modes of the bidirectional ZSI into the following groups:

- [1] Complete Inductor Energy-supplying Mode (CIEM)
- [2] Incomplete Inductor Energy-supplying Mode (IIEM)
- [3] Zero-crossing Input Current Mode (ZPCM)
- [4] Non-zero-crossing Input Current Mode (NPCM)
- [5] Zero-crossing Inductor Current Mode (ZICM)
- [6] Non-zero-crossing Inductor Current Mode (NICM)

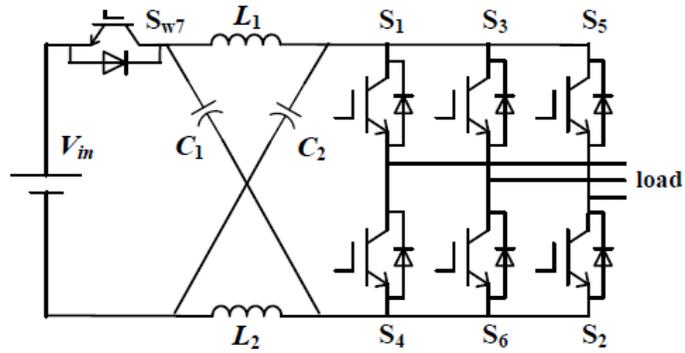


Figure 2.34: B-ZSI

Two modes (NICM and ZICM) of operation of Z source inverters exist; this is as results of the fact that the current of the inductor intersect the zero point or not. There are two groups of NICM mode of operation; CIEM and ILEM and their waveforms of the inductor current and capacitor voltage are shown in Figure 2.35 a and b respectively. The inductor current and capacitor voltage for the other mode of operation ZICM is shown in Figure 2.36.

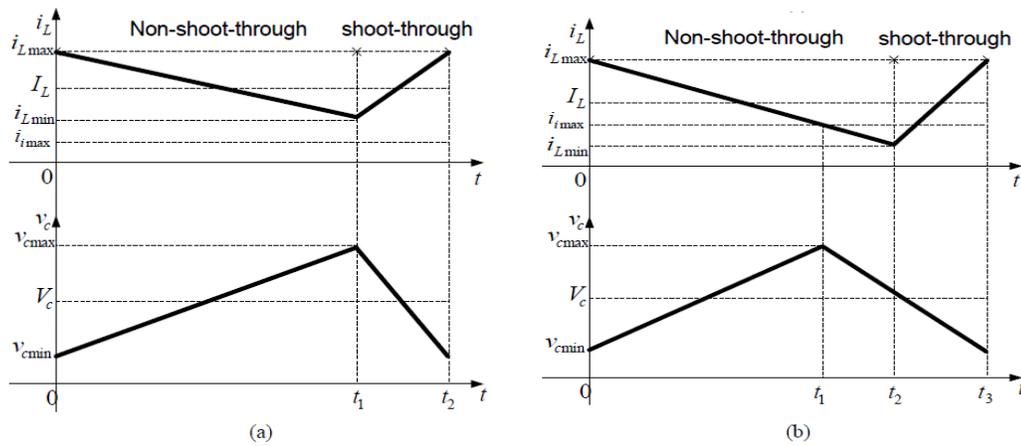


Figure 2.35: NICM of B-ZSI. (a) CIEM. (b) ILEM.

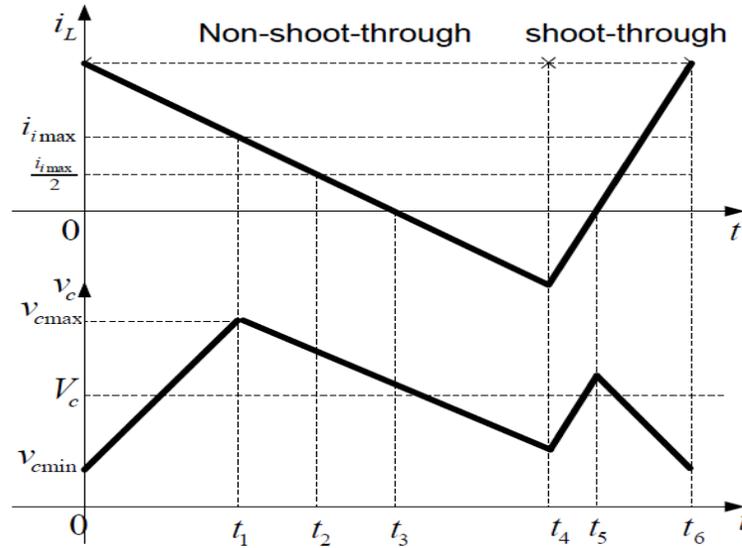


Figure 2.36: ZICM of B-ZSI

2.11 QZSI Based 1ph to 3ph

Several quasi Z source topology and applications have been presented since the four different quasi impedance topologies were presented in 2008 (Anderson, J., & Peng, F. Z., 2008). The first publication based application of qZSI is in photovoltaic energy generation system (Cintron-Rivera et al, 2009). Subsequently other forms of application have been published. In (Khosravi, N. A. e al, 2014), a qZSI topology is presented with reduced number of components and also three phase system is derived from a single phase inverter. The circuit of the proposed inverter is composed of four switches (H Bridge) and two capacitors in series with a neutral point in them. Figure.37 shows the circuit structure of the proposed inverter. The following advantages makes the HBqZSI more suitable for practical applications than the conventional ZSI; four switches means reduced switching losses, THD content is minimized, cost of the system is reduced because of less component usage. The application of space vector PWM translates into quality dc link voltage into the main converter circuitry hence filter cost and losses are eliminated. The structure of Figure 2.33 is made up of quasi impedance block, the H bridge block together series chain capacitors, three phase load and an LC filter block. The load is a resistive connected in wye connection. This topology is also suitable for 3-ph induction motor applications.

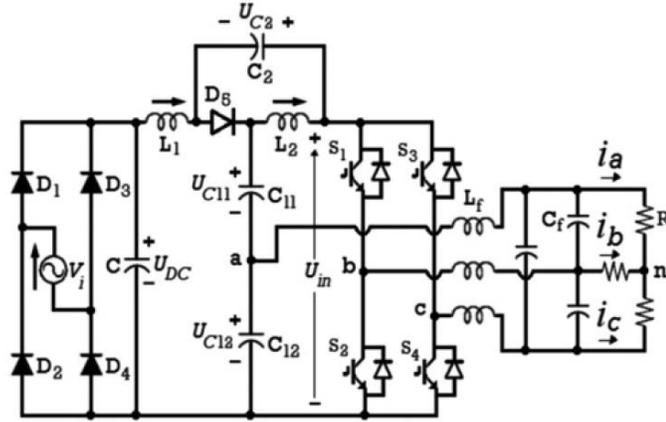


Figure 2.37: qZSI based 1ph to 3ph

As in the case of the case of all impedance based networks, the modes of operation of the converter is two; shoot through and non-shoot through. The shoot through mode is achieved by turning on switches S_1, S_2 or S_3, S_4 simultaneously, in this state the load voltage is zero and the inductors are charged by the capacitors and diode D_5 is reverse biased. The non-shoot mode is made up of active state and zero state.

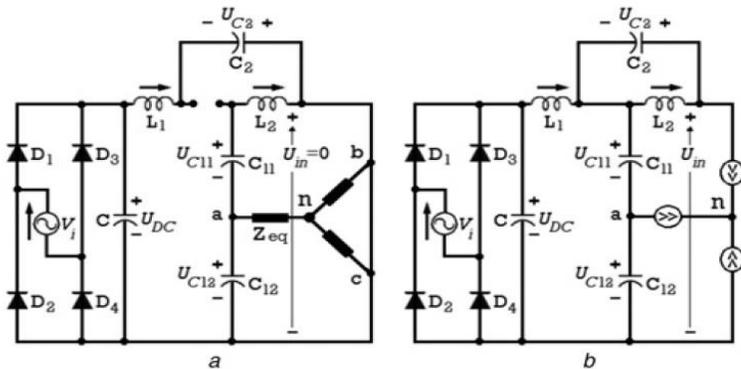


Figure 2.38: a) shoot through mode b) non shoot through mode

Power ripple of second order harmonic affects quasi Z source inverters design and performance hence analysis of the effects of current ripple and low frequency voltage is explored in (Liu, Y et al, 2015). Apart from multilevel inverters, qZSI is attracting a lot of attention in photovoltaic system applications because of its favorable wide range voltage endurance characteristics. Also the combination of cascaded multilevel inverter topologies with quasi impedance structure produces a robust inverter with many important qualities for PV system applications. Examples of such promising features are; maximum power tracking of individual panels, buck-boost capabilities, the number of modules required is 0.33 times less than the cascaded multilevel inverter (Xue, Y., Ge, B., & Peng, F. Z, 2012).

The second order harmonic (2ω) causes low frequency power ripple which brings about the 2ω wavelets on quasi impedance dc link, capacitor voltage and inductor current. The wavelets or ripples are

detrimental to smooth design and operation of qZSI hence they must be reduced to an acceptable range. As at the time of the publication of (Liu, Y et al, 2015) no literature has been published to investigate the effects of second order harmonic on qZSI. In the case of multilevel inverters, several publications have been made which address the concern of 2ω and three phase qZSI analysis has been done to curtail the effects second order effects on inductor current, dc link and capacitor voltage. (Liu, Y et al, 2015; Xue, Y et al, 2012; Xue, Y et al, 2011; et al, 2014; Rajakaruna, S., & Jayawickrama, L., 2010). The circuit structure is similar to all qZSI but with PV as source input.

A similar topology of qZSI is proposed to investigate the effects of the second order harmonics on systems design and performance. In this topology the qZSI has energy storage device (battery) connected in parallel to the capacitor. The main analysis of this paper (Liang, W et al, 2018) is to add a battery to topology and also use asymmetrical impedance components to see the effects on the system size which is a good parameter for an efficient converter. The asymmetrical quasi impedance based inverter has the ability to reduce the volume, size and eventually the cost and most importantly maximize the power density of the system (Liang, Z et al, 2015; . Hu, Z. Liang, and X. He, 2016; S. Hu, Z. Liang, D. Fan, and X. He, 2016).

2.12 QZSI and T type Inverter

A quasi Z source inverter combined with T type multilevel inverter is proposed in (Pires, V. F et al, 2016) and its operations investigated under two modes; normal operating condition and fault operating conditions. Application of the conventional 3-ph 2-level converter is enormous in industry due to its simple structure and ease of control, low cost and very high efficiency but there are some demerits which hinders the optimum operation of this converter; only buck capabilities unless boost converter is added to the structure, dead time or short circuit. The ZSI topology overcomes all this disadvantages [Abu-Rub, H et al, 2013; Battiston, A et al, 2014; T.-W. Chun, E.-C. Nho, 2015; Pires, V. F et al, 2014 Guo, F., et al., 2013; Husev, O et al, 2015).

The qZSI, which is an improvement of the conventional ZSI topology, provides the following attributes; continuous input current from the source, wide range of voltage applications and reduced ratings of components. Also the combination of qZSI and other multilevel inverters is not successful but able to retain the advantages of the two topologies hence several publications has been made about multilevel inverter based qZSI (Ott, S et al, 2011). The presented topology of (Abu-Rub, H et al, 2013) is shown in Figure 2.39.

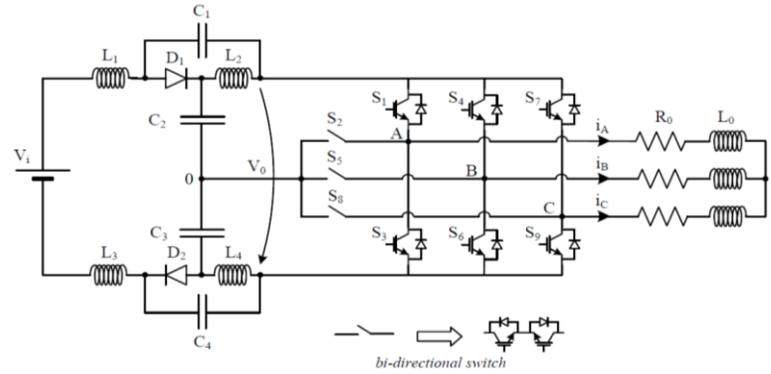


Figure 2.39: qZSI + T type inverter

The circuit of qZSI + T type inverter is made up of two quasi impedance network connected to a two series chain capacitor with a neutral point between the capacitor connection, a T type composed of bidirectional and unidirectional is connected an RL load. The number of bidirectional switch is 3 and 6 unidirectional switches for H Bridge. Two modes of operations exist; shoot through and non-shoot through. Five levels of voltage can be produced at the inverter and their magnitude is dependent on the boost factor. Two conditions of fault are critical for the components in the converter i.e. open circuit and short circuit. The short circuit fault is already protected by the impedance network so the open circuit fault was investigated by (Abu-Rub, H et al, 2013). An open circuit fault in any of the lower or upper legs leads to a new arrangement of the circuit to produce a new topology. For example if there should be a fault in phase A in Figure 2.39, its corresponding configuration is shown in Figure 2.40. The new topology is derived by precluding all switches on that leg (phase A) turning on its corresponding bidirectional switch (S_2), also the modulation methodology will change. Figure 2.41 show the new arrangement or topology if the open circuit fault occurs in any of the bidirectional switches which links the impedance network to the T type inverter. In this specific example, the bidirectional switch S_2 is disabled due to open circuit fault. The change in the modulation strategy is not as huge as in the open circuit fault of a phase leg.

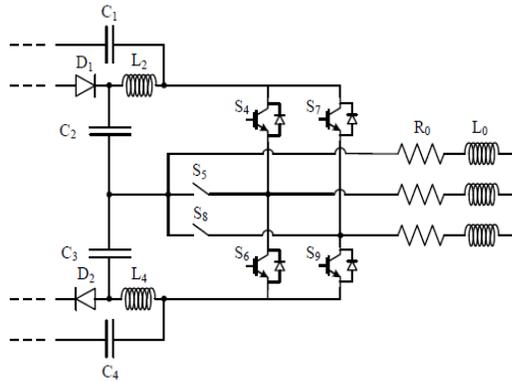


Figure 2.40: qZSI + T type inverter fault mode

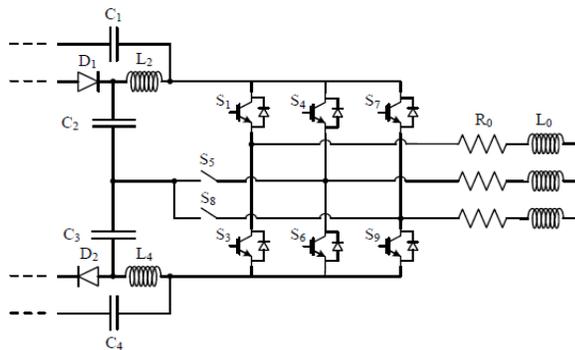


Figure 2.41: qZSI + T type inverter fault mode

2.13 Quasi Z Source Multipoint Converter

A quasi impedance inverter fused with multipoint power converter is presented in (Han, S. H et al, 2015) and the topology is referred to as ZIMPC. The goal is ZIMPC is to be applied in switched reluctance motor to allow for wide-scope of motor speed control and also to minimize the dc link capacitance. Hence the use of electrolytic capacitance which negatively impacts on cost, lifespan and power density of asymmetrical multilevel inverter will be avoided. The ZIMPC will reduced the power ripples of the system by employing capacitors with smaller size hence the cost of the system will be minimized.

Application of only integrated multipoint converter in speed control of switched reluctance motor drive cause higher voltage stress on the switches and capacitors due to the boost factor and this leads reduced system efficiency and the overall performance of the system is highly affected because higher voltage is required for speed control (Sun, D et al , 2015). One major advantage of quasi impedance network is reduced component stress hence amalgamating the qZS with IMPC to produce qZIMPC will lead to reduce voltage stress on the components. The circuit of qZIMPC is shown in Figure 2.42 A similar circuit employing the quasi impedance together with asymmetrical H Bridge known as qZSAHB is

shown in Figure 2.43. The circuit in Figure 2.42 requires extra leg to provide the shoot through mode.

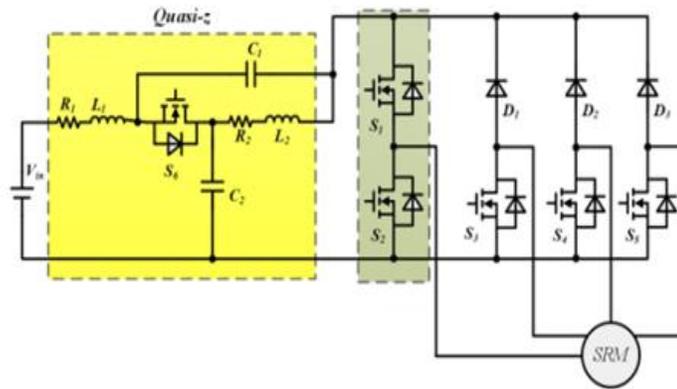


Figure 2.42: qZIMPC

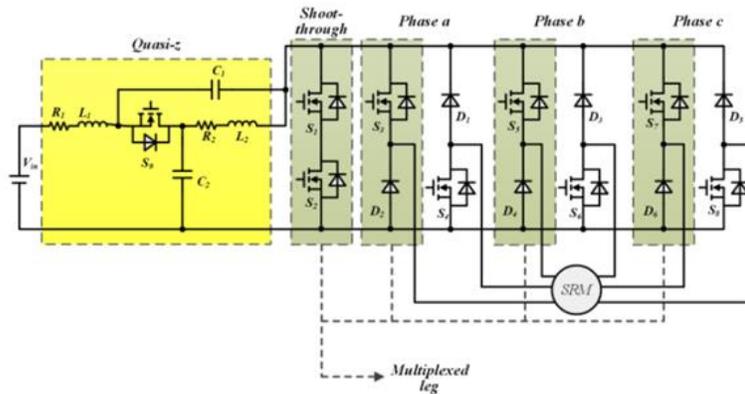


Figure 2.43: qZSAHB

Compared to asymmetrical H bridge topology the proposed qZIMPC has the following advantages which are summarized in Table 2.5;

1. The dc source voltage is not modified by the capacitor voltage because the two are not linked together.
2. The magnitude of the capacitors ripple voltage and average voltage should be high as possible in order to minimize the capacitance value to the least feasible level.
3. Electrolytic capacitor is eliminated because the source current is filtered by an inductor.
4. The impedance source provides an easily changeable dc link voltage which useful in the speed control of the switched reluctance motor.
5. The component count is minimized which directly translates to reduced cost and improved power density.

Table 2.5: Comparison between Proposed ZIMPC and conventional ASHB Topology

Topology	Size	Cost	Efficiency	Input current ripple
ZIMPC	Small	Low	High	Low
ASHB	Large	High	High	High
Topology	Semiconductor voltage stress	Semiconductor current stress	Capacitor voltage stress	CPSR
ZIMPC	High	High	High	Large
ASHB	Medium	Medium	Medium	Medium

2.14 qSBZS+T-type

Quasi switched boost topologies are further improvements on the quasi impedance source inverter to basically maximize the boost factor as much as possible. A quasi switched boost T type inverter is presented in (Nguyen, M. K et al, 2016), its pulsewidth control methods, analysis verification of the inverter are investigated. The voltage output level of the proposed inverter is 3. In other to reduce the current ripples, novel PWM control technique is proposed. The proposed control technique, the duty cycle of the shoot through mod is kept constant and the duty cycles (of the switches) are varied, this helps to maintain a very high modulation index. The circuit of the proposed qSBZS+T-type is shown in Figure 2.44. Figure 2.45 shows the various states of operation of the inverter; shoot through and non-shoot through. There are four modes (Figure 2.45a to Figure 2.45d) of non-shoot through which represents the active states of the switches and one shoot through mode; Figure 2.45e.

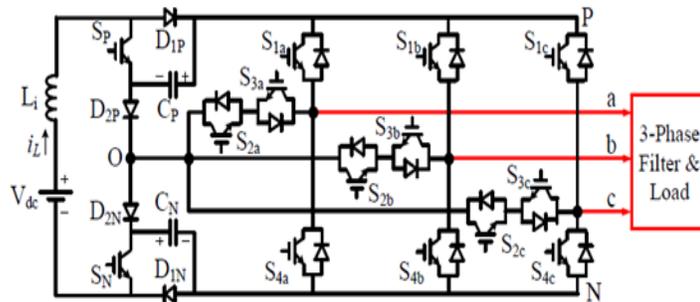


Figure 2.44: qSBZS+T-type

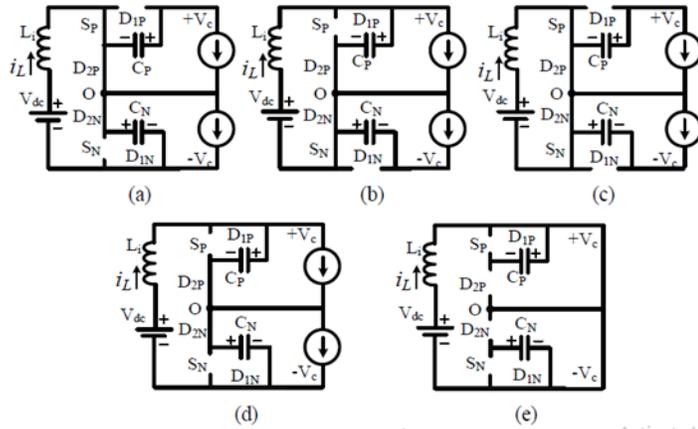


Figure 2.45: Modes of operation of qSBZS+T-type

The circuit of Figure 2.44 is derived by adding an impedance network which is made up of two switches, four diodes, two capacitors and an inductor (which connected in series to the dc source) to traditional the three-level T type inverter. This methodology is helps in boosting the output ac voltage and the inductor provides continuous current input from the source. The mode of operation is summarized into table 2.6 and its corresponding boost factor is given by (2.42). Comparison of the proposed invert to other similar topologies is presented in Table 2.7

$$B = \frac{2M}{4-6D_o-d_1-d_2} \dots\dots\dots (2.41)$$

Table 2.6: Switching States of the Proposed QSBT²I (x=a, b, c)

Mode	Triggered Switches	ON Diodes	V_x
NST 1	S_P	D_{2P}, D_{1N}, D_{2N}	$+V_C, 0$ or $-V_C$
NST 2	S_N	D_{1P}, D_{2P}, D_{2N}	$+V_C, 0$ or $-V_C$
NST 3	S_P, S_N	D_{2P}, D_{2N}	$+V_C, 0$ or $-V_C$
NST 4	S_{1x}, S_{2x}	$D_{1P}, D_{2P}, D_{1N}, D_{2N}$	$+V_C$
	S_{2x}, S_{3x}		0
	S_{3x}, S_{4x}		$-V_C$
ST	$S_{1x}, S_{2x}, S_{3x}, S_{4x}$	D_{1P}, D_{1N}	0

Table 2.7: Comparison of the three – level QSBT²I with other impedance – source – based three level inverter

	3L-ZSI with 1-LC [16]	3L-ZSI with 2-LC [13]	HB-SBI [24]	3L-BNI [25]	1S3L-BNI [26]	qSBT ² I with Proposed PWM
Inductors	2	4	2	2	1	1
Capacitors	2	4	2	2	2	2
Diodes (*)	20	20	6	22	22	16
Sources	2	2	2	2	1	1
Switches	12	12	4	14	14	14
Boost Factor, B	$1/(1-2D_0)$	$1/(1-2D_0)$	$(1-D_0)/(1-3D_0)$	$1/(1-2D_0)$	$1/(1-2D_0)$	$[1/(1-2D_0), 2/(1-2D_0)]$
Voltage Gain, G	$M/(2M-1)$	$M/(2M-1)$	$M^2/(3M-2)$	$M/(2M-1)$	$M/(2M-1)$	$[M/(2M-1), 2M/(2M-1)]$
Input Current	<i>Discontinuous</i>	<i>Discontinuous</i>	<i>Discontinuous</i>	<i>Continuous</i>	<i>Continuous</i>	<i>Continuous</i>
Peak-Peak Inductor Current	$\frac{D_0(1-D_0)TV_{dc}}{2(1-2D_0)L_f}$	$\frac{D_0(1-D_0)TV_{dc}}{4(1-2D_0)L_f}$	$\frac{D_0(1-D_0)TV_{dc}}{2(1-3D_0)L_f}$	$\frac{D_0(1-D_0)TV_{dc}}{2(1-2D_0)L_f}$	$\frac{D_0(1-D_0)TV_{dc}}{(1-2D_0)L_f}$	$\frac{D_0TV_{dc}}{2L_f}$
Current Ripple	<i>Very high</i>	<i>Very high</i>	<i>Very high</i>	<i>Low</i>	<i>Low</i>	<i>Very low</i>
Capacitor Voltage Stress	$\frac{(1-D_0)V_{dc}}{1-2D_0}$	$\frac{(1-D_0)V_{dc}}{2(1-2D_0)}$	$\frac{(1-D_0)V_{dc}}{2(1-3D_0)}$	$\frac{0.5V_{dc}}{1-2D_0}$	$\frac{0.5V_{dc}}{1-2D_0}$	$\left[\frac{0.5V_{dc}}{1-2D_0}, \frac{V_{dc}}{1-2D_0}\right]$
Switch Voltage Stress	<i>Not Applicable</i>	<i>Not Applicable</i>	$\frac{(1-D_0)V_{dc}}{2(1-3D_0)}$	$\frac{0.5V_{dc}}{1-2D_0}$	$\frac{0.5V_{dc}}{1-2D_0}$	$\left[\frac{0.5V_{dc}}{1-2D_0}, \frac{V_{dc}}{1-2D_0}\right]$
Output voltage	Three-phase, 3L	Three-phase, 3L	Single-phase, 3L	Three-phase, 3L	Three-phase, 3L	Three-phase, 3L

(*) including body diodes. 3L: Three-level.

2.15 Quasi Switched Boost Cascaded HB Inverter

A cascaded H-bridge topology is improved by the addition of quasi switched boost impedance network. As stated above the quasi switched boost is an improvement over the quasi Z source network having the following merits; reduced component number and higher boost factor. In (Bratcu, A. I et al, 2011) the quasi switched boost impedance structure is combined with H Bridge inverter to produce 5 level qSBCHBI. This topology combines the advantages of the cascaded H Bridge inverter (quality output waveform, reduced harmonic content, reduced filter component ratings and good resistant to the effects of EMIs) and the quasi impedance network. The topology of qSBCHBI is shown in Figure 2.46.

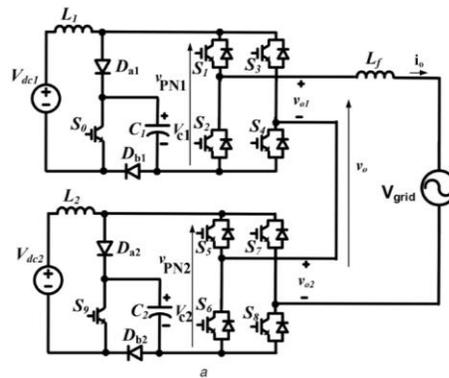


Figure 2.46: qSBCHBI

The proposed qSBCHBI is made up of two modules of H Bridge connected in series. Each module has

dc voltage source quasi switched boost impedance network connected to it. The impedance network is made up of one switch, one inductor, one capacitor and two diodes. The output voltage of qSBCHBI is the addition of the output voltages of the modules; V_{o1} and V_{o2} as shown in Figure 2.46. Table 1 compares two cascaded quasi Z source topologies. From the table 2.8, it is evident that the proposed topology has reduced component count hence the cost of the system is decreased but the switching losses is increased because two more switches are employed in qSBCHBI. Higher levels of output voltage will reduced the system size.

Table 2.8 : Comparison between cascaded five – level qSBI and qZSI

	Cascaded qSBI	Cascaded qZSI
number of inductors	2	4
number of capacitors	2	4
number of diodes	12	10
number of switch	10	8

Just as in the case all impedance source structures, two modes of operations exist; shoot through mode and non-shoot through mode. Figure 2.47a and 2.47b shows these two modes respectively. In the shoot through mode switch S_o is gated on and the two diodes D_a and D_b are reverse biased. The inductor is charged by the capacitor and the dc link voltage V_{PN} is zero. In the non-shoot through mode switch S_o is opened and diodes D_a and D_b are forward biased, the inverter circuit power is supplied by the inductor and it functions as a current source. (2.42) and (2.43) give the KVL for the two modes respectively. The voltage output level of this proposed inverter is not limited to 5 but can be extended to a much higher levels as desired. In multilevel inverters, high levels of output voltage correspond to much higher quality output waveforms.

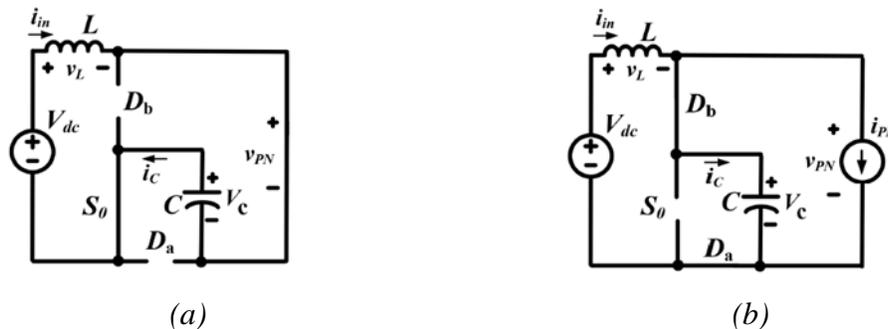


Figure 2.47: a) Shoot through b) Non-shoot through

$$v_L = L \frac{di_L}{dt} = V_{dc} + V_C \dots \dots \dots (2.42)$$

$$\begin{cases} V_L = V_{dc} - V_c \\ V_c = V_{PN} \end{cases} \dots\dots\dots (2.43)$$

2.16 Quasi switched Boost dc-dc Converter

An isolated high boost quasi switched boost inverter is presented in (Wu, G., et al, 2015). This topology has the following merits; the source current is continuous, the system is definitive because its operation in open and short circuits are not restricted, the isolation transformer has minimized turns ratio, variable shoot through duty cycle does not change the voltage waveforms of the secondary and primary windings. Isolated and non-isolated converters have received much attention in recent years in areas of higher boosting capabilities. Galvanic seclusion is not present in non-isolated converters hence the following methods have been provided: cascaded topologies, switched capacitor, coupled inductor, voltage multiplier units, switched inductor to function in transformer less systems to provide high boost and maximum power density and efficiency (ang, Y et al, 2015 , Nymand, M., & Andersen, M. A,2010). Isolated converters were proposed to address the drawbacks in the no-isolated topologies; these drawbacks are mainly about safety standards (Wu, G et al, 2015). Step-up converters combined with transformers and voltage lift methodologies are some examples of isolated converters (LaBella, T., & Lai, J. S, 2014 , Nguyen, M. K et al, 2018).

The proposed high step-up quasi switch boost dc to dc converter is shown in Figure 2.48. The circuit is composed of quasi switched boost inverter, voltage double rectifier and isolation transformer. The impedance network is made up of two diodes, one inductor and capacitor each, the inverter circuit has four semiconductor switches with four anti-parallel diodes, one step-up seclusion transformer and the voltage double rectifier has two capacitors and two diodes. The modes of operations are continuous conduction mode and discontinuous conduction mode. Also shoot through and non-shoot through modes exist.

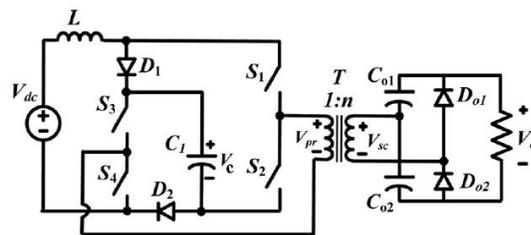


Figure 2.48: Quasi switched boost dc-dc converter

2.17 SC/qSBI

Combinations of two switched topologies are presented in (Ahmed, H. F et al, 2016) the switched

capacitor and the quasi switched boost topologies. This new topology known as SC/qSBI is achieved by adding a diode and a capacitor to the quasi switched boost inverter. The merit of the proposed topology is reduced stress on the active and passive components and high voltage gain or high boost factor. The switched boost inverters and quasi switched boost inverter are improvement on the traditional impedance source inverter-ZSI. They are better than the latter because the number of components required are reduced. Also these topologies are preferred to other converters because they provide single stage conversion, continuous source current input, buck-boost capabilities. The proposed SC/qSBI topology is shown in Figure 2.49. Two types of SC/qSBI are presented. The difference lies in the position of the active switch in the impedance network, in the first type (a) the switch is connected between the inductor and the diode D_y and the second type (b) the switch is connected with the source and inverter to the ground or negative connection. The components in the impedance network are two capacitors (C_1 and C_0), three diodes (D_1 , D_y and D_x), one inductor and one active switch. Also one major advantage of the proposed inverter is the ability to extend it to form multicell top produce multilevel waveforms at the output.

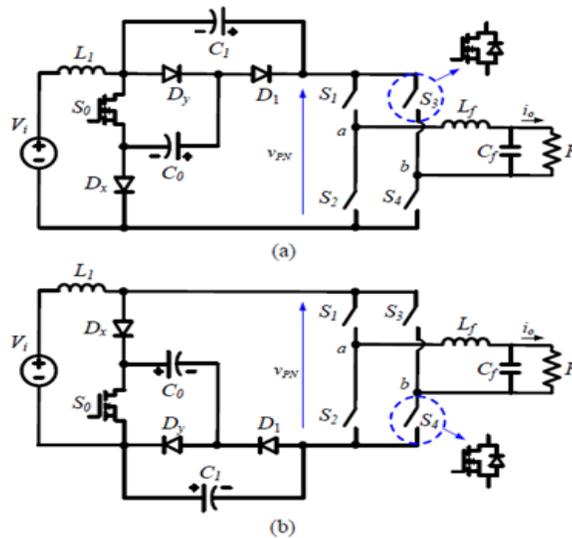


Figure 2.49: SC/qSBI a) type 1 b) type 2

Figure 2.49 represents the modes of operation of the inverter. Type 1 will be used as a case study to explain the modes of operation. In the shoot through mode, switches S_0 , S_1 and S_2 are gated on simultaneously to produce short circuit at the inverter side. At this state the inverter voltage is zero and diode D_1 conducts but diodes D_x and D_y do not conduct because of the negative voltage across the. Capacitor C_0 is discharging whiles inductor L_1 and capacitor C_1 are charged. All this occurs during the period $D.T$ and D is the duty cycle of the shoot through and T is period of switching. If we apply

KVL/KCL to Figure 2.50a, the following mathematical expressions will be produced:

$$\begin{cases} V_{L1} = V_i + V_{C0} \\ V_{C0} = V_{C1} \\ V_{PN} = 0 \end{cases} \dots\dots\dots (2.44)$$

$$\begin{cases} i_{C0} = -i_{C1ST} - I_{L1} \\ i_{C1} = i_{C1ST} \end{cases} \dots\dots\dots (2.45)$$

Figure 2.50b represents the non-shoot through mode of the inverter, switch S0 is turned off and the inverter operation is the same conventional modes of operation; active states and zero state. Diode D1 is now non-conducting while's diodes Dx and Dy are conducting. Capacitor C0 is fully charged and capacitor C1 and inductor L1 are discharged. If we apply KVL/KCL to Figure 2.50a, the following mathematical expressions will be produced:

$$\begin{cases} V_{L1} = V_i - V_{C0} \\ V_{PN} = V_{C0} + V_{C1} \end{cases} \dots\dots\dots (2.46)$$

$$\begin{cases} i_{C0} = I_{L1} - I_{PN} \\ i_{C1} = -I_{PN} \end{cases} \dots\dots\dots (2.48)$$

The boost factor of the proposed switched capacitor – quasi switched boost inverter is twice that of the quasi boost inverter and is given in (2.49).

$$B = \frac{2}{1-2D} \dots\dots\dots (2.49)$$

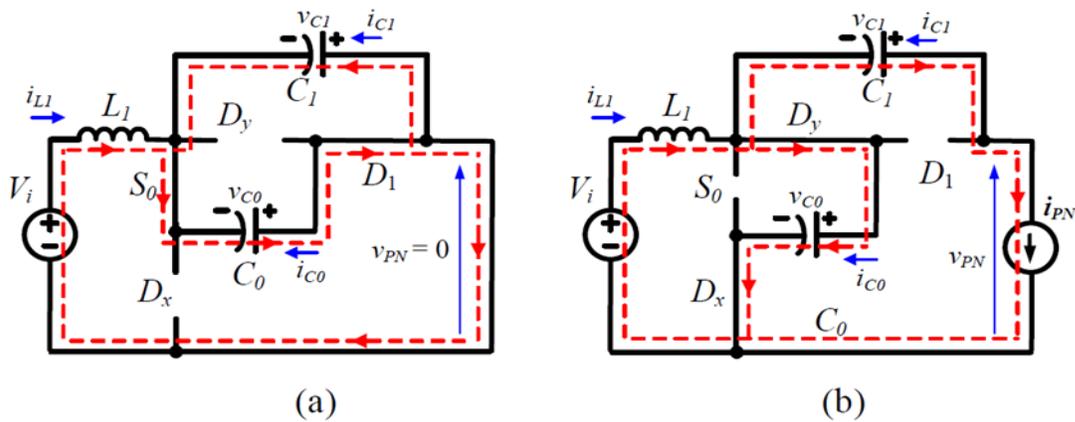


Figure 2.50: Operational states of SC/qSBI

The multi cell structure of the proposed switched capacitor – quasi switched boost inverter is shown in Figure 2.51 and the boost factor is represented in two forms i.e. when n is odd or even.

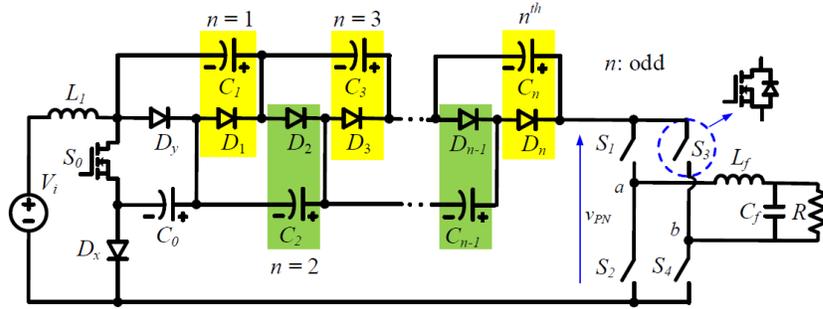


Figure 2.51: Multicell structure of SC/qSBI

Boost factor B =

$$\begin{cases} \frac{2+in(\frac{n}{2})}{1-[2+in(\frac{n}{2})]D} & n = \text{odd number} \\ \frac{1+\frac{n}{2}}{1-(2+\frac{n}{2})D} & n = \text{even number} \end{cases} \dots\dots\dots (2.50)$$

2.18 SCL/qZSI

The switched capacitor/coupled inductor quasi Z source topology (Peng, F. Z., Shen, M., & Qian, Z., 2005) is derived by combining three other impedance sourced topologies: the switched capacitor, the switched couple inductor with three windings and the quasi Z source inverter.

This new topology is referred to as SCL/qZSI and it possess all the advantages of three topologies; reduced voltage stress on the active and passive components. Higher boost factor, immunity to the effects EMI, continuous input current, reduced component count, the applied modulation index is hence quality output waveforms are produced, inrush current at startup is reduced, common node for the source voltage. in the inverter circuit (Shen, M., et al, 2006 , Adda, R et al, 2013). The proposed SCL/qZSI is shown in Figure 2.52. The circuit is made up of the impedance network which is composed of the switched capacitor, switched coupled inductor and the quasi impedance network and the three phase H bridge circuit made up of six switches. The impedance structure has one inductor, three windings of coupled inductor, two capacitors, three diodes. The modes of operations are shoot through state and the non-shoot through state which are shown in Figure 2.53a and 53b respectively.

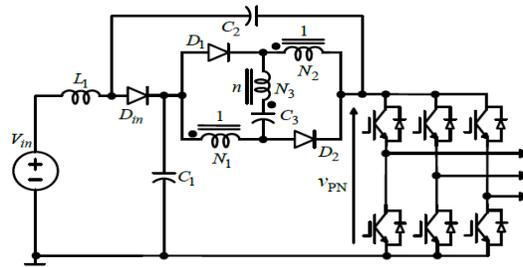


Figure 2.52: SCL/qZSI

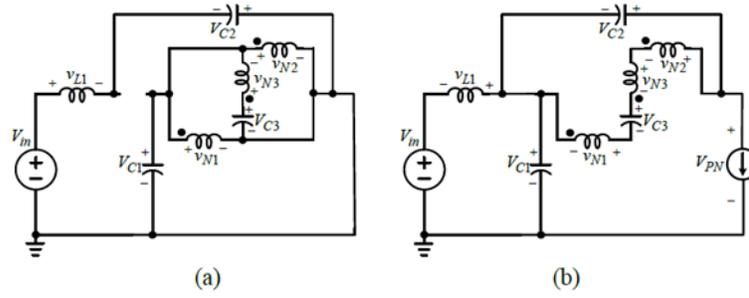


Figure 2.53: a) Shoot through b) non-shoot through

In the shoot through state diode D_{in} is reversed biased and diode D_1 and D_2 are forward biased, capacitor C_1 charges windings N_1 and N_2 , also C_1 charges capacitor 3 via windings N_3 . In the non-shoot through state, diode D_{in} is forward biased and diode D_1 and D_2 are reverse biased. Power to the inverter circuit is provided capacitor C_3 and the three windings. Applying KVL/KCL to Figure 2.53a and 53b will produce (2.51) and (2.52) respectively.

$$\begin{cases} V_{L1} = V_{in} + V_{C2} \\ V_{N1} = V_{C1}, V_{N3} = nV_{N1} \\ V_{C3} = (n + 1)V_{C1} \end{cases} \dots\dots\dots (2.51)$$

$$\begin{cases} V_{L1} = V_{PN} - V_{in} - V_{C2} \\ V_{C2} - V_{C3} = V_{N1} + V_{N2} + V_{N3} \\ V_{N1} + V_{N2} + V_{N3} = V_{PN} - V_{C1} - V_{C3} \end{cases} \dots\dots\dots (2.52)$$

The boost is given by (2.53) where n is the turns ratio of the windings

$$B = \frac{n+2}{(1-(3+n)D)} \dots\dots\dots (2.53)$$

Table 2.9: Comparison of selected transformer type impedance source inverters

Topology	TSI-TZSI	Y- ZS	Σ ZSI	ITQSZI	ArZSI	LCCTZSI	TQZSI	r ZSI	TransAZSI
Component count	1-T	1-3wT	2-T	1-T	1-T	1-T	2-T	1-T	1-T
	1-C	1-C	2-C	1-L	1-L	1_L	1-D	1-C	1-C
	1-D	1-D	1-D	2-C	2-C	2-C	2-C	1-D	1-D
C.I.C	No	No	No	Yes	Yes	Yes	Yes	No	Yes
Inrush current	Yes	Yes	Yes	No	No	No	No	Yes	Yes
Common ground	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
Boost Factor	$(1/1 - (n+1)D_0)$	$(1/1 - kD_0)$	$(1/1 - rD_0)$	$(1/1 (n + 2)D_0)$	$[1/1 (2 + (1/rz - 1)D_0)]$	$(1/1 - (n + 1)D_0)$	$(1/1 - (n_1 + n_2 + 2)D_0)$	$[1/1 - (1 + (1/rz - 1)D_0)]$	$(1/1 - (n + 1)D_0)$

Footnotes:

1-T: one transformer

1-3wT: one transformer with 3 windings

2-C: two capacitors

1-D: one diode

2.19 Conclusion

The goal of this chapter of my thesis is a review of Z source inverter topologies or structures taken into considerations the type of topology, mathematical analysis, its application in either industry or academia. This review has exposed to me the qualities of Z source inverter such high boost functionality, single stage voltage conversion, shoot through capabilities which protects the inverter from the negative effective EMIs. The Z source inverter employs an impedance network between the source and the main inverter circuit to produce high boost or increase the voltage gain which absent in the conventional voltage or current source inverters. Also voltage source converters are applicable in dc-ac inversion, dc-dc conversion, ac-dc rectification and ac-ac conversion.

CHAPTER 3

POWER CIRCUIT DESCRIPTION AND SIMULATION RESULTS

3.1 Introduction

The process of changing dc voltage/power to ac voltage/power is known as inversion; this process is realized by the use of principal device called an inverter. The first inverter is commonly known as the conventional 2-level inverter which is a voltage source inverter- VSI. The voltage source inverter also known as voltage source converter (when used for both inversion and rectifying purposes) has wide areas of applications but it's fraught with many limitations: a. it's a buck or step down inverter that's the output voltage is always less than the input voltage unless a buck-boost converter is applied. When used as a rectifier, it's a boost rectifier circuit, b. applications of buck-boost converter in VSI topology increases the cost of the unit, reduces the efficiency of the system and complicated control technique is introduced, shoot through property is absent in VSI or CSI hence EMIs immunity is absent, inductor – capacitor filter is required to reduce power systems noises. The introduction of conventional Z source inverter solved the limitations of VSI and CSI, ZSI also has a number of limitation such as limited boosting capabilities and high number of passive components as well as limited control of the impedance structure due to lack active components.

3.2 Chosen Topology

The circuit impedance source topology is known as switched boost inverter (SBI); its circuit is shown in Figure 3.1. The circuit of switched boost inverter is composed of passive and active components as the impedance network sandwiched between the dc source and the single phase inverter bridge. The active components are two diodes and a switch, while one inductor and one capacitor constitute the passive components. The output of the H Bridge inverter is connected with an inductor-capacitor (LC) filter to minimize the harmonic content in the output voltage.

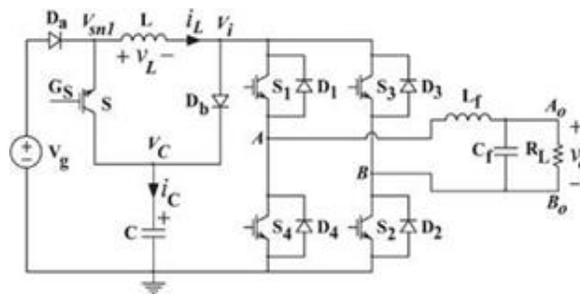


Figure 3.2.1: Switched boost inverter

The circuit analysis of the switched boost inverter is similar to the traditional impedance source network; shoot through analysis and non-shoot through analysis. In the shoot through mode, switch G_s is gated on and this results in diodes D_b and D_a being turned off because the capacitor voltage is greater than the source/input voltage, at this state the inductor is charged by the capacitor and the discharging current from the capacitor equals to the inductor current. The duration of this process is $D.T_s$ during switching period of T_s . The circuit of the shoot through mode is shown if Figure 3.2a. The shoot through mode is achieved by turning on simultaneously all switches on the same leg; this renders the inverter bridge short circuited and hence the input voltage v_i to the inverter bridge which is the output voltage from the impedance network is zero. The non-shoot through mode is shown in Figure 3.2b and this occurs during the switching period of $T_s (1 - D)$; in this mode, the switch G_s is switched off. The input voltage to the bridge circuit is supplied by the main source V_g and the inductor v_L , also the capacitor is charged by these two voltages (V_g and v_L). The two diodes D_a and D_b are forward biased. Due to the inductor in series with the main voltage source, the input to the inverter bridge is now a current source hence the inverter bridge becomes current source inverter. The inverter input current i_i is the difference between the inductor current and the capacitor current. Figure 3.3 show the equivalent switched boots inverter circuit in its simplified form.

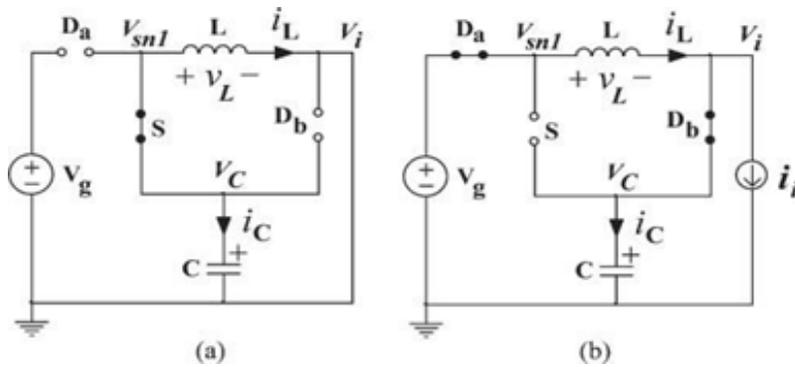


Figure 3.2.2: a) shoot through b) non-shoot through

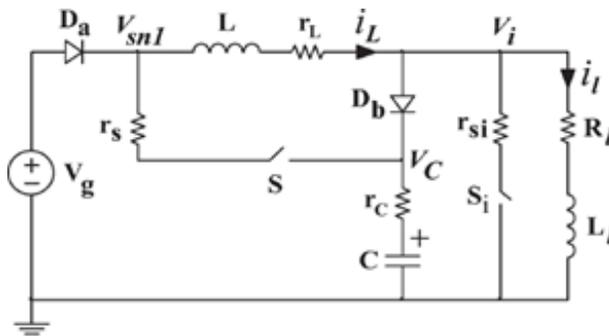


Figure 3.2.3: Clarified switch boost inverter circuit.

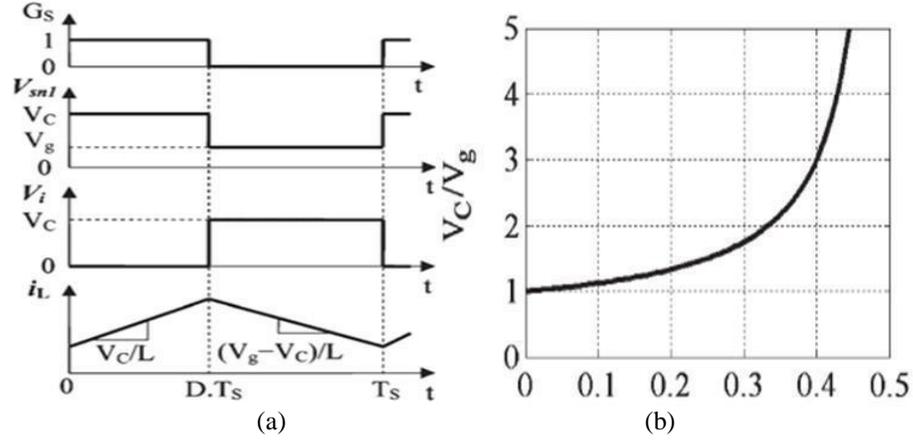


Figure 3.2.4: a) SBI stable state waveforms b) SBI duty ratio

Using the stable state waveform analysis of Figure 3.4a, the following mathematical equations are derived for the shoot through and non-shoot through modes. The inductor voltage, capacitor current and the inverter bridge voltage are given by v_L , i_C , and v_i respectively.

$$v_L = V_C, 0 < t < D.T_s \text{ and } v_L = V_g - V_C, D.T_s < t < T_s \quad (3.3)$$

$$i_C = -i_L, 0 < t < D.T_s \text{ and } i_C = i_L - i_i, D.T_s < t < T_s \quad (3.4)$$

$$v_i = 0, 0 < t < D.T_s \text{ and } v_i = V_C, D.T_s < t < T_s \quad (3.5)$$

The following equations (3.6) to (3.8) are derived from the above equations after applying small ripple estimation.

$$v_L = V_C, 0 < t < D.T_s \text{ and } v_L = V_g - V_C, D.T_s < t < T_s \quad (3.6)$$

$$i_C = -I_L, 0 < t < D.T_s \text{ and } i_C = I_L - I_i, D.T_s < t < T_s \quad (3.7)$$

$$v_i = 0, 0 < t < D.T_s \text{ and } v_i = V_C, D.T_s < t < T_s \quad (3.8)$$

The inverter bridge input voltage V_i which is known as the dc link voltage is determined by (3.9) and its derived after applying charge second balance rule:

$$V_i = V_C(1 - D) \quad (3.9)$$

To determine the passive component values, KCL (Kirchhoff's current law) and KVL (Kirchhoff's voltage law) can be applied to Fig. 3a and 3b, to derive the equations below. When switch S is closed, diodes D_a and D_b are reverse biased because V_C is greater V_L and also the SBI is in the shoot through state hence they are in no-conduction mode but when switch S is opened (non-shoot through state), diodes D_a and D_b are forward biased hence they are in conduction mode. The inductor voltage V_L equals to the capacitor voltage V_C and the inductor voltage is given by:

$$V_L = V_C \quad (3.11)$$

Generally, the voltage across an inductor is given by

$$V_L = L \frac{di_L}{dt} \quad (3.12)$$

Hence the inductor current i_L is given by

$$i_L = \frac{V_C}{L}t + I_{LV} \quad (3.13)$$

When the voltage across switch S is zero, the following mathematical equations are valid:

$$V_S = 0$$

$$i_S = i_L = \frac{V_C}{L}t + I_{LV} \quad (3.14)$$

The voltage across diodes D_1 and D_2 are given by:

$$V_{D1} = V_i - V_C \quad (3.15)$$

$$V_{D2} = -V_C \quad (3.16)$$

$$i_{D1} = i_{D2} = 0 \quad (3.17)$$

When the voltage between the switched boost network and H-bridge is zero

$$V_{dc} = 0 \quad (3.18)$$

$$i_{dc} = i_S = i_L = \frac{V_C}{L}t + I_{LV} \quad (3.19)$$

Then the capacitor current becomes:

$$i_C = -i_L = -\frac{V_C}{L}t - I_{LV} \quad (3.20)$$

When the voltage across switch S is not zero, the following mathematical equations are valid:

$$V_S = V_C - V_i \quad (3.21)$$

Then the current across the switch becomes zero.

$$i_S = 0 \quad (3.22)$$

$$V_{D1} = V_{D2} = 0 \quad (3.23)$$

$$i_{D1} = i_L = \frac{V_i - V_C}{L}t + I_{LP} \quad (3.24)$$

For state 1, i_{dc} equals to the current across the low pass filter inductor and for state 2, i_{dc} equals to zero, however the capacitor current is given by:

$$i_C = i_{D2} = i_L - i_{dc} = \frac{V_i - V_C}{L}t + I_{LP} - i_{Lf} \text{ for state 1,} \quad (3.25)$$

$$\text{For state 2, } i_C = i_{D2} = i_L - i_{dc} = \frac{V_i - V_C}{L}t + I_{LP} \quad (3.26)$$

3.3 Conclusion

Analysis and simulation of the proposed impedance source inverter known as Switched Boost Inverter has been investigated in this chapter. The mathematical analysis of the inverter to determine various components ratings has been done, also the two modes of operations of the Z source topologies has been verified. Two techniques (conventional PWM and Modified PWM) for inverter control was applied for simulation and the results generated in Figure 3.5 to Figure 3.6.

3.4 Switch Boost Inverter Controlled by PWM

In the switched boost inverter, the source or input voltage is increased by virtue of the shoot through mode but in the case of conventional VSI controlled by conventional PWM method, the shoot through mode is not applicable; applying the shoot through mode will result in the destruction of switches. Two method of PWM technique is applicable in the control of the switched boost inverter; a) conventional PWM (Xu, P., Zhang, X., Zhang, C. W., Cao, R. X., & Chang, L, 2006) and b) modified PWM. The conventional PWM control method's gate signal for the proposed switched boost inverter is shown in Figure 3.5. Four gate signals are generated because of the single H Bridge inverter; this done by comparing the four reference signals to the carrier signal (triangular) as shown in Figure 3.5. By summing the shoot through modes ($ST1 + ST2$), the gate signal of switch S in Figure 3.1 is generated. From Figure 3.5 it can be seen that each period of switching of the modulation method contains four shoot through modes; this means that there are four switching cycles for switches S and this can translate to higher losses due to switching and inconsistent frequency, the four reference signals are Ref_{s1} , Ref_{s2} , Ref_{s3} and Ref_{s4} .

The modified pulse width modulation technique's output waveform is shown in Figure 3.6. This technique is an improvement on the conventional PWM technique which is combined with UVS (unipolar voltage switching). Unlike the conventional PWM, the modified PWM switching cycles for switch S is limited to two for each period and the switching frequency is not variable but constant. In choosing the carrier signal, switching frequency f_s should very greater than the output frequency f_o .

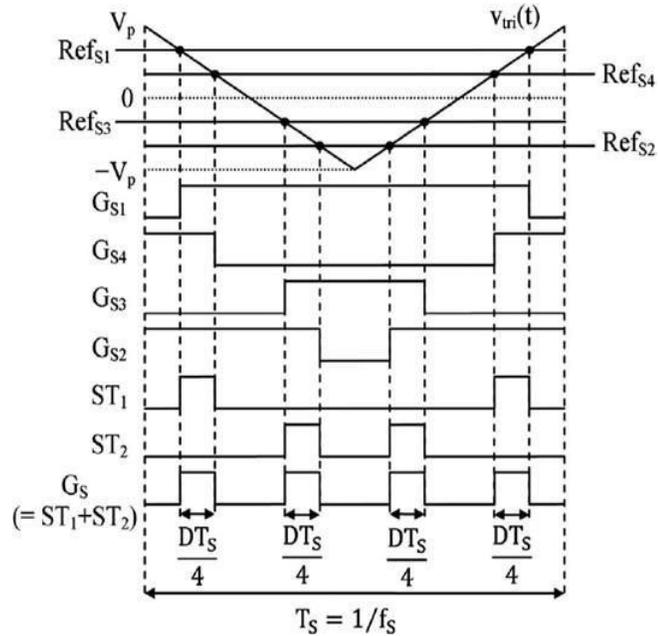


Figure 3.4.1: Conventional PWM control signals

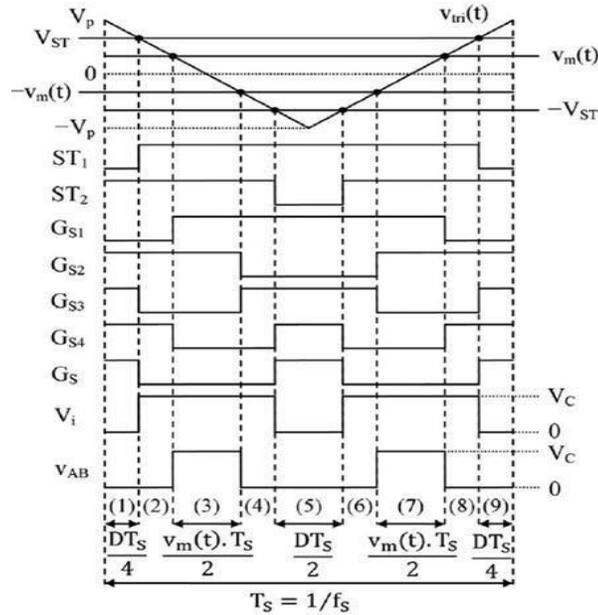


Figure 3.4.2: Modified PWM control signals

Comparison of triangular carrier signal (amplitude V_p) and sinusoidal reference signal is done to generate the gate control signals of S1 and S2. To generate the signals for the two shoot through modes ST1 and ST2, triangular carrier signal is compared to the positive and negative values of a constant amplitude value as shown in Figure 3.6. Other figures as associated with modified control method are shown below.

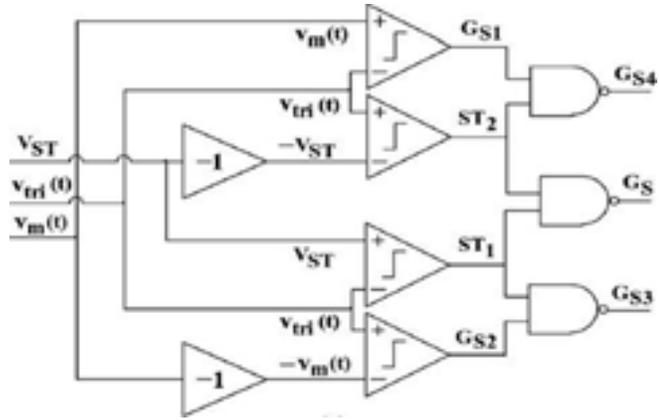


Figure 3.4.3: Control circuit of modified PWM

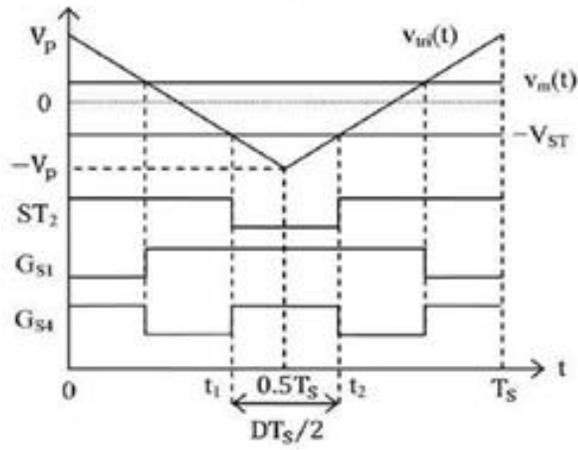


Figure 3.4.4: Shoot through waveform

3.5 Simulation Results

Simulation results for the two PWM techniques will be presented and comparison of switched boost inverter and conventional Z source inverter will be investigate. Changing the value of V_{ST} will lead a change in the duty ratio D of the shoot through mode as shown in Figure 3.6. The relationship between V_{ST} and D is given by (3.27). The output voltage waveform v_{AB} and the input voltage waveform V_i is shown in Figure 3.8. There are five inters for the output voltage, three of them are zero states and two are power states i.e. $v_{AB} = 0$ and $v_{AB} = V_C$ respectively. This occurs in one switching period and the five states occur in one switching cycle. The duty ratio D selection is necessary to overlap of the shoot through phase and power phase, expressions (3.28) to

(3.29) helps in resolving that. The parameters used for the simulation of the two cases of switched boost inverter are given in Table 1.

$$D = 1 - \frac{V_{ST}}{V_P} \quad (3.27)$$

$$\left[D \cdot T_S < T_S - \max\left(\frac{v_m(t) \cdot T_S}{V_P}\right) \right], D < 1 - M \quad (3.28)$$

$$M = \max \left[\frac{v_m(t)}{V_P} \right] \quad (3.29)$$

The maximum fundamental component of the output voltage expression is given by (3.30):

$$v_{AB} = M \left[\frac{1-D}{1-2D} \right] v_g = M \cdot V_C \quad (3.30)$$

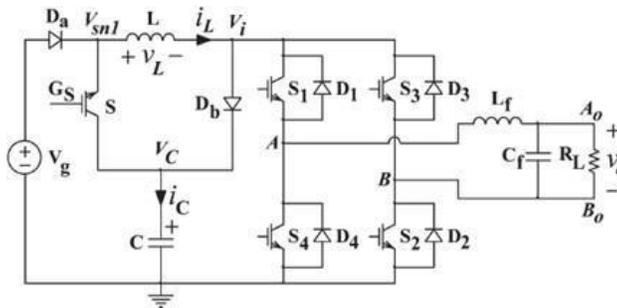


Figure 3.5.1: SBI circuit for simulation

Table 3.5.1: Simulation Parameters

Component	SWITCHED BOOST INVERTER	
	Conventional PWM	Modified PWM
Input Voltage V_i	64	64
Impedance inductor L	5.6mH	5.6mH
Filter inductor L_f	4.6mH	4.6mH
Impedance capacitor C	470F	470F
Impedance Capacitor C_f	10F	10F
Load resistor R_o	25ohm	25ohm
Switching frequency f_o	5kHz	5kHz
D_{Ref1}	0.8	0.8
D_{Ref2}	0.4	
$D_{V_{ST}}$	-	0.6
D_{V_m}	-	0.5

Simulation results for the first PWM method i.e. conventional pulse width modulation method as discussed in the above literature is shown below:

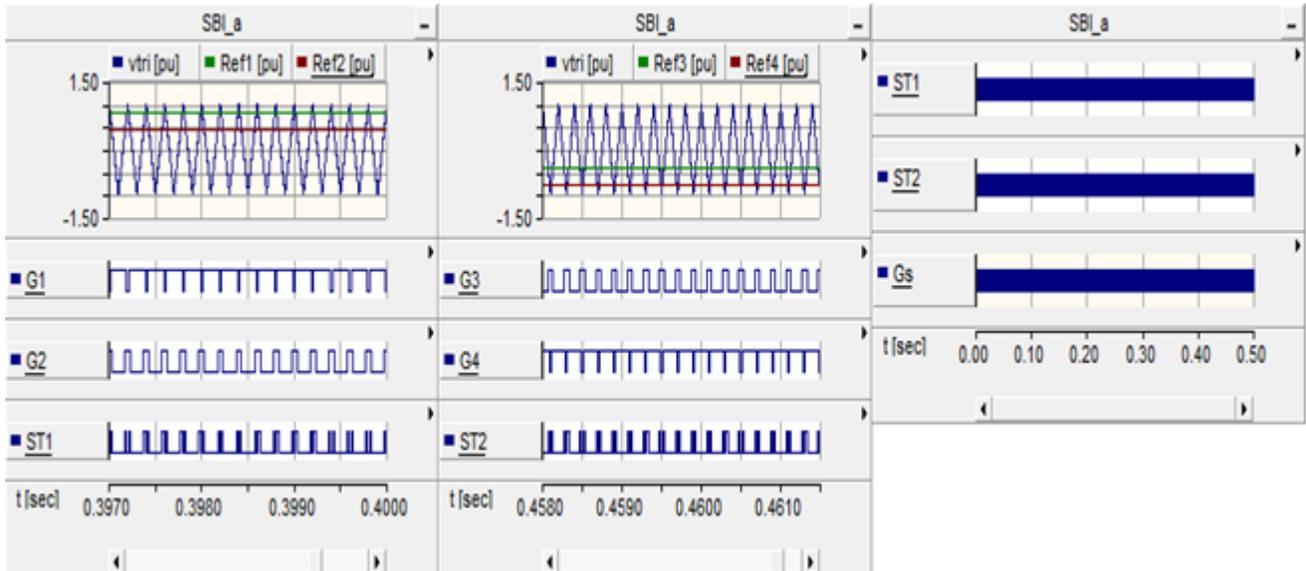


Figure 3.5.2: SBI circuit for simulation

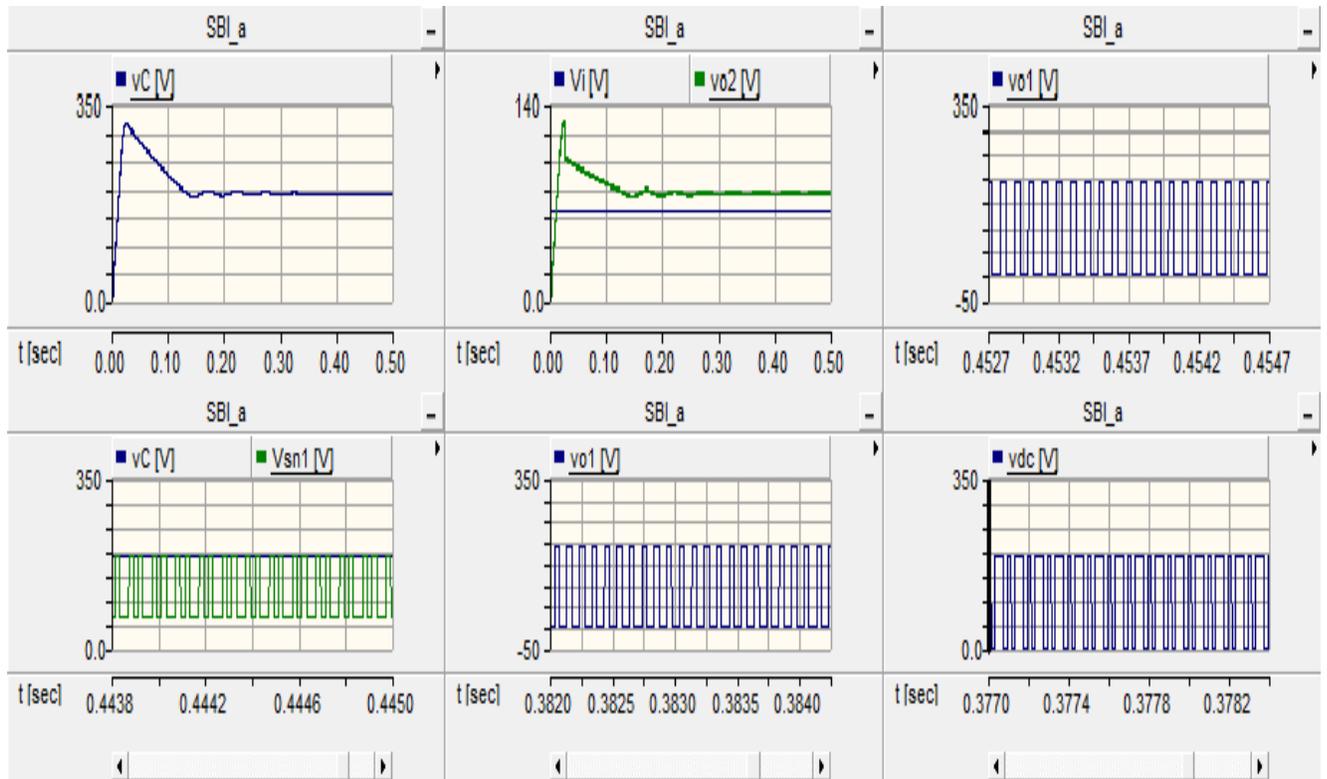


Figure 3.5.3: SBI circuit for simulation

Simulation results for the second PWM method ie modified pulse width modulation technique as discussed in the above literature is shown below:

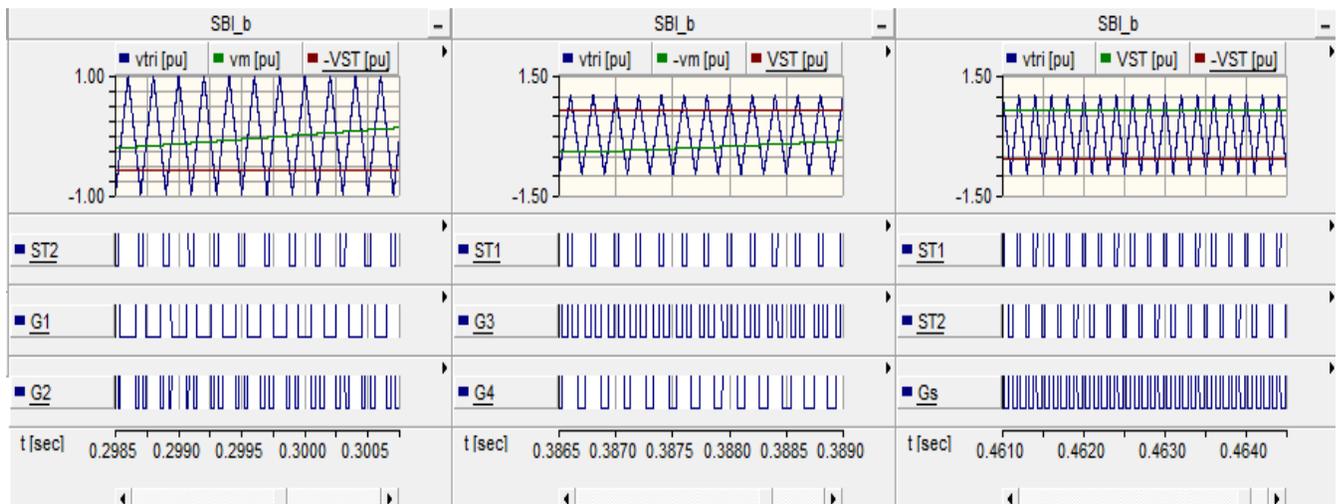


Figure 3.5.4: SBI circuit for simulation

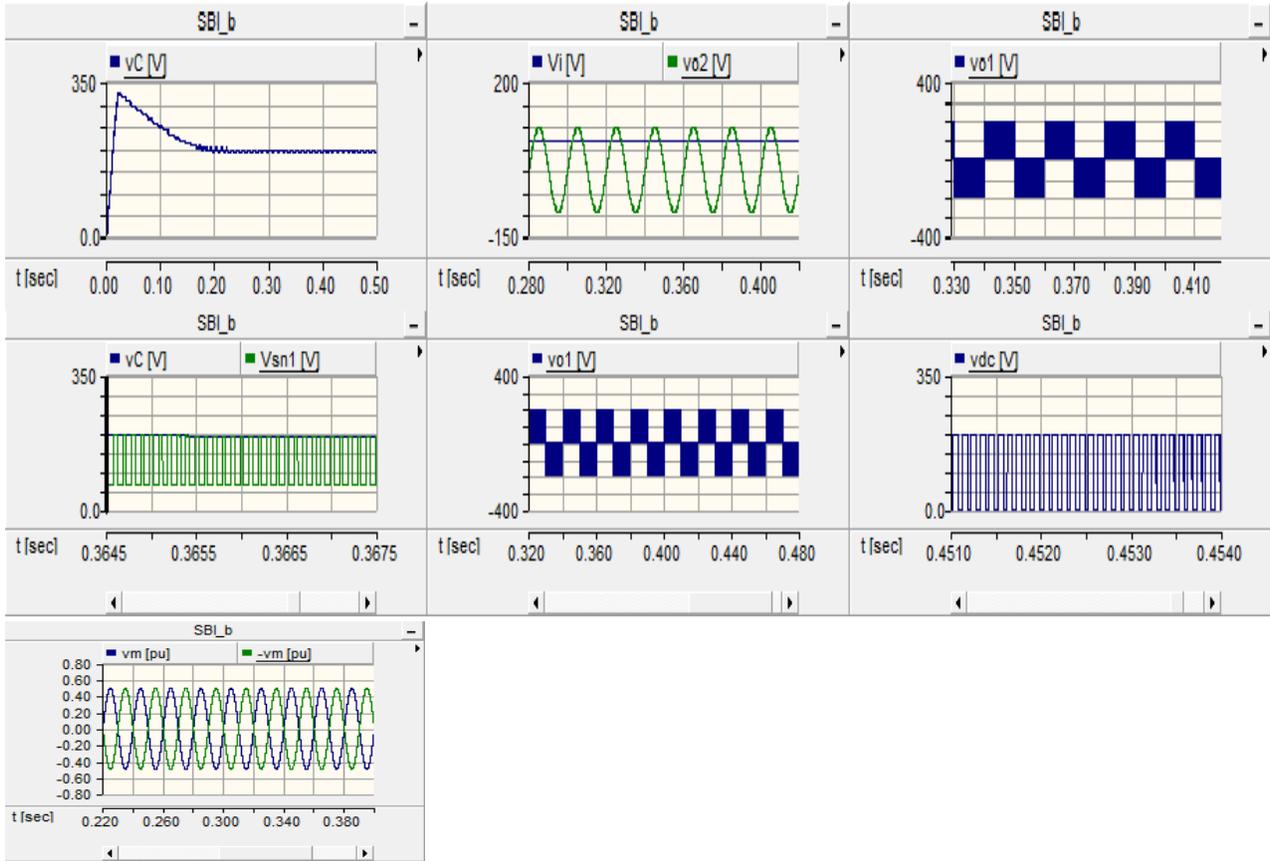


Figure 3.5.5: SBI circuit for simulation

Simulation results for the first PWM method i.e. conventional pulse width modulation method as discussed in the above literature is shown in Figure 3.10 and Figure 3.11. In Figure 3.11 the two reference signals (Ref1 and Ref2) output waveforms together with the control signals of gates G1 to G4 are shown. The carrier signal is given by v_{tri} . Also the shoot through states ST1 and ST2 together produces the control signal for gate G_s . Figure 3.11 shows the component voltage and current, the input and output voltage are also shown. The capacitor voltage and switch voltage are represented by v_C and V_{sn} , the source voltage and the inverter bridge input which is also the output voltage of the Z source network are given by V_i and V_{dc} respectively. It should be noted that $L_f C_f$ filter is connected at the output and V_{01} is the output voltage before the filter and V_{02} is the output voltage after the filter. Figure 3.12 and Figure 3.13 show the output waveforms for the second PWM method which is the modified PWM. The parameters of the graph for the two control methods are similar the difference lies in the carrier signal and the method for generating the various gate signals.

CHAPTER 4

CONCLUSION AND RECOMMENDATIONS

4.1 Conclusion

Voltage source inverters have wide areas of applications because the input is voltage source and it's suitable for many applications which require voltage source as the input. Variable or adjustable speed drives and FACTS devices are some major of the major applications areas of voltage source inverters. Although VSI can be applied to high power system, it's most suitable in medium power applications because they are able to generate output voltage with very high quality waveforms. The voltage source inverter also known as voltage source converter (when used for both inversion and rectifying purposes) has wide areas of applications but it's fraught with many limitations such: it's a buck or step down inverter that's the output voltage is always less than the input voltage unless a buck-boost converter is applied. When used as a rectifier, it's a boost rectifier circuit, applications of buck-boost converter in VSI topology increases the cost of the unit, reduces the efficiency of the system and complicated control technique is introduced, shoot through property is absent in VSI or CSI hence EMIs immunity is absent, inductor – capacitor filter is required to reduce power systems noises. Current source inverters have some limitations such as: the current source inverter is a boost inverter. and when applied as rectifier, it's a buck rectifier circuit, buck dc converters are required to reduce the cost hence, cost of system and efficiency increases and reduces respectively, Open circuit on a load side is a big problem when preventive measures are not taken and reverse voltage path should be provide or blocked.

The introduction of Z source or impedance networks into VSI and CSI topologies solves the problems of buck or boost quality depending on the structure and shoot through property of ZSI provides immunity to the effects of EMIs and boost the voltage gain proportions of ZSI based inverters. The conventional Z source based inverter solves major drawbacks of VSI and CSI but they also introduce some limitations such as increased cost and size hence they are not appropriate for use in low power systems when they following factors are off great concern; cost, weight and size.

The switched boost inverter topology (SBI) was introduced to solve the limitations of the traditional impedance source inverter (ZSI). Due to the sheer size of capacitor required in LC network of ZSI, the size, weight and cost of ZSI topology is significantly increased and low power systems are not appropriate areas for usage or application. The switched boost inverter is made up of two passive components; inductor and capacitor and two passive switch components; diodes and one active switch component; IGBT. SBI retains all the advantages of the traditional ZSI plus merits of reduced passive components in the SBI structure.

Comparing the SBI and ZSI topologies shows that the two topologies have similar mathematical equations except in the case of dc link voltage where the SBI's value is lower due to this equation $1 - D$. In the case of component count, SBI topology has reduced number of passive components but an increase in the active and passive switch components. Due to the introduction of the active switch component in the switched boost topology, the SBI can be viewed as an active realization of the ZSI topology. The total number of components in the two topologies are five each and but ZSI has one capacitor more than SBI hence the structure of SBI is minimized, the weight and cost of the structure is also reduced. Detailed explanations of components stress is done experimentally in (Ravindranath, A et al, 2013). Analysis and PWM control of switched boost inverter. IEEE Transactions on industrial electronics, 60(12), 5593-5602, (Mohan, N., & Undeland, T. M., 1995) where it's confirmed that SBI has lower peak voltage for the dc link hence the voltage stress on the inverter bridge components is less; the comparison was based on same input parameters for ZSI and SBI but the modulation index in SBI is much higher than that of ZSI. Also it's confirmed that the switch utilization ratio for the two topologies are almost same. Both ZSI and SBI are able to protect inverter bridge components in the advent of shoot through caused electromagnetic noise interference or short circuit faults; this advantage is lacked in VSI and CSI topologies. However, the SBI has some drawbacks when compared to ZSI; increased number of diodes and switches i.e. one diode and an extra switch is introduced in the SBI topology. Switching losses will increase the SBI due to the extra switch. More semiconductor switches means superior defense mechanism is required to protect the switches but current in the SBI topology is consistently limited due to the inductor. The dc link voltage $(1 - D)$ is also less in SBI topology; to achieve same dc link voltage levels as in ZSI topology, higher modulation index is required.

SBI topology was presented in this thesis and simulation done for two PWM control methods; conventional and modified. Comparison of SBI and ZSI was also investigated.

4.2 Recommendations

Although switched Boost inverter topology offers better boosting capabilities when compared conventional Z source inverter, the introduction of the active switch into the structure increases the cost of and losses the inverter. In the case of losses, conduction and switching losses are present in the SBI topology while only conduction losses are present conventional ZSI. The cost is increased also because the trigger circuit which is not required in the conventional ZSI. For future work, a detailed investigation of the two topologies ZSI and SBI should be investigated with reference to financial cost for a period of time to determine the best topology for practical applications.

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