ISEYAS TEKLAY MUSSA DESIGN AND ANALYSIS OF DC-DC MULTILEVEL BOOST CONVERTER NEU 2019

# DESIGN AND ANALYSIS OF DC-DC MULTILEVEL BOOST CONVERTER

**A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY**

**By**
**ISEYAS TEKLAY MUSSA**

**In Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical and Electronics Engineering**

**NICOSIA, 2019**

# DESIGN AND ANALYSIS OF DC-DC MULTILEVEL BOOST CONVERTER

**A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY**

**By**
**ISEYAS TEKLAY MUSSA**

**In Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical and Electronics Engineering**

**NICOSIA, 2019**

**ISEYAS TEKLAY MUSSA: DESIGN AND ANALYSIS OF DC-DC MULTILEVEL BOOST CONVERTER**

**Approval of Director of Graduate School of Applied Sciences**

**Prof. Dr. Nadire CAVUS**

**We certify that this thesis is satisfactory for the award of the degree of Master of Science in Electrical and Electronics Engineering**

**Examining Committee in Charge:**

| | |
|---|---|
| Prof.Dr. Ebrahim Babaei | Supervisor, Faculty of Electrical and Computer Engineering, University of Tabriz |
| Assist. Prof. Dr. Lida Ebrahimi Vafaei | Department of Mechanical Engineering, NEU |
| Assist. Prof. Dr. Parvaneh Esmaili | Department of Electrical and Electronics Engineering, NEU |

I hereby declare that all information in this document has been obtained and presented in accordance with the academic rules and ethical conduct. I also declare that, as required by these rules and conducts, I have fully cited and referenced all materials and results that are not original to this work.

Name, Surname: Iseyas Teklay Mussa
Signature:
Date:

## ACKNOWLEDGEMENTS

Firstly of all glory to everything, for all the unlimited kindness, support and loveliness made on me to accomplish my research work successfully. I would like to pass a million thanks to my supervisor and lecturer/EEE/NEU Prof.Dr Ebrahim Babaei for his marvelous ability of guidance, encouragement, patience and support to make the work more valuable and compatible. In addition, my appreciations are extend to the NEU that gave me a grateful opportunity to join the department of Electrical and Electronics Engineering with their well-equipped facilities and qualified faculty members to acquire more in-depth knowledge of the intended field of study and research ability.

At last but foremost, words are not sufficient to express my deepest sense of gratitude to my lovely parents and family members for their endless guidance, support and prayer that enables me to achieve my future career with full of willingness. They are highly rated people and always be respected in my sight. Special thanks to my close friends for their great inspiration, financial support and deep thoughts throughout my studies.

**To my parents…**

## ABSTRACT

The evolution of power conversion systems have been emerged, since nineteenth century. The need of high voltage DC-converters has showed expeditious growth over the past years for various applications, such as alternative renewable energy sources. Thus, the technological advancements in the demand of power supply significantly changed in the fields of power system and power electronics. DC-DC topologies are the foremost powerful methodologies of power converters. A boost converter (BC) is the most popular prototype of DC-DC converters practiced in different power electronics applications. The major objective of this modular research is to design and implement an adaptive multilevel boost converter (MBC), to provide a multiple output voltages by controlling and regulating the self-voltage balancing switch capacitors of the traditional BC based MBC with the help of PWM controlled single switch. The proposed alternative converter is mainly build up by integrating $2n-1$capacitors, $2n-1$diodes and a single inductor for $n$ times MBC. Another improvement of this paper is to introduce a new structure of MBC, with a central input voltage source to reduce the power consumption in the lower level. The fundamental function of the presented topology is to generate an optimal high voltage boost ratio, with a suitable low power rating devices to block and achieve one level of voltage at each stage. This topology is utilized as a DC-source for variety applications, like fuel cell systems and photovoltaic sources (PV) which operate at low power that needs unidirectional current and self-balanced controlled voltage levels, which is very useful in boosting the output before being inverted and grid connected. The vital merits of MBC are large boost gain at limited value of duty cycle, operating at steady continuous input current, no need of transformer and balanced output voltage, which enables to work the MBC at high switching frequency. The principle of the selected converter is simulated under various conditions, to prove the accuracy of the estimated equations and experimental results and demonstrate that the designed topology operates at its maximum acceptable voltage gain.



***Key words:*** Power conversion system; DC-DC boost converter; DC-DC multilevel boost converter; continuous conduction mode; discontinuous conduction mode; voltage gain.

## ÖZET

Güç dönüşüm sistemlerinin gelişimi on dokuzuncu yüzyıldan beri ortaya çıkmıştır. Yüksek voltajlı DC dönüştürücülere olan ihtiyaç, geçmiş yıllarda alternatif yenilenebilir enerji kaynakları gibi çeşitli uygulamalar için hızlı bir büyüme göstermiştir. Bu nedenle, güç kaynağı talebindeki teknolojik gelişmeler, güç sistemi ve güç elektroniği alanlarında önemli ölçüde değişmiştir. DC-DC topolojileri, en güçlü güç dönüştürücü teknikleri. Bir güç dönüştürücü (BC), farklı güç elektroniği uygulamalarında uygulanan en popüler DC-DC dönüştürücü prototipidir. Bu modüler araştırmanın asıl amacı, geleneksel BC tabanlı MBC'nin kendi kendine voltaj dengeleme şalter kapasitörlerini PWM kontrollü yardımıyla kontrol ederek ve düzenleyerek çoklu çıkış voltajları sağlamak üzere uyarlanabilir çok seviyeli bir güçlendirici dönüştürücü (MBC) tasarlamak ve uygulamaktır tek anahtar. Önerilen alternatif dönüştürücü esas olarak $n$ MBC için $2n-1$ kondansatörleri, $2n-1$ diyotları ve tek bir indüktörü entegre ederek oluşturulur. Bu yazının bir başka iyileştirmesi, düşük güç tüketimini azaltmak için merkezi bir giriş voltaj kaynağı olan yeni bir MBC yapısı sunmaktır. Sunulan topolojinin temel işlevi, her aşamada bir voltaj seviyesini bloke etmek ve elde etmek için uygun bir düşük güç derecelendirme cihazına sahip optimum bir yüksek voltaj yükseltme oranı oluşturmaktır. Bu topoloji, yakıt hücresi sistemleri ve fotovoltaik kaynaklar (PV) gibi çeşitli uygulamalar için, tek yönlü akım ve kendinden dengeli kontrollü voltaj seviyelerine ihtiyaç duyan düşük güçte çalışan ve daha önce çıktının arttırılmasında çok yararlı olan çeşitli uygulamalar için DC kaynağı olarak kullanılır ters ve ızgara bağlı. MBC'nin hayati değerleri, sürekli sürekli giriş akımında çalışan, transformatöre ve dengeli çıkış voltajına ihtiyaç duymayan, sabit anahtarlama devresinde, yüksek anahtarlama frekansında MBC'nin çalışmasını sağlayan yüksek güç artışıdır. Seçilen dönüştürücünün prensibi, tahmin edilen denklemlerin ve deneysel sonuçların doğruluğunu kanıtlamak ve tasarlanan topolojinin maksimum kabul edilebilir voltaj kazancında çalıştığını göstermek için çeşitli koşullar altında simüle edilmiştir.



***Anahtar kelimeler:*** Güç dönüşüm sistemi; DC-DC yükseltme dönüştürücü; DC-DC çok seviyeli güç çevirici; sürekli iletim modu; süreksiz iletim modu; voltaj kazancı.

## TABLE OF CONTENTS

**ACKNOWLEDGEMENTS**…….. i
**ABSTRACT**…… iii
**ÖZET**…….. iv
**LIST OF TABLES**……. Viii
**LIST OF FIGURES**……... ix
**LIST OF ABBREVIATIONS**……... xi

**CHAPTER 1: INTRODUCTION**

1.1 Motivation of the Research……... 1
1.2 Problem Statement……. 3
1.3 General Objectives and Aims…… 5
1.4 Research Approach……... 5
1.5 Expected Research Contributions……. 6
1.6 Thesis Outlines and Structure…… 7

**CHAPTER 2: LITERATURE REVIEW OF THE PREVIOUS FINDINGS**

2.1 Background Description of the Review…… 8
2.2 Convectional DC-DC Boost Converter (One-Level BC)…….. 11
2.2.2 Continuous conduction mode (CCM)…… 12
2.2.2 Critical conduction region……. 14
2.2.3 Discontinuous conduction mode (DCM)……... 15
2.3 DC-DC Multilevel Boost Converter…….. 17
2.3.1 Existing multilevel DC-DC boost converter…….. 17
2.3.2 Proposed DC-DC multilevel boost converter…… 19
2.3.3 Advantages of the Proposed Multilevel Boost Converters……... 19

**CHAPTER 3: RESEARCH DESIGN AND MODELING OF THE PROPOSED CONVERTER**

3.1 Two-Level DC-DC Boost Converter……. 20
3.1.1 Two-level DC-DC boost converter analysis in CCM…… 22
3.1.2 Two-level DC-DC boost converter analysis in DCM…… 24
3.1.3 Inductor’s equivalent series resistor (ESR) on the voltage gain of two-level

DC-DC boost converter……. 24
3.1.4 Evaluation of diodes and switch voltage drop effect on the two-level DC-DC MBC…….. 26
3.1.5 Design and description of the two-level DC-DC boost converter……. 28
3.1.6 Voltage stress on the switch in two-level DC-DC boost converter…….. 31
3.2 Three-Level DC-DC Boost Converter…….. 32
3.2.1 Three-level DC-DC boost converter analysis in CCM…….. 34
3.2.2 DC-DC three-level boost converter analysis in DCM…….. 35
3.2.3 The effect of the ESR on the voltage gain of three-level DC-DC BC…….. 36
3.2.4 The effects of diodes and switch voltage drop in three-level DC-DC MBC… 37
3.2.5 Design and analysis of the three-level DC-DC boost converter……... 38
3.2.6 Voltage stress on the switch in three-level DC-DC step up converter……. 43
3.3 DC-DC Four-Level Boost Converter…… 43
3.3.1 Analysis of the four-level DC-DC MBC in CCM……. 45
3.3.2 Analysis of the four levels DC-DC MBC in DCM…… 46
3.3.3 The Effect of the ESR on the voltage gain of four-level DC-DC MBC……... 46
3.3.4. Evaluation of the diodes and switch voltage drop effects on the four-level DC-DC MBC……. 48
3.3.5 Design of four-level DC-DC boost converter…… 50
3.3.6 Voltage stress on the switch in four-level MBC……... 51
3.4 DC-DC *n* -Level Multilevel Boost Converter (MBC)…….. 51
3.4.1 Analysis of *n* -level DC-DC MBC in CCM…….. 53
3.4.2 Analysis of *n* -level DC-DC MBC in DCM…….. 54
3.4.3 The Effect of the ESR on the voltage gain of *n* -level DC-DC MBC…….. 54
3.4.4 Diodes and switch voltage drop effects on DC-DC MBC……. 55
3.4.5 Design of the DC-DC *n* -level MBC……. 55
3.4.6 Voltage stress on the switch in DC-DC *n* -level MBC…….. 56
3.4.7 The efficiency and output voltage ripples of the DC-DC *n* -level MBC…….. 56
3.5 The Structure of the Dual-Level DC-DC BC with Central Voltage Source …… 59
3.5.1 Two-level DC-DC BC analysis with central voltage source in CCM and DCM…….. 60
3.5.2 The Effect of ESR on the boost ratio of two-level DC-DC boost converter

with central voltage source in CCM and DCM……. 61

3.5.3 Analysis of diodes and switch voltage drop effects in DC-DC dual- level boost converter with central voltage source…….. 61

3.6 Three-Level DC-DC MBC with Central Voltage Source……. 62

3.6.1 Three-level multiplier DC-DC converter analysis with CVS in CCM and DCM…….. 64

3.6.2 Investigation of diodes and switch voltage drop effects on three-level DC-DC boost converter with central voltage source…….. 65

3.7 DC-DC *n* -Level MBC with Central Voltage Source……... 66

3.7.1 Analysis of *n* -level DC-DC MBC with CVS in CCM and DCM…… 67

3.7.2 Diodes and switch voltage drop effects on *n* -level DC-DC MBC with CVS... 68

**CHAPTER 4: PROCESS CONTROL STRATEGY AND SIMULATION ANALYSIS**

4.1 Process Control Block Diagram…… 69

4.2 Simulation Results……. 69

4.2.1. Validation of the analyzed equations for first stage DC-DC boost converter…….. 70

4.2.2. Evaluation of the expressions accuracy for two-level DC-DC boost converter…….. 72

4.2.3 Verification of the results obtained for three-level DC-DC boost converter… 74

4.2.4 Estimation of the expressions accuracy for four-level DC-DC boost converter…….. 76

4.2.5 Validation of the equations for DC-DC dual-level boost converter with CVS……... 79

4.2.6 Verification of the obtained equations for three-level DC-DC MBC with CVS……... 81

**CHAPTER 5 CONCLUSIONS AND FUTURE SCOPES**

5.1 Conclusion……. 84

5.2 Future Scopes of the Work…… 85

**REFERENCES**…….. 86

## LIST OF TABLES

**Table 2.1:** Various boost topologies with voltage gain, voltage stress and specific Parameters……. 18

**Table 2.2:** High voltage gain, high efficiency DC-DC boost converter design requirements for high power application…….. 18

**Table 4.1:** Parameters of the single-stage DC-DC boost converter……... 70

**Table 4.2:** Designing Parameters for two-level DC-DC boost converter…….. 72

**Table 4.3:** Parameters of the three-level DC-DC boost converter……. 74

**Table 4.4:** Parameters of the four-level incremental DC-DC converter…… 76

**Table 4.5:** Specifications for DC-DC dual-level boost converter with CVS……. 79

**Table 4.6:** Specifications of the three-level DC-DC boost converter with CVS……... 81

## LIST OF FIGURES


**Figure 1.1:** PV Power controlling system block diagram for high level grid connected two-stage power conversion systems……. 2

**Figure 1.2:** Isolated against non-isolated DC-DC boost converters high level block diagram…… 4

**Figure 2.1:** Conventional DC-DC boost converter power circuit diagram……... 12

**Figure 2.2:** DC-DC one-level boost converter working mode circuit diagrams……... 12

**Figure 2.3:** Voltage and current waveforms for conventional DC-DC BC……... 13

**Figure 2.4:** Voltage gain against duty cycle for convectional BC……. 14

**Figure 3.1:** Two-level DC-DC boost converter circuit diagram…… 20

**Figure 3.2:** DC-DC dual-level boost converter on/off mode circuit diagrams…….. 21

**Figure 3.3:** Voltage and current waveforms of DC-DC dual-level boost converter…. 22

**Figure 3.4:** Three-level DC-DC boost converter circuit diagram…….. 32

**Figure 3.5:** Power circuit diagram of the three-level DC-DC boost converter for on/off modes…… 33

**Figure 3.6:** Voltage and current waveforms for three-level DC-DC boost converter... 34

**Figure 3.7:** Voltage ripple waveforms for capacitors ($C_1, C_2, C_3, C_2'$ and $C_3'$) and output voltage…….. 42

**Figure 3.8:** Four-level DC-DC MBC circuit diagram…… 43

**Figure 3.9:** Circuit diagram of the four-level DC-DC MBC for on/off modes……..... 44

**Figure 3.10:** Voltage and current waveforms of the four-level DC-DC MBC…….. 45

**Figure 3.11:** Four-level MBC boost ration variation curve against operating duty cycle for different values of $\frac{R_{ESR,L}}{R}$ ……. 47

**Figure 3.12:** Power circuit diagram for DC-DC $n$-level MBC……. 51

**Figure 3.13:** Voltage and current waveforms of the $n$-level DC-DC MBC…….. 52

**Figure 3.14:** Efficiency against duty cycle for ($n$=4) MBC of figure 3.8…… 57

**Figure 3.15:** Efficiency versus output power for ($n$=4) MBC of figure 3.8……. 58

**Figure 3.16:** Two-level DC-DC boost converter circuit diagram with CVS……. 59

**Figure 3.17:** Two-level DC-DC boost converter with CVS circuit diagram for on/off modes……. 60

**Figure 3.18:** Three-level DC-DC MBC circuit diagram with central voltage source… 63

**Figure 3.19:** Three-level DC-DC BC with a central voltage source for on/off

modes……. 63
**Figure 3.20:** Power Circuit diagram for $n$-level DC-DC MBC with CVS……... 66
**Figure 3.21:** Voltage and current waveforms of $n$-level DC-DC MBC with CVS….. 67
**Figure 4.1:** Proposed converter process control block diagram……..... 69
**Figure 4.2:** Voltage and current output waveforms for DC-DC conventional BC…... 70
**Figure 4.3:** Inductor voltage and current waveforms for one-level boost converter…. 71
**Figure 4.4:** Switch voltage waveform for one-level DC-DC boost converter…….. 71
**Figure 4.5:** Voltage and current output waveform for two-level DC-DC MBC…… 72
**Figure 4.6:** Capacitors ($C_1$ and $C_2$) voltage waveforms for two-level DC-DC MBC… 73
**Figure 4.7:** Inductor Voltage and current waveforms for two-level DC-DC MBC….. 73
**Figure 4.8:** Switch voltage waveform for dual-level DC-DC step-up converter…….. 74
**Figure 4.9:** Voltage and current output waveforms for three-level DC-DC MBC…… 75
**Figure 4.10:** Capacitor ($C_1$ to $C_3$) voltage waveforms for three-level DC-DC MBC… 75
**Figure 4.11:** Inductor voltage and current wave forms for DC-DC three-level MBC... 76
**Figure 4.12:** Switch voltage waveform of DC-DC three-level boost converter…… 76
**Figure 4.13:** Voltage and current output waveforms for four-level DC-DC MBC…... 77
**Figure 4.14:** Capacitors ($C_1$ to $C_4$) voltage waveforms for DC-DC four-level MBC…. 77
**Figure 4.15:** Inductor voltage and current waveforms for DC-DC four-level MBC…. 78
**Figure 4.16:** Switch voltage waveform for four-level DC-DC boost converter…… 78
**Figure 4.17:** Voltage and current output waveforms for two-level MBC with CVS.... 79
**Figure 4.18:** Capacitors ($C_1$ and $C_{-1}$) voltage waveforms for two-level MBC with CVS…… 80
**Figure 4.19:** Inductor voltage and current waveforms for two-level MBC with CVS…… 80
**Figure 4.20:** Switch voltage waveform for two-level MBC with CVS……. 81
**Figure 4.21:** Voltage and current output waveforms of the three-level MBC with CVS…… 82
**Figure 4.22:** Voltage waveforms of ($C_1$, $C_2$ and $C_{-1}$) for three-level MBC with CVS… 82
**Figure 4.23:** Inductor voltage and current waveforms for three-level MBC with CVS……... 83
**Figure 4.24:** Switch voltage waveform for three-level DC-DC MBC with CVS…….. 83

## LISTS OF ABBREVIATIONS

| | |
|---|---|
| **AC:** | Alternative Current |
| **BC:** | Boost converter |
| **CVS:** | Central Voltage Source |
| **CCM:** | Continuous Conduction Mode |
| **DC:** | Direct Current |
| **DCM:** | Discontinuous Conduction Mode |
| **ESR:** | Equivalent Series Resistance |
| **HVDC:** | High Voltage Direct Current |
| **MPPT:** | Maximum Power Point Tracking |
| **MBC:** | Multilevel Boost Converter |
| **PV:** | Photovoltaic |
| **PE:** | Power Electronics |
| **PWM:** | Pulse Width Modulation |
| **VSC:** | Voltage Source Converter |

# CHAPTER 1
# INTRODUCTION

This chapter mainly deals with the system development of research motivations, problem description, basic objective, research approaches, work contributions, literature survey and the organizations of the system.

## 1.1 Motivation of the Research

During this era all the power electronics (PE) controlled technologies need a utilized power conversion control strategy, to convert energy from one source to another source. The transfer of power from the input to the output side is manipulated by selecting an appropriate semiconductor device controlled converter, which is capable of operating at high frequency to maintain optimal required voltage. The fast growth of electronic equipment and devices operating separately or in combination to convert electric energy efficiently, made power electronics to be more applicable in broad areas compared to another engineering fields. As a result the field of PE got a great interest by the global energy conversion system for integrating smart grids with main distribution generations to provide quality power control and upgrade the efficiency of power to satisfy the demand of energy requirement (Elbuluk and Da Silva, 2013).

According to the world global energy system in the current years our world is experiencing electric power crises as a result of high demand of energy consumptions. This is caused due to the fast diminishing of fossil-fuel sited convectional power supply systems and the rapid increase of electric energy based technology advancement. Therefore, significant researches have been developed to solve this issue. The possible feasible solutions are to develop an effective renewable power generations, advanced power conversion control systems and enhancement the efficiency of current power generation. Even though, a lot of power converters have been developed, still an improvement is required in the existing converters due to their low efficiency, high cost, low switching frequency and low voltage gain. For example, renewable energies like PV systems, wind turbine and full-cell generating low voltages need a high voltage converting device before inverting to AC source connected to the main grid of the system (Mudliyar, 2013) as indicated in Figure

1.1. Because, these types of energy sources are clean, more feasible and practically accepted their application is more fame through worldwide. Such, energy systems generate variable low voltages; as a result a stabilized DC-DC step-up converter is required to produce a stable output. In addition, high voltage DC-DC converters increases the number of output voltage levels and reduces the output current, thus power loss are minimized.

In general, there are two groups of DC-DC step-up converters, the isolated and the non-transformer converters. Isolated converters usually applicable in areas where, an intermediate medium frequency operated transformer is required between the input and output power sides for especial safety purpose. There are a number of such topologies have been evolved with high voltage gain, but their application is limited to certain areas due to their low efficacy and output stability (Mademlis, 2015).

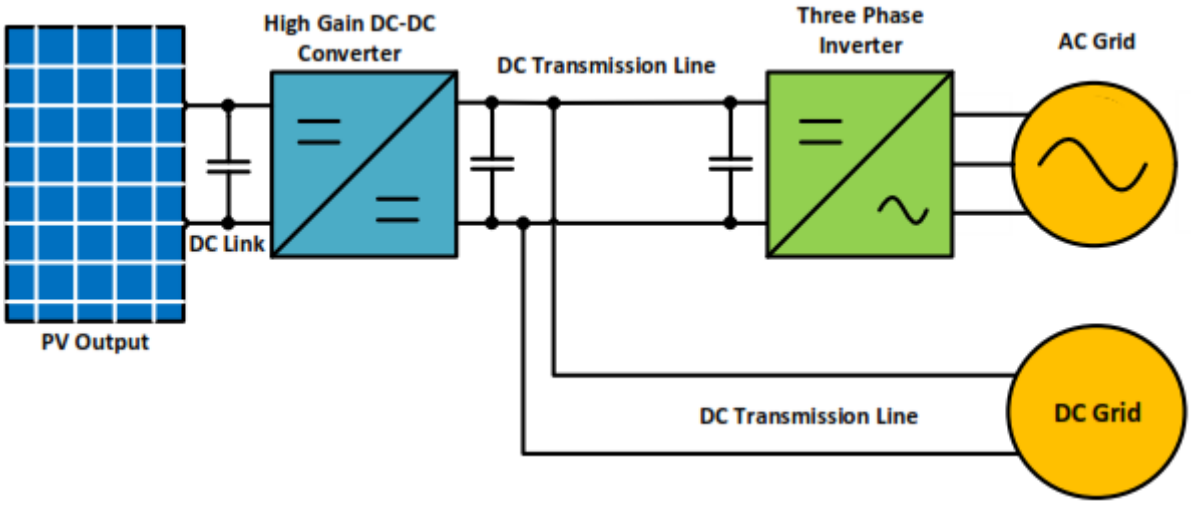



**Figure 1.1:** PV Power controlling system block diagram for high level grid connected two-stage power conversion systems

In contrast, the boost ratio of the traditional DC-DC non-isolated converters is not much higher for these types of applications, due to their high value of parasitic capacitors and inductors which likely limits the boost ratio. Consequently, transformer-less multilevel boost converter with higher voltage gain, large efficiency and flexible performance can be performed with convectional step-up converter as its base structure (Soman, 2017). This can be done, by upgrading the convectional converters and introducing new topologies of converters with high switching frequency, low cost, better efficiency, minimized size,

reduced weight and optimal boost ratio. Multilevel converters are some of the few advancement topologies emerged in 21 century with multiple output and maximum power ratio (Rosas and Martin, 2008). Therefore, DC-DC multilevel boost converters (MBC) are pulse-width modulation (PWM) technique controlled DC-DC converters, which integrates the traditional step-up converter with the voltage switched capacitors to generate various voltage output levels as well as a self-balanced voltage using a single switch, $2n-1$ capacitors, $2n-1$diodes and one inductor for any desired MBC stage ( Peng et al., 2008).

## 1.2 Problem Statement

As energy conversion system is a wide area of PE fields and power derives, it is applicable for different sectors, such as research development, industrial, communication technologies, computer applications, transportation and renewable energy connected system. As a result the discovering of new topologies is today's trendy issue. In practical applications, power conversion techniques are divided in to four topologies named as rectifiers, inverters, DC choppers and AC-AC (Rashid , 2001). Based on the proposed research objectives this study is mainly focused on DC-DC boost converters. According to their functions, applications, designing system and characteristics there are a considerable number of isolated and non-isolated DC-DC step-up converters have been discovered yet, as the general block diagram layout of these family converters is illustrated in Figure 1.2. However, due to their technical features and large demand in power conversion system the need of DC-DC prototypes rather than AC power supply markets increased rapidly. Thus, the requirements of low and high voltage power density in electronics industry become more. As transformers do for AC power conversion system, researchers spent much time to find an easy solution for converting one DC source to another DC voltage source with very high efficiency and voltage gain. Semiconductor devises like capacitors, inductors, which has a high capability of energy storing with high on-off switching frequency promises researchers to convert DC source to much higher power stages (Luo and Ye, 2004).

In convectional AC distributions and transmission systems the conversion of power is done by using step up or step down transformers. For example, a single-phase electric system with an input source of 220V line voltage has a two-phase of power structures requires a step-up grid connected inverter to get an output voltage of 380V high. An improved high

voltage ratio is obtained in isolated transformer connected converters while increasing the turn ratio in the transformer. This type of system needs large size of transformer and generates high harmonic distortions, thus the cost of the system increases (Shephed, 2004). However, at this time with the fast increase of renewable energies, the above mentioned power conversion system is becoming less effective, for such system with much lower power generating source, like PV panels. Since, the output voltage of most PV cells varied from 20V to 50V, a high boost ratio DC-DC boost converter is required at the output side of the cells. Usually, almost for all convectional step-up topologies when the output voltage gain increases much higher, the duty cycle increases close to unity. As a result, the ripple current of an inductor, ripple voltages of the capacitor become higher and a high current turning-off power electronic device is needed. Thus, there is an increase in conduction losses, harmonic distortions, switching losses and very low power factor which results in low efficiency. Although, the above mentioned DC topologies brought a solution, still the demand of high amount of voltage ratio is not solved due to low switching frequency, low efficiency and power losses.

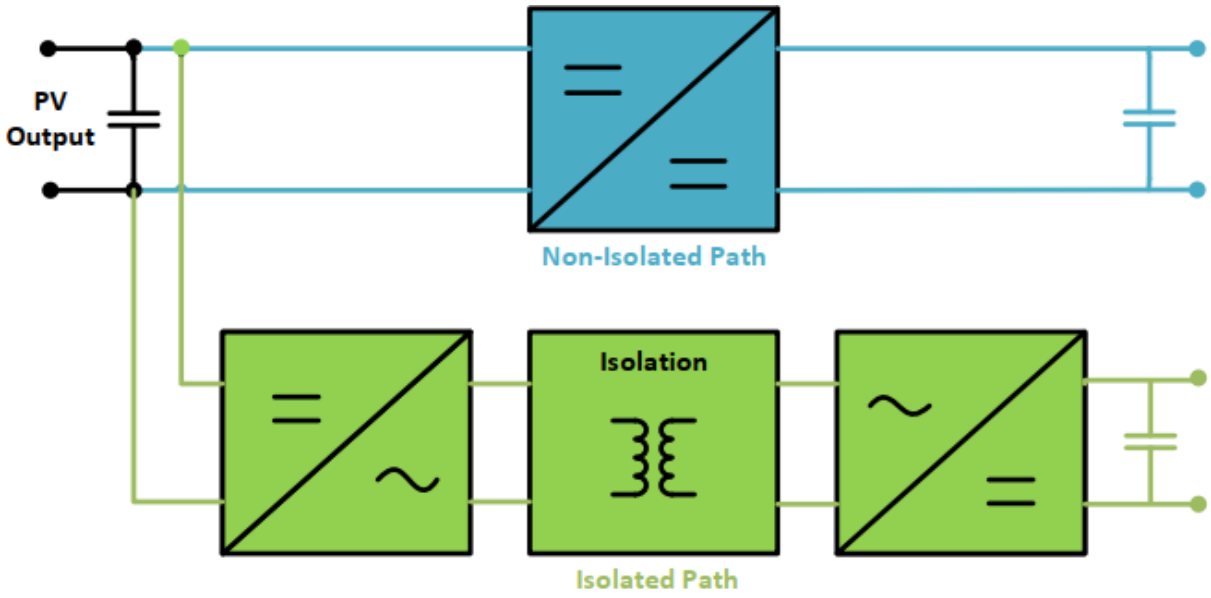



**Figure 1.2:** Isolated against non-isolated DC-DC boost converters high level block diagram

Therefore, the drawbacks of convectional converters is replaced by multilevel converters models, which are highly practiced in areas such as, renewable power systems rating at high power and voltage. The superior advantages of multilevel converters are minimum

harmonic distortion, improved power quality, low switches voltage stress, maximal boost ratio, high switching frequency, simple control structure and better efficiency (Qin, 2016). The principle of designing the proposed converter to overcome the desired solution can be viewed in two phases. The first phase is analyzing and designing a MBC with a voltage source at its base. In this, topology the existence of higher current in the lower stage semiconductor devices leads to consume more power than upper level. This limitation can be minimized by manipulating a variable MBC levels with voltage source at its central position as second phase. The implementation is designed by integrating less number of passive components a with suitable low power rating semiconductor devices. The significance of the proposed topology is to maintain a balanced output voltage levels required by the HVDC power transmission system and suitable AC-grid connected DC-link source, for high-power PV applications by improving better boost ratio and efficiency. A typical high voltage multilevel DC-link converter connects the two phases of DC/DC and DC/AC with the grid as shown in Figure 1.1.

## 1.3 General Objectives and Aims

The major objective of this modular research is to design, analyze, investigate and implement an advanced multilevel boost converter (MBC), in order to improve a large voltage conversion gain for high-power PV applications, to provide a desired balanced multiple output voltages at the HVDC power transmission system and to be served as suitable DC-link source for grid connected AC inverters. The modeling strategies are based on the traditional DC boost converter principles, to built-up $n$ level MBC by integrating, controlling and regulating the self-voltage balancing switch capacitors, without altering the fundamental structure of the basic converter. The aim is to overcome the drawbacks of limited boost ratio related with the low level power stages due to their parasitic losses and increased value of duty cycle. Thus, the overall target is to achieve an optimal high voltage gain and efficiency.

## 1.4 Research Approach

The designing system of this new topology is a combination PWM controlled DC-DC fundamental boost converter and voltage switching capacitors to achieve a high voltage

ratio. The structure of this prototype is built up based on the number of high value boost levels required, by integrating DC input voltage source, $2n-1$capacitors, $2n-1$diodes, one inductor and one switch without altering the principal circuit of the traditional step-up converter. The modeling approach of this proposed converter can be viewed in two main comparative converters of similar design; the lower base voltage source based $n$ times MBC and central-voltage source based $n$ times MBC. The main heart of this work is its controlling scheme, the overall system is utilized using only one high frequency operating switch with low loss controlled by PWM. This controlling strategy has an immediate relation with input current and output voltage. By controlling the duty cycle of the controlling signal the input current is controlled to improve high value of variable output voltages. Further, the validity of the investigated calculations is simulated using PSCAD software method. As a result, controlling the switching frequency and the duty ratio of the MBC a high voltage gain is achieved.

### 1.5 Expected Research Contributions

In, practical applications there have been a lot of DC-DC boost converters families discovered for high voltage conversion systems. In most cases as the conversion ratio increases their duty cycle also increase close to unity with low switching frequency, as a result switch loss and power loss increase which let to decrease the total efficiency. Furthermore, some other related MBC due to their limited voltage gain, unbalanced output voltage and the number of more switches used their efficiency is not much as required for high power applications. All these drawbacks could be solved by the newly proposed MBC by increasing the number of levels using PWM controlling system. Initially, the mathematical equations and graphical representations for current and voltage for all components are being analyzed according the performance of the desired power circuit of the converter. In addition, to investigate the impact of the parasitic loss and semiconductor voltage drops on the boost ratio. Moreover, to verify that, the outputs of the simulations, practical implementation and theoretical experiments will be exactly the same. In general to prove that, the output current is decreased while the output voltage is increased for any stage of the designed MBC. Consequently, the value of the duty cycle will be limited to the

required level which allows the converter to operate at very high switching frequency and the voltage gain of the converter is achieved better.

## 1.6 Thesis Outlines and Structure

The organization of this thesis is arranged mainly in to five chapters:

**Chapter-1:** The first chapter is entirely focused on the introduction part exploring the motivations of the work, problems of the research, general objectives and scopes, how the performance of the research is approached, expected contributions, achievements and the thesis outlines how the work is handled.

**Chapter-2:** In this chapter a comparative literature review is discovered on the previous proposed topologies with similar design, functions and application area related to the study of this research paper. The demerits, positive sides, their characters, significance, differences, similarities and their performance are analyzed and compared to take measurable investigation useful in designing the system of the work. In addition the general background explanations of DC-DC boost converters, existing MBC and brief narration of the proposed MBC are also studied in this chapter.

**Chapter-3**: The modeling and designing approaches of the proposed converter are analyzed and assessed in this chapter, for MBC with base voltage source and central-voltage source.

**Chaptr-4:** The simulation analysis and control strategies for verifying the validity of the practical assessment and the derived expressions.

**Chapter-5:** At last, system based conclusions of the research, recommendations and suitable possible corrective future scopes of the work are presented.

# CHAPTER 2
# LITERATURE REVIEW OF THE PREVIOUS FINDINGS

The limitations of convectional DC-DC converters performance and designing system as well as some of the MBC for achieving large voltage gain and efficiency have been studied in many research works in different ways, in which the contribution of many of these researches is mostly targeted to renewable energy sources and related applications are stated in (Balakrishnan et al., 2013); ( Dam and Mandal, 2018); (Chan and Masri, 2014); (Rai et al., 2012) and ((Rasheed et al., 2016). Subsequently, this chapter will try to figure out the literature review of the previous findings, so far contributed similar to the topic of the research dissertation.

## 2.1 Background Description of the Review

The popularity of DC power system for boost converters has got more attention in both static and dynamic electrical applications. It is a motivated factor to develop further advanced high level power electronics DC boost converters in the last 20 years as clearly revised in (Monem et al., 2013). Especially, with the diminishing of the convectional electrical sources of energy, fast growth of the demand of power supply and the gradual increase of the alternative renewable energy sources, such as PV systems with fluctuating low power, the need of large boost ratio converters is highlighted. Therefore, there have been many new step-up converters discovered including the traditional one, to decrease the losses, reduce the converter size and minimize the cost, as a result to upgrade the voltage gain and the total efficiency. Today, it is estimated that the advancement in the evolution of the DC-DC high level boost converters stepped up huge transformation, resulting in reliable, more lightly and effective power conversion system is in use (Misoca, 2007).

Everyone can agree that, it is one of the greatest achievements occurred in the world in the past century, the radical growth of DC-DC converters for variety applications of power conversion topologies to boost a voltage varying from low to high power levels that opens the road to the development of multilevel converter. The comprehensive case study investigated the evolution of DC-DC step up converters form the past until the present was

first introduced in ((Forouzesh and Lehman, 2017). The essence of the study mainly focused on the analysis of different techniques of DC-DC boosting topologies to gather information on how these converters are made, what components are needed and how energy is controlled based on their features and voltage rating technique. In this paper, a comparative study was made to get their similarities, difference, advantages and drawbacks based on their power density, efficiency, cost, reliability and complexity.

Researchers also tried to investigate and develop an advanced high level DC-DC step-up converter other than convectional one for extra high voltage applications. A modified DC-DC boost converter is a typical example designed to generate up to 400V with an external controller as proposed in (Sanjeevikumar and Rajambal, 2008). This type of converter requires large number of inductors to store energy and each inductor needs its own diode to block the revers current from the switch. In addition, an external control algorism, large duty cycle nearer to unity, huge value of capacitor for charging purpose are required and only operates in continuous conduction mode. Thus, its application is only limited to specific high power conversion applications.

Some of the non-isolated high voltage-gain DC-DC boost converters with an improved efficiency for PV cell applications are designed using more than two clamped circuits. This, type of converter used several inductors with high turn ratio in parallel, more than two switches, capacitors, voltage multiplier at the output side to get high voltage gain, as clearly analyzed in (Almousa et al., 2016). However, due to its large number of conducting modes, increased switch loss and its complex design, it is less economical and can operate to some limited high voltage levels. The efficiency and designing system of the current multilevel topology is compared and analyzed relatively to the various branches of traditional boost converter, cascaded step-up converters based on their size, weight, cost and simplicity in which the MBC outweighs most as discovered in (Kumar, 2017) for high power applications. A non-isolated three-level step up converter was also designed for PV cell systems to generate high voltage with improved efficiency, low inductor size using voltage balancing capacitors. However, this type of converter requires an external voltage and current sensing controller for balancing capacitor voltage and the duty cycle to monitor the MPPT. Thus, due to its complexity, large size, more switch stress, the need of external

controlling algorism and its application is limited up to three-levels, this topology is not suitable to the more high level voltage PV power systems as presented in (Balakishan et al., 2015).

The need of high voltage conversion system not only limited for renewable energy source generating applications, but also it is very interesting issue for regenerative braking (both in electric and hybrid vehicles) applications ,such as elevators, cranes and railways. These applications require a high power during braking time and traditionally use many batteries or capacitors in series to attain that energy for a short period of time. However, such technology is not economical, due to its luck of control system, large size and low efficiency. A cascaded multilevel DC-DC converter promises that will replace the above mentioned drawbacks with reduced weight, size and increase efficacy operating at high frequency with a simple controlling system by connecting supercapacitors in series to achieve high power as briefly state in (Miracle et al., 2013). Although, this type of design brought some solution, yet it has some disadvantages, since it uses more number of HB convertors with multiple input source and needs a separate control for voltage and energy balancing system that leads to increasing loses and reduction of efficiency.

Another family of multilevel converter was developed for high voltage applications, such as VSC and HVDC converter systems using steady state analysis technique. Even though, it solves some of the drawbacks of the low level DC converters, traditional converters and is applicable to several levels with high voltages and high efficiency, it has its own limitation. The system needs more number of switching devices, complex designing and analyzing system, low switching frequency, requires carful investigation on calculations due to inaccurate result errors. As a result the above mentioned factors makes it more complex, increases harmonics and high costive as investigated in (Song et al., 2013). MBC aren’t only useful for PV application but also extended to industrial and transportation systems. For example a capacitor clamped DC-DC MBC with high efficacy, minimum size and capable of resisting high temperature, was designed for industrial automotive applications (Cao et al., 2013). In this literature review the aim is to investigate and analyze the disadvantages of the previous present related finding with high size, power loss, low efficiency and low power density which is applicable only for low power

traditional capacitor clamped DC-DC. In this paper, the author tried to achieve the desired goal using overdamped and underdamped strategies to get large conversion ratio. However, the use of a large number of switches and high capacitance value in designing scheme makes the topology very costive, complex design and control system.

To achieve a very large boost ratio in traditional boost converters, a high value of duty cycle nearer to one is required that leads to low switching off time with a high current ripples and more power losses as shown in Figure 2.4. In addition, the influence of voltage stress on the switches and diodes also affected directly, as the output voltage ripples increases. As a result, to design a high quality utilized DC-DC step-up converter is an essential aspect in a high power system applications, such as renewable energy source. High voltage renewable energy systems are characterized by their own distinct features of having, high boost ratio, large efficiency, limited duty cycle, low loss and being non-transformer circuits (Khazaei et al., 2016). Therefore, the objective of this research is to solve the revised drawbacks of the above mentioned topologies.

### 2.2 Convectional DC-DC Boost Converter (One-Level BC)

A step-up DC-DC converter is used to generate a much higher output voltage with a low value of input voltage, in which a constant regulated DC voltage is required for various applications. Conventionally, using a battery cells or others DC sources in series to enhance a large voltage is not economical due to its high cost, large space and low efficiency. In contrast, the use of magnetic field of an inductor and capacitors to story energy temporary and release are more effective in high switching boost converters with low loss and ripples. Thus, a boost converter with a low inductor's series resistance is preferred to obtain better voltage gain and directly controls the input and output ripples of both current and voltage (Thomas, 2014). The power circuit of a convectional DC-DC boost converter is shown in Figure 2.1. The working principle of this converter can be divided into two modes. The first mode starts by turning on the switch $S$ at the moment $t = 0$ until $t = DT$. In this mode, the flow of the current passes through the inductor $L$ and the switch $S$. The second mode starts when the switch $S$ is turned off at the moment $t = DT$, which is the duration of the diode $D$ being switched on to a switching time $T$. The current that had passed through the switch $S$ now passes through the inductor $L$, diode $D$, capacitor

$C$, and load resistance $R$. The current of inductor $L$ in this mode begins to decrease, so that the switch $S$ turns on in the next period of time. In this mode, the stored energy in the inductor $L$ is transmitted to the load resistance $R$.

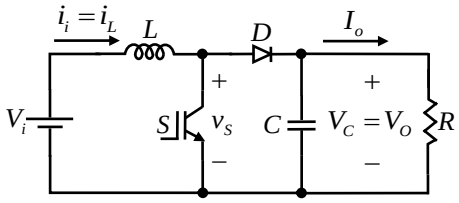
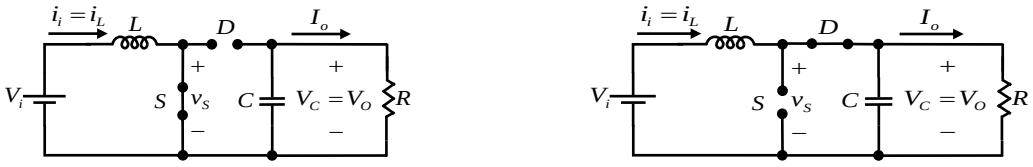



**Figure 2.1:** Conventional DC-DC boost converter power circuit diagram

For the conventional DC-DC boost converter, there are three modes of conduction, namely continuous conduction region, critical conduction region and discontinuous conduction region.

### 2.2.1 Continuous conduction mode (CCM)

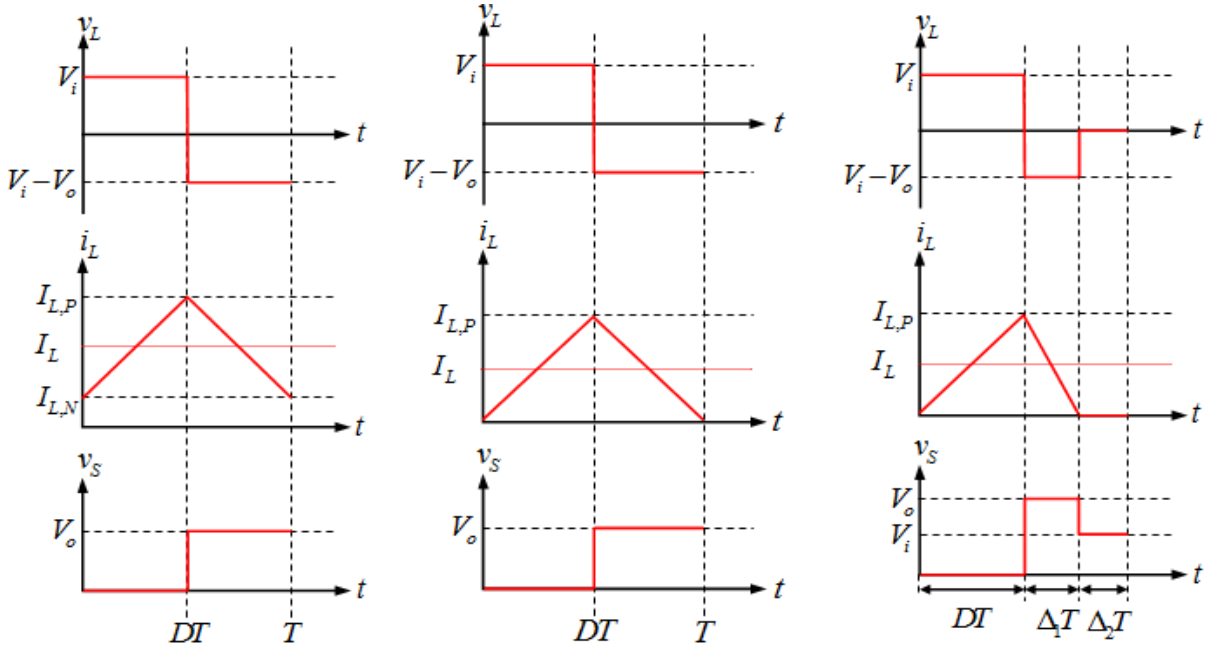
This mode itself is sub divided in to two modes. The equivalent circuits for the first and second working modes in the continuous conduction region are shown in the Figure 2.2.




(a) First mode (b) Second mode

**Figure 2.2:** DC-DC one-level boost converter working mode circuit diagrams

The waveforms of the voltages and currents for convectional DC-DC boost converter are shown in Figure 2.3(a), for a continuous load current.




(a) CCM (b) Critical conduction region (c) DCM

**Figure 2.3:** Voltage and current waveforms for conventional DC-DC boost converter

According to Figure 2.3(a), the inductance current $i_L$ through the inductor $L$ during the time period $DT$ (when the switch $S$ is switched on and the diode $D$ is off) will be as follows:

$$i_L = I_{L,N} + \frac{V_i}{L} t \tag{2.1}$$

In reference to Figure 2.3(a), the inductor current through the inductance $L$ during the time period $(1-D)T$ (when the switch $S$ is off and the diode $D$ is on) can be defined as:

$$i_L = I_{L,P} + \frac{V_i - V_o}{L}(t - DT) \tag{2.2}$$

The boost ratio of the conventional DC-DC boost converter in the CCM for $V_C = V_o$ is expressed as follows:

$$\frac{V_C}{V_i} = \frac{1}{1-D} \quad = \quad \frac{V_o}{V_i} = \frac{1}{1-D} \tag{2.3}$$

The average inductor current ($I_L$) of the convectional DC-DC boost converter in the CCM, can be expressed as shown below:

$$I_L = \frac{V_o}{(1-D)R} = \frac{I_o}{(1-D)} \tag{2.4}$$

In general for traditional boost converters as the boost ratio increases the value of duty cycle approaches to unity. The graph shown in the figure below is drawn for different values of $\frac{R_L}{R}$ as per the expression provided by equation 3.104.

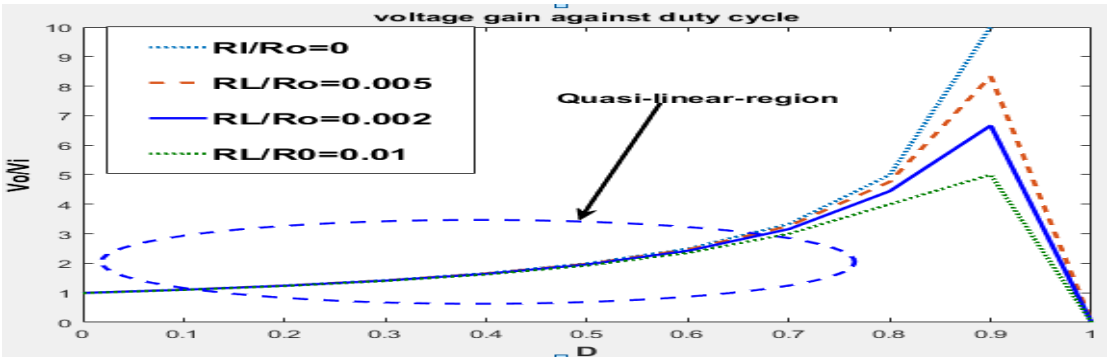



**Figure 2.4:** Voltage gain against duty cycle for convectional BC

In the time period $(1-D)T$ (when the switch $S$ is off and the diode $D$ is on), in the circuit including the switch $S$, the diode $D$, and the load resistance $R$, then the voltage $V_S$ of the switch $S$ will be as follows:

$$V_S = V_o \tag{2.5}$$

In the time interval $DT$ (when the switch $S$ is on and the diode $D$ is off), the voltage of the switch of $S$ is zero.

### 2.2.2 Critical conduction region

The wave forms of the voltages and currents for the critical conduction region are shown in Figure 2.3(b). In this figure, the current passing through the inductance $L$ during the time period $DT$ (when the switch $S$ is on and the diode $D$ is off) will be as follows:

$$i_L = \frac{V_i}{L} t \tag{2.6}$$

And referring the same figure, the current passing through the inductor $L$ during the time $(1-D)T$ (when the $S$ switch is off and the diode $D$ is on) will be as follows:

$$i_L = I_{L,P} + \frac{V_i - V_o}{L}(t - DT) \tag{2.7}$$

In the time interval $(1-D)T$ (when the switch $S$ is off and the diode $D$ is on), the voltage of the switch $S$ in the circuit including switch $S$, the diode $D$, and load resistance $R$, will be as follows:

$$V_S = V_o \tag{2.8}$$

In the time period $DT$ (when the switch $S$ is on and the diode $D$ is off), the voltage of the switch is zero.

### 2.2.3 Discontinuous conduction mode (DCM)

The wave forms of the voltages and currents for the critical conduction region are shown in Figure 2.3(c). According to this figure, the current passing through the inductance $L$ in the duration of $DT$ (when the switch $S$ is on and the diode $D$ is off) will be as follows:

$$i_L = \frac{V_i}{L}t \tag{2.9}$$

Again with respect to Figure 2.3(c), the current passing through the inductor $L$ over the time $\Delta_1 T$ (when the switch $S$ is off and the diode $D$ is on) will be deduced as:

$$i_L = I_{L,P} + \frac{V_i - V_o}{L}(t - DT) \tag{2.10}$$

Then, with reference to the same figure, the current passing through the inductor $L$ is zero at the time $\Delta_2 T$ (when the switch $S$ and diode $D$ are off). As a result the converter's voltage gain in DCM for $V_C = V_o$ will be given by the following formula:

$$\frac{V_C}{V_i} = \frac{\Delta_1 + D}{\Delta_1} = \frac{V_o}{V_i} = \frac{\Delta_1 + D}{\Delta_1} \tag{2.11}$$

The average inductor current $I_L$ of the boost converter in the DCM, will be expressed as follows:

$$I_L = \frac{V_o(\Delta_1 + D)}{\Delta_1 R} \tag{2.12}$$

In the $\Delta_1 T$ time interval in the loop including the switch $S$, the diode $D$, and the load resistance $R$, the voltage of the switch $S$ will be written as:

$$V_S = V_o \tag{2.13}$$

In the time period $\Delta_2 T$, in the circuit containing the voltage source $V_i$, the inductor $L$ and the switch $S$, and considering that the voltage of the inductors $L$ is zero. At this time interval the voltage of the switch $S$ is as follows:

$$V_S = V_i \tag{2.14}$$

In the first half cycle of $DT$ (when the switch $S$ is on and the diode $D$ is off), the voltage of the switch $S$ is zero. Therefore, for a given boost converter the designing system is controlled by having specific critical values in order to operate continuously as shown below. The critical values for the inductor and the capacitors are directly proportional to the value of duty cycle.

$$Lc = \frac{DR(1-D)^2}{2f} \tag{2.15}$$

$$Cc = \frac{D}{R2f} \tag{2.16}$$

And the voltage ripples as well as current ripples are controlled by controlling the values of the capacitor, inductor and duty cycle.

$$\Delta IL = \frac{ViD}{Lf} \tag{2.17}$$

$$\Delta Vc = \frac{VoD}{CfR} \tag{2.18}$$

$$\Delta Vc = \Delta Vo = \frac{ViD}{CfR(1-D)} \tag{2.19}$$

## 2.3 DC-DC Multilevel Boost Converter

In general view multilevel boost converters (MBC) are a power electronics semiconductor devices (PESD) based converters which has the capability of stepping-up the magnitude of various values of DC input voltage sources at the output side. The number of the input source may be a single or more than two sources, but the generated output voltage sources are more than two levels (Skvarenina, 2002). Now days, the significance of this topologies is more dominant in energy generating sectors in the applications where, a high power conversion is required. Renewable energies, such as PV cells in photovoltaic systems and full cells are some of the recent alternative options that require a boosting of voltage due to their distinct feature of generating low voltage (Ganesan and Prabhakar, 2013). The performance of these converters is utilized by integrating low power rating power electronics devices, like capacitors, inductors, power switches and diodes. The working principle is mainly based on charging and discharging of the inductors and capacitors (Puneeth and Nattarasu, 2014). Thus achieving high boost ratio and efficiency using low input DC sources makes these types of converters more comfortable than other categories of topologies. Likewise, using more number of power electronic components is a negative side of these structures.

### 2.3.1 Existing multilevel DC-DC boost converter

As explained in the previous sections MBC are the new improvement of converters so far discovered in recent years, in which most of these structures are directed toward the high voltage conversion areas, thus their popularity has been increasing with time. Almost, all the existing MBC are similar in their performance, design, operation and characteristics, the only differences are in the number of power electronics components used, power loss, voltage ratio obtained, variety of efficiency, voltage stress on switches, complexity of the circuit, number of voltage levels generated, quality of control circuit, limitation of duty cycle and the balancing of output voltages as indicated in Table 2.2. In most cases, the boost ratio obtained was varied from 6 to 10 with the value of duty cycle run from 0.5 up to 1, in which some of these converters achieved a high voltage gain with large value of duty cycle which leads to high ripples and voltage stress as a result efficiency is reduced. The designing parameters of some existing MBC are compared against their conversion

ratio, voltage stress, duty cycle and number of device used as shown below in the Table 2.1.

**Table 2.1:** Various boost topologies with voltage gain, voltage stress and specific Parameter

| Category | Capacitors | Inductors | Diodes | Switches | Voltage Gain | Voltage Stress |
|---|---|---|---|---|---|---|
| Convectional Boost Converter | 1 | 1 | 1 | 1 | $\frac{V_o}{V_i}=\frac{1}{1-D}$ | $v_S=V_o$ |
| Switched Capacitor MBC | 2 | 0 | 2 | 3 | - | $v_S=3V_i$ |
| Switched Inductor MBC | $2N-1$ | 2 | $2N+2$ | 1 | $\frac{V_o}{V_i}=\frac{N(1-D)}{1-D}$ | $V_S=\frac{V_o}{N-0.5}$ |
| Three Level MBC | $2N-1$ | 1 | $2N-1$ | 1 | $\frac{V_o}{V_i}=\frac{3}{1-D}$ | $V_S=\frac{V_o}{3}$ |
| $N$ Level MBC | $2N-1$ | 1 | $2N-1$ | 1 | $\frac{V_o}{V_i}=\frac{N}{1-D}$ | $V_S=\frac{V_o}{N}$ |

**Table 2.2:** High voltage gain, high efficiency DC-DC boost converter design requirements for high power application

| Parameters | Recommended Level | Verification |
|---|---|---|
| Voltage Boost Ratio | High | Improve the maximal required DC stage with low input source |
| Parasitic Element (Resistance) | Minimal | Limits the value of voltage gain by controlling the value of duty cycle |
| Semiconductor Devices Voltage Stress | Low | Reduce switch loss |
| Number of Components Used and their Rating | Minimum | Reduces the weight and cost of the converter |
| Input/output Current flow Rate | Continuous | Low ripple current and a capacitor with low value |
| Switching System | Soft switching | Low switching loss |
| Duty Cycle | Medium | Current and voltage ripples are reduced |

### 2.3.2 Proposed DC-DC multilevel boost converter

The proposed multilevel DC-DC boost converter is a DC-DC converter based on pulse width modulation (PWM) that uses a convectional DC-DC converter and voltage switched capacitor to generate various voltage levels in the output using only a single-switch, $2n-1$ diodes, one inductor and $2n-1$ capacitors for $n$ times MBC. This converter is used as a DC-link in various applications, such as photovoltaic (PV) systems, or fuel cells that need a multiple regulated voltage levels, with continuous unidirectional current flow and self-balanced voltages for grid-connected AC inverters and HVDC distribution systems. The main merits of this proposed converter are high voltage gain with limited duty cycle and no transformer is needed, continuous input current, modular design, and operating at optimal switching frequency without changing the basic structure of the traditional boost converter.

### 2.3.3 Advantages of the Proposed Multilevel Boost Converters

The proposed topology has some advantages over the existing high voltage boost converters.

- High conversion ratio is improved without out extremely large value of duty cycle
- Operating at steady continuous input/output currents
- The need of transformer is eliminated
- Variable balanced output voltages
- Operates at very high switching frequency
- Low current and voltage ripples
- Comfortable DC-link for grid connected multilevel inverters
- Low voltage stress on switch compared to output voltage

# CHAPTER 3
# RESEARCH DESIGN AND MODELING OF THE PROPOSED CONVERTER

The designing and analysis of large level of the DC-DC MBC operating at a higher switching frequency requires a mathematical modelling and approximation to estimate its maximum operating boost ration. The performance of the proposed topology will be described in detail in the following main parts.

## 3.1 Two-Level DC-DC Boost Converter

If two diode and two capacitors are added in the structure presented in Figure 2.1, then the two-level boost DC-DC converter is formed as indicated in Figure 3.1.

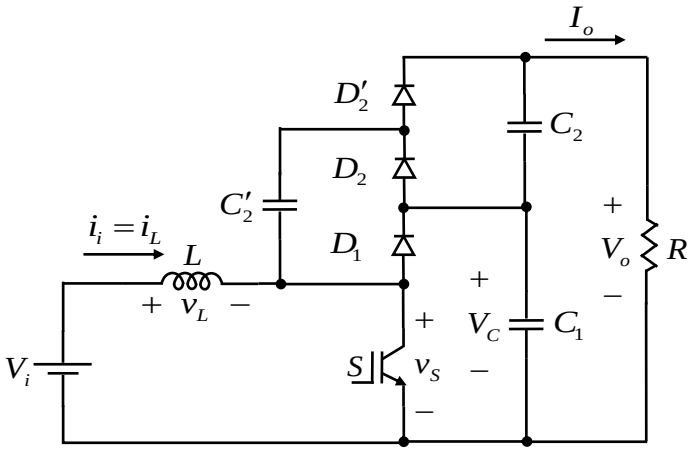
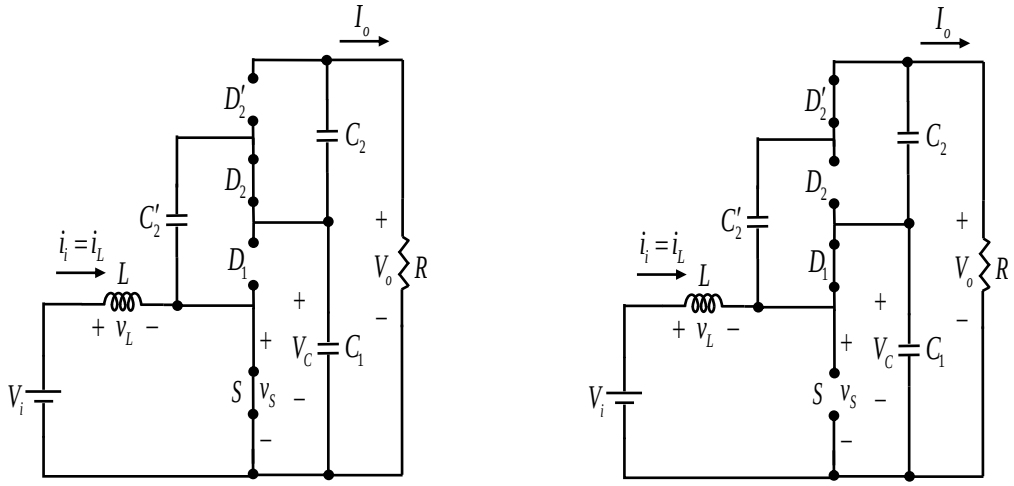



**Figure 3.1:** Two-level DC-DC boost converter circuit diagram

According to Figure 3.1, the first level includes the switch $S$, the diode $D_1$ and the capacitor $C_1$, and the second level consists of diodes ($D_2$ and $D_2'$) and capacitors $C_2$ and $C_2'$. The advantage of this structure is increasing the number of voltage levels by adding capacitors and diodes without changing the main circuit. According to Figure 3.1, the difference between the two-level incremental DC-DC converter and the one-level incremental DC-DC converter is that in a dual-level boost DC-DC converter, the output voltage is twice the output voltage of the single-stage converter. This result is due to the existence of a voltage doubles at the output of the conventional converter. The equivalent circuit of DC-DC dual-level boost converter shown in Figure 3.2(a) is formed, when the

switch $S$ is on. During the switching on state of the switch, the inductor $L$ is connected to the voltage source $V_i$. Due to the fact that the switch $S$ is on, the presence of the voltage of capacitor $C_1$ causes the diode $D_1$ to turn off. If the voltage of the capacitor $C_2'$ is smaller than the voltage of the capacitor $C_1$, then $C_1$ clamps capacitor $C_2'$ through diode $D_2$ and the switch $S$. In this case, the presence of capacitor $C_2$ voltage causes the diode $D_2'$ to be turned off.




(a) On mode (b) Off mode

**Figure 3.2:** DC-DC dual-level boost converter on/off mode circuit diagrams

The equivalent circuit of the two-level boost converter in the interval when the switch $S$ is off is shown in Figure 3.2(b). In this period of time, the inductor current turns on the diodes $D_1$ and $D_2'$. As long as the diode $D_1$ is on, the presence of the voltage of the capacitor $C_2'$ will cause the diode $D_2$ to turn off. The waveforms of the voltages and currents of the DC-DC dual-level boost converter are shown in Figure 3.3. In this figure, 1and 0 are the on/off states of the switch $S$. In the time interval $(1-D)T$ (when the switch $S$ is off and the diodes $D_1$ and $D_2'$ are on), voltage of the switch in the circuit including the switch $S$, the diode $D_1$ and the capacitor $C_1$ is the same as the capacitor voltage $V_C$ ($v_S = V_C$). At the time interval $DT$ (when the switch $S$ and the diode $D_2$ are on), the voltage of the switch $S$ is zero. In the following sections, the two-level DC-DC boost converter is analyzed in continuous and discontinuous conduction regions.

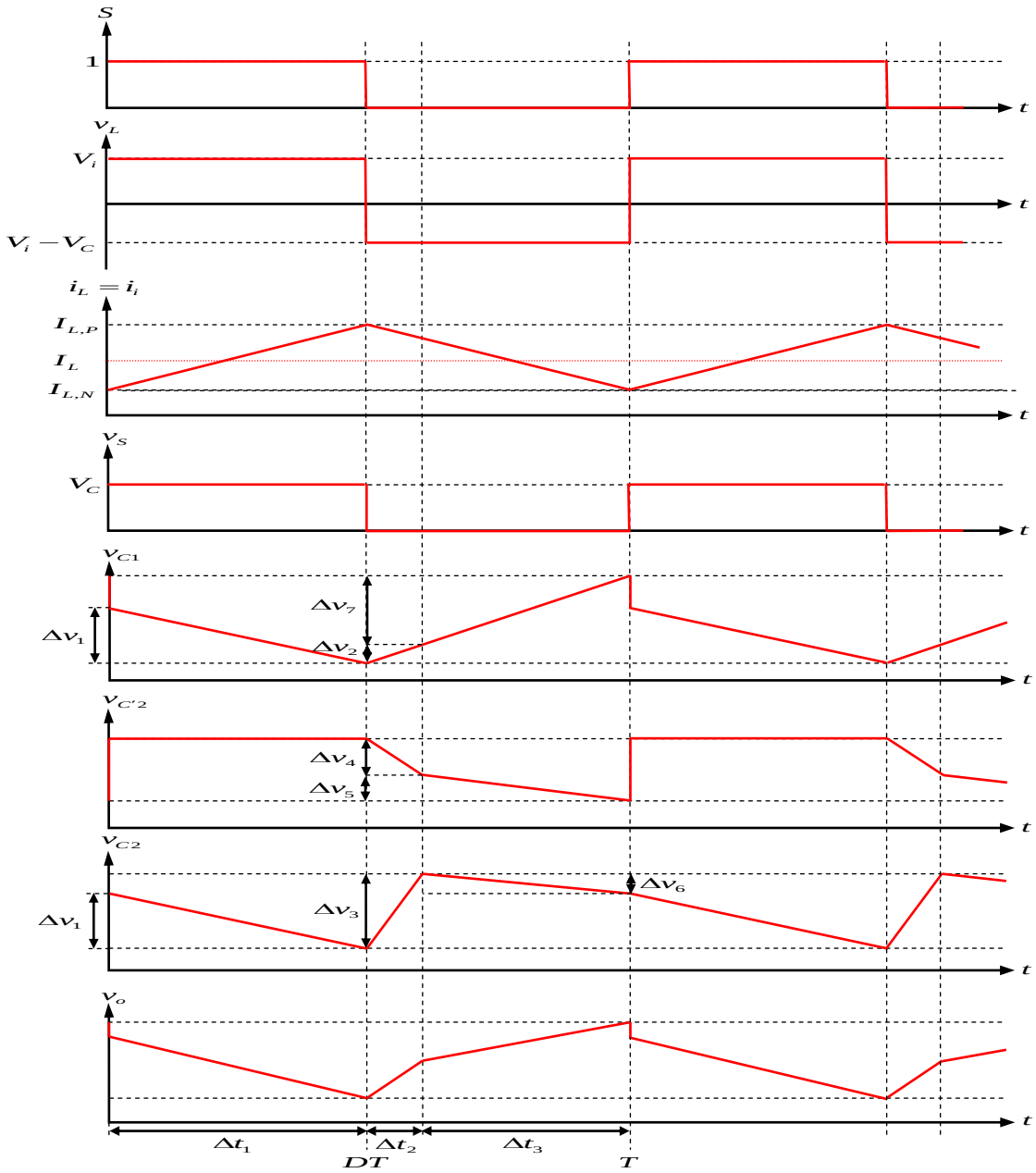



**Figure 3.3:** Voltage and current waveforms of DC-DC dual-level boost converter

### 3.1.1 Two-level DC-DC boost converter analysis in CCM

In the time interval $DT$ (when the switch $S$ and diode $D_2$ are switched on) the flow of the inductor current $I_L$ through the inductor with a voltage of $v_L = V_i$ in the loop including the voltage source $V_i$, the inductor $L$ and the switch $S$, is given by:

$$i_L = I_{L,N} + \frac{1}{L}\int_0^t v_L dt = I_{L,N} + \frac{V_i}{L}t \qquad (3.1)$$

But, during $(1-D)T$ interval (when the switch $S$ is off and the diodes $D_1$ and $D_2'$ are on), in the circuit including the voltage source $V_i$, the inductor $L$, and the capacitor $C_1$ provided that $v_L = V_i - V_C$ and the current $I_L$ passing through the inductor $L$ is:

$$i_L = I_{L,P} + \frac{1}{L}\int_{DT}^{t} v_L dt \; = i_L = I_{L,P} + \frac{V_i - V_C}{L}(t - DT) \tag{3.2}$$

Based on Figure 3.1, for DC-DC two-level boost converter, assuming that the capacitors $C_1$ and $C_2$ have the same capacitance and the voltage of the capacitors $C_1$ and $C_2$ are equal, then $V_{C1} = V_{C2} = V_C$, and the output voltage across the load will be:

$$V_o = 2V_C \tag{3.3}$$

According to the relations 2.3 and 3.3, the voltage gain of the two-level DC-DC boost converter in the continuous conduction region is defined as:

$$\frac{V_o}{V_i} = \frac{2}{1-D} \tag{3.4}$$

According to Figure 3.1, the input power $P_i$ and output power $P_o$ of the converter with the average of the input current $I_i$ and output current $I_o$ are always kept equal and the output current is defined as:

$$I_o = \frac{V_o}{R} \tag{3.5}$$

Then using the equations 3.3, 3.4 and 3.5 in the power equality the average inductor current of this level converter is expressed as shown below provided that $I_i = I_L$.

$$P_i = P_o$$

$$V_i I_i = V_o I_o$$

$$V_o \times \frac{V_o}{R} = 2V_C \times \frac{2V_C}{R} = \frac{2^2 V_C{}^2}{R} = V_i I_i$$

$$I_L = \frac{1}{V_i} \times \frac{2^2 V_C{}^2}{R} = \frac{V_C}{V_i} \times \frac{2^2 V_C}{R} \tag{3.6}$$

By replacing equation 2.3, into the above relation the average inductor current is expressed as:

$$I_L = \frac{2^2 V_C}{R(1-D)} \tag{3.7}$$

From equation 3.7 it can be seen that the input current can be controlled by varying the value of the duty cycle $D$ using PWM, which is very important in many applications, such as renewable energies and useful in calculating the maximum power point by tracking the input current.

### 3.1.2 Two-level DC-DC boost converter analysis in DCM

According to the relations 2.11 and 3.3, the voltage gain of the two-level DC-DC boost converter in the discontinuous conduction region will be as follows:

$$\frac{V_o}{V_i} = 2\frac{\Delta_1 + D}{\Delta_1} \tag{3.8}$$

Substituting equation 2.11 into 3.6, the average flow of the inductor current in the discontinuous conduction region is defined as:

$$I_L = \frac{2^2 V_C (\Delta_1 + D)}{R\Delta_1} \tag{3.9}$$

### 3.1.3 Inductor's equivalent series resistor (ESR) effect on the voltage gain of the two-level DC-DC boost converter

For all step-up DC-DC converters with an increasing power, the maximum voltage gain in ideal mode is infinite. In practical applications, this gain is limited by the parasitic resistance of the passive elements. In all case of boost converters, the most limitation is the existence of "equivalent series resistance (ESR)" with an inductor in the input side. This phenomenon is due to the fact that the input current is equal to the product of the output current and the gain of the voltage. It should be noted that the use of high switching frequency allows the use of a smaller inductor with a smaller ESR, thus a converter designed with high switching frequency will play an important role in reducing this effect.

***a. The effect of the ESR on the voltage gain of the two-level DC-DC MBC in CCM***

In reference to Figure 3.2, the following relationships are maintained for the time interval $DT$ when the switch $S$ is on and for the time period $(1-D)T$ when the switch $S$ is off respectively.

$$v_L = V_i - I_L R_{ESR,L} \tag{3.10}$$

$$v_L = V_i - V_C - I_L R_{ESR,L} \tag{3.11}$$

Where, $R_{ESR,L}$ is the equivalent series resistance of the inductor $L$ and $v_L$ is the voltage of the inductor $L$. Considering the above relations at steady state, the average voltage of the inductor in a total period of time is zero.

$$D(V_i - I_L R_{ESR,L})T + (1-D)(V_i - V_C - I_L R_{ESR,L})T = 0$$

$$V_i = (1-D)V_C + I_L R_{ESR,L} \tag{3.12}$$

Substituting equations 3.3 and 3.7 into the above equation the boost ratio of the dual-level boost converter considering the effect of the inductor's ESR will be as follows:

$$V_i = (1-D)\frac{V_o}{2} + \frac{2V_o}{(1-D)R} R_{ESR,L}$$

$$\frac{V_o}{V_i} = \frac{1}{\frac{1-D}{2} + \frac{2R_{ESR,L}}{(1-D)R}} \tag{3.13}$$

By comparing the relationships 3.4 and 3.13 it is clearly noted that, the ESR of the inductor $L$ reduces the gain of the voltage.

***b. The Effect of the ESR on the voltage gain of the two-level DC-DC MBC in DCM***

Referring with respect to Figure 3.2, the following relationships will be established for two-stage DC-DC step-up converter in a DCM during the on/off states:

$$v_L = V_i - I_L R_{ESR,L} \tag{3.14}$$

$$v_L = V_i - V_C - I_L R_{ESR,L} \tag{3.15}$$

$$v_L = 0 \tag{3.16}$$

The relations 3.14 to 3.16 for the time interval $DT$ when the switch $S$ is on and for the time interval $\Delta_1 T$ and $\Delta_2 T$ when the switch is off are established respectively. Applying the voltage balance low during the total period of time, then the average voltage of the inductor is equal to zero.

$$D(V_i - I_L R_{ESR,L})T + \Delta_1(V_i - V_C - I_L R_{ESR,L})T + \Delta_2(0) = 0$$

$$V_i(\Delta_1 + D) = \Delta_1 V_C + (\Delta_1 + D) I_L R_{ESR,L} \tag{3.17}$$

While substituting the relations 3.3 and 3.8 into 3.17, then the voltage gain of the two-level DC-DC boost converter in a DCM considering the effect of the inductor's ESR is given by the equation shown below:

$$V_i(\Delta_1 + D) = \Delta_1 \frac{V_o}{2} + (\Delta_1 + D)\frac{2V_o(\Delta_1 + D)}{R\Delta_1} R_{ESR,L}$$

$$\frac{V_o}{V_i} = \frac{(\Delta_1 + D)}{\frac{\Delta_1}{2} + \frac{2(\Delta_1 + D)^2}{R\Delta_1} R_{ESR,L}} \tag{3.18}$$

### 3.1.4 Evaluation of diodes and switch voltage drop effect on two-level DC-DC MBC

In practical applications, the voltage drop across the diodes and the switches in MBC should be considered, since it affects the capacitors not to be charged to the value of $V_C$ (voltage at the lowest capacitor). This effect will be studied in this section. The voltage drop in conventional switches and power diodes can be estimated up to 2 volts (is much smaller compared to lower powers). In medium voltage and high voltages applications, the voltage drop on the elements can be neglected, but in low voltage applications, the voltage drop of the elements should be considered. Considering Figure 3.2a, the equation of voltages in the circuit containing the capacitor $C_2'$, switch $S$, capacitor $C_1$, and the diode $D_2$, is obtained as:

$$V_{C'2} + V_S - V_{C1} + V_{D2} = 0 \tag{3-19}$$

Where, $V_{C'2}$, $V_S$, $V_{C1}$ and $V_{D2}$ are the voltages of the capacitor $C_2'$, the switch $S$, the capacitor $C_1$, and the diode $D_2$ respectively. For calculation simplicity, it is assumed that the voltage drop across the switch $S$ and the diodes are considered to be the same, in other words:

$$V_S = V_{D2} = V_d \tag{3.20}$$

By replacing the above relation in to the equation 3.19, the following expression is deduced:

$$V_{C'2} = V_{C1} - 2V_d \tag{3.21}$$

Again with respect to Figure 3.2b, in the circuit, including the capacitor $C_2'$, the diode $D_2'$, the capacitor $C_2$, and the diode $D_1$ the voltage expression is given by:

$$-V_{C'2} + V_d + V_{C2} - V_d = 0 \tag{3.22}$$

By substituting equation 3.21 into the relation 3.22 the voltage of the capacitor $C_2$, will be calculated as:

$$V_{C2} = V_{C1} - 2V_d \tag{3.23}$$

Therefore, the output voltage of the two-level DC-DC step-up converter shown in Figure 3.1 is expressed by the following equation while considering the effect of the voltage drops across the switch and diodes.

$$V_o = V_{C1} + V_{C2} = V_{C1} + V_{C1} - 2V_d = 2V_{C1} - 2V_d \tag{3.24}$$

Thus, the efficiency of the switched capacitor of the two-level step-up DC-DC converter is defined as shown below, while considering the above effects.

$$\frac{V_o}{2V_{C1}} = \frac{2V_{C1} - 2V_d}{2V_{C1}} = 1 - \frac{V_d}{V_{C1}} \tag{3.25}$$

### 3.1.5 Design and description of the two-level DC-DC boost converter

By selecting an appropriate value of the capacitors for the desired converter, the output voltage ripple of the two-level DC-DC boost converter is reduced to the minimum value. As shown in Figure 3.2(a), when the switch $S$ is turned on, the capacitor $C_1$ has a higher voltage than the capacitor $C_2'$ because always capacitor $C_1$ charges at the end of the half cycle process. Thus, the capacitor $C_1$ charges capacitor $C_2'$ through the diode $D_2$ until they have equal voltages. During the switching on state the capacitors $C_1$ and $C_2'$ are connected in parallel.

$$C = C_1 + C_2' \tag{3.26}$$

At the time before the switch $S$ is turned on, the total charge stored in the capacitors $C_1$ and $C_2'$ will be as follows:

$$Q_{12'}(0^-) = Q_1(0^-) + Q_{2'}(0^-) = C_1 V_{1bc} + C_2' V_{2'bc} \tag{3.27}$$

In the above equation, $Q_{12'}(0^-)$ is the sum of the stored charges in the capacities $C_1$ and $C_2'$ at the moment before turning on the switch $S$, while $Q_1(0^-)$ and $Q_{2'}(0^-)$ indicates the charges stored in the capacitors $C_1$ and $C_2'$ at the moment before closing the switch $S$ respectively. The respective voltages of the capacitor $C_1$ and $C_2'$ are $V_{1bc}$ and $V_{2'bc}$ at the moment just before the switch $S$ is closed. According to the principle of energy conservation, it is expressed as:

$$Q_{12'}(0^+) = Q_{12'}(0^-)$$
$$CV = C_1 V_{1bc} + C_2' V_{2'bc} \tag{3.28}$$

In the above relation, $Q_{12'}(0^+)$ and $V$ are the total charge stored and voltages of the capacitors $C_1$ and $C_2'$ after the switch $S$ have been turned on. Based on the above relation, equation (3.28) can be expressed as:

$$V = V_{1ac} = V_{2'ac} = \frac{C_1 V_{1bc} + C_2' V_{2'bc}}{C_1 + C_2'} \tag{3.29}$$

From the above relation, $V_{1ac}$ and $V_{2'ac}$ are the voltages of the capacitors $C_1$ and $C_2'$ at the moment after the switch $S$ is turned on. After the switch $S$ is activated diode $D_2$ is turned on, and capacitor $C_2'$ starts charging by the capacitor $C_1$. As a result the capacitor $C_2'$ does not transfer energy to the load during the duration when the switch $S$ is on and its voltage remains constant during this period. At the same time, the capacitors $C_1$ and $C_2$ are arranged in series and starts to discharge their voltage because these capacitors are supplying the load. Then, the voltage drop during this time of conduction is $(\Delta v_1)$ assuming that all capacitors have the same capacitance value. The current through the capacitors is given by:

$$i_C = C\frac{dv_C}{dt} \tag{3.30}$$

Thus approximating $\frac{dv_C}{dt} \approx \frac{\Delta v_C}{\Delta t}$, the above relation can be rewritten as follows:

$$\Delta v_C = \frac{1}{C} i_C \Delta t \tag{3.31}$$

Since the capacitors have the same value of capacitance, the voltage drops across each capacitor are equal.

$$\Delta v_{C1} = \Delta v_{C2} = \frac{1}{C_1} i_{C1} \Delta t_1 = \frac{1}{C_2} i_{C2} \Delta t_1 \tag{3.32}$$

In the above equation, $\Delta t_1$ is the discharge time of the capacitors $(C_1, C_2)$ and $(\Delta v_{C1}, \Delta v_{C2})$ are the voltage drops across the two capacitors $C_1$ and $C_2$ at the time interval when the switch $S$ is closed respectively. Therefore the voltage drop of the load feeding capacitors is the same as the as the voltage drop across the load $(\Delta v_1)$ and the discharging currents are equal to the load current $(i_{C1} = i_{C2} = I_o)$ in the same interval time as shown below.

$$\Delta v_1 = \Delta v_{C1} = \Delta v_{C2}$$

$$\Delta v_1 = \frac{1}{C_1} I_o \Delta t_1 = \frac{1}{C_2} I_o \Delta t_1 \tag{3.33}$$

The above equation expresses the voltage drop across the load. In reference to Figure 3.2(b), at the moment when the switch $S$ is deactivated, the current of the inductor $L$ turns on the diode $D_2'$. The duration of switching off of the switch $S$ can be sub divided into two time intervals $\Delta t_2$ and $\Delta t_3$. In first time interval $\Delta t_2$ of the off state, the voltage of the capacitors $C_2'$ is greater than the voltage of the capacitors $C_2$ that makes diode $D_1$ keeps in off mode until their voltages get balanced. During this period, the discharge current through the capacitor $C_2'$ is $I_L$ ($i_{C'2} = I_L$) and the charging current of the capacitors $C_1$ and $C_2$ is the same as ($i_{C1} = i_{C2} = I_L - I_o$). At the moment when the voltages of the capacitor $C_2$ and $C_2'$ are equalized, the diode $D_1$ turns on and this parallel capacitors are now ready to supply power to the load in series with capacitors $C_1$. As soon as when the conduction mode of the above interval ends, the second interval of the off state begins with a time period of $\Delta t_3$. Based on the above occasions, the variable voltage drops across the capacitors $C_1$, $C_2$ and $C_2'$ are calculate at time intervals $\Delta t_2$ and $\Delta t_3$. The voltage drops ($\Delta v_2$, $\Delta v_3$) of the capacitors $C_1$ and $C_2$ in the time interval $\Delta t_2$ are the same and expressed as follows.

$$\Delta v_2 = \Delta v_3 = \frac{1}{C_1} i_{C1} \Delta t_2 = \frac{1}{C_2} i_{C2} \Delta t_2$$

$$\Delta v_2 = \Delta v_3 = \frac{1}{C_1} (I_L - I_o) \Delta t_2 = \frac{1}{C_2} (I_L - I_o) \Delta t_2 \qquad (3.34)$$

The amount of voltage drop $\Delta v_4$ across the capacitor $C_2'$ in the time interval $\Delta t_2$ is also given by:

$$\Delta v_4 = \frac{1}{C_2'} i_{C'2} \Delta t_2$$

$$\Delta v_4 = \frac{1}{C_2'} I_L \Delta t_2 \qquad (3.34)$$

During the second conduction mode of the off state in the time interval $\Delta t_3$, both the capacitors $C_2$ and $C_2'$ are in parallel and delivers power to the load in series with capacitor $C_1$ with a discharging current $\frac{I_o}{2}$ in which($i_{C2} = i_{C'2} = \frac{I_o}{2}$). However, capacitor $C_1$ keeps charging

with a current $I_L - I_o$ during the same time interval where $i_{C1} = I_L - I_o$. The voltage drop ( $\Delta v_5$, $\Delta v_6$) across the two capacitors $C_2$ and $C_2'$ at the time interval $\Delta t_3$ is given as:

$$\Delta v_5 = \Delta v_6 = \frac{1}{C_2} i_{C2} \Delta t_3 = \frac{1}{C_2'} i_{C'2} \Delta t_3$$

$$\Delta v_5 = \Delta v_6 = \frac{1}{C_2}\left(\frac{I_o}{2}\right)\Delta t_3 = \frac{1}{C_2'}\left(\frac{I_o}{2}\right)\Delta t_3 \qquad (3.35)$$

The increase voltage ( $\Delta v_7$) of the capacitors $C_1$ in the time interval $\Delta t_3$ is as follows:

$$\Delta v_7 = \frac{1}{C_1} i_{C1} \Delta t_3$$

$$\Delta v_7 = \frac{1}{C_1}(I_L - I_o)\Delta t_3 \qquad (3.36)$$

The output voltage of the two-level DC-DC boost converter is equal to $v_{C1} + v_{C2}$. Therefore, the ripple at the output voltage can be expressed as the summation of the voltage ripples in capacitor $C_1$ and capacitor $C_2$. Thus, the values of the capacitors and switching frequency are selected based on the designing system proved above to reduce the voltage ripples for practical applications. The required ripple current on the input side also controlled, by calculating the inductor current in the base level of the convectional step up convertor.

### 3.1.6 Voltage stress on the switch in two-level DC-DC boost converter

With reference to Figure 3.2(b), the voltage across the switch in the circuit containing the switch $S$, capacitor $C_1$ and diode $D_1$ during the off state of the switch $S$, is given by:

$$V_S = V_{C1} \qquad (3.37)$$

By substituting equation (3.3) into the above relation given that $V_{C1} = V_{C2} = V_C$ the voltage stress of the switch in the two-level DC-DC MBC will be derived as:

$$V_S = \frac{V_o}{2} \qquad (3.38)$$

## 3.2 Three-Level DC-DC Boost Converter

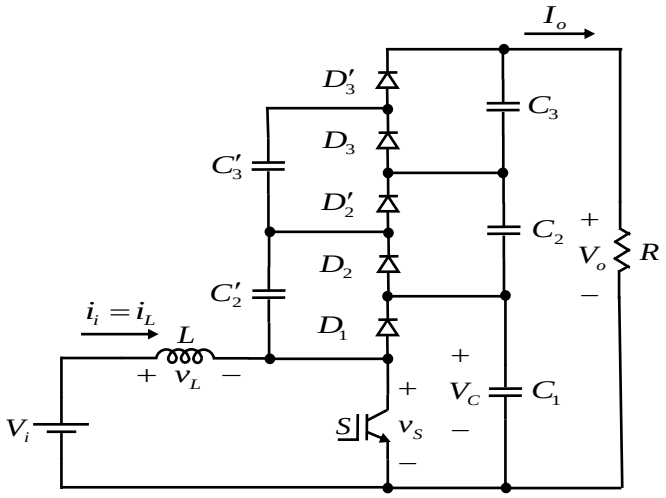
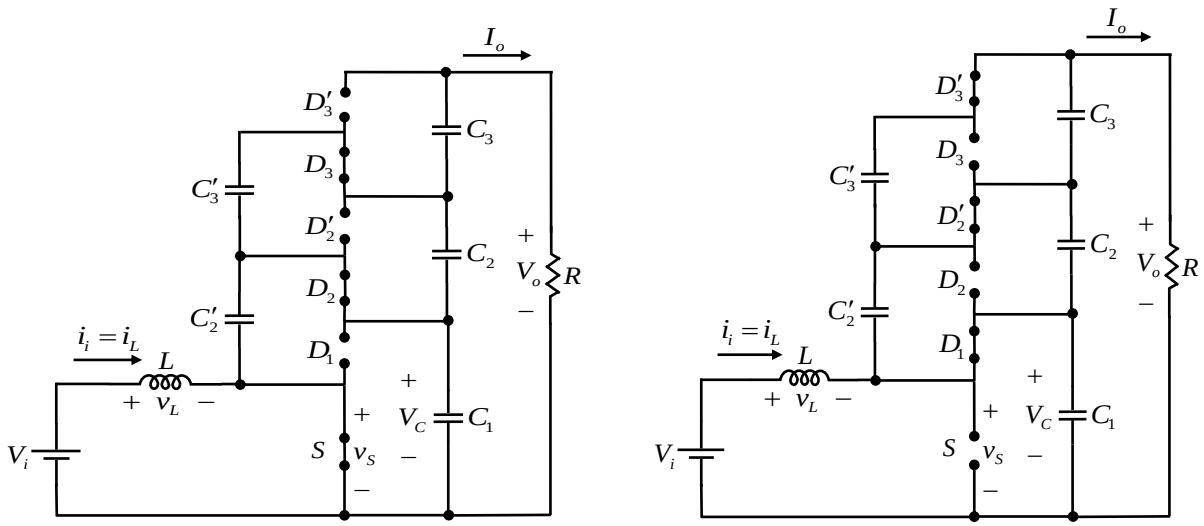



**Figure 3.4:** Three-level DC-DC boost converter circuit diagram

The three-level DC-DC boost converter circuit diagram is shown in Figure 3.4.The equivalent circuit of the three-level DC-DC step up converter in the first half cycle is shown in Figure 3.5(a), when the switch $S$ is turned on. As shown in this figure the switch $S$, the inductor ($L$) are connected in series with the voltage source $V_i$. In this mode of operation the voltages across the load feeding capacitors $C_1$, $C_2$ and $C_3$ is greater the voltage across the clamped capacitors $C_2'$ and $C_3'$, thus the presence of higher voltage in the capacitor $C_1$, $C_2$ and $C_3$ causes the diodes $D_1$, $D_2'$ and $D_3'$ to be off mode, while $D_2$ and $D_3$ remain in on state for transferring energy from capacitors $C_1$ and $C_2$ to the capacitors $C_2'$ and $C_3'$ respectively. The charging system continues until the voltage across the charging-discharging capacitors will be the same.




(a) On mode (b) Off mode

**Figure 3.5:** The power circuit of the three-level DC-DC boost converter for on/off modes

The equivalent circuit of the three-level DC-DC boost converter for the next half cycle is shown in Figure 3.5(b), when the switch $S$ is in off state. During this time interval, the current flowing through the inductor $L$ reaches its maximum peak and causes the diodes $D_1$, $D_2'$ and $D_3'$ to be turned on, while the diodes $D_2$ and $D_3$ are in off mode, due to the presence the voltages across the capacitor $C_2'$ and $C_3'$. The waveforms of the voltages and currents of the three-level DC-DC boost converter are shown in Figure 3.6. In this figure, 1 means high and 0 means low of the switch $S$. In the time interval $(1-D)T$ (when the switch off and the diodes $D_1$, $D_2'$ and $D_3'$ are on), in the circuit including the switch $S$, the diode $D_1$, and the capacitor $C_1$, the voltage $V_S$ across the switch ($S$) will be defined as.

$$V_S = V_C \tag{3.39}$$

However, during the first time interval $DT$ (when the switch $S$ is and diodes $D_2$ and $D_3$ are on), the voltage of the switch is zero. In the preceding section the details of the three-level DC-DC step up converter is analyzed in continuous and discontinuous conduction regions with the help of wave forms.

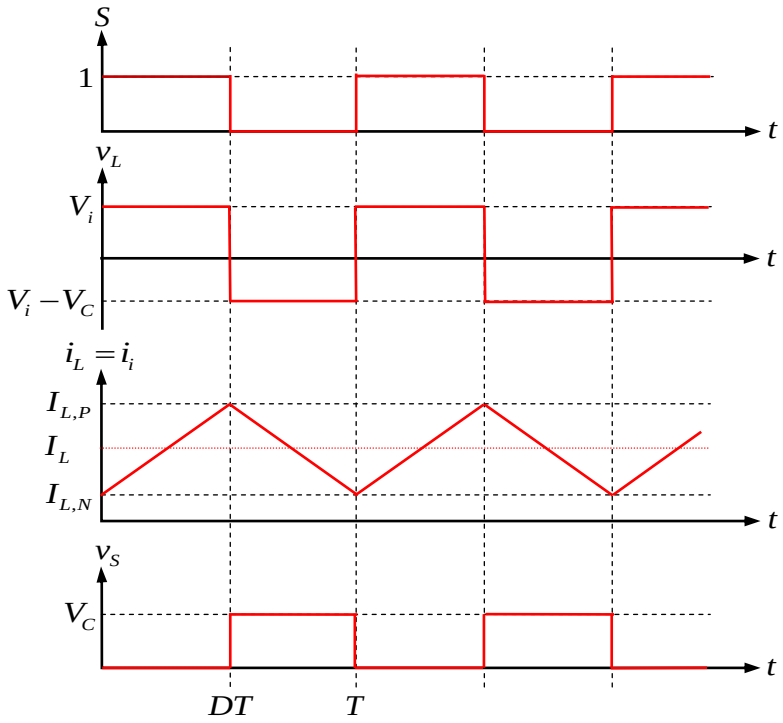



**Figure 3.6:** Voltage and current waveforms for three-level DC-DC boost converter

### 3.2.1 Three-level DC-DC boost converter analysis in CCM

The same procedures are followed to evaluate the expression of the inductor current as conducted in section 3.1 for both CCM and DCM. During the on state, in the time interval $DT$ (when the switch $S$ and the diodes $D_2$ and $D_3$ are on) the following relation are analyzed for the current ($i_L$) passing through the inductor $L$ given that $v_L = V_i$:

$$i_L = I_{L,N} + \frac{1}{L}\int_0^t v_L dt = I_{L,N} + \frac{V_i}{L}t \qquad (3.40)$$

In the time interval $(1-D)T$ (when the $S$ switch is off and the diodes $D_1$, $D_2'$ and $D_3'$ are on), the current ($i_L$) passing through the inductor $L$ is analyzed as follows provide that the inductor voltage will be $v_L = V_i - V_C$:

$$i_L = I_{L,P} + \frac{1}{L}\int_{DT}^t v_L dt = I_{L,P} + \frac{V_i - V_C}{L}(t - DT) \qquad (3.41)$$

Considering Figure 3.4 for a three-level incremental DC-DC converter assuming that the capacitors $C_1$ to $C_3$ have the same capacitances, as a result the voltage of the capacitors $C_1$ to $C_3$ will be equal, and thus the following relationships are established:

$$V_{C1} = V_{C2} \quad = V_{C3} = V_C$$

$$V_o = 3V_C \tag{3.42}$$

Thus, in reference with equations 2.3 and 3.42 the voltage gain of the three-level DC-DC boost converter in the continuous conduction region can be expressed as:

$$\frac{V_o}{V_i} = \frac{3}{1-D} \tag{3.43}$$

And the average inductor current in this mode for this stage will be given by the equation shown below comparing and relating to the expressions 2.4 and 3.7.

$$I_L = \frac{3^2 V_C}{R(1-D)} \tag{3.44}$$

### 3.2.2 DC-DC three-level boost converter analysis in DCM

The equation 3.45 and 3.46 represents the voltage ratio and average inductors current of the three-level DC-DC boost converter in the discontinuous conduction region and the evaluations are directly related with the derivation procedures followed in equations of 3.8 and 3.9 as shown below respectively.

$$\frac{V_o}{V_i} = 3\frac{\Delta_1 + D}{\Delta_1} \tag{3.45}$$

$$I_L = \frac{3^2 V_C (\Delta_1 + D)}{R\Delta_1} \tag{3.46}$$

### 3.2.3 The effect of the ESR on the voltage gain of three-level DC-DC boost converter

***a. The effect of ESR on the voltage gain of the three-level DC-DC MBC in CCM***

According to Figure 3.4, considering the effect of equivalent series resistance $(R_{ESR,L})$ of the inductor $L$ the converter's boost ratio is limited by the parasitic element as verified in the equation shown below. This equation is evaluated by substituting equations 3.42 and 3.44 in to the expression given by 3.12.

$$V_i = (1-D)\frac{V_o}{3} + \frac{3V_o}{(1-D)R}R_{ESR,L} \tag{3.47}$$

Therefore, the boost ratio of the three-level DC-DC step- up converter considering the effect of the ESR of the inductance $L$ in a CCM can be reduced to the following equation.

$$\frac{V_o}{V_i} = \frac{1}{\frac{1-D}{3} + \frac{3R_{ESR,L}}{(1-D)R}} \tag{3.48}$$

***b. The Effect of the ESR on the voltage gain of three-level DC-DC MBC in DCM***

Based on Figure 3.4, considering the effect of equivalent series resistance $(R_{ESR,L})$ of the inductor $L$ on the converter' voltage gain in a DCM, the simplified equation will be calculated by replacing the relations 3.42 and 3.46 into 3.17 as deduced below.

$$V_i(\Delta_1 + D) = \Delta_1\frac{V_o}{3} + (\Delta_1 + D)\frac{3V_o(\Delta_1 + D)}{R\Delta_1}R_{ESR,L} \tag{3.49}$$

Thus, the voltage gain of the three-level DC-DC step- up converter considering the effect of the ESR of the inductance $L$ in a DCM can be expressed as:

$$\frac{V_o}{V_i} = \frac{(D+\Delta_1)}{\frac{\Delta_1}{3} + \frac{3(\Delta_1 + D)^2}{R\Delta_1}R_{ESR,L}} \tag{3.50}$$

### 3.2.4. The effects of diodes and switch voltage drop in three-level DC-DC MBC

Considering Figure 3.5(a), the voltage equations in the circuit including the elements ($C_2'$, $S$, $C_1$ and $D_2$) and ($C_3'$, $D_3$, $C_2$ and $D_2$) are given by the equations 3.5 and 3.52 respectively.

$$V_{C'2} + V_d - V_{C1} + V_d = 0$$

$$V_{C'2} = V_{C1} - 2V_d \tag{3.51}$$

$$-V_{C'3} + V_d + V_{C2} - V_d = 0 \tag{3.52}$$

Again with reference to Figure 3.5(b), in the loop containing the ($C_2'$, $D_2'$, $C_2$ and $D_1$) and the circuit with ($C_3'$, $D_3'$, $C_3$, and $D_2'$) the voltage expressions are given by the following two equations respectively.

$$-V_{C'2} + V_d + V_{C2} - V_d = 0 \tag{3.53}$$

$$-V_{C'3} + V_d + V_{C3} - V_d = 0 \tag{3.54}$$

Combining the equations 3.51 and 3.53 the voltage of the capacitors $C_2$ will be defined by:

$$V_{C2} = V_{C1} - 2V_d \tag{3.55}$$

Substituting the above equation in to 3.52 the voltage of capacitor $C_3'$ can be expressed as:

$$V_{C'3} = V_{C1} - 2V_d \tag{3.56}$$

And finally by replacing the above relation into 3.54, the voltage of the capacitor $C_3$ is given by:

$$V_{C3} = V_{C1} - 2V_d \tag{3.57}$$

Thus, the total output voltage of the three-level DC-DC converter as indicated on Figure 3.4, considering the effects of diodes and switch voltage drops can be expressed by:

$$V_o = V_{C1} + V_{C2} + V_{C3} = 3V_{C1} - 4V_d \tag{3.58}$$

From the above relation obtained, the efficiency of the switched capacitor of the three-level DC-DC MBC will be given by:

$$\frac{V_o}{3V_{C1}} = \frac{3V_{C1} - (3-1)\times 2V_d}{3V_{C1}} = 1 - \frac{2\times 2V_d}{3V_{C1}} \tag{3.59}$$

### 3.2.5 Design and analysis of the three-level DC-DC boost converter

The minimized value of the output voltage ripple in the three-level DC-DC MBC can be utilized, by selecting an appropriate value for the capacitors. Figure 3.5 shows the possible switching states of the triple-stage DC-DC MBC. As indicated in Figure 3.5(a), when the switch is closed, the capacitors $C_1$ and $C_2$ have a higher voltage than the capacitors $C_2'$ and $C_3'$. During this time interval, the capacitors $C_2'$ and $C_3'$ get charged from the capacitors $C_1$ and $C_2$ through the diodes $D_2$ and $D_3$ respectively. At the moment of switching on of the switch $S$, the capacitors $C_1$ and $C_2'$ are connected in parallel and their equivalent capacitor will be $C = C_1 + C_2'$ and the total charge stored in the capacitors $C_1$ and $C_2'$, at the time before the switch $S$ is turned on will be as follows:

$$Q_{12'}(0^-) = Q_1(0^-) + Q_{2'}(0^-) = C_1 V_{1bc} + C_2' V_{2'bc} \tag{3.60}$$

In the above equation, $Q_{12'}(0^-)$ represents the sum of the stored charge in the capacities $C_1$ and $C_2'$ while $Q_1(0^-)$ and $Q_{2'}(0^-)$ are the charges stored in the capacitors $C_1$ and $C_2'$ at the moment before turning on the switch $S$ respectively. In addition, $V_{1bc}$ and $V_{2'bc}$ are the voltages across the two capacitors $C_1$ and $C_2'$ at the same time. According to the energy conservation principle, the total charge stored before and after of the two complement charging-discharging capacitors is equal.

$$Q_{12'}(0^+) = Q_{12'}(0^-)$$

$$CV = C_1 V_{1bc} + C_2' V_{2'bc}$$

$$V = V_{1ac} = V_{2'ac} = \frac{C_1 V_{1bc} + C_2' V_{2'bc}}{C_1 + C_2'} \tag{3.61}$$

Where, $Q_{12'}(0^+)$ is the total energy stored in capacitors ($C_1$ and $C_2'$) and $V$ is the voltage of the equivalent capacitor of the capacitors $C_1$ and $C_2'$ after the switch $S$ is closed respectively and the voltages of these individual capacitors after charging are $V_{1ac}$ and $V_{2'ac}$. The same procedure is conducted to analysis the relationship of the stored energy before and after charging for the capacitors $C_2$ and $C_3'$ as explained in the above section for the same period of time with an equivalent capacitor $C' = C_2 + C_3'$, the total stored charge in capacitors $C_2$ and $C_3'$ just before the switching on of the switch $S$ is will be as follows:

$$Q_{23'}(0^-) = Q_2(0^-) + Q_{3'}(0^-) = C_2 V_{2bc} + C_3' V_{3'bc} \tag{3.62}$$

In the above expression, $Q_{23'}(0^-)$ is the total charge stored in capacitors ($C_2$ and $C_3'$) and $Q_2(0^-)$, $Q_{3'}(0^-)$, $V_{2bc}$ and $V_{3'bc}$ are the respective voltages and charges for these capacitors at the moment before the switch $S$ is closed. According to the principle of energy conservation, the total energies stored in the capacitors before and after charging are the same.

$$Q_{23'}(0^+) = Q_{23'}(0^-)$$

$$C'V = C_2 V_{2bc} + C_3' V_{3'bc}$$

$$V = V_{2ac} = V_{3'ac} = \frac{C_2 V_{2bc} + C_3' V_{3'bc}}{C_2 + C_3'} \tag{3.63}$$

In this expression, $Q_{23'}(0^+)$ is the total energy stored in the capacitors ($C_2$ and $C_3'$) and $V$ is the voltage of the equivalent capacitance of the two capacitors $C_2$ and $C_3'$ after the switch $S$ have been turned on. As expressed in the above equation, $V_{2ac}$ and $V_{3'ac}$ are the balanced voltages of the two capacitors $C_2$ and $C_3'$ after the complete time process of discharging-charging for the first half cycle. After, the charging process of the capacitors is completed, the diodes $D_2$ and $D_3$ are opened and the capacitors ($C_2'$ and $C_3'$) no more transfer their stored energy into the load. Thus, the voltages of these capacitors remain stable during the switching on state. At the same time, the load is supplied a power by the series arranged capacitors ($C_1, C_2$ and $C_3$) and their voltages dropped down. Further, assuming that all capacitors in the circuit have the same capacitance and their voltage drops ($\Delta v_1$) also be the

same. During the discharge time interval $\Delta t_1$ of the first half cycle the voltage drops, $\Delta v_{C1}$, $\Delta v_{C2}$ and $\Delta v_{C3}$ across the these capacitors and their corresponding flow of the currents $i_{C1} = i_{C2} = i_{C3} = I_o$ are the same. Then the expression of the voltage drops using the approximated equality $\frac{dv_C}{dt} \approx \frac{\Delta v_C}{\Delta t}$ can be rewritten as follows:

$$i_C = C\frac{dv_C}{dt}$$

$$\Delta v_C = \frac{1}{C} i_C \Delta t$$

$$\Delta v_1 = \Delta v_{C1} = \Delta v_{C2} = \Delta v_{C3} = \frac{1}{C_1} i_{C1}\Delta t_1 = \frac{1}{C_2} i_{C2}\Delta t_1 = \frac{1}{C_3} i_{C3}\Delta t_1$$

$$\Delta v_1 = \frac{1}{C_1} I_o \Delta t_1 = \frac{1}{C_2} I_o \Delta t_1 = \frac{1}{C_3} I_o \Delta t_1 \qquad (3.64)$$

The second phase of the conduction mode is analyzed with respect to Figure 3.5(b), during the off state. At the moment when the switch $S$ is opened, the current of the inductor $L$ causes the diode $D_3'$ to turn in on mode. The duration of the switching off mode of the switch $S$ is divided into two time periods $\Delta t_2$ and $\Delta t_3$. In the beginning of the time interval $\Delta t_2$, the voltage of the capacitor $C_3'$ is greater than the voltage of the capacitor $C_3$, while the diode $D_2'$ will be in off state. Also, the sum of the voltages of the two capacitors $C_2'$ and $C_3'$ is more than the sum of the voltages of the two capacitors $C_2$ and $C_3$, so that the diode $D_1$ will be turn off in the same time interval. During, the charging-discharging of time interval $\Delta t_2$ the capacitors $C_2'$ and $C_3'$ are discharged by a current $I_L$, while the capacitors $C_1$, $C_2$ and $C_3$ get charged by the current $I_L - I_o$. At the moment when the voltages of the complement capacitors ($C_3$ and $C_3'$) and capacitors $C_2$ and $C_2'$ as indicated in the brackets are equal, their respective conducting diodes $D_2'$ and $D_1$ are turned on and the time period $\Delta t_3$ starts. Thus, the variable voltage drops across the capacitors $C_1$, $C_2$, $C_3$, $C_2'$ and $C_3'$ in the time intervals $\Delta t_2$ and $\Delta t_3$ are analyzed and calculated as follows respectively. The increased values of the voltage drops $\Delta v_2$, $\Delta v_3$ and $\Delta v_4$ of the capacitors $C_1$, $C_2$ and $C_3$ in the time interval $\Delta t_2$ provided that the charging currents $i_{C1} = i_{C2} = i_{C3} = I_L - I_o$ is written as:

$$\Delta v_2 = \Delta v_3 = \Delta v_4 = \frac{1}{C_1} i_{C1} \Delta t_2 = \frac{1}{C_2} i_{C2} \Delta t_2 = \frac{1}{C_3} i_{C3} \Delta t_2$$

$$\Delta v_2 = \Delta v_3 = \Delta v_4 = \frac{1}{C_1} (I_L - I_o) \Delta t_2 = \frac{1}{C_2} (I_L - I_o) \Delta t_2 = \frac{1}{C_3} (I_L - I_o) \Delta t_2 \qquad (3.65)$$

The amount of voltage drops $\Delta v_5$ and $\Delta v_6$ across the two capacitors $C_2'$ and $C_3'$ in the same time interval $\Delta t_2$ given that the discharging currents $i_{C'2} = i_{C'3} = I_L$ can be defined as:

$$\Delta v_5 = \Delta v_6 = \frac{1}{C_2'} i_{C'2} \Delta t_2 = \frac{1}{C_3'} i_{C'3} \Delta t_2$$

$$\Delta v_5 = \Delta v_6 = \frac{1}{C_2'} I_L \Delta t_2 = \frac{1}{C_3'} I_L \Delta t_2 \qquad (3.66)$$

In the last time interval $\Delta t_3$ of the off state, the capacitors ($C_2$ with $C_2'$) and capacitors ($C_3$ with $C_3'$) are aligned in parallel and delivers power to the load in series with the capacitor $C_1$ with a discharging current $\frac{I_o}{2}$. But, the capacitor $C_1$ continues charging with a current $I_L - I_o$ until the cycle terminated. The voltage drops $\Delta v_7$ and $\Delta v_8$ across the two capacitors $C_2$ and $C_2'$ over the time interval $\Delta t_3$ for $i_{C2} = i_{C'2} = \frac{I_o}{2}$ will be expressed as follows:

$$\Delta v_7 = \Delta v_8 = \frac{1}{C_2} i_{C2} \Delta t_3 = \frac{1}{C_2'} i_{C'2} \Delta t_3$$

$$\Delta v_7 = \Delta v_8 = \frac{1}{C_2} \left( \frac{I_o}{2} \right) \Delta t_3 = \frac{1}{C_2'} \left( \frac{I_o}{2} \right) \Delta t_3 \qquad (3.67)$$

The values of the voltage drop $\Delta v_9$ and $\Delta v_{10}$ across the capacitors $C_3$ and $C_3'$ in the same time interval $\Delta t_3$, provided that $i_{C3} = i_{C'3} = \frac{I_o}{2}$ can be defined as:

$$\Delta v_9 = \Delta v_{10} = \frac{1}{C_3} i_{C3} \Delta t_3 = \frac{1}{C_3'} i_{C'3} \Delta t_3$$

$$\Delta v_9 = \Delta v_{10} = \frac{1}{C_3} \left( \frac{I_o}{2} \right) \Delta t_3 = \frac{1}{C_3'} \left( \frac{I_o}{2} \right) \Delta t_3 \qquad (3.68)$$

And finally the voltage drop $\Delta v_{11}$ across the charging capacitors $C_1$ during the time interval $\Delta t_3$ for $i_{C1} = I_L - I_o$ is given by:

$$\Delta v_{11} = \frac{1}{C_1} i_{C1} \Delta t_3$$

$$\Delta v_{11} = \frac{1}{C_1} (I_L - I_o) \Delta t_3 \qquad (3.69)$$

The output voltage ripple of the three-level DC-DC boost converter is equal to $v_{C1} + v_{C2} + v_{C3}$. So that, the output voltage ripple can be expressed as the sum of the voltage ripples of the capacitor $C_1$, $C_2$, and $C_3$. The wave forms of the voltage ripples of the capacitors ($C_1$, $C_2$, $C_3$, $C_2'$ and $C_3'$) and the output voltage ripple are shown in Figure3.7.

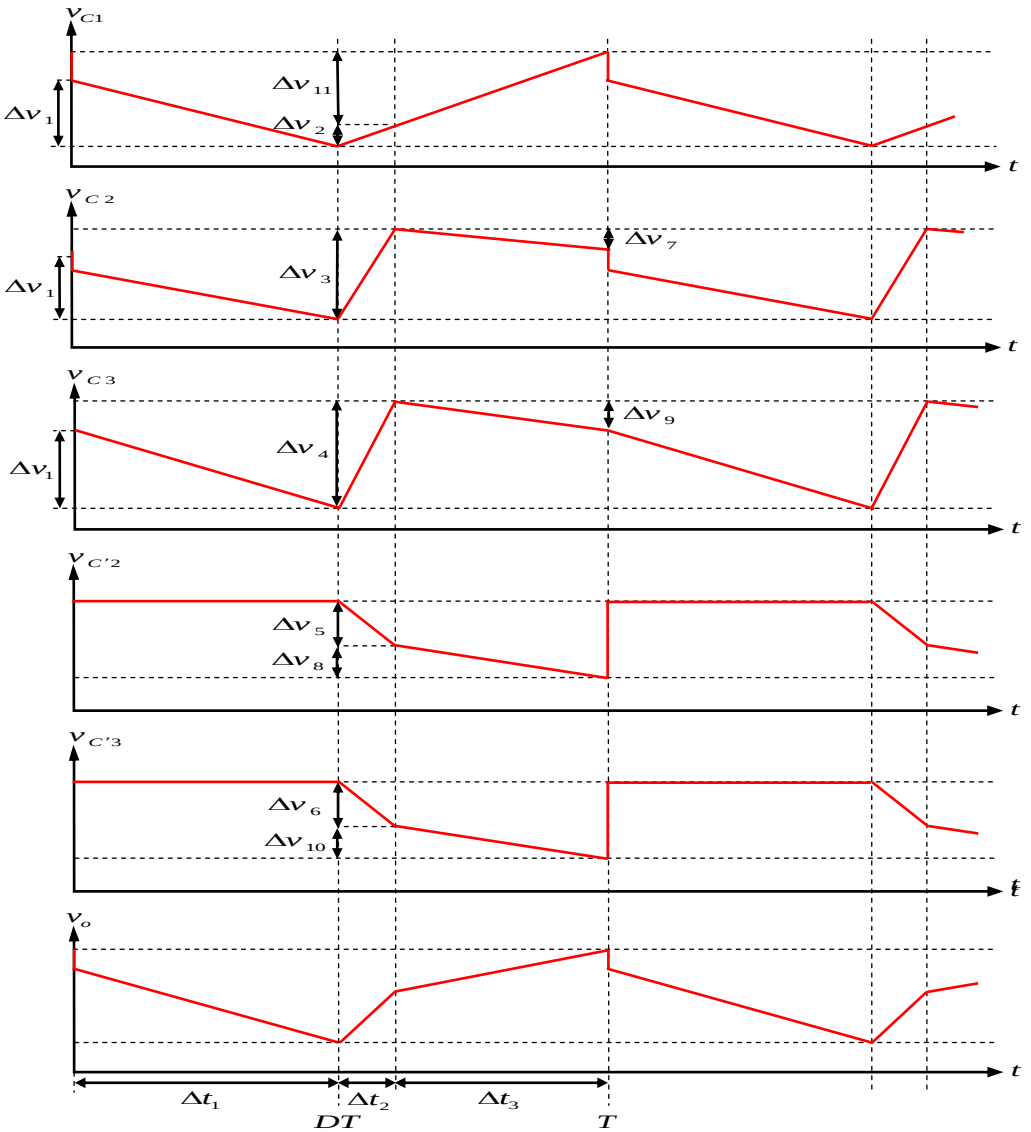



**Figure 3.7:** Voltage ripple waveforms for capacitors ($C_1$, $C_2$, $C_3$, $C_2'$ and $C_3'$) and output voltage

### 3.2.6 Voltage stress on the switch in three-level DC-DC step up converter

In reference to Figure 3.5(b), during the switching off mode in the circuit including the switch $S$, capacitor $C_1$ and diode $D_1$, based on the expression 3.42, the voltage stress on the switch in the three-level MBC can be defined by the following formula:

$$V_S = V_C = \frac{V_o}{3} \tag{3.71}$$

## 3.3 DC-DC Four-Level Boost Converter

The four-level incremental DC-DC converter circuit is shown in Figure 3.8.

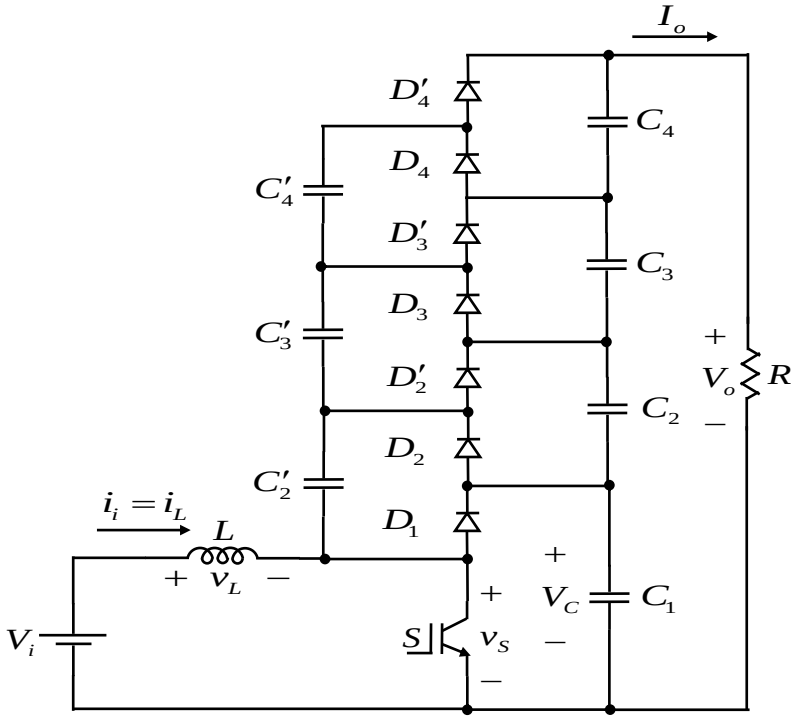
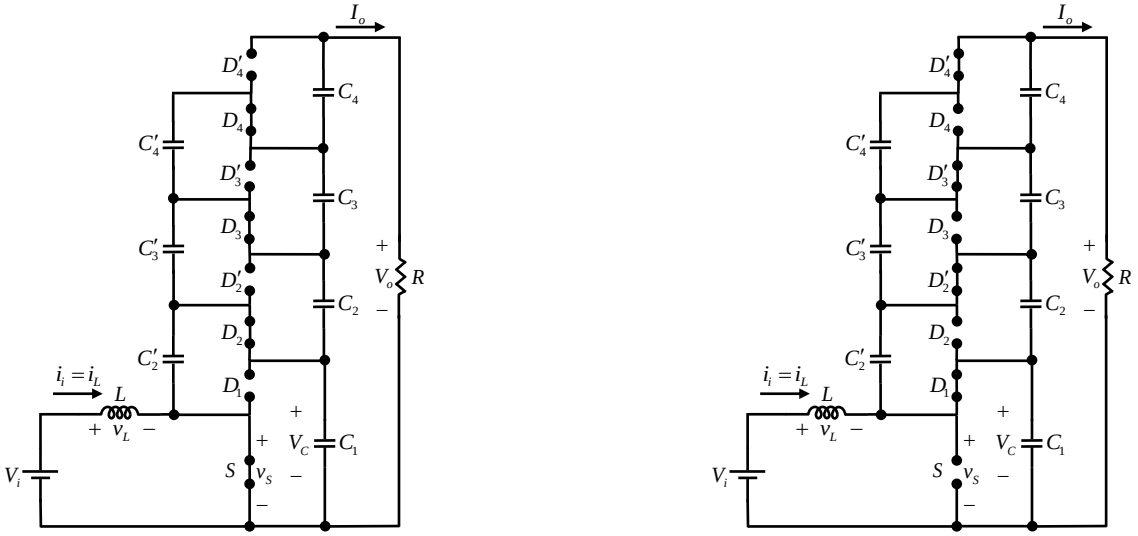



**Figure 3.8:** Four-level DC-DC MBC circuit diagram

The equivalent circuit of the four-level boost converter in the interval when the switch $S$ is turned on is shown in Figure 3.9(a). As shown in Figure 3.9(a), the inductor $L$ is connected to the input voltage source $V_i$ during the switching on period of the switch $S$. During this time interval, due to the existence of the higher voltages across the load feeding capacitors( $C_1, C_2, C_3$ and $C_4$) causes diodes ( $D_1, D'_2, D'_3$ and $D'_4$) to be turn off, while the presence of

smaller voltages across the capacitors ($C_2'$, $C_3'$ and $C_4'$) than the capacitors($C_1$, $C_2$ and $C_3$), causes the diodes ($D_2$, $D_3$ and $D_4$) in on mode respectively.




(a) On mode (b) Off mode

**Figure 3.9:** Circuit diagram of the four-level DC-DC MBC for on/off modes

The equivalent circuit diagram of the four-level DC-DC MBC in the interval when the switch $S$ is off is shown in Figure 3.9(b). In this time interval, the inductor's $L$ current reaches is maximum peak causes the diodes $D_1$, $D_2'$, $D_3'$ and $D_4'$ in on mode. However, as a result of the balanced voltage present across the capacitors ($C_2'$, $C_3'$ and $C_4'$) charged during the first cycle makes the diodes($D_2$, $D_3$ and $D_4$) to be in open mode respectively. The wave forms of the voltage and current sources of this level of converter are shown in Figure 3.10. In this figure, 1 means high and 0 means low of the switch $S$. In the $(1-D)T$ time interval (when the switch $S$ is off and the diodes $D_1$, $D_2'$, $D_3'$ and $D_4'$ are switched on), the voltage of the switch $S$ will be the same as the voltage across the capacitor ($v_S = V_C$). At the time interval $DT$ (when the switch $S$ and $D_2$, $D_3$ and $D_4$ diodes are on) the voltage of the switch $S$ is zero. In the following sections, the four-level DC-DC MBC is analyzed in continuous and discontinuous conduction regions.

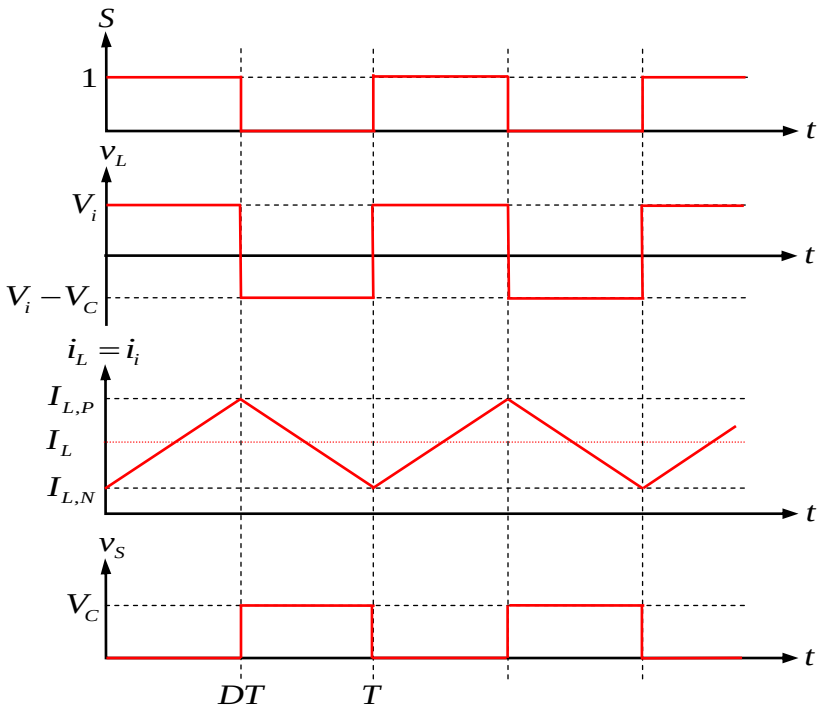



**Figure 3.10:** Voltage and current waveforms of the four-level DC-DC MBC

### 3.3.1 Analysis of the four-level DC-DC MBC in CCM

In the $DT$ time interval (when the switch $S$, $D_2$, $D_3$ and $D_4$ diodes is on), the flow of the current $I_L$ through the inductor can be analyzed as :

$$i_L = I_{L,N} + \frac{1}{L}\int_0^t v_L dt = I_{L,N} + \frac{V_i}{L}t \qquad (3.72)$$

In the next time interval $(1-D)T$ (when the switch $S$ is off and $D_1$, $D_2'$, $D_3'$ and $D_4'$ diodes are on), the current ( $I_L$ ) passing through the inductor $L$ can be defined as:

$$i_L = I_{L,P} + \frac{1}{L}\int_{DT}^t v_L dt = I_{L,P} + \frac{V_i - V_C}{L}(t - DT) \qquad (3.73)$$

With reference to Figure 3.8 for a four-level DC-DC MBC, assuming that the capacitors $C_1$ to $C_4$ have the same capacitance and the voltages across the capacitors $C_1$ to $C_4$ will be equal, then the expression of the voltages will be as shown below:

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_C$$

$$V_o = 4V_C \tag{3.74}$$

According to the equations 2.3 and 3.74, the voltage gain of the four-level incremental DC-DC converter in CCM will be as follows:

$$\frac{V_o}{V_i} = \frac{4}{1-D} \tag{3.75}$$

Based on previous derived average current equations for two and three levels the average inductor current for four-level MBC is deduced as:

$$I_L = \frac{4^2 V_C}{R(1-D)} \tag{3.76}$$

### 3.3.2 Analysis of the four levels DC-DC MBC in DCM

Combining the on equations 2.11 and 3.74, the boost ratio of the four-level DC-DC MBC in DCM will be defined as follows:

$$\frac{V_o}{V_i} = 4\frac{\Delta_1 + D}{\Delta_1} \tag{3.77}$$

And the inductor current in DCM is expressed as:

$$I_L = \frac{4^2 V_C(\Delta_1 + D)}{R\Delta_1} \tag{3.78}$$

### 3.3.3 The Effect of the ESR on the voltage gain of four-level DC-DC MBC

#### *a. The Effect of the ESR on the voltage gain of four-level DC-DC MBC in CCM*

According to Figure 3.8, considering the effect of the equivalent series resistance $R_{ESR,L}$ of the inductor $L$, the following relations are valid for the inductor's voltage in the interval $DT$ and $(1-D)T$, when the switch $S$ is on and the switch $S$ is off. When the expressions 3.74 and 3.76 are replaced in equation 3.12, the voltage gain of the four-level DC-DC MBC considering the effect of the ESR of the inductor $L$ in CCM is given by:

$$V_i = (1-D)\frac{V_o}{4} + \frac{4V_o}{(1-D)R}R_{ESR,L}$$

$$\frac{V_o}{V_i} = \frac{1}{\frac{1-D}{4} + \frac{4R_{ESR,L}}{(1-D)R}} \tag{3.79}$$

In Figure 3.11, the voltage gain of the four-level incremental DC-DC converter is plotted against the duty cycle for different values of $\frac{R_{ESR,L}}{R}$. It is seen that the shape of the graph exhibits a larger quasi-linear region compared to the conventional converter. When the operating duty cycle is closer to unity, the region of the graph is getting more nonlinear. In such way, the graph proves that the boost ratio for the four-level incremental DC-DC converter can be improved best, if the converter operates with a duty cycle closer to $D$ = 0.5. So that, $D$ = 0.5 provides the best point for the four-level structure, even for all multilevel topologies.

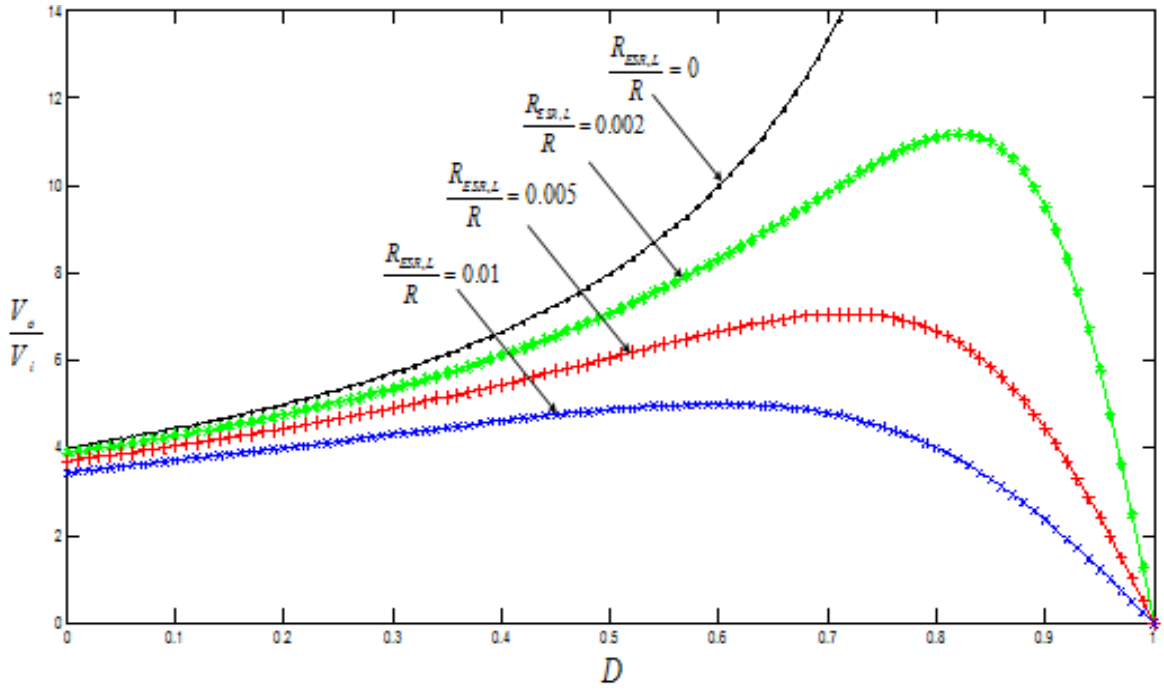



**Figure 3.11:** Four-level MBC boost ration variation curve against operating duty cycle for different values of $\frac{R_{ESR,L}}{R}$

***b. The Effect of inductor's ESR on the boost ratio of MBC ( n =4) in DCM***

In reference to Figure3.8, considering the effect of the equivalent series resistance ESR of the inductor $L$ , in the interval $DT$ and $(1-D)T$ , when the switch $S$ is on and the switch $S$ is off in DCM , the boost ratio of the four-level DC-DC MBC can be expanded as shown below by substituting the equations 3.74 and 3.78 into the relation 3.17.

$$V_i(\Delta_1 + D) = \Delta_1 \frac{V_o}{4} + (\Delta_1 + D)\frac{4V_o(\Delta_1 + D)}{R\Delta_1} R_{ESR,L}$$

$$\frac{V_o}{V_i} = \frac{(D + \Delta_1)}{\frac{\Delta_1}{4} + \frac{4(\Delta_1 + D)^2}{R\Delta_1} R_{ESR,L}} \tag{3.80}$$

### 3.3.4. Evaluation of the diodes and switch voltage drop effects on the four-level DC-DC MBC

Consider, in reference to Figure 3.9(a), the voltage equations in the circuit including ( $C_2'$ , $S$ , $C_1$ and $D_2$ ), ( $C_3'$ , $D_3$ , $C_2$ and $D_2$ ) and ( $C_4'$ , $D_4$ , $C_3$ and $D_3$ ) are given by the following expressions.

$$V_{C'2} + V_d - V_{C1} + V_d = 0$$

$$V_{C'2} = V_{C1} - 2V_d \tag{3.81}$$

$$-V_{C'3} + V_d + V_{C2} - V_d = 0 \tag{3.82}$$

$$-V_{C'4} + V_d + V_{C3} - V_d = 0 \tag{3.83}$$

According to Figure 3.9(b), the voltage expressions in the circuit containing ( $C_2'$ , $D_2'$ , $C_2$ and $D_1$ ), ( $C_3'$ , $D_3'$ , $C_3$ and $D_2'$ ) and ( $C_4'$ , $D_4'$ , $C_4$ and $D_3'$ ) considering the effect of diodes and switch can be given as shown below respectively.

$$-V_{C'2} + V_d + V_{C2} - V_d = 0 \tag{3.84}$$

$$-V_{C'3} + V_d + V_{C3} - V_d = 0 \tag{3.85}$$

$$-V_{C'4} + V_d + V_{C4} - V_d = 0 \tag{3.86}$$

Then, the voltage drop across the capacitors $C_2$ combining equations 3.81 and 3.84 will be:

$$V_{C2} = V_{C1} - 2V_d \tag{3.87}$$

And the voltage of capacitor $C_3$ can be calculated by mixing the relations 3.82 and 3.87 as shown below:

$$V_{C'3} = V_{C1} - 2V_d \tag{3.88}$$

By replacing the above relation in to 3.85 the voltage of the capacitors $C_3$ will be defined by:

$$V_{C3} = V_{C1} - 2V_d \tag{3.89}$$

Again, combining the expressions 3.83 and 3.89 the voltage drop across the capacitor $C_4'$ will be given as:

$$V_{C'4} = V_{C1} - 2V_d \tag{3.90}$$

Finally, the voltage across the capacitor $C_4$ can be evaluated by substituting the above equation in to (3.86) as:

$$V_{C4} = V_{C1} - 2V_d \tag{3.91}$$

Thus, based on all the equations derived the output voltage of the four-level DC-DC converter is represented by the following equation:

$$V_o = V_{C1} + V_{C2} + V_{C3} + V_{C4} = 4V_{C1} - 6V_d \tag{3.92}$$

Therefore, according to the above relation of the output voltage expression for the four-level DC-DC MBC, the efficiency of the switched capacitor of the converter is given by the equation provided below, while considering the effect of the diodes and switch voltage drops on the converter:

$$\frac{V_o}{4V_{C1}} = \frac{4V_{C1} - (4-1)\times 2V_d}{4V_{C1}} = 1 - \frac{3\times 2V_d}{4V_{C1}} \tag{3.93}$$

### 3.3.5 Design of four-level DC-DC boost converter

The ripples of the output voltage of the four-level DC-DC boost converter are reduced to the minimum required value by selecting appropriate values for the capacitors. Figure 3.9 shows the possible switching state power circuit diagrams. As shown in Figure 3.9(a), capacitors $C_1, C_2,$ and $C_3$ have a higher voltage than the capacitors $C_2', C_3'$ and $C_4'$ when the switch $S$ is closed. The capacitors $C_1, C_2$ and $C_3$ transfers energy to the capacitors $C_2', C_3'$ and $C_4'$ through the diodes $D_2, D_3,$ and $D_4$ until their voltages are balanced respectively. After this moment, the $D_2, D_3$ and $D_4$ diodes are turned off and the capacitors $C_2', C_3'$ and $C_4'$ stopes from transferring their energy to the load. Thus, their voltage remains stable during the switching on of the switch $S$. However, the capacitors $C_1, C_2, C_3$ and $C_4$ arranged in series starts to reduce in voltages as they supply power to the load.

During, the next half cycle with reference to Figure 3.9(b), when the switch $S$ is opened, the current of the inductor $L$ forward biased the diode $D_4'$. The duration of the switching off of the switch $S$ can be divided into two time intervals $\Delta t_2$ and $\Delta t_3$. At starting time of $\Delta t_2$, the voltage of the capacitor $C_4'$ is greater than the voltage of the capacitor $C_4$ as well as the sum of the voltages of the two capacitors ($C_3'$ and $C_4'$) and the sum of the voltages of the capacitors ($C_2', C_3'$ and $C_4'$) is more than the sum of the voltages of their complement capacitors ($C_3$ and $C_4$) and capacitors($C_1, C_2, C_3,$ and $C_4$) respectively. As a result their corresponding respective diodes $D_3', D_2'$ and $D_1$ are in reveres biased mode. During this time interval ($\Delta t_2$), the capacitors $C_2', C_3'$ and $C_4'$ starts to discharge with a current $I_L$ and the capacitors $C_1, C_2, C_3,$ and $C_4$ get charged by the current $I_L - I_o$. At the moment when the voltages of the compliment couple capacitors ($C_4$ and $C_4'$), capacitors ($C_3$ and $C_3'$) and capacitors ($C_2$ and $C_2'$) as indicated in the brackets are equal, their corresponding diodes $D_3'$, $D_2'$ and $D_1$ are automatically turned on respectively. Then, the second time period ($\Delta t_3$) of the off state starts and the capacitors $C_2$ and $C_2'$, capacitors $C_3$ and $C_3'$, and the capacitors $C_4$ and $C_4'$ are arranged in parallel. At this time, the capacitors ($C_2$ and $C_2'$), capacitors ($C_3$ and $C_3'$

) and capacitors ( $C_4$ and $C_4'$ ) are discharged by the current $\frac{I_o}{2}$ and the capacitor $C_1$ continues to charge until the cycle ends with a current $I_L - I_o$.

### 3.3.6 Voltage stress on the switch in four-level MBC

In reference to Figure 3.9(b), during the switching off mode of the switch $S$, in the loop including switch $S$, capacitor $C_1$ and the diode $D_1$, the voltage of the switch is defined as:

$$V_S = V_C \tag{3.94}$$

By substituting equation 3.74, into the above relation the voltage stress on the switch for the four-level MBC can be rewritten as follows:

$$V_S = \frac{V_o}{4} \tag{3.95}$$

## 3.4 DC-DC $n$-Level Multilevel Boost Converter (MBC)

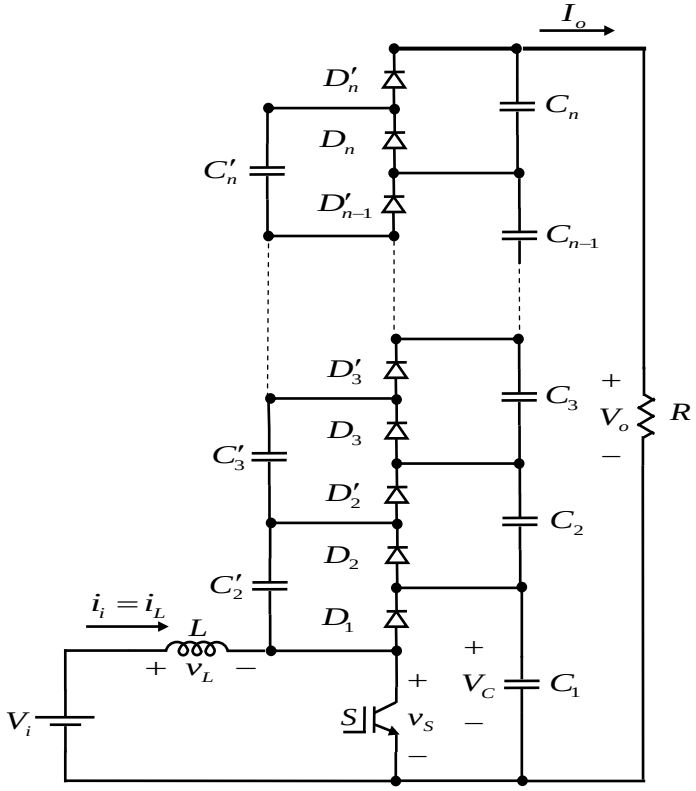



**Figure 3.12:** Power circuit diagram for DC-DC $n$-level MBC

Figure 3.12 shows the DC-DC converter circuit of the $n$-level MBC, which includes $n$ number of voltage levels. In this figure, the first stage consists of the switch $S$, diode $D_1$ and capacitor $C_1$, and the second level consists of diodes ($D_2$ and $D_2'$) and capacitors ($C_2$ and $C_2'$). For a general statement after the first stage of each level, there are two diode and two capacitors are added. Consequently, the are a total of $n$ times DC-DC MBC consists of $2n-1$diodes, $2n-1$capacitors, one switch, one inductor, $n$ times output voltage levels and $n+1$ number of converters level with respect to zero voltage level. The wave forms of the voltages and currents of the $n$-times DC-DC MBC are indicated in Figure 3.13. In this figure 1, indicates high and 0 represents low of the switch $S$. In the time interval $(1-D)T$ (when the switch $S$ is off and the diodes $D_1$, $D_2'$, $D_3'$, $D_4'$ to $D_n'$ are on) the voltage stress of this topology on the switch in the circuit including the switch $S$, diode $D_1$ and capacitor $C_1$ will be $v_S = V_C$. At the time interval $DT$ (when the switch $S$ and diodes $D_2$, $D_3$, $D_4$ and $D_n$ are on), the voltage of the switch $S$ is zero. In this proceeding section, the $n$-level DC-DC MBC is analyzed in continuous and discontinuous conduction modes.

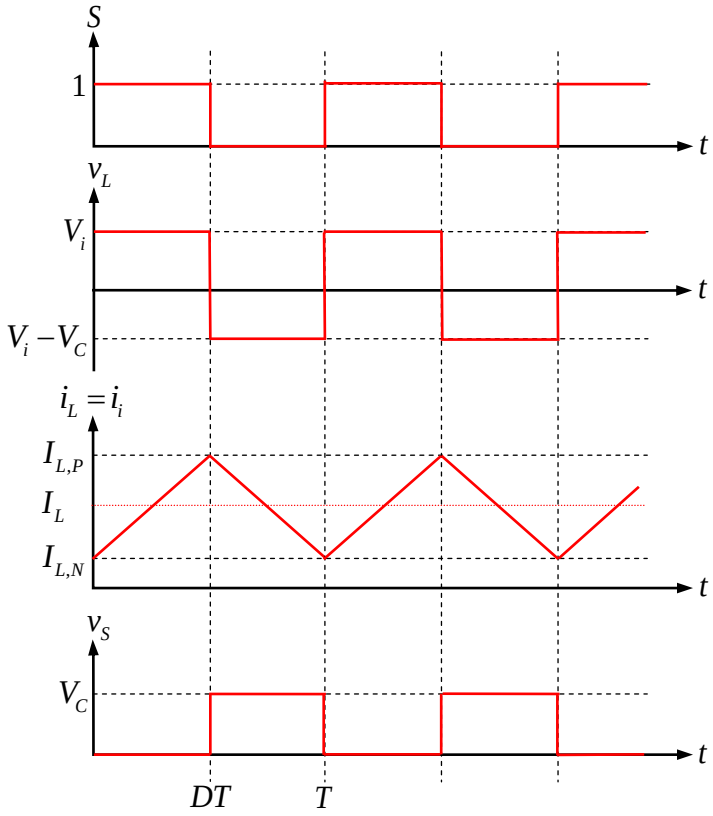



**Figure 3.13:** Voltage and current waveforms of the $n$-level DC-DC MBC

### 3.4.1 Analysis of $n$-level DC-DC MBC in CCM

The current $i_L$ passing through the inductor $L$ in the time interval $DT$ (when the switch $S$ and diodes $D_2$, $D_3$, $D_4$ to $D_n$ are on), is expressed as:

$$i_L = I_{L,N} + \frac{1}{L}\int_0^t v_L dt = I_{L,N} + \frac{V_i}{L}t \tag{3.96}$$

During the next half cycle in the time interval $(1-D)T$ (when the switch $S$ is off and the diodes $D_1$, $D_2'$, $D_3'$, $D_4'$ to $D_n'$ are on), the current $i_L$ passing through the inductor $L$ is written as:

$$i_L = I_{L,P} + \frac{1}{L}\int_{DT}^t v_L dt = I_{L,P} + \frac{V_i - V_C}{L}(t - DT) \tag{3.97}$$

According to the design of the power circuit diagram Figure 3.12, in order to reduce the converter's cost and to have a balance output voltage levels assume that all the capacitors $C_1$ to $C_n$ have the same capacitance and the voltages of the capacitors $C_1$ to $C_n$ will be equal. Then the following conditions are concluded in relation to the voltages across all capacitors.

$$V_{Cj} = V_C \qquad for \quad j = 1, 2, \ldots, n$$
$$V_o = nV_C \tag{3.98}$$

Based on the relationship of the expressions 2.3 and 3.98, the voltage gain of the $n$-level DC-DC MBC in CCM will be defined as:

$$\frac{V_o}{V_i} = \frac{n}{1-D} \tag{3.99}$$

The formula for calculating the average inductor current $I_L$ for $n$-level DC-DC MBC in CCM can be formulated by substituting equation 3.98 into 3.5 considering the relationships of the output power and input power as given by the relation $V_i I_i = V_o I_o$ and combining with the equation 2.3 provided that $I_i = I_L$, the expression can be expanded as shown by 3.101.

$$V_o \times \frac{V_o}{R} = nV_C \times \frac{nV_C}{R} = \frac{n^2 {V_C}^2}{R} = V_i I_i$$

$$I_L = \frac{1}{V_i} \times \frac{n^2 {V_C}^2}{R} = \frac{V_C}{V_i} \times \frac{n^2 V_C}{R} \quad (3.100)$$

$$I_L = \frac{n^2 V_C}{R(1-D)} \quad (3.101)$$

### 3.4.2 Analysis of *n*-level DC-DC MBC in DCM

According to the relations 2.11 and 3.98, the boost ratio of the $n$-level DC-DC MBC in DCM will be defined as:

$$\frac{V_o}{V_i} = n\frac{D+\Delta_1}{\Delta_1} \quad (3.102)$$

In the discontinuous conduction region, according to the relations 2.11 and 3.100, the average flow of the inductor's current of the $n$-level DC-DC MBC will be as follows:

$$I_L = \frac{n^2 V_C (\Delta_1 + D)}{R\Delta_1} \quad (3.103)$$

### 3.4.3 The Effect of the ESR on the voltage gain of *n*-level DC-DC MBC

#### *a. The Effect of the ESR on the voltage gain of n-level DC-DC MBC in CCM*

According to the power circuit of Figure 3.12, considering the effect of the inductor's equivalent series resistance ( $R_{ESR,L}$ ) over the whole period of time operation, the boost ratio of the $n$-level DC-DC MBC in CCM will be as follows by combining the expressions 3.12, 3.98 and 3.10.

$$V_i = (1-D)\frac{V_o}{n} + \frac{nV_o}{(1-D)R} R_{ESR,L}$$

$$\frac{V_o}{V_i} = \frac{1}{\frac{1-D}{n} + \frac{nR_{ESR,L}}{(1-D)R}} \quad (3.104)$$

***b. The Effect of the ESR on the voltage gain of the $n$-level DC-DC MBC in DCM***

Based on the circuit diagram of the Figure 3.12, the voltage gain of the $n$-level DC-DC MBC in DCM considering the effect of the ESR of the inductor $L$, by substituting the expressions 3.98 and 3.103 into 3.17 can be defined as:

$$V_i(\Delta_1 + D) = \Delta_1 \frac{V_o}{n} + (\Delta_1 + D)\frac{nV_o(\Delta_1 + D)}{R\Delta_1} R_{ESR,L}$$

$$\frac{V_o}{V_i} = \frac{(D + \Delta_1)}{\frac{\Delta_1}{n} + \frac{n(\Delta_1 + D)^2}{R\Delta_1} R_{ESR,L}} \qquad (3.105)$$

### 3.4.4 Diodes and switch voltage drop effects on DC-DC MBC

Based on the investigations and similarities made through the expressions 3.25, 3.59 and 3.93, considering the effect of the diodes and switch voltage drops on the converter the efficiency for the switched capacitor MBC for $n$-levels can be expressed as:

$$\frac{V_o}{nV_{C1}} = \frac{nV_{C1} - (n-1)\times 2V_d}{nV_{C1}} = 1 - \frac{(n-1)\times 2V_d}{nV_{C1}} \qquad (3.106)$$

Analyzing the behavior of the MBC with respect to the equation 3.106, it is observed that a multilevel multiplier DC-DC converter is ideal for the applications with a number of hundred volts, in which $V_d$ can be ignored compared with lower voltage $V_C$. Thus, the power loss of the switch will be evaluated as the conventional step-up converter. It should be pointed out that, the switching losses are directly proportional to voltage that the switch able to block, which is the most important significance of this topology to turn down the effect of this switch stress in comparison with other methodologies.

### 3.4.5 Design of the DC-DC $n$-level MBC

The ripples of the output voltage for $n$-level DC-DC MBC can be monitored and reduced to the required value, by defining the exact capacitors value used for design. According to Figure 3.12, when the switch $S$ is closed, the capacitors ($C_1, C_2, C_3$ to $C_{n-1}$) have a higher value of voltages than the capacitors ($C_2', C_3', C_4'$ to $C_n'$). During this time interval, the capacitors $C_1, C_2, C_3$ to $C_{n-1}$ charge capacitors ($C_2', C_3', C_4'$ to $C_n'$) through the diodes($D_2, D_3, D_4$

to $D_n$) respectively. After the charging-discharging capacitors voltages are balanced, the diodes $D_2$, $D_3$, $D_4$, and $D_n$ are reverse biased and the capacitors ($C_2'$, $C_3'$, $C_4'$ to $C_n'$) stopes from delivering their energy to the load and their voltage exhibit a stable graph during the whole switching on period of the switch $S$. At the same time, the load is supplied a power from the series arranged capacitors $C_1$, $C_2$, $C_3$, $C_{n-1}$ to $C_n$ and their voltage dropped to feed the load. The duration of the switching off cycle of the switch $S$ is divided into two sub time intervals ($\Delta t_2$ and $\Delta t_3$). In first interval $\Delta t_2$ of this cycle, the capacitors $C_2'$, $C_3'$, $C_4'$ to $C_n'$ are discharged by the current $I_L$, and the capacitors $C_1$, $C_2$, $C_3$ to $C_n$ are charged by the $I_L - I_o$ current. During, the second time interval $\Delta t_3$ of this period the complement capacitors ($C_2$ and $C_2'$), ($C_3$ and $C_3'$), ($C_4$ and $C_4'$) to the capacitors ($C_n$ and $C_n'$) are placed in parallel ready to deliver power to the load. Thus, the capacitors ($C_2$ and $C_2'$), capacitors ($C_3$ and $C_3'$), capacitors ($C_4$ and $C_4'$) to capacitors ($C_n$ and $C_n'$) start to discharged by a current $\frac{I_o}{2}$ and the base capacitor $C_1$ continues to charge with a current $I_L - I_o$ to store energy for the next repeated cycle.

### 3.4.6 Voltage stress on the switch in DC-DC *n*-level MBC

According to Figure 3.12, the voltage stress on the switch during the switching off mode in the circuit including the switch $S$, capacitor $C_1$, and diode $D_1$, will be given by $V_S = V_C$. Therefore, based on the correspondence and explorations made on the expressions 3.38, 3.71 and 3.95 the voltage stress on the switch for $n$-level DC-DC MBC will be rewritten as:

$$V_S = \frac{V_o}{n} \tag{3.107}$$

### 3.4.7 The efficiency and output voltage ripples of the DC-DC n-level MBC

Assume that the converter is designed considering the effect of the inductor's ESR, then the efficiency for any level of MBC is analyzed using the formulas 3.5, 3.98 and 3.101 in the efficiency equation provided below.

$$\eta = \frac{P_o}{P_i} = \frac{P_o}{P_o + I_L{}^2 R_L} = \frac{\frac{V_o{}^2}{R}}{\frac{V_o{}^2}{R} + I_L{}^2 R_L}$$

$$= \frac{\frac{(nV_C)^2}{R}}{\frac{(nV_C)^2}{R} + \frac{n4V_c{}^2}{R^2(1-D)^2} R_L}$$

$$\eta = \frac{1}{1 + \frac{n^2 R_L}{(1-D)^2 R}} \qquad (3.108)$$

The above expression indicates the general efficiency equation for MBC of any level. If the converter is one-level (convectional boost converter) the relation is deduced to the formula as given below and it is understood that our converter operates in ideal mode if the effect of the ESR is neglected.

$$\eta = \frac{1}{1 + \frac{R_L}{(1-D)^2 R}} \qquad (3.109)$$

The efficiency of a multilevel boost converter for ($n$ =4) is drown against duty cycle for various values of $\frac{R_L}{R}$ in the next page as shown in Figure 3.14.

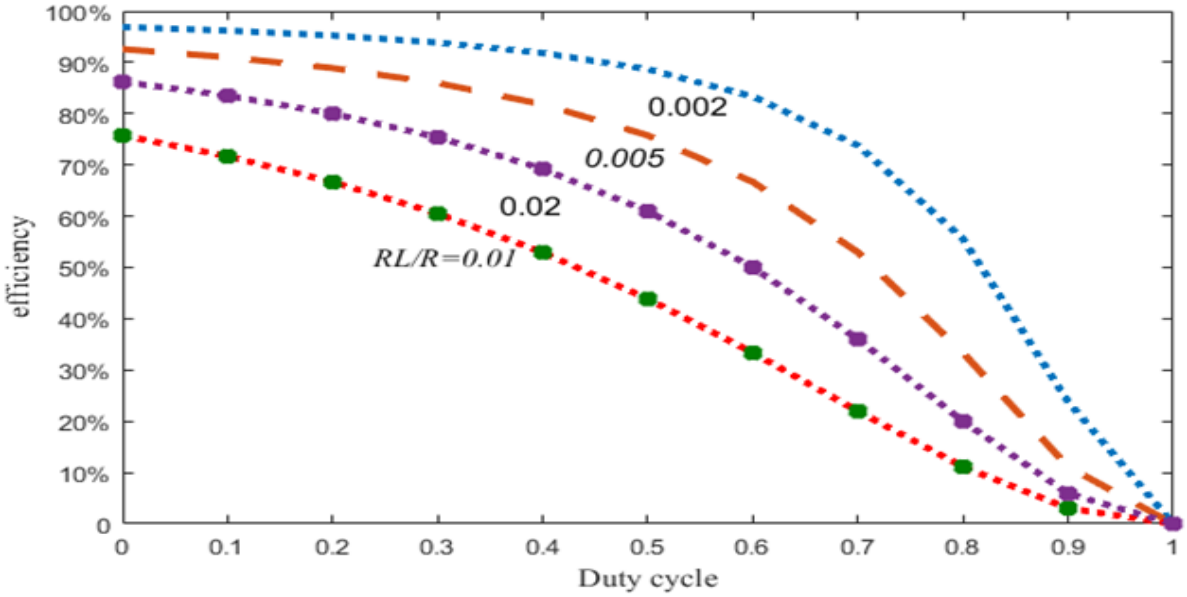



**Figure 3.14:** Efficiency against duty cycle for ($n$ =4) MBC of figure 3.8

Equation 3.108 can be also rewritten as the expression shown below:

$$\eta = \frac{1}{1+\frac{P_o n^2 R_L}{P_o (1-D)^2 R}}$$

$$\eta = \frac{1}{1+\frac{V_o^2 n^2 R_L}{P_o R (1-D)^2 R}} \tag{3.110}$$

The above equation is another way which compares the efficiency of MBC with the output power for any level of the convert for $\frac{R_L}{R} = 0.002$ as clearly shown in the graph labeled in Figure 3.15.

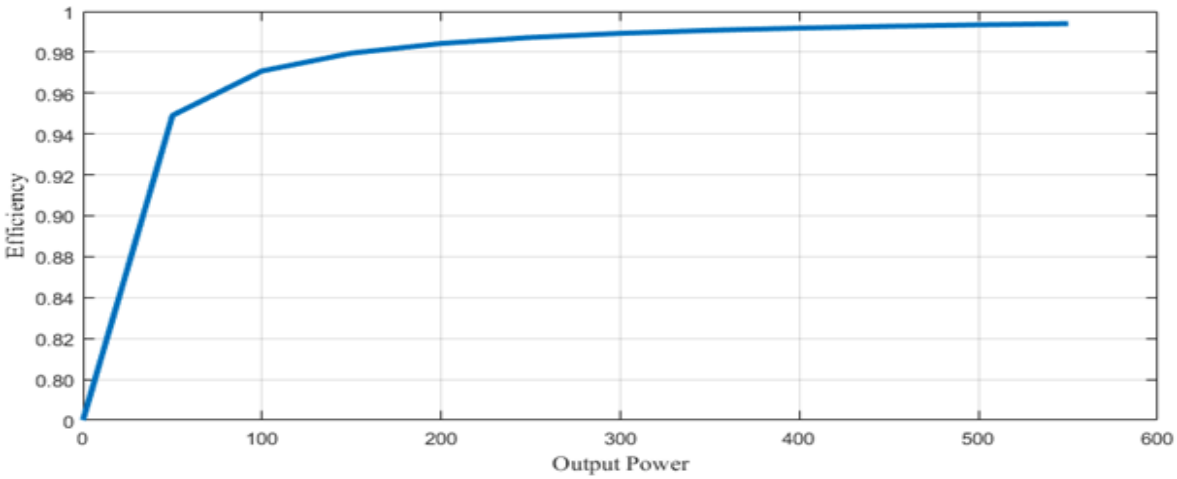



**Figure 3.15:** Efficiency versus output power for ( $n$ =4) MBC of figure 3.8

The output voltage ripples of the MBC for any level of the converter based on the investigations made and as shown in Figures 3.3 and 3.7 the voltage ripples of all load feeding capacitors are equal and the ripples of the output voltage is the summation of all load power supplying capacitors.

$$\Delta v_{C1} = \Delta v_{C2} = \Delta v_{C3} ..... = \Delta v_{Cn} = \Delta v_C \tag{3.111}$$

$$\Delta v_o = \Delta v_{C1} + \Delta v_{C2} + \Delta v_{C3} + ..... + \Delta v_{Cn} = n\Delta v_C$$

$$\Delta v_O = \Sigma_1^n \Delta v_{Cn} = n\Delta v_C \tag{3.112}$$

Combining the expressions of 2.19, 3.99 and 3.112 the output voltage ripples of the MBC is given by:

$$\Delta Vo = \frac{ViDn^2}{CfR(1-D)} \tag{3.113}$$

### 3.5 The Structure of the Dual-Level DC-DC BC with Central Voltage Source (CVS)

In this section, a tactical improvement is made to the structure of the two-level DC-DC converter as presented in Figure 3.1. The new version of this converter is shown in Figure 3.16. One of the disadvantages of the proposed topology as shown in Figure 3.1 is that, the flow of the current in lower-level semiconductors is higher than the upper one. Therefore, low-level semiconductors consume more power than high-level semiconductors. Such drawbacks are more common in most MBC and can be minimized by putting the voltage source in the middle of the circuit rather than in the base.

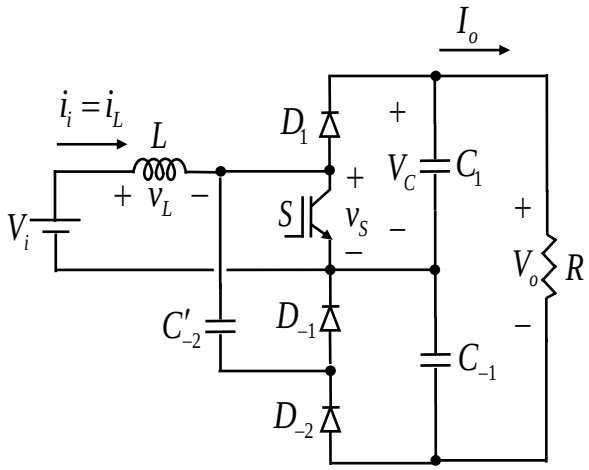
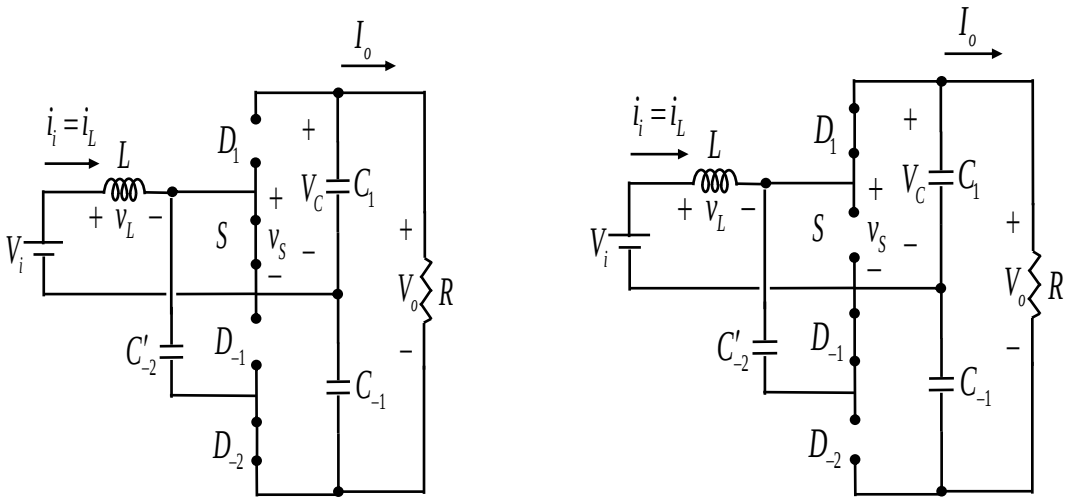



**Figure 3.16:** Two-level DC-DC boost converter circuit diagram with CVS

The equivalent circuit diagram of the DC-DC dual-level step-up converter with a central voltage source, when the switch $S$ is on is shown in Figure 3.17(a). During the switching on mode the switch $S$, the inductor $L$ and the voltage source $V_i$ are connected in one loop. In this, time interval the diode $D_1$ is turned off, due to the existence of the voltage of capacitor $C_1$ and the diode $D_{-1}$ will also be in closed position due to the voltage of capacitor $C'_{-2}$. But, the diode $D_{-2}$ will be in on state. Since, the voltage of the capacitor $C_{-1}$ is smaller than the voltage of the capacitor $C'_{-2}$. The equivalent power circuit of the two-level DC-DC

boost converter with the central voltage source at the time when the switch $S$ is off is shown in Figure 3.17(b). In this period, the current flowing through the inductor $L$ forward biased the diodes $D_1$ and $D_{-1}$. In the same time, as the sum of the voltages of the two capacitor $C_1$ and C-1 is more than the voltage of the capacitor $C'_{-2}$, causes the diode $D_{-2}$ to turn off.




(a) On mode (b) Off mode

**Figure 3.17:** Two-level DC-DC boost converter with CVS circuit diagram for on/off modes

The waveforms of the voltages and currents of the two-level DC-DC boost converter with the central voltage source are the same as shown in Figure 3.6 during the on/off state. The voltage across the switch is $v_S = V_C$ $DT$ in time interval and zero at $(1-D)T$ interval.

### 3.5.1 Two-level DC-DC BC analysis with central voltage source in CCM and DCM

According to the power circuit of Figure 3.16, for two-level DC-DC boost converter with a central voltage source, assuming that the capacitors $C_1$ and $C_{-1}$ have the same capacitance as well as voltages, then their voltages assumed to be equal $V_{C-1} = V_{C1} = V_C$ and $V_o = 2V_C$. Thus, as explained in section 3.1.1the voltage gain and the inductor average current of the two-level DC-DC boost converter with a central voltage source in the CCM will be given by the following respective equations.

$$\frac{V_o}{V_i} = \frac{2}{1-D} \qquad (3.114)$$

$$I_L = \frac{2^2 V_C}{R(1-D)} \tag{3.115}$$

The boost ratio and the average inductor currents expression analysis in DCM are similar to the equations evaluated in section 3.1.2 as shown below respectively.

$$\frac{V_o}{V_i} = 2\frac{\Delta_1 + D}{\Delta_1} \tag{3.116}$$

$$I_L = \frac{2^2 V_C(\Delta_1 + D)}{R\Delta_1} \tag{3.117}$$

### 3.5.2 The Effect of ESR on the boost ratio of two-level DC-DC boost converter with CVS in CCM and DCM

Based on the circuit diagram of the Figure 3.16, the derivation principle of the voltage gain of the two-level DC-DC BC with a central voltage source in CCM and DCM considering the effect of the ESR of the inductor $L$ is the same as analyzed in sections 3.1.3 and 3.1.4. Thus, the equations for CCM and DCM can be expressed as follows respectively.

$$\frac{V_o}{V_i} = \frac{1}{\frac{1-D}{2} + \frac{2R_{ESR,L}}{(1-D)R}} \tag{3.118}$$

$$\frac{V_o}{V_i} = \frac{(\Delta_1 + D)}{\frac{\Delta_1}{2} + \frac{2(\Delta_1 + D)^2}{R\Delta_1} R_{ESR,L}} \tag{3.119}$$

### 3.5.3 Analysis of diodes and switch voltage drop effects in DC-DC dual- level boost converter with CVS

Considering the circuit diagram of Figure 3.17a and Figure 3.17b, including the ($C'_{-2}$, $S$, $C_{-1}$ and $D_{-2}$) and ($C'_{-2}$, $D_1$, $C_1$ and $D_{-1}$) respectively, then their respective voltage equations across the circuit for $V_S = V_{D-2} = V_d$ are expressed as follows:

$$-V_{C'-2} + V_S + V_{C-1} + V_{D-2} = 0$$

$$V_{C'-2} = V_{C-1} + 2V_d \tag{3.120}$$

$$-V_{C'-2} + V_d + V_{C1} - V_d = 0 \tag{3-121}$$

Substituting equation 3.120 into the above expression, the following equation is obtained for the voltage across the capacitor $C_1$:

$$V_{C1} = V_{C-1} + 2V_d \tag{3.122}$$

The output voltage of the two-level DC-DC boost converter with a central voltage source as shown in Figure 3.16, considering the above relation is given by the following equation:

$$V_o = V_{C1} + V_{C-1} = V_{C-1} + V_{C-1} + 2V_d = 2V_{C-1} + 2V_d \tag{3.123}$$

Thus based on the above derived voltage expressions, the efficiency of the switched capacitors with respect to the load output voltage for the DC-DC two-stage BC with a central voltage source is given as:

$$\frac{V_o}{2V_{C-1}} = \frac{2V_{C-1} + 2V_d}{2V_{C-1}} = 1 + \frac{V_d}{V_{C-1}} \tag{3.124}$$

### 3.6 Three-Level DC-DC MBC with Central Voltage Source

The three-level DC-DC step-up converter power circuit diagram with a central voltage source is shown in Figure 3.18 in next page. The equivalent circuit diagram of the triple-stage boost converter with the central voltage source in the interval when the switch $S$ is on is shown in Figure 3.19(a). During the switching on state of the switch, the inductor $L$ is connected in series with the voltage source $V_i$. Due to the fact that the switch is closed and the presence of the voltage across the capacitor $C_1$ causes the diode $D_1$ to turn off. Considering, the voltage across the capacitor $C_2'$ is smaller than the voltage of the capacitor $C_1$, so that diode $D_2$ will turn on and diode $D_2'$ will be turned off due to the voltage of the capacitor $C_2$. Also, comparing the capacitor voltages in the lower case, the voltage of the capacitor $C_{-1}$ is smaller than the capacitor $C_{-2}'$ voltage, in which the diode $D_{-2}$ will be switched on, but the existence of the capacitor voltage $C_{-2}'$ causes the diode $D_{-1}$ reveres biased.

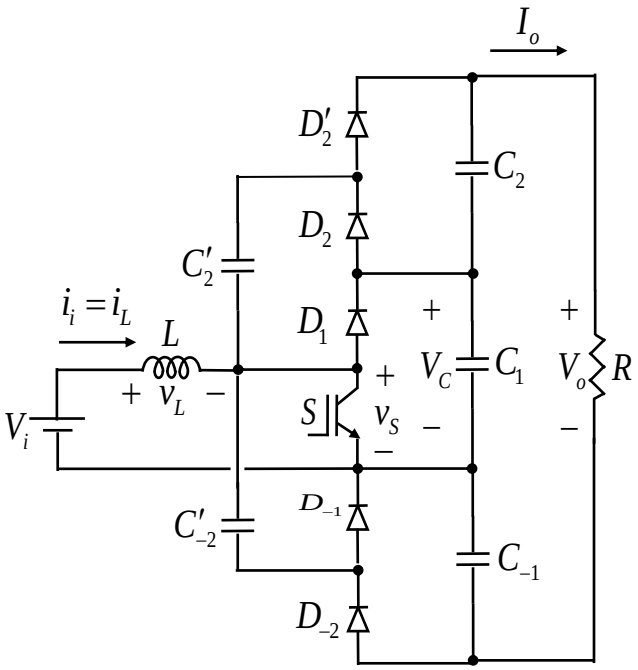
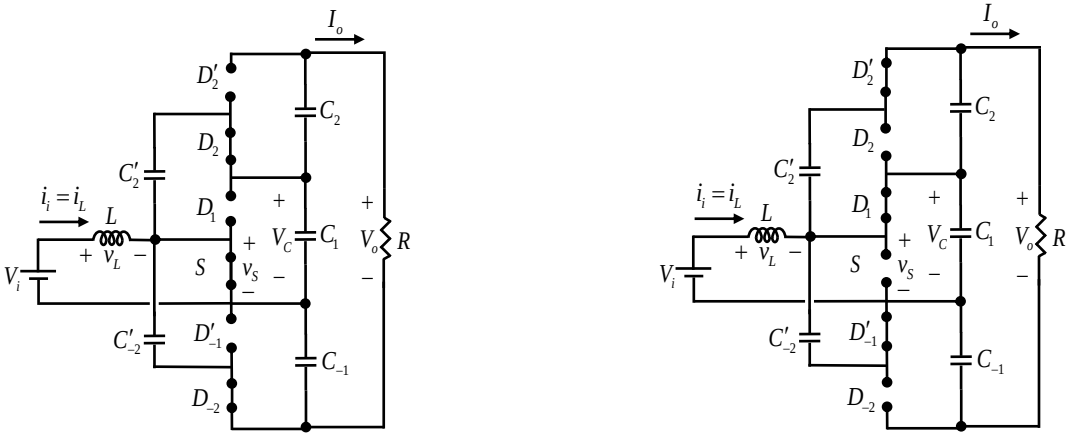



**Figure 3.18:** Three-level DC-DC MBC circuit diagram with central voltage source

The analogue power circuit of the three-level DC-DC BC with the central voltage source in the next half cycle, when the switch $S$ is off is shown in Figure 3.19(b). In this period of time, the current of the inductor $L$ turns on the diodes $D_1$ and $D'_2$. In this case, the presence of capacitor voltage $C'_2$ causes the diode $D_2$ to turn off. As a result, when the diode $D_1$ is on, the sum of the capacitor voltages $C_1$ and $C_{-1}$ is greater than the voltage of the capacitor $C'_{-2}$, then the diode $D_{-2}$ is automatically turned off and the diode $D_{-1}$ is forward biased, due to the current of the inductor $L$.




(a) On mode (b) Off mode

**Figure 3.19:** Three-level DC-DC BC with a central voltage source for on/off modes

The wave forms of the voltages and currents of the triple-stage DC-DC BC with central voltage source for all components are identical as shown in Figure 3.6 over the complete cycle in which the equation of the current also the same in CCM and DCM.

### 3.6.1 Three-level multiplier DC-DC converter analysis with CVS in CCM and DCM

Based on the value of the design parameters and the schematic designing circuit diagram of Figure 3.18, for a three-level DC-DC BC with a central voltage source the capacitance values of the capacitors $C_{-1}$ to $C_2$ and their voltages are assumed to be the same at all provided that $V_{C-1} = V_{C1} = V_{C2} = V_C$ and $V_o = 3V_C$. Then, the boost ratio and the average inductor current in CCM as well as in DCM are the same to the expressions deduced in sections 3.2.1 and 3.2.2 as given below consecutively.

$$\frac{V_o}{V_i} = \frac{3}{1-D} \tag{3.125}$$

$$I_L = \frac{3^2 V_C}{R(1-D)} \tag{3.126}$$

$$\frac{V_o}{V_i} = 3\frac{\Delta_1 + D}{\Delta_1} \tag{3.127}$$

$$I_L = \frac{3^2 V_C(\Delta_1 + D)}{R\Delta_1} \tag{3.128}$$

And, the boost ratio of the three-level incremental DC-DC converter with a central voltage source, considering the effect of the inductor's ESR both in CCM and DCM will be expressed as:

$$\frac{V_o}{V_i} = \frac{1}{\frac{1-D}{3} + \frac{3R_{ESR,L}}{(1-D)R}} \tag{3.129}$$

$$\frac{V_o}{V_i} = \frac{(\Delta_1 + D)}{\frac{\Delta_1}{3} + \frac{3(\Delta_1 + D)^2}{R\Delta_1} R_{ESR,L}} \tag{3.130}$$

From the above relation it can be seen that the ESR of the inductor $L$ limits the voltage gain of the converter.

### 3.6.2 Investigation of diodes and switch voltage drop effects on three-level DC- DC boots converter with central voltage source

To calculate the effects of the diodes and switch voltage drops on the converter considering the circuit diagram of Figure 3.19a, in the circuit including ($C'_{-2}$, $S$, $C_{-1}$ and $D_{-2}$), ($C'_2$, $S$, $C_1$, and $D_2$) as well as in figure 3.19b in the circuit containing ($C'_{-2}$, $D_1$, $C_1$ and $D_{-1}$) and ($C'_2$, $D'_2$, $C_2$ and $D_1$). Assuming that $V_S = V_{D-2} = V_d$, then the voltage expression in the above circuits can be given by the following equations.

$$-V_{C'-2} + V_S + V_{C-1} + V_{D-2} = 0$$

$$V_{C'-2} = V_{C-1} + 2V_d \tag{3.131}$$

$$V_{C'2} + V_d - V_{C1} + V_d = 0 \tag{3.132}$$

$$-V_{C'-2} + V_d + V_{C1} - V_d = 0 \tag{3.133}$$

$$-V_{C'2} + V_d + V_{C2} - V_d = 0 \tag{3.134}$$

The voltage of the capacitor $C_1$ can be calculated by replacing the relation 3.131 into 3.133 and is given by:

$$V_{C1} = V_{C-1} + 2V_d \tag{3.135}$$

Substituting the above relation into equation 3.132 the voltage of the capacitors $C'_2$ is the same as:

$$V_{C'2} = V_{C-1} \tag{3.136}$$

Equation 3.134 is combined with the above expression to find the voltage across the capacitors $C'_2$ as given below:

$$V_{C2} = V_{C-1} \tag{3.137}$$

Then, the output voltage of the three-level DC-DC boost converter with central voltage source represented by circuit diagram as shown in Figure 3.18, based on the above analyzed voltage expression is given by the following equation:

$$V_o = V_{C_2} + V_{C1} + V_{C-1} = V_{C-1} + V_{C-1} + V_{C-1} + 2V_d = 3V_{C-1} + 2V_d \tag{3.138}$$

Thus, based the above relation, the efficiency of the capacitor switched three-level DC-DC boost converter with the source of the central voltage will expressed as:

$$\frac{V_o}{3V_{C-1}} = \frac{3V_{C-1} + 2V_d}{3V_{C-1}} = 1 + \frac{2V_d}{3V_{C-1}} \tag{3.139}$$

### 3.7 DC-DC *n* -Level MBC with Central Voltage Source

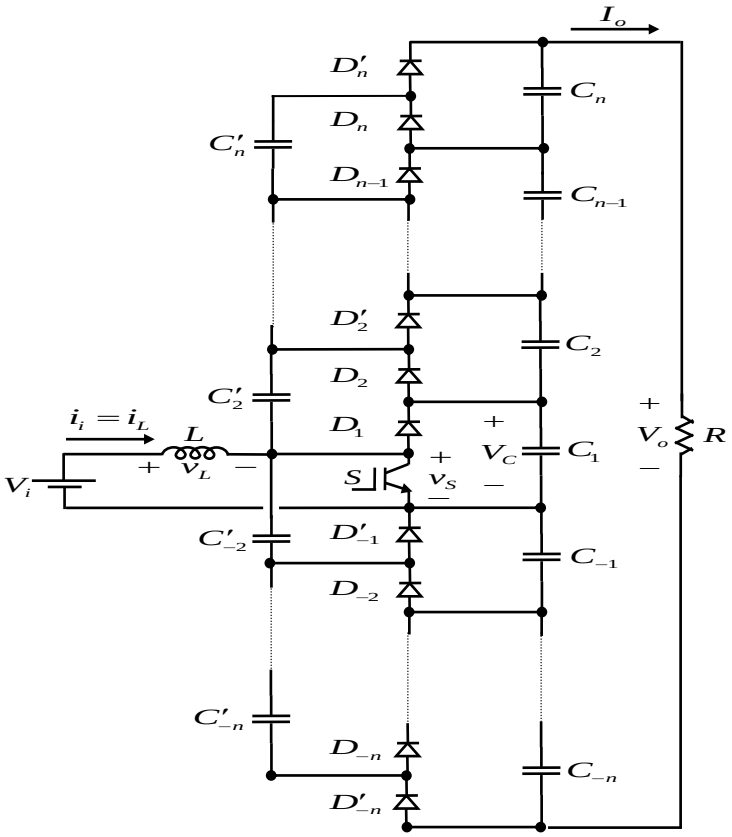



**Figure 3.20:** Power Circuit diagram for *n* -level DC-DC MBC with CVS

The *n* -level DC-DC MBC circuit power with the central voltage source is shown in Figure 3.20 and the wave forms of the voltages and currents of the three-level DC-DC converter components with the central voltage source are shown in Figure 3.21. In this wave form,

1and 0 are the high and low states of the switch $S$. In the time interval $(1-D)T$ (when the switch $S$ is off and the diodes ($D_{-1}, D'_{-2}, D'_{-3}$ to $D'_{-n}$ and $D_1, D'_2, D'_3$ to $D'_n$) are on), then the voltage $V_S$ across the switch in the loop including the switch $S$, the diode $D_1$ and capacitor $C_1$ with a voltage $V_C$ will be $v_S = V_C$. In the time interval $DT$ (when the switch $S$ and the diodes $D_2$, $D_3, D_{-2}$, $D_{-3}$ to $D_n$ and $D_{-n}$ are on), the voltage across the switch $S$ is zero. In the following relevant section, the $n$-levels DC-DC MBC is analyzed with a central voltage source in continuous and discontinuous conduction regions.

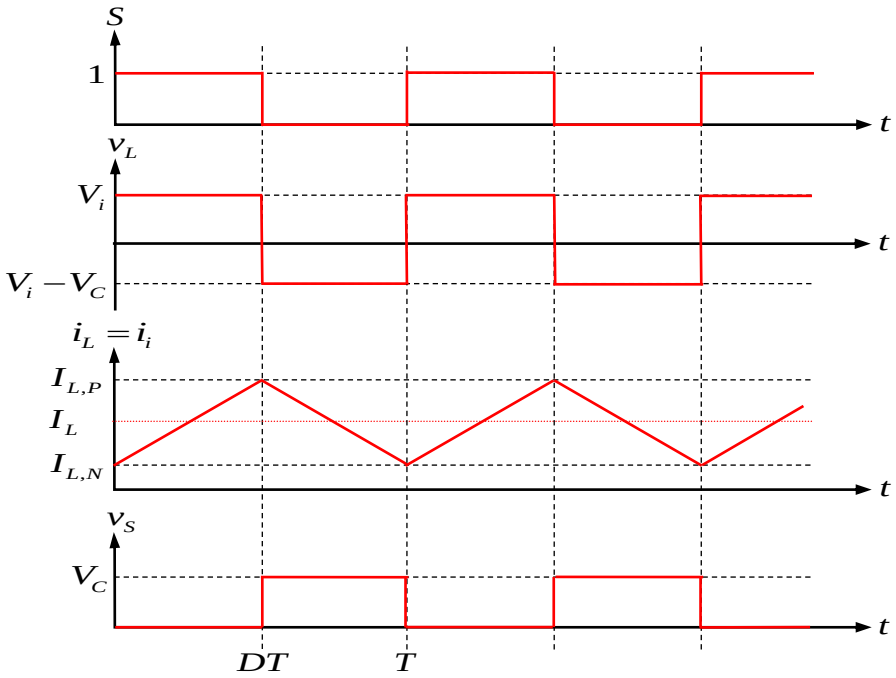



**Figure 3.21:** Voltage and current waveforms of $n$-level DC-DC MBC with CVS

### 3.7.1 Analysis of $n$-level DC-DC MBC with central voltage source in CCM and DCM

According to Figure 3.20, for $n$-level DC-DC MBC with a central voltage source, assuming that the capacitors $C_{-n}$ to $C_n$ have the same capacitance and their corresponding voltage also are equal, then the output voltage of this topology $n$ times the capacitor voltage.

$$V_{Cj} = V_C \qquad for \quad j = -n, \ldots, -2, -1, 1, 2, \ldots, n$$

$$V_o = nV_C \tag{3.140}$$

As the procedures followed in section 3.4 to evaluate the expression for boost ration and inductor current, then the equation of voltage gain and the average inductor current for

the $n$-level MBC with the central voltage source in the CCM and DCM are the same as follows respectively.

$$\frac{V_o}{V_i} = \frac{n}{1-D} \tag{3.141}$$

$$I_L = \frac{n^2 V_C}{R(1-D)} \tag{3.142}$$

$$\frac{V_o}{V_i} = n\frac{\Delta_1 + D}{\Delta_1} \tag{3.143}$$

$$I_L = \frac{n^2 V_C (\Delta_1 + D)}{R\Delta_1} \tag{3.144}$$

Considering the effect of the inductor's ESR in reference to Figure 3.20, during the total period of time, the conversion ratio of the $n$-level MBC with the central voltage source in CCM and DCM is given by the following respective formulas as discussed and analyzed in section 3.4.

$$\frac{V_o}{V_i} = \frac{1}{\frac{1-D}{n} + \frac{nR_{ESR,L}}{(1-D)R}} \tag{3.145}$$

$$\frac{V_o}{V_i} = \frac{(\Delta_1 + D)}{\frac{\Delta_1}{n} + \frac{n(\Delta_1 + D)^2}{R\Delta_1} R_{ESR,L}} \tag{3.146}$$

### 3.7.2 Diodes and switch voltage drop effects on $n$-level DC-DC MBC with CVS

As explained and investigated in the previous voltage output equations 3.124 and 3.139, for the two lower level, the expression of output voltage in relation to the capacitor voltage for any $n$-level MBC with central voltage source considering the influence of the diodes and switch voltage drops can be expressed as:

$$\frac{V_o}{nV_{C-1}} = \frac{nV_{C-1} + 2V_d}{nV_{C-1}} = 1 + \frac{2V_d}{nV_{C-1}} \tag{3.147}$$

# CHAPTER 4
# PROCESS CONTROL STRATEGY AND SIMULATION ANALYSIS

## 4.1 Process Control Block Diagram

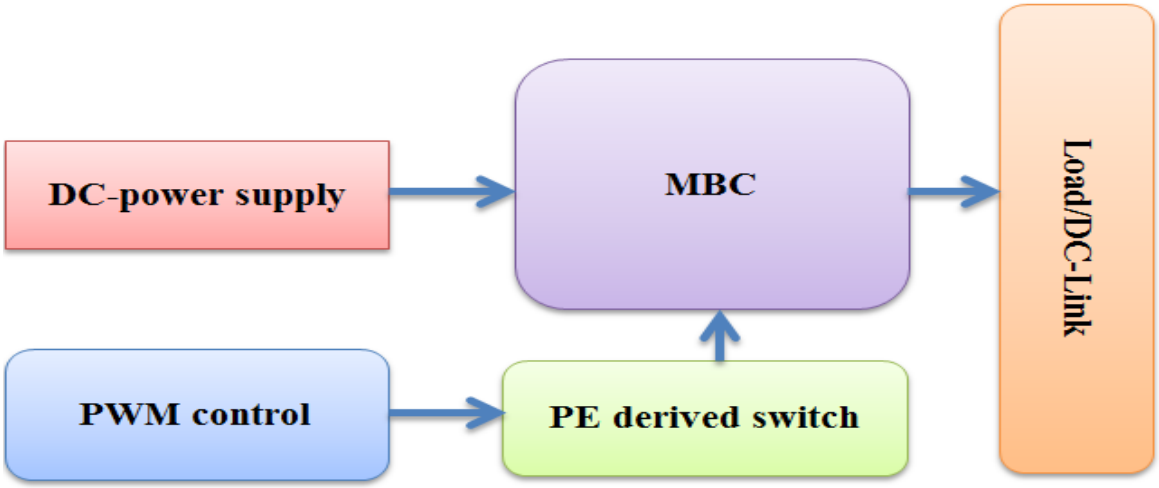



**Figure 4.1:** Proposed converter process control block diagram

As shown in the above schematic diagram of the proposed topology, the system is mainly composed of five blocks. The input power source at low value is continuously supplied to the main circuit and the on/off modes of the power electronic derived switch is controlled by receiving a proper signal from the PWM controller depending on the value of the switching frequency. The function of the main circuit (MBC) is to boost the low value of the input voltage at much higher output voltage according the selected level and the output is delivered to the load or to the DC-link system.

## 4.2 Simulation Results

In this chapter, the DC-DC $n$-level MBC is simulated in order to verify the accuracy of the estimated and analyzed equations in chapter two and three. In addition, to evaluate the validity of the obtained expressions for all stages of the DC-DC MBC, the topologies are implemented in the PSCAD / EMTDC software environment and the simulation results are presented, compared and labeled in the form of graphs. The specific parameters are given in the form of tables for each level of the converter that are used for direct calculations and

simulation purposed. The graphs and simulation solutions demonstrate that, the theoretical and experimental results are almost the same.

### 4.2.1. Validation of the analyzed equations for first stage DC-DC boost converter

**Table 4.1:** Parameters of the single-stage DC-DC boost converter

| **Parameters** | **Values** |
|---|---|
| Voltage Source($V_i$) | 50$V$ |
| Inductance($L$) | 1.33mH |
| Duty cycle($D$) | 0.5 |
| Capacitance($C$) | 100µF |
| Load Resistance($R$) | 100Ω |
| Switching frequency($f$) | 100 kHz |

The specific parameters required for the single level boost converter are shown in Table 4.1. From the derived boost ratio equation 2.3, the average value of the output voltage of the converter will be equal to $V_o = 100V$. Also, the average value of the output current is the same as $I_o = 1A$ by equation 2.4. The simulation results presented in Figure 4.2, justify the accuracy of the obtained equations to calculate the output voltage and current of the conventional DC-DC incremental converter.

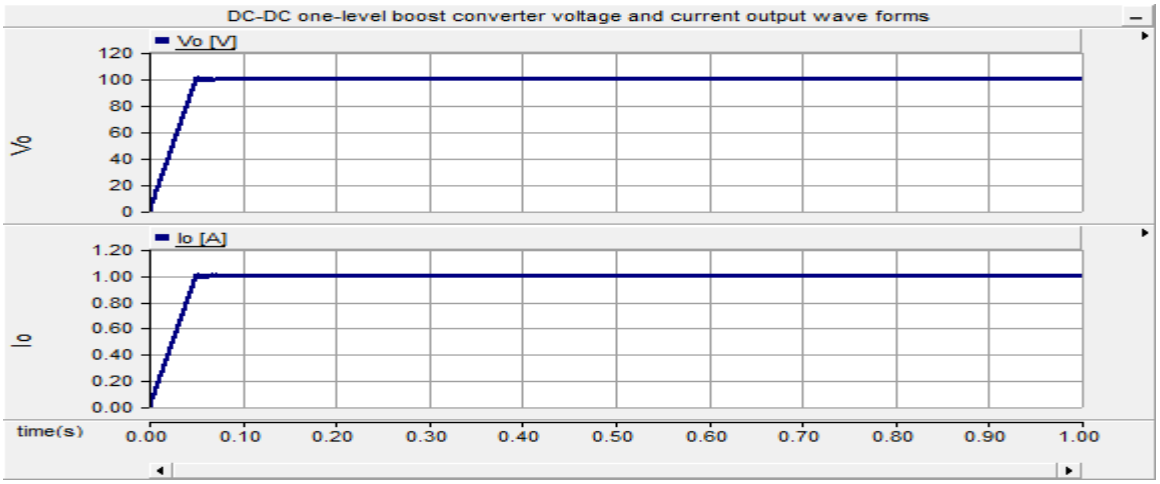



**Figure 4.2:** Voltage and current output waveforms for DC-DC conventional BC

Based on the power circuit of Figure 2.2a and the values of Table 4.1, the voltage of the inductor in in the first half cycle with time interval $DT = 5\mu S$ is equal to $V_L = 50V$ and in the next period at $(1-D)T = 5\mu S$ time interval is equal to $V_L = -50V$. According to the equation 2.4 the mean value of the inductor $L$, which is the same as the average input current will be evaluated as $I_L = 2.1A$. The wave forms of the voltage and current of the inductor are shown in Figure 4.2, which confirms the accuracy of the above calculations.

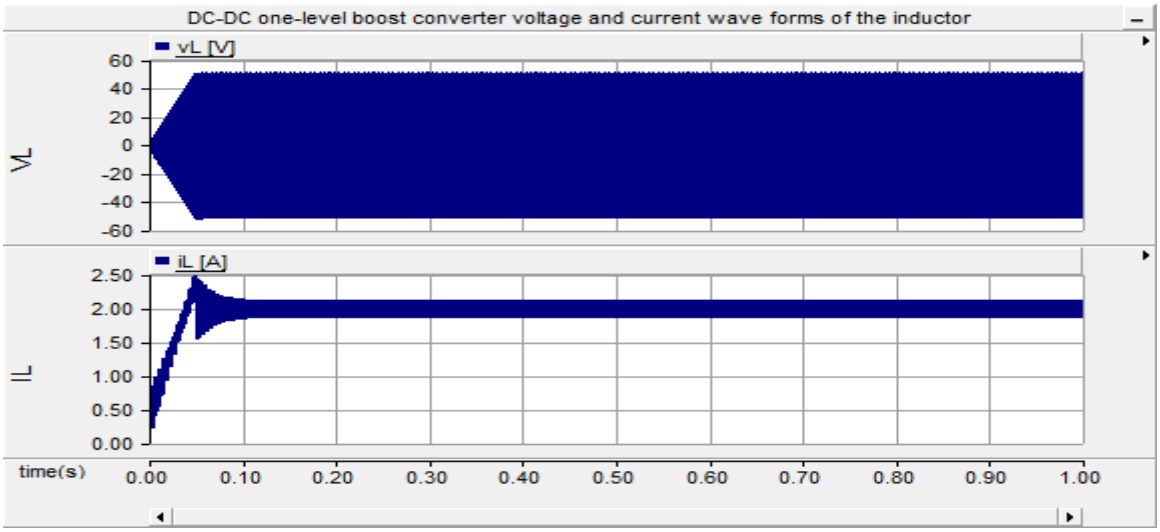



**Figure 4.3:** Inductor voltage and current waveforms for one-level boost converter

The voltage drop across the switch from the given relation 2.8 and the parameter values of Table 4.1, in the time interval $(1-D)T = 5\mu S$, will be equal to $V_s = 100V$. Also, the voltage of the switch in the first half cycle will be zero at the time interval of $DT = 5\mu S$. The voltage waveform across the switch for the two modes shown in Figure 4.4 verifies the above calculations.

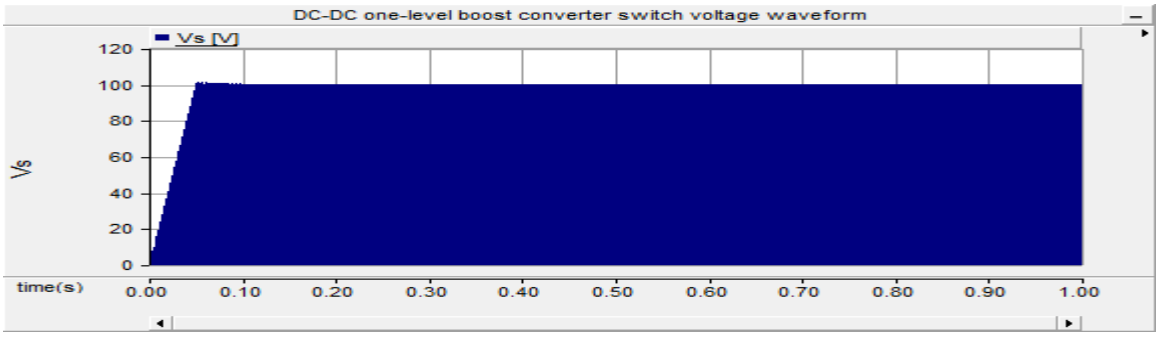



**Figure 4.4:** Switch voltage waveform for one-level DC-DC boost converter

### 4.2.2. Evaluation of the expressions accuracy for two-level DC-DC boost converter

**Table 4.2:** Designing Parameters for two-level DC-DC boost converter

| **Parameters** | **Values** |
|---|---|
| Voltage Source($V_i$) | 50$V$ |
| Inductance($L$) | 1.33mH |
| Duty cycle($D$) | 0.5 |
| Capacitance($C_1, C_2, C_2'$) | 100µF |
| Load Resistance($R$) | 100Ω |
| Switching frequency($f$) | 100 kHz |

The components in the above table are for two-level MBC simulation aspects. The average value of the output voltage ($V_o = 200V$) and output current ($I_o = 2A$) of the converter are calculated according to the equations 3.4 and 3.5. The simulation results presented in Figure 4.5, confirm the accuracy of the obtained relations to calculate the output voltage and output current of this special level of converter.

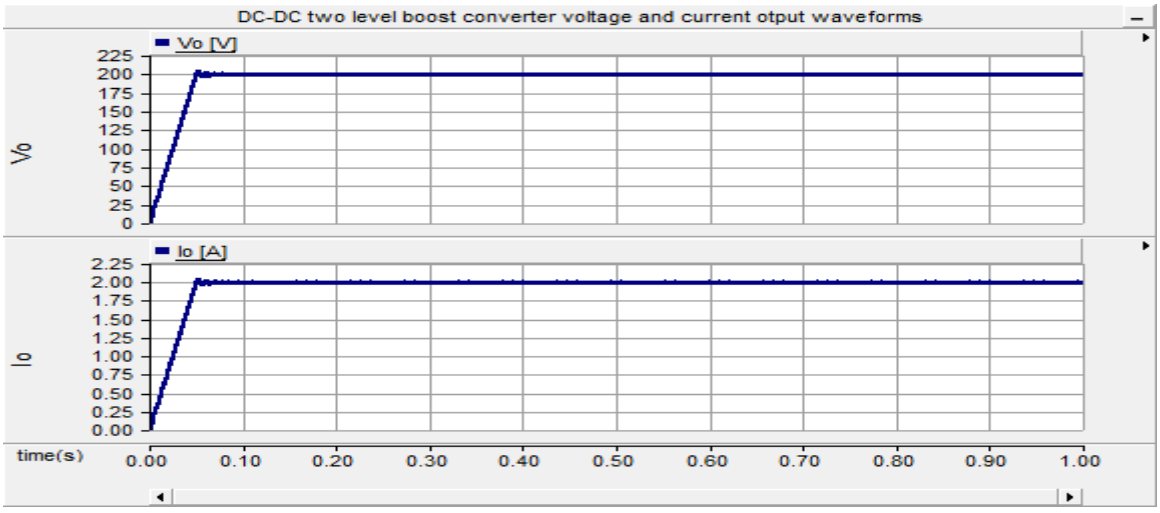



**Figure 4.5:** Voltage and current output waveform for two-level DC-DC MBC

Since the output voltage of the simulated converter is equal to $V_o = 200V$, using the given equation 3.3 the average voltages of the two capacitors $C_1$ and $C_2$ are calculated equal to $V_{C1} = V_{C2} = 100V$. Thus, the wave forms of the two capacitors voltages illustrated in Figure

4.6, verifies that their voltages are the same and matches with the result obtained using the direct formulas.

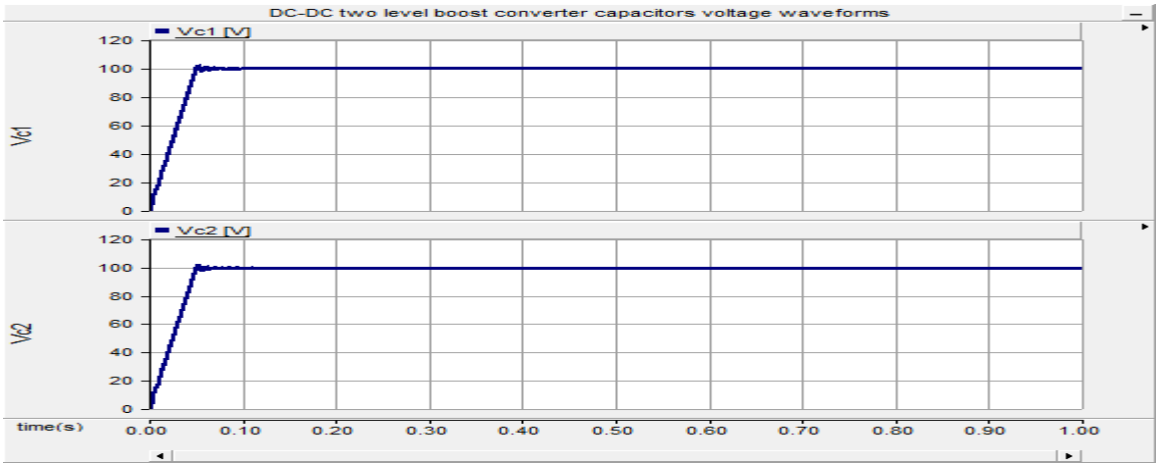



**Figure 4.6:** Capacitors ($C_1$ and $C_2$) voltage waveforms for two-level DC-DC MBC

The average inductor voltages are always constant for all levels as explained in chapter three its value over the time period $DT = 5\mu S$ and $(1-D)T = 5\mu S$ based on the specifications stated in Table 1.2, to give a voltages of $V_L = 50V$ and $V_L = -50V$ respectively. The average value of the inductor's input current also will be $I_L = 8A$ using the equation 3.7. Therefore, the waveforms of the voltage and current of the inductor shown in Figure 4.7, confirms the validity of the above calculations.

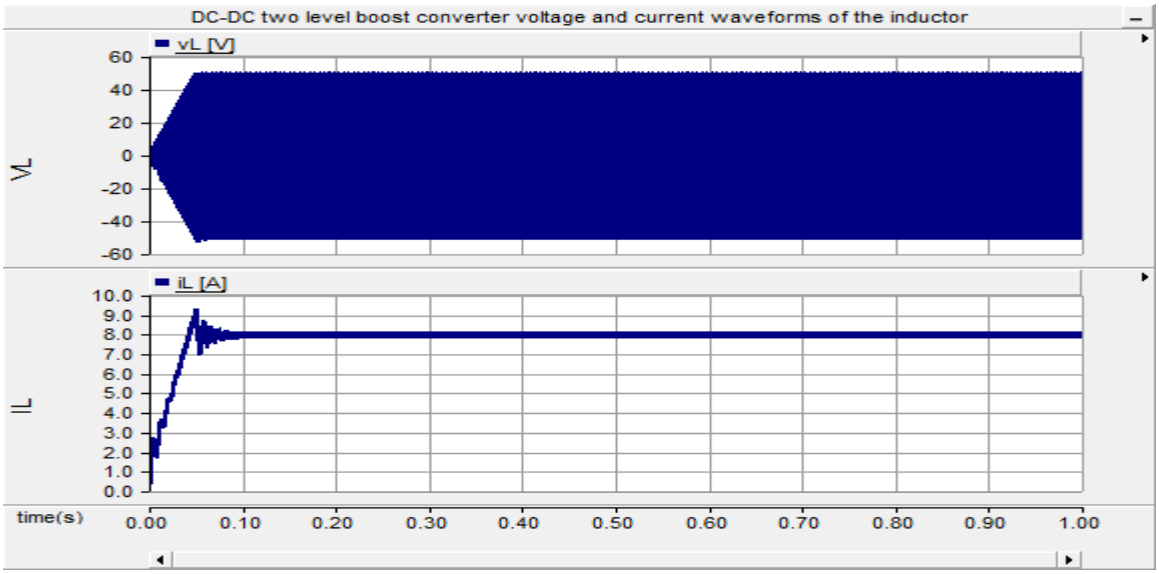



**Figure 4.7:** Inductor voltage and current waveforms for two-level DC-DC MBC

As specified in Table 4.2 the voltage across the switch using the given equation 3.38 in the time interval $(1-D)T = 5\mu S$ will be equal to $V_s = 100V$. Also, the voltage of the switch in the first half cycle $DT = 5\mu S$ is zero. The voltage wave form of the switch is shown in Figure 4.7, which confirms that the simulation results are the same as the direct calculations.

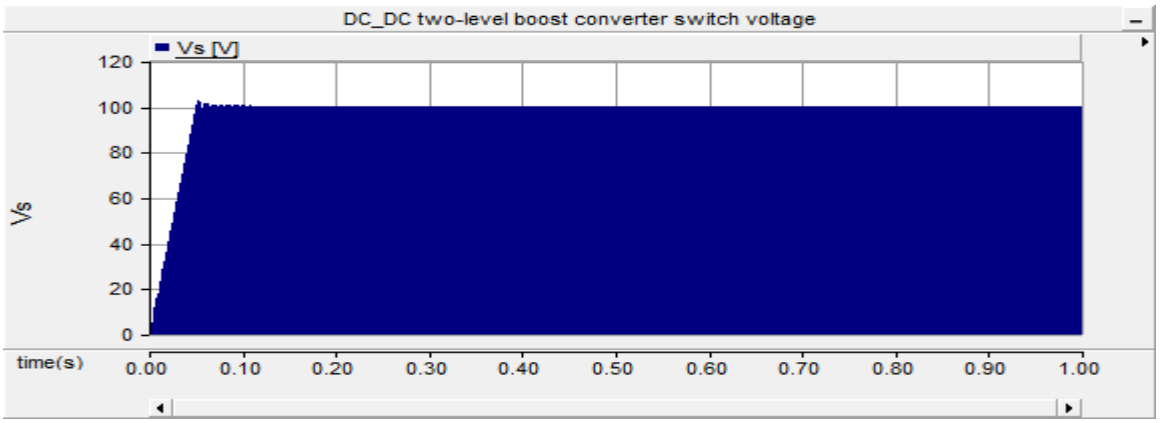



**Figure 4.8:** Switch voltage waveform for dual-level DC-DC step-up converter

### 4.2.3 Verification of the results obtained for three-level DC-DC boost converter

**Table 4.3:** Parameters of the three-level DC-DC boost converter

| **Parameters** | **Values** |
|---|---|
| Voltage Source($V_i$) | $50V$ |
| Inductance($L$) | 1.33mH |
| Duty cycle($D$) | 0.5 |
| Capacitance($C_1, C_2, C_3, C_2'$ and $C_3'$) | 100µF |
| Load Resistance($R$) | 100Ω |
| Switching frequency($f$) | 100 kHz |

Equations 3.43 and 3.5 are used to evaluate the average values of the output voltage $V_o = 300V$ and the output current $I_o = 3A$ of the converter. The simulation solutions drawn in Figure 4.8 verify the accuracy of the obtained formulas to calculate the output voltage and current of the converter.

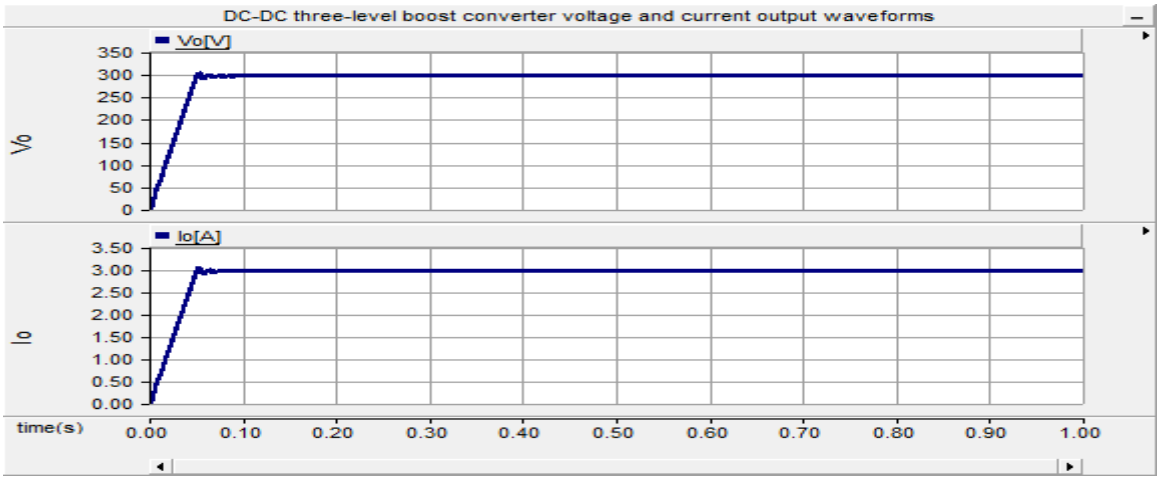



**Figure 4.9:** Voltage and current output waveforms for three-level DC-DC MBC

The average voltages across the capacitor $C_1$, $C_2$ and $C_3$ equal to $V_{C1} = V_{C2} = V_{C3} = 100V$, are calculated based on the equation 3.42 and the output voltage of the simulated converter is equal to $V_o = 300V$. Further, the capacitor voltage wave forms and simulation results of the converter shown in Figure 4.9, supports that their voltages are the same and prove the validity of the expressions.

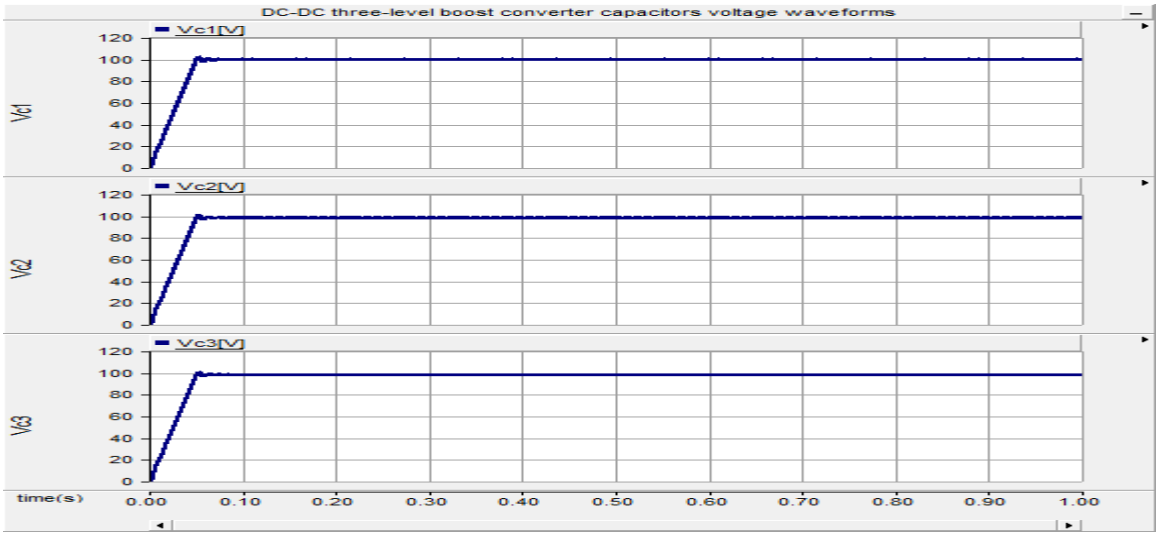



**Figure 4.10:** Capacitor ( $C_1$ to $C_3$ ) voltage waveforms for three-level DC-DC MBC

According to the description of section 3.2.1and the parameter values of Table 4.3, the voltage of the inductor $L$ in the time intervals of $DT = 5\mu S$ and $(1-D)T = 5\mu S$ are calculate to be $V_L = 50V$ and $V_L = -50V$ respectively. The average value of the inductor current with respect to the equation 3.44 will be $I_L = 18A$. The validity of the above calculations is confirmed by the wave forms of the voltage and current of the inductor shown in Figure 4.10.

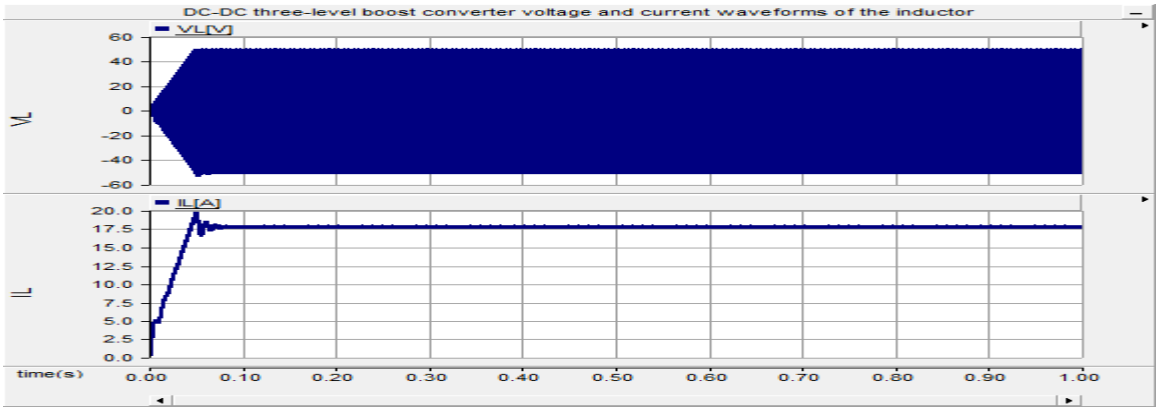



**Figure 4.11:** Inductor voltage and current wave forms for DC-DC three-level MBC

In addition, the voltage stress on the switch in the time period $(1-D)T = 5\mu S$ is estimated equal to $V_s = 100V$ according to the equation 3.71 and is equal to zero in the time interval $DT = 5\mu S$. The switch voltage wave form provided in Figure 4.11 verifies the accuracy of the evaluated results.

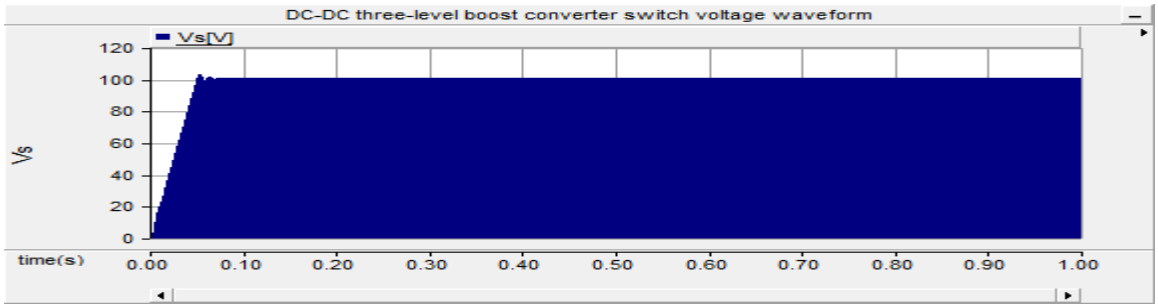



**Figure 4.12:** Switch voltage waveform of DC-DC three-level boost converter

### 4.2.4 Estimation of the expressions accuracy for four-level DC-DC boost converter

**Table 4.4:** Parameters of the four-level incremental DC-DC converter

| **Parameters** | **Values** |
|---|---|
| Voltage Source($V_i$) | $50V$ |
| Inductance($L$) | 1.33mH |
| Duty cycle($D$) | 0.5 |
| Capacitance($C_1, C_2, C_3, C_4, C_2'$ , $C_3'$ and $C_4'$) | 100µF |
| Load Resistance($R$) | 300Ω |
| Switching frequency($f$) | 100 kHz |

The average value of the output voltage $V_o = 400V$ and current $I_o = 1.33A$ of the converter are evaluated with respect to the relations 3.75 and 3.5 respectively. These results are agreed with the simulation results presented in Figure 4.12 to prove the accuracy of the voltage and current output expressions of the converter.

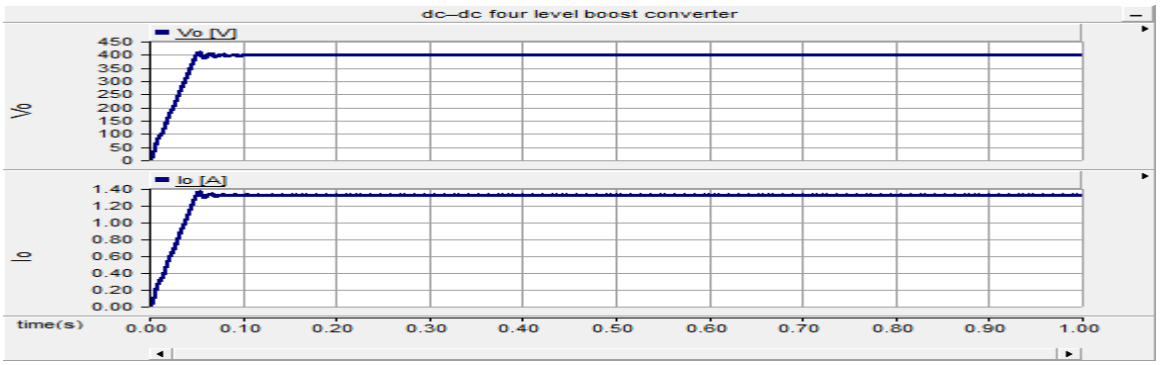



**Figure 4.13:** Voltage and current output waveforms for four-level DC-DC MBC

The average voltages across the capacitors $C_1, C_2, C_3$ and $C_4$ are evaluated according to the relation 3.74 equal to $V_{C1} = V_{C2} = V_{C3} = V_{C4} = 100V$, with an output voltage of the simulated converter is equal to $V_o = 100V$. Therefore, the wave forms of the capacitor voltages shown in Figure 4.13 and the assumption made to the capacitors $C_1, C_2, C_3$ and $C_4$ to be equal, confirm the validity of the above expressions.

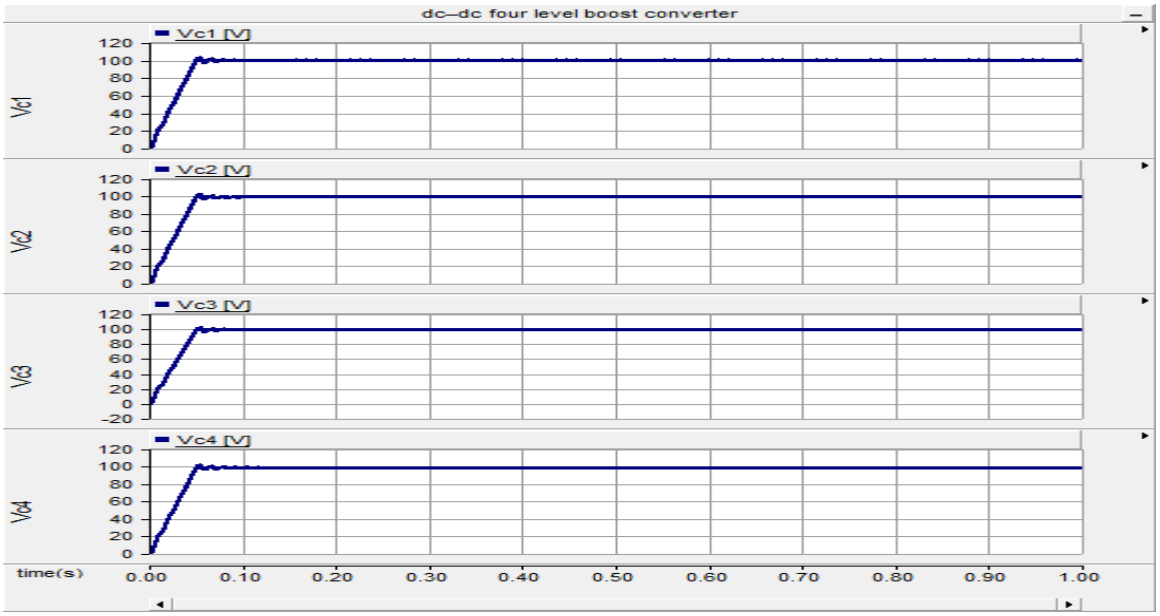



**Figure 4.14:** Capacitors ($C_1$ to $C_4$) voltage waveforms for DC-DC four-level MBC

The voltage and current waveforms of the inductor $L$ presented in Figure 4.14 verifies the accuracy of the analyzed calculations based on the values of Table 4.4. Thus, according to the working principle of MBC, the value of the average voltages of the inductor are estimated to $V_L = 50V$ and $V_L = -50V$ in the time intervals of $DT = 5\mu S$ and $(1-D)T = 5\mu S$ respectively. And, from the expression 3.76 the average inductor current which is equal to the average input current will be evaluated as $I_L = 10.7A$.

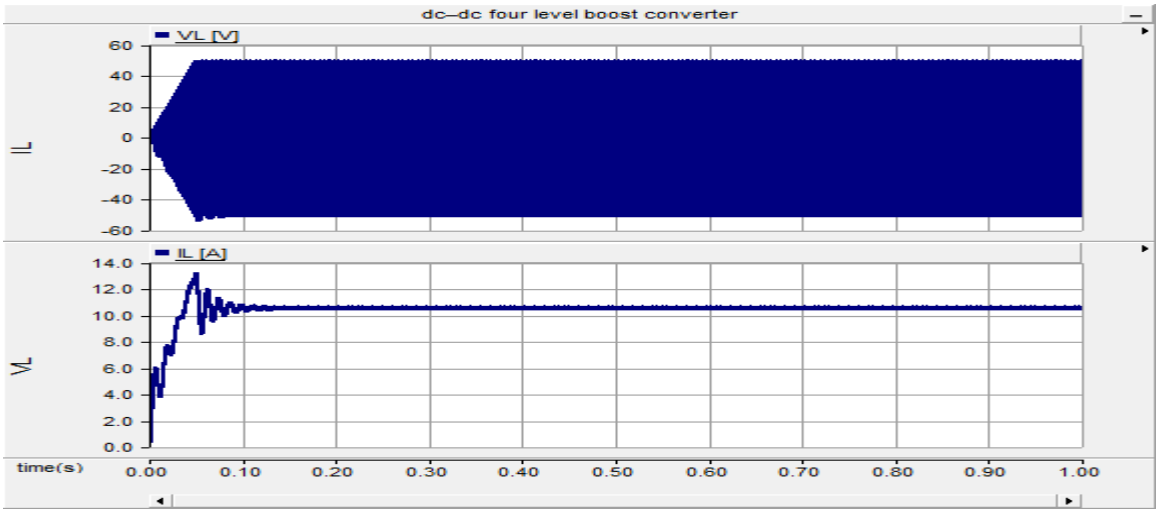



**Figure 4.15:** Inductor voltage and current waveforms for DC-DC four-level MBC

Furthermore, with respect to the relation 3.95 and the specifications of Table 4.4, the voltage stress across the switch in the time period $(1-D)T = 5\mu S$ will be equal to $V_s = 100V$. Also, in the first half cycle of $DT = 5\mu S$ the voltage stress of the switch will be zero. The simulation voltage wave form of the switch shown in Figure 4 15 verifies the accuracy of the above calculations.

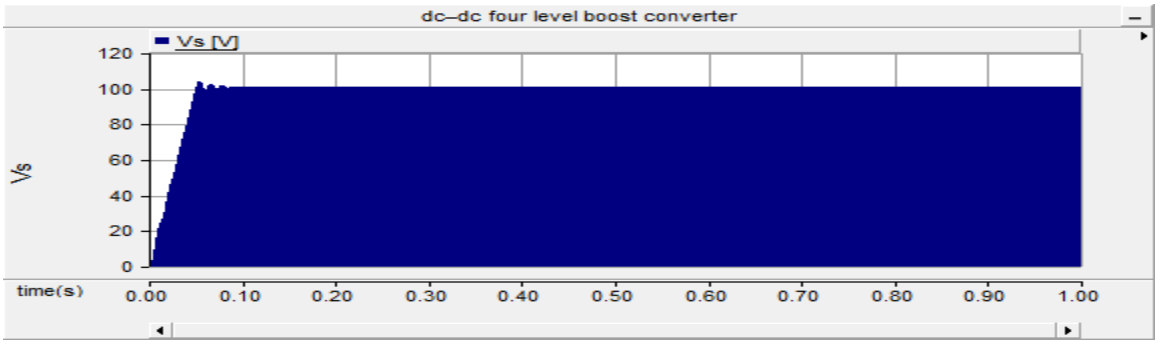



**Figure 4.16:** Switch voltage waveform for four-level DC-DC boost converter

### 4.2.5 Validation of the equations for DC-DC dual-level boost converter with CVS

**Table 4.5:** Specifications for DC-DC dual-level boost converter with CVS

| **Parameters** | **Values** |
|---|---|
| Voltage Source($V_i$) | $50V$ |
| Inductance($L$) | 1.33mH |
| Duty cycle($D$) | 0.5 |
| Capacitance($C_1$, $C_{-1}$ and $C'_{-2}$) | 100µF |
| Load Resistance($R$) | 100Ω |
| Switching frequency($f$) | 100 kHz |

The average values of the output voltage $V_o = 200V$ and the output current $I_o = 2A$ of the converter are assessed using the equations given by 3.114 and 3.5. The precise of the above calculations is verified by the simulation results and waveforms presented in Figure 4.16.

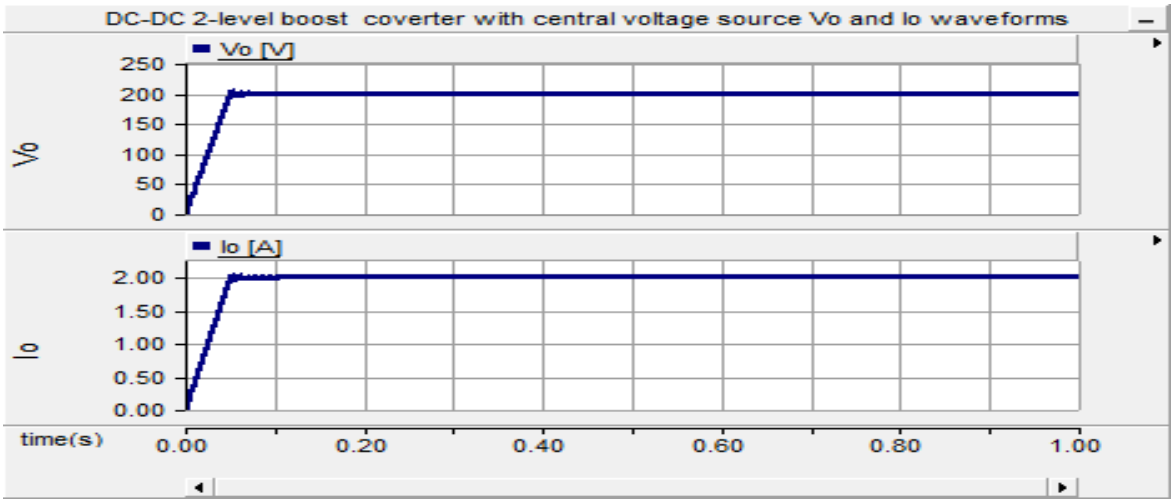



**Figure 4.17:** Voltage and current output waveforms for two-level MBC with CVS

The average voltages $V_{C1} = V_{C-1} = 100V$ across the load feeding capacitors $C_1$ and $C_{-1}$ are calculated by the same equation 3.3, with an output voltage $V_o = 100V$ of the simulated converter. The waveforms shown in Figure 4.17 and the assumptions made to the values of the capacitors confirm the validity of the analyzed equations.

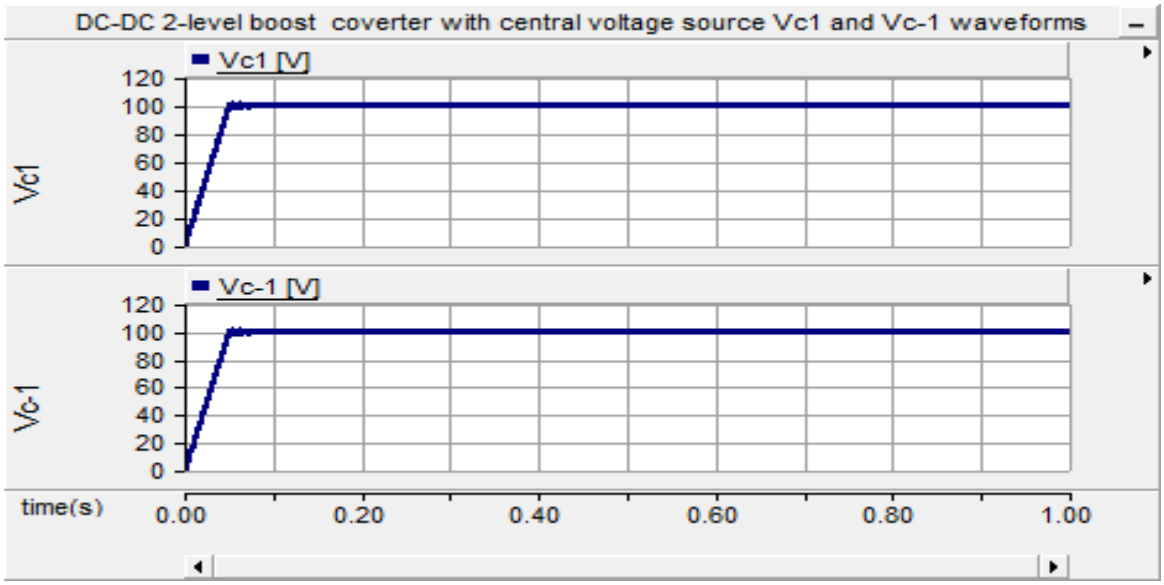



**Figure 4.18:** Capacitors ($C_1$ and $C_{-1}$) voltage waveforms for two-level MBC with CVS

According to the given values in Table 4.5 and the concept of MBC, the voltages of the inductor in the intervals $DT = 5\mu S$ and $(1-D)T = 5\mu S$ are evaluated as $V_L = 50V$ and $V_L = -50V$ respectively. Also, from the estimated equation 3.117 the average value of the inductor current $I_L = 8A$ is calculated. The waveforms of the simulation are shown in Figure 4.18 confirm the accuracy of the estimation.

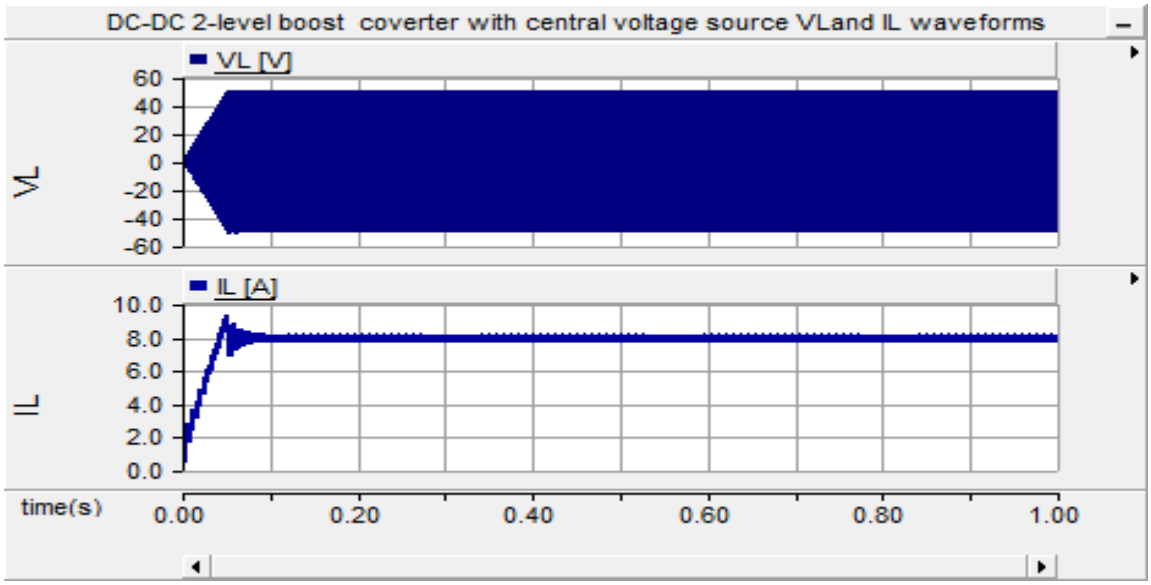



**Figure 4.19:** Inductor voltage and current waveforms for two-level MBC with CVS

The voltage stress of the converter on the switch in the duration of $(1-D)T = 5\mu S$ is calculated as $V_s = 100V$ with the same equation given by 3.38 and the specifications shown in Table 4.5. And the voltage stress is zero in the first half cycle at $DT = 5\mu S$. The verifications of the calculations are illustrated in Figure 4.19.

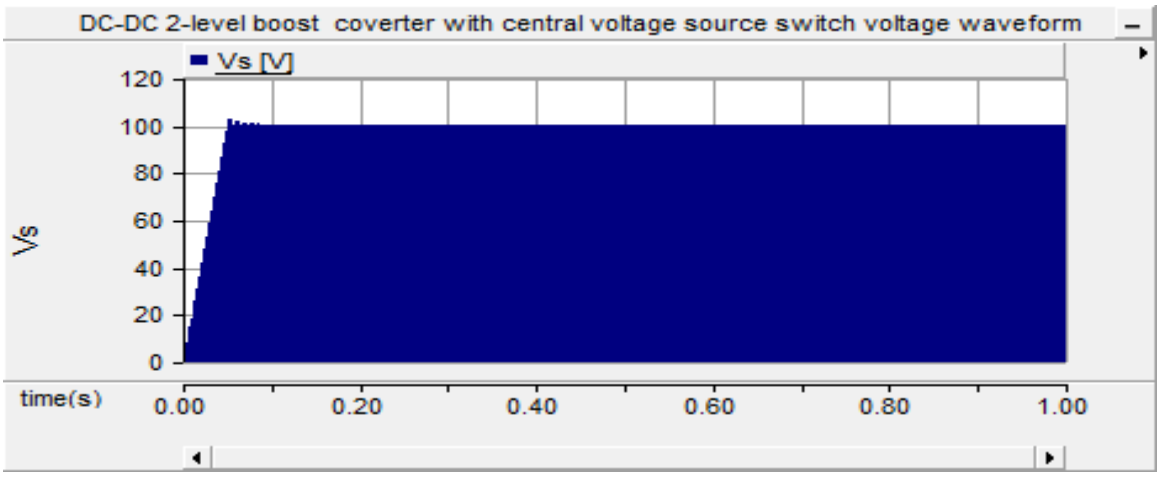



**Figure 4.20:** Switch voltage waveform for two-level MBC with CVS

### 4.2.6 Verification of the obtained equations for three-level DC-DC MBC with CVS

**Table 4.6:** Specifications of the three-level DC-DC boost converter with CVS

| **Components** | **Specifications** |
|---|---|
| Voltage Source($V_i$) | $50V$ |
| Inductance($L$) | 1.33mH |
| Duty cycle($D$) | 0.5 |
| Capacitance($C_1$,, $C_2$, $C_2'$, $C_{-1}$ and $C_{-2}'$) | 100µF |
| Load Resistance($R$) | 100Ω |
| Switching frequency($f$) | 100 kHz |

The equations 3.43 and 3.5 are used to evaluate the average values of the output voltage and current of the converter exactly as $V_o = 300V$ and $I_o = 3A$ respectively. The waveforms of the converter presented in Figure 4.20 prove the accuracy of the solutions.

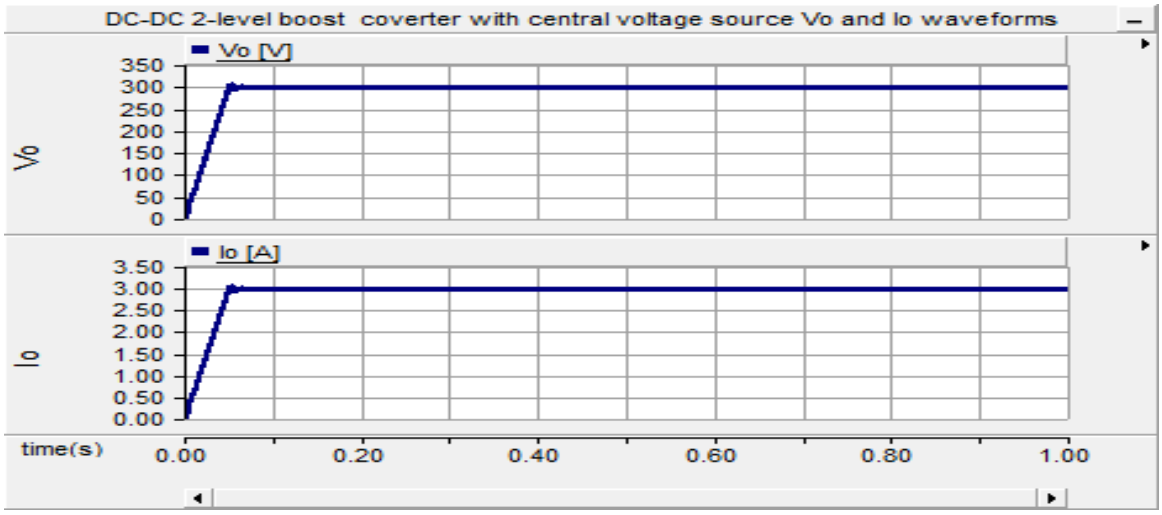



**Figure 4.21:** Voltage and current output waveforms of the three-level MBC with CVS

From, the converter's simulation results an output voltage of $V_o = 100V$ is generated, thus the voltage across the capacitors $C_1, C_2$ and $C_{-1}$ are estimate to $V_{C1} = V_{C-1} = V_{C2} = 100V$ using the given expression 3.42. Furthermore, the validity of the assumptions made to the capacitance value and the above calculations are supported by the waveforms shown in Figure 4.21.

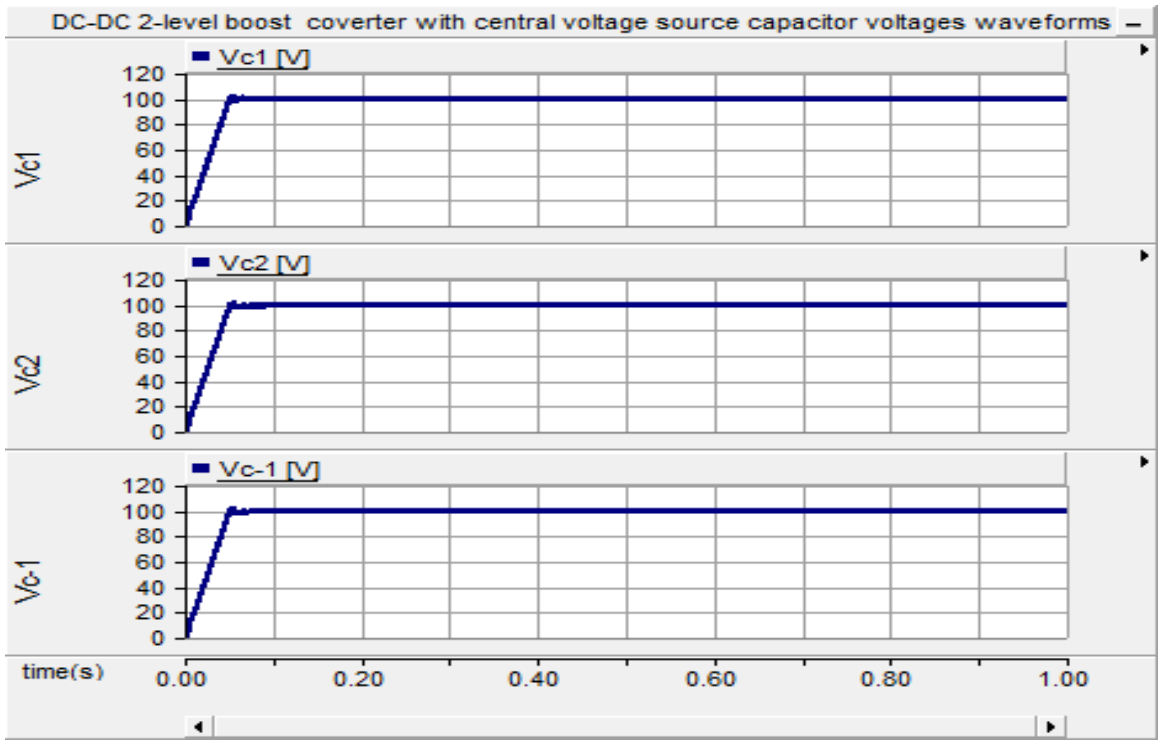



**Figure 4.22:** Voltage waveforms of ($C_1, C_2$ and $C_{-1}$) for three-level MBC with CVS

According to the explanation given in section 3.2.1, the average voltages of the inductor in the in the time intervals $DT = 5\mu S$ and $(1-D)T = 5\mu S$ are calculate to get a values $V_L = 50V$ and $V_L = -50V$. The average value of the inductor current, which is the same as the average input current, will be estimated $I_L = 18A$ using the relation 3.44. The inductor's voltage and current waveforms are shown in Figure 4.22 to verify the result.

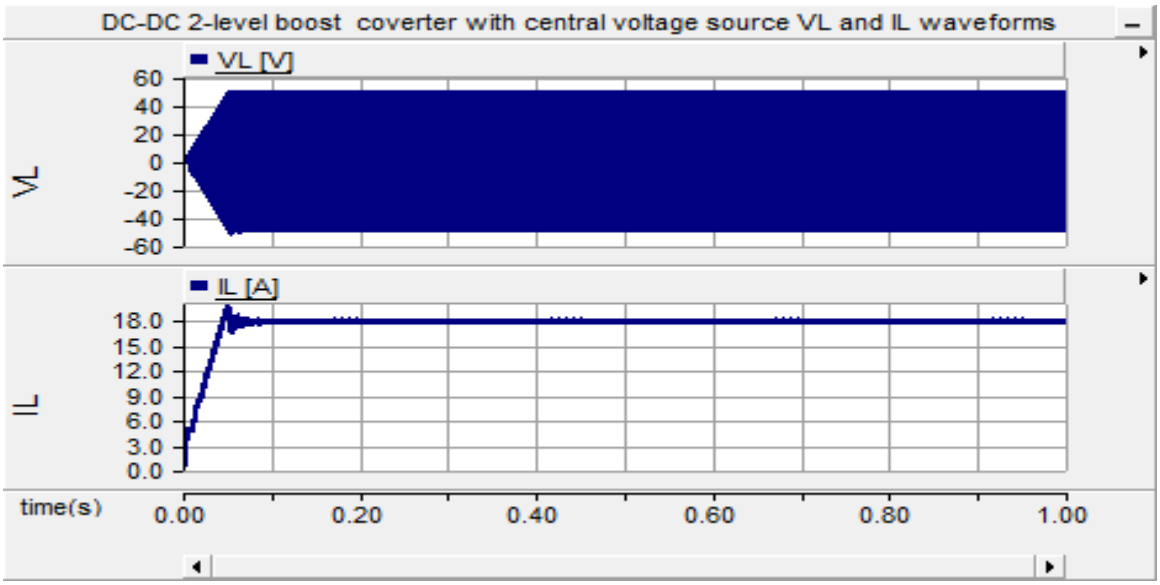



**Figure 4.23:** Inductor voltage and current waveforms for three-level MBC with CVS

Using the equation (1-262) and the values of Table 1.6, the voltage stress on the switch at $(1-D)T = 5\mu S$ will be calculated to a value of $V_s = 100V$. But, in the time interval $DT = 5\mu S$ the switch voltage is zero. The validity of the calculations is confirmed by the waveform shown in Figure 4.23.

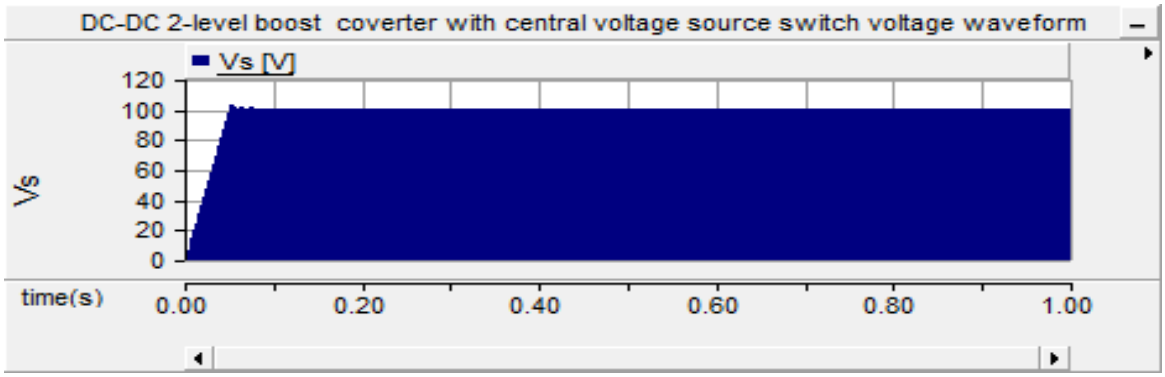



**Figure 4.24:** Switch voltage waveform for three-level DC-DC MBC with CVS

# CHAPTER 5
# CONCLUSIONS AND FUTURE SCOPES

## 5.1 Conclusion

As the key objective of this research is concerned with the high voltage conversion aspects, the work is entirely focused on advanced voltage multiplier DC-DC converters for HVDC /AC grid connected PV sectors via DC-link. The methodology of designing and analysis of the selected alternative converter was mainly established on the principle of MBC. The topology was performed by combining the fundamental structure of DC-DC BC with high voltage boosting capability switched capacitors without altering its principal prototype. In addition, $2n-1$capacitors, $2n-1$ diodes, one inductor and PWM controlled single switch were integrated to build up the $n$ times MBC. The desired conversion ratio was improved by providing a multiple output voltages while controlling and regulating the self-voltage balancing switch capacitors using PWM controlling apparatus. The presented work was carried out to analyze and implement the modular research according the required number of voltage levels starting from the simple to the extended higher stages of MBC. Moreover, the mathematical equation for currents, voltages, boost ration and efficiency were estimated and the impact of the parasitic loss as well as semiconductor voltage drops on the boost ratio were also investigated. The converter was simulated to confirm that the theoretical calculations and experimental solutions were analogue. From the obtained results and the presented graphs it is shown that the converter operates continuously at a duty cycle 0.5 with a voltage gain varies from 4.5 to 8 even at higher values of ratio and also the performed system assures the continuity of input/output current flow for high voltage areas. In the previous work the conversion ratio was ran from 2.5 until 4.5 at higher value of duty cycle. Furthermore, the efficiency of this topology was estimated greater than 99% with a reduced output current and increased output voltage, as a result the voltage stress on switch as well as the ripples of current and voltage are minimized. Finally, the voltage gain of the MBC is achieved better with a duty cycle limited to the desired level of the intended applications, which allows the high power system to work at very high switching frequency.

## 5.2 Future Scopes of the Work

Even though, the contributed work is enough sufficient to implement practically, but there are several possible future enhancements that can be further developed for this thesis. In the proposed converter as the number of stages increases the number of capacitors and diodes also increases, thus in future a major potential achievement is to introduce a MBC with less number of such semiconductor devices for higher levels. Another essential improvement is to expand the principle of this work for multilevel inverters with balanced output voltages and to design a multilevel boost converter with triple inputs that is PV-panel, full-cell and battery.

## REFERENCES


Almousa, M., Moeini , A., & Modares, S. (2016). A High Efficiency DC/DC Boost Converter for Photovoltaic Applications. *International Journal of Soft Computing and Engineering (IJSCE), 06*(02), 31-37.

Balakishan, C., Sandeep, N., & Aware, M. (2015). Design and Implementation of Three-Level DC-DC Converter with Golden Section Search Based MPPT for the Photovoltaic Applications. *Hindawi Advances in Power Electronics, 2015*, 1-9.

Balakrishnan, D., Shanmugam, D., & Indiradevi, K. (2013). Modified Multilevel Inverter Topology for Grid Connected PV Systems. *American Journal of Engineering Research (AJER), 02*(10), 378-384.

Cao, D., Jiang, S., & Peng, F. (2013). Optimal Design of a Multilevel Modular Capacitor-Clamped DC–DC Converter. *IEEE Transactions on Power Electronics, 28*(08), 3816-3826.

Chan, P., & Masri, S. (2014). *DC-DC Boost Converter with Constant Output Voltage for Grid Connected Photovoltaic Application System*. Retrieved from www.research gate.net/265045922.

Dam , S., & Mandal, P. (2018). An Integrated DC–DC Boost Converter Having Low-Output Ripple Suitable for Analog Applications. *IEEE Transactions on Power Electronics, 33*, pp. 5108-5117.

Elbuluk , M., & Da Silva, E. (2013). Fundamentals of Power Electronics. In *Power Electronics for Renewable and Distributed Energy Systems* (pp. 7-59). London: Springer.

Forouzesh , M., & Lehman , B. (2017). Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies and Applications. *IEEE Transactions on Power Electronics, 32*(12), 9143-9178.

Ganesan, G., & Prabhakar, M. (2013). Multi-Level DC-DC Converter for High Gain Applications. *International Journal of Power Electronics and Drive System (IJPEDS), 03*(04), 365-373.

Khazaei, P., Almousa , M., & Modares, S. (2016). A High Efficiency DC/DC Boost Converter for Photovoltaic Applications. *International Journal of Soft Computing and Engineering (IJSCE), 06*(02), 31-37.

Kumar, L. (2017). Control of a Modular Multilevel DC/DC Converter for Regenerative Applications. *International Research Journal of Engineering and Technology (IRJET), 04*(10), 1014-1020.

Luo, F., & Ye, H. (2004). *Advanced DC-DC Converters.* Nanyang, Singapore: Nanyang Technological University.

Mademlis, G. (2015). *Control and Design of the Multistage Stacked Boost Architecture (MSBA).* Thessaloniki, Greece: Aristotle University of Thessalonik.

Miracle, D., Campos , M., & Rufer, A. (2013). Design and Control of a Modular Multilevel DC/DC Converter for Regenerative Applications. *IEEE Transactions on Power Electronics, 28*(08), 3970-3979.

Misoca, F. (2007). *Comparative Study of DC–DC Converters' Effects on the Output Characteristics of Direct Ethanol Fuel Cells and Nicd Batteries.* Kansas: Kansas State University Manhattan.

Monem, M., Hegazy , O., & Omar, N. (2013). Comparative Study of Different Multilevel DC/DC Converter Topologies for Second-Life Battery Applications. *EVS27 International Battery, Hybrid and Fuel Cell Electric Vehicle Symposium*, (pp. 1-10). Barcelona.

Mudliyar, K. (2013). *Multi-Phase Multi-Stage DC-DC Converter.* Karnataka, India: Manipal Instituteof Technology.

Peng, F., Ramirez, J., & Rosas, J. (2008). A DC-DC multilevel boost converter. *IET Power Electronics, 03*(01), 129-137.

Puneeth, K., & Nattarasu, V. (2014). Modeling and Analysis of Three Level DC-DC Boost Converter for High Gain Applications. *International Journal of Engineering Science and Innovative Technology (IJESIT), 03*(03), 339-351.

Qin, R. (2016). *Study on Three-level DC/DC Converter with Coupled Inductors.* Blacksburg, Virginia: Virginia Polytechnic Institute and State University.

Rai, J., Gupta , N., & Bansal, P. (2012). Design and Analysis of DC-DC Boost Converter. *International Journal of Advance Research and Innovation, 04*(03), 499-552.

Rasheed, M., Omar, R., & Sulaiman, M. (2016). Design and Development of DC-DC Boost Converter based on DSP TMS320F2812 for PV Application. *Indian Journal of Science and Technology, 9(44)*, 1-13.

Rashid , M. (2001). *Power Electronics Series Engineering Handbook.* Florida, U.S.A: Academic Press Series in Engineering.

Rosas, J., Ramirez, J., & Martin, P. (2008). Novel DC–DC multilevel boost converter. *IEEE Power Electronics Specialists Conference*, (pp. 2146-2151).

Sanjeevikumar , P., & Rajambal, K. (2008). Extra-High-Voltage DC-DC Boost Converters Topology with Simple Control Strategy . *Hindawi Modelling and Simulation in Engineering, 2008*, 1-8.

Shephed, W. (2004). *Power converter Circuits.* New york, U.S.A: Marcel Dekker, Inc. Press.

Skvarenina, T. (2002). Multilevel Converters Purdue University. In *The power Electronics Hand Book* (pp. 240-255). West Lafayette, Indiana: CRC Press LLC.

Soman, E. (2017). *Multilevel Converters with Smart control for Wave Energy Conversion.* Uppsala, Sweden: Uppsala University.

Song, Q., Liu, W., & Rao, H. (2013). A Steady-State Analysis Method for a Modular Multilevel Converter. *IEEE Transactions on Power Electronics, 28*(08), 3702-3713.

Thomas, L., Midhun, S., & Thomas , J. (2014). DC to DC Boost Converter for Custom BasedApplication. *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, 03*(02), 7655-7658.