DESIGN AND ANALYSIS OF DEVELOPED SEPIC CONVERTER

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

BY

EJIOFOR MAC-ROWLAND CHIDERA

In Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical and Electronics Engineering

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EJIOFOR MAC-ROWLAND CHIDERA: THE DESIGN AND ANALYSIS OF A SEPIC CONVERTER AND A NEW PROPOSED SEPIC CONVERTER (DC-DC CONVERTER)

Approval of Director of Graduate School of Applied Sciences

Prof. Dr. Nadire ÇAVUŞ

We certify this thesis is satisfactory for the award of the degree of Masters of Science in Electrical and Electronics Engineering

Examining Committee in Charge:

Prof. Dr. EbrahimBabaeiSupervisor, Department of Electrical and Electronics Engineering, University of Tabriz

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name:

Signature:

Date:

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ABSTRACT

The purpose of this thesis is to show the increase in efficiency when a SEPIC converter is designed as a closed loop instead of the basic open loop converter and also to show the increase in efficiency when the new proposed SEPIC converter is used compared to the old topology and we would see all this as we go through the paper. By the use of a PID controller and PWM modulator we analyze the SEPIC converter to see the increase in efficiency of a closed loop converter when compared to an open loop SEPIC converter and how the output voltage increases using the same components rating of the circuits. Know that a SEPIC converter works both as a boost and as a buck converter depending on the value of the duty cycle and it is preferred mostly because of this function and the fact that it provides an output with the same polarity unlike the buck-boost converter. Going on we analyzed the closed loop circuit of the SEPIC converter and the efficiency with the output results to show the increase in efficiency compared to the open loop SEPIC converter. Lastly and most importantly looking at the new proposed SEPIC converter which we apply some changes by adding two resonant capacitors in parallel to the two switching components simultaneously both in the open and closed loop SEPIC converter using the same parameters but as an improved circuit with the aim of achieving better performance and output results.

Keywords: SEPIC converter (single ended primary inductor converter); ZVS (zero voltage switching); PID controller (proportional integral derivative controller); Resonant capacitors; Efficiency

ÖZET

Bu tezin amacı, bir SEPIC dönüştürücüsünün, temel açık döngü dönüştürücüsü yerine kapalı bir döngü olarak tasarlanması durumunda verimlilikteki artışı göstermek ve aynı zamanda önerilen yeni SEPIC dönüştürücüsü, eski topolojiye kıyasla kullanıldığında verimlilik artışını göstermektir. ve tüm bunları kağıttan geçerken görüyoruz. Bir PID denetleyicisi ve PWM modülatörü kullanarak, bir açık döngü SEPIC dönüştürücüsüyle karşılaştırıldığında kapalı döngü dönüştürücüsünün verimliliğindeki artışı ve açık devre SEPIC dönüştürücüsüyle karşılaştırıldığında çıkış voltajının devrelerin aynı bileşen sınıfını kullanarak nasıl arttığını görmek için SEPIC dönüştürücüsünü analiz ederiz. Bir SEPIC dönüştürücüsünün, görev döngüsünün değerine bağlı olarak hem bir destek hem de bir konvertör olarak çalıştığını ve çoğunlukla bu işlev ve kova yükseltme konvertörünün aksine aynı polariteye sahip bir çıktı sağladığı için tercih edildiğini bilin . Devam edersek, SEPIC dönüştürücüsünün kapalı devre devresini ve açık döngü SEPIC dönüştürücüsüyle karşılaştırıldığında verimdeki artışı göstermek için çıktı sonuçları ile verimliliği analiz ettik. Son olarak ve en önemlisi, hem açık hem de kapalı devre SEPIC dönüştürücüsünde aynı parametreleri kullanarak, aynı amaçlarla geliştirilmiş bir devre olarak aynı anda iki anahtarlama bileşenine paralel olarak iki rezonant kapasitör ekleyerek bazı değişiklikler yaptığımız, önerilen yeni SEPIC dönüştürücüsüne bakıyoruz. daha iyi performans ve çıktı sonuçları elde etmek.

Anahtarkelimeler: SEPIC dönüştürücü (tekuçlubirincilindüktördönüştürücü); ZVS (sıfırvoltajanahtarlaması); PID kontrolörü (oransal integral türevkontrolörü): Rezonanskondansatörler; verimlilik

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LIST OF ABBREVIATIONS

ZVS:	Zero Voltage Switching
SEPIC:	Single Ended Primary Inductor Converter
ZCS:	Zero Current Switching
DCM:	Discontinuous Conduction Mode
CCM:	Continuous Conduction Mode
DC:	Direct Current
PWM:	Pulse Width Modulation
KVL:	Kirchoffs Voltage Law
RMS:	Root Mean Square
PID:	Proportional, Integral, Derivative Controller
ESR:	Equivalent Series Resistance
PCB:	Printed Circuit Board
LI-ON:	Lithium Ion
Ni-MH :	Nickel Metal Hydride

CHAPTER 1
INTRODUCTION

1.1 Introduction

All electronics devices contain circuits for it to function and these circuits must have a way of regulating their supply voltage for appropriate functionality. A voltage regulator is also an electronic circuit used for controlling and regulating the output of the input supply voltage to a desired output voltage. And with the change and advancement in technology a more advanced and improved circuit is needed as time passes for different applications to achieve accurate results and more efficient output. This has led to the improvement and upgrade of previously produced circuits. So in this paper first shown is a direct current to a direct current circuit (converter) used for voltage regulation of an unregulated direct power source to produce the desired output. As the paper continues it is narrowed down to the new proposed circuit topology made to produce a highly efficient circuit used for voltage regulation, generally the new circuit topology produces less loss of energy and lower possibility of damage in the circuit even when carrying out a high frequency operation. Before going deep into the idea of the paper, get the idea generally on a DC-DC converter which the paper is on.

What are DC-DC converters, first understand the functions of dc-dc converter before moving forward into the main idea of this project. So it is safe to start by saying there are many power converters in electric power system applications such as AC-DC converters (rectifier), DC-AC converters (inverters), AC-AC converters and what we will be looking at in this paper DC-DC converter is an electrical circuit or system that converts a direct current source from one voltage to another without changing the form of the current. It consists of switches for controlling the connection or disconnection of the power supply, energy storage components like inductors and capacitors. They are generally used as voltage regulators to produce a regulated power supply. DC-DC converters are generally

used in automobiles, portable chargers, DVD players, laptop chargers, etc. Note that voltage regulation is necessary for the safety of the devices (as well as function).

There are different classes of DC-DC converters and it could be used to either step-up (boost) the voltage level, step down (buck) the voltage level and in some cases maintain the same input voltage level at the output.

1.2 Objective

This thesis is aimed at a specific type of DC-DC converter known as a single ended primary inductor converter, which is similar to a buck-boost converter topology only that it is better because unlike the buck-boost converter it produces an output voltage having the same polarity as the input. This project focuses on a converter that can be used for the functions of step up and step down of voltage level or maintaining the same voltage level over a large range of input voltage. So improving the basic circuit that is used later for a better operation and lesser losses, when you compare the improved circuit to the basic circuit even when running high frequency operations the difference is clear and all these are mentioned below.

In this paper looking at a SEPIC converter in its basic original topology as it first made up by AT&T Bell laboratory in the 1970's, with the purpose of making a new circuit that has properties different from contemporary circuits. The main idea was to buck and boost the voltage without inversion of polarity at its output. Going into the paper and analyzing this new circuit topology, which has been improved from the basic SEPIC converter topology by the addition of a resonant capacitor in parallel to the two switching devices in a basic SEPIC circuit? The purpose of this is to apply the use of resonant switching accompanied with frequency control techniques that are constant to achieve an expanded range of efficient operations. The new converter analyzed here has been done in reference to a new family of ZVS- PWM converter used for high frequency operations and design methods that provide the use of reduced energy storage requirements are introduced. This converter introduced is a resonant converter that implements resonant switching and a suitable

control method for high frequency operation. It is seen that it has high efficiency over very wide input voltage when compared with output voltage ranges. Suitable for stepping up and stepping down with little energy storage required therefore producing a lovely transient response. The improvement is all for a more efficient circuit with reduced kisses while using soft switching techniques. Also looked at is the theoretical working procedure of the SEPIC converter in the next chapter after also seeing brief definitions of different dc-dc converters. Then design, calculate parameters, simulate and analyze the SEPIC converter in its basic form both as open loop and closed loop, then do the same also for the new proposed SEPIC converter in chapter three all to be simulated in MATLAB Simulink then we analyze our results gotten from the models. Finally concluding the whole book based on analysis of the output results and explaining what was achieved from the whole simulation and analysis. Note that in chapter three the circuit is analyzed as the open loop conventional SEPIC converter first then show how it works as buck converter and how it can work as boost converter then move on to the closed loop conventional SEPIC converter and also show the improvement from its open loop stage then, introduced is the new proposed topology and also showing its working state as an open loop while comparing the result to that of a conventional open loop SEPIC converter then also do the same for the new proposed SEPIC converter when it's a closed loop and compare it with the conventional closed loop SEPIC converter showing majorly the improvements in performance. A similar stuff could have been done using the CUK converter because it also solves the issue of polarity and efficiency that occurs in buck–boost converter but it causeslarge electrical stresses for its components unlike the SEPIC which eliminates such challenges that's why a SEPIC converter is preferred here in this paper.

CHAPTER 2
LITERATURE REVIEW

2.1 DC-DC Converter

As previously explained a DC-DC converter is a converter used for voltage regulation that allows the input voltage to either be stepped up, stepped down or regulated to produce the same voltage as that of its input. There are different types of DC-DC converters which we mention here the buck converter, the boost converter, the buck-boost converter, CUK converter, SEPIC converter, zeta converters and a few others. Some include the combination of two converters as in the case of buck-boost converter to get a specific function. As in the world just like technology advances so does topologies of DC-DC converters advance. Daily new circuits are made to improve the efficiency and working conditions of previously made converter. it is best to talk on a few mentioned converters describing them briefly before going into the main purpose of the paper.

2.1.1 Buck Converter

Here this can be defined as a circuit specifically used for the reduction in the voltage level of the input to produce a lower voltage level at the output and generally known as step down converters. Example is a computer or radio's charger or adapter, the pc or radio functions at a low voltage level when compared to that one delivered by the transformer to a home and even the one delivered directly by a socket at home so therefore an adapter is required to step down the voltage gotten from the socket to a suitable voltage that enables the functioning of the radio or pc without it over heating and its components destroying. And also it provides just enough voltage that enables the radio and pc to function. So it regulates it by stepping it down just perfectly where its volts is enough to make the pc work and not too much like the one directly from the socket that could make it over heat and damage. Below seen is a diagram showing a basic buck converter.

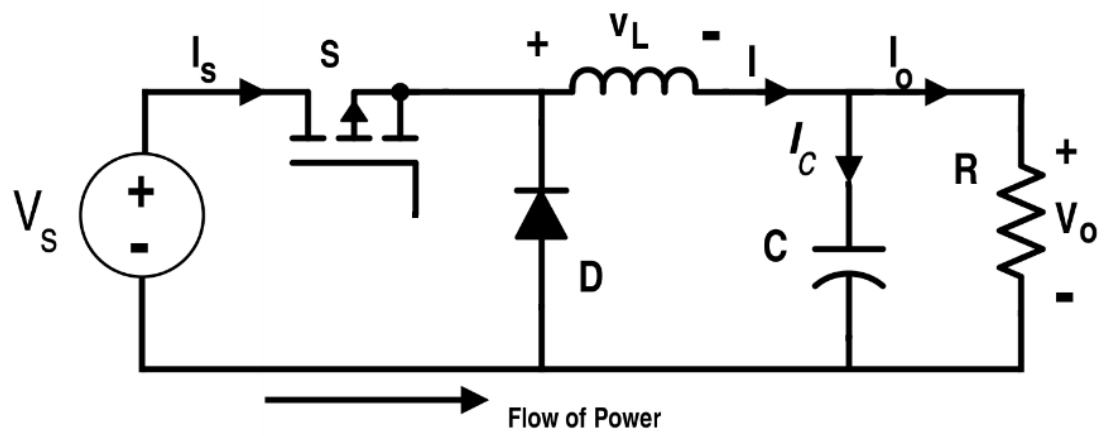

Figure 2.1: A basic buck converter circuit

2.1.2 Boost Converter

This is the opposite of a buck converter and it is a circuit which simply steps up or boosts the voltage level gotten at its input to produce a higher voltage level at its output. Example is a battery sourced power circuits.

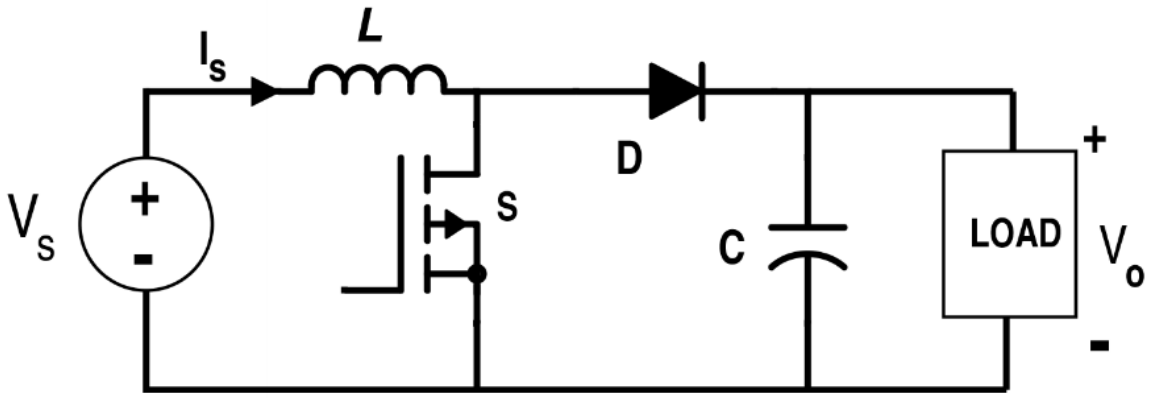

Figure 2.2: A basic boost converter circuit

2.1.3 Buck-Boost Converter

In this converter both the functions of bucking and that of boosting are produced. Meaning we have a power circuit used both for regulation of voltage as a step down and a step up

depending on what's needed and it creates an inverse polarity at the output when compared to the input voltage.

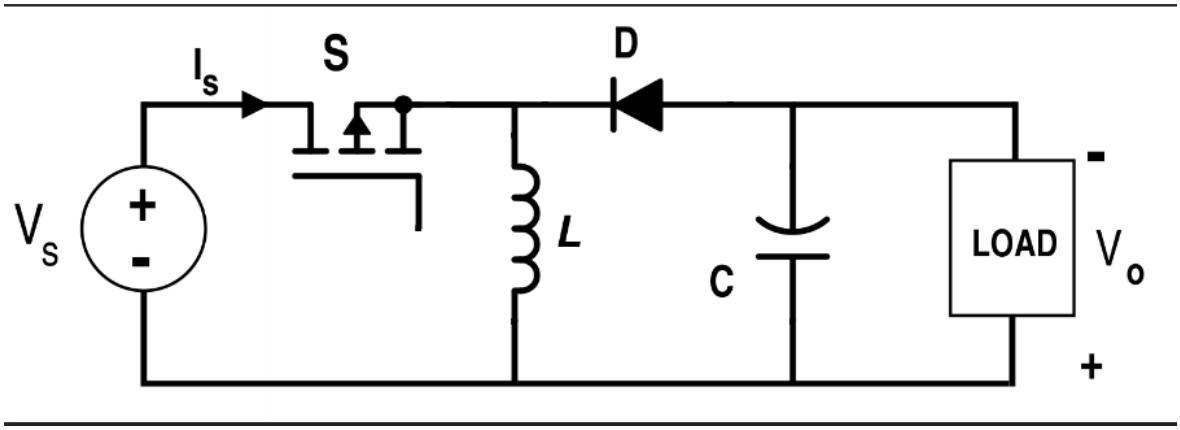

Figure2.3: A basic buck-boost converter circuit

Do not forget also the CUK converter, the fly-back converter, ZETA converter and the likes sometimes not only buck and boost could be combined to provide a new converter others can also be combined in such a manner. So now looking at the SEPIC converter extensively that includes the basic SEPIC working procedure and the new proposed circuit also before proceeding to designing and simulations of the both.

2.2 SEPIC Converter

As the acronym used as its name goes by it is a single ended primary inductor converter which is a fourth order system used in stepping down, stepping up or maintaining voltage levels in switching circuits having the same polarity between its input and output voltage, also having the ability to be extended to multiple outputs. Its output is controlled by the duty cycle of the main switching device. A SEPIC converter also produces a highly efficient circuit with efficiency of 85% and above. We should note that as we stated that the output is controlled by the duty cycle of the switch we mean it's the duty cycle that controls the ability of the SEPIC converter circuit to either buck, maintain or boost the output voltage depending on what is required. Below is a diagram of a basic SEPIC converter.

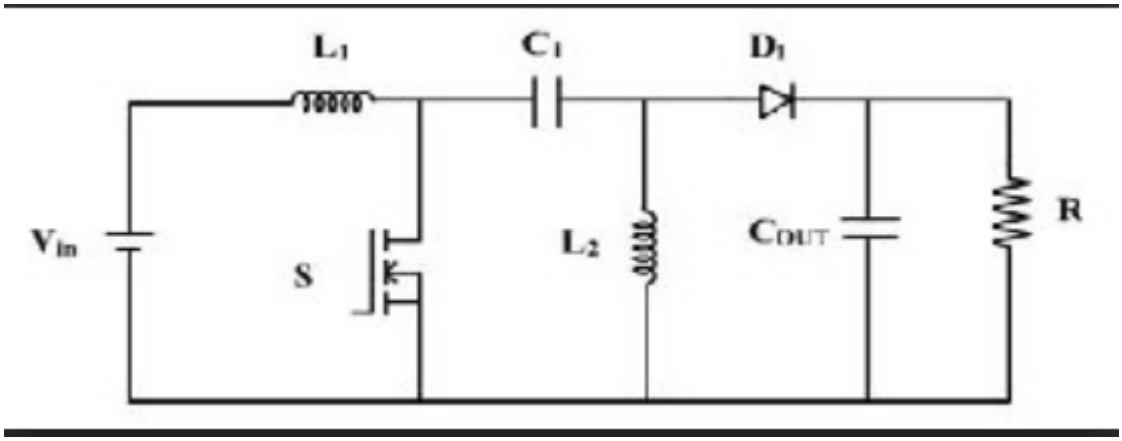

Figure 2.4: A basic SEPIC converter circuit

The image provided helps us understand the design and working procedures of the circuit properly and from what we can see it has two switching components S and D_1. It also has three energy storage elements L_1, L_2, C_1 and C_2 as filter at output. As known the working mode of any switch circuits is dependent on the continuous flow of current in the inductors and voltage across capacitors. So there are different operation modes depending on inductor current and capacitor voltage being continuous or not. Looking at the operation modes of the SEPIC converter.

2.2.1 Operation Modes

We would look at a SEPIC converter both as an open loop converter and as a closed loop converter with a controller present. The SEPIC converter either operates in a CCM (continuous conduction mode) or in DCM (discontinuous conduction mode). Basically here we would look at the operation mode of the circuit as an open loop SEPIC in continuous conduction mode and then as a closed loop also in CCM. First, describing CCM and DCM operation modes briefly before diving deeper into the CCM operation mode of the open loop and closed loop SEPIC converter.

2.2.2 CCM (Continuous Conduction Mode)

In this case, it defines a SEPIC converter to be operating under CCM when the current through the first inductor labeled L_1 never goes down to zero. There it is always conducting all through the circuits run time.

2.2.3 DCM (Discontinuous Conduction Mode)

In this case a SEPIC converter is branded as being in DCM when the current passing through the second inductor named L_2 as seen in the figure four is all is allowed to go to zero at a point.

So narrowing it down in the design, modeling and analysis and assuming the following conditions

- Low ripple on capacitors
- The diode is assumed to have a zero diode voltage
- Low parasitic resistance
- And it is functioned in CCM

The basic SEPIC circuit as seen in figure four consists of input voltage (V_{in}), input inductor (L_1), Coupling capacitor (C_S), Diode (D_1), output Capacitor (C_O), input capacitor (C_{in}), input parasitic resistance (r_1), Load (R_L), (L_2) connected between D_1 and C_S.

$$D_{on} = t_{on}/T \text{ and } D_{off} = t_{off}/T \qquad (2.1)$$

Where T is the period, t_{off} and t_{on} is the off and on time of switch. And a MOSFET switch (S_1) with duty cycle (D)is used. According to the assumptions of CCM the circuit both in the off and on state of the switch is drawn below and it operation mode explained. Note that there are two methods of analysis, namely the circuit averaging method and the state space averaging method and would look at both methods of analyzing the operation modes of the SEPIC converter and the new proposed SEPIC converter.

2.2.4Circuit Averaging Method of Basic SEPIC Converter

In the CCM circuits mode of operation both C_1 and C_2 or we can say C_S and C_{out} are to be assumed as sufficiently large that the voltage ripple across them both is known to be small. Following the direct path for V_1 passing through C_1, L_1, L_2 and back to V_{IN} we note that $V_{Cs}= V_{IN}$ and $V_{Cout} = V_{out.}$ The two stages of operation are firstly when S1 is on the diode is off and when the switch turns off the diode starts conducting. Meaning it has two stages for switching method.

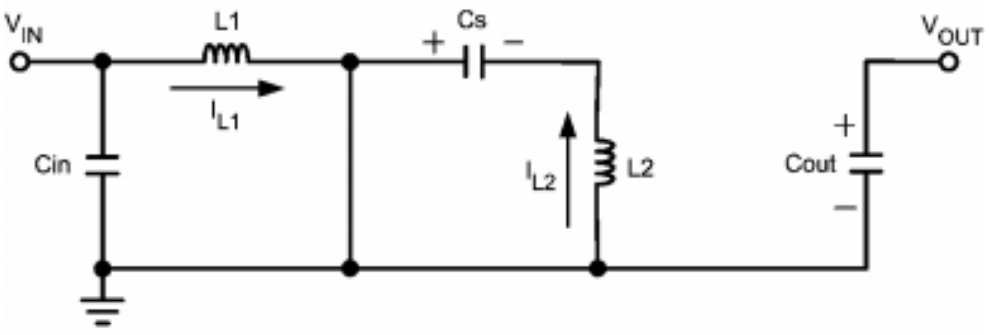

Figure 2.5: A basic SEPIC converter when S_1 is on and D_1 is off

The diagram in figure five is the first stage of the SEPIC converter when the active switch is in its ON state. Note that the whole simulation is done in CCM and would also show the mathematical calculations to explain the two stages of the basic SEPIC converter both in circuit averaging and state space averaging methods of analysis. It includes even the circuit balancing in both stages and when designing our circuit in Simulink, the thesis would show the calculations for the component values or parameter selections. It is best to start by saying that in the first stage when the switch is on the energy is transferred from (V_{IN}) input to the inductor L_1 and at this point voltage across the inductor L_1 is the same as the input voltage (V_{IN}), while the energy stored in the coupling capacitor C_s or C_1 is transferred to the output inductor L_2. The load is also supplied by energy stored in the output capacitor C_{out} or C_2 as shown in figure five. Knowing this helps balance the circuit and show the mathematical analysis of circuit averaging method below.

Applying KVL to circuit when S1 is On

Considering L1

$$IL1 = \frac{VIN}{L1} TON (2.2)$$

Where,

$$V_{L1}=V_{IN} \quad (2.3)$$

Considering L2

$$IL2 = \frac{Vc1}{L2} TON \quad (2.4)$$

$$V_{IN} * t_{on} = V_O(T-t_{on}) \quad (2.5)$$

Therefore equation (2.5) becomes

$$\frac{Vo}{VIN} = \frac{ton}{T-ton} \quad (2.6)$$

Duty cycle D is calculated as

$$D = \frac{ton}{T} \quad (2.7)$$

There fore

$$ton = DT \quad (2.8)$$

We would assume that variable M is equals to

$$M = \frac{Vo}{VIN} \quad (2.9)$$

So substituting M into equations (2.6) we get

$$M = \frac{ton}{T-ton} = \frac{DT}{T-DT} = \frac{D}{1-D} \quad (2.10)$$

Assuming L1 and L2 are large enough that the resulting current ripple is small.

$$Io = (IL1 + IL2)(1 - D) = (IL1 + IL2)\left(\frac{1}{M+1}\right) \quad (2.11)$$

The two inductors L_1 and L_2 to be used could be wound on the same core or two different ones should have the same value.

$$V_{L1}= -V_{L2} \quad (2.12)$$

From the circuit we can say that

$$V_{IN}=V_{L1}+V_{CI}+V_{L2} \quad (2.13)$$

We should note that because of the average voltage therefore;

$$V_{c1}=V_{IN} \quad (2.14)$$

Next look at the switch current, the root mean square current of switch (I_{S1RMS}) is calculated as;

$$I_{S1\ (RMS)}= (IL1 + IL2)\sqrt{D} = Io\sqrt{M + M^2} \quad (2.15)$$

Next are the diode current and voltage calculations;

$$I_{D1\ (average)} =Io$$

$$V_{D1}= V_{IN}+V_O=\frac{1+1}{M} Vo \quad (2.16)$$

Inductor currents;

$$I_{L1\ (RMS)}=I_{L1}=M*Io \quad (2.17)$$

$$IL_{2\ (RMS)}=Io \quad (2.18)$$

Capacitor currents;

$$I_{C1\ (RMS)} =\sqrt{(I^2L1(1 - D)} + \sqrt{I^2L2} = Io\sqrt{M} \quad (2.19)$$

$$I_{C2\ (RMS)} =\sqrt{(I^2o(D)} + \sqrt{(IL1 + IL2 + Io)^2} \quad (2.20)$$

Peak to Peak ripple voltage on CS;

$$\Delta V_{Cs}= \frac{Io*D}{Cs*fsw} \quad (2.21)$$

Where,f_{sw} is the switching frequency of the switch. Note that the capacitor should be rated for a large RMS current relative to output power making it better for low power applications. Usually in this case the RMS current through the capacitor is small relatively to the capacitor technology. The rating of voltage of capacitor used in SEPIC converter must be bigger than the highest input voltage, so in experiments tantalum and ceramic capacitors are the best suited choices.

Power calculations for input and output are given below;

$$V_{IN}*I_{L1}=V_O *I_O \quad (2.22)$$

This is simplified using equation (2.9) to give;

$$M=\frac{Vo}{VIN} = \frac{IL1}{Io} \quad (2.23)$$

Stage 2: When switch goes off and D_1 starts conducting is the second stage that we look at here. Below is the equivalent circuit diagram when switch is off.

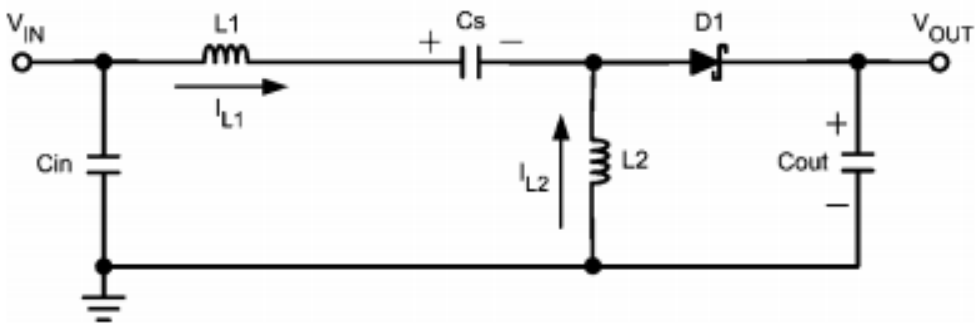

Figure 2.6: A basic SEPIC converter when switch is off and D_1 is on

When switch is off as seen in figure six above the energy that has been stored in input inductors Li is transferred to C1 or Cs while that which got stored in L2 by Cs in the ON state of switch is transferred to C2, charging C2 and also providing energy to the load through the conducting diode. When the cycle finishes switch closes and the process starting from first stage repeats itself. For continuous conduction mode some energy is always retained in inductors L1 and L2 so their currents (IL1 &IL1≠0) never go to zero. So using KVL.

When S1 is off;

T_{off}= (1-D) T

Considering L_1 we can say $V_O = V_{C2}$.

$$I_{L1}=\frac{VIN-Vc1-Vo}{L1}Toff=\frac{VIN-Vc1-Vo}{L1}(1-D)T \quad (2.24)$$

Considering L_2;

$$I_{L2}=-\frac{Vo}{L2}Toff=-\frac{Vo}{L2}(1-D)T \quad (2.25)$$

The average voltage across L_1 and L_2= 0 because it is discharging so;

$$V_{IN}- V_{C1}-V_{L1}-V_{L2}=0 \quad (2.26)$$

$V_{IN}= V_{C1}$; where, $V_{L1}=V_{L2}=0$

From equation (2.) substituting into equation (2.) we have;

$$I_{L1}=\frac{VIN-Vc1-Vo}{L1}(1-D)T=\frac{Vc1-Vc1-Vo}{L1}(1-D)T \quad (2.27)$$

Therefore it becomes;

$$I_{L1}=\frac{-Vo}{L1}(1-D)T \quad (2.28)$$

Ok so now from the ON and OFF state stating this below;

$$I_{L1on}+I_{L1off}=0 \quad (2.29)$$

Implying;

$$\frac{VIN}{L1}TON+(\frac{-Vo}{L1}Toff)=0 \quad (2.30)$$

Knowing that Ton=DT and T_{off} = (1-D) T and substituting into above equation to get;

$$\frac{VIN}{L1}DT-\frac{Vo}{L1}(1-D)T=0 \quad (2.31)$$

So

$$V_O=\frac{Vin*D}{1-D} \quad (2.32)$$

Vo is the average output voltage of the whole circuit. While for a lossless circuit the output current is calculated as below;

$$Io=\frac{1-D}{D}Iin \quad (2.33)$$

L2 and L1 would have same values when using a coupled inductor so inductors of same value is used and magnitude would be the same also the peak – peak ripple current is calculated as;

$$\Delta I_{L1\&L2}=\frac{Vin*D}{fsw*L1} \quad (2.34)$$

The diode current in the off state of the switch can also be calculated as;

$$I_{D1}=I_{CS}-I_{L2}$$

As mentioned earlier in total accordance with the change in duty cycle the SEPIC converter acts as a buck or boost in the sense that when the duty cycle of the switch regulator is 50% the output voltage is to be the same as the iput. When it is greater than 50% , the output value is going to be higher than the input acting as boost converter (step up), when the duty cycle is anything less than the 50%, then the output would be lower than and the circuit acts as a buck converter (step down) here. There is always an output voltage in the

operation mode of a SEPIC converter. The ability of the SEPIC converter to either buck, boost or maintain the input voltage level can be only achieved and depends on the coupling capacitor and the filter inductor L_2. L_1 and S_1 make a standard boost converter that creates voltage (V_{S1}) greater than input voltage (V_{IN}). The value of the voltage is achieved by the duty cycle of S_1, so we have;

$V_O = V_{S1} - V_{IN}$ where $C_S = V_{IN}$ (2.35)

Therefore we can say that;

$V_{S1} < 2V_{IN}$ (buck) (2.36)

$V_{S1} > 2V_{IN}$ (boost) (2.37)

2.2.5State Space Averaging Method of Circuit Analysis

As mentioned earlier,it is safe to analyze the circuit using two methods and already we have seen the first method now we look at the second method of analysis known as the state space averaging method. The state space averaging method involves approximating the switching converter as a linearized system, which is continuous. Here the switching frequency (f_{SW}) must be greater than the effective filter's cutoff or break frequency (f_C). When analyzing a closed loop circuit we should consider that the power stage is in a non-linear state so it has to be approximated to a linear state because it is easier to analyze in that state. Noting that after the approximation to a linear state the closed loop circuit should then be controlled using a feedback loop method and a BODE plot is used to determine the necessary compensation to the feedback loop, for providing specific steady state and transient response that we would like to get. So the state space averaging analysis is used here. The equations are done using matrix operations defining the relationship of the state variables to the input and output. It is best to begin by defining the different variables used here below.

Where;

$\dot{X}$= the time derivative of state variable vector or electric charge of converter

A= system matrix of the converter

x= the state variable vector

B= input matrix of converter

u= input

Y= output

C= output matrix of converter

D= duty ratio or cycle of switch S_1

E= matrix of direct transmission of converter

Knowing that the network has two stages when operating in CCM as mentioned over and over again previously, we would describe the two stages in state space averaging method.

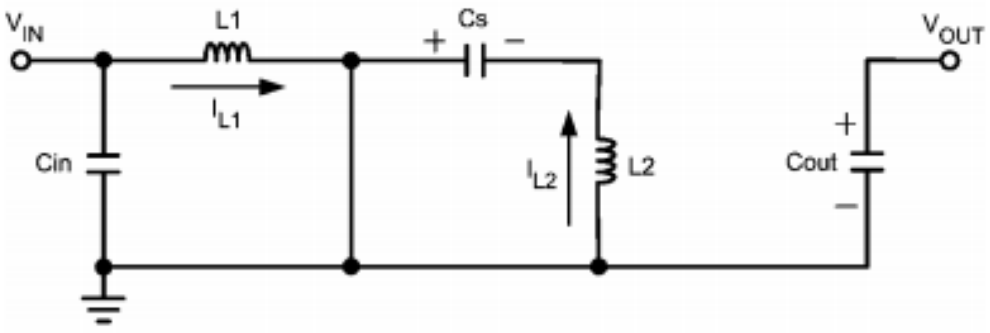

Figure 2.7: Abasic SEPIC converter when $S_1$is on and $D_1$is off

$$\dot{X}= Ax +Bu \quad (2.38)$$

$$Y= Cx +Eu \quad (2.39)$$

When switch is on S_1 is defined as;

S_1 on $(0< t < DT)$

So

$$\dot{X}= A_1x +B_1u =A_1x +B_1V_{IN} \quad (2.40)$$

When switch is off S_1 is defined as;

S_1 off $(0< t < (1-D)\ T)$

So

$$\dot{X}= A_2x +B_2u = A_2x +B_2V_{IN} \quad (2.41)$$

The whole operation of the circuit results in the equation below because the response in each state should be time weighted and averaged;

$$\dot{X}= \{A_1D+ A_2(1-D)\}\ x + \{B_1D+ B_2\,(1-D)\}\ V_{IN} \quad (2.42)$$

Output voltage is described as;

$$Y= V_O= Cx +Eu= Cx +EV_{IN} \quad (2.43)$$

As we have said again and again the desired voltage can be achieved by controlling the duty cycle. This can be varied using a controller to by-pass the disturbances we get in an open loop circuit. The state vectors of the basic SEPIC converter are defined as;

$$X(t)= \begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \end{bmatrix}$$

Knowing I_{L1} and I_{L2} are currents through inductors L_1 and L_2 respectively while V_{C1} or V_{CS} and V_{C2} or V_{CO} are voltages across Capacitor C_S and C_{out} respectively. The diode and Switch are in complementary states.

So starting with stage 1;

When S1 is on and D1 is off (reverse bias) L1 charges from the input as we mentioned in circuit averaging method while L2 charges from Cs and Co discharges to the output the state space averaging equation in this stage is;

$$\dot{X}= \begin{bmatrix} \frac{dIL1}{dt} \\ \frac{dVc1}{dt} \\ \frac{dIL2}{dt} \\ \frac{dVc2}{dt} \end{bmatrix}$$

Where the derivatives values are given as below according to the stage 1 circuit;

$$\frac{dIL1}{dt} = \frac{VIN}{L1}$$

$$\frac{dVc1}{dt} = \frac{-IL2}{C1}$$

$$\frac{dIL2}{dt} = \frac{Vc1}{L2}$$

$$\frac{dVc2}{dt} = \frac{-Vc2}{RC2}$$

So we can translate this as whole to a matrix form to fit the equation below;

$\dot{X}$= Ax +Bu (on state)

So

$$\dot{X}=\begin{bmatrix}\frac{dIL1}{dt}\\ \frac{dVc1}{dt}\\ \frac{dIL2}{dt}\\ \frac{dVc2}{dt}\end{bmatrix}=\begin{bmatrix}0 & 0 & 0 & 0\\ 0 & 0 & \frac{-1}{C1} & 0\\ 0 & \frac{1}{L2} & 0 & 0\\ 0 & 0 & 0 & \frac{-1}{RC2}\end{bmatrix}\begin{bmatrix}IL1\\ Vc1\\ IL2\\ Vc2\end{bmatrix}+\begin{bmatrix}\frac{1}{L1}\\ 0\\ 0\\ 0\end{bmatrix}VIN \qquad (2.44)$$

The above is theequation expressed as the matrix form. From here we can get the other variables when we compare equations (2.38) and equations (2.44) to be;

$$A_1=\begin{bmatrix}0 & 0 & 0 & 0\\ 0 & 0 & \frac{-1}{C1} & 0\\ 0 & \frac{1}{L2} & 0 & 0\\ 0 & 0 & 0 & \frac{-1}{RC2}\end{bmatrix}$$

$$B_1=\begin{bmatrix}\frac{1}{L1}\\ 0\\ 0\\ 0\end{bmatrix}$$

So now we look into stage 2 of the basic SEPIC converter, when the switch S1 is off and diode D1 is on (conducting) as seen in diagram below.

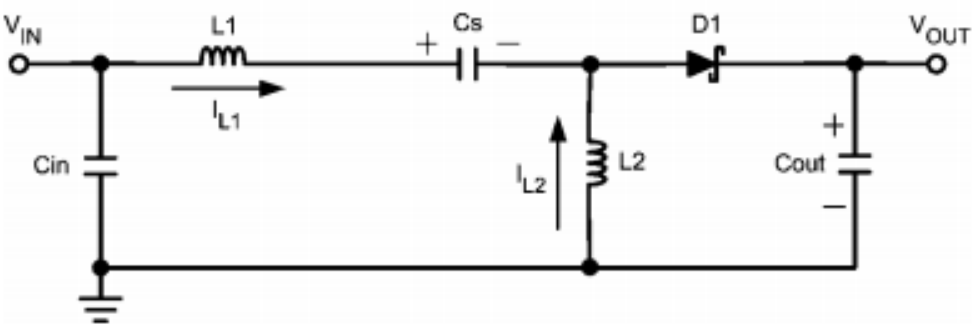

Figure 2.8:A basic SEPIC converter when S1 is off and D1 is on

We have the following derivative values;

$$\frac{dIL1}{dt}=\frac{VIN-Vc1-Vc2}{L1}$$

$$\frac{dVc1}{dt} = \frac{IL1}{C1}$$

$$\frac{dIL2}{dt} = \frac{-Vc2}{L2}$$

$$\frac{dVc2}{dt} = \frac{IL1+IL2}{C2} - \frac{Vc2}{RC2}$$

So we can translate this as whole to a matrix form to fit the equation below;

$\dot{X}$= Ax +Bu (off state)

So

$$\dot{X}=\begin{bmatrix} \frac{dIL1}{dt} \\ \frac{dVc1}{dt} \\ \frac{dIL2}{dt} \\ \frac{dVc2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L1} & 0 & \frac{-1}{L1} \\ \frac{1}{C1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C2} & 0 & \frac{1}{C2} & \frac{-1}{RC2} \end{bmatrix} \begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \end{bmatrix} VIN \qquad (2.45)$$

The above is the equation expressed as the matrix form. From here we can get the other variables when we compare equations (2.38) and equations (2.45) to be;

$$A_2=\begin{bmatrix} 0 & \frac{-1}{L1} & 0 & \frac{-1}{L1} \\ \frac{1}{C1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C2} & 0 & \frac{1}{C2} & \frac{-1}{RC2} \end{bmatrix}$$

$$B_2=\begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

So from the analysis we have gotten A_1, A_2, B_1, B_2, therefore $\dot{X}$ can be generally described below both on and off state as;

$$\dot{X}= \{A_1D+ A_2(1\text{-}D)\}\ x + \{B_1D+ B_2(1\text{-}D)\}\ V_{IN} \qquad (2.46)$$

Substituting our matrix representation of the variables above into equation we can say this in matrix form is shown as;

$$\dot{X}= \{\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C1} & 0 \\ 0 & \frac{1}{L2} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC2} \end{bmatrix} D+ \begin{bmatrix} 0 & \frac{-1}{L1} & 0 & \frac{-1}{L1} \\ \frac{1}{C1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C2} & 0 & \frac{1}{C2} & \frac{-1}{RC2} \end{bmatrix} (1\text{-}D)\} \begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \end{bmatrix} +$$

$$\begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \{D+ (1\text{-}D)\}\ V_{IN}$$

And the general output matrix form is represented as;

$$Y= [0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{IN}$$

From this we can relate our output state space equation and compute the matrix form of the output state variables E and C;

$$C= [0 \quad 0 \quad 0 \quad 1]$$

$$E= [0]$$

Next we derive the transfer function of the system. And as we know the formula for transfer function of any system H(s) is the Laplace transform of the output divided by the Laplace transform of the input;

$$H(s) = \frac{output}{input} = \frac{Y(s)}{U(s)} \qquad (2.47)$$

So we start by finding the Laplace transform of $\dot{X}$ which isX (s) so we can get our Y(s). Okay now knowing our,

$$\dot{X}= Ax +Bu$$

And

$$Y= Cx +Eu$$

The Laplace transform of $\dot{X}$ is;

$$Sx(s) = Ax(s) +Bu(s) \qquad (2.48)$$

Which we can simplify as;

$$Sx(s) - Ax(s) =Bu(s)$$

$$Bu(s) = x(s) [IS-A] \qquad (2.49)$$

Note we have to multiply S by an identity matrix to match A, because A is in matrix form. So;

$$X(s) = \frac{Bu(s)}{[IS-A]} = [IS - A]^{-1}Bu(s) \quad (2.50)$$

Substituting X(s) into the Laplace transform of Y which is;

$$Y(s) = Cx(s) + Eu(s)$$

We have;

$$Y(s) = C[IS - A]^{-1}Bu(s) + Eu(s) \quad (2.51)$$

So the transfer function of the system is;

$$H(s) = \frac{Y(s)}{U(s)} = \frac{C[IS-A]^{-1}Bu(s) + Eu(s)}{u(s)} = C[IS - A]^{-1}B + E$$

Knowing E=0 from equation (2.) we have;

$$H(s) = \frac{Y(s)}{U(s)} = C[IS - A]^{-1}B \quad (2.52)$$

2.3 The New Proposed ZVS SEPIC Converter

The difference between the basic SEPIC converter and the proposed ZVS SEPIC converter that is resonant is the two resonant capacitors added in parallel to the switching devices switch S1 and Diode D1 as we stated earlier. This is done for the purpose of increasing the efficiency of the SEPIC converter, reducing the cost of the SEPIC converter and increasing the response time of the system. The new SEPIC converter has resonant capacitors and inductors involved that are fined tuned to reduce magnetic components count, create a more efficient system and increase the speed at which the whole system responds. In this new circuit topology, L1 becomes in resonance with the combined switching capacitance of the capacitor C_{SW} across the switch and the coupling capacitance Cs.While L2 is in resonance with the capacitance across the diode CD which is responsible for resonant rectification. The switching loss and stress is reduced by the introduction of these new capacitors, so we also attain a ZVS condition at when the switch comes on which helps increasing the efficiency of the system. Below we have the diagram of the new design of the SEPIC converter and then carry out our analysis of the on and off stages of the switch using state space averaging method below.

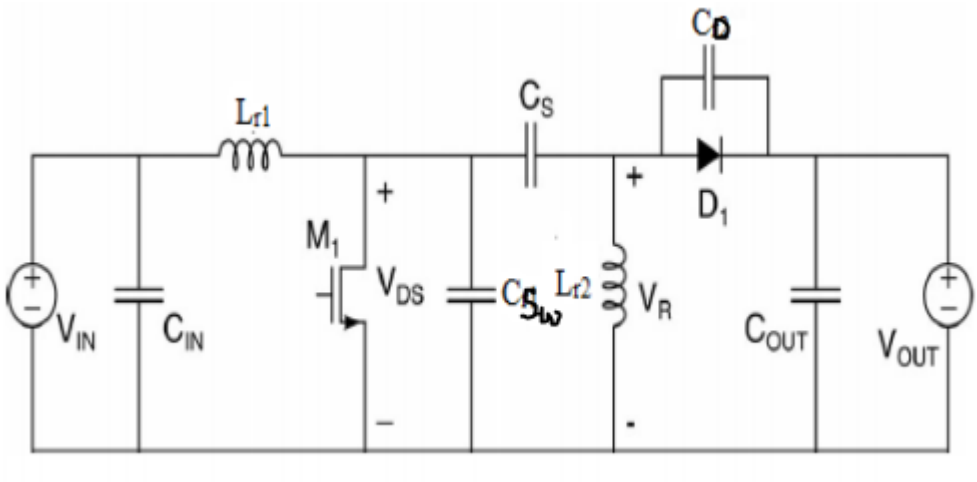

Figure 2.9: The new ZVS SEPIC converter

So using state space averaging method of analyzing this new sepic we still have to consider the stages of the circuit above which would be when switch S_1 or Mosfet switch M_1 is on while diode is non conducting and second stage when M_1 is off and diode D_1 is conducting.

For stage 1;

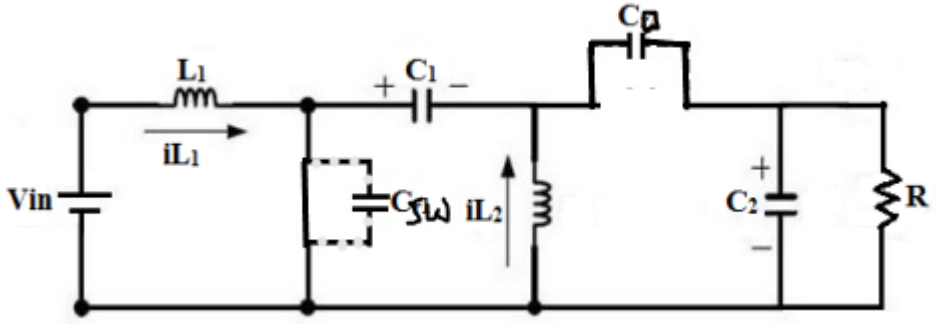

Figure 2.10: The new ZVS SEPIC converter when S1 is on and D1 is off

When switch M1 is on and diode D1 is off, we have the diagram as seen above and our state space equation for stage one is seen below. The state variables in this new converter are I_{L1}, V_{C1}, I_{L2}, V_{C2}, V_{CSW}, V_{CD}.

So when switch is on we have;

$$X(t)= \begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \\ \text{Vcsw} \\ \text{VcD} \end{bmatrix}$$

And the derivative is seen as;

$$\dot{X}= \begin{bmatrix} \frac{dIL1}{dt} \\ \frac{dVc1}{dt} \\ \frac{dIL2}{dt} \\ \frac{dVc2}{dt} \\ \frac{dVsw}{dt} \\ \frac{dVcD}{dt} \end{bmatrix}$$

Knowing this we can describe each derivative value according to the circuit in figure

$$\frac{dIL1}{dt} = \left(\frac{VIN}{L1}\right)$$
$$\frac{dVc1}{dt} = -\frac{IL2}{C1}$$
$$\frac{dIL2}{dt} = \frac{Vc1}{L2}$$
$$\frac{dVc2}{dt} = -\frac{Vc2}{Rc2}$$
$$\frac{dVsw}{dt} = 0$$
$$\frac{dVcD}{dt} = \frac{IL2}{CD}$$

Stating the above variables we can now use this to get our state space equation in matrix form.

$$\dot{X}= \begin{bmatrix} \frac{dIL1}{dt} \\ \frac{dVc1}{dt} \\ \frac{dIL2}{dt} \\ \frac{dVc2}{dt} \\ \frac{dVsw}{dt} \\ \frac{dVcD}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C1} & 0 & 0 & 0 \\ 0 & \frac{1}{L2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{CD} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \\ \text{Vcsw} \\ \text{VcD} \end{bmatrix} + \begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{IN} \qquad (2.53)$$

From the above equations, we can extract our matrix values for A1, B1 which is given as;

$$A1=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C1} & 0 & 0 & 0 \\ 0 & \frac{1}{L2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC2} & 0 & 0 \\ 0 & 0 & \frac{1}{CD} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

While;

$$B1=\begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

For stage 2

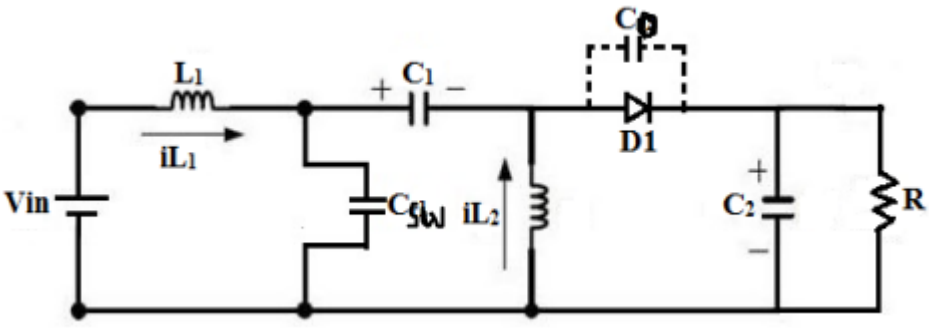

Figure 2.11: The new ZVS SEPIC converter when S1 off and D1 on

When the switch is off and diode D1 is ON we have the above circuit and the state space averaging equation is seen below;

$$\frac{dIL1}{dt} = \frac{VIN - Vsw}{L1}$$

$$\frac{dVc1}{dt} = -\frac{IL2}{C1}$$

$$\frac{dIL2}{dt} = -\frac{Vc1}{L2}$$

$$\frac{dVc2}{dt} = \frac{IL1+IL2}{C2} - \frac{Vc2}{RC2}$$

$$\frac{dVsw}{dt} = -\frac{IL2}{Csw}$$

$$\frac{dVcD}{dt} = 0$$

Knowing that we can now write the matrix form of our state space averaging equation as;

$$\dot{X}=\begin{bmatrix} \frac{dIL1}{dt} \\ \frac{dVc1}{dt} \\ \frac{dIL2}{dt} \\ \frac{dVc2}{dt} \\ \frac{dVsw}{dt} \\ \frac{dVcD}{dt} \end{bmatrix}=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C1} & 0 & 0 & 0 \\ 0 & \frac{-1}{L2} & 0 & 0 & 0 & 0 \\ \frac{1}{C2} & 0 & \frac{1}{C2} & \frac{-1}{RC2} & 0 & 0 \\ -\frac{1}{Csw} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \\ \text{Vcsw} \\ \text{VcD} \end{bmatrix}+\begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}\text{V}_{\text{IN}} \qquad (2.54)$$

So from this we can state the matrix of the state space variables A2 and B2 as;

$$\text{A2}=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C1} & 0 & 0 & 0 \\ 0 & \frac{-1}{L2} & 0 & 0 & 0 & 0 \\ \frac{1}{C2} & 0 & \frac{1}{C2} & \frac{-1}{RC2} & 0 & 0 \\ -\frac{1}{Csw} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

And,

$$\text{B2}=\begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Knowing our output Y= Cx+Eu we can represent C as;

C=[0 0 0 0 01]

So from the analysis this is gotten A_1, A_2, B_1, B_2, therefore $\dot{X}$ can be generally described below both on and off state as;

$$\dot{X}= \{A_1D+ A_2(1\text{-}D)\}\ x + \{B_1D+ B_2(1\text{-}D)\}\ V_{IN}$$

Substituting the matrix representation of the variables above into equation we can say this in matrix form is shown as;

$$\dot{X}= \{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C1} & 0 & 0 & 0 \\ 0 & \frac{1}{L2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC2} & 0 & 0 \\ 0 & 0 & \frac{1}{CD} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} D....$$

$$\ldots(1\text{-}D)\begin{bmatrix} IL1 \\ Vc1 \\ IL2 \\ Vc2 \\ \text{Vcsw} \\ \text{VcD} \end{bmatrix} + \begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \ldots \ldots \{D+ (1\text{-}D)\}\ V_{IN} \qquad (2.55)$$

2.3.1 Soft Switching Transition Techniques

For understanding the process of our proposed design we need to know what it means for our system to undergo soft switching procedure at the switch and how it helps improve our circuit in general. In a converter and at the switch when performing high frequency operation we could use a hard switching method which has the following limitations such as causing switching losses, stresses on the circuits components, electromagnetic interference which comes due to high change current and voltage with time and also energy losses across the system at inductors and capacitors. The solution to overcome this issue is by a soft switching technique at our switches. This can be done in two different methods namely the zero voltage switching (ZVS) which have been mentioned previously and the zero current switching (ZCS) method. When the switch goes through hard switching it experiences a waveform as seen below;

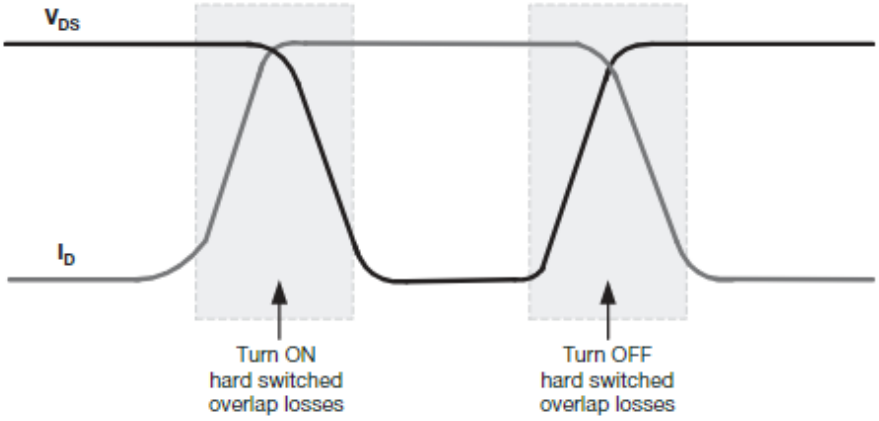

Figure 2.12: Expected waveform of hard switching at switch

and from the above diagram we can see that we experience losses both at turn on and turn off which affects the systems efficiency by reducing it. So applying soft switching techniques eliminates these losses either at turn on or turns off depending on the method introduced. We look at the two soft switching techniques that helps improve our system. But we only applied ZVS for improving our system. We would start by discussing what it means to achieve ZVS at the switch. The zero voltage switching (ZVS), here when this is applied to the switch the main aim is to bring the switch voltage to zero at turn on before applying the gate voltage which causes ideal and zero loss transition and reduced loss at turn off of the switch and we do this by applying a capacitor in parallel to the switch. The capacitor is used as a loss less snubber and this technique is what we used in our new proposed SEPIC converter in both switching devices. We can see these designs below.

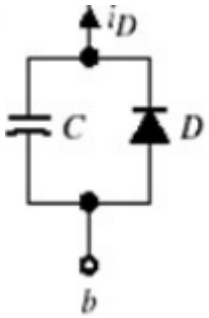

Figure 2.13: When ZVS is implemented at diode

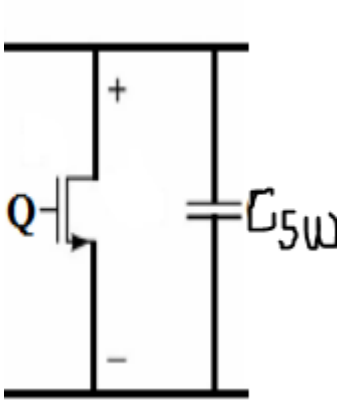

Figure 2.14: An Example of ZVS at MOSFET switch

When this is applied we get the following waveforms across the switch.

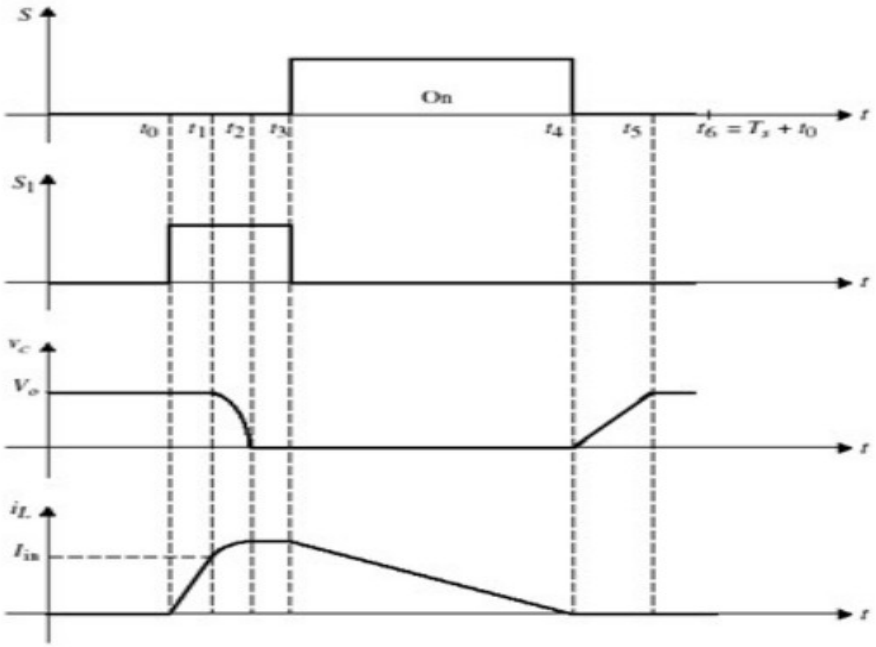

Figure 2.15: Waveforms of ZVS across the switch (a) Switch signal on and off time (b) PWM signal (c) Switch voltage waveform at on and off (d) Current waveform on and off

From the waveforms in figure 2.15 we can see that the switch voltage at turn on is zero so ZVS is achieved. Another method of achieving soft switching as stated earlier is by the zero current switching (ZCS) this we didn't use in our design and simulation but I would go ahead to explain it and show the waveforms for future purposes. Here the main idea as the name implies is to achieve a situation where the switch current or current passing through the switch goes to zero at turn off (not turn on like in the ZVS) before the gate voltage is removed (not applied as in the ZVS) creating an ideal and zero loss transition at turn on. We do this by applying an inductor in series with the switch to act as a loss less snubber causing a transition with lower losses this therefore increases the efficiency of the system. Below we see a diagram showing the setup of the ZCS when implemented.

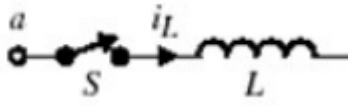

Figure 2.16: An example of the implementation of ZCS

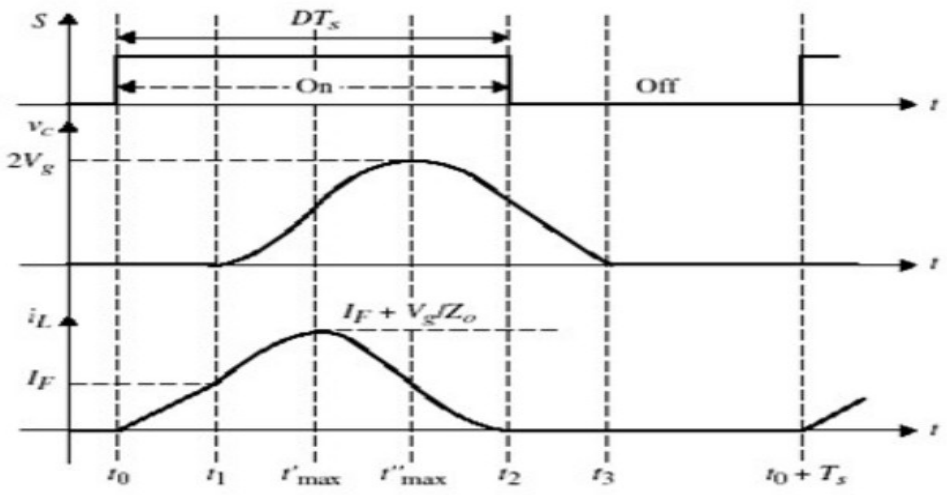

Figure 2.17: Waveforms of ZVS across the switch (a) Switch signal on and off time (b) Switch voltage waveform at on and off (c) Current waveform on and off

From the above wave form we can see that at the last wave form when the switch is about to come off the signal of the current is brought to zero before the gate voltage Vg is removed. Therefore, it achieves a zero current switching technique. The idea of both ZVS and ZCS is used for different types of switch, meaning when dealing with an IGBT type of switch it is best to use the zero current switching (ZCS) technique and for the MOSFET switch which we used here it more ideal to use a zero voltage switching (ZVS) technique as implemented in our proposed SEPIC circuit.

2.3.2 The Control Method Used For Closed Loop SEPIC Converter

First we need to understand what it means for a circuit to be in open loop and also what it means to be closed loop before we go further to talk about controlling the output of a circuit and the methods of doing so. When a circuit is said to be in an open loop state here we refer to it as just being plain in the sense that the output has no influence or control over the system. So irrespective of the output the system functions using the input and the process to give the result. Here the output is does not give a feedback to be compared to the input result and make changes that creates a desired output, the system is solely dependent on the input and process through which it goes through to give the output result. Below we see a block diagram of an open loop system.

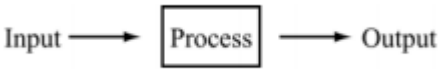

Figure 2.18: Block diagram example of an open loop system

So in terms of the SEPIC converter we have a clock diagram that looks like this

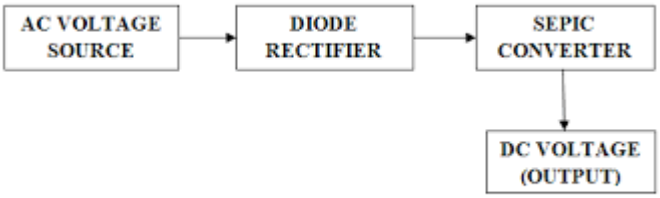

Figure 2.19: Block diagram of an open loop SEPIC converter with AC voltage source.

As we can see there is no presence of feedback or a controller to control the output of the system. So we can say our system above is an open loop state. Then just like the name sounds a closed loop system is the opposite of an open loop system. Here there is the presence of a feedback which is sent from the output and compared with the input to check for differences which is used in the control and adjustment of the system to provide a specific output at the system and this process continues till a specific output is achieved. In a closed loop system the function of the system is very dependent on the output result of the system. Below we see an example of a general block diagram system in closed loop.

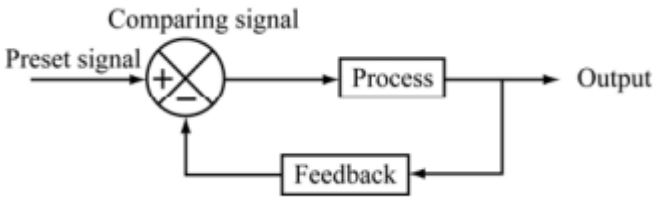

Figure 2.20: Block diagram example of a closed loop system

So for a closed loop SEPIC converter we have our block diagram looking like this below.

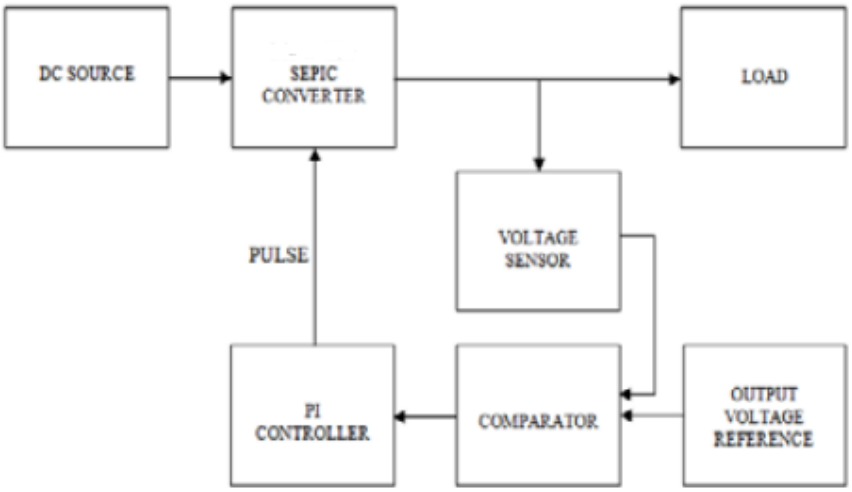

Figure 2.21: Block diagram of a closed loop SEPIC converter with DC voltage source.

We can see the presence of the feedback using a PI controller which we would explain as we proceed and also the voltage reference that is compared to the output voltage used for control through the PI controller. So moving on now we understand the idea of a closed and an open loop system we would now explain the controller, which we used in our system. When working in a closed loop system for the SEPIC converter we have to use a specific tuner for controlling the output results and increasing the efficiency of the system and this is known as a PI controller, which is derived from a PID control system without involving the derivative term of the controller.

2.3.3 PI Tuning For Controlling Output Value

The main objective of the controller tuning is to ensure the circuit achieves a desired output or achieves an output close to the mark set by using a reference even in case of rapid disturbances, changes, noise being introduced into the system, the circuit components changing rapidly and errors that arises at different times in a circuit. The controller helps by pass such obstacles in a system and this advantage is not present in an open loop system. We have three different modes under the PID controller from which the PI is gotten. Which are given as below,

P that stands for proportional, I standing for integral and lastly means derivative. In control tuning we should know that a single mode of tuning for example using just the P(proportional) or just the I(integral) aspect of the controller is barely ever used. It is mostly a combination of the modes to give the perfect control scheme for the desired output. For example, we can combine the P and I (PI) which we did for our SEPIC converter controlling or the P and D (PD) or using all three (PID) which is used most at times for controlling a circuit. Below we see a block diagram of a PID controller for starters.

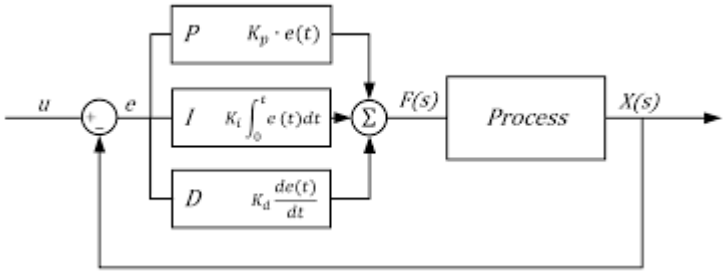

Figure 2.22: Block diagram of a PID controller

So going further I can say that generally a PID or PI controller continuously gets the value of error (e) by comparing a specific set reference value or constant set value to the already measured operation variable and calculating the difference between this two values which it uses in the correction or as a control function based on the various P, I or P, I and D terms depending on how it is being implemented. Looking deeply into each term we have;
First of the Proportional Term; this term explains that there is an output value gotten which is proportional to the current error value e in respect to time. Error value described as e(t). Hence we can describe this mathematically as the following equation as seen in the block diagram.

$$P_{out} \alpha e_{(t)}$$

Therefore making it;

$$P_{out} = Kp * e(t) \quad (2.56)$$

Where Kp is the proportional gain constant.

Secondly we have the Integral Term; this term describes that the output value produced is proportional to both the magnitude of error and the duration of error and mathematically it is described as;

$In_{out} \alpha \int_0^{-t} e(\tau) d\tau$

This can also be defined as the summation of instant errors over a given period of time showing a complete compilation of errors that ought to have been corrected. The equation becomes;

$$In_{out} = Ki * \int_0^{-t} e(\tau) d\tau \quad (2.57)$$

Having Ki defined as the integral gain constant.

Lastly we look at the derivative term even though it is not going to be used in our design, we have it explained as; this is the derivative of the error as the term name goes, which is solved by finding out the errors' slope over time and doing a product of its rate of change with time and the gain constant. It is mathematically represented as;

$$D_{out} = K_d * \frac{de(t)}{dt} \quad (2.58)$$

Where K_d is defined as the derivative gain or the magnitude of contribution by the derivative term to the whole controlling action of the controller.

For our design of the closed loop SEPIC converter we used the PI combination as we mentioned earlier and this combination causes forced oscillations to be removed and also the steady state errors to be eliminated. The speed response reduces as a disadvantage when the integral mode comes into play and the system at times becomes unstable because of the integral mode. The below block diagram is the actual controller used in the circuits closed loop design.

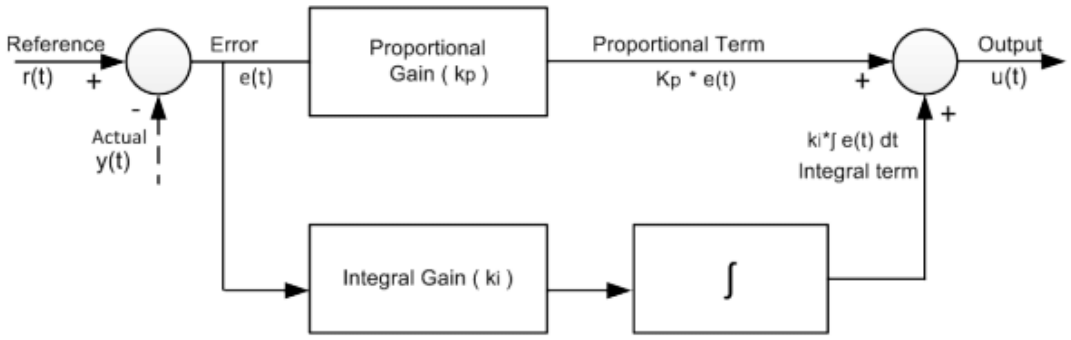

Figure 2.23: Block diagram of a PI controller

For tuning a PID or PI controller I would list different methods used but note that I did mine manually in the design of my circuit. So the different methods of tuning this controller are as follows; Ziegler-Nichols method, Ciancone and Marline Method, Cohen-Coon Method, FertickMethod , trial by error method and some few others also being used for the tuning of the controller depending on the desired output. For manually tuning the PI controller by the trial by error method which we used in our simulation and design, we have to do it gradually and it is straight forward. First we set Ki and Kd values as zero, then we start tuning the proportional term value until the system starts to display an oscillating behavior then we stop and then adjust the integral term value Ki next till the oscillation stops. Since we don't involve the derivative term we leave the Kd value as zero in our Simulink block parameter.

CHAPTER 3
DESIGN, SIMULATION AND RESULTS OF SEPIC CONVERTER

Now to come to the crucial chapter of the thesis where we would be designing both the basic SEPIC converter in open loop and closed loop also the bragged about new SEPIC converter that is more efficient than the basic SEPIC converter both in closed and open loop. Start definitely by naming and choosing the parameter values used for simulation and all of this was done using simple simulation software which called SIMULINK in MATLAB. You could also do it in any electronic simulation application don't get me wrong just used MATLAB because of being familiar with it. First as said earlier we would define the parameter or component values used for the simulation also so showing calculations used to get the values or ratings used when necessary. Arranging the simulations as follows, coming up first is the open loop basic SEPIC converter with no specific improvement made to it and showing its circuit diagram as designed in MATLAB then under it the various output results gotten from it all this when it is maintaining the output voltage that is no bucking or boosting of the voltage intended here. Next up showing what it means for this SEPIC converter to be stepping the voltage down by change of duty ratio or cycle and also when it acts stepping up the voltage at the output next also by change of duty cycle. Next going ahead after showing an open loop basic SEPIC converter working as buck and a boost converter, to show the closed loop also basic SEPIC converter when it maintains the voltage and the various output results under it. Then also would be to introduce the new SEPIC converter that achieves ZVS in open loop state which is also more efficient when comparing the open loop new SEPIC to the open loop basic SEPIC. Then, next is doing the same for the closed loop new SEPIC design. Lastly is to calculate the efficiency of all of them and show our comparison as follows;

Open loop basic SEPIC VS closed loop basic SEPIC.

Open loop basic SEPIC VS open loop new SEPIC.

Closed loop basic SEPIC VS closed loop new SEPIC.

The whole circuits should be designed and simulated in this chapter having the following assumptions, first the circuits operate in a continuous conduction mode (CCM), and there is low ripple across the capacitors and lastly involving a resistor in series with the input capacitor in all the simulations having a value of 0.008Ω. While the load used for all circuit designs is rated at 10Ω

3.1 Open Loop Basic SEPIC

In simulating, we have the specification values used in our circuit design and simulation.

Table 3.1: The specifications for open loop basic SEPIC

Name(s)	Values
Input Voltage (V_{IN})	12Volts
Output Ripple Current Rating	25-40% of I_L or Io in (Amps)
Output Ripple Voltage Rating	3% of V_L or Vo (Volts)
Duty Ratio or Cycle (D)	0.5 or 50%
Switching Frequency (fsw)	50Hz
Output Current I(o)	1.5 (Amps)

Having assumed the duty cycle to be 0.5 or 50% as seen in the table

Since the duty ratio is already selected there is no need to find it, but in a situation when it is not given the output voltage (Vo) would be given, so the calculation for getting the duty ratio is a as follows;

For a lossless circuit duty ratio is seen as;

$$D = \frac{Vo}{VIN + Vo} \tag{3.1}$$

But because of the parasitic elements which is introduced that causes losses across the whole circuit we would have to consider our voltage drop (Vd) across the circuit. This consideration makes the new duty ratio to be calculated as;

$$D = \frac{Vo + Vd}{VIN + Vo + Vd} \tag{3.2}$$

So from the above equation it can be said that the duty cycle would be at maximum value when input voltage is at minimum and vice versa in a condition where a range of input voltage values are given. So in such a case you have the VIN rated as between V_{INmax} - V_{INmin} i.e.: V_{IN} is $V_{INmin} \leq V_{IN} \geq V_{INmax}$the calculation for maximum and minimum duty cycle becomes;

$$Dmax = \frac{Vo+Vd}{VINmin+Vo+Vd} \quad (3.3)$$

And

$$Dmin = \frac{Vo+Vd}{VINmax+Vo+Vd} \quad (3.4)$$

Note as already stated in previous chapter that having a range of input voltage values given for a specific desired output to be achieved. The duty cycle will either be more than 50% when the input voltage is lower than the desired output voltage (step up) and would be less than 50% when the input voltage is less than the desired output voltage (step down). But now having the V_{IN} given and duty cycle also given, calculate the output voltage as follows;

Assuming a voltage drop of 0.7 volts, where;

VIN=12v, D=0.5 and Vd= 0.7v.

From $D = \frac{Vo+Vd}{VIN+Vo+Vd}$

Solving for Vo to get equation as below;

$$Vo = \frac{DVIN+DVd-Vd}{1-D} = \frac{0.5(12)+0.5(0.7)-0.7}{1-0.5} = 11.3v$$

Confirm this calculation from the simulation when the time comes. So the expected output waveform is 11.3v

When selecting thee component values use the following calculations as in next sub-chapter.

3.2 Parameters Value Selection

Here use specific calculations as mentioned in the previous chapters to find the values used when selecting the components needed for this simulation and it is shown below;

Inductor Selection

According to the table our peak to peak ripple current is going to be estimated as 40% of the maximum input current at VIN.

Therefore as seen in previous chapter the inductor ripple current is,

$\Delta I_{L1}=\Delta I_{L2}$

Where;

$L_1=L_2$ because the same values are used instead of a coupled inductor.

So the inductor ripple current (ΔI_L);

$$\Delta I_{L1}=\Delta I_{L2}=Iin * 40\% = Iout * \left(\frac{Vo}{VIN}\right) * 40\% = 1.5 * \left(\frac{11.3}{12}\right) * 40\% = 0.565A$$

With the above calculated you get the inductor value to be used in the simulation as;

$$L_1=L_2= \left(\frac{VIN}{\Delta IL1 * fsw} * D\right) = \left(\frac{12}{0.565 * 50k} * 0.5\right) = 212.4\mu H$$

Next do also calculate the inductor peak to peak current as;

$$I_{L1(peak)} = Iout * \frac{Vo+Vd}{VIN} * \left(1 + \frac{40\%}{2}\right) = 1.5 * \frac{11.3+0.7}{12} * 1.2 = 1.8A$$

$$I_{L2(peak)} = Iout * \left(1 + \frac{40\%}{2}\right) = 1.5 * 1.2 = 1.8A$$

Power Switch Selection

Here for the power switch use a MOSFET switch in the simulation. So the calculations used to determine the selection of the switch's rating is as follows;

Switch's peak current and it is calculated as;

$$I_{s1(peak)} \text{ or } I_{M1(peak)} = I_{L1(peak)} + I_{L2(peak)} = 1.8+1.8 = 3.6A$$

Root Mean Square (RMS) Current of Switch is;

$$I_{s1(RMS)} = Io \sqrt{\frac{(Vo+VIN) * Vo}{VIN^2}} = 1.5\sqrt{\frac{(11.3+12) * 11.3}{12^2}} = 2.03A$$

So the power dissipation at the switch is calculated using the formula below;

$$P_{s1} = I^2_{s1(RMS)} * Ron * D_{max} + (V_{IN}+V_o) * I_{s1(peak)} * \frac{(Sgd * fsw)}{Ig} \quad (3.6)$$

Where;

P_{s1} is the power dissipation or loss of switch

$I_{s1\ (RMS)}$ is the root mean square (RMS) current of switch

Ron is the on resistance of switch or resistance of switch at turn on

D_{max} is the maximum duty cycle

V_{IN} is the input voltage

V_O is the output voltage calculated

$I_{s1(peak)}$ is the Switch's peak ripple current

Sgdis the switch gate drain charge

f_{sw} is the switching frequency

Ig is the gate drive current

Take note that the power dissipation or loss at switch also includes the conduction and switching losses in it.

Diode Selection

Here put into consideration the minimum peak reverse voltage that the diode must control so as not to get damaged and its calculation is given as below;

$$V_{RD} = V_{IN(max)} + V_{O\ (max)} \quad (3.7)$$

Here Schottkydiode is mostly preferred because they reduce efficiency loss.

Output Capacitor Selection (C_2 or C_O)

When dealing with SEPIC converters you must know that, if switch is on, the energy is transferred from the capacitor to the inductor charging it and this causes large ripple currents. Therefore when selecting the capacitor you must consider one which can handle the maximum root mean square current $I_{(RMS)}$ which is calculated as;

$$I\ c_{(RMS)} = Io * \sqrt{\frac{Vo+Vd}{VIN(\min)}} \quad (3.8)$$

Also the equivalent series resistance (ESR) and the outputs bulk capacitance control the output ripple. Assuming a case where ESR contributes to half of the ripple and the remaining is caused by the capacitance amount. Saying that theVripple here is assumed to be 2% of the output voltage so the calculations for the two are as follows;

$$\text{ESR} \leq \frac{Vripple * 0.5}{\text{IL1(peak)} + \text{IL2(peak)}} = \frac{0.02 * 11.3 * 0.5}{3.6} = 0.031\Omega$$

And output capacitors capacitance is calculated as;

$$\text{Co} \geq \frac{Io * D}{Vripple * Vd * fsw} \geq \frac{1.5 * 0.5}{0.02 * 11.3 * 0.7 * 50k} \geq 0.0000948F = 94.8\mu F$$

Ceramic capacitors are recommended here in a case of an experiment being made.

Input Capacitor Selection

When selecting this capacitor know that thanks to the inductor there is a low ripple current, so use the RMS current for selection here which is calculated as;

$$I_{CIN(RMS)} = \frac{\Delta IL}{\sqrt{12}} = \frac{1.8}{\sqrt{12}} = 0.52A$$

But in the simulation, selected is a capacitor with value of $C_{IN} \geq 10\mu F$ to prevent impedance interactions with the input supply.

Coupling Capacitor Cs Selection

This is selected based on the RMS current which is calculated as;

$$I_{Cs(RMS)} = Io\sqrt{\frac{Vo + Vd}{VIN(\min)}} \qquad (3.9)$$

Also the rating of the coupling capacitor must be having a large RMS current relative to output power. Here the voltage rating of Cs > maximum input Voltage when a range of input is given and Cs is set as 10μF.

The peak to peak ripple voltage on Cs can be calculated as;

$$\Delta V\ cs = \frac{Io * Dmax}{Cs * fsw} = \frac{1.5 * 0.5}{10\mu * 50k} = 1.5v$$

So having calculated and selected the parameters make a new table so it is easier to understand.

Table 3.2: Full component values for open loop basic SEPIC

Name(s)	Values
Input Voltage (V_{IN})	12Volts
Output Ripple Current Rating	25-40% of I_L or Io in (Amps)
Output Ripple Voltage Rating	3% of V_L or Vo (Volts)
Duty Ratio or Cycle (D)	0.5 or 50%
Switching Frequency (fsw)	50Hz
Output Current I(o)	1.5 (Amps)
Coupling Capacitor (Cs)	10µF
Input Capacitor (C_{IN})	10 µF
Output Capacitor (Co)	94.8 µF
Inductors (L_1& L_2)	212.4 µH

Now below, shown is the circuit diagram as designed in MATLAB Simulink and output results of the circuit.

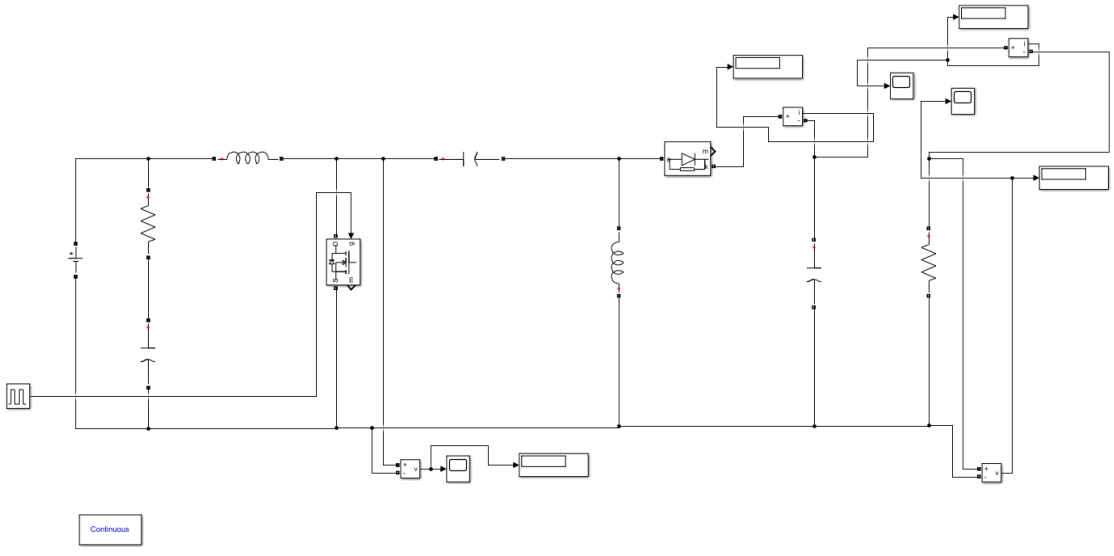

Figure3.1: Open loopbasic SEPIC converter

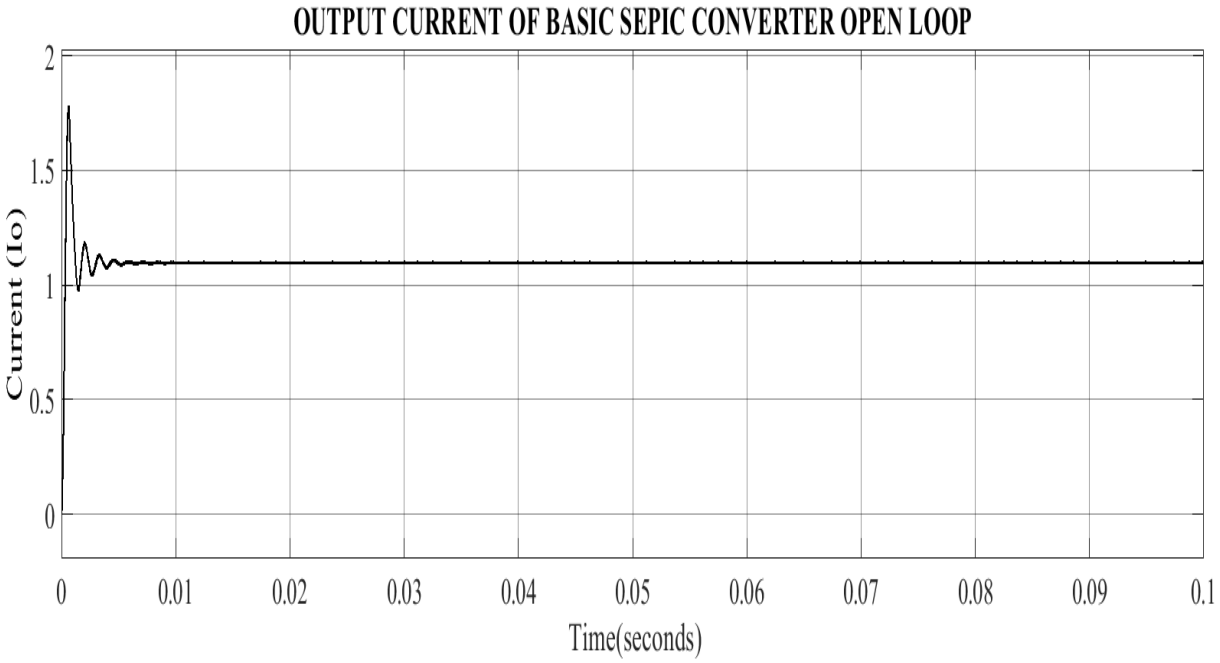

Figure 3.2: Output current of Basic SEPIC for 12V

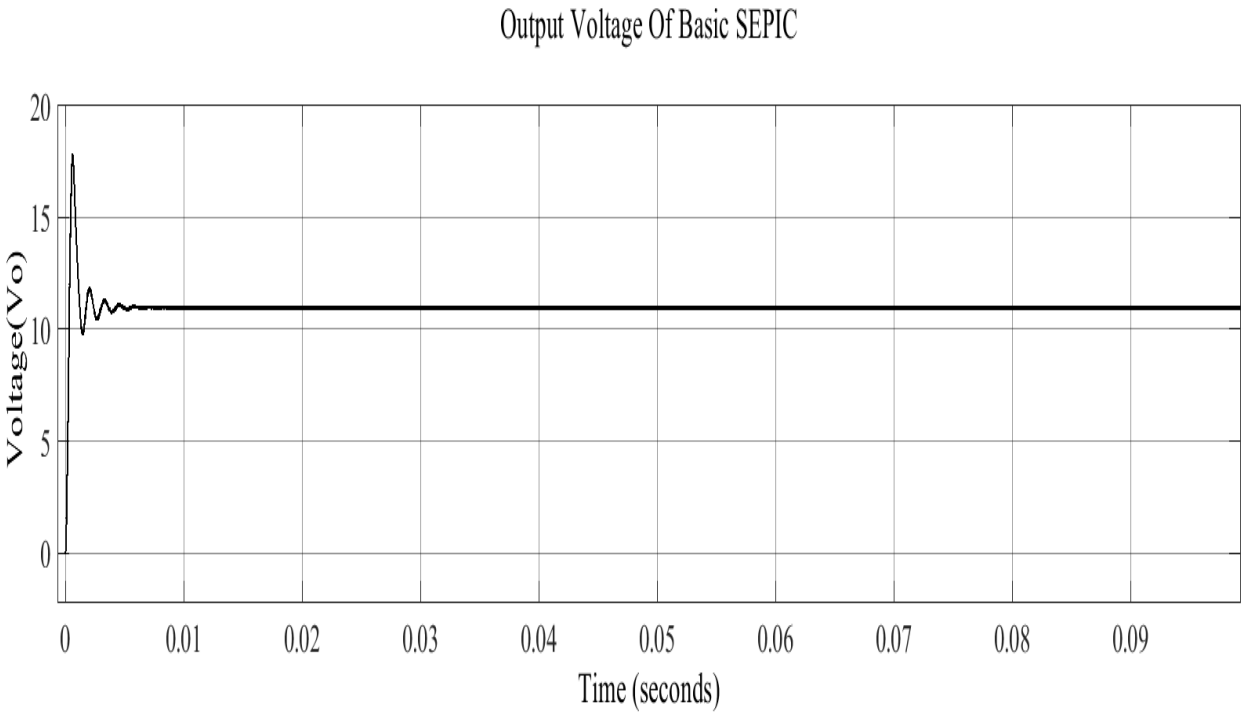

Figure 3.3: Output voltage of basic SEPIC converter for 12Volts

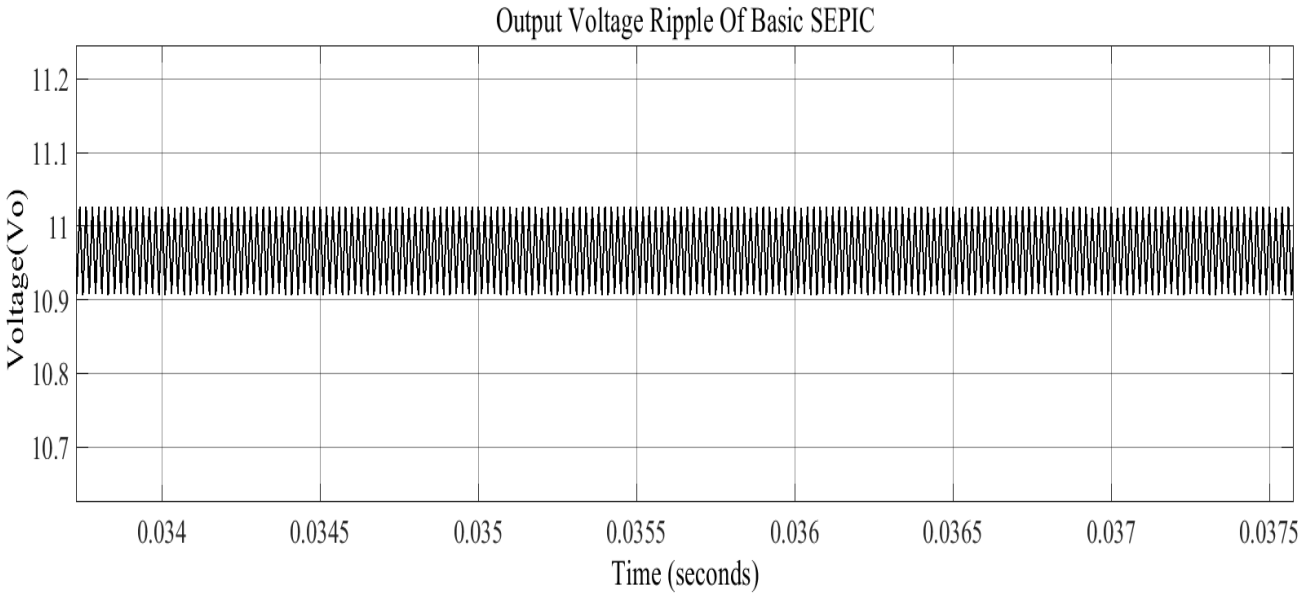

Figure 3.4: Output voltage ripple of basic SEPIC for 12Volts

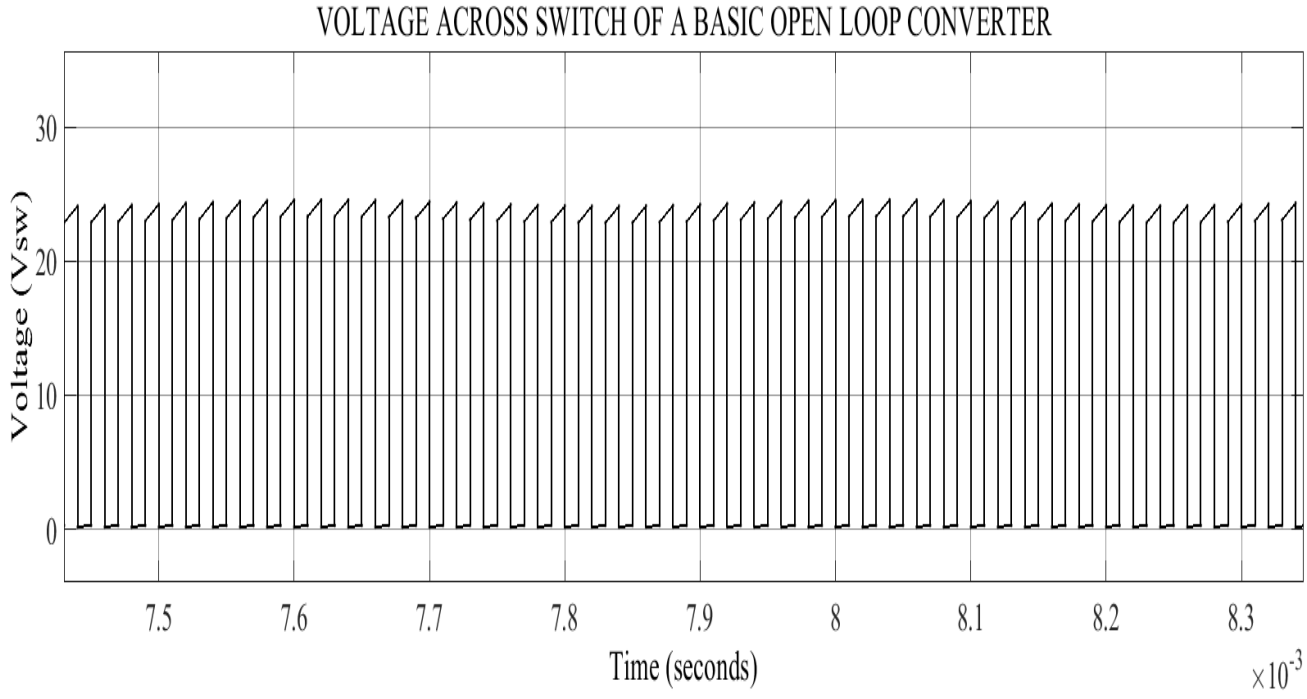

Figure 3.5: Switch voltageof basic SEPIC converter showing (no ZVS) for 12volt Vin

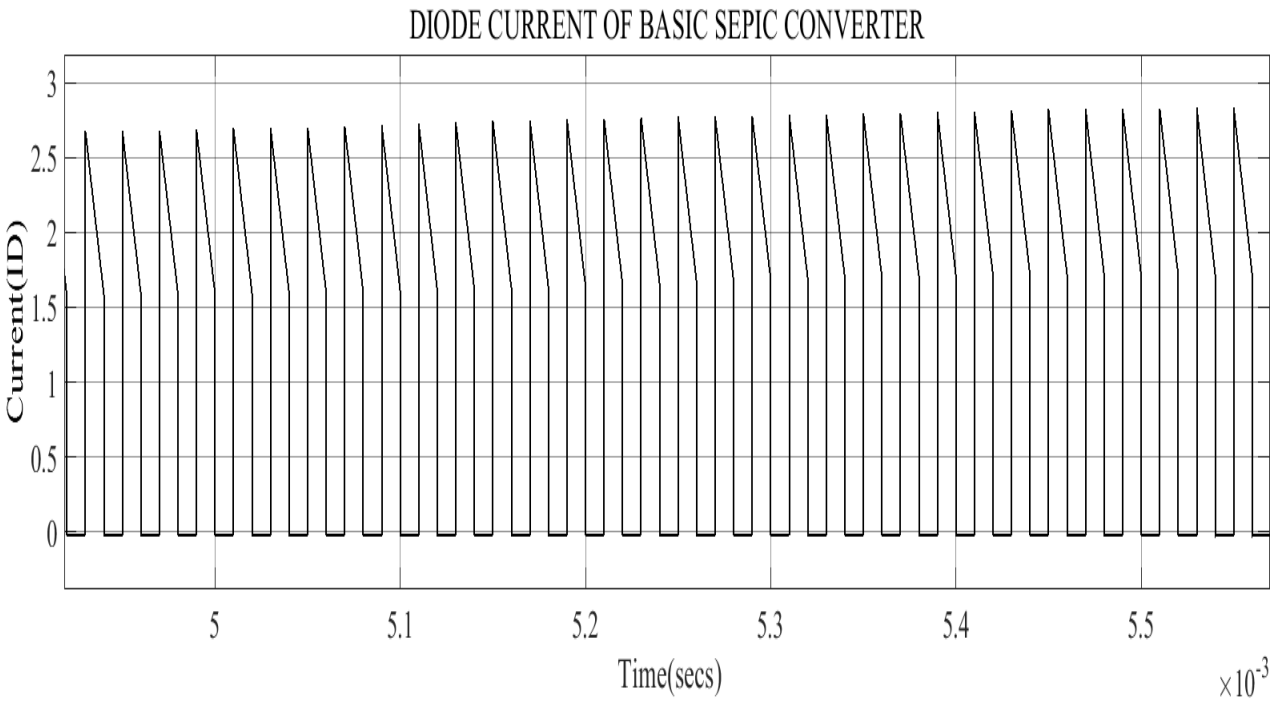

Figure 3.6: Diode current of basic SEPIC converter for 12volt Vin

From the figure above you can see that in the wave form for output voltage there is an overshoot at start of the simulation when the switch comes on and then it drops to a steady state after oscillating for a while and the voltage value is less than the 12v which is the input voltage showing a drop in volts of almost 0.9v so the output voltage goes between the ranges of 11.01v and 11.19v. Also from the voltage at the switch you can see that it also never goes to exactly zero throughout the simulation meaning ZVS is not achieved here at switch's turn on. Also the voltage level as switch from the wave form shows a voltage of 22v to 24 ranges confirming the equations below.

$V_{S1} < 2V_{IN}$ (buck)

$V_{S1} > 2V_{IN}$ (boost)

$V_{S1} = 2V_{IN}$ (maintaining)

3.3 Closed Loop Basic SEPIC

Below you see the design for the closed loop basic SEPIC with a controller being introduced into the system and the set reference voltage is 12v same as the input voltage. Using a PI controller and also putting a table below for easy understanding.

Table 3.3: Values for closed loop basic SEPIC

Name(s)	Values
Input Voltage (V_{IN})	12Volts
Output Ripple Current Rating	25-40% of I_L or Io in (Amps)
Output Ripple Voltage Rating	3% of V_L or Vo (Volts)
Duty Ratio or Cycle (D)	0.5 or 50%
Switching Frequency (fsw)	50Hz
Output Current I(o)	1.5 (Amps)
Coupling Capacitor (Cs)	10µF
Input Capacitor (C_{IN})	10 µF
Output Capacitor (Co)	94.8 µF
Inductors (L_1& L_2)	212.4 µH
Proportional Term (Kp)	1
Integral Term (Ki)	1

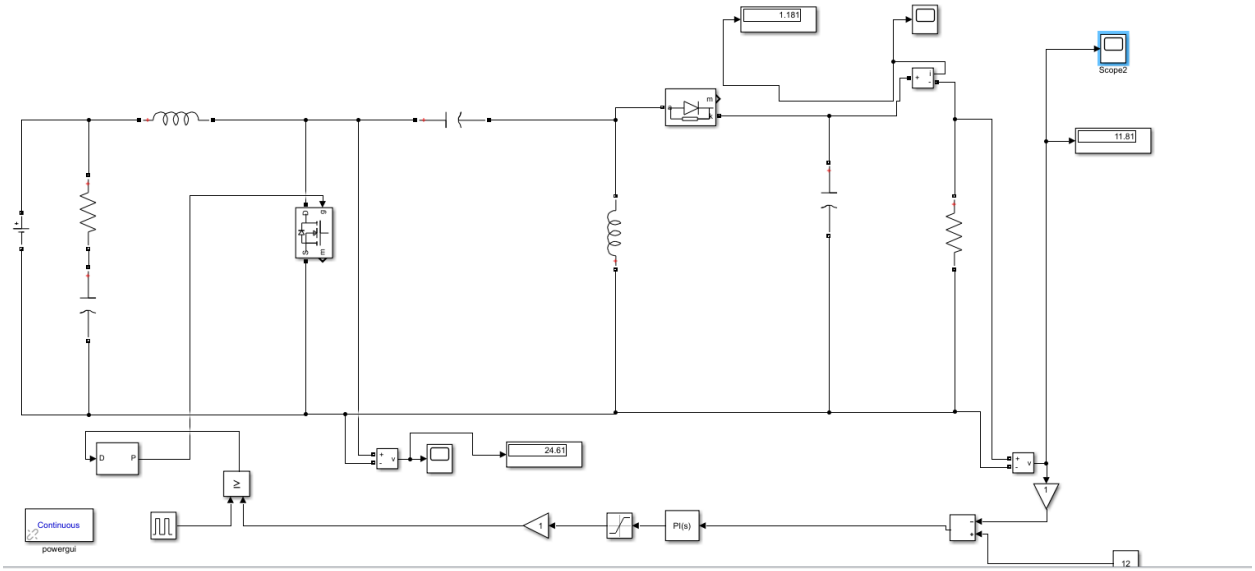

Figure 3.7: Closed loop basic SEPIC converter

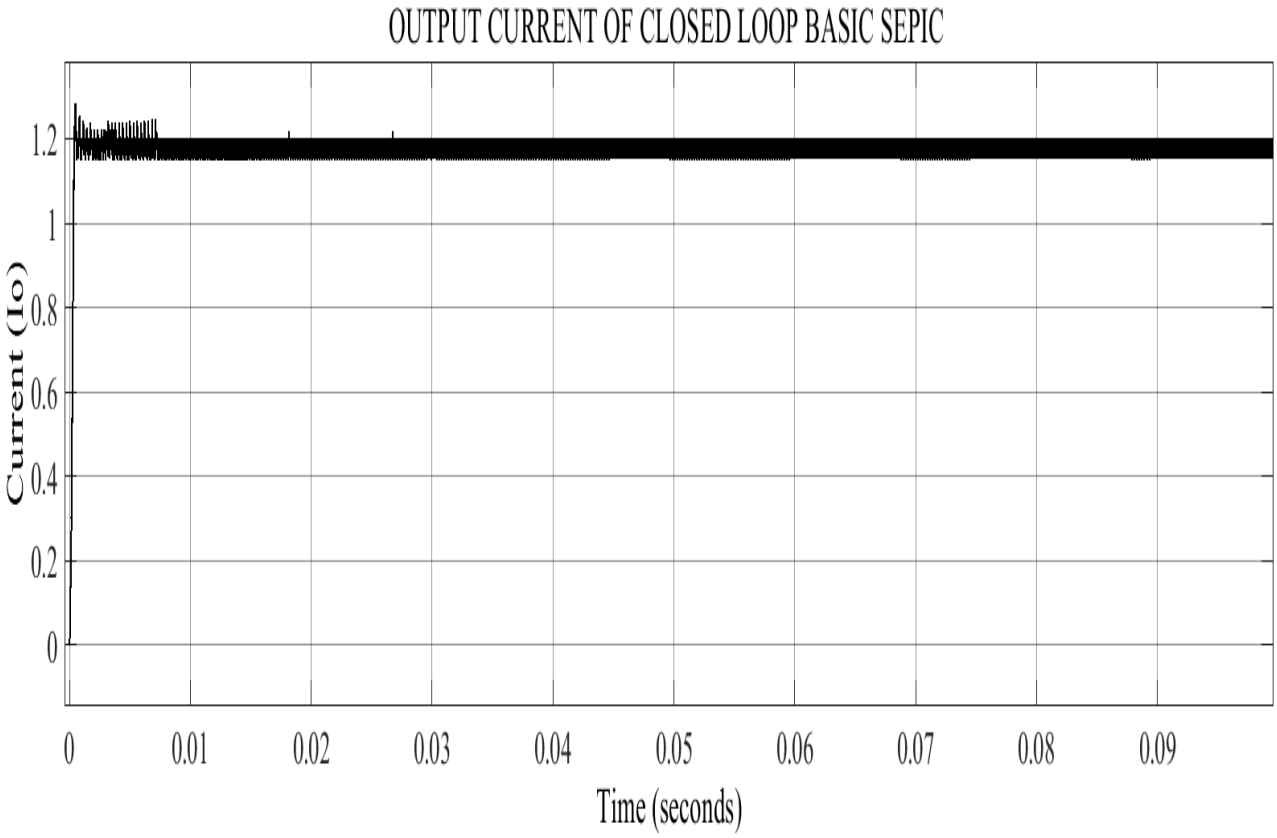

Figure 3.8: Output current of closed loop basic SEPIC converter at 12volts(Vin)

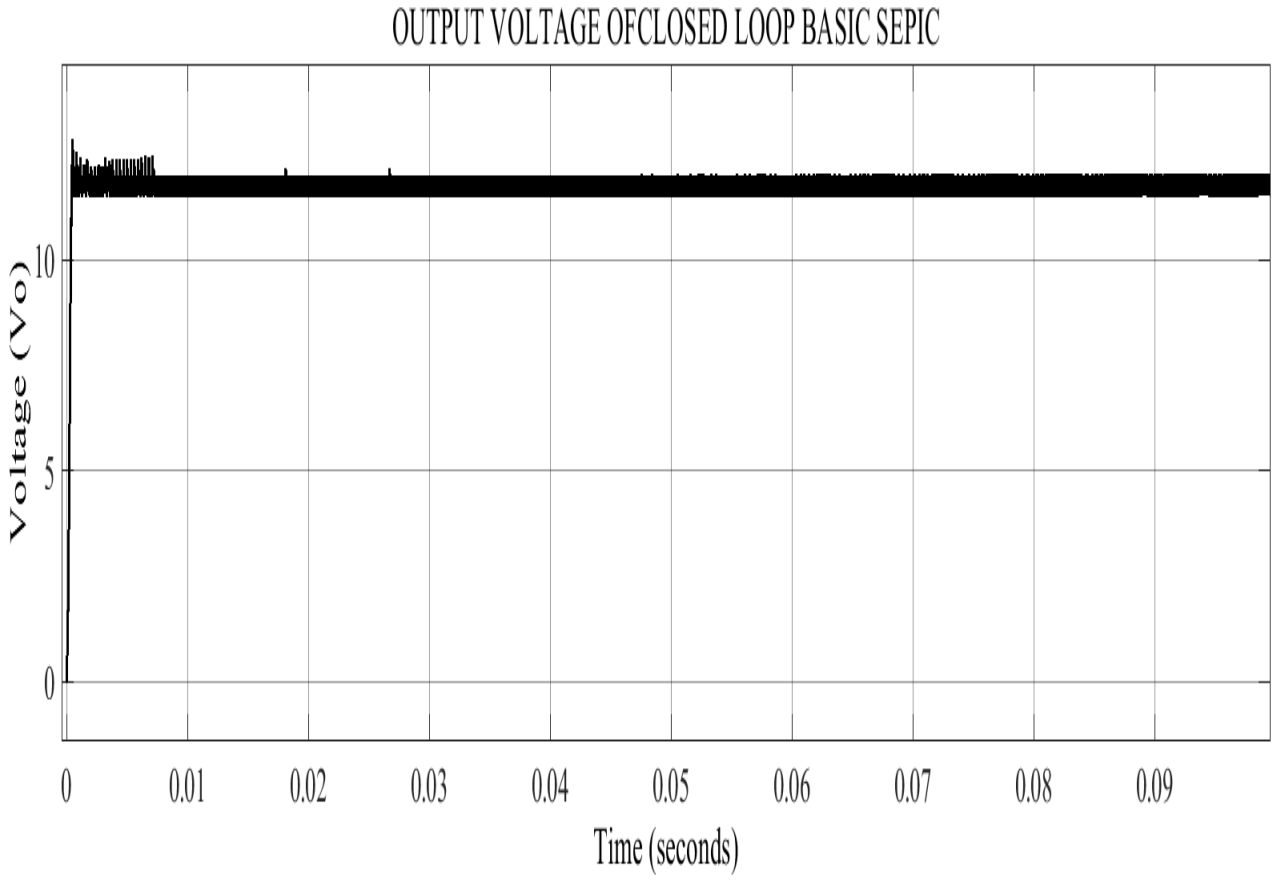

Figure 3.9: Output voltage of closed loop basic SEPIC converter at 12volts(Vin)

Here see the output current and voltage waveforms. Unlike the open loop system of the basic SEPIC it can be seen that the waveform rises slowly with time till it achieves steady state and the output voltage range from the circuit borders between 11.6v and 12v at steady state clearly showing more efficiency and a better circuit because there is a little overshoot present when it reaches steady state in comparison with the basic SEPIC in open loop form. So it can be said that it has been properly controlled.

3.4 New SEPIC

Here introducing two new capacitors in parallel to the diode and switch, and to you calculate the new capacitors to know the capacitance value that is going to be used. The calculation is given as shown below and notes that it involves the inductor which resonates with it when calculating the capacitors value.

$$L_1 = \frac{1}{16\pi^2 * fsw^2 * Csw} \quad (3.10)$$

$$L_2 = \frac{1}{16\pi^2 * fsw^2 * CD} \quad (3.11)$$

This equation changes since it looks for C_D and Csw, to become;

$$Csw = \frac{1}{16\pi^2 * fsw^2 * L1} = \frac{1}{16\pi^2 * 50k^2 * 212.4\mu} = 0.0.012\mu F$$

$$Csw = C_D$$

Now a new table for the new SEPIC circuit is introduced.

Table 3.4: Values for new SEPIC converter design and simulation

Name(s)	Values
Input Voltage (V_{IN})	12Volts
Output Ripple Current Rating	25-40% of I_L or Io in (Amps)
Output Ripple Voltage Rating	3% of V_L or Vo (Volts)
Duty Ratio or Cycle (D)	0.5 or 50%
Switching Frequency (fsw)	50Hz
Output Current I(o)	1.5 (Amps)
Coupling Capacitor (Cs)	10µF
Input Capacitor (C_{IN})	10 µF
Output Capacitor (Co)	94.8 µF
Inductors (L_1& L_2)	212.4 µH
Resonant Capacitors (Csw&C_D)	0.012µF

Open Loop New SEPIC Converter

Having calculated all the necessary values for this simulation, shown below is the new proposed SEPIC converter design as done in Simulink.

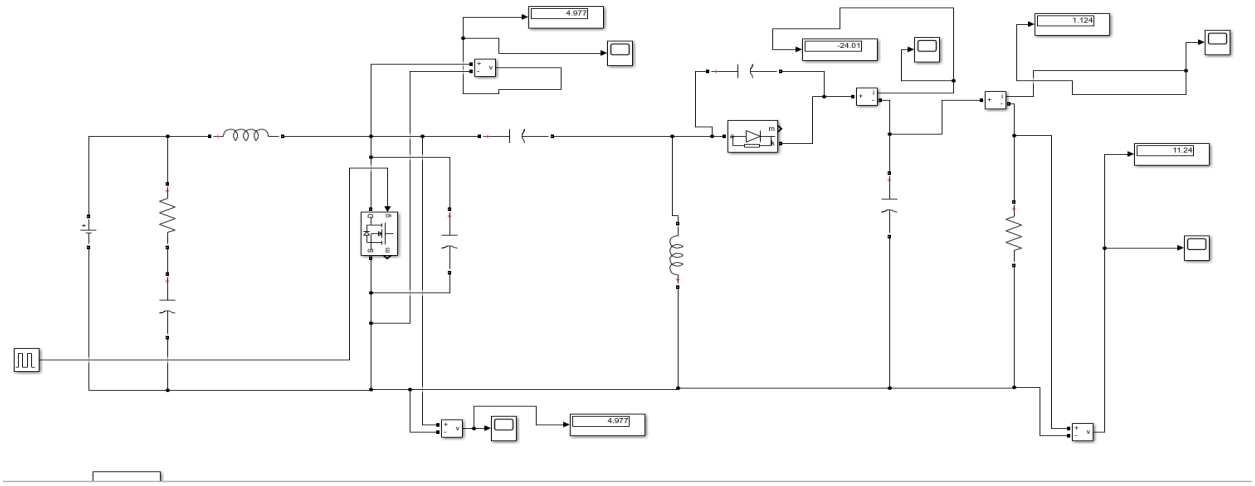

Figure 3.10: New SEPIC open loop converter

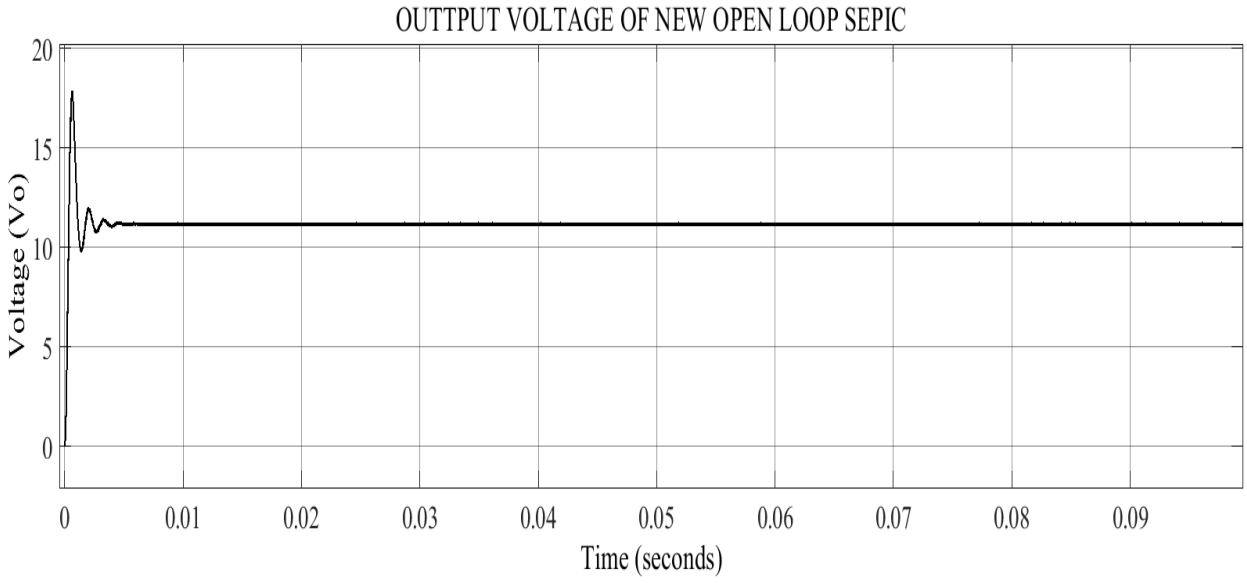

Figure 3.11: The Output voltage of new SEPIC open loop converter for 12volts (Vin)

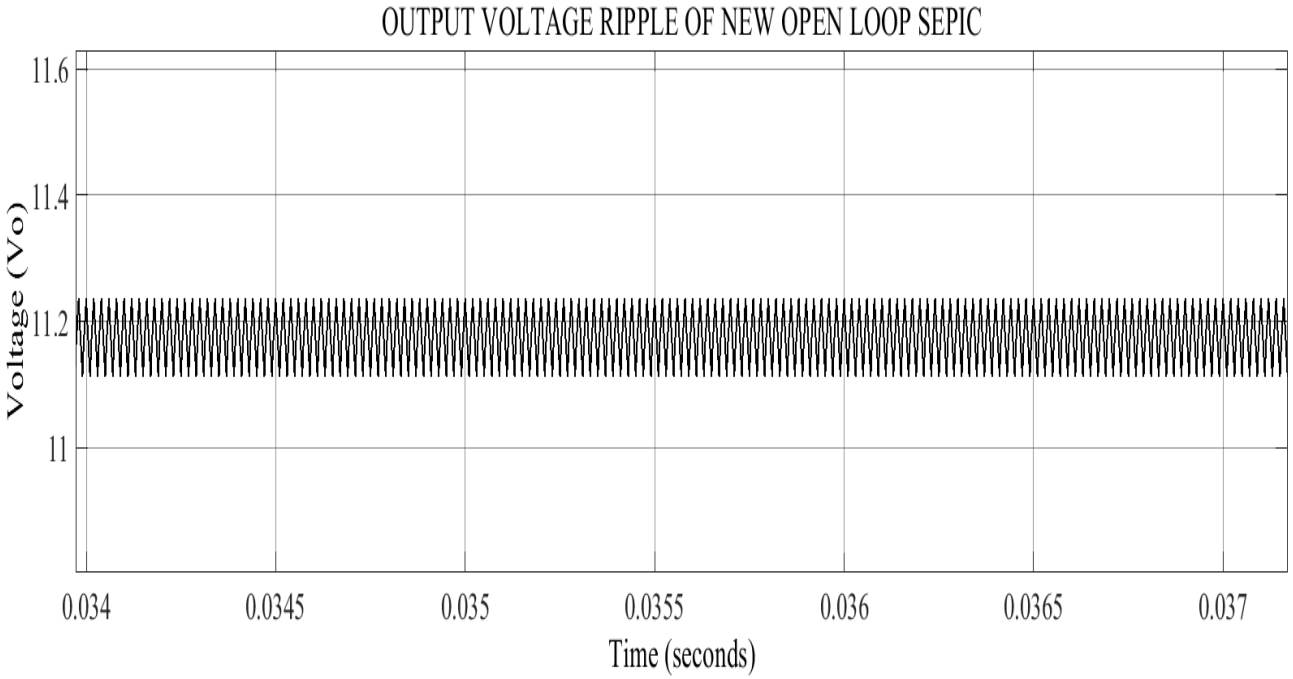

Figure 3.12: Output ripple voltage new SEPIC open loop converter for 12volts (Vin)

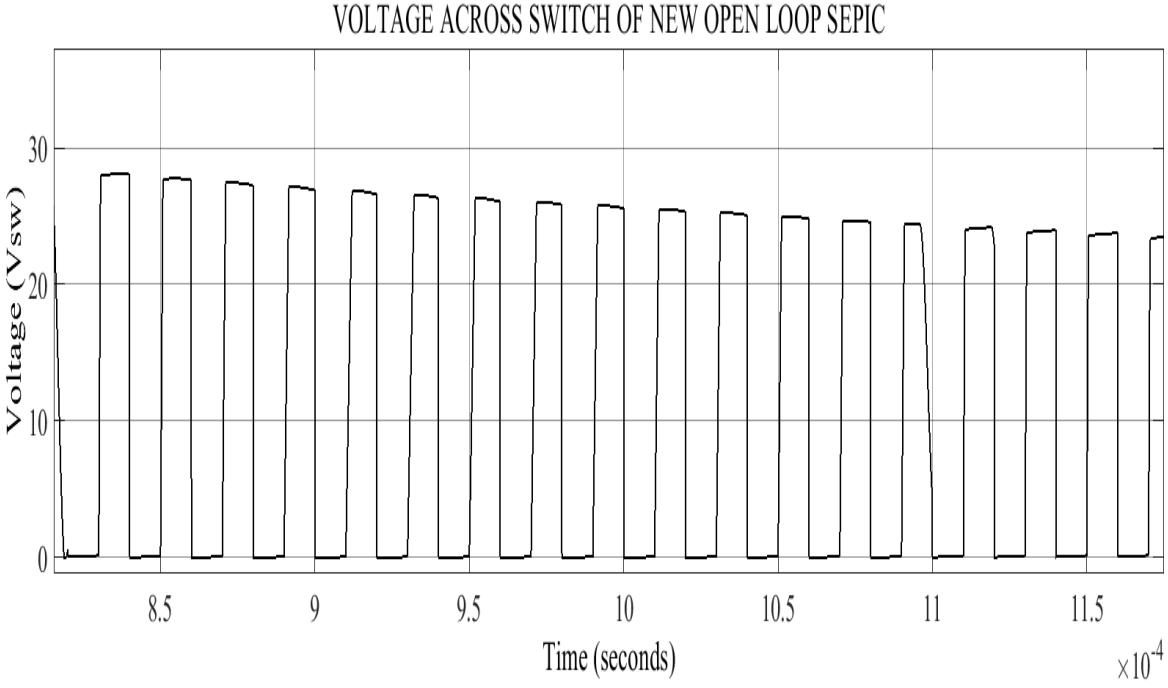

Figure 3.13: Voltage across switch showing ZVS new SEPIC open loopconverter for 12v

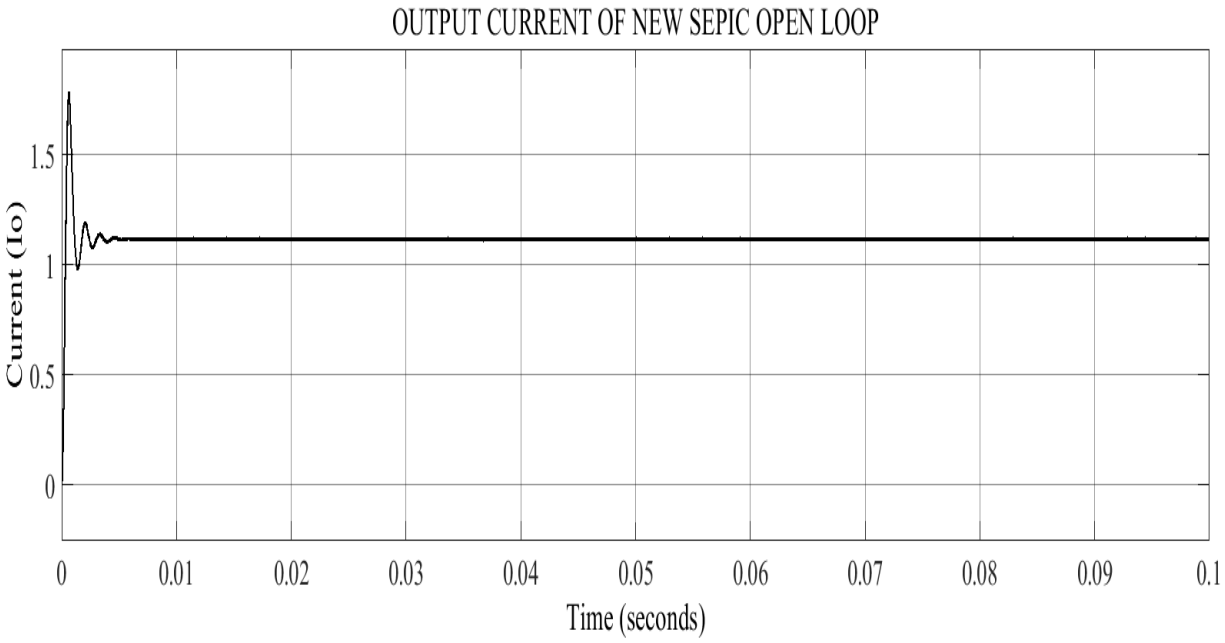

Figure 3.14: Output currentnew SEPIC open loop converter for 12volts (Vin)

From the figures above you can see that first in comparison with the previous simulated open loop basic SEPIC converter from the output voltages you can see that there is a reduction in time in which this system goes to steady state. In this new open loop proposed SEPIC converter the output voltage achieves steady state faster. From the waveform of the voltage across the MOSFET switch you can also see that ZVS condition is achieved at turn on of the switch, in the output voltage ripple waveform you can see when compared to that of an open loop basic converter you have less voltage ripple and most of all the range of voltage at the output increases to 11.20v to 11.30v so there is an increase in efficiency.

3.5 New Closed Loop SEPIC Converter

Now moving on to do the same here but not adding new tables because it's the same parameters value that is used as the new open loop SEPIC. So below is the MATLAB design and the various outputs gotten.

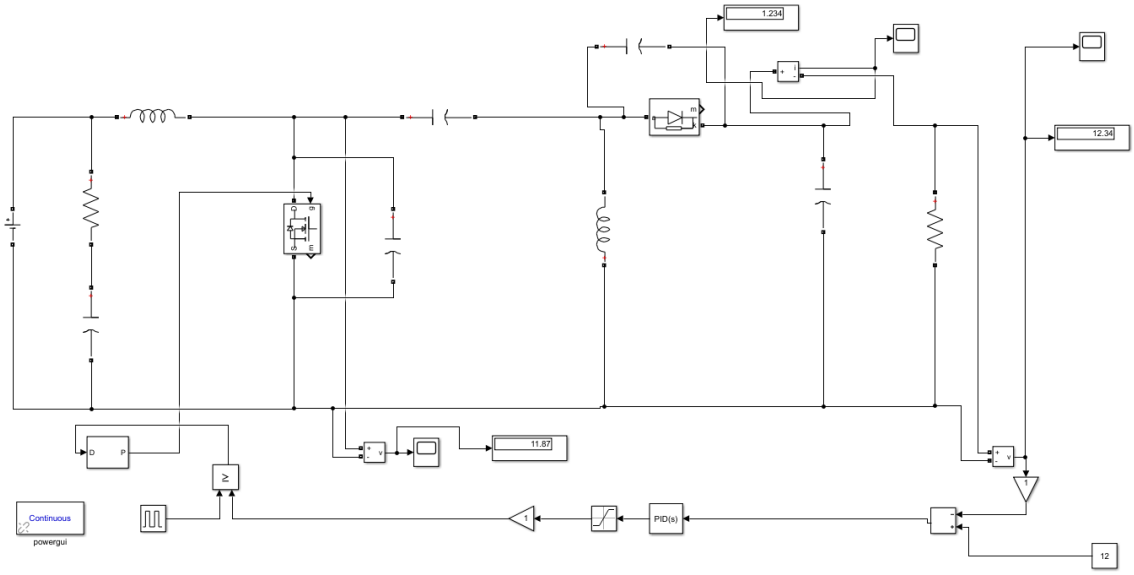

Figure 3.15: New closed loop SEPIC converter

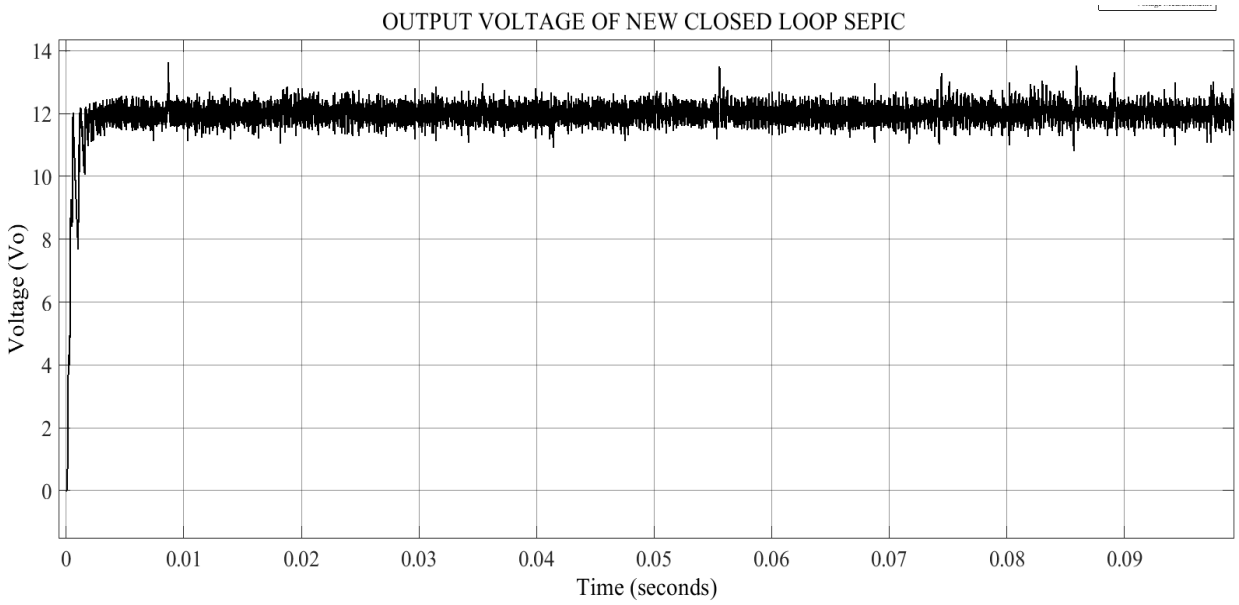

Figure 3.16: Output voltage of new closed loop SEPIC converter for 12Volts (Vin)

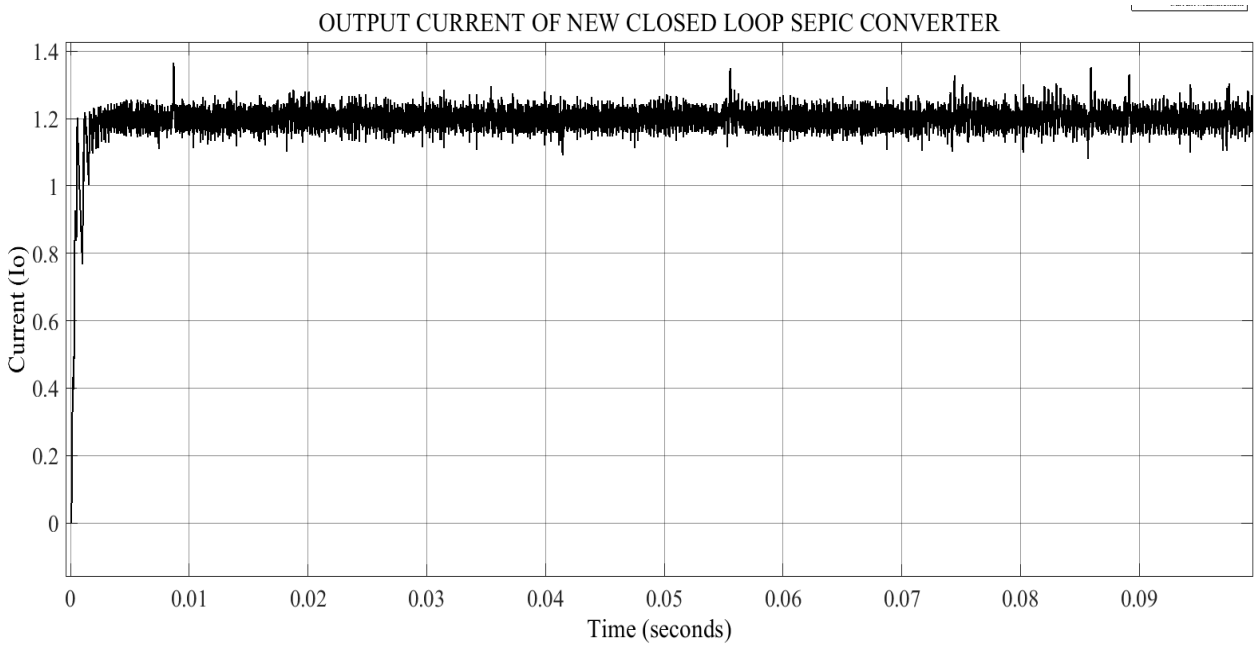

Figure 3.17: Output current of new closed loop SEPIC converter for 12Volts (Vin)

Similarly to the above there is the output voltage and current showing a higher efficiency when compared to the basic SEPIC converter in the closed loop stage a higher output voltage range of 11.8v to 12.1v at steady state and unlike the closed loop basic SEPIC converter there is no overshoot when it gradually increases with time to achieve steady state. Note the P and I terms are maintained as same in the closed loop basic SEPIC.

3.6 An Open Loop Basic SEPIC Converter as a Buck-Boost Converter

Here still using the same table as the first open loop basic SEPIC with every parameter value being the same apart from the duty cycle.

As A Buck Converter;

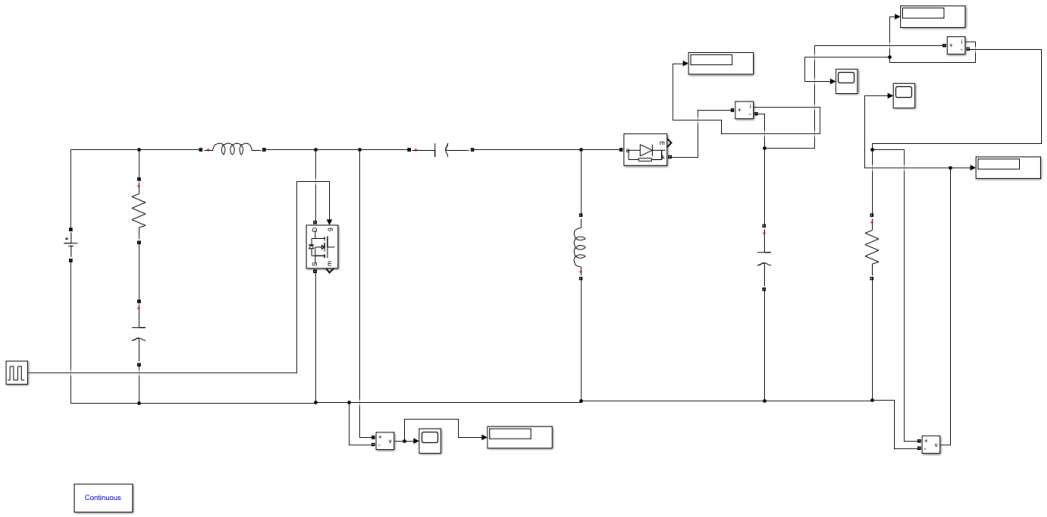

Figure 3.18: New SEPIC open loop converter as buck converter

Table 3.5: Component values of SEPIC open loop as a buck converter

Name(s)	Values
Input Voltage (V_{IN})	12Volts
Output Ripple Current Rating	25-40% of I_L or Io in (Amps)
Output Ripple Voltage Rating	3% of V_L or Vo (Volts)
Duty Ratio or Cycle (D)	0.3 or 30%
Switching Frequency (fsw)	50Hz
Output Current I(o)	1.5 (Amps)
Coupling Capacitor (Cs)	10µF
Input Capacitor (C_{IN})	10 µF
Output Capacitor (Co)	94.8 µF
Inductors (L_1& L_2)	212.4 µH

By reducing our duty cycle to 0.3 to check the SEPIC output values and waveforms to show it working as a step down converter

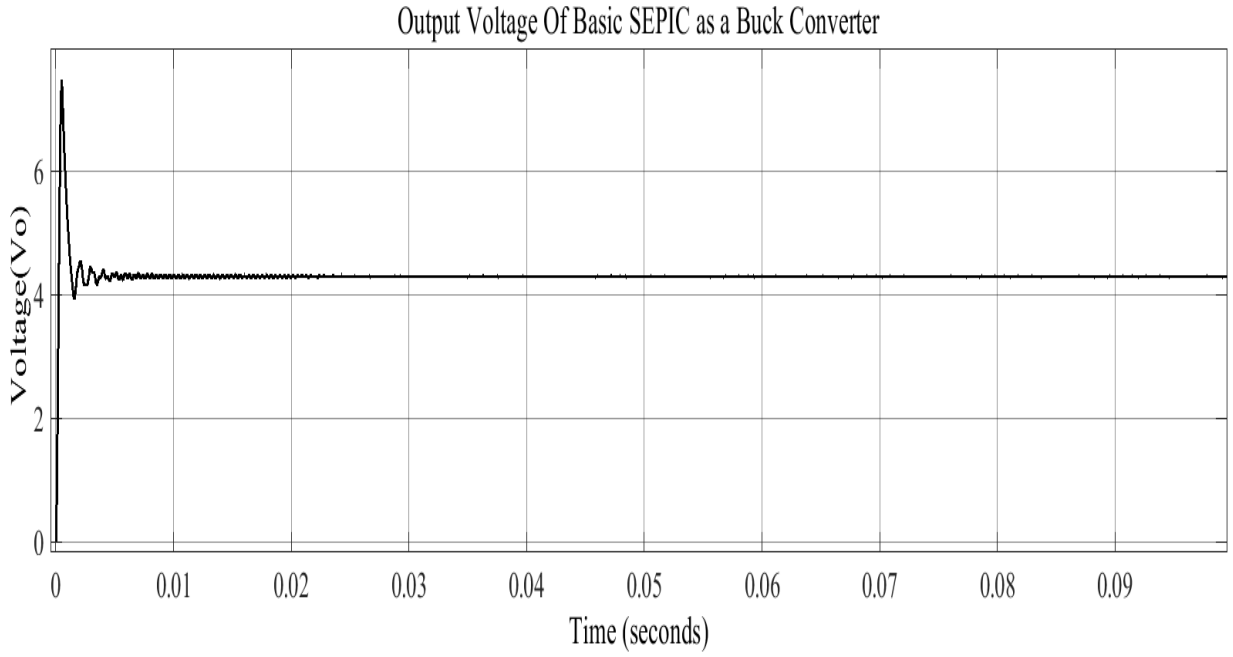

Figure 3.19: Output voltage of basic SEPIC as a buck converter for 12Volts (Vin)

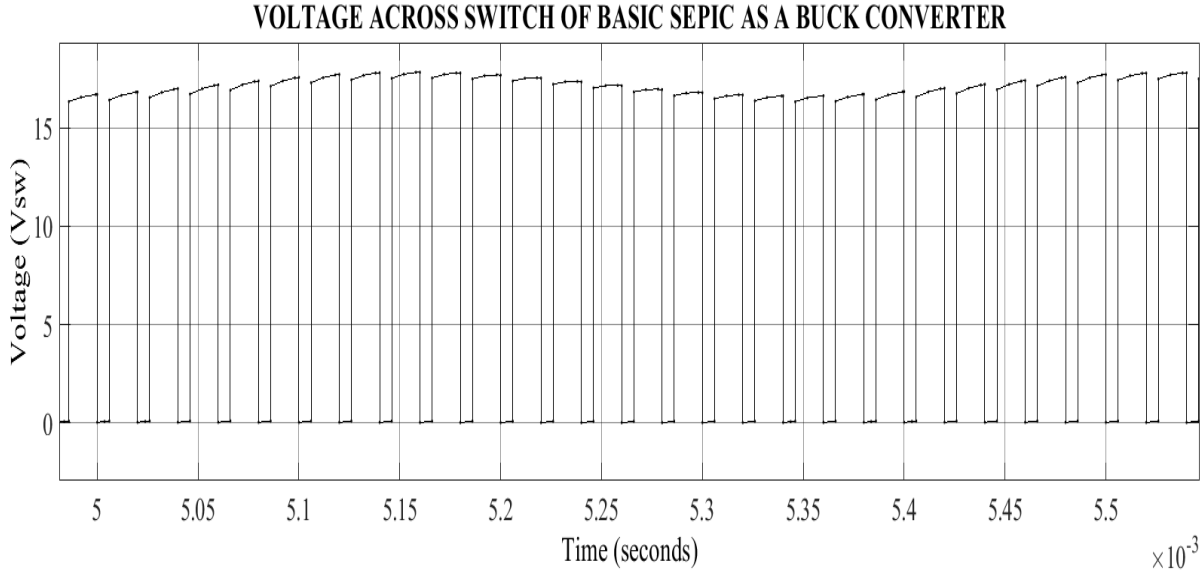

Figure 3.20: Voltage across switch of basic SEPIC as a buck converter for 12Volts (Vin)

So from our above waveforms it shows that when the duty cycle is reduced to 0.3 or anything less than 0.5 the circuit steps down the input voltage at output to about 4.2v and the switch wave form confirms our equation below.

$V_{S1} < 2V_{IN}$ (buck)

16.8v < 24V (step down)

As A Boost Converter

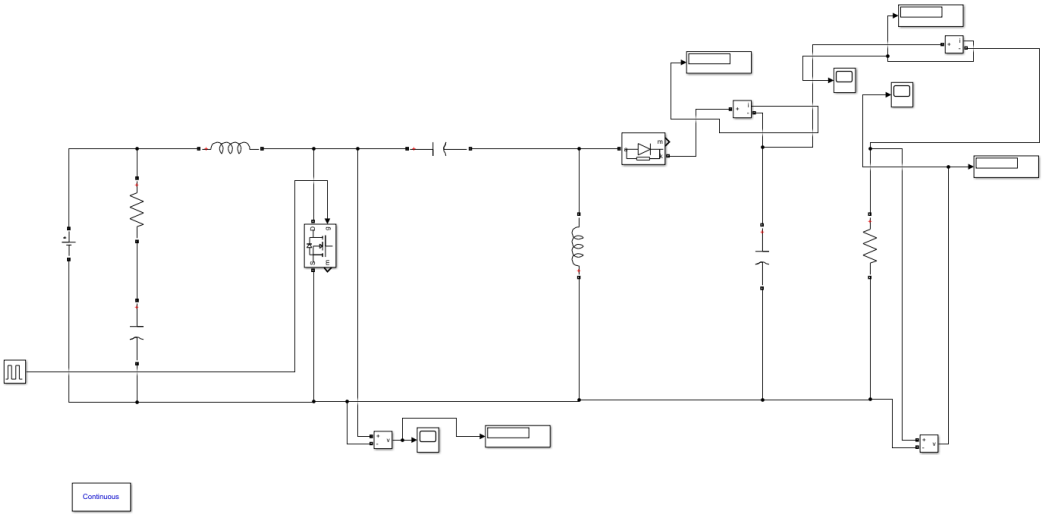

Figure 3.21: New SEPIC Open Loop Converter As Buck Converter

Table 3.6: Component values of SEPIC open loop as a buck converter

Name(s)	Values
Input Voltage (V_{IN})	12Volts
Output Ripple Current Rating	25-40% of I_L or Io in (Amps)
Output Ripple Voltage Rating	3% of V_L or Vo (Volts)
Duty Ratio or Cycle (D)	0.8 or 80%
Switching Frequency (fsw)	50Hz
Output Current I(o)	1.5 (Amps)
Coupling Capacitor (Cs)	10µF
Input Capacitor (C_{IN})	10 µF
Output Capacitor (Co)	94.8 µF
Inductors (L_1& L_2)	212.4 µH

By reducing the duty cycle to 0.8 you can see check the SEPIC output waveforms to show it working as a step up converter

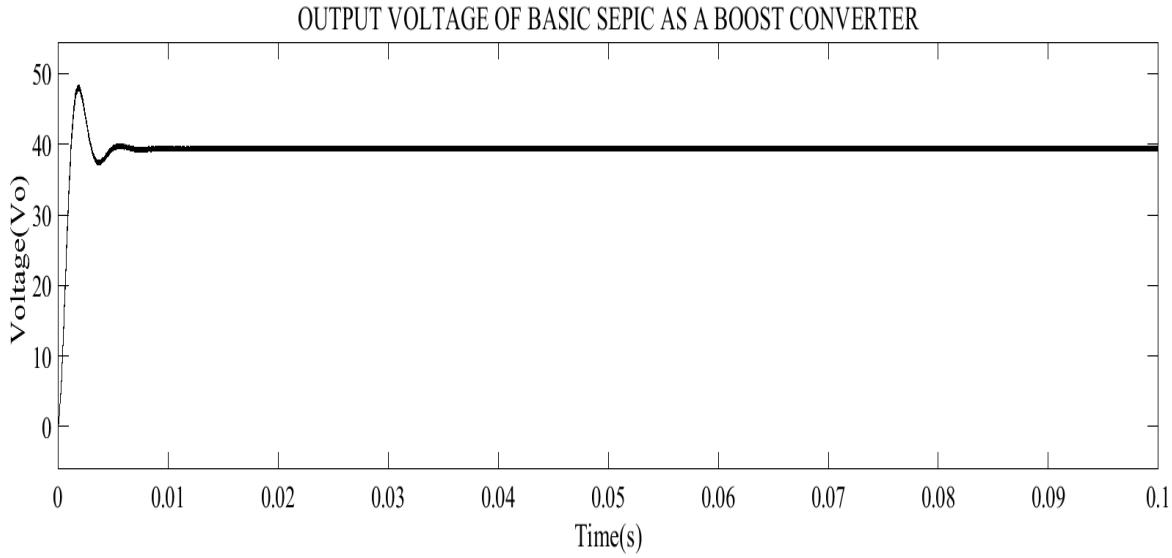

Figure 3.22: Output voltage of basic SEPIC showing step up of voltage for 12Volts (Vin)

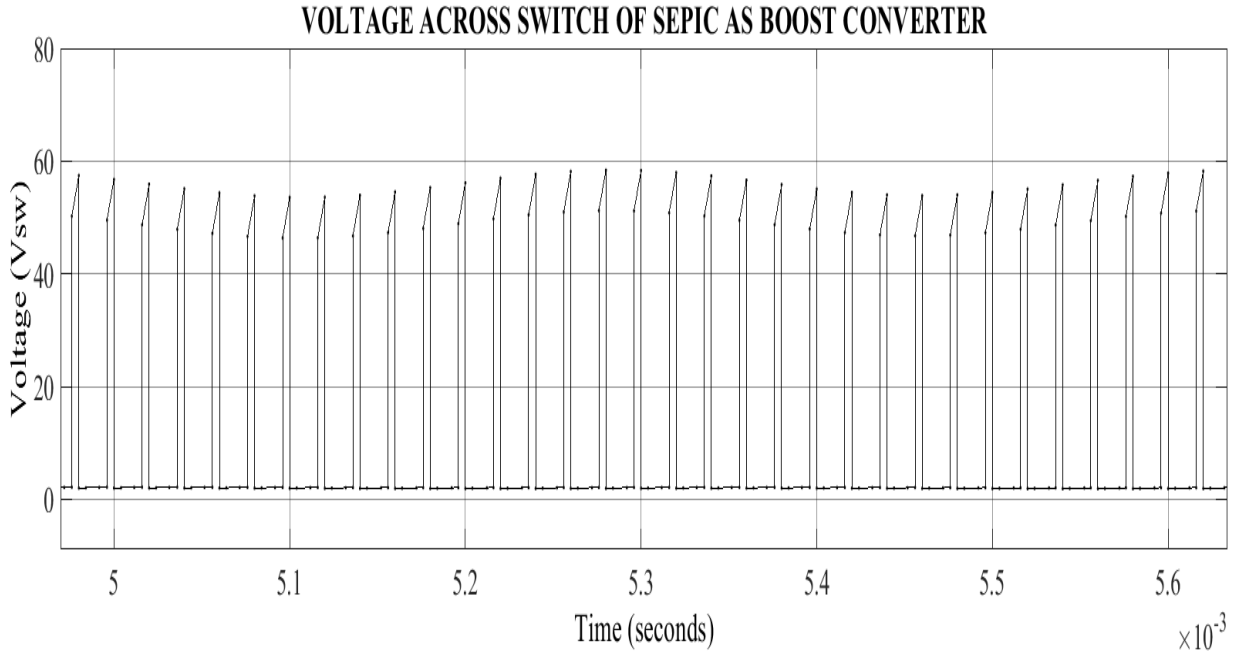

Figure 3.23: Voltage across switch of basic SEPIC as a buck converter for 12Volts (Vin)

So once again from our waveforms above it shows that the output voltage goes to almost 40v at steady state when the duty cycle is increased to 80% stepping up the voltage level of input voltage of 12v and the switch voltage at (0.005-0.0056)seconds confirms the equation shown next when the SEPIC acts as a boost converter.

$V_{S1} > 2V_{IN}$ (boost)

56v >24V (step up)

3.7 Efficiency Analysis

Having finished the simulations, now the focus is on calculating the efficiency of all the circuits using MATLAB before concluding this thesis. Now the next step is to make a table to show the different efficiency calculations of the various circuits that is simulated during this work.

Tables 3.7: Respectively Showing the Efficiency comparisons of the circuits

Converter	Efficiency %
Open Loop Basic SEPIC	91.42
Closed Loop Basic SEPIC	99.4

Converter	Efficiency %
Open Loop Basic SEPIC	91.42
New Open Loop SEPIC	93.5

Converter	Efficiency %
Closed Loop Basic SEPIC	99.4
New Closed Loop SEPIC	99.97

Converter	Efficiency %
New Open Loop SEPIC	93.5
New Closed Loop Basic SEPIC	99.97

.

As it was said to get shown. So here the efficiency analysis can be seen as straight forward as it is that the new proposed SEPIC converter is more efficient than the basic SEPIC circuit design. Comparing both the basic SEPIC and the new SEPIC converter.

CHAPTER 4
CONCLUSION

So from the results and analysis you can see that a SEPIC converter is a very interesting converter not only for the fact that it is very efficient but the working process of it is quite fun. It was fun researching about it and it does have a lot of advantages, it is a very good converter when it comes to regulation of voltage even without the upgrades made to it you can see that it has an efficiency of above 90 percent when the parameters are properly selected. You can see that it also maintains the polarity at the input hence making it more preferable for use than the popularly known buck-boost converter. In this work I did make further advancements to the basic SEPIC converter topology by adding resonating capacitors across the diode and the MOSFET switch which are the switching devices to achieve soft switching in the circuit by bringing the voltage down to zero at turn on before the gate voltage is applied causing a reduction in transition loss and you can clearly see the influence on it by the increase in efficiency of the newly proposed SEPIC converter. So bypassed a lot of faults and reduced losses across the switch. Put into consideration also the effect of a controller applied across the basic SEPIC converter we can see by applying feedback and controlling the output you have an efficiency that is close to perfect which also got perfected more by introducing the resonant capacitors into the closed loop basic SEPIC converter. Generally satisfied with the output results and can say that the whole system was greatly improved my introducing these techniques. Let's take into consideration that even in the closed loop control of the conventional SEPIC converter there was still a slight over shoot not to talk of the over shoot we see when it is not being controlled but with the introduction of the resonating capacitors we eliminate that rapid over shoot which would protect the circuits components and the whole device from damages. So it can be boldly stated that the new resonant SEPIC converter which achieves soft switching by applying ZVS can operate efficiently over a wide variety of input voltage and also can perform excellently when high frequency operation is involved. Take into account also the time it takes to get to steady state, when the capacitors are introduced both

in open and closed loop of the new SEPIC converter we see that it achieves steady state much faster than when there are no resonant capacitors involved in it. Also you saw examples of it working as buck- boost converter only better because its output gets to maintain the same polarity as its input so this converter can be used for a very large range of operations. The more efficient topology is preferred definitely, because it reduces the chance of components damaging, while running a high frequency operation that provides a beautifully working system with positive output voltage both when controlled with a PI controller and when it is open looped. For future purposes in experimental application you should note that it is wiser to use a coupled inductor instead of separate inductors to reduce cost, the required space on PCB and input ripple current is eliminated also. The SEPIC converter is used in real life applications like equipment's that require battery, Light emitting diodes lightening devices, Lithium ion (Li-ion) and nickel-metal hydride (NiMH) battery chargers, devices that are hand held and DC supply that have wide range input voltages. Thank You for reading, hope you enjoyed it.

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