SALAH M. ALI ESSALLAMI
SINGLE-SWITCH PWM CONVERTERS WITH HIGH STEP-UP CONVERSION RATIO
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A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

By
SALAH M. ALI ESSALLAMI

In Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name: Salah M. Ali Essallami

Signature:

Date:

To my beloved Mother…

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ABSTRACT

The essential requirement for many applications that uses dc-dc converters is that, the converter should have a high voltage conversion ratio with high efficiency and small number of semiconductor components. In this thesis, a set of three single-switch PWM high-voltage dc-dc converters have been proposed. These converters satisfy the above specifications with additional advantages. They operate at constant frequency and constant duty cycle. The proposed converters are obtained by modifying the classical Zeta, Sepic and Cuk converters with a special switched-capacitor circuit. A comprehensive description and mathematical analysis of the power circuits are presented. In order to complement the theoretical analysis a simulation is conducted on the converter circuits using PSCAD software. A comparison is made between the new converters and their conventional counterparts based on the theoretical results, in all the three cases a significant improvement has been identified. Both the theoretical and the simulation results indicated that the new converter topologies outperformed the classic ones. Furthermore, the presented converter structures give considerable savings in weight, cost and size. Although, the presented converters are faced with pulsating output currents problem, nevertheless, they are suitable for applications where extremely high-voltage output is the priority with small output current.

***Keywords*:** Dc-dc converter, Single-switched PWM high-voltage dc-dc converters, Zeta-Sepic-Cuk Converters, switched-capacitor circuit, PSCAD software

ÖZET

DC-dc dönüştürücüler kullanan birçok uygulama için temel gereklilik, dönüştürücünün yüksek verimlilik ve az sayıda yarı iletken bileşenle yüksek bir voltaj dönüşüm oranına sahip olması gerektiğidir. Bu tezde, üç adet tek anahtarlı PWM yüksek voltajlı dc-dc dönüştürücülerden oluşan bir set önerilmiştir. Bu dönüştürücüler, yukarıdaki özellikleri ek avantajlarla karşılamaktadır. Sabit frekansta ve sabit görev döngüsünde çalışırlar. Önerilen dönüştürücüler, klasik bir Zeta, Sepic ve Cuk dönüştürücülerini özel bir anahtarlamalı kapasitör devresiyle değiştirerek elde edilir. Güç devrelerinin kapsamlı bir açıklaması ve matematiksel analizi sunulmaktadır. Teorik analizin tamamlanabilmesi için, PSCAD yazılımı kullanılarak dönüştürücü devreler üzerinde bir simülasyon gerçekleştirilmektedir. Yeni dönüştürücüler ile konvansiyonel meslektaşları arasında kuramsal sonuçlara dayalı bir karşılaştırma yapılmış, üç durumda da önemli bir gelişme tespit edilmiştir. Hem teorik hem de simülasyon sonuçları, yeni çevirici topolojilerinin klasik olanlardan daha üstün olduğunu gösterdi. Ayrıca sunulan dönüştürücü yapılar, ağırlık, maliyet ve büyüklükte önemli ölçüde tasarruf sağlar. Her ne kadar sunulan dönüştürücüler, darbeli çıkış akımları sorunuyla karşı karşıya olsalar da, son derece yüksek voltaj çıkışının küçük çıkış akımı ile önceliği olduğu uygulamalar için uygundurlar.

Anahtar kelimeler: Dc-dc converter, Single-switched PWM high-voltage dc-dc converters, Zeta-Sepic-Cuk Converters, switched-capacitor circuit, PSCAD software.

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LIST OF ABBREVIATIONS

DC:	Direct Current
AC:	Alternating Current
L-C:	Inductor Capacitor
PWM:	Pulse Width Modulated
EMI:	Electromagnetic interference
ZCS:	Zero Current Switching
ZVC:	Zero Voltage Switching
CCM:	Continuous Conduction Mode
DCM:	Discontinuous Conduction Mode
PSCAD:	Power System Computer Aided Design
IBC:	Interleaved Boost Converters
SCBC:	Switched-Capacitor Based Converters
CIBC:	Coupled-Inductor Based Converters
RCN:	Ripple Cancellation Network
ZDC:	Zeta-Derived Converter
SDC:	Sepic-Derived Converter
CDC:	Cuk-Derived Converter

CHAPTER 1

INTRODUCTION

1.1 Overview

DC-DC converter converts DC voltage from one level to another. The DC-DC converters are high-frequency power conversion circuits that use high-frequency switching and inductors, transformers, and capacitors to smooth out switching noise into regulated DC voltages. The most common topologies are the buck, boost, buck-boost and Sepic converters. A buck converter steps down a voltage, producing a voltage lower than the input voltage. On the hand, boost converter steps up a voltage, producing a voltage higher than the input voltage. A buck-boost converter steps a voltage up or down, producing a voltage equal to or higher or lower than the input voltage. A Sepic converter is used for similar applications as the buck-boost, but provides some advantages in some applications (Maker.io, 2016). Many electronic equipment such as, servo-motor drives, computer periphery power supplies, high-intensity-discharge (HID) lamps for automobile headlamps X-ray power generators, the dc back-up energy system for an uninterruptible power supply (UPS), and fuel cells required dc–dc converters with a high step-up voltage ratio. A common requirement for the above applications is the development of a greater performance in high step-up dc–dc converter (Ismail, Al-Saffar, Sabzali, & Fardoun, 2008).

In order to achieve a high voltage gain ratio and improve converter performance and efficiency, a number of converter topologies have been introduced in the literature. It has been shown that interleaving techniques with transformer or coupled inductors can achieve a high voltage gain ratio (Henn, Silva, & Prac, 2010). Nevertheless, despite the improved performance showed by this topology, the use of two active switches with additional protection circuits across them increases the cost and complexity of the circuit. Another cost-effective solution for a high voltage conversion ratio was presented by using a single active switch with a clamp-mode coupled inductor (Zhao, Tao, Hu, & Lee, 2001). However, between the leakage inductance of the coupled inductor and the parasitic capacitor of the output diode the pulsating input current and high peak current exist through the clamp capacitor is the presence of a resonant circuit.

Other structures based on a combined boost-flyback converter with a reduced switch voltage stress and high-voltage conversion ratio are presented in (Tseng & Liang, 2004). However, the input current is no longer continuous in these topologies, thus large input filter is required. Meanwhile, in an effort to address the above drawbacks, in this thesis a single-switch dc–dc converter with high voltage gain is proposed. The new converter has achieved numerous advantages including reduced voltage stress on the switching elements, high voltage at the output at smaller duty-cycle. The presented converter is suitable for many applications where high output-voltage is desired.

1.2 Aim and Objectives

The aim of this thesis work is to design and simulate a new family of a single-switch three-diode dc–dc pulse width-modulated (PWM) converter operating at constant frequency and constant duty cycle. This is going to be accomplished by achieving the following objectives:

1. Designing a switched-capacitor (SC) cell.

2. Modifying the conventional dc-dc converters (Cuk-Sepic-Zeta) based on these cell structures.

1.3 Methodology

In this thesis, the design process begins with design of a new switched-capacitor (SC) cell. The cell is composed of two identical capacitors and three diodes. Based on these cell structures and the conventional dc–dc converters (Cuk–Sepic–Zeta), five basic new dc–dc PWM converters are generated. PSCAD software is used for the simulation of the converters.

1.4 Significance and Scope

The proposed converter differs from the conventional dc to dc step up converter, and offers a number of advantages which includes; higher voltage gain with small output voltage ripples, higher attainable output voltage with lower operating duty cycle. Other advantages of the proposed converter include lower voltage stress on the semiconductor devices, reduced size and weight, simpler structure and control, and automatic power factor correction (PFC). Furthermore, due to reduced voltage stress on the diodes Schottky diodes can be used for

alleviating the reverse-recovery current problem, as well as decreasing the switching and conduction losses.

1.5 Organization of Thesis

The thesis report comprises of four chapters. Chapter one gives general overview of the thesis. A review on some of the converter structures that have been introduced in the literature to increase the voltage gain ratio and improve converter performance and efficiency is given in chapter two. Chapter three discusses the power circuit description, developments and the simulation results are presented in chapter four. Finally, chapter six gives conclusion of the thesis work and discusses some recommendations for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Background

Recently, high-voltage ratio dc-dc converters are becoming popular by virtue of their suitability in numerous equipment which include motor drives (Kim, J., Ha, K., Krishnan, 2012), uninterruptible power supply (UPS) (Abusara, M.A., Guerrero, J.M., Sharkh, 2014), X-ray power generators , electric vehicles (Yilmaz, M., Krein, 2013), and many more. Basic requirement for such applications is the development of high efficiency, high performance, low cost, reduced stresses on the semiconductors, robustness and simplicity of the converters used (Ismail et al., 2008).

In line with that, this chapter presents a review of some of the most significant boost dc–dc converter topologies. The converters are classified based on interleaving techniques, coupled-inductor based and switch-capacitor based, this is shown in figure.2.1. A among the most significant converters a comparison is made in each class.

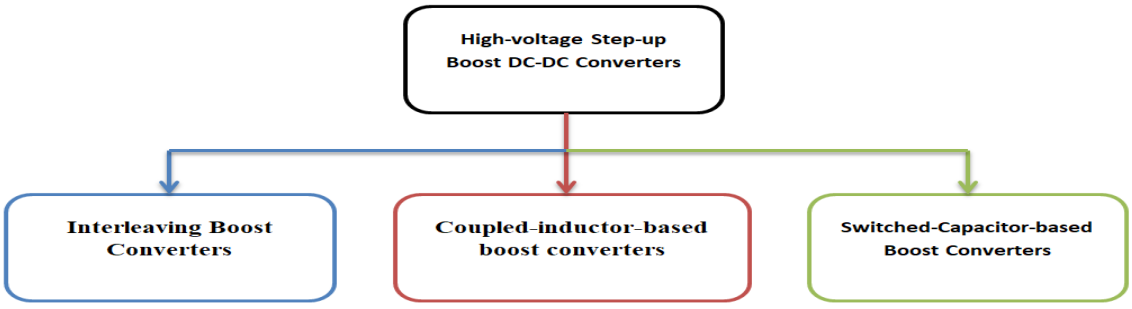


Figure 2.1: High-Voltage Step-up Boost Converters (Tang, Wang, & He, 2014)

2.2 Interleaving Techniques

2.2.1 Conventional interleaved boost converters (IBC)

An interleaved boost converter is proposed in (Garth, D.R., Muldoon, W.J., Benson, G.C., Costague, 1971). The proposed 2-phase interleaved converter is shown in Figure 2.2, in which the input current is split among two switches, two diodes and two inductors. Based on the number of phases, the inductor's operating frequency is now multiple of the switching frequency, while the currents flowing through the switches are just portions of the input current. This reduces the electromagnetic interference (EMI), inductors size and filter size.

A number of trade-offs are possible, for instant, one can reduce the switching frequency by a factor N to increase the conversion efficiency and also in order to reduce the converter size the inductance per cell can be reduce by the similar factor N.The resulting system will produce N^2 times larger per-cell ripple compared to a single-cell converter, however the total interleaved ripple will be the same. For this reason interleaving is used to improve the power density and with the reduction of the ripple current associated with conversion efficiency (Garth, D.R., Muldoon, W.J., Benson, G.C., Costague, 1971).

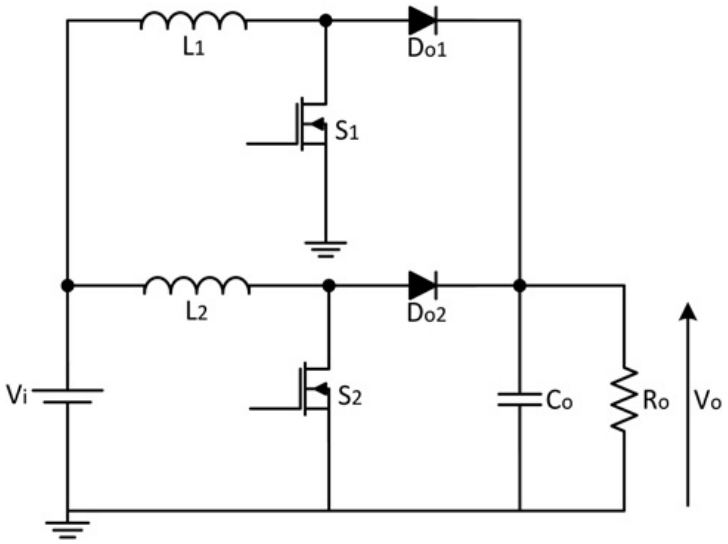


Figure 2.2: Two-phase conventional boost interleaved converter (Garth, D.R., Muldoon, W.J., Benson, G.C., Costague, 1971)

However, in this topology voltage stress across switches and diodes is equal to the output voltage, which makes it insufficient for high output-voltage applications. Also the converter efficiency is

limited by the reverse recovery of the boost diodes. And the static gain is equal to that of conventional boost converter.

2.2.2 IBC with voltage doubler

With unity turn ratio an autotransformer is used in the converter proposed in (Jang & Jovanović, 2004), this is shown in Figure 2.3, in this circuit, between the switches the current is equally shared. To increase the static gain voltage doubler is used the output. the output voltage across the switches is less than or equal to 50%. The input current ripple is minimized and the input current is continuous. The main shortcoming of such converter is the presence of auxiliary transformer and also an inductor per cell of the interleaved converter, which result in increased dimensions and cost.

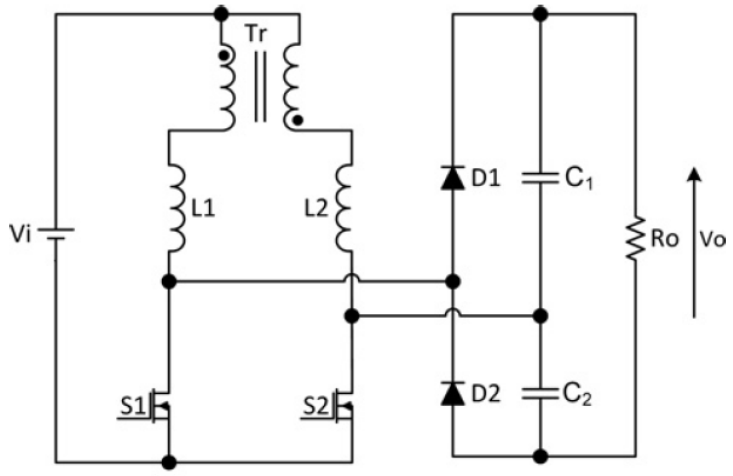


Figure 2.3: Two-phase IBC with voltage doubler (Jang & Jovanović, 2004)

2.2.3 Coupled-inductor IBC

In another paper (Henn et al., 2010) a novel coupled-inductor IBC was introduced. This converter provides a significant improvement in gain compared to conventional boost converter topology. The main features of this topology are large voltage step-up with reduced voltage stress across the main switches, voltage balancing between output capacitors, low input-current ripple, high switching frequency, which reduce the structure volume and weight. In order to obtain high gain, a voltage-doubler circuit is magnetically coupled to the conventional–interleaved boost as shown in Figure 2.4. Also, to result in higher output voltage, the number of semiconductor devices is the

same as in the traditional interleaved boos1t arrangement, though two coupled inductors L1 and L2 are added,. The interleaved-boost switching cycle is composed of four stages.

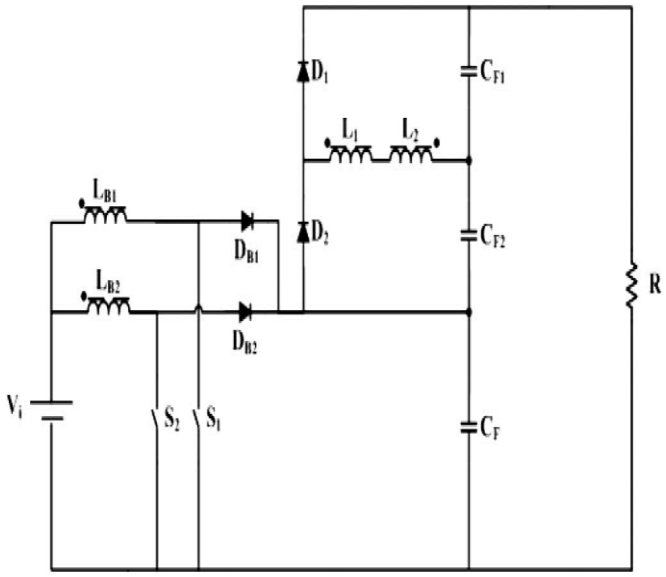


Figure 2.4: Proposed high-voltage-gain boost converter(Henn et al., 2010)

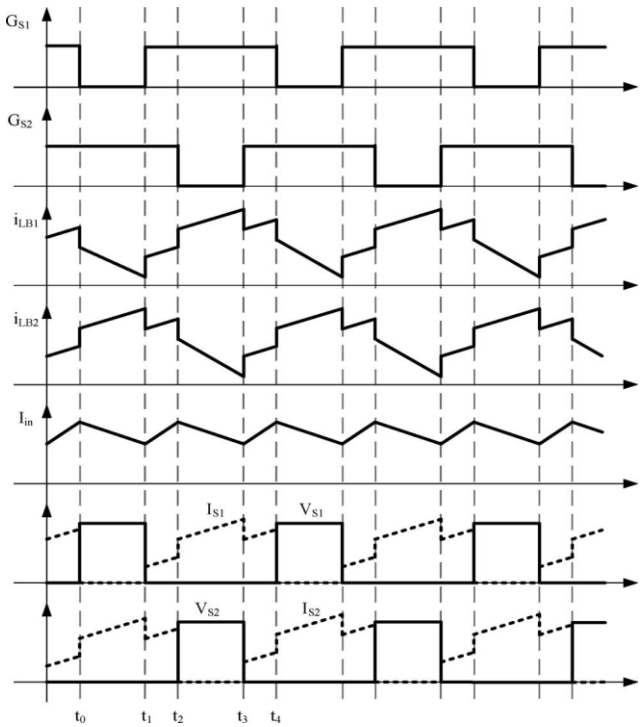


Figure 2.5: Main theoretical waveforms (Henn et al., 2010)

The static voltage gain was obtained as:

$$G = \frac{V_o}{V_i} = \frac{(2nk)+1}{1-D} \quad (2.1)$$

Figure 2.6 illustrates the relation between the static gain and the duty cycle (G × D), for different values of magnetic coupling coefficient (k) and transformer turns-ratio (n). From this figure it can be noticed, even though a unitary transformer turns-ratio is adopted, the static voltage gain is far higher than the one obtained using a conventional-boost converter, also with the duty cycle near 50%.

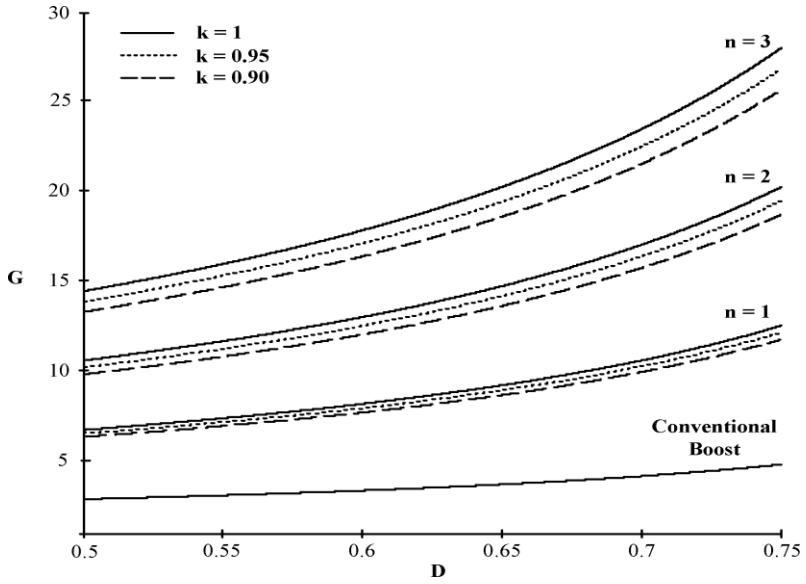


Figure 2.6: Relation G and D for different values of n and k (Henn et al., 2010)

Related to this topology the main drawbacks are the duty cycle limitation, as it must be higher than 50%, initial charge of output capacitors and soft starts is needed, which common in to structure deriving from conventional boost converters.

2.2.4 Soft-Switched Interleaved Boost Converters

Park (2011) proposes a multiphase dc-dc converter scheme of new soft switching interleaved boost converters that is suitable for high step-up and high-power applications (Park, Park, & Choi, 2011).To result in high component availability and easy thermal distribution, the proposed converter is configured with proper numbers of series and parallel connected basic cells which lead to flexibility in device selection.

The basic cell used to build the proposed converter and the generalized circuit of the proposed converter are shown in Figure 2.7 and 2.8 respectively. In Figure 2.7, N is the number of output series-connected basic cell and P is the number of output parallel-connected basic cell. “N” could be increased to get higher output voltage while “P” could be increased to get higher output power. Also, by increasing N and P, respectively the voltage and current ratings of diodes can be reduced. Therefore, by proper choice of N and P optimum devices in the sense of cost and availability can be selected.

Furthermore, choosing higher value of N reduces the required duty cycle, resulting in reduced voltage rating of the component. However, this in turn increases the numbers of components. Therefore, N is chosen to be as low as possible if voltage ratings of the components are within some limit.

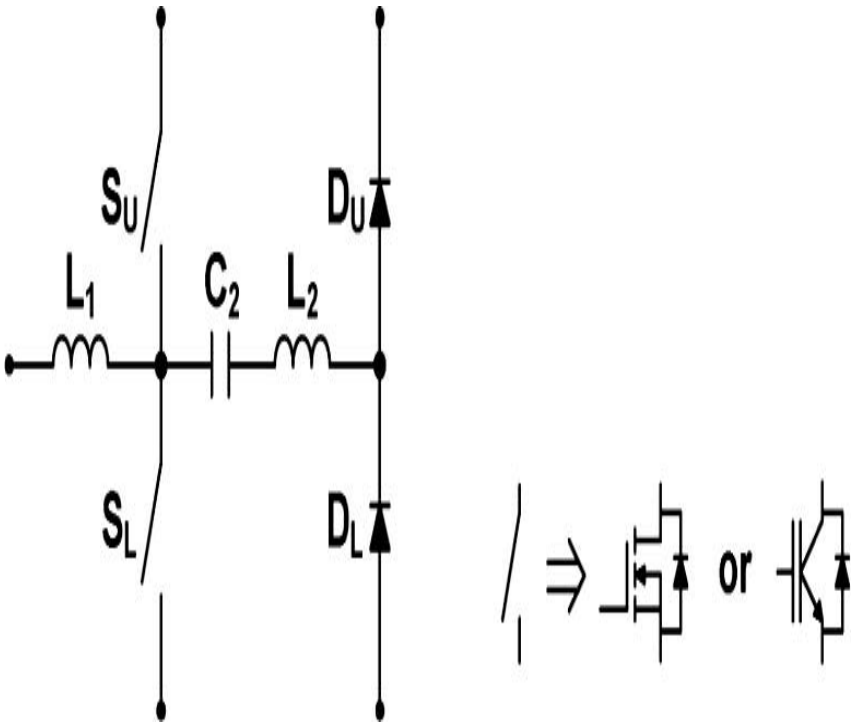


Figure 2.7: Basic cell of the proposed interleaving high step-up converter (Park et al., 2011)

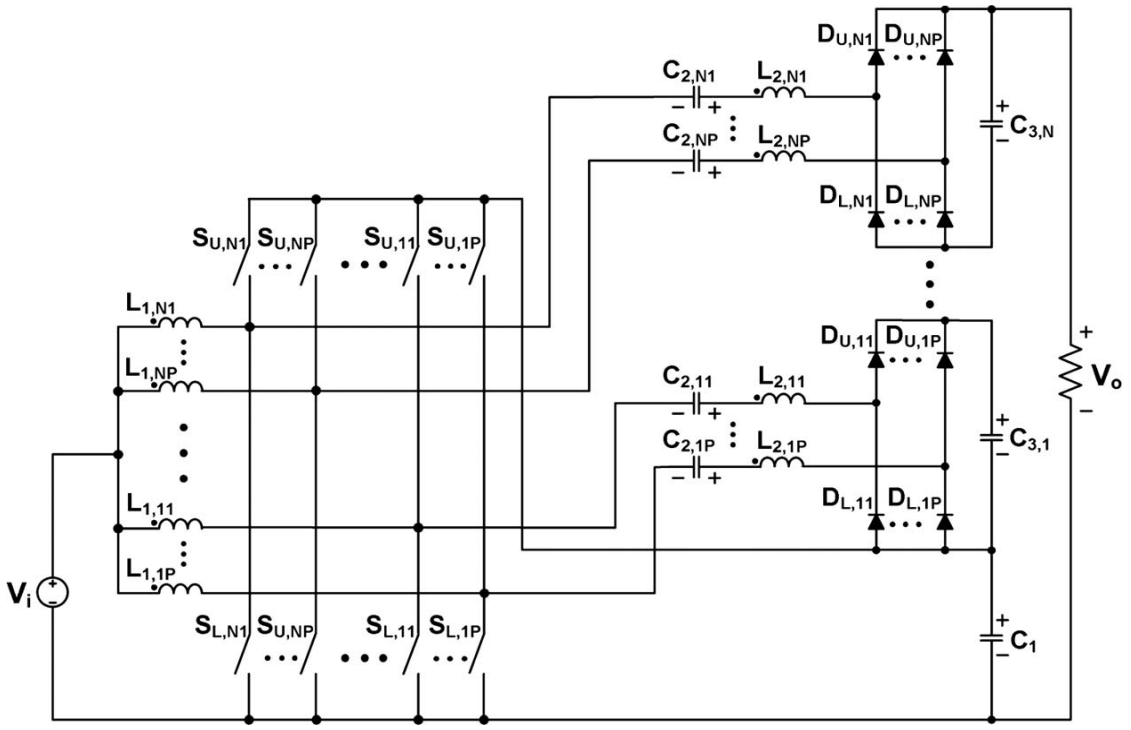


Figure 2.8: Generalized circuit topology of the proposed interleaved high step-up dc–dc converter (Park et al., 2011)

Assuming that the voltages across C1, C2, np, and C3, during the switching period of TS n are constant, I–O voltage gain of the proposed converter is obtained as

$$\frac{V_o}{V_i} = \frac{D\alpha - \alpha + \sqrt{\alpha(D^2\alpha - 2D\alpha + \alpha + 2\beta + 2\beta N)}}{\beta} \tag{2.2}$$

$where\ \alpha = DR_o\ and\ \beta = 4f_sL_2$

compared to that of the conventional boost converter, the effective voltage gain of the proposed converter is almost N + 1 times. Since reduced duty ratio leads to reduced current stresses on the components. This is a very desirable feature in high step-up applications, resulting in increased efficiency.

The propose converter offers a number of advantages including; reduced voltage stresses of switches and diodes, ZCS turn-off of the diodes and ZVS turn-on of the switches in CCM, low-input current ripple due to the interleaved structure, reduced energy volumes of most passive components and extendibility to desired voltage gain and power level.

2.2.5 IBC with Ripple Cancellation Network (RCN)

An IBC with RCN is developed in (Gu & Zhang, 2013). The RCN includes two coupled inductors, two capacitors and two inductors. The coupled inductors of the network share the same core with the main inductors. The interleaved structure with the RCN and the key steady waveforms are depicted in Figure 2.9 and Figure2.10.

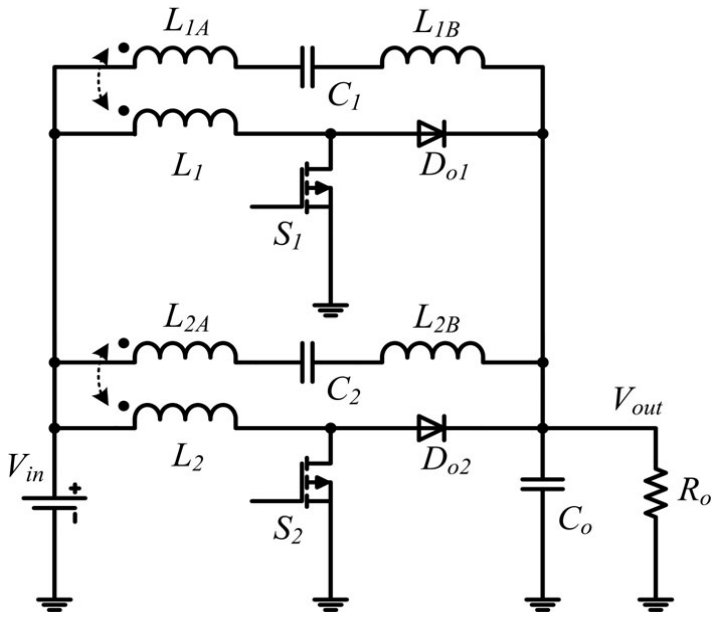


Figure 2.9: Circuit Configuration (Gu & Zhang, 2013)

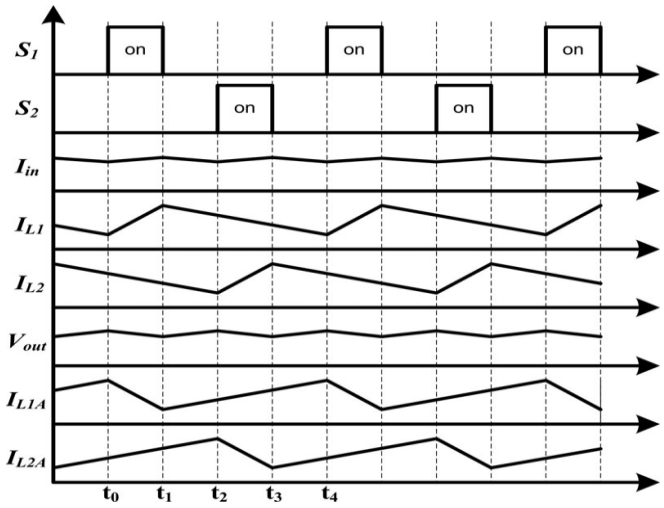


Figure 2.10: Key steady waveforms (Gu & Zhang, 2013)

The four stages of the converter can be simplified into two typical stages and the corresponding equivalent circuits for each operational stage are shown in Figure 211.

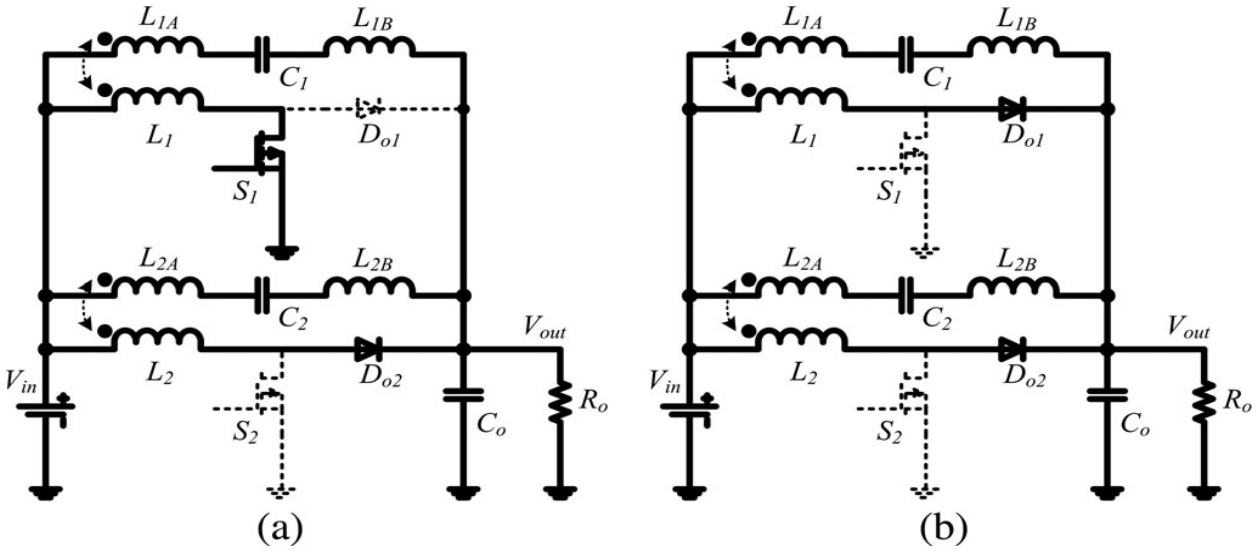


Figure 2.11: Operation stages of the proposed converter. (Gu & Zhang, 2013)
(a) Stage 1 [t0 − t1]. (b) Stage 2 [t1 − t2]

For time interval [t0, t1]: The switch S1 turns ON and the switch S2 is OFF at t0. The main inductor L1 of the converter is charged linearly by the input voltage, causing its current IL1 increase linearly. The output diode Do1 maintains in OFF state with the voltage stress equivalent to the output voltage. In the meantime, the energy stored in the main inductor L2 starts to be transferred to the load Ro. Because of the coupled relation between the main inductor and ripple cancellation branch, zero current ripples can be achieved.

Within the time range [t1, t2]: At t1, the switches S1 and S2 are all in OFF state. Both main inductors L1 and L2 start to transfer their energy to the load Ro, so the inductor currents IL1 and IL2 decrease linearly. The voltage stresses of the switches S1 and S2 are equal to the output voltage. In this mode, the coupled inductor branches still work as an RCN to minimize the input current ripple.

This converter improves on the conventional IBC, by adding two capacitors, two coupled inductors, and two inductors as RCN. Therefore, in addition to the advantages of the conventional

IBC, the proposed converter achieves input current ripple cancellation without significant increase in the current stress and converter loss.

2.3 Coupled-inductor-based boost converters (CIBC)

2.3.1 Conventional CIBC

It has been shown that static gain of dc-dc converters can be improved by employing coupled inductors. In this context, the leakage inductance is utilized to restrict the falling rate of the diode, so as to minimise the diode reverse recovery problem. Moreover, the coupled inductor can serve as a transformer to avert excessive duty cycles and to lessen the current ripple in high step up conversions. A high voltage gain CIBC is proposed in (Zhao & Lee, 2003) and shown in Figure 2.12a, in this circuit which the turns ratio can be appropriately adjusted to achieve the desired result. The idea is that, the static gain can be increased as desired by manipulating the turns ratio through this simple and up-front technique, also the duty cycle is kept constant. Nevertheless, there may be high voltage spikes due to leakage inductance, which will make the voltage stress across the switches larger giving rise to excessive EMI noise and reduces efficiency. And also pulsating input current.

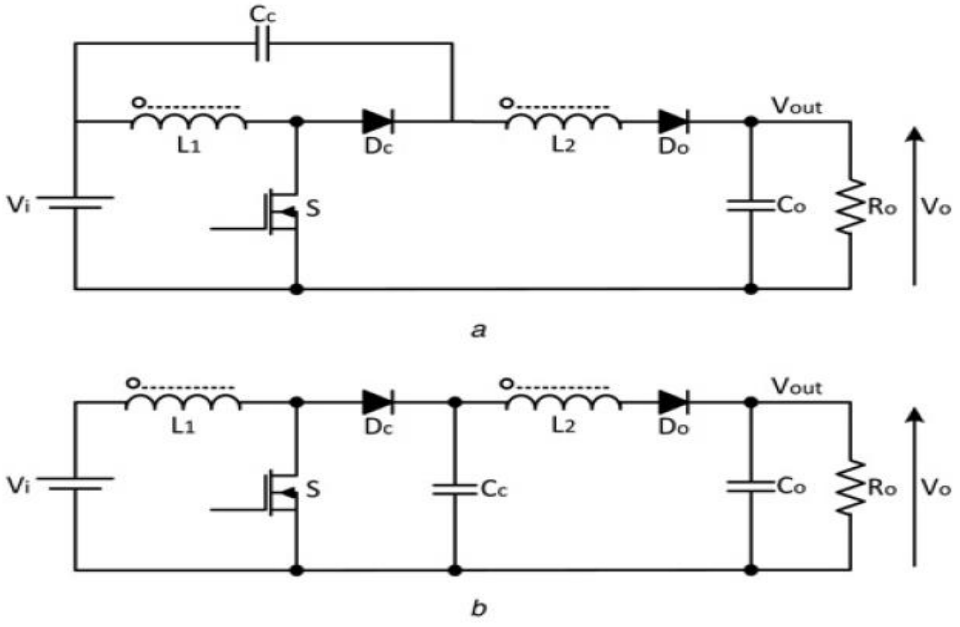


Figure 2.12: High-voltage Gain CIBC (a) High-voltage gain CIBC (Zhao & Lee, 2003) (b) High-voltage gain CIBC with clamping circuit (Silva et al., 2009)

The above topology is modified in (Silva et al., 2009) by using a clamping circuit. The circuit is as shown in Figure 2.12b, the purpose of the additional clamping circuit is to minimize the voltage stress across the switch introduced by the leakage inductances from the coupled-inductor. This provides a robust, straightforward and low-cost solution. However, the total voltage on the diode D_o is extremely high, hence necessitating the use of expensive semiconductors that intrinsically produce low switching rate and high forward voltage drop. Considering that efficiency is generally low, while EMI level is considerable as a result of input current pulsating, this method is proposed for high voltage step up and low input voltages (Silva et al., 2009).

2.3.2 High step-up Converter with Quasi-Active Switched-Inductor (QSAL)

Here, dual switch converter is proposed. This converter merges QA-SL together with conventional boost converter. It is composed of two switches, two capacitors, three diodes and two coupled-inductors. The primary sides of coupled inductors are charged in parallel by the input source, and the secondary sides of coupled inductors are discharged in series with the input source and two capacitors to achieve high step-up voltage gain with an appropriate duty ratio. The two sets of diode-capacitor circuits assist to increase the voltage conversion gain and also reduce the voltage stress across the switches by mitigating voltage spike caused due to leakage inductance of the coupled inductor. Additionally, the conversion efficiency is improved because the reverse recovery issue of the diode at the output is also taken care of and the other two diodes turn off inherently and therefore have no reverse-recovery issue.

Figure 2.13 shows the basic circuitry of the QASL boost converter. The two coupled-inductors are arranged in fly-back. During the switching on, the two coupled-inductors are connected in parallel from the primary side and being charged from the input supply; on the other hand during the off state, the coupled-inductors act in series and hence discharge to the load, likewise the input supply.

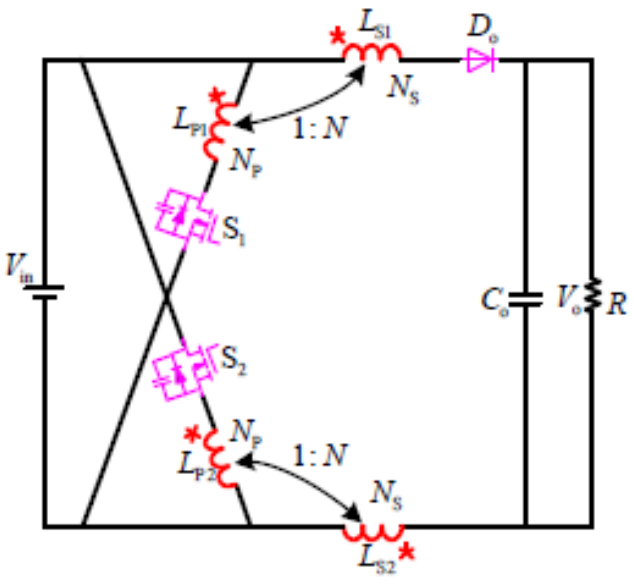


Figure 2.13: Basic QA-SL Converter Circuit (Transactions & Electronics, 2015)

The voltage gain for the converter in Figure 2.9 is $((2\mathrm{N}-1)\ \mathrm{D}+1)/(1-D)$, With D equal to the duty cycle ratio of the switches. The main shortcomings of this topology are; large voltage spike across the switches and reduced voltage-gain. To overcome voltage spikes resulting from leakage inductance and improve the gain, additional two capacitors and two diodes are incorporated as shown in Figure2.14.

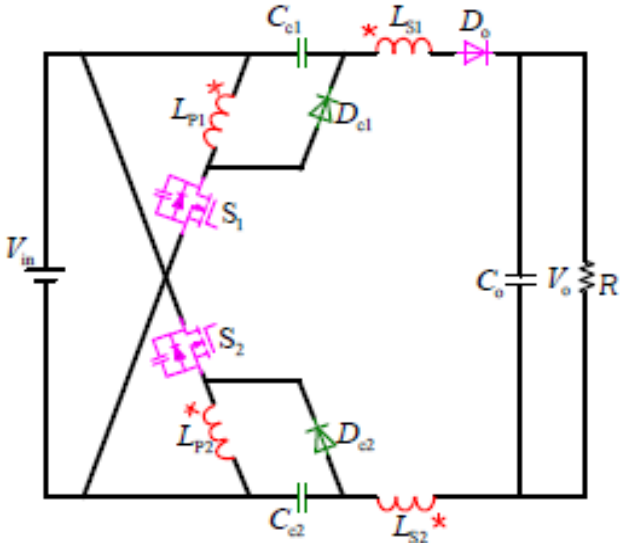


Figure 2.14: Dual Switches QA -SL Boost Converter (Transactions & Electronics, 2015)

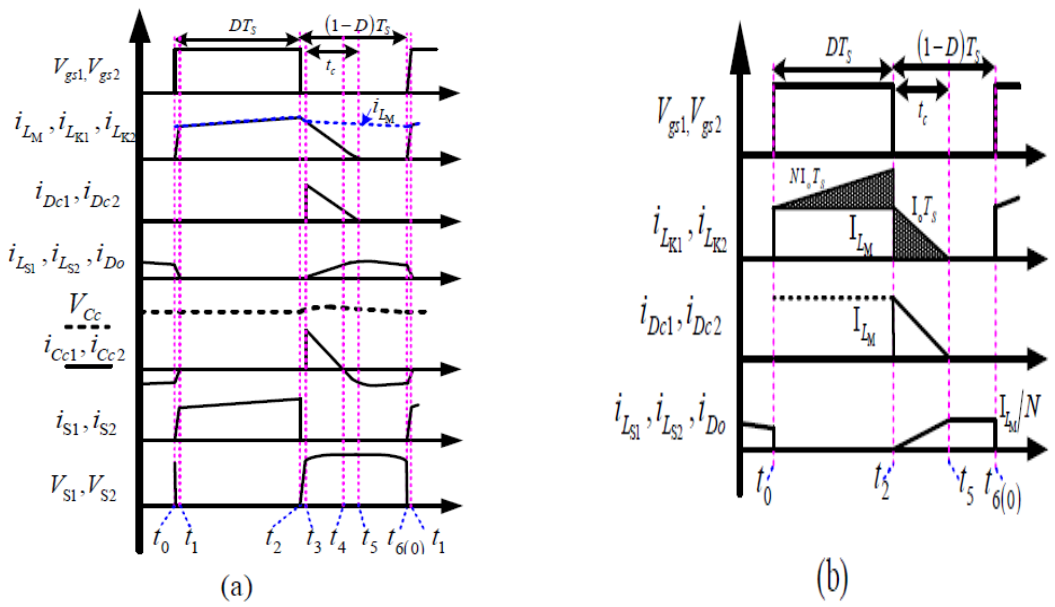


Figure 2.15: (a) Waveform of dual QA-SL Converter; (b) Simplified Waveform (Transactions & Electronics, 2015)

The improved voltage gain is given as

$$G = \frac{D(N(K+1)+1)+1}{1-D} + \frac{D(K-1)}{1-D} \tag{2.3}$$

Which shows that the voltage gain depends on the leakage coefficient N and turn ratio k. The relationships are shown in Figure2.15.

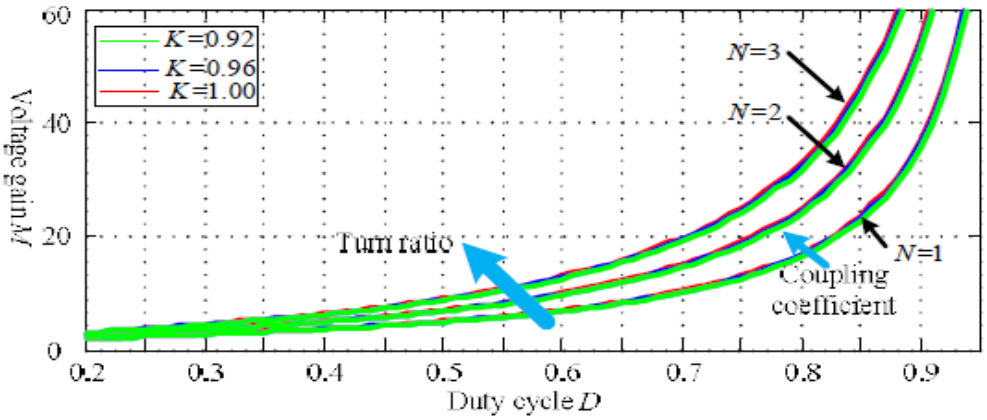


Figure 2.16: Leakage Inductance Effect on The Voltage Gain (Transactions & Electronics, 2015)

2.3.3 Hybrid Boost-flyback Converter

The ordinary coupled-inductor flyback converter is capable of producing high voltage gain, at the expense of poor efficiency due to leakage inductance, hence limiting its usage to extremely low power applications. Conventional boost converters on other hand are not able to produce high-voltage gain, because of equivalent series resistor of the boost inductor however, they attained high efficiency at low output-voltage gain. A hybrid boost-flyback converter is developed by connecting their outputs together to achieved high voltage gain. In this arrangement, the boost converter acts like a clamping circuit (Tseng & Liang, 2004). The hybrid circuit is shown in Figure 2.17 it is moderately easy solution employing few passive and semiconductors components. In this configuration, voltage across the switches is intrinsically clamped by the output-capacitor. Furthermore, voltage stress around the switch is minimized. The voltage stress around the output-diode is also minimized, relieving the reverse recovery issue.

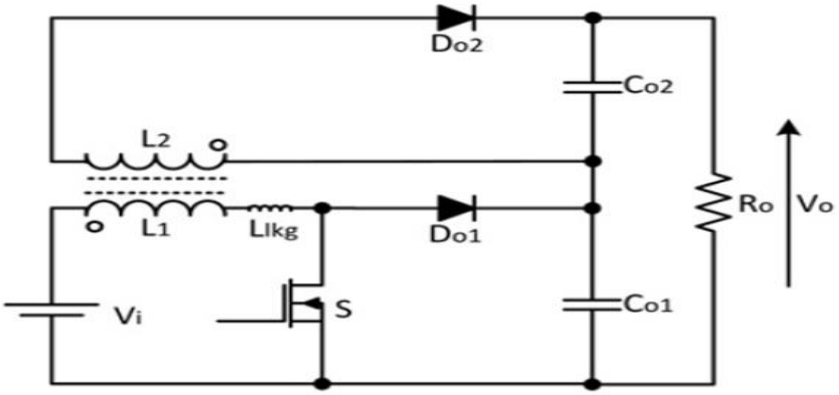


Figure 2.17: Hybrid boost-flyback converter (Tseng & Liang, 2004)

The voltage gain of this hybrid converter is expressed as:

$$\frac{V_o}{V_I} = \frac{1+D\frac{N_2}{N_1}}{1-D} \tag{2.4}$$

Which indicates that high output-voltage gain can be achieved at low duty ratio by increasing the coupled-inductor turn ratio N. The primary characteristics of this converter include high voltage gain, high efficiency, low voltage stress across the switches and design simplicity. Nevertheless, there is pulsating input current, hence requiring the use of additional filter to reduce EMI.

2.3.4 Hybrid Boost+flyback Converter with Voltage Multiplier

Another strategy is used in (Baek, Ryoo, Kim, Yoo, & Kim, 2005) to combine the flyback and conventional boost converters. This scheme utilizes a voltage multiplier circuit as shown in Figure 2.18. This provides an essential option that permits tradeoffs between the coupled-inductor turns ratio and the number of voltage multiplier circuits, with additional flexibility in the design process. In this topology the output voltage is greater than the voltage stress around the switch. Furthermore, it is not influence by the number of multipliers cells or turns ratio, making this topology sufficient to high voltage step up and low input voltage ratings. The major issue of these converter topologies is about the voltage balance between output capacitors, due to the fact that they are serially connected.

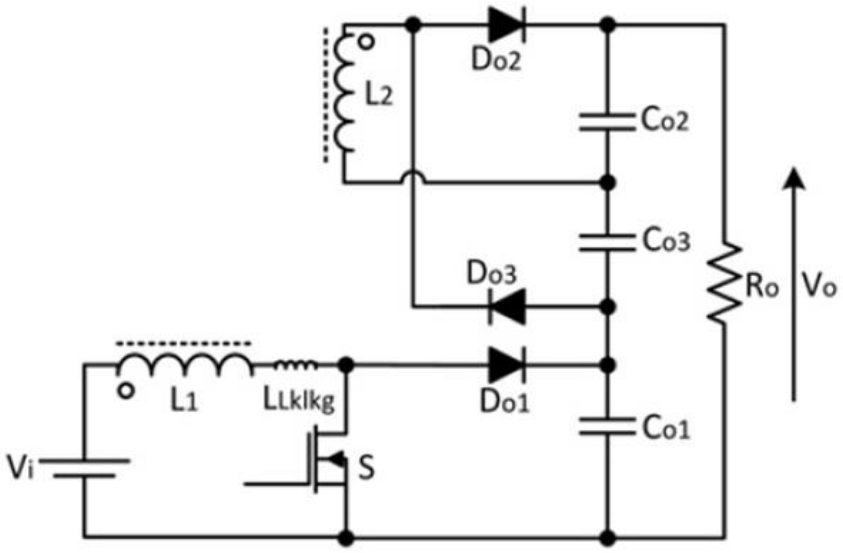


Figure 2.18: Hybrid Boost+flyback Converter with VMC
(Baek, Ryoo, Kim, Yoo, & Kim, 2005)

2.4 Boost Converters Based on Switched Capacitor

Voltage gain can be increase by combining conventional dc-dc converters with capacitors through. To further increase the static gain of the gain coupled-inductors can similarly be incorporated with switched-capacitors through adjusting the amount of coupled-inductor turns ratio (Liang et al.,

2012). Switched-capacitor inductor technique can also pave way for attaining large voltage step-up at the expense of increase number of components.

2.4.1 High-voltage Gain Boost DC-DC Converter with Switched-Capacitor (SC) Circuit

A novel converter based on switched-capacitor is presented in (Abutbul, Gherlitz, Berkovich, & Ioinovici, 2003) which is repeated here in Figure 2.19, from this circuit it can be seen that high voltage step up can be attained by increasing SC cells. The reverse recovery problem on output diode is taken care of due to the fact that it operates with low duty cycle. The capacitors share the same current making them to act as series connected voltage sources. Their various equivalent resistances have to be carefully minimised to avoid compromising efficiency. The circuit complexity increases as more switches are added. It is pertinent explain that different voltage stresses exist across the switches hence resulting in multiple ratings in the active switches specifications.

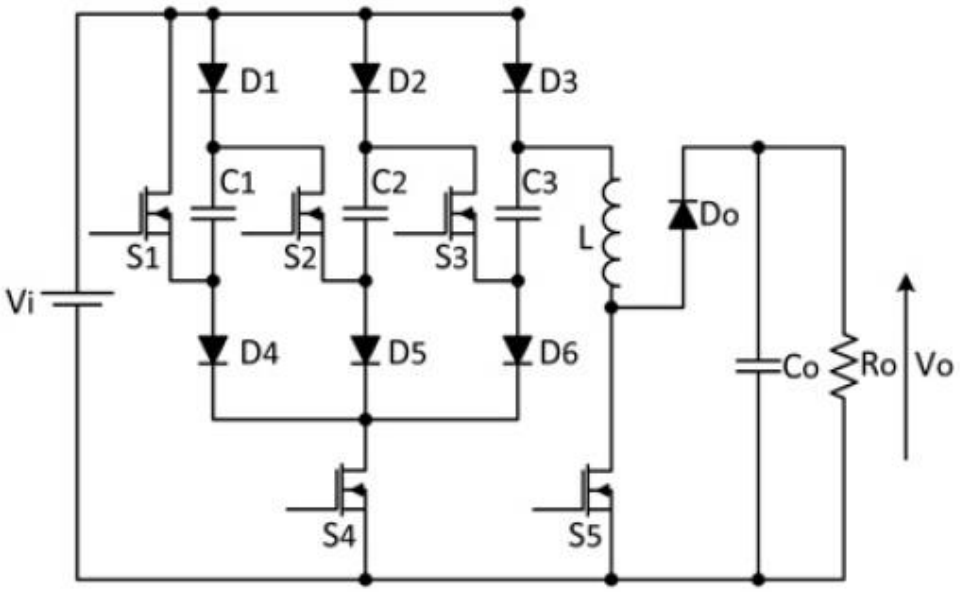


Figure 2.19: Switched-Capacitor (SC) Based Boost Converter (Abutbul et al., 2003)

2.4.2 Transformer less Boost Converters with High Voltage Ratio

In (Axelrod & Berkovich, 2003) a boost topology is combine with basic cell consisting of two diodes, two capacitors and an active switch to developed a transformer-less high voltage step up

converter shown in Figure 2.20. This scheme is same as the 1-switch quadratic converter, although two diodes and three capacitors were used, while they differ in static gain. However, compared with classical cascaded converters, there is reduction in the voltage stress around the switch. The efficiency is affirmed to remain equal to the efficiency of the classical boost converter (Axelrod & Berkovich, 2003). Therefore, this proposed topology is not suitable for high power applications.

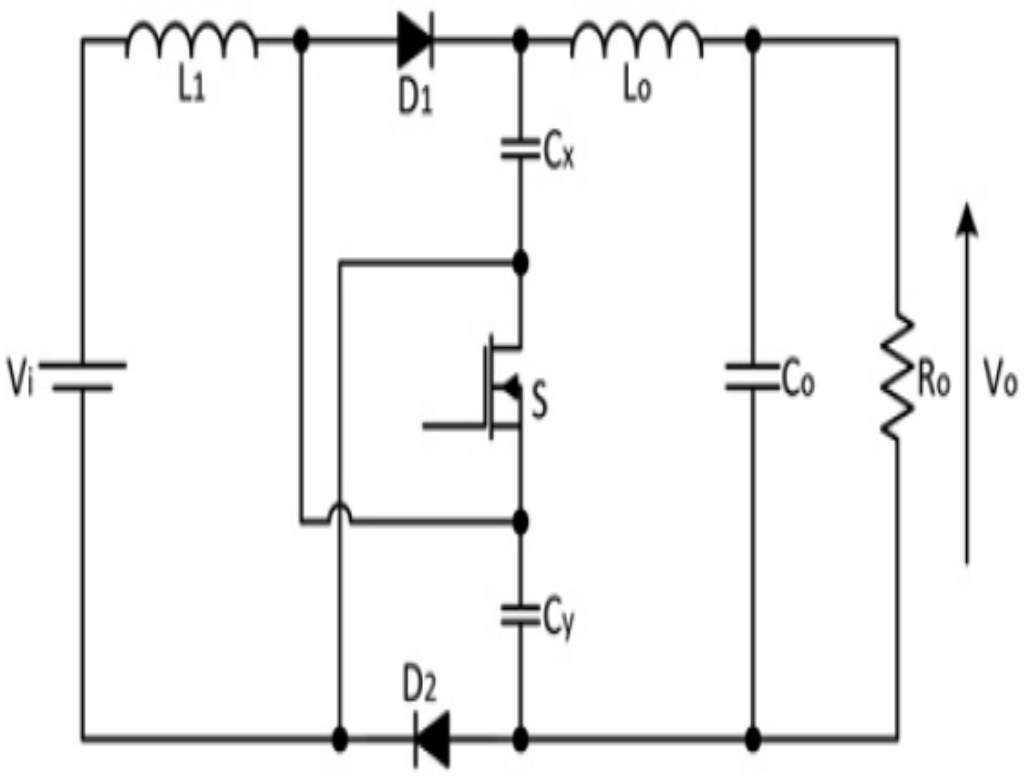


Figure 2.20: SC-based Boost Converter (Axelrod & Berkovich, 2003)

2.4.3 SC-Based Multilevel Boost Converter

A boost converter with switched capacitor circuit is presented in (Rosas-Caro et al, 2009) which is shown here in Figure 2.21. With this topology it is possible to achieved double voltage gain compared with ordinary boost converter, while achieving self-voltage balancing within capacitors at the output the voltage stress around the principal switch is reduced. The voltage gain can be further improved by using modular method, nevertheless it is not suitable for high-power levels and high-current because there is increase in the input inductance and relatively increased current stress across the switch.

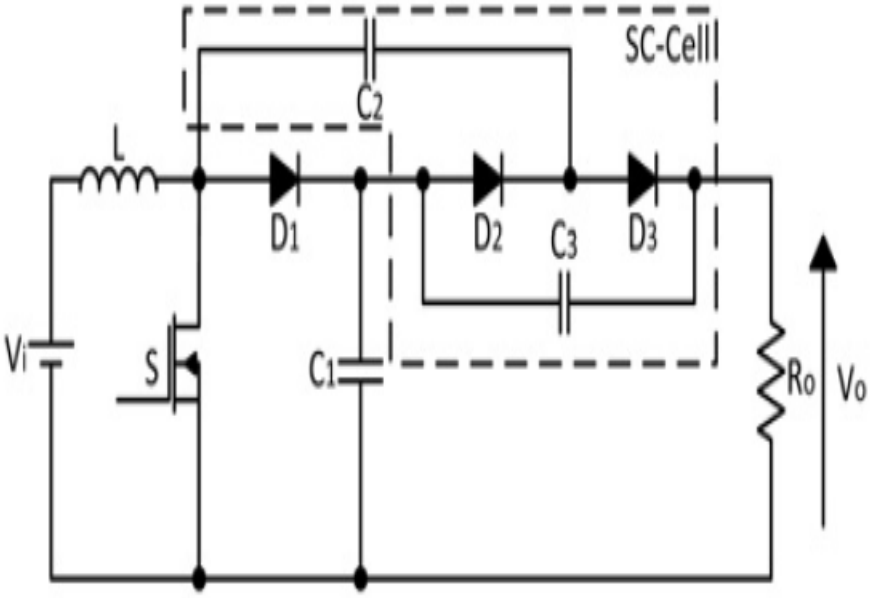


Figure 2.21: SC-Based boost converter Presented in (Rosas-Caro et al, 2009)

2.4.4 High-Voltage Gain SC-Based Active-Network Converter (SC-ANC)

A variant of the above topology is presented in (Tang, Wang, & He, 2014) which is shown in Figure 2.22. This topology added to the circuit an active switch and one inductor. As in the above topology self-voltage balancing is retained among the capacitors at the output.

Also there is reduction in the semiconductor's voltage ratings. Moreover, compared to (Rosas-Caro et al., 2009) there is significant improvement in the static gain. However, additional circuit elements are introduced in this configuration; also there is additional complexity in the drive circuitry because different reference nodes are used for the switches.

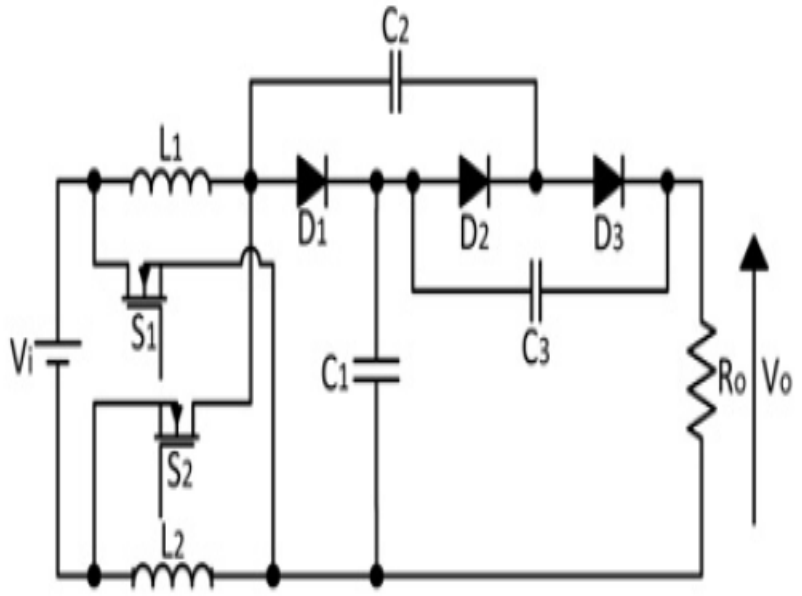


Figure 2.22: SC-ANC (Tang, Wang, & He, 2014)

2.4.5 SC-Based Step-up Resonant Converters

A novel group of switch-capacitor based resonant converters is proposed in (Law, Cheng, & Yeung, 2005). These converter topologies possess the advantages of conventional switching-mode power supply (SMPSs) and SC-based converters. Numerous voltage conversion ratios are possible by adjusting the number of SC cells. The resonant circuit help in alleviating the ordinary SC converter problem of current spike. Figure 2.23 and Figure 2.24 show the n-mode step-up voltage conversions and the switch-capacitor cell respectively. Zero current switching is in the operation of the switches inside the circuit this is possible due to extremely small resonant inductor used and the resonance of the switching capacitors. High-efficiency together with high frequency operations is feasible.

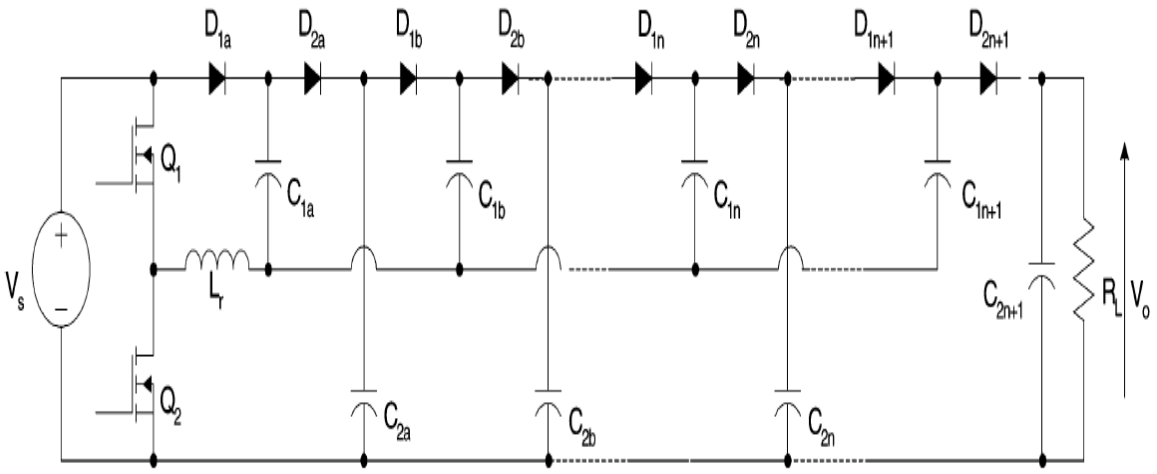


Figure 2.23: n-mode of SC-Resonant Converter (Law et al., 2005)

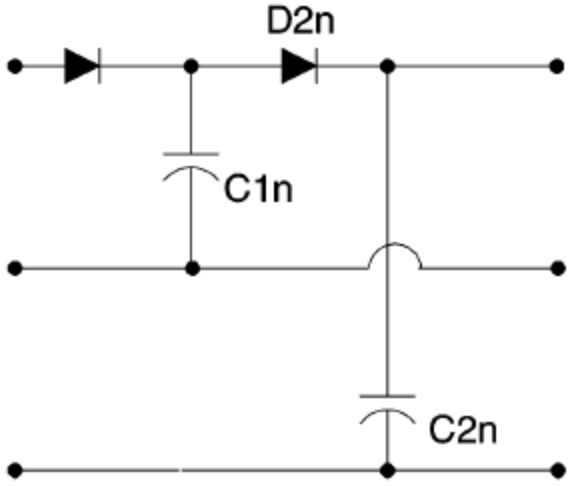


Figure 2.24: SC Cell Proposed in (Law et al., 2005)

2.4.6 MIMO DC-DC Boost Converters

To add flexibility to dc-dc boost converters a structure for multi-input multi-output (MIMO) is proposed in (Babaei & Abbasi, 2015). This is converter is able to handle energy sources with varying V-I characteristics. The proposed converter utilizes the conventional dc-dc boost converter and SC-based converters to provide output voltages at different levels as desired. In this scheme, by increasing levels of the output voltage it's able to decrease the voltage stress across switches. In this topology, for example for n-input m-output mode, only $n + 1$ switches plus one inductor are needed, which reduces the size, weight, losses and overall complexity. Figure 2.25a shows the

power circuit for an n-input m-output boost converter and the switching order of $S_1, S_2, S_n \; and \; S_{n+1}$ are shown in Figure 2.25b.

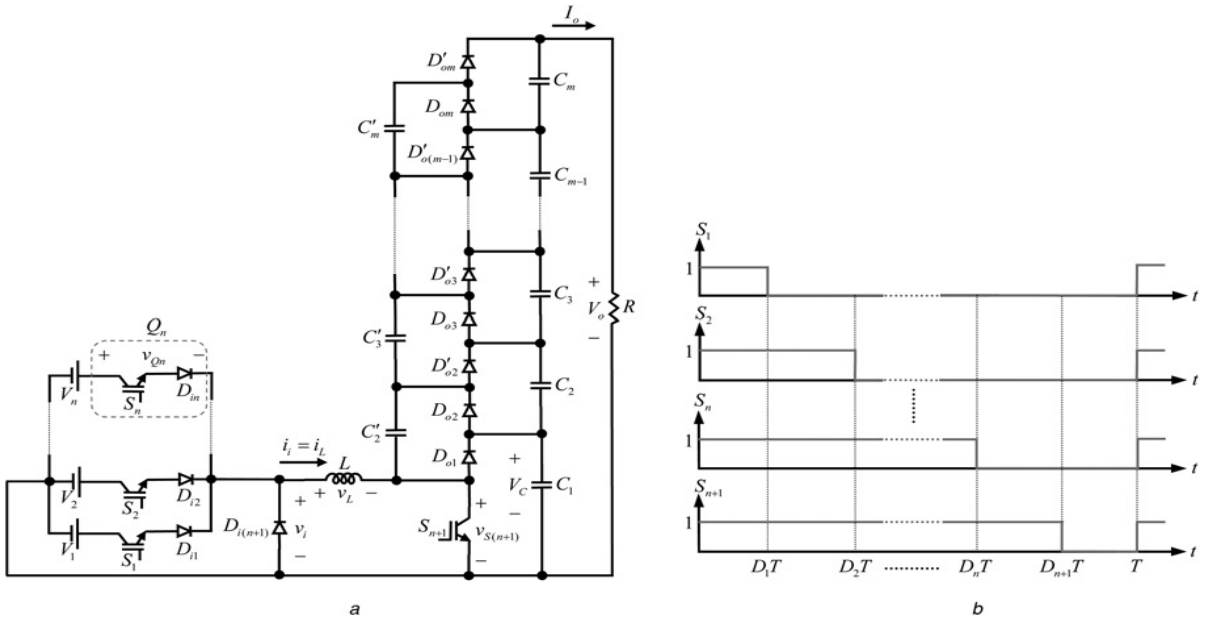


Figure 2.25: MIMO DC-DC Converter
(a) MIMO dc–dc boost converter (b) Switching order (Babaei & Abbasi, 2015)

The voltage gain for the proposed converter was found to be

$$\frac{V_o}{V_i} = \frac{m}{1-D_{n+1}} \tag{2.5}$$

V_o and V_i are the output and input voltages average values, respectively.

The voltage stress across switch S_{n+1} is

$$V_{S(n+1)} = V_C = \frac{V_o}{m} \tag{2.6}$$

The proposed converter presented as advantages; a high-voltage gain with low duty cycle, transformer-less, modularity capability, continues input current, high-switching frequency and ability to handle different sources with varying V-I characteristics. the proposed converter can be

used in PV systems when combine with a dc-link and other applications where multiple controlled voltage levels is required

2.5 Comparison

For the purpose of comparison some converter topologies from each technique i.e. interleaving, coupled-inductor and switch-capacitor techniques are compared based on their static gain, number of switches, voltage stress on switches, number of diodes, auxiliary transformers, number of capacitors, duty cycle range, number of inductors and operating frequency. This is shown in Table 1.

This chapter has presented a review on high-voltage step-up boost dc–dc converter topologies. Conventional boost converter is not suitable for applications requiring a high-power due to the fact that their output power is handled by only two semiconductor elements. Interleaving technique improve the efficiency since the output current is divided in to two to reduce losses. Alternatively, Coupled-inductor based techniques give another solution for achieving high voltage step-up through proper selection of the turn's ratio. However, there is relatively poor efficiency due to leakage inductance. It has been shown that in the literature that using switch-capacitors, it is possible to achieve high-voltages output particularly when used in a modular approach, but generally there has to be trade-offs between efficiency, static gain and number of components.

Table 2.1: Comparison of High-Voltage Step-up Converter Topologies

Characteristics[a]									
Author(s)	**VS**	**G**	**NS**	**ND**	**NC**	**NI**	**AT**	**DR**	**Freq.**
Interleaving Techniques									
Garth et al. (1971)	V_o	$\left(\frac{1}{1-D}\right)$	N	N	1	N	–	$0 < D < 1$	Nxf_s
Jang et al. (2004)	$V_o/_2$	$\left(\frac{4}{1-D}\right)$	2	2	2	2	1	$0 < D < 1$	$f_s/_2$
Gustavo et al. (2010)	$\frac{V_o}{2nk+1}$	$\left(\frac{2nk+1}{1-D}\right)$	2	$2nk+2$	$2nk+1$	2	–	$0.5 < D < 1$	$f_s/_2$
Park et al. (2011)	$\frac{V_o}{2NP+1}$	$\frac{D\alpha-\alpha+\sqrt{\alpha(D^2\alpha-2D\alpha+\alpha+2\beta+2\beta N)}}{\beta}$	$2NP$	$2NP$	NP	$2NP$	–	$0 < D < 1$	$f_s/_2$
Coupled-Inductor Based Converters									
Zhao et al. (2003)	$\frac{V_o}{(1+n-D)}$	$\left(\frac{(n+1-D)}{1-D}\right)$	1	2	2	2	–	$0 < D < 1$	f_s
Tseng et al. (2004)	$\frac{V_o}{1+D.n}$	$\left(\frac{1+D.n}{1-D}\right)$	1	2	2	2	–	$0 < D < 1$	f_s
Ju-Wong et al. (2005)	$\frac{V_o}{1+VMC.n}$	$\left(\frac{1+VMC}{1-D}\right)$	1	3	2	2	–	$0 < D < 1$	f_s
Switched-capacitor-based boost converters									

Abutbul et al. (2003)	$-$	$\left(\frac{\left((n+1)-n.D\right)}{1-D}\right)$	$N+2$	$2.n+1$	$n+1$	1	$-$	$0<D<1$	f_s
Axelrod et al. (2003)	$\frac{V_o}{1+D}$	$\left(\frac{(1+D)}{1-D}\right)$	1	2	3	2	$-$	$0<D<1$	f_s
Rosas-Caro et al. (2010)	$\frac{V_o}{n}$	$\frac{N}{1-D}$	1	$2N+1$	$2N+1$	1	$-$	$0<D<1$	f_s
Tang et al. (2014)	$\frac{2V_o}{3+D}$	$\frac{3+D}{1-D}$	2	$2.n+1$	$2.n$ $+1$	2	$-$	$0<D<1$	f_s

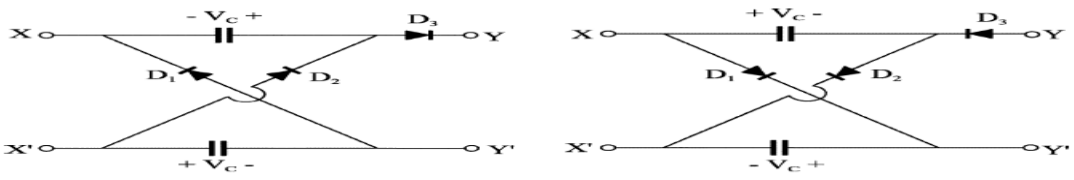
[a]*Characteristics: Voltage Stress across the Switch(es) (**VS**), Static Gain (**G**), Number of Switches (**NS**), Number of diodes (**ND**), Number of Capacitors (**NC**), Number of Inductors (**NI**), Auxiliary Transformers (**NT**), Duty cycle Range (**DR**), Operating Frequency (**Freq**.).*

CHAPTER 3

POWER CIRCUIT DESCRIPTION, DEVELOPMENTS AND THE SIMULATION RESULTS

3.1 Switch-Capacitor Circuit (SC cell)

In this design process, we considered two switching capacitor circuits shown in Figure 3.1. Depending on whether the input-output voltage polarity is opposite or positive it is categorized as inverting and non-inverting sc cells. This cell comprises of three diodes and two similar capacitors. By employing these SC cells three hybrid PWM converters are developed by modifying the existing conventional dc-dc converters (Zeta-Sepic-Cuk) (Dongyan Zhou, Andzrej Pietkiewicz, 1999; Jozwik & Kazimierczuk, 1989). These are the Cuk-Derived Converter Zeta-Derived Converter and Sepic-Derived Converter and. All of these new converters function as a voltage divider. For the purpose of analysis, following assumptions are made: 1) The components are all operating under ideal situation and 2) the voltages around he capacitors are constant during the switching period T_s.



(a) Non-inverting Circuit (b) Inverting Circuit

Figure 3.1: Switch-Capacitor Cell

3.2 Zeta-Derived Converter

This converter topology is obtained by modifying the conventional Zeta converter. The hybrid Zeta-derived topology is shown in Figure 3.2. This circuit is achieved by using the noninverting SC cell shown in Figure. 3.1(a) to replace the capacitor C, output capacitor and the output inductor of the conventional Zeta circuit. This arrangement enhances the operational performance of the Zeta converter.

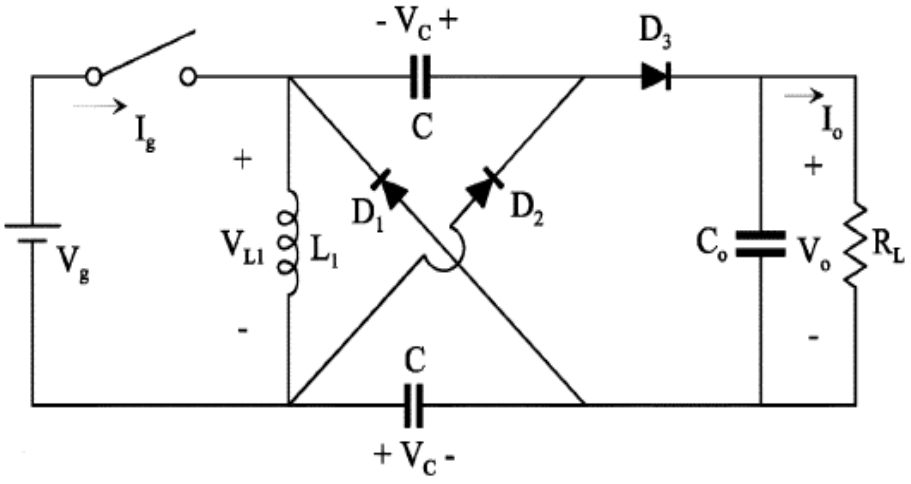
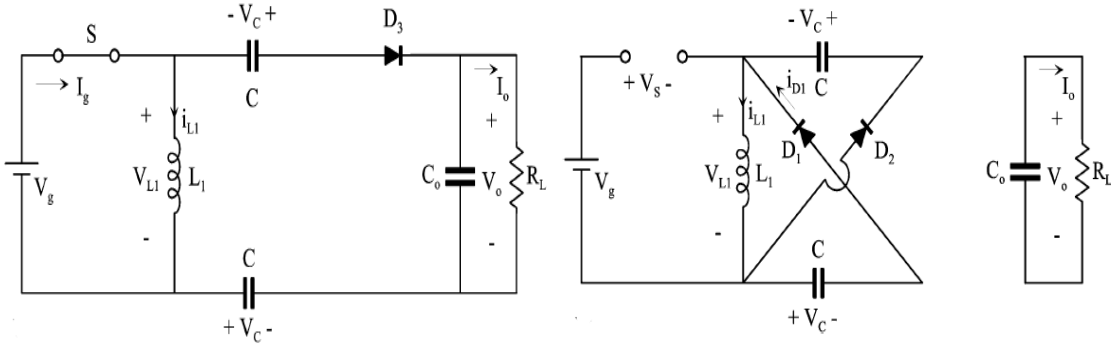


Figure 3.2: Zeta-Derived Converter

Assuming a negligible current ripple via the inductor L_1, following switching conditions occurred: During the switching-on period; the circuit behaves as in Figure 3.3(a) in which both diodes D_1 and D_2 are turned off due to the negative voltage $-(V_C + V_g)$ across them. While the output diode D_3 is turned on. Hence, the load R_L and the output capacitor C_o are being charged by the series capacitors. On the other hand, during the switching-off period; the circuit behaves as in Figure 3.3(b) where the negative voltage $(V_C - V_o)$ turns the diode D_3 off, while D_1 and D_2 turned on. Both capacitors C are being charged up by $\frac{1}{2} i_{L1}$ each, while current I_o is being supplied to the load by discharging C_o.



(a) Switch-on topology (b) Switch-off topology

Figure 3.3: Topological stages for the converter switching

During T_{on}, the capacitors' C voltage is given by

$$V_C = \frac{1}{2}(V_o - V_g) \tag{3.1}$$

By applying voltage-balance on the input inductor, we get

$$V_C = \frac{DV_g}{1-D} \tag{3.2}$$

Substituting (3.2) in to (3.1) the voltage conversion ratio G is obtained as follows

$$\frac{DV_g}{1-D} = \frac{1}{2}(V_o - V_g)$$

$$\frac{V_o}{V_g} = \frac{2D + (1-D)}{1-D}$$

$$G = \frac{V_o}{V_g} = \frac{(1+D)}{(1-D)} \tag{3.3}$$

Accordingly, the voltage stress across the switch G_S

$$G_S = \frac{V_S}{V_o} = \frac{(1+G)}{2G} \tag{3.4}$$

It can be easily deduced from (3.3) and (3.4) that the voltage gain of this hybrid Zeta converter is greater than that of the classical Zeta converter; $^{D}/_{1-D}$, and also as compared to that of classical Zeta converter i.e $^{(1+G)}/_{G}$. the voltage stress across the switch is reduced by half.

3.3 Sepic-Derived Converter

Employing a similar principle, another high voltage converter topology is obtained by modifying the conventional Sepic converter. This converter topology is shown in Figure 3.4. the noninverting SC is achieved using cell shown in Figure. 3.1(a). The switching topologies are shown in Figure 3.5.

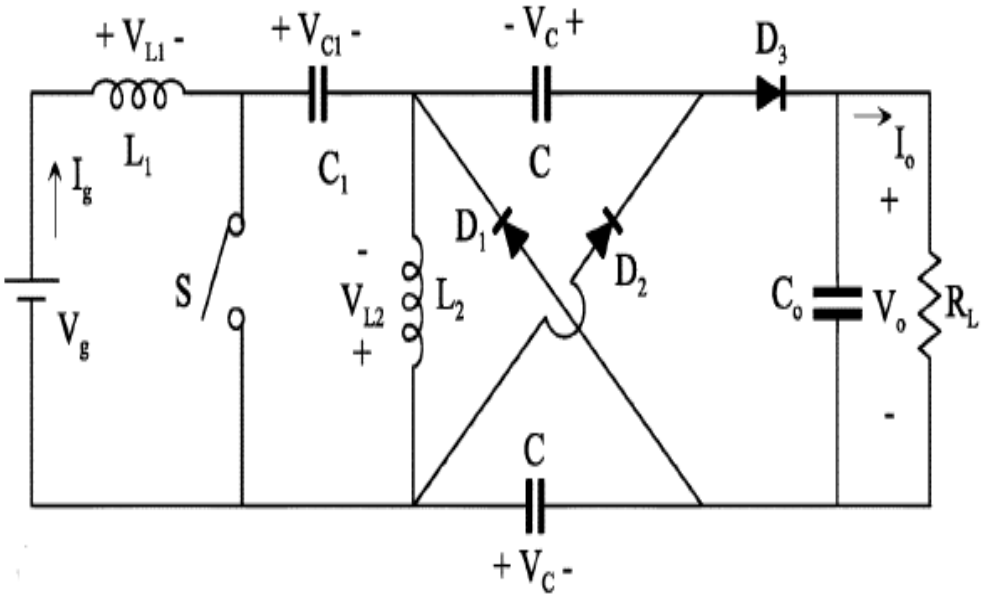
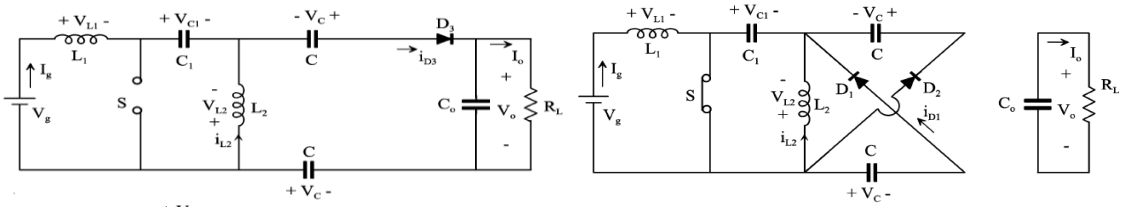


Figure 3.4: Sepic-Derived Converter

Assuming a negligible current ripple via the input inductor L_1, following switching conditions occurred: As the switch is turned on the circuit behaves as in Figure 3.5(a) where diodes D_1 and D_2 are turned on at the same time. While the negative voltage $(V_g - V_o)$ across the output diode D_3 turned the diode off. Hence, in this interval Both series capacitors C are being charged up, while current I_o is being supplied to the load R_L by discharging C_o.When the switch is turned off, the circuit behaves as in Figure 3.5(b) where the negative voltage $(V_g - V_o)$ across the diodes D_1 and D_2 turned them off. While i_{L1} forward biased diode D_3 and is turned on. Therefore, the output capacitor is being charged up and the series capacitors are being discharged.



(a) Switch-off topology (b) Switch-on topology

Figure 3.5: Switching Topologies

Implying from Figure. 3.5 and applying volt-second balance on input inductor L_1 gives

$$DV_g = (1 - D)(V_o - 2V_C). \tag{3.5}$$

During the switch-on interval

$$V_C = V_g. \tag{3.6}$$

Substituting (3.5) in to (3.6) the voltage conversion ratio G is obtained as follows

$$DV_g = (1 - D)\big(V_o - 2V_g\big).$$

$$(1 - D)V_o = V_g(D + 2(1 - D)).$$

$$\frac{V_o}{V_g} = \frac{D + 2(1 - D)}{1 - D}$$

$$G = \frac{V_o}{V_g} = \frac{(2-D)}{(1-D)} \tag{3.7}$$

Accordingly, the voltage stress across the switch G_S

$$G_S = \frac{V_S}{V_o} = \frac{(G-1)}{G} \tag{3.8}$$

3.4 Cuk-Derived Converter

In similar passion, this converter topology is also obtained by modifying the classical Cuk converter. The Zeta-derived structure is shown in Figure 3.6. This circuit is obtained by using inverting SC cell shown in Figure. 3.1(b) to replace the immediate capacitor C, the output inductor and output capacitor of the conventional Cuk circuit. This arrangement enhances the operational performance of the Zeta converter. During its operation the capacitors' connection changes from parallel to series.

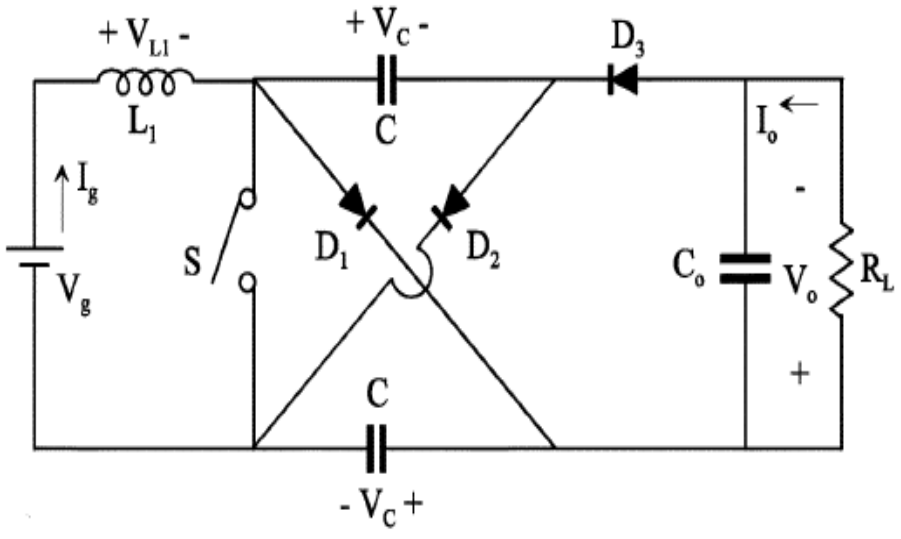
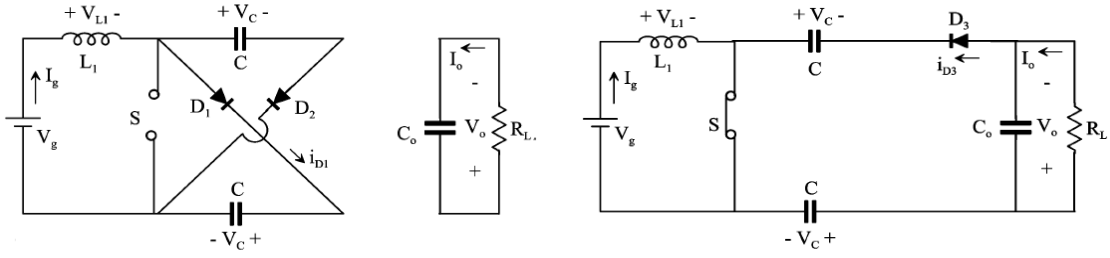


Figure 3.6: Cuk-Derived Converter

Assuming a negligible current ripple via the inductor L_1, following switching conditions are achieved: During the switching-on period; the circuit behaves as in Figure 3.7(a) where both diodes D_1 and D_2 are turned off due to the negative voltage $-V_C$ across them. While the output diode D_3 is turned on. Hence, in this interval the load R_L and the output capacitor C_o are being charged up by the series capacitors.

On the other hand, during the switching-off period; the circuit behaves as in Figure 3.7(b) where the negative voltage $(V_C - V_o)$ turns the diode D_3 off, while D_1 and D_2 turned on forming path for the current I_g. Both capacitors C are being charged up by $\frac{1}{2}I_g$ of the input current each, while current I_o is being supplied to the load by discharging C_o.



(a) Switch-off topology. (b) Switch-on topology.

Figure 3.7: Topological stages for the Switching.

During T_{on}, the capacitors' C voltage is given by

$$V_C = \frac{V_o}{2} \tag{3.9}$$

By applying voltage-balance on the input inductor, we get

$$V_C = \frac{V_g}{1-D} \tag{3.10}$$

from (3.9) and (3.10) the voltage conversion ratio G is obtained as follows

$$\frac{V_g}{1-D} = \frac{V_o}{2}$$

$$G = \frac{V_o}{V_g} = \frac{2}{(1-D)} \tag{3.11}$$

Accordingly, the voltage stress across the switch G_S

$$G_S = \frac{V_S}{V_o} = \frac{1}{2} \tag{3.12}$$

It can be easily observed from (3.11) and (3.12) that the voltage gain of this high voltage Cuk converter is higher than that of the classical Cuk converter which is $D/1-D$, and also the voltage stress across the switch is constant.

For the purpose of comparison, the new converters are compared with their classical counterparts. This is shown in Table 3.1.

Table 3.1: Comparison between the New Converters and the Classical Topologies

Converter Topologies	**Voltage Conversion Ratio** $\mathbf{G = {V_o}/{V_g}}$	**Switch Voltage Stress** $\mathbf{Gs = {V_s}/{V_s}}$
Classical Zeta Converter	$\frac{D}{(1-D)}$	$\frac{(1+G)}{G}$
High-Voltage Zeta-derived Converter	$\frac{(1+D)}{(1-D)}$	$\frac{(1+G)}{2G}$
Classical Sepic Converter	$\frac{D}{(1-D)}$	$\frac{(1+G)}{G}$
High-Voltage Sepic-derived Converter	$\frac{(2-D)}{(1-D)}$	$\frac{(G-1)}{G}$
Classical Cuk Converter	$\frac{D}{(1-D)}$	$\frac{(1+G)}{G}$
High-Voltage Cuk-derived Converter	$\frac{2}{(1-D)}$	$\frac{1}{2}$

3.5 Simulation Results

To validate the theoretical results a simulation is conducted using PSCAD/Simulink software. For the purpose of this simulation the converter parameters are chosen arbitrarily. The Simulink models of the Zeta-derived, Sepic-derived and Cuk-derived converter topologies are shown in Figure 3.8, Figure3.10 and Figure 3.12 respectively.

In Figure 3.9 the capacitor and voltage the input/output voltages waveforms for the Zeta-derived converter are shown. The waveforms indicated that both equations (3.2) and (3.3) which suggested that the output voltage $V_o = 2V_c + V_g$ are considerably fulfilled. In a similar passion, the output voltage and the capacitor voltage waveforms for the Sepic-derived converter topology are shown in Figure3.11. Similarly, the waveforms has shown that both equations (3.6) and (3.7) are approximately fulfilled. Finally, the capacitor voltage and the output voltage waveforms for the Cuk-derived converter structure are shown in Figure3.13. Furthermore, the waveforms have shown that both equations (3.10) and (3.11) in which $V_o = 2V_c$ are approximately fulfilled.

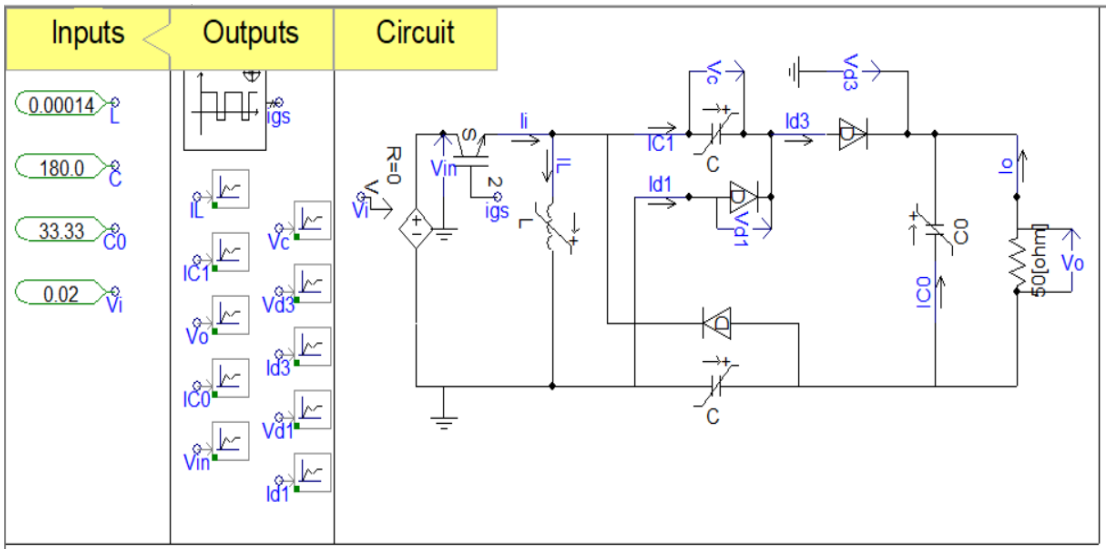


Figure 3.8 Zeta-derived Converter PSCAD Model

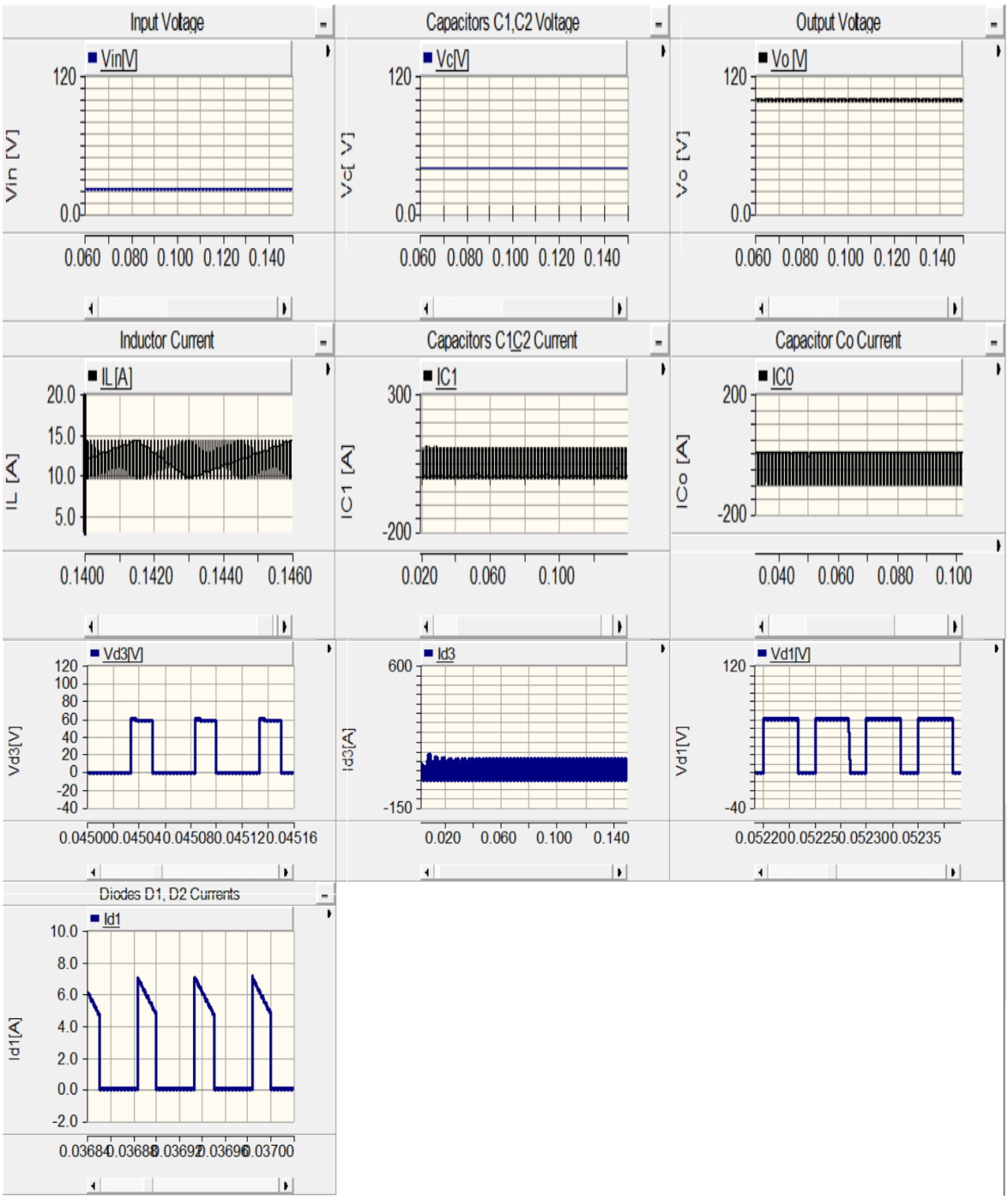


Figure 3.9: Zeta-derived Converter Voltages and Currents. Circuit Parameters: $V_{in} = 20V$, $f_s = 20kHz,\ D = 0.67, L_1 = 14\mu H, C_{1a} = C_{1b} = 180\mu F, C_o = 33.3\mu F, R = 50\Omega$.

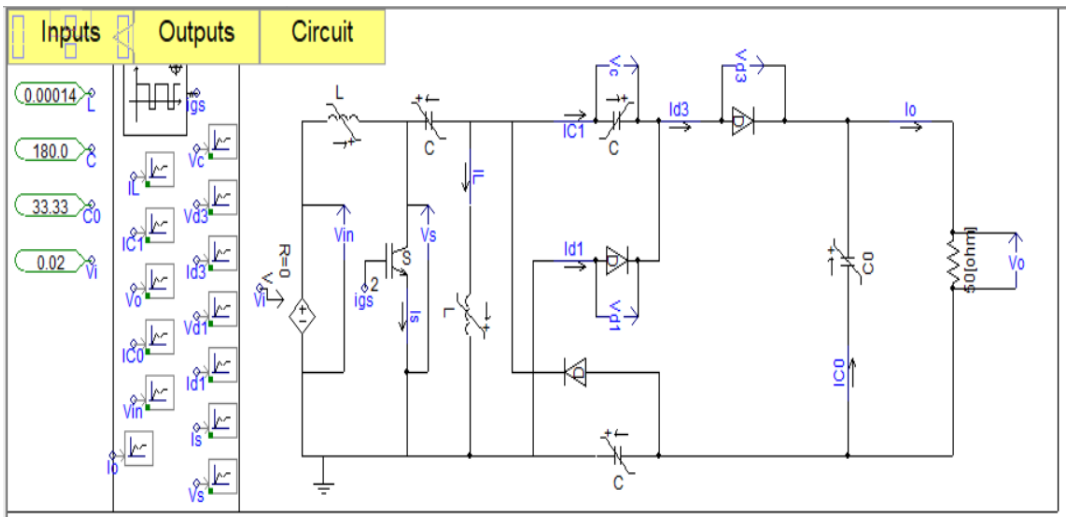


Figure 3.10: Sepic-derived Converter PSCAD Model

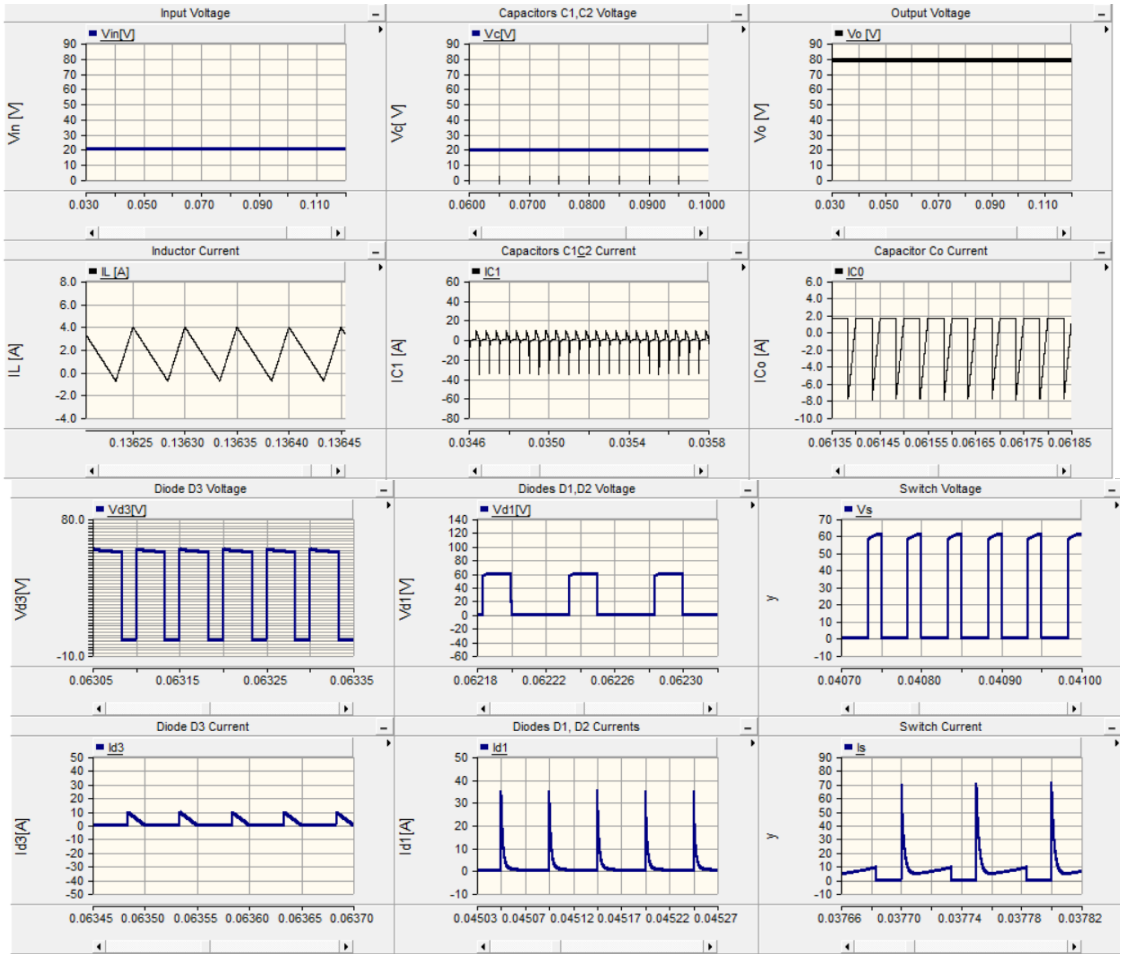


Figure 3.11: Sepic-derived Converter Voltages and Currents.Circuit Parameters: $V_{in} = 20V$, $f_s = 20kHz,\ D = 0.67, L_1 = 14\mu H, C_{1a} = C_{1b} = 180\mu F, C_o = 33.3\mu F, R = 50\Omega$.

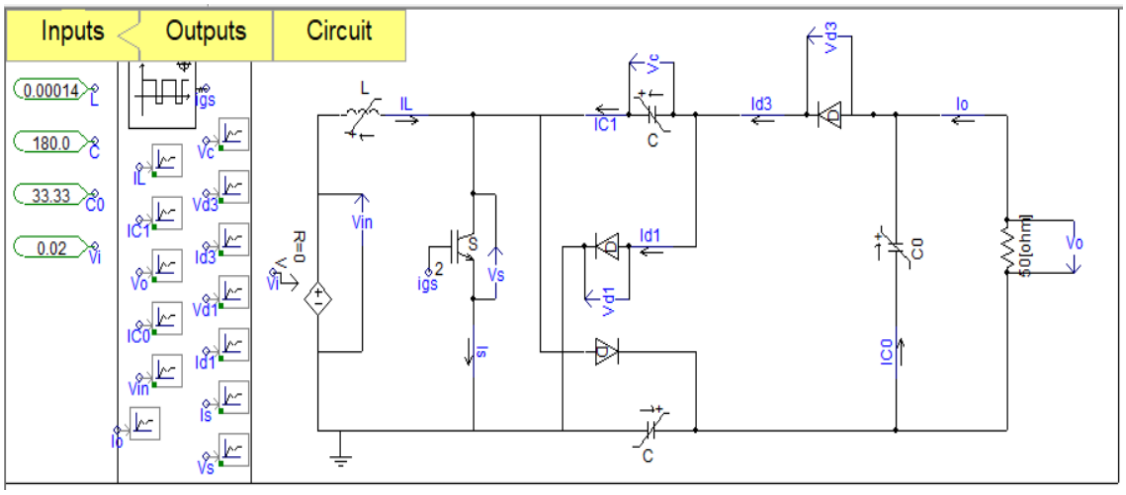


Figure 3.12: Cuk-derived Converter PSCAD Model

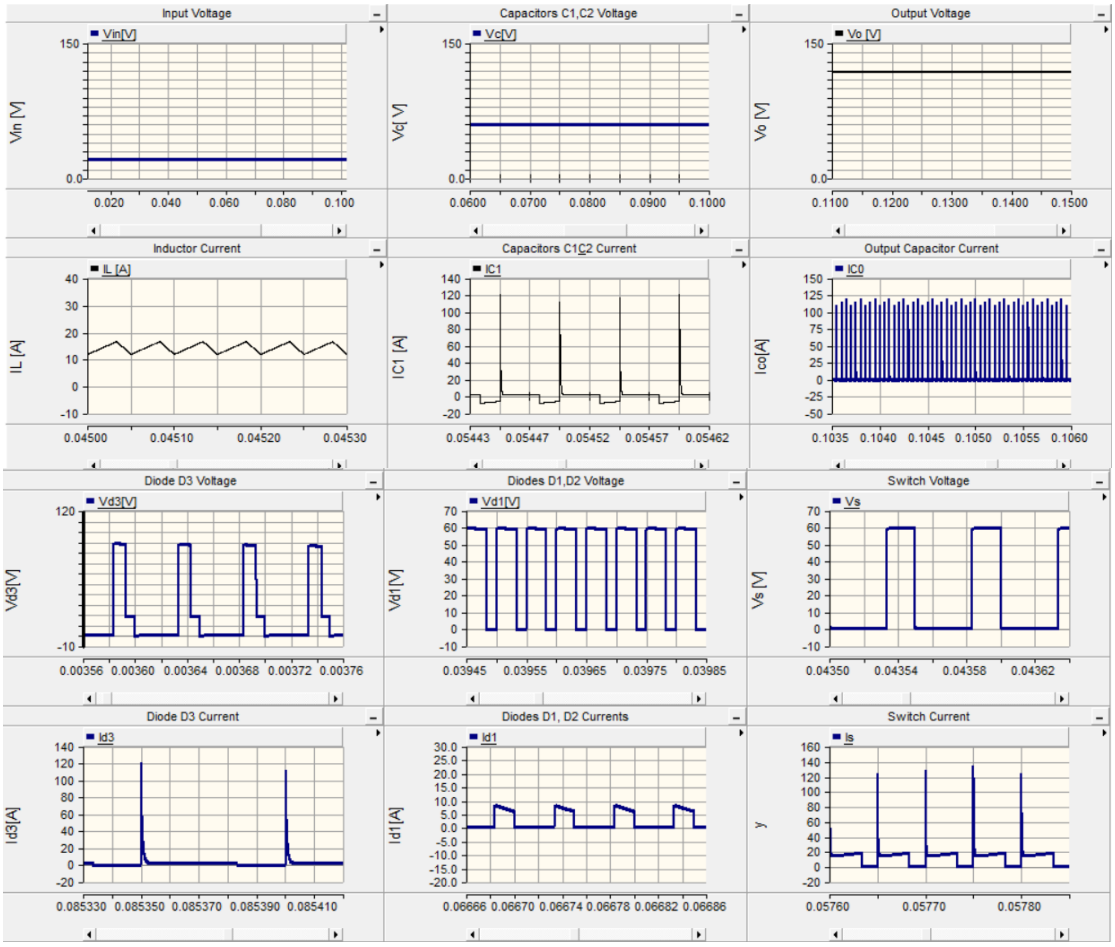


Figure 3.13: Cuk-derived Converter Voltages and Currents. Circuit Parameters: $V_{in} = 20V$, $f_s = 20kHz,\ D = 0.67, L_1 = 14\mu H, C_{1a} = C_{1b} = 180\mu F, C_o = 33.3\mu F, R = 50\Omega$.

This chapter has described the design procedure and principle of operation of the new derived converters. The theoretical analysis of the new converter circuits has been carried out. To validate our theoretical result a simulation is conducted using PSCAD. For simplicity the simulation evaluation is limited to validating the theoretical results with respect to voltage ratios. A comparison is made between the new converters and their conventional counterparts based on the theoretical results, in all the three cases a significant improvement has been identified

CHAPTER 4

CONCLUSIONS AND RECOMMENDATIONS

4.1 Conclusions

The basic Zeta, Sepic and Ćuk dc-dc converters have over long period gained popularity in many low-power applications that requires no isolated dc-dc converters. They operate in either step up or step-down mode based on the value of their duty ratio D. Their main property is a voltage conversion ratio given by $D/1-D$.

Recently, many applications such as communication, X-ray power generators, high-intensity-discharge (HID) lamps for automobile headlamps to mention few requires very high DC voltage conversion ratio bigger than that produced by the classical converters. Forcing the duty cycle to very large values in order to achieve the requirement is unrealistic as it will affect the diode recovery, and introduces large EMI emission. Furthermore, owing to the fact that diode's commutation time would take all the duration for its conduction $(1-D)T_S$ operating at high frequencies is not feasible. By using transformers, the DC voltage-gain can be improved, but this would increase the size and incur additional losses. Cascading the converters in quadratic structure would provide solution, however, the product term in their efficiency have made them less efficient. The introduction of switched-capacitor-based DC converters has paved a way for obtaining higher DC voltage-ratios.

A new group of three single-switch PWM high-voltage dc-dc converters have been presented in this thesis. The introduced converter topologies were obtained by modifying the basic Zeta, Sepic and Cuk converter circuits with a switched-capacitor arrangement. The switched capacitor cell is made by replacing the rectifier diode with two diodes and splitting the energy transfer capacitor in to two, from the conventional Zeta, Sepic and Cuk converters. Meanwhile, the new converter topologies act as voltage-divider-circuit, where the energy-transfer capacitors C are charged when the diodes D_1 and D_2 are turned on and when D_1 and D_2 are reversed biased the capacitors discharges in series.

The analysis of the introduced converters' operation in continues conduction mode is presented. A simulation is conducted on the converter circuits using PSCAD software to support the theoretical facts. Both the theoretical and the simulation results indicated that the new converter topologies provide higher DC-voltage-ration when compared with canonical Zeta, Sepic and Cuk converters. Furthermore, there is no need for additional processing of the energy due to the fact that the incorporated switched-capacitor cell splits the energy transfer, this result in significant increase in efficiency.

The presented converter structures give considerable savings in weight, cost and size. Although, the presented converters are faced with pulsating output currents problem, nevertheless, they are suitable for applications where extremely high-voltage output is the priority with small output current.

4.2 Recommendations

To achieve higher voltage-gain for the same duty cycle, the switched-capacitor cell can be structured for n diodes and capacitors. The efficiency can also be improved by using soft-switching techniques to reduce switching stress and losses, proper selection of capacitors with smaller ESR. Furthermore, to alleviate the problem of output voltage ripples it is recommended that an additional LC-type low-pass high-frequency filter be incorporated to further reduce the ripples. The supplementary filter together with the output capacitor will provide meaningful noise attenuation.

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