DC-DC BOOST CONVERTER BASED ON THREE Z-SOURCE NETWORKS

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

By
MOHAMED A. KHALIFA AWELI

In Partial Fulfilment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

NICOSIA, 2019

MOHAMED A. KHALIFA AWELI
DC-DC BOOST CONVERTER BASED ON THREE Z-SOURCE NETWORKS
NEU 2019

DC-DC BOOST CONVERTER BASED ON THREE Z-SOURCE NETWORKS

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

By
MOHAMED A. KHALIFA AWELI

In Partial Fulfilment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

NICOSIA, 2019

MOHAMED A. KHALIFA AWELI: DC-DC BOOST CONVERTER BASED ON THREE Z-SOURCE NETWORKS

Approval of Director of Graduate School of Applied Sciences

Prof. Dr. Nadire CAVUS

We certify this thesis is satisfactory for the award of the degree of Master of Science in Electrical and Electronic Engineering

Examining Committee in Charge:

Assist. Prof. Dr.Parvaneh Esmaili	Committee Chairman, Department of Electrical and Electronic Engineering, Engineering, NEU
Prof. Dr. Ebrahim Babaei	Supervisor, Department of Electrical and Computer Engineering, University of Tabriz-Iran
Assist. Prof. Dr. LidaVafaei	Department of Mechanical Engineering, NEU

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name: Mohamed A. Khalifa Aweli

Signature:

Date:

ACKNOWLEDGEMENTS

I would like to express my deep and sincere gratitude to my research supervisor, Prof. Dr. Ebrahim Babaei, Near East University, Northern Cyprus, for giving me the opportunity to conduct this research by providing invaluable guidance throughout the process. His dynamism, vision, sincerity and motivation have deeply inspired me. He has taught me the methodology to carry out the research and to present the research works as clearly as possible. It was a great privilege and honor to work and study under his guidance. I am extremely grateful for what he has offered. I would also like to thank him for his friendship, empathy, and great sense of humor.

I would also like to take the time to thank my friends and family for their immense contribution, suggestions and moral support. I would also like to thank my examination committee for taking their time to review my thesis.

I am extremely grateful to my parents for their love, prayers, caring and sacrifices while educating and preparing me for my future. Also, I will like to express my thanks to my brothers and sisters, for their support and valuable prayers.

To my beloved parents…

ABSTRACT

This thesis presents a design and simulation of dc-dc boost converter based on three active Z-source networks. Contrary to conventional Z-networks that usually contain passive elements, this converter contains active Z-networks. The converter retains all the advantages of classical Z-source converters including high voltage gain and it can also operate in both normal (continuous conduction mode) and abnormal (discontinuous conduction mode) load conditions. Another salient feature of this converter circuit is that only one switching device is used. The presented converter circuit is realized by adding three Z-source networks to conventional boost converter, Z-network 1 and Z-network act as the first and second boost stages respectively, while Z-network 2 which contains the switching device serves as the switching stage. A comprehensive description and analysis of the power circuits are presented. The analysis of the converter has been conducted under six modes of operation depending on the switch and diodes conditions. These operational modes are grouped into six cases depending on the inductor and capacitor currents; consisting of two continues current mode (CCM) and four discontinues modes (DCM). The converter circuit is simulated using PSCAD/EMTDC package. This converter topology provides reduction in voltage stress and increase in efficiency. It may be used to produce high voltage gain required for many industrial applications especially renewable energy systems.

***Keywords*:** Dc-dc converter; Z-source network; Boost converter; Renewable energy; Photovoltaic (PV) arrays; Fuel cell; PSCAD/EMTDC package

ÖZET

Bu bitirme tezi, üç aktif Z-kaynak şebekeye bağlı olarak, doğruakım-doğruakım yükseltici çevirgecin tasarım ve simulasyonunu sunmaktadır. Bu çevirgeç, pasif elemanlar içeren konvansiyonel Z-şebekelerin aksine bu çevirgecin aktif Z-şebekelerini içermesi yönüyle benzersizdir. Çevirgeç; yüksek gerilim kazanımı dahil olmak üzere, klasik Z- kaynak çevirgeçlerinin tüm avantajlarını sürdürmekte ve ayrıca normal (sürekli iletme modu) ve anormal (sürekli olmayan iletme modu) yükleme şartlarında çalışabilmektedir. Bu çevirgeç devrenin diğer bir dikkat çekici özelliği, burada sadece birtek anahtarlama cihazının kullanılmasıdır.

Sunulan çevirgeç devre; üç adet Z-kaynak şebekenin, yükseltici çevirgece eklenmesiyle, Z- şebeke 1 ve Z-şebekenin sırasıyla birinci ve ikinci yükseltici safhaları olarak hareket etmesiyle gerçekleştirilmekte ve anahtarlama cihazı içeren Z- şebeke 2 de anahtarlama safhası olarak hizmet vermektedir. Güç şebekelerinin kapsamlı açıklaması ile durağan durum analizi sunulmaktadır. Çevirgecin durağan durum analizi; anahtar ve diyot şartlarına bağlı olarak, altı kullanma modu altında yapılmıştır. Bu kullanma usulleri, indüktör ve kapasitör akımlarına bağlı olarak altı vaka şeklinde gruplandırılmıştır. Bu altı vakadan ikisi sürekli iletme moduna (CCM) tekabül ederken geriye kalan dört vaka da sürekli olmayan iletme moduna (DCM) tekabül etmektedir. Kuramsal analizi tümlemek için, devre bir model üzerinde PSCAD/EMTDC paket programı kullanılmak suretiyle simülasyon uygulanmıştır.

Bu çevirgeç ilingepoloji, gerilim zorlamada düşüş ve verimde de artış sağlamaktadır. O, şebekeye bağlanan çevirgeçlerde, fotovoltaik diziler (PV) ve yakıt hücreleri gibi temiz kaynaklardan düşük gerilimin yüksek gerilime artırılması amacıyla, birçok endüstriyel uygulamada ve özellikle yenilenebilir enerji sistemlerinde gerekli olan yüksek gerilim kazanımına erişebilmektedir.

***Anahtar Kelimeler*:** Doğru akım – doğru akım çevirgeci; Z-kaynak şebekesi; Yükseltici çevirgeç;Yenilenebilir Enerji; Fotovoltaik (PV) diziler; Yakıt hücreleri; PSCAD/EMTDC Paket programı

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AC:	Alternating Current
CCM:	Continuous Conduction Mode
CIBC:	Coupled-Inductor Based Converters
DCM:	Discontinuous Conduction Mode
DC:	Direct Current
IBC:	Interleaved Boost Converters
PSCAD:	Power System Computer Aided Design
PV:	Photovoltaic
PWM:	Pulse Width Modulated
SCBC:	Switched-Capacitor Based Converters
UPS:	Uninterruptible power systems
ZS:	Impedance source

CHAPTER 1

INTRODUCTION

1.1 Introduction

The demand of DC-DC boost converters is increasing exponentially with increase of power electronics technology-based applications in industries. For instance, in renewable power systems boost dc-dc converters are needed to step up the low voltages obtained from clean sources to higher voltages for grid-connected inverters (Wuhua Li, Liu, Wu, & He, 2007). Other applications where dc-dc boost converters are of paramount importance include servo-motor drives, energy backup un-interruptible power systems (UPS), automobile head lamps, communication systems, to mention but few (Ismail, Al-Saffar, Sabzali, & Fardoun, 2008). A regular prerequisite for the aforementioned implementations is the evolvement of a greater performance in powerful boost converters. These made boost converters an interesting area of research where many proposed circuits have been introduced to sustain and satisfy the specifications requirements.

From theoretical perspective, infinite gain and very high efficiency can be obtained from ideal conventional boost converters. This is not feasible in practical because of the power losses and parasitic nature of their components. Moreover, the current semiconductor fabrication technologies have not succeeded in producing cost-effective switches and diodes that can withstand the voltage stress of conventional dc-dc converters, which again limits the practical applicability of the converters. From the practical point of view, the highest available voltage gain from these conventional converters is far less than applications' requirements. The maximum attainable voltage gain with traditional boost dc-dc converters is within the range of 5-6 multiple of input voltage (Al-Saffar, Ismail, & Sabzali, 2013; Choi & Lee, 2012; Tsai et al., 2011).

Cascading technique appeared to provide a solution to acquire the required voltage gain. In this technique a number of boost converters are connected in series with output of one converter serving as input to the next converter. The most popular converter topology based on this method are quadratic converters (Feng, Liu, & Lee, 2002), a control circuit

and two switches are used, but still the voltage gain is insufficient. There are many improved versions of cascaded converters like quadratic power converter (Wijeratne & Moschopoulos, 2012), boost converters with Cockroft-Walton voltage multiplier, and various interleaved boost converters with current ripples reduction (Henn, Silva, & Prac, 2010; Weichen Li, Xiang, Li, Li, & He, 2013; Wuhua Li et al., 2013). However, these converters become more complicated because of the additional control circuits and switching devices, these reduces the overall system reliability and efficiency in addition to increase in the cost (Wildrick, Lee, Cho, & Choi, 1995). To address the problems isolation transformer with turn-ratios have been used in the circuits, although the circuit's reliability and gain are improved but presence of transformer increases losses which reduces the efficiency and also there is a considerable increase in circuit volume and weight (Cacciato, Consoli, Attanasio, & Gennaro, 2010).

Peng introduced a unique converter topology using an LC network named Z-network, to serve as interface between the DC source and the converter. This network solved consists of symmetrical passive components connected in X-shape. The new source differs from the conventional sources and is popularly known as Z-source (Peng, 2003a). Z-source technique has solved many of the limitations of conventional converters and exhibit unique features for instance, it provides a high output-voltage, and can handle a current shoot-through problem. Consequently, Z-source strategy has been applied in DC-DC converters to achieve broader output voltage. Peng has presented a number of Z-source circuits (Ge, Lei, Qian, & Peng, 2012; Rosas-Caro, Peng, Cha, & Rogers, 2009) with their associated control strategies (Y. Li, Jiang, Cintron-Rivera, & Peng, 2013; Shen et al., 2006). Thereafter, many Z-source circuits with high voltage gain have been presented in the literature with a considerable number of advantages (Galigekere & Kazimierczuk, 2012; D. Li, Loh, Zhu, Gao, & Blaabjerg, 2013; Qian, Peng, & Cha, 2011; Vinnikov & Roasto, 2011). Nevertheless, the output-voltage of these Z-source converters is not sufficient for many industrial applications, which make the case of improving converter gain still open.

1.2 Motivation

Nowadays, renewable energy systems have dominated and replaces other energy sources due to its economic and environmental importance. In this system boost dc-dc converters are needed to step up the low voltages obtained from source to higher voltages for grid-

connected converters. Due to the instability in the energy source for example in photovoltaic energy systems, load conditions become abnormal in some interval corresponding to discontinuous conduction mode (DCM), therefore the required converter should not only provide high voltage gain, but should also be able to maintain stable operation under abnormal load condition.

This thesis, present, analyse and simulate a three active Z-network boost converter, that have all the advantages of Z-source converter including high voltage gain and also have additional advantage of operating under normal (CCM) and abnormal (DCM) load conditions. Which not only have the advantages of the Z-network converters, but also can reach much higher voltage-gains.

1.3 Thesis objectives

- Power circuit description.
- Analysis of the converter operations in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) with corresponding equivalent circuits and key waveforms.
- Converter parameters design.
- Simulation of the converter circuit on PSCAD software to verify the feasibility of the converter.

1.4 Thesis significance

- A special converter with three active Z-network using single-switch
- Operates both under normal current condition (CCM) and abnormal current condition (DCM)
- The converter provides a very high gain voltage which makes it suitable for renewable power systems application particularly as a photovoltaic converter to step up low voltage from cells to high voltage for grid-connected converters.

1.5 Scope and Limitations

The analysis is carried out with assumption that all the components are operating under ideal condition. The freewheeling diodes of the switches are also ignored in the analysis. The presented converter operates in boost mode. Only simulation results are presented.

1.6 Thesis outline

The thesis report comprises of four chapters arranged as follows: Chapter one gives introduction and background of the thesis. Chapter two presents a literature review on Z-source converters. Chapter three gives the converter circuit description, CCM and DCM operation analysis, parameters design and simulation results. Finally, conclusion and recommendations given in chapter four.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The purpose of DC-DC Converters in general is to converts DC voltage from one level to another. The DC-DC converters are high-frequency power conversion circuits that use high-frequency switching and inductors, transformers, and capacitors to smooth out switching noise into regulated DC voltages. The most common topologies are the buck, boost, buck-boost and Sepic converters. A buck converter steps down a voltage, producing a voltage lower than the input voltage. On the hand, boost converter steps up a voltage, producing a voltage higher than the input voltage. A buck-boost converter steps a voltage up or down, producing a voltage equal to or higher or lower than the input voltage. A Sepic converter is used for similar applications as the buck-boost, but provides some advantages in some applications (Maker.io, 2016).

Nowadays, power electronics dc-dc converters have become popular during the last thirty years and the number of applications is increasing. This is because of their suitability in numerous equipment and systems which include; motor drives (Kim, J., Ha, K., Krishnan, 2012), uninterruptible power supply (UPS) (Abusara, M.A., Guerrero, J.M., Sharkh, 2014), X-ray power generators, electric vehicles (Yilmaz, M., Krein, 2013), and many renewable energy based systems. Basic requirement for such applications is the development of high efficiency, high performance, low cost, reduced stresses on the semiconductors, robustness and simplicity of the converters used (Ismail et al., 2008). Renewable energy power systems requires step-up converter for increasing small voltage obtained from these sources to higher voltages for grid-connected inverters (Wuhua Li et al., 2007).

Peng introduced a unique converter topology using an LC network named Z-network, to serve as interface between the DC source and the converter. This network solved consists of symmetrical passive components connected in X-shape. The new source differs from the conventional sources and is popularly known as Z-source (Peng, 2003a). Z-source

technique has solved many of the limitations of conventional converters and exhibit unique features for instance, it provides a high output-voltage, and can handle a current shoot-through problem. Consequently, Z-source strategy has been applied in DC-DC converters to achieve broader output voltage. Peng has presented a number of circuits based on Z-network (Ge et al., 2012; Rosas-Caro et al., 2009) with their associated controls strategy (Y. Li et al., 2013; Shen et al., 2006). Thereafter, many Z-network converters with high output-voltage are presented in the literature with a considerable number of advantages (Galigekere & Kazimierczuk, 2012; D. Li et al., 2013; Qian et al., 2011; Vinnikov & Roasto, 2011). Nevertheless, the output-voltage of such converters insufficient for a lot of applications, that make the case of improving converter gain still open.

The purpose of this chapter is to present a concise literature review on the major Z-source network converters, starting with basic Z-source inverter circuit. Further improvements on basic ZSI circuit are also discuss. Finally, the application of Z-source converters in renewable energy systems, particularly PV cells systems and charging of electric vehicle battery are discussed.

2.2 Z Source Inverter

The ZSI which was proposed in 2003 by (Peng, 2003b) is a power electronic converter which is mostly applied in dc – ac power conversion; it has exciting characteristics such as single stage power inversion and the buck-boost properties. The ZSI is composed of four passive components of two capacitors and two inductors designed in X structure which constitutes the impedance structure or source. The impedance structure is placed in-between the source and the main converter body hence forming the impedance source inverter. Figure 2.1 shows the basic ZSI topology which uses the shoot through state to increase the voltage gain or increase the magnitude of the source voltage; this advantage of the ZSI over other power electronic converters increases its scope of operation and reliability, produces single stage of power conversion (dc-ac), it has reduced cost, provides high efficiency, its size or volume is also reduced and has least component count. The application of ZSI in emerging energy sources such wind farms, photovoltaic systems, mini hydropower system and other current power electronic conversion systems such as

hybrid and electric cars is propitious (Ellabban & Abu-Rub, 2016; Liu, Abu-Rub, & Ge, 2014).

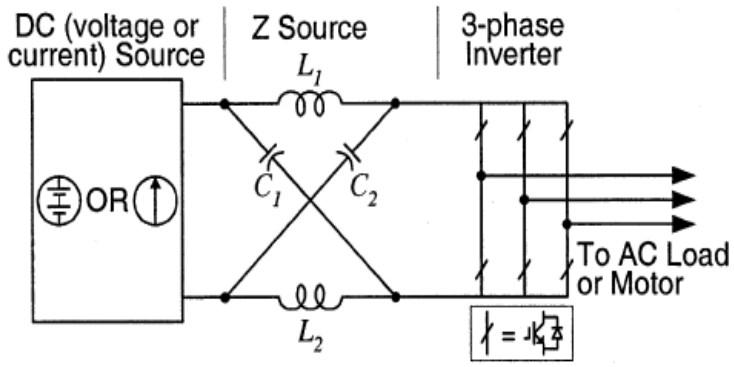
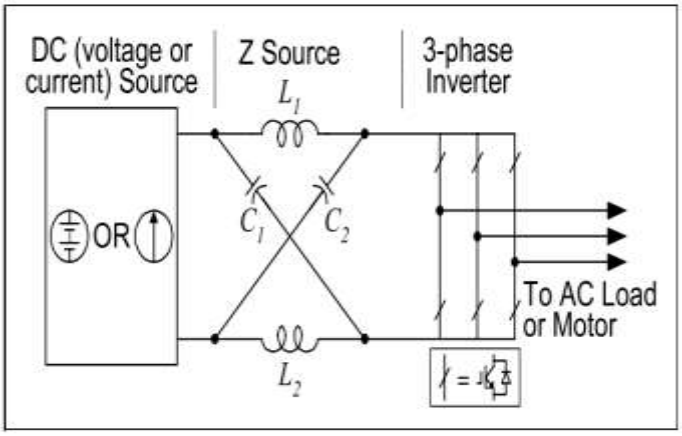
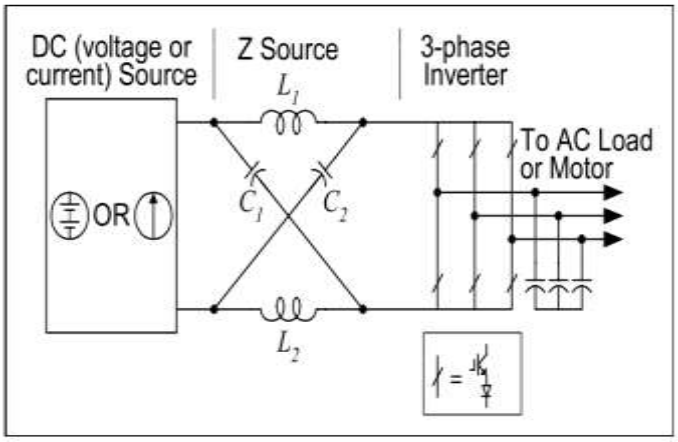


Figure 2.1: Basic ZSI structure (Peng, 2003b)

The applications of ZSI is not limited to only dc-ac conversion but can also be applied to the following types of conversion; ac-dc, dc-dc, and ac-ac. Also, the impedance network of ZSI can be placed in any converter topology where the source is either VSI or CSI where the output of the converter has multilevel waveform functionality. There are several limitations of the conventional voltage source converter or current source converters such as; application of extra converter for buck-boost functions thereby increasing the cost of the system, volume of the system also increases considerably, efficiency is adversely affected because double stage conversion increases system losses. Turning on all switches on the same phase or leg will lead to short circuit or a condition called shoot-through which leads to destruction of the converter. The conventional VSI or CSI have poor immunity to electromagnetic interference (EMI) which is one of the major causes of unintentional gating of switches. Several topologies have been developed after the basic ZSI of Figure 2.1 was presented in 2003 because of a number of drawbacks of the basic ZSI structure; there was very large inrush current during beginning of converter operation, the power flow was unidirectional due to the diode, suitable for semi heavy-load applications, the source current flow is discontinuous, higher capacitor voltage in impedance network, secluded source and inverter dc rail (Ellabban & Abu-Rub, 2016). A series or anti-parallel combination of switches and diodes can be used as shown in figure 2.2 (a) and 2.2(b) respectively.



(a)



(b)

Figure 2.2: ZS converter with anti-parallel combination (Ellabban & Abu-Rub, 2016)

Nevertheless, above ZSI circuits have some shortcomings and challenges. Such as high starting current inrush, inability to handle heavy load, input current discontinuity, power flow in one direction, reduced efficiency, to mention some. Therefore, numerous improvements have been proposed in the literature to alleviate these shortcomings of classical ZS converter topology.

2.3 Δ-Sources Network

Several impedance network topologies have been published which seeks to improve or increase the voltage gain and also reduce the passive components in the impedance

network. Answer to this is found in the coupled inductor application in Z source structures because they offer reduced cost and weight coupled with increased voltage gain at reduced component count. A new impedance network derived from the Y source structure, this topology is a novel (Δ-Source) one which provides least losses in the windings and also little magnetizing current hence productive application of the core material is gained resulting in reduced volume and weight. The cost of the Y source structure increases because of closed loop control is required to minimize the effects of leakage reactance (Hakemi, Sanatkar-Chayjani, & Monfared, 2017). The Δ-Source applies delta connection methodology in the connection of the three coupled inductors. Also, the adverse effects of leakage inductance are greatly minimized to improve the converter performance. The circuit of the proposed impedance network; Δ-Source network is shown in Figure 2.3. The shoot through and non-shoot through circuit are shown in Figure 2.4 a and b respectively.

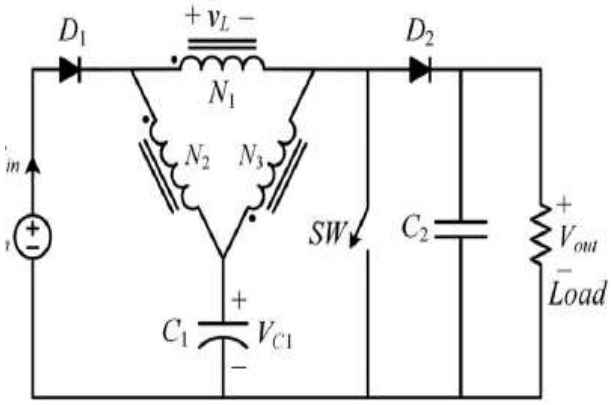


Figure 2.3: Δ-Source network (Hakemi et al., 2017)

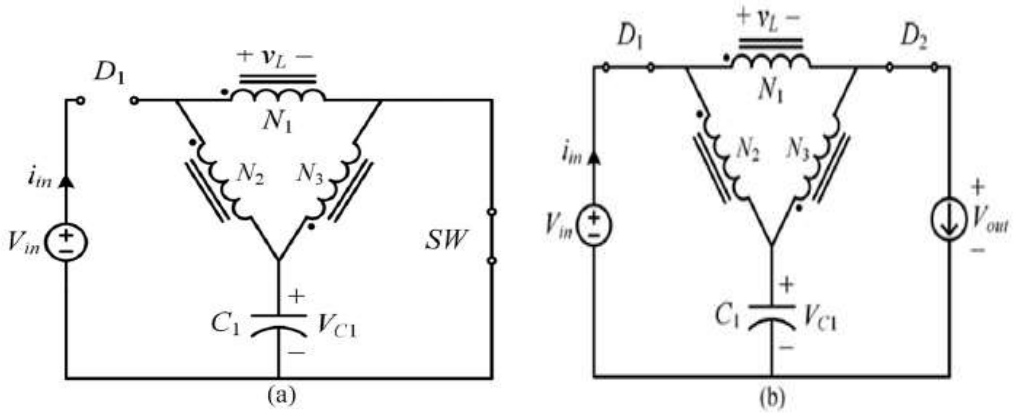


Figure 2.4: Δ-Source network (a) ST circuit (b) NST circuit (Hakemi et al., 2017)

2.4 Switched Boost Inverter

This inverter has the qualities of the traditional Z-source based inverter (ZSI) with added attributes such as reduced passive component numbers, better immunity to effects of EMIs. The circuit configuration of the switched boost inverter is shown in Figure 2.5. The impedance structure is composed of two diodes (D_a, D_b), one inductor L and capacitor C, and an active switch S. the simplicity of the proposed inverter produces a compact layout. The peak gain of the switched boost occurs at 0.5 duty cycle which is similar to that of the traditional Z source e topology. The SBI is not suitable for application where very high boost factor is required because its boost factor is 1 – D time that of the conventional Z source inverter (D. Li et al., 2013).

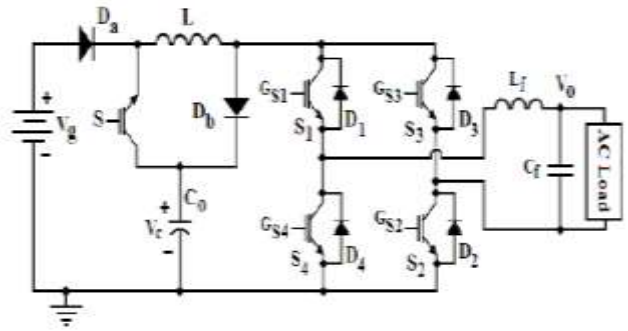


Figure 2.5: Switched boost inverter (D. Li et al., 2013)

An improved version of switched boost inverter is presented in (Tang, Zhang, & Xie, 2007). This converter topology called "current-fed switched inverter (CFSI)" possess a number of important features like; it has all the merits of basic Z-source inverter circuit as well SBI circuit. The voltage gain produce by this topology is same as ZSI and retains the component count of SBI. In addition, they have better immunity to effects of EMIs, continuous current input abilities thus suitable for renewable energy applications. The proposed CFIS structure with its corresponding shoot through waveform is shown in Figure 2.6 (a) and (b) respectively. Comparison between CFSI, SBI and ZSI is shown in table 2.1.

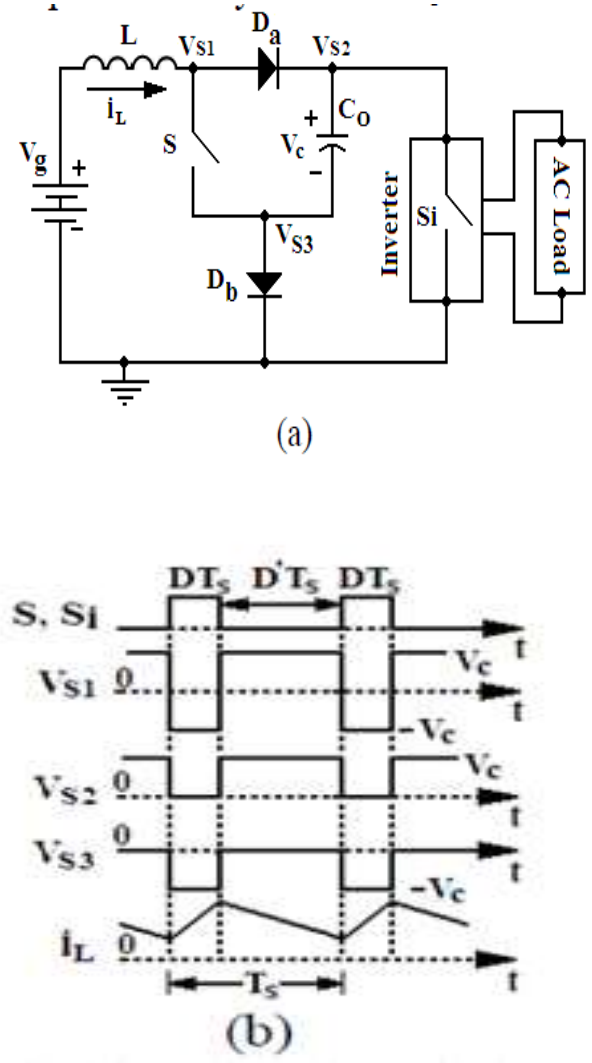


Figure 2.6: (a) CFIS circuit (b) shoot through waveform (Tang et al., 2007)

Table 2.1: Performance Comparison Boost Converter Circuits (Ellabban & Abu-Rub, 2016)

Attributes	***Boost-VSI***	***ZSI***	***SBI***	***CFSI***
No. of stages	2	1	1	1
No. of passive elements	4	6	4	4
No. of active switches	5	4	5	5
No. of passive switches	5	5	6	6
Immunity to EMI noise	no	Yes	yes	yes
Nature of input current	continuous	Discontinuous	discontinuous	discontinuous
Max. input voltage	$\frac{V_g}{(1-D)}$	$\frac{V_g}{(1-2D)}$	$\frac{(1-D)}{(1-2D)}V_g$	$\frac{V_g}{(1-2D)}$
Modulation index	$0 < m < 1$	$0 < m < (1-D)$	$0 < m < (1-D)$	$0 < m < (1-D)$

2.5 Improved Switched-Inductor based ZSI

The improved switched-inductor based ZSI is introduced to solve the drawbacks of conventional ZSI; such voltage-stress around the capacitors, limited voltage gain, high start up inrush-current and discontinuous current flow from the source. Also, a higher duty cycle corresponds to reduced modulation index hence the quality of the output voltage is greatly reduced; total harmonic distortion content is increased.

To boost the voltage gain of the ZSI topology, several different topologies have been presented to address that drawback; switched capacitor-SC, switched inductor-SL, combination of switched capacitor and switched inductor-SC-SL, voltage lift-VL, voltage multiplier. The improved switched inductor topology was proposed because the switched inductor was unable to solve the problems of large voltage-stress across the components and large inrush currents. The topology ISLZSI is hybrid between SLZSI topology and IZSI topology as shown in Figure 2.7. Figure 2.8 shows the equivalent circuits, while the two states of operations of the converter are shown in Figure 2.9 (a) and 2.9 (b).

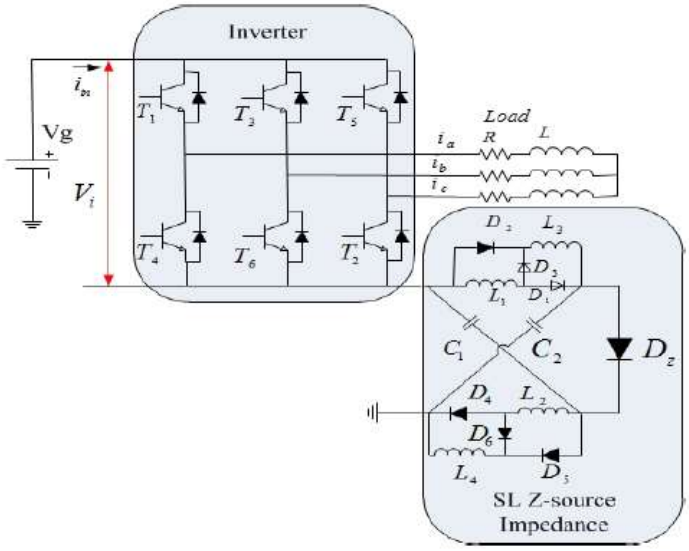


Figure 2.7: Improved SL Z source inverter (D. Li et al., 2013)

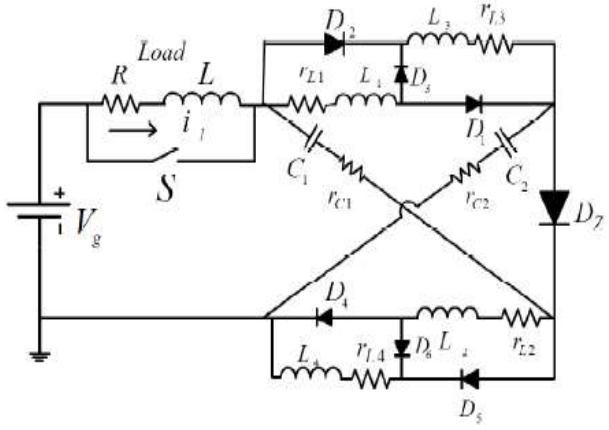


Figure 2.8: ISLZSI equivalent circuit (D. Li et al., 2013)

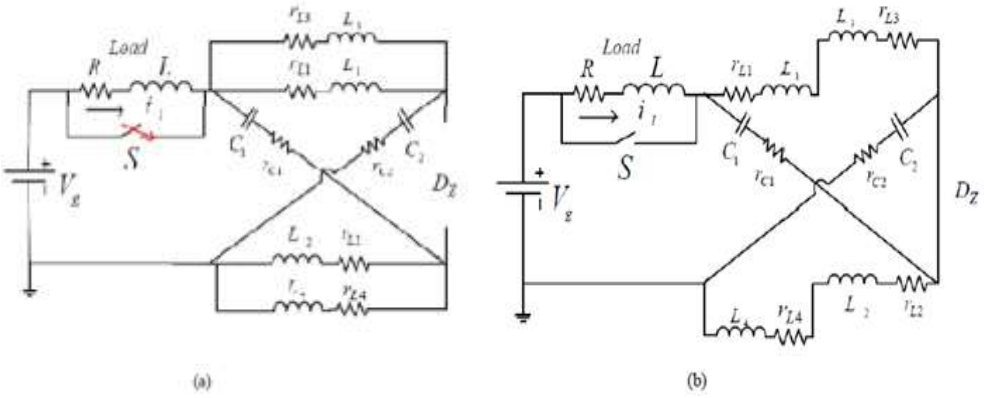


Figure 2.9: Operations states of ISLZSI topology (D. Li et al., 2013)

2.6 Enhanced Boost ZSI

A different Z source topology known as the enhanced boost ZSI. This topology is derived from the combination of two other Z source topologies. The proposed topology EB-ZSI; produce quality output waveforms because higher modulation index (reduced duty cycle) is utilized. The boost factor is also significantly improved in the EB-ZSI, also EB-ZSI use the same value of duty ratio to produce higher boost factor than qZSI topologies, switched inductor ZSI topologies, cascaded ZSI topologies (Ellabban & Abu-Rub, 2016). Again, when compared to qZSI topologies, switched inductor ZSI topologies, cascaded ZSI topologies EBZSI has lower voltage stress on passive components and switches. The inductor rating in EBZSI is minimal hence reduced system cost and reduced loses. The circuit of the proposed topology utilizes two impedance networks to achieve higher boosting factor and it's represented in Figure 2.10.

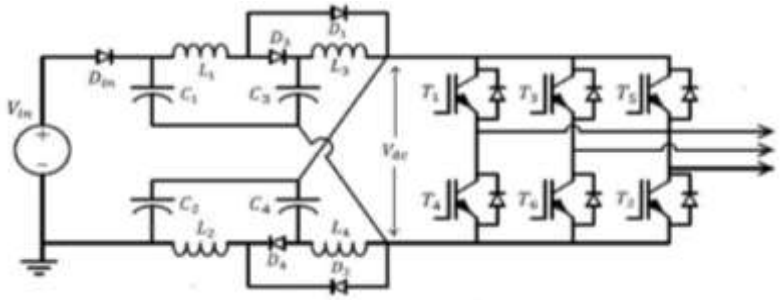


Figure 2.10: Enhanced boost ZSI (Ellabban & Abu-Rub, 2016)

The operation of EB-ZSI is similar to other impedance source topologies i.e. two states of operation exist; shoot through and non-shoot through modes. In the shoot through state Figure 2.11, all switches on any leg of the converter are concurrently switched on. Two diodes D_1 and D_2 are forward biased and two other diodes D_3 and D_4 are turned off because of negative current flowing across them. Also the input diode D_{in} is reversed biased because the capacitor voltage is greater than the source voltage V_{in}. In the non-shoot through state Figure 2.12, diodes D_1 and D_2 are reverse biased and diodes D_3 and D_4 together with Din are forward biased.

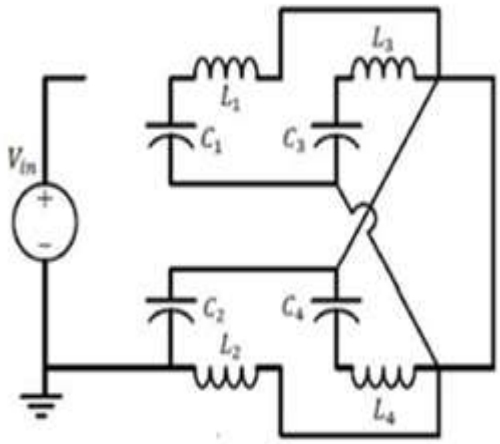


Figure 2.11: EB-ZSI shoot through mode (Ellabban & Abu-Rub, 2016)

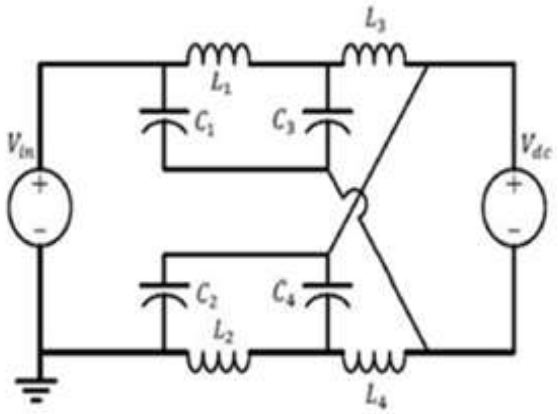


Figure 2.12: EB-ZSI non-shoot through mode (Hossam-Eldin, Abdelsalam, Refaey, & Ali, 2018)

2.7 Enhanced Boost qZSI

There are other similar topologies but the difference lies in the impedance network. This presented topology utilizes an active switch and has two less inductor/capacitor network when compared to similar topology which uses 2 switched Z source network even though it produces the same boost factor. Also the number of diodes is reduced by one and incorporates an active switch into the circuit. The efficiency is highly improved because the component stress is minimized by half thus significant reduction in the conduction losses (Nguyen, Lim, & Kim, 2012).

2.8 Neutral Point Clamped qZSI

The NPCqZSI topologies combine the advantages of the NPC and qZSI; quality output waveform with reduced harmonic content, single stage inversion, high efficiency, buck-boost capabilities, continuous drawn current at source, high immunity to EMIs, reduced component stress caused by voltage, shoot through potential, a three level NPCqZSI topology is presented which has continuous current input advantage when compared to other NPCqZSI topologies (Bayhan, Trabelsi, Ellabban, Abu-Rub, & Balog, 2016). The 3L-NPCqZSI topology is derived by joining two impedance networks as shown in Figure 2.13. This technique results in the topology having wide range of source voltage application such as PV systems, continuous current input from source, heavily reduced component stress, high switching capabilities hence high quality output voltage waveforms. Analysis of the circuit is similar to qZSI analysis plus the switching pattern for the neutral point clamped inverter.

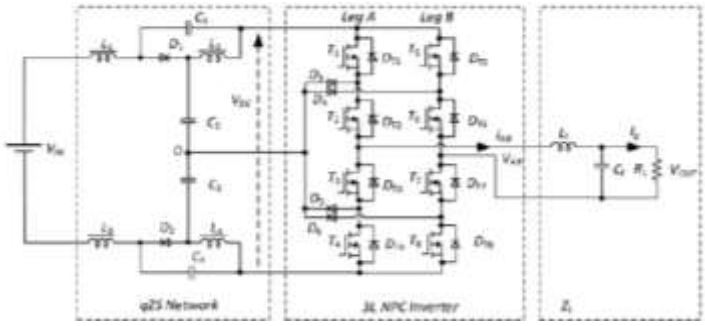


Figure 2.13: 3L NPCqZSI (Loh, Gao, Blaabjerg, Feng, & Soon, 2007)

Two circuits of modified quasi ZSI are provided, the first is a three level modified qZSI and the second is cascaded 5 level modified qZSI shown. The proposed circuit is made up quasi impedance network, neutral point clamped circuit and an H bridge connected to the load. The operation of the circuit is composed of two modes; shoot through and non-shoot through.

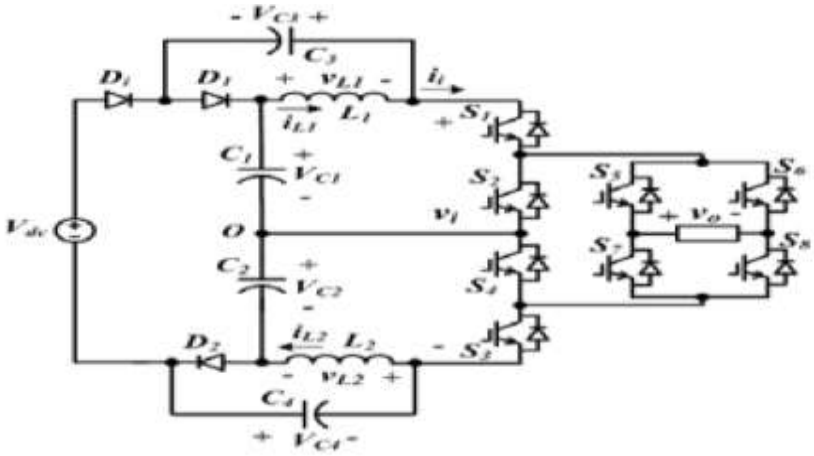


Figure 2.14: Modified qZSI (Bayhan et al., 2016)

Figure 2.15 show the five-level modified quasi Z source cascaded inverter. This topology being 5-level inverter means that it's a symmetrical topology, varying the voltage source each cell of the topology will produce a much higher level which will translate into quality output wave form.

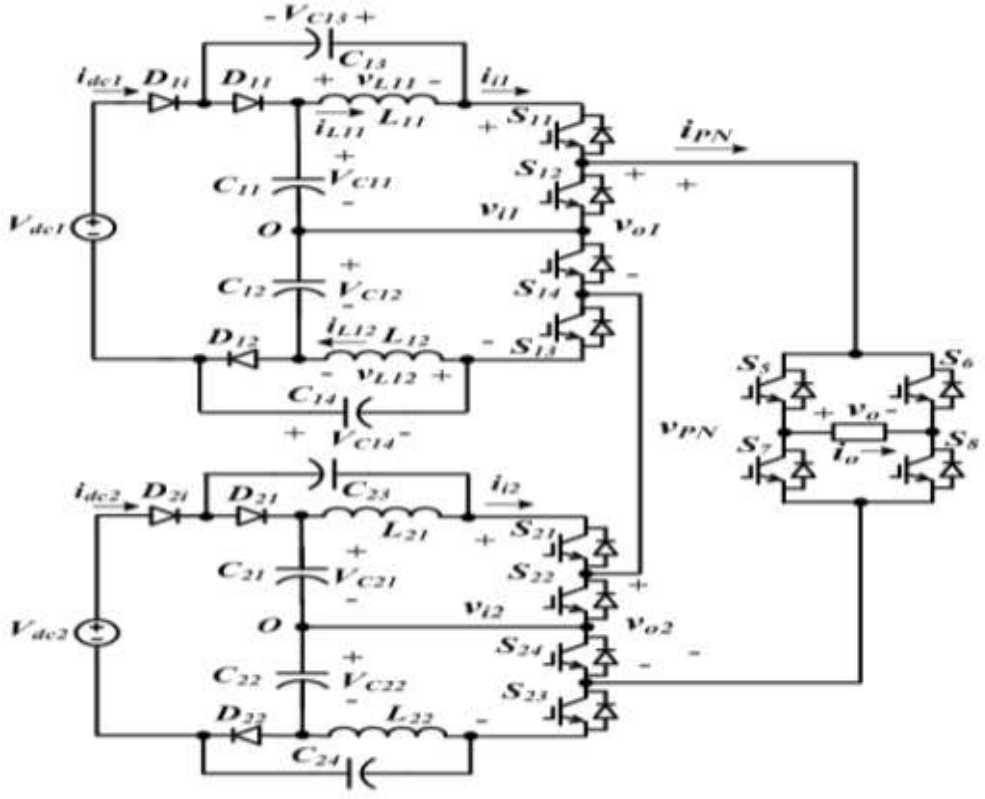


Figure 2.15: 5-level Modified qZSI (Bayhan et al., 2016)

2.9 Z-H Buck Converter

A new type of Z source topology is presented in (Ahmadzadeh & Babaei, 2015) which is known as Z-H buck converter. This structure combines the half-bridge structure with impedance network but with reduced component count in the impedance structure. Figure 2.16 shows the Z H buck converter system. The type of switches used depends on the application type; when the converter is used as chopper, inverter or rectifier, unidirectional switches are employed and bidirectional switches used when the converter is applied as a cycloconverter. The main purpose of this topology is step down the input voltage to a desirable level (Ahmadzadeh & Babaei, 2015).

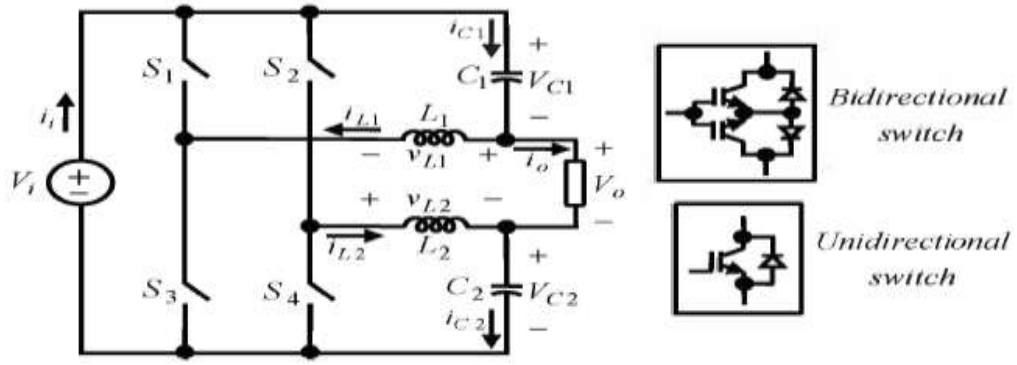


Figure 2.16: Z H buck converter (Ahmadzadeh & Babaei, 2015)

2.10 Z Source dc-dc Converter

Conventional boost dc-dc converters has been applied widely for output power boosting and can produce infinite voltage when the duty ratio is equivalent to one. However parasitic resistance causes limitation on the peak level of the duty cycle. Theoretically the voltage gain of this converter is infinite but in practical applications it's limited (Wuhua Li et al., 2007; Qian et al., 2011; Tang et al., 2007). To overcome the limitations of this converter, several topologies of converters have been proposed, examples are; non isolated boost dc-dc converter, non-isolated with voltage multiplier technique (Axelrod & Berkovich, 2003; Prudente, Pfitscher, Emmendoerfer, Romaneli, & Gules, 2008), switched inductor topology (Al-Saffar et al., 2013; Axelrod, Berkovich, & Ioinovici, 2003; D. Li et al., 2013; Tang, Fu, Wang, & Xu, 2015; Transactions & Electronics, 2015), switched capacitor topology (Abutbul, Gherlitz, Berkovich, & Ioinovici, 2003; Abutbul, Gherlitz, Berkovich, Ioinovici, & Member, 2003; Law, Cheng, & Yeung, 2005; D. Li et al., 2013;

Liang, Chen, Yang, Chen, & Ioinovici, 2012; Tang, Wang, & He, 2014), cascaded topology (D. Li et al., 2013; Modules, Walker, Walker, & Sernia, 2015).

The above so-called improved topologies are too complex to operate also escalates the overall cost of the system and the system volume is also enlarged, efficiency is also reduced. The Z source network can overcome all the drawback of this converter and also render a high boosting ability with higher efficiency. An example of the impedance network coupled to a dc-dc converter (Tang et al., 2007) is shown in Figure 2.12 (a) whiles Figure 2.12 (b) shows the novel version of the ZS dc-dc converter. The difference between the topologies is that the diode in Figure 2.12 (a). is substituted to an inductor in Figure 2.29 (b). Detailed explanations of the merits and demerits of various improved Z source topologies have been presented in (Ellabban & Abu-Rub, 2016).

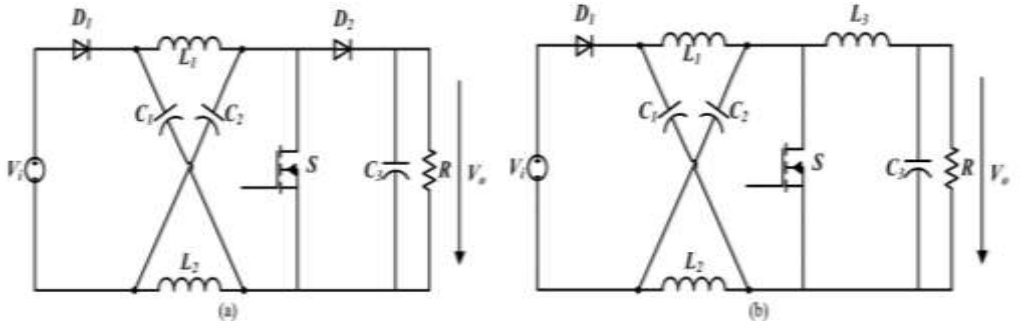


Figure 2.17: Z-source dc-dc converter (Galigekere & Kazimierczuk, 2012)

The advantage of this dc-dc converter is the high voltage gain attributes and the common ground between the input and output sections of the converter. Slight adjustment of the load location produces the magnitude of the high voltage gain desired, other merits of the converter is the low voltage stress on the components and simple layout of the converter. The application of this converter can be in two folds; in single stage power conversion systems and double stage power conversion systems like PV systems. The application of this topology in double stage conversion system will produce highly efficient system and allow maximum power tracking. The difference between this topology and conventional converter in figure 2.18 is the position of the load and ground with respect to the source input, also the load and the source input are located on the same section of the impedance network of the converter and share the ground.

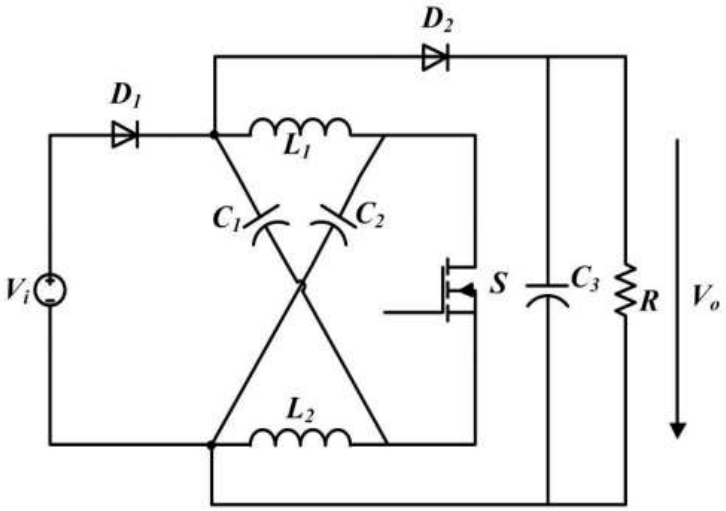


Figure 2.18: Z source dc-dc converter (Galigekere & Kazimierczuk, 2012)

The proposed topology has fewer semiconductor switches when compared to the boost topology but the proposed topology also has more passive components than the boost topology. The size and weight of the boost topology will be much higher due to the heat sink.

2.11 Applications of ZSI in Renewable Energy Systems

Power origination from non-conventional energy sources like solar will have an important task in the recent electricity demand solar technology has been well grown and is one of the most assuring sources of non-conventional energies (Parikh & Parikh, 2012).

A typical setup of a power electronic system application where converters are used as a power processing component to provide an input-output interface is shown in figure 2.19. The power flows from the input to the output through a processor stage, which is controlled through a negative feedback signal from either the input or the output (or both).

In a PV system for example, the power input will always be a DC signal given by the functionality of the PV cell (which is varying with the amount of energy absorbed from the sun). The power processor can be described as a power conversion stage. It typically consists of one or more converters, often with an energy storage element included.

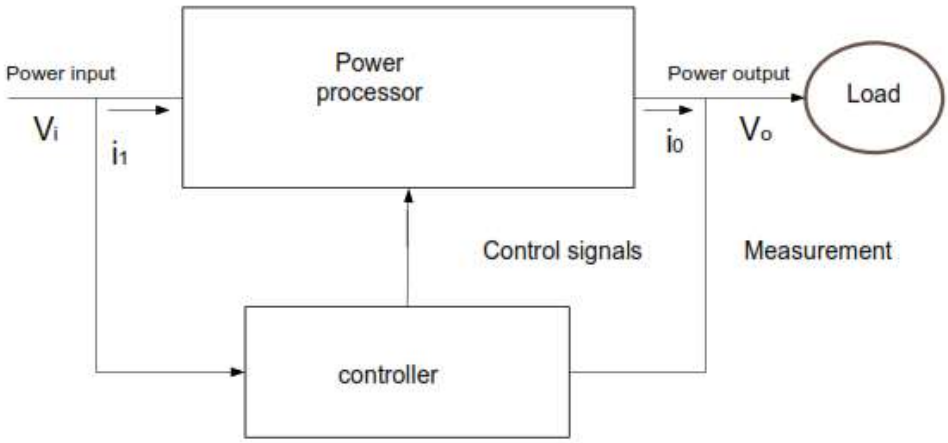


Figure 2.19: Block diagram of a power electronic system (Ja'far, 2012)

A PV system intended for grid connection usually has a power processor as shown in figure 2.20. The controller can be implemented to control both the converters separately to ensure a stable interface between each of the stages, i.e. between the input and converter1and converter 2 and the output.

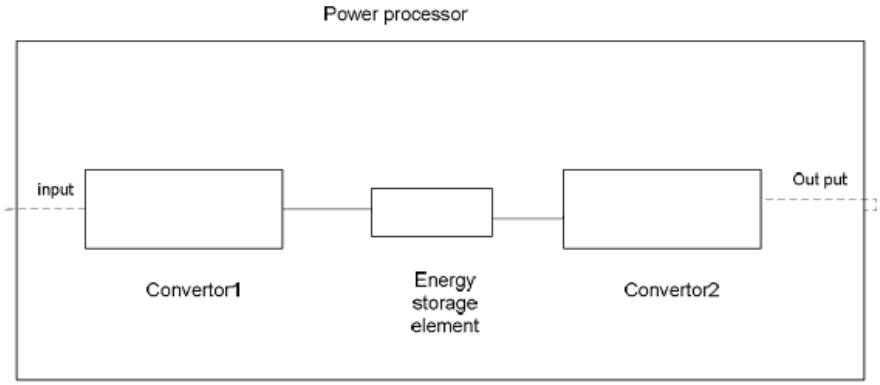


Figure 2.20: Block diagram of a power processor (Ja'far, 2012)

The voltage produced by the photovoltaic cells will vary according to the sunlight intensity (irradiance), but the system output requires a constant voltage value to be able to process and control the electric energy in the system (i.e. the voltages, currents, frequency) there is a need for a power electronic interface. The power electronics application in photovoltaic system is using the most efficient technique to extract the maximum power from the PV cell.

Kayatri et al (Kayatri, Rajan, & Vengatesh, 2016), have demonstrated the function of Z-network converter in PV power generation system with maximum power point tracking (MPPT) control strategies. The fundamental element of PV system is a PV cell. The PV array system has a combination of PV modules which are connected in series, parallel and series-parallel configurations also predominantly affect the performance of the Photovoltaic system. The PV panel has very low conversion efficiency therefore, a 3-Z-Network Boost Converter topology has been used to transmit solar power from the PV array to the load with high Voltage gain and results in better efficiency as the switching losses are minimized. The MPPT control technique maximizes the energy from the PV modules by extracting maximum feasible energy. For this reason, MPPT control techniques have been grown. Many different algorithms have been developed to track the MPP. MPPT techniques are chosen depending upon the complexity, the required number of sensors, cost, performance, the convergence speed, and application area. Figure 2.21 indicates the block diagram of the system.

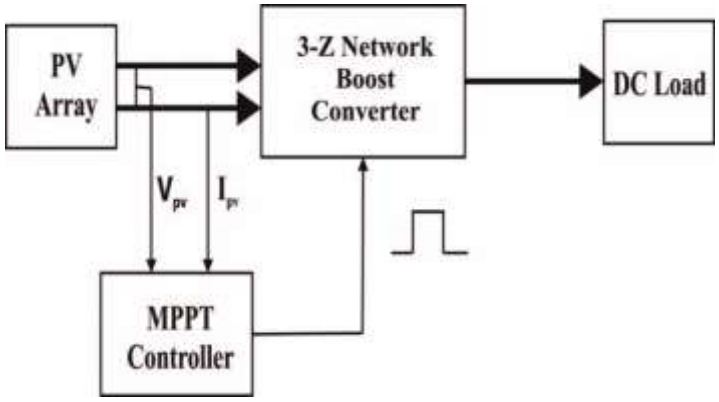


Figure 2.21: Block diagram of the proposed system (Kayatri et al., 2016)

Integration of z source topologies into residential or grid connected photovoltaic systems has increased over the years due to the elimination of double stage conversion with single stage conversion provided by z source inverters. Z source inverter based residential photovoltaic system convert or change direct voltage into alternating voltage, provide boosting capabilities if PV voltage is less, and can achieve peak power supply from photovoltaic panels. Two types of conventional inversion existed before the introduction of impedance structures; single stage inversion with a transformer and double stage inversion without transformer but two converters; dc-dc and dc-ac were utilized. Figure 2.22 and

Figure 2.23 show the two topologies. In other to produce 220V of ac voltage, the photovoltaic systems should produce about 340 – 680 V_{dc}. These voltage ranges mean increase cost and increased stress on the components however if the Z source topology is applied, the output power of the PV systems can be reduced to 225 – 450 Vdc which translates to reduced component ratings hence reduced component stress and reduced cost.

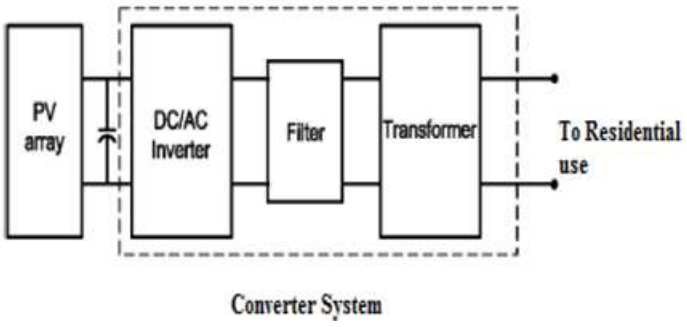


Figure 2.22: Single stage transformer converter system (Wei, Tang, & Xie, 2010)

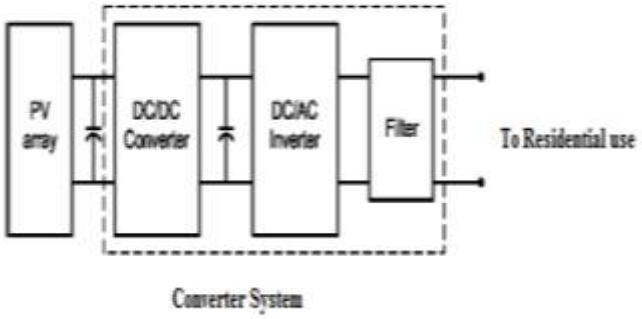


Figure 2.23: Double stage converter system (Wei et al., 2010)

A resonant Z source converter (González-Santini, Zeng, Yu, & Peng, 2016) with power factor correction is applied in wireless power transfer applications such as the charging of electric vehicle batteries. The Z source resonant converter executes output voltage regulation and power factor correction simultaneously due to impedance network in the structure of the converter. A simplified diagram of electric vehicle charging is shown in Figure 2.22. The system utilizes online inductive power transfer principle, the electric vehicle has pickup coil located at the bottom of the car which connects wireless to the charging station to charge batteries on board the vehicle.

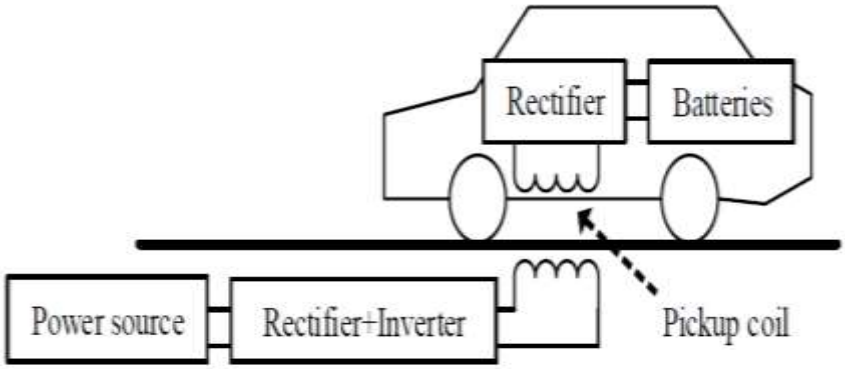


Figure 2.24: Wireless EH charging system (González-Santini et al., 2016)

Figure 2.23 show the conventional on-board battery charger in electric vehicles. This topology is made up of double stage power conversion i.e. ac to dc and dc to dc. From the diagram, the first stage of power conversion is a simultaneous task of changing ac to dc by means of rectification and also power factor correction. The other part is a dc to dc conversion and it's dependent on the desired dc voltage at the output.

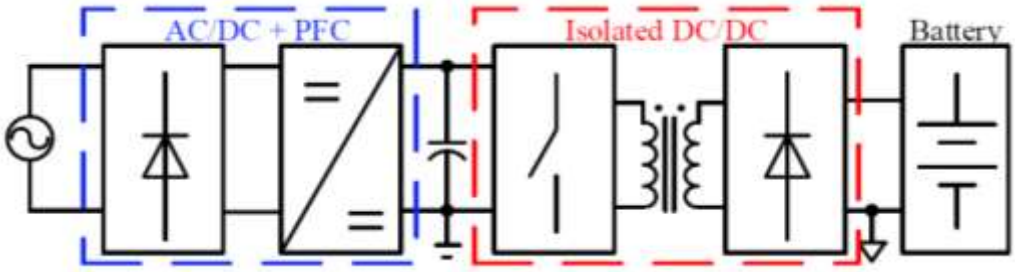


Figure 2.25: Conventional on-board battery charging system (González-Santini et al., 2016)

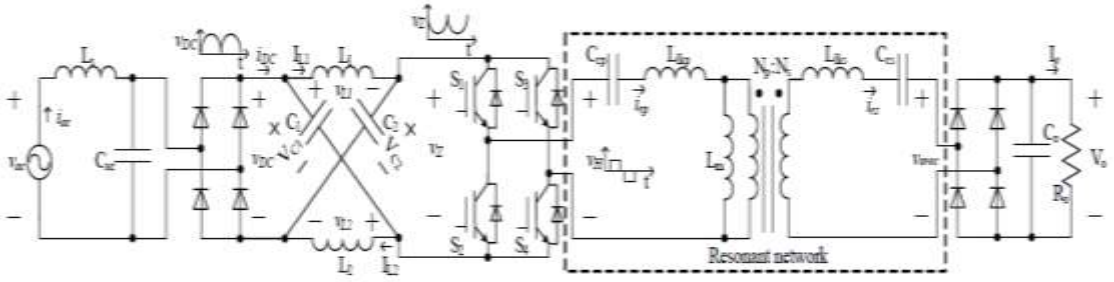


Figure 2.26: Z source resonant converter for OBC (González-Santini et al., 2016)

The advantages of the traditional boost converter for on board battery charger are; low cost of the converter, power factor and power density are high, has good efficiency (Musavi,

Edington, Eberle, & Dunford, 2011). This topology is not suitable for high power applications the efficiency decreases due to the high losses incurred at the rectifier stage hence powers up to 3.5kW are suitable range for applications (Musavi et al., 2011; Yilmaz, M., Krein, 2013). The inclusion of Z-source network as shown in figure 2.24 handles the short comings and extended the capabilities.

CHAPTER 3

POWER CIRCUIT DESCRIPTION, DEVELOPMENT AND SIMULATION RESULTS

3.1 Introduction

In this chapter the circuit description, analysis and simulation results for the 3-Z-Network converter (Zhang, Member, Zhang, & Li, 2014) are presented. The chapter begins by describing the converter circuit and its development. This is followed by the steady-state analysis of the converter in both continuous current mode (CCM) and discontinuous current mode (DCM). The simulation result from PSCAD software is presented at the end of the chapter. To simplify the analysis, it is assumed that all the circuit components are ideal and the freewheeling diode is also ignored.

3.2 Circuit Description

The converter circuit is shown in Figure 3.1, it is consisting of three active Z networks. Unlike conventional Z networks, that usually contain passive elements, this converter contains active Z networks. In this converter circuit, Z-network 1 comprising of diodes D_1, D_2 and D_3, and inductors L_1 and L_2 acts as the first boost stage; Z-network 2 contains the switch Q, diodes D_4 and D_5 and capacitor C_1, it is the switching stage; and finally Z-network 3 acts as second boost stage, which includes diodes D_6, D_7 and D_8, and inductors L_3 and L_4. As evidently seen from the circuit only one switch is used.

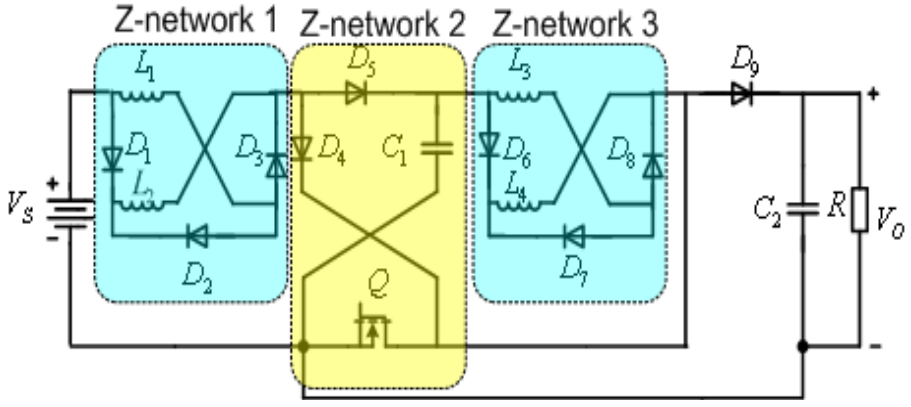


Figure 3.1: Converter circuit diagram

3.3 Circuit Analysis in CCM and DCM

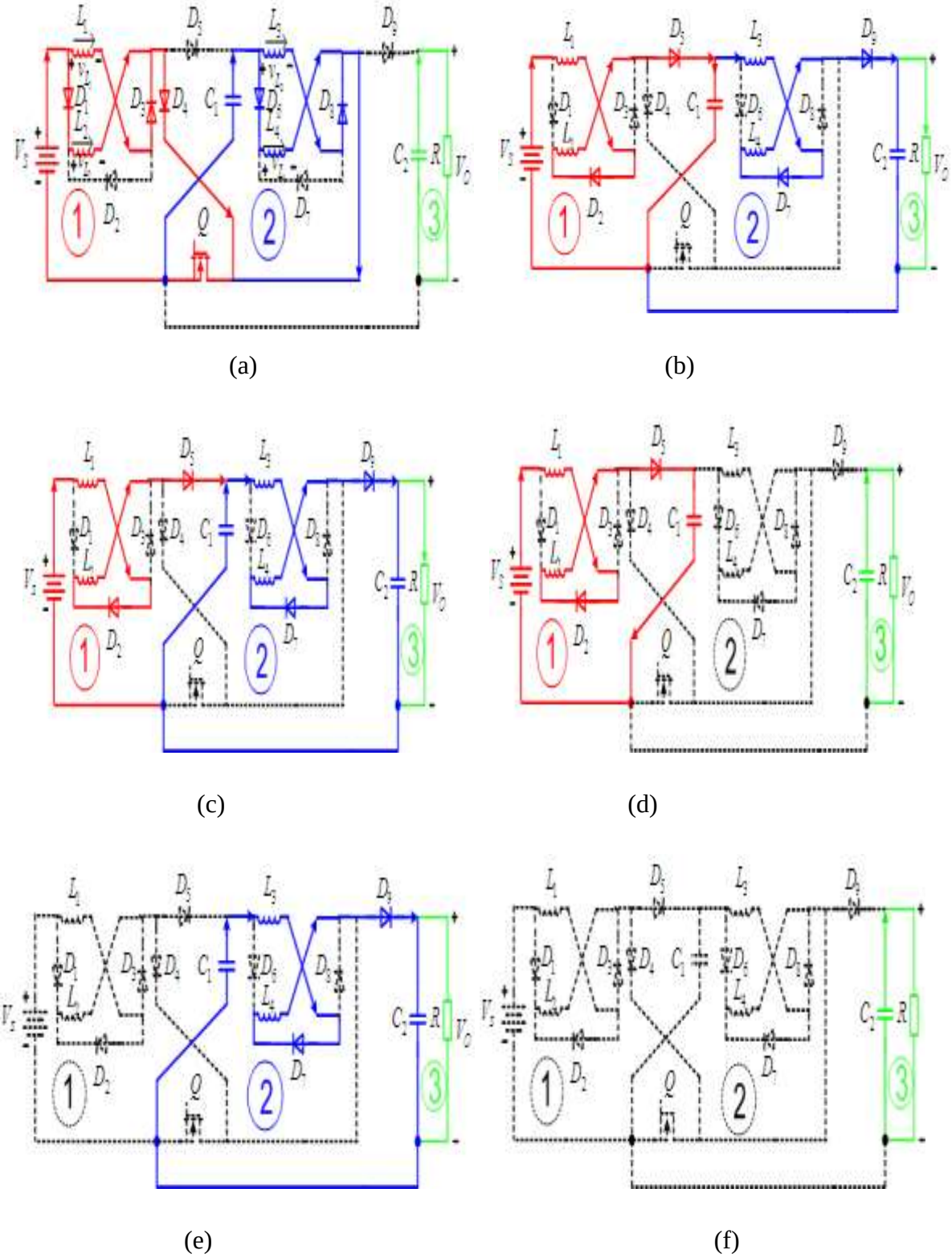
The converter circuit operates in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The converter is said to be operating in CCM if the inductor current does not reach zero level within the switching cycle, and is said to operate in DCM if the inductor current goes to zero during some interval within the switching cycle. In this section six operational cases; two CCMs and four DCMs are examined. These cases result from the various modes of diodes and capacitor current.

Within the switching period (on and off) of the switch Q, the inductor charges and discharges energy alternatively. Similarly, the inductor current increases and decreases alternatively. As a result, situations occurred where the inductor current reach and remain at zero for some interval (DCM).

The converter operates in six modes and various combination of these modes result in six cases. The corresponding equivalent circuits of these modes are shown in figure 3.2 (a)-(f). Within the circuits, v_{L1}, v_{L2}, v_{L3} and v_{L4} represent the voltages across inductors L_1, L_2, L_3 and L_4 respectively. Moreover, clockwise direction is considered as the positive direction of the reference current. In addition, the exact states of the components of the circuit are shown in Table 3.1.

Table 3.1: Components States in Each Mode

	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6
Q	On	Off	Off	Off	Off	Off
D1 & D3	On	Off	Off	Off	Off	Off
D2	Off	On	On	On	Off	Off
D4	On	Off	Off	Off	Off	Off
D5	Off	On	On	On	Off	Off
D6 & D8	On	Off	Off	Off	Off	Off
D7	Off	On	On	Off	On	Off
D9	Off	On	On	Off	On	Off



(a) (b)

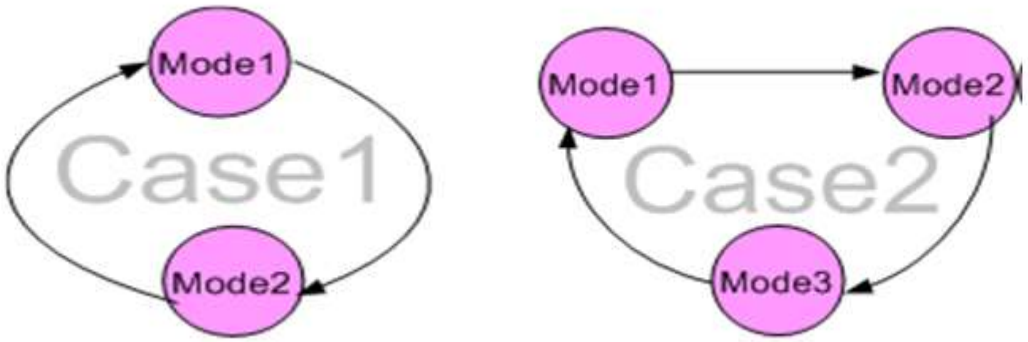
(c) (d)

(e) (f)

Figure 3.2: Equivalent circuits.(a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) mode 6

3.3.1 Continuous Conduction Mode (CCM)

In this section the converter operation in CCM is analyzed in detail. Two cases fall under this category; Case one corresponding to $mode1 \rightarrow mode2$ and case two which correspond to $mode1 \rightarrow mode2 \rightarrow mode3$. This is depicted in figure 3.3.



(a) (b)

Figure 3.3: Transitions between modes in CCM.

(a) Case one. (b) Case two

3.3.1.1 Case one

Fig. 3.3 (a) shows the diagram corresponding to this case. There are two modes in this case; mode 1 and mode 2 whose equivalent circuits are shown in figure 3.2(a) and figure 3.2(b). The steady state switching waveform shown in figure 3.4 is used to describe the operation of the converter in this case, different colors are used to indicate two modes in one period.

Following notation are used in the key waveforms: D represent the switching duty cycle, t_o the starting of a period, t_1 transition interval from one mode to another, and $t_2 = T$ is the end of period. In addition, i_{D1}, i_{D2}, i_{D3}, i_{D4}, i_{D5}, i_{D6}, i_{D7}, i_{D8}, i_{D9}, i_{l1}, i_{l2}, i_{l3}, i_{l4}, i_{C1}, i_{C2} represent the currents of diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9, inductors L_1, L_2, L_3, L_4, and capacitors C_1, and C_2 respectively.

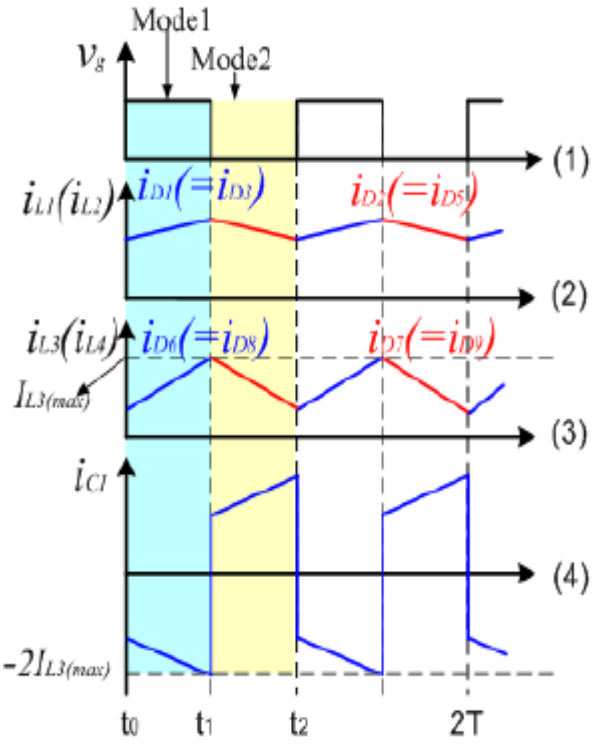


Figure 3.4: Waveform of the converter in Case one (1) Switching voltage V_g of switch Q. (2) waveform of $i_{L1}(i_{L2})$, blue indicate waveform of $i_{D1}(= i_{D3})$, and the red indicate waveform of $i_{D2}(= i_{D5})$. (3) shows the waveform of $i_{L3}(i_{L4})$, blue colour indicate waveform of $i_{D6}(= i_{D8})$, and the red indicate waveform of $i_{D7}(= i_{D9})$. (4) depict waveform of waveform of $i_{L1}(i_{L2})$, blue indicate waveform of $i_{D1}(= i_{D3})$, and the red indicate waveform of i_{c1}.

Mode 1: $t \in [t_0, t_1]$: shown in figure 3.2(a), when switch Q is turn on, positive voltage appears across diodes D_1, D_3 and D_4 turning them on simultaneously, D_2 takes negative voltage and turns off. Consequently, L_1 and L_2 are in parallel and their combination is in series with D_4, Q and V_s, forming loop 1 as indicated in red lines. L_1 and L_2 are charged by V_s, then i_{l1} and i_{l2} increased. Accordingly, we have:

$$i_{D1} = i_{D3} = i_{L1} = i_{L2} \tag{3.1}$$

$$i_{D2} = 0 \tag{3.2}$$

$$i_{D4} = i_{D1} + i_{D3} = 2i_{L1} \tag{3.3}$$

$$v_{L1} = v_{L2} = V_s \tag{3.4}$$

$V_{L1} and\ V_{L2}$ are the corresponding voltages of inductors $L_1\ and\ L_2$.

Concurrently, negative voltages across D_5, and D_7 turn them off, while the D_6, and D_8 withstand the positive voltage and turn on. Meanwhile, L_3 and L_4 are connected in parallel, and in series with Q and C_1 forming loop 2 as indicated in blue color. Inductors L_3 and L_4 are charged up by the capacitor C_1 and then i_{L3} and i_{L4} increased. The waveforms are marked with blue colors in figure 3.4, from which following relationships can be established.

$$i_{D6} = i_{D8} = i_{L3} = i_{L4} \tag{3.5}$$

$$i_{D5} = 0 \tag{3.6}$$

$$i_{C1} = -2i_{L3} \tag{3.7}$$

$$v_{L3} = v_{L4} = v_{C1} \tag{3.8}$$

v_{L3}, v_{L4} and v_{C1} are the corresponding voltages of inductors L_3, L_4 and the capacitor C_1.

In the meantime, D_9 takes negative voltage and turns off, load R becomes in cascade with C_2 forming loop 3, indicated in green lines. Then, energy is discharged from C_2 to R. and the output voltage v_o becomes

$$v_o = v_{C2} \tag{3.9}$$

Mode 2: $t \in [t_1, t_2]$: As shown in figure 3.2(b), at $t_1$the switch Q is turn off, and a change from mode 1 to mode 2 occur. When Q is off, negative voltage appears across diodes D_1, D_3, D_4, D_6 and D_8 and they are turned off, however D_2, D_5, D_7 and D_9 take positive voltage and turn on, three loops resulted from this mode. That is, the $V_s - L_1 - D_2 - L_2 - D_5 - C_1$ loop, where the capacitor C_1 is been charged by the source V_s, and inductors $L_1\ and\ L_2$. In addition, the currents i_{L1} and i_{L2} decreases as shown with red lines in figure 3.4 (2), and currents of D_2 and D_5 equal to i_{L1} , and as shown in Figure 3.4 (4) i_{C1} increases.

Applying KVL in loop 1:

$$V_s - v_{C_1} - v_{L_2} - v_{L_1} = 0 \tag{3.10}$$

And therefore, we got

$$i_{D2} = i_{D5} = i_{L1} = i_{L2} \quad (3.11)$$

$$i_{D1} = i_{D3} = i_{D4} = 0 \quad (3.12)$$

$$v_{L1} + v_{L2} = V_s - v_{C1} \quad (3.13)$$

Meanwhile, $V_s, L_1, D_2, L_2, D_5, L_3, D_7, L_4, D_9$, and C_2 form the second loop indicated in red and blue lines, in which $V_s, L_1, L_2, L_3,$ and L_4 discharge energy to C_2 and load R. i_{C2} decreases with respect to the discharged energy to the load resistance R. In addition, the i_{L3} and i_{L4} that are shown in red lines in Figure 3.4 (3) decreases, and current of D_7 and D_9 equal to i_{L3} because of the series connection. i.e.:

Applying KVL and KCL in loop 2:

$$i_{D7} = i_{D9} = i_{L3} = i_{L4} \quad (3.14)$$

$$i_{D6} = i_{D8} = 0 \quad (3.15)$$

$$v_{L3} + v_{L4} = V_s - (v_{L1} + v_{L2} + v_{C2}) \quad (3.16)$$

3.3.1.2 Case two

The flow diagram for case two is shown in Figure 3.3 (b). This is also a CCM but unlike case one there are three modes under this case depending on i_{C1} direction; mode 1, mode 2 and mode 3 whose equivalent circuits are shown in figures 3.2(a), 3.2(b) and 3.2(c).

The steady state switching waveform presented in figure 3.5 is used to describe the operation of the converter in this case, different colors are used to indicate the three modes in one period. Therein, t_o is the starting of a period, t_1 transition interval from mode1 to mode 2 given as $t_1 = t_o + DT$, t_2 transition interval from mode 2 to mode 3 and t_3 is the end of period.

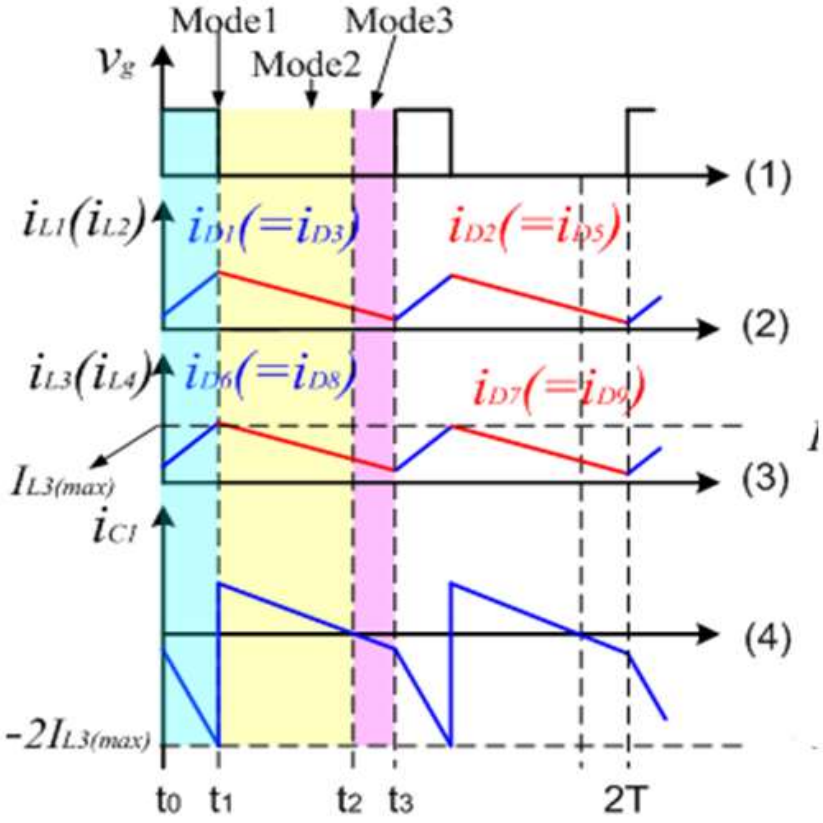


Figure 3.5: Waveform of the converter in Case two

Mode 1: $t \in [t_0, t_1]$: The analysis and discussion are similar to mode1 of case one.

Mode 2: $t \in [t_1, t_2]$: The analysis and discussion are similar to mode 2 of case one, with exception of capacitor current i_{C_1} which decreases as shown in figure 3.5 (4).

Mode 3: $t \in [t_2, t_3]$: At $t = t_2$: capacitor currents $i_{C_1} = i_{C_2} = 0$, and this mark the beginning of mode 3 whose equivalent circuit is shown in fig. 3.2 (c), therein, the switch Q and diodes D_1, D_3, D_4, D_6, and D_8 are off, while D_2, D_5, D_7 and D_9 are on. There are two loops in this mode shown with different colors.

Loop 1 is just like loop 1 of mode 2. In loop 2, i_{C_1} goes from zero to negative, therefore C_1 also discharge energy to the subsequent circuit, and the equations are obtained as in case one.

3.3.2 Discontinuous Current Mode (CCM)

Here, the converter operation in DCM is analyzed in detail. Four cases fall under this category as depicted in figure 3.6.

Case three: $mode1 \rightarrow mode2 \rightarrow mode4$

Case four: $mode1 \rightarrow mode2 \rightarrow mode3 \rightarrow mode5$

Case five: $mode1 \rightarrow mode2 \rightarrow mode4 \rightarrow mode6$

Case six: $mode1 \rightarrow mode2 \rightarrow mode3 \rightarrow mode5 \rightarrow mode6$

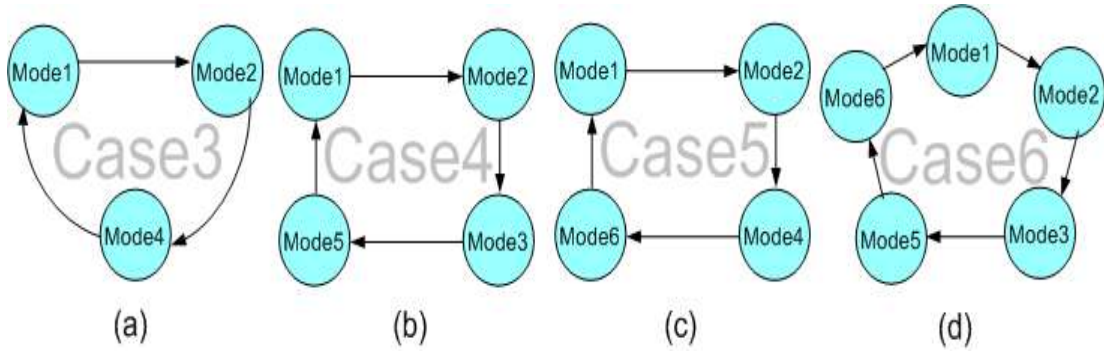


Figure 3.6: Flow between modes in DCM.

(a) Case one. (b) Case two (c) Case three (d) Case four

3.3.2.1 Case three

The flow diagram of this case is shown in figure 3.6 (a), unlike case one and case two, case three is a discontinuous conduction mode (DCM). In this case, there are three modes; modes 1, 2 and 4 with their associated equivalent circuits shown in Figures 3.2 (a), 3.2 (b) and 3.2 (d).

The steady state switching waveform shown in fig. 3.7 is used to describe the operation of the converter in this case, different colors are used to indicate three modes in one period. Therein, t_o represent the starting of a period, t_1 mode transition from mode 1to mode 2, given as $t_1 = t_o + DT$, t_2 transition interval from mode 2 to mode 4 and $t_3 = T$ is the end of period.

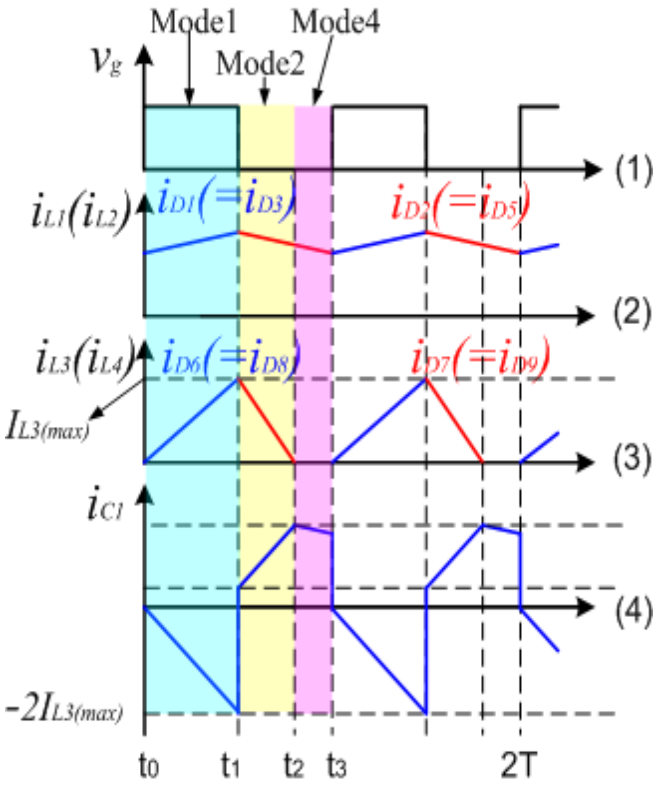


Figure 3.7: Waveform of the converter in Case three

Mode 1: $t \in [t_0, t_1]$: The analysis and discussion are similar to mode1 of case one.

Mode 2: $t \in [t_1, t_2]$: The analysis and discussion are similar to mode 2 of case one.

Mode 4: $t \in [t_2, t_3]$: This mode occur when the inductor currents i_{L3} *and* i_{L4} reduces to zero while switch Q remain off, as seen from figure 3.7 in this mode $i_{D7} = i_{D9} = i_{L3} = i_{L4} = 0$. From figure 3.2 (d), the switch Q and diodes D_1, D_3, D_4, D_6, D_7, D_8 and D_9 are off, while D_2 and D_5 are on. The two loops are shown with different colors.

Loop 1 (red color): $V_s - L_1 - D_2 - L_2 - D_5 - C_1$ from which we have $i_{C1} = i_{D2} = i_{D5} = i_{L1} = i_{L2}$. The energy of the L_1 *and* L_2 inductors and the source charges the capacitor C_1, so that current i_{C1} increases.

$$i_{C1} = i_{D2} = i_{D5} = i_{L1} = i_{L2} \tag{3.17}$$

$$i_{D1} = i_{D3} = i_{D4} = 0 \tag{3.18}$$

Within loop 2 indicated in green color, capacitor C2 discharges energy to load R.

$$V_o = v_{C2} \tag{3.19}$$

3.3.2.2 Case four

The flow diagram of this case is shown in fig. 3.6 (b), like case three this is also discontinuous current mode (DCM). In this case, there are four modes; modes 1, 2, 3 and 5, with their associated equivalent circuits shown in Figures 3.2 (a), 3.2 (b), 3.2 (c) and 3.2 (e).

The waveforms shown in figure 3.8 is used to describe the operation of the converter in this case, different colors are used to identify the four modes in one period. Therein, t_o represent the starting of a period, t_1 mode transition from mode 1to mode 2, given as $t_1 = t_o + DT$, t_2 transition interval from mode 2 to mode 3, t_3 transition interval from mode 3 to mode 5, and $t_4 = T$ is the end of period.

Mode 1: $t \in [t_0, t_1]$: The procedure is exactly equal to mode1 of case two.

Mode 2: $t \in [t_1, t_2]$: The procedure is exactly equal to mode 2 of case two.

Mode 3: $t \in [t_2, t_3]$: This function is almost the same as Mode 2 in case two. Nevertheless, as shown in figure 3.8 (2) inductor currents $i_{L1}\ and\ i_{L2}$ reduced to zero, and then mode 5 take place.

Mode 5: $t \in [t_3, t_4]$: Loop 1 finished when $i_{L1}\ and\ i_{L2}$ became zero. Subsequently, energy is discharged from C_1 $L_3\ and\ L_4$ to C_2 and R. Moreover, energy is discharged from C_2 and R. Therefore, i_{C2} reduces from positive to negative. Subsequently, energy is discharged from C_1, C_2 $L_3\ and\ L_4$ to R.

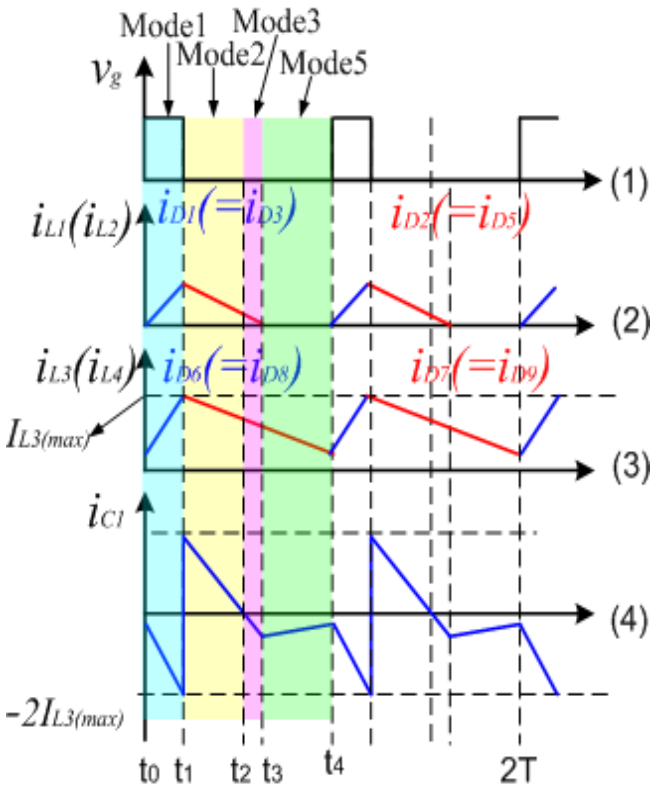


Figure 3.8: Waveform of the converter in Case four

3.3.2.3 Case five

The flow diagram of this case is shown in figure 3.6 (c), like case three and 4 this is also discontinuous current mode (DCM). As currents i_{L1} *and* i_{L2} reduced to zero in mode 4 of case three, only loop 3 remain and this is considered as case five. Similarly, in this case there are four modes; modes 1, 2, 4 and 6, with their associated equivalent circuits shown in Figures 3.2 (a), 3.2 (b), 3.2 (d) and 3.2 (f).

The waveforms shown in figure 3.9 is used to describe the operation of the converter in this case, four different colors are used to identify the four modes in one period. Therein, t_o represent the starting of a period, t_1 mode transition from mode 1to mode 2, given as $t_1 = t_o + DT$, t_2 transition interval from mode 2 to mode 4, t_3 transition interval from mode 4 to mode 6, and $t_4 = T$ is the end of period.

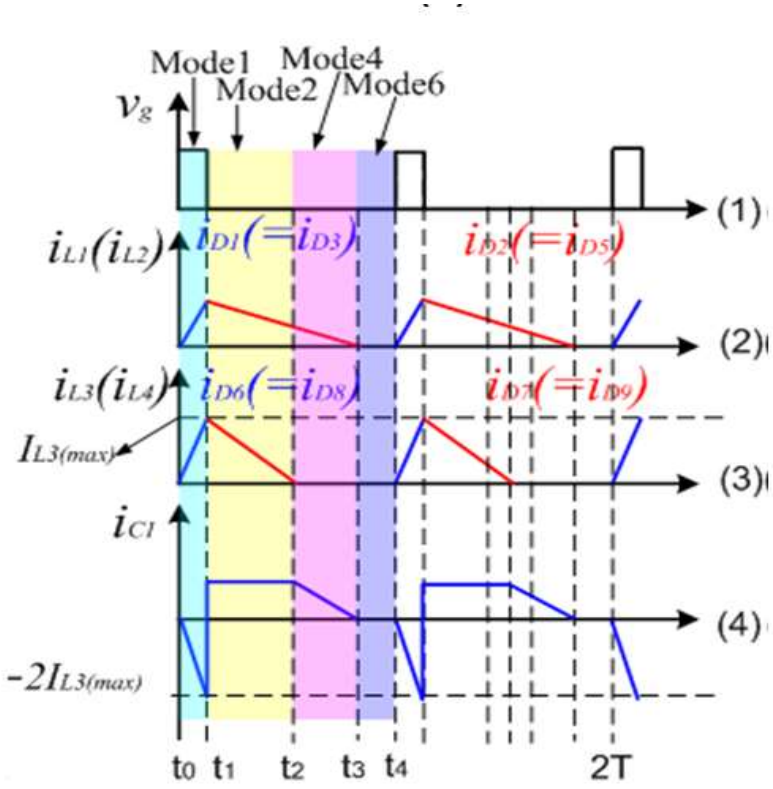


Figure 3.9: Waveform of the converter in Case five

Mode 1: $t \in [t_0, t_1]$: The procedure is exactly equal to that of mode1 of case three.

Mode 2: $t \in [t_1, t_2]$: The procedure is exactly equal to mode 2 of case three.

Mode 4: $t \in [t_2, t_3]$: The procedure is exactly equal to that of mode 4 of case three.

Mode 6: $t \in [t_3, t_4]$: Mode 6 occur when i_{L1} and i_{L2} became zero and switch Q remain off. Subsequently, energy is discharged from C_2 to R and i_{C2} remain constant.

3.3.2.4 Case Six

The flow diagram of this case is shown in fig. 3.6 (d), like case three, 4 and 5 this is also discontinuous current mode (DCM). This mode occurs when inductor currents i_{L3} and i_{L4} reduced to zero in mode 5 of case four. In this case there are five operational modes; modes 1, 2, 3, 5 and 6, with their associated equivalent circuits shown in Figures 3.2 (a), 3.2 (b), 3.2 (c), 3.2 (e) and 3.2 (f).

The waveforms shown in figure 3.10 is used to describe the operation of the converter in this case, four different colors are used to identify the four modes in one period. Therein,

t_o represent the starting of a period, t_1 mode transition from mode 1to mode 2, given as $t_1 = t_o + DT$, t_2 transition interval from mode 2 to mode 3, t_3 transition interval from mode 3 to mode 5, t_4 transition interval from mode 5 to mode 6 and $t_5 = T$ is the end of period.

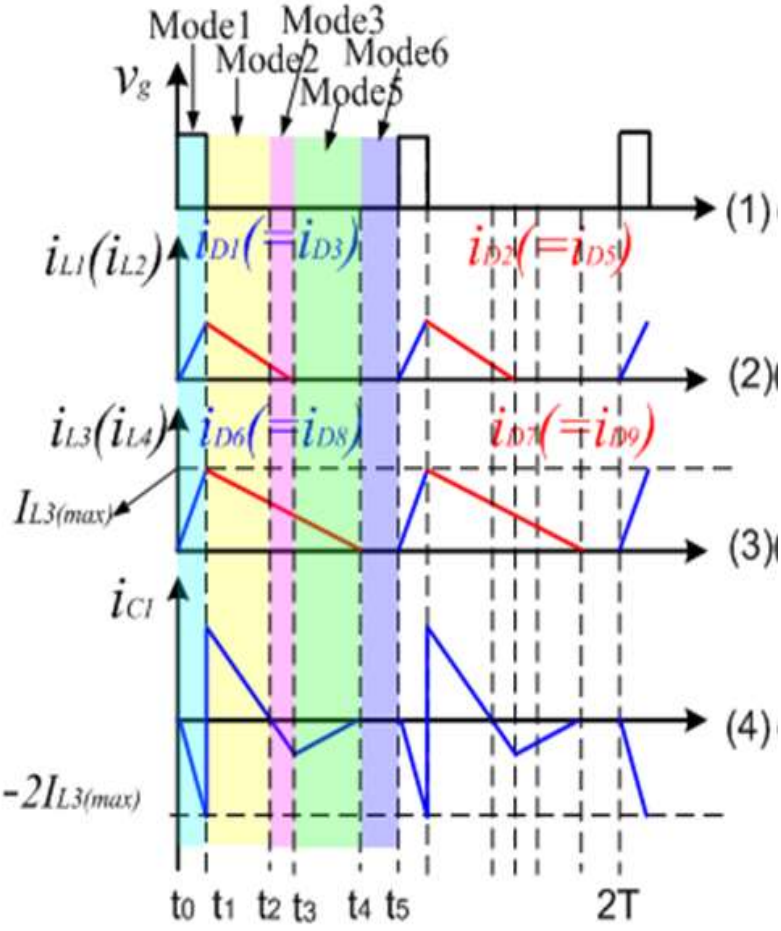


Figure 3.10: Waveform of the converter in case six

Mode 1: $t \in [t_0, t_1]$: The procedure is exactly equal to that of mode1 in case four.

Mode 2: $t \in [t_1, t_2]$: The procedure is exactly equal to mode 2 in case four.

Mode 3: $t \in [t_2, t_3]$: The procedure is exactly equal to that of mode 3 of case four.

Mode 5: $t \in [t_3, t_4]$: The function is exactly equal to that of mode 3 of case four.

Mode 6: $t \in [t_4, t_5]$: Mode 6 occur when i_{L1}, i_{L2}, i_{L3} and i_{L4} became zero and the switch Q remain off. In this case, energy is discharged from C_2 to R and i_{C2} remain constant.

3.4 Output Voltage and Voltage Stress

Here, voltage analysis of the referenced converter is presented. Considering case one and case two the output voltage can be established as follows. Using volt-second constant theory, we have

$$\int_0^{DT}(v_{L1}+v_{L2})dt+\int_{DT}^{T}(v_{L1}+v_{L2})dt=0 \quad (3.20)$$

$$\int_0^{DT}(v_{L3}+v_{L4})dt+\int_{DT}^{T}(v_{L3}+v_{L4})dt=0 \quad (3.21)$$

Using equations (3.4), (3.8), (3.13) and (3.16) in to equation (3.20) we have

$$\int_0^{DT}(V_s+V_s)dt+\int_{DT}^{T}(V_s-v_{C1})dt=0 \quad (3.22)$$

$$2\int_0^{DT}V_s\,dt+\int_{DT}^{T}(V_s-v_{C1})dt=0$$

From which we get

$$2V_sDT+(V_s-V_{C1})(1-D)T=0 \quad (3.23)$$

Similarly, by using equations (3.4), (3.8), (3.13) and (3.16) in to equation (3.21) we have

$$2\int_0^{DT}v_{C1}\,dt+\int_{DT}^{T}(v_{C1}-V_o)dt=0 \quad (3.24)$$

From which we get

$$2V_{C1}DT+(V_{C1}-V_o)(1-D)T=0 \quad (3.25)$$

Solving for V_{C1} from (3.23) we get,

$2V_sDT+TV_s-DTV_s-V_{C1}(1-D)T=0,$

$V_s(2DT+T-DT)-V_{C1}(1-D)T=0,$

$V_s(1+D)T-V_{C1}(1-D)T=0.$

And

$$V_{C1}=\frac{1+D}{1-D}\,V_s \quad (3.26)$$

Similarly, solving for V_o from (3.25) we get,

$2V_{C1}DT + TV_{C1} - DTV_{C1} - V_o(1-D)T = 0,$

$(1+D)V_{C1} = (1-D)V_o.$

And

$$V_o = \frac{1+D}{1-D}\, V_{C1} \tag{3.27}$$

Substituting for V_{C1} from (3.26) into (3.27) we get

$$V_o = V_s(\frac{1+D}{1-D})^2 \tag{3.28}$$

Meanwhile,

$$V_{C_2} = V_o = V_s\left(\frac{1+D}{1-D}\right)^2 \tag{3.29}$$

From (3.28) the voltage gain

$$M = \frac{V_o}{V_S} = \left(\frac{1+D}{1-D}\right)^2 \tag{3.30}$$

The comparison of the voltage gains of conventional converter, the three-Z-source network converter (discussed in this thesis) and quadratic converter is depicted in figure 3.11. it is easy to see that the three-Z-source network converter gain is higher compared with others.

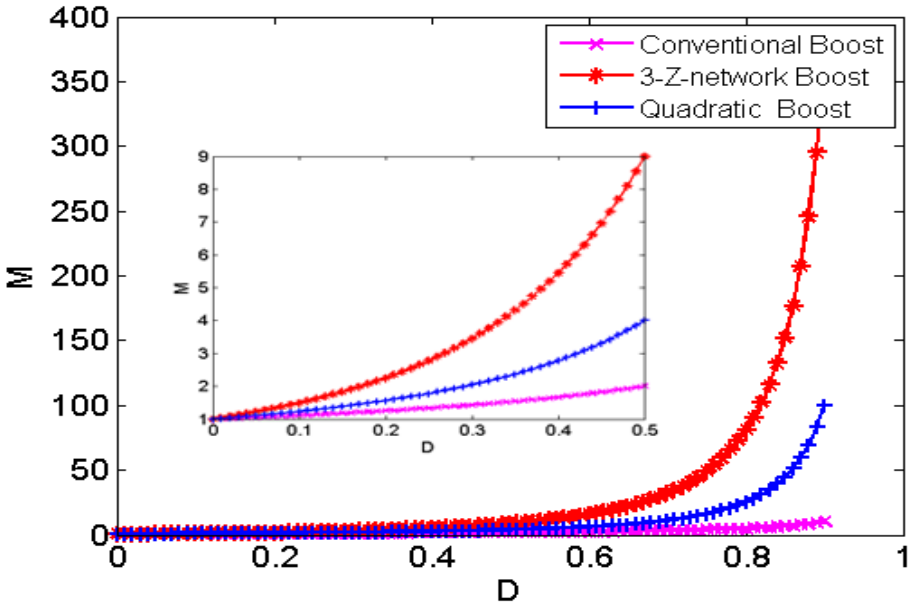


Figure 3.11: Voltage gain M Vs duty Cycle D

For average voltages across the inductors L_1 and L_2 represented as V_{L1} and V_{L2} respectively, when the Q is on, the two voltages are equal to V_s, but when Q is off by applying KVL we get

$$V_s - V_{L1} - V_{L2} - V_{C1} = 0 \tag{3.31}$$

Substituting for V_{C1} (3.26) into (3.31) and the fact that $V_{L1} = V_{L2}$;

$$V_s - \frac{1+D}{1-D} V_s = 2V_{L1},$$

And hence,

$$V_{L1} = V_{L2} = -V_s \frac{D}{1-D} \tag{3.32}$$

This implies that

$$V_{L1} = V_{L2} = \begin{cases} V_s, & when\ Q\ is\ on \\ -V_s \frac{D}{1-D} & when\ Q\ is\ off \end{cases} \tag{3.33}$$

Similarly, for the average voltages across the inductors L_3 and L_4 represented as V_{L3} and V_{L4} respectively, the expressions are similar to that of V_{L1} and V_{L2} in (3.33) multiplied by $\frac{1+D}{1-D}$.

$$V_{L1} = V_{L2} = \begin{cases} V_s \frac{1+D}{1-D}, & when\ Q\ is\ on \\ -V_s \frac{D(1+D)}{(1-D)^2} & when\ Q\ is\ off \end{cases} \tag{3.34}$$

Table 3.2 shows the summary of the voltage stress across the semiconductor components in CCM.

For V_Q; in mode 1 where Q is on, the voltage across the switch is zero and for the modes 2 and 3, where Q is off the voltage across the switch is:

$$v_Q = V_o = V_{C_2} = \frac{(1+D)^2}{(1-D)^2} V_s \tag{3.35}$$

For V_{D1} and V_{D3}; in mode 1 where Q is on, the two voltages are zero while for the modes 2 and 3, where Q is off:

$$v_{D_1} = v_{D_3} = -V_{C_1} = \frac{D}{1-D} V_s \tag{3.36}$$

For V_{D2}; in mode 1, when Q is on, the voltage is V_s, and for mode 2 and 3, where Q is off, D_2 is short circuited and the voltage is zero.

For V_{D4}; in mode 1, when Q is on, the voltage is zero and for the modes 2 and 3, where Q is off by applying KVL;

$$-V_s + V_{L1} + V_{L2} - v_{D4} + V_o = 0 \tag{3.37}$$

Substituting for the unknowns in (3.37) we have:

$$v_{D_4} = -V_s - \frac{2D}{1-D} V_s + \frac{(1+D)^2}{(1-D)^2} V_s = \frac{(1-D)^2 V_s + 2D(1-D)V_s - (1+D)^2 V_s}{(1-D)^2} = \frac{2D(1+D)}{(1-D)^2} V_s \tag{3.38}$$

For V_{D5}; in modes 2 and 3, where Q is off, is D_5 short-circuited, and the voltage is zero and, for mode 1, when Q is on:

$$v_{D_5} = V_{C_1} = \frac{1+D}{1-D} V_s \tag{3.39}$$

For V_{D6}; and V_{D8} in mode 1 where Q is on, the two voltages are zero and for modes 2 and 3, where Q is off:

$$v_{D_6} = v_{D_8} = -V_{L_3} = \frac{D(1+D)}{(1-D)^2} V_s \tag{3.40}$$

For V_{D7}; in modes 2 and 3, where Q is off, D_5 is short-circuited, and voltage is zero and, for mode 1, when Q is on:

$$v_{D_7} = V_{C_1} = \frac{1+D}{1-D} V_s \tag{3.41}$$

For V_{D9}; in modes 2 and 3, when Q is turned off, D9 is short-circuits, for the mode 1, where Q is turned on:

$$v_{D_9} = V_{C_2} = V_o = \frac{(1+D)^2}{(1-D)^2} V_s \tag{3.42}$$

Table 3.2: Voltage Stress Across the Semiconductor Components in CCM

	Mode1	Mode2 or Mode3
v_Q	0	$V_s \frac{(1+D)^2}{(1-D)^2}$
v_{D_1} & v_{D_3}	0	$V_s \frac{D}{1-D}$
v_{D_2}	V_s	0
v_{D_4}	0	$V_s \frac{2D(1+D)}{(1-D)^2}$
v_{D_5}	$V_s \frac{1+D}{1-D}$	0
v_{D_6} & v_{D_8}	0	$V_s \frac{D(1+D)}{(1-D)^2}$
v_{D_7}	$V_s \frac{1+D}{1-D}$	0
v_{D_9}	$V_s \frac{(1+D)^2}{(1-D)^2}$	0

3.5 Parameter Selections and Simulation Results

In this section simulation result for validation using PSCAD / EMTDC-V4.2 is presented. The results are as follows:

3.5.1 Parameter Selection

The parameter selection is to determine the inductance and the capacitance of the inductor and capacitor respectively, given the desired output voltage V_o and output current I_o, a switching period T and pre-assigned permitted fluctuation range $x_L\%$ for inductance and $x_C\%$ for the capacitance.

Inductance of an inductor can be defined as

$$L = \frac{V_L dt_L}{di_L} \tag{3.43}$$

Where $dt_L = DT$ is the time when the switch is on, and di_L is inductor current ripple which is express in terms of the fluctuation factor $x_L\%$ as

$$di_L = x_L\% I_L \tag{3.44}$$

And,

$$I_{L1} = I_{L2} = I_o \frac{1+D}{(1-D)^2} \tag{3.45}$$

$$I_{L3} = I_{L4} = I_o \frac{1}{1-D} \tag{3.46}$$

Using the inductor currents equations (3.45), (3.46) and average inductor voltages (3.33) and (3.34) in to (3.44) and (3.43)

$$L_1 = L_2 = \frac{V_s D(1-D)^2 T}{x_L\% I_o (1+D)} \tag{3.47}$$

$$L_3 = L_4 = \frac{V_s (1+D) DT}{x_L\% I_o} \tag{3.48}$$

Similarly, capacitance of the capacitor is defined as

$$C = \frac{I_C dt_C}{dv_C} \tag{3.49}$$

Where $dt_C = DT$ is the time when the switch is on, and dv_C is capacitor voltage ripple which can be express in terms of the fluctuation factor $x_C\%$ as

$$dv_C = x_C\% V_C \tag{3.50}$$

The capacitor currents $I_{C1} = 2I_{L3}$ and $I_{C2} = I_o$ when the switch Q is on, then using these two equations and (3.50) in to (3.49)

$$C_1 = \frac{2I_o DT}{x_C\% V_{in}(1+D)} \tag{3.51}$$

$$C_2 = \frac{I_o(1-D)^2 DT}{x_C\%(1+D)^2 V_{in}} \tag{3.52}$$

3.5.2 Simulation Results

Following parameters are assumed for the simulation: $C_1 = 220\mu F, C_2 = 470\mu F, L_1 = L_2 = 100\mu H, L_3 = L_4 = 200\mu H,\ T = 10\mu s, V_{in} = 12V$.

Figure 3.12 (a)-(f) shows the simulation result for case one, with duty ratio $D = 0.5\ and\ load\ R = 400\Omega$. From the converter simulation result waveforms, it can be seen that; the output voltage V_o is approximately $108.7\,V$, which is approximately equal to the calculated value of $108\,V$, calculated using equation (3.28). the average values of the inductor currents $IL_1 = IL_2 = 1.6A,\ IL_3 = IL_4 = 0.9A$, average values of the capacitor currents $IC_1 = 0.96$. Furthermore, the current flows through the inductors IL_1 (figure 3.12 (b)) and IL_3 (figure 3.12 (c)) are continuous and therefore case one is continuous current mode (CCM).

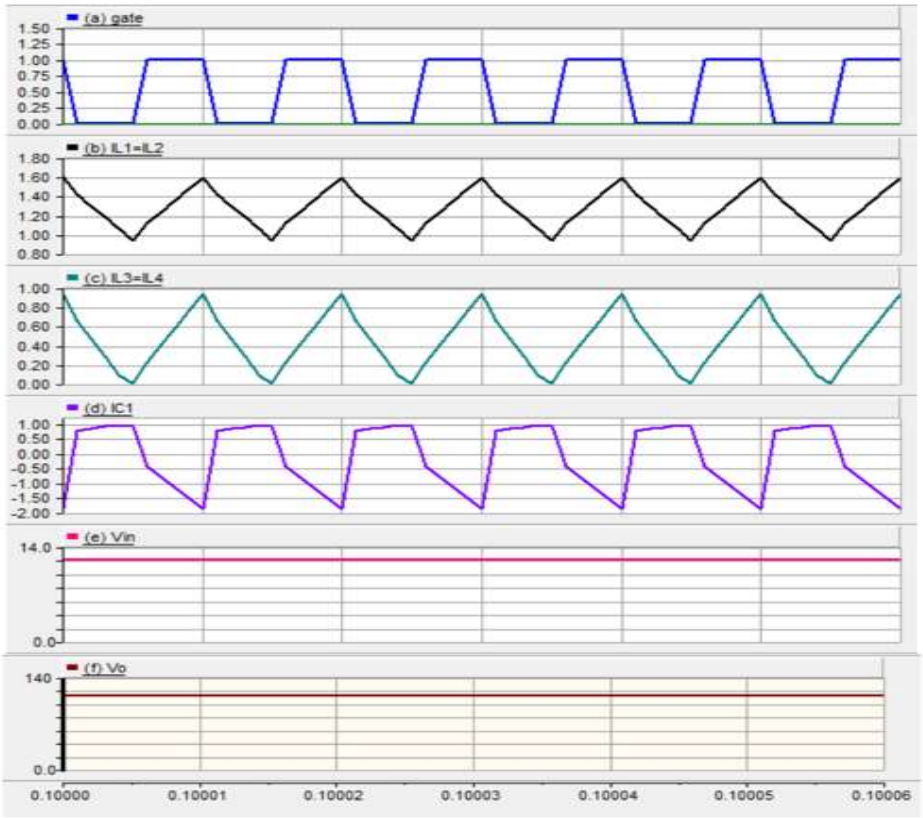


Figure 3.12: Simulation Results in Case one (a) VGS Switch voltage source (b) L_1 inductor current IL_1 (c) L_3 inductor current IL_3 (d) C_1 Capacitor current (e) Input Voltage V_{in} (f) Output Voltage V_o.

Figure 3.13 (a)-(f) shows the simulation result for the second case, with duty ratio$D = 0.2$ and load resistance $R = 200\Omega$. The converter current and voltage waveforms for an input voltage $V_{in} = 12V$ are as follows; output voltage V_o is approximately $27\,V$, which is approximately equal to the calculated value of $27\,V$, calculated using equation (3.28). The average values of the inductor currents $IL_1 = IL_2 = 0.37A$, $IL_3 = IL_4 = 0.23A$, average values of the capacitor currents $IC_1 = 0.24A$. Furthermore, the current flows through the inductors IL_1 (figure 3.13 (b)) and IL_3 (figure 3.13 (c)) are continuous and therefore case two is also CCM.

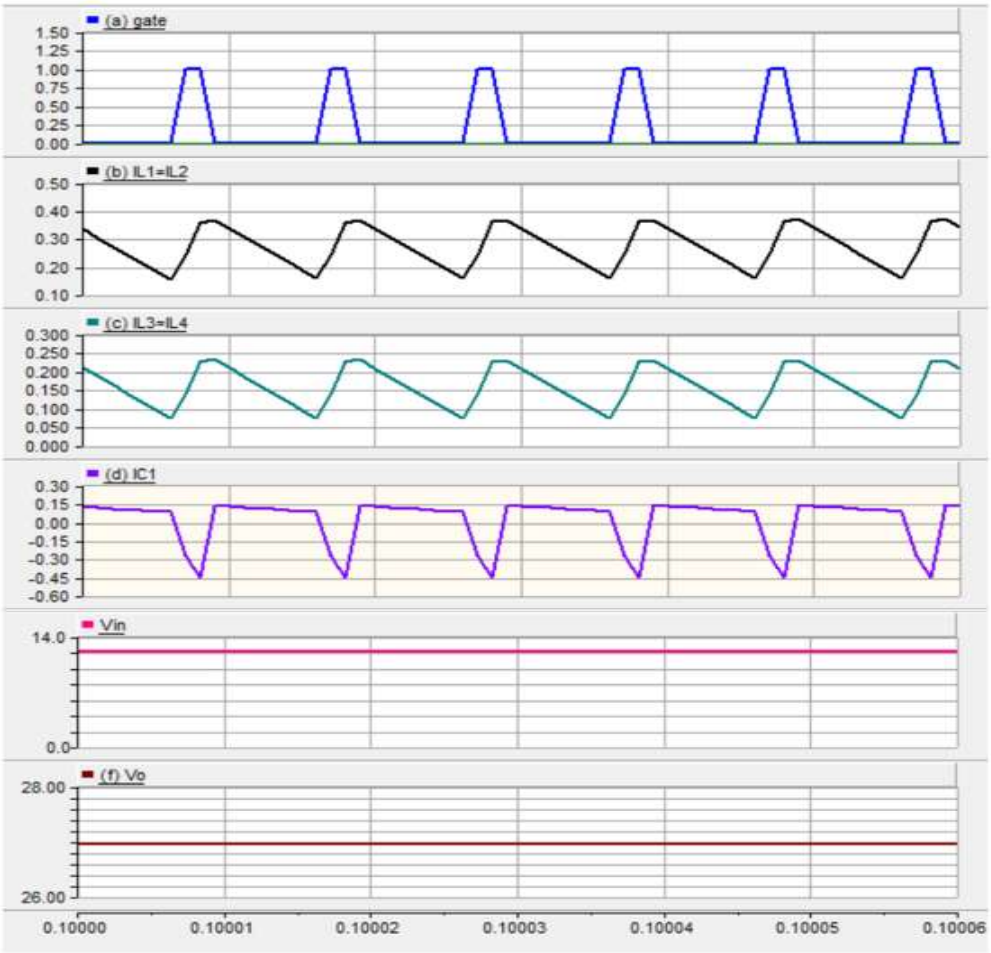


Figure 3.13: Simulation Results in Case two (a) VGS Switch voltage source (b) L_1 inductor current IL_1 (c) L_3 inductor current IL_3 (d) C_1 Capacitor current (e) V_{in} input voltage (f) Output Voltage V_o.

Figure 3.14 (a)-(f) shows the simulation result for this case, with duty ratio $D = 0.52$ and load resistance $R = 400\Omega$. The converter current and voltage waveforms for an input voltage $V_{in} = 12V$ are as follows; output voltage V_o is approximately $120\,V$, which is approximately equal to the calculated value of $120.33\,V$, calculated using equation (3.28). The average values of the inductor currents $IL_1 = IL_2 = 1.5\,A$, $IL_3 = IL_4 = 0.9\,A$, average values of the capacitor currents $IC_1 = 0.9\,A$. Furthermore, the inductor current waveform IL_1 (figure 3.14 (b)) and IL_3 (figure 3.14 (c)) indicated that case three is discontinuous current mode (DCM).

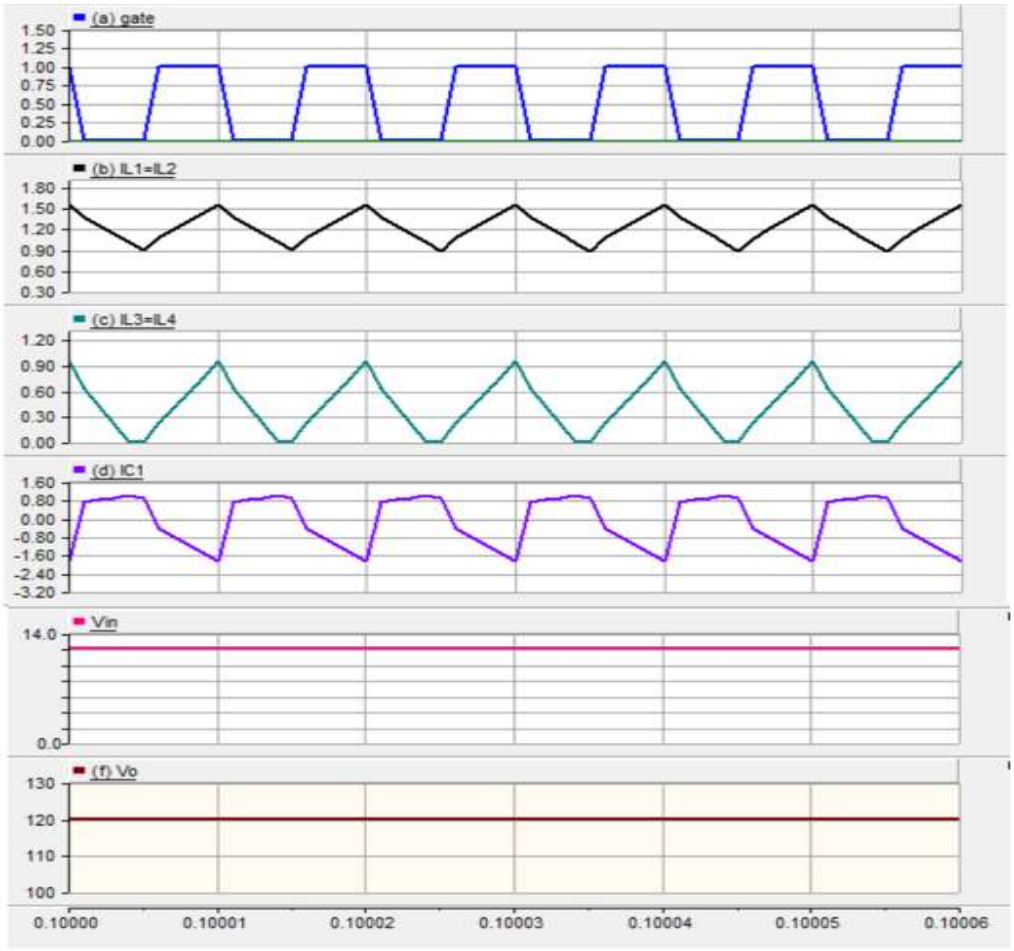


Figure 3.14: Simulation Results in Case three (a) VGS Switch voltage source (b) L_1 inductor current IL_1 (c) L_3 inductor current IL_3 (d) C_1 Capacitor current (e) Input voltage V_{in} (f) Output Voltage V_o.

Fig. 3.15 (a)-(f) shows the simulation result for this case, with duty ratio $D = 0.1$ and load resistance $R = 300\Omega$. The converter current and voltage waveforms for an input voltage $V_{in} = 12V$ are as follows; output voltage V_o is approximately $18.2\,V$, which is approximately equal to the calculated value of $18\,V$, calculated using equation (3.28). The average values of the inductor currents $IL_1 = IL_2 = 0.139\,A$, and $IL_3 = IL_4 = 0.09\,A$, average values of the capacitor currents $IC_1 = 0.028\,A$. Furthermore, the inductor current waveform IL_1 (figure 3.15 (b)) and IL_3 (figure 3.15 (c)) indicated that case four is also discontinuous current mode (DCM).

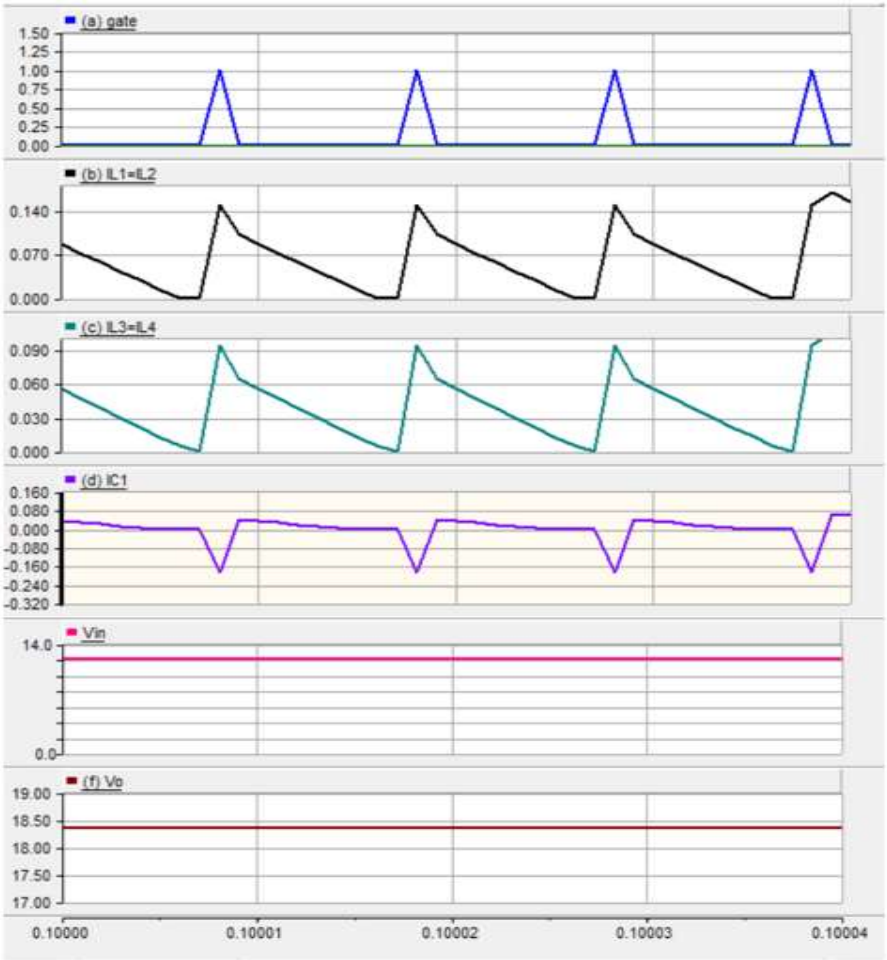


Figure 3.15: Simulation Results in Case four (a) VGS Switch voltage source (b) L_1 inductor current IL_1 (c) L_3 inductor current IL_3 (d) C_1 Capacitor current (e) Input voltage V_{in} (f) Output Voltage V_o.

Figure 3.16 (a)-(f) shows the simulation result for this case, with duty ratio $D = 0.25$ and load resistance $R = 500\Omega$. The converter current and voltage waveforms for an input voltage $V_{in} = 12V$ are as follows; output voltage V_o is approximately $35.4\,V$, which is approximately equal to the calculated value of $33.33\,V$, calculated using equation (3.28). The average values of the inductor currents $IL_1 = IL_2 = 0.31\,A$, and $IL_3 = IL_4 = 0.22\,A$, average values of the capacitor currents $IC_1 = 0.34\,A$. Furthermore, the inductor current waveform IL_1 (figure 3.16 (b)) and IL_3 (figure 3.16 (c)) indicated that case five is also discontinuous current mode (DCM).

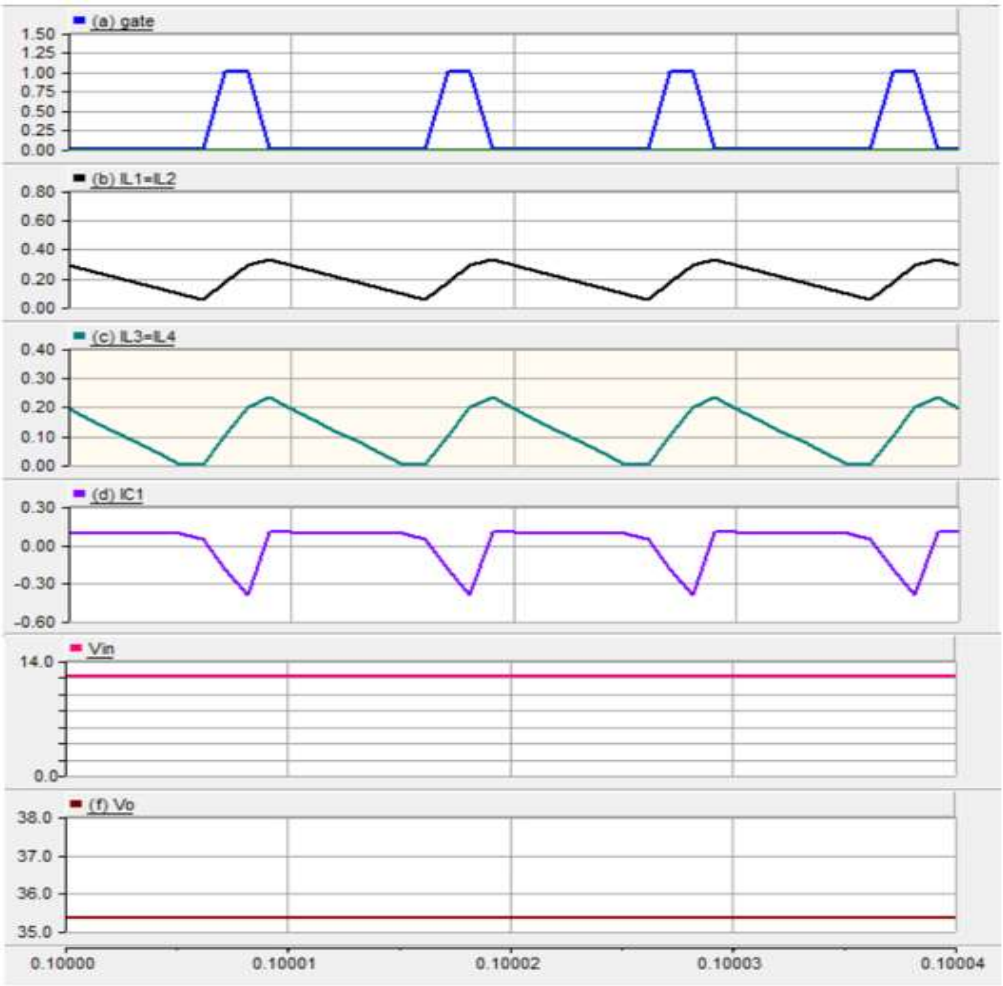


Figure 3.16: Simulation Results in Case five (a) VGS Switch voltage source (b) L_1 inductor current IL_1 (c) L_3 inductor current IL_3 (d) C_1 Capacitor current (e) Input voltage V_{in} (f) Output Voltage V_o.

Figure 3.17 (a)-(f) shows the simulation result for this case, with duty ratio $D = 0.13$ and load resistance $R = 400\Omega$. The converter current and voltage waveforms for an input voltage $V_{in} = 12V$ are as follows; output voltage V_o is approximately $20.5\,V$, which is approximately equal to the calculated value of $21\,V$, calculated using equation (3.28). The average values of the inductor currents $IL_1 = IL_2 = 0.16\,A$, and $IL_3 = IL_4 = 0.11\,A$, average values of the capacitor currents $IC_1 = 0.04\,A$. Similarly, the inductor current waveform IL_1 (figure 3.17 (b)) and IL_3 (figure 3.17 (c)) indicated that case six is also discontinuous current mode (DCM).

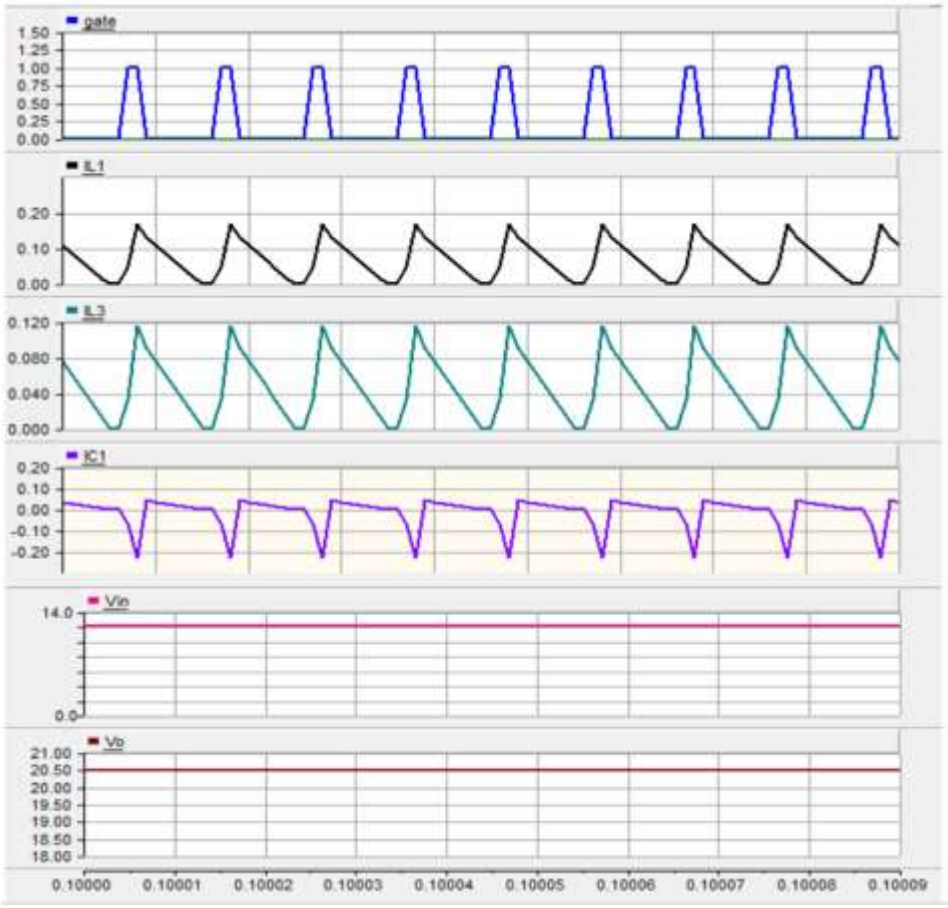


Figure 3.17: Simulation Results in Case six (a) VGS Switch voltage source (b) L_1 inductor current IL_1 (c) L_3 inductor current IL_3 (d) C_1 Capacitor current (e) Input Voltage V_{in} (f) Output Voltage V_o.

3.6 Conclusion

This chapter has described the design procedure and principle of operation of the 3-Z-Network converter. The theoretical analysis both in CCM and DCM consisting of six cases of the converter circuits has been carried out. To validate the theoretical result a simulation is conducted using PSCAD. In all the six cases the simulation results satisfied the corresponding theoretical results.

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

Step-up dc-dc converters also known as boost converters necessary in renewable energy systems, these converters are used to step up the low voltages obtained from source to higher voltages for grid-connected converters. These converters should have high voltage gain and be able to operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM), because of load instability in such applications.

Conventional boost converters will fail in many practical applications due to limited voltage gain and low efficiency, because of high power losses, voltage stress across the semiconductor devices and parasitic nature of their components. Therefore, from the practical point of view, voltage gain from these conventional converters is far less than applications' requirements. Cascading boost converters in series such as in quadratic converters has improve the voltage gain but despite the additional switches and control circuits used still the voltage gain is insufficient. Attempt to improve the converter gain by using voltage multipliers and interleaving technique requires additional control circuits and switching devices which makes the circuit more complicated and subsequently reduces the overall system reliability and efficiency and increase cost. Although the circuit's reliability and gain are improved by using isolation transformer but presence of transformer increases losses which reduces the efficiency and also there is a considerable increase in circuit volume and weight.

The LC impedance network invented by Peng, to serve as interface between input dc-source and the main converter circuit. The Z-source technique has solved many of the limitations of conventional converters. Z-source converters can provide a high voltage gain and can work in both CCM and DCM. Nevertheless, the output-voltage of these Z-source converters is not sufficient for many industrial applications especially the renewable energy applications.

In this thesis, design and simulation of a three Active-Z-network boost converter is presented. This converter is unique for the fact that contrary to conventional Z-networks that usually contain passive elements, this converter contains active Z-networks. The converter has all the advantages of Z-source converter including high voltage gain and it can also operate in both normal (CCM) and abnormal (DCM) load conditions.

The converter circuit consist of three active Z-network, Z-network 1 and Z-network 3 act as the first and second boost stages respectively, while Z-network 2 which contains the switching device serves as the switching stage. Hence, only one switch is used in this topology.

The steady state analysis of the converter has been conducted and six modes of operation are considered based on the switch and diodes conditions. Various combination of these modes are grouped and analyzed into six cases depending on the inductor and capacitor currents. In all the six operation modes suitable equivalents circuits and key waveforms are used for the analysis. Two cases correspond to continuous conduction mode (CCM) and the remaining four cases discontinuous conduction mode (DCM). The converter is said to be operating in CCM when inductor current never stay at zero-level within the switching cycle, and is said to be in DCM when the current stays at zero for some interval within the switching cycle.

In all the cases voltages and currents relationships are obtained by using Kirchoff's laws voltage stress across all the semiconductor components are established. The converter voltage gain is obtained and the result is plotted and compared with voltage gains of conventional converter and quadratic converter which shows that the 3-Z-Network converter gain is higher compared with others.

Simulation of the converter circuit is done to verify the feasibility of the converter in practical applications, and verify the results obtained theoretically. Using simulation, deep idea about the system can be obtained and possible improvements can be made by the designer before experiments.

The well-known software PSCAD / EMTDC-V4.2 is used for the simulation and the results is reported. The output voltage and average currents through the inductors and capacitors from both the theory and simulation are compared. In all the six cases the simulation results satisfied the corresponding theoretical results.

The presented converter topology uses a single switch and provide reduction in voltage stress and increase in efficiency. It can reach a high voltage gain required for many industrial applications especially renewable energy systems, to increase the low voltage from clean sources such as photovoltaic (PV) arrays and fuel cells to high voltage for grid-connected converters.

4.2 Future work

Possible improvements can be made to further the performance of this converter. An attempt should be made to improve the voltage gain of this converter for applications that required a higher output voltage than this. To achieve higher voltage-gain for the same duty cycle, the switched-capacitor cell can be structured for n diodes and capacitors. The efficiency can also be improved by using soft-switching techniques to reduce switching stress and losses, proper selection of capacitors with smaller ESR. More detailed analysis should be carried out including prototype experiment.

REFERENCES

Abusara, M.A., Guerrero, J.M. & Sharkh, S. M. (2014). Line-interactive UPS for microgrids. IEEE Trans. *Ind. Electronics, 61*(3), 1292–1300.

Abutbul, O., Gherlitz, A., Berkovich, Y. & Ioinovici, A. (2003). Boost Converter with High Voltage Gain Using a Switched Capacitor Circuit. Proc. Int. Symp. on Circuits and Systems, 2003, Pp. III-296–III-299, III(296), 1–4.

Abutbul, O., Gherlitz, A., Berkovich, Y., Ioinovici, A. & Member, S. (2003). *Step-Up Switching-Mode Converter With High Voltage Gain Using a Switched-Capacitor Circuit*, *50*(8), 1098–1102.

Ahmadzadeh, T. & Babaei, E. (2015). Z-H buck converter: Analysis and simulation. In 6th Annual International Power Electronics, *Drive Systems, and Technologies Conference, PEDSTC* (pp. 436–441). IEEE. https://doi.org/10.1109/PEDSTC.2015.7093314

Al-Saffar, M. A., Ismail, E. H. & Sabzali, A. J. (2013). Family of ZC-ZVS converters with wide voltage range for renewable energy systems. *Renewable Energy*, *56*, 32–43. https://doi.org/10.1016/j.renene.2012.12.037

Axelrod, B. & Berkovich, Y. (2003). Transformerless Dc-Dc Converters With A Very High Dc Line-To-Load Voltage Ratio. I*n Int. Symp. on Circuits and Systems* (Vol. III, pp. 5–8).

Axelrod, B., Berkovich, Y. & Ioinovici, A. (2003). A Family of Interleaved DC – DC Converters Deduced From a Basic Cell With Winding-Cross-Coupled Inductors (WCCIs) for High Step-Up. *Proceedings of the 2003 International Symposium on Circuits and Systems, ISCAS '03*. 3(4), 1791–1801.

Bayhan, S., Trabelsi, M., Ellabban, O., Abu-Rub, H. & Balog, R. S. (2016). A five-level neutral-point-clamped/H-Bridge quasi-impedance source inverter for grid connected PV system. *IECON Proceedings* (Industrial Electronics Conference), 2502–2507. https://doi.org/10.1109/IECON.2016.7793710

Cacciato, M., Consoli, A., Attanasio, R., & Gennaro, F. (2010). Soft-switching converter with HF transformer for grid-connected photovoltaic systems. IEEE Transactions on Industrial Electronics, 57(5), 1678–1686. https://doi.org/10.1109/TIE.2009.2032201

Choi, W. Y. & Lee, C. G. (2012). Photovoltaic panel integrated power conditioning system using a high efficiency step-up DC-DC converter. *Renewable Energy, 41*, 227–234. https://doi.org/10.1016/j.renene.2011.10.023

Ellabban, O., & Abu-Rub, H. (2016). Z-Source Inverter: Topology Improvements Review. *IEEE Industrial Electronics Magazine, 10*(1), 6–24. https://doi.org/10.1109/MIE.2015.2475475

Feng, X., Liu, J. & Lee, F. C. (2002). Impedance specifications for stable DC distributed power systems. *IEEE Transactions on Power Electronics, 17*(2), 157–162. https://doi.org/10.1109/63.988825

Galigekere, V. P. & Kazimierczuk, M. K. (2012). Analysis of PWM Z-source DC-DC converter in CCM for steady state. *IEEE Transactions on Circuits and Systems I: Regular Papers, 59*(4), 854–863. https://doi.org/10.1109/TCSI.2011.2169742

Ge, B., Lei, Q., Qian, W. & Peng, F. Z. (2012). A family of Z-source matrix converters. *IEEE Transactions on Industrial Electronics, 59*(1), 35–46. https://doi.org/10.1109/TIE.2011.2160512

González-Santini, N. S., Zeng, H., Yu, Y. & Peng, F. Z. (2016). Z-Source Resonant Converter With Power Factor Correction for Wireless Power Transfer Applications. *IEEE Transactions on Power Electronics, 31*(11), 7691–7700. https://doi.org/10.1109/TPEL.2016.2560174

Hakemi, A., Sanatkar-Chayjani, M. & Monfared, M. (2017). Δ-Source Impedance Network. *IEEE Transactions on Industrial Electronics, 64*(10), 7842–7851. https://doi.org/10.1109/TIE.2017.2698421

Henn, G. A. L., Silva, R. N. A. L. & Prac, P. P. (2010). Interleaved-Boost Converter With High Voltage Gain. *IEEE Transactions On Power Electronics*, *25*(11), 2753–2761. https://doi.org/10.1109/TPEL.2010.2049379

Hossam-Eldin, A., Abdelsalam, A. K., Refaey, M. & Ali, A. A. (2018). A topological review on recent improvements of three-phase impedance source inverter. 2017 19th International Middle-East Power Systems Conference, MEPCON 2017 - Proceedings, 2018–Febru (December), 1106–1112. https://doi.org/10.1109/MEPCON.2017.8301320

Ismail, E. H., Al-Saffar, M. A., Sabzali, A. J. & Fardoun, A. A. (2008). A family of single-switch PWM converters with high step-up conversion ratio. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *55*(4), 1159–1171. https://doi.org/10.1109/TCSI.2008.916427

Ja'far, S.E.A.H.J. (2012). Design and Simulation of a Photovoltaic System with Maximum Power Control to Supply a Load with Alternating Current.

Kayatri, S., Rajan, S. E., & Vengatesh, R. P. (2016). Investigation of 3-Z-Network boost converter for Photovoltaic power generation system using MPPT control strategies. *In 2016 International Conference on Circuit, Power and Computing Technologies* (ICCPCT) (pp. 1–8). IEEE. https://doi.org/10.1109/ICCPCT.2016.7530144

Kim, J., Ha, K., Krishnan, R. (2012). Single-controllable-switch-based switched reluctance motor drive for low cost, variable-speed applications. *IEEE Transaction on Power Electronics*, *27*(1), 379–387.

Law, K. K., Cheng, K. W. E. & Yeung, Y. P. B. (2005). Design and Analysis of Switched-Capacitor-Based Step-Up Resonant Converters. *IEEE Transactions On Circuits And Systems*, *52(*5), 943–948.

Li, D., Loh, P. C., Zhu, M., Gao, F. & Blaabjerg, F. (2013). Generalized multicell switched-inductor and switched-capacitor Z-source inverters. *IEEE Transactions on Power Electronics, 28*(2), 837–848. https://doi.org/10.1109/TPEL.2012.2204776

Li, W., He, Y., He, X., Sun, Y., Wang, F. & Ma, L. (2013). Series asymmetrical half-bridge converters with voltage autobalance for high input-voltage applications. *IEEE Transactions on Power Electronics, 28*(8), 3665–3674. https://doi.org/10.1109/TPEL.2012.2227807

Li, W., Liu, J., Wu, J., & He, X. (2007). Design and analysis of isolated ZVT boost converters for high-efficiency and high-step-up applications. *IEEE Transactions on Power Electronics, 22*(6), 2363–2374. https://doi.org/10.1109/TPEL.2007.909195

Li, W., Xiang, X., Li, C., Li, W. & He, X. (2013). Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for distributed PV generation system. *IEEE Transactions on Power Electronics, 28*(1), 300–313. https://doi.org/10.1109/TPEL.2012.2199771

Li, Y., Jiang, S., Cintron-Rivera, J. G. & Peng, F. Z. (2013). Modeling and control of quasi-z-source inverter for distributed generation applications. *IEEE Transactions on Industrial Electronics, 60*(4), 1532–1541. https://doi.org/10.1109/TIE.2012.2213551

Liang, T. J., Chen, S. M., Yang, L. S., Chen, J. F. & Ioinovici, A. (2012). Ultra-large gain step-up switched-capacitor DC-DC converter with coupled inductor for alternative sources of energy. I*EEE Transactions on Circuits and Systems I: Regular Papers, 59*(4), 864–874. https://doi.org/10.1109/TCSI.2011.2169886

Liu, Y., Abu-Rub, H. & Ge, B. (2014). Z-source/quasi-Z-source inverters: Derived networks, modulations, controls, and emerging applications to photovoltaic conversion. *IEEE Industrial Electronics Magazine, 8*(4), 32–44. https://doi.org/10.1109/MIE.2014.2307898

Loh, P. C., Gao, F., Blaabjerg, F., Feng, S. Y. C. & Soon, K. N. J. (2007). Pulsewidth-Modulated Z-Source Neutral-Point-Clamped Inverter. *IEEE Transactions on Industry Applications, 43*(5), 1295–1308. https://doi.org/10.1109/TIA.2007.904422

Maker.io. (2016). Introduction to DC-DC Converters. Retrieved June 2, 2018, from https://www.digikey.com/en/maker/blogs/introduction-to-dc-dc-converters

Modules, P., Walker, G., Walker, G. R. & Sernia, P. C. (2015). Cascaded DC – DC Converter Connection of Cascaded DC – DC Converter Connection of Photovoltaic Modules, (January), 24–29. https://doi.org/10.1109/TPEL.2004.830090

Musavi, F., Edington, M., Eberle, W. & Dunford, W. G. (2011). Energy efficiency in plug-in hybrid electric vehicle chargers: Evaluation and comparison of front end AC-DC topologies. *IEEE Energy Conversion Congress and Exposition: Energy Conversion Innovation for a Clean Energy Future, ECCE 2011, Proceedings,* 273–280. https://doi.org/10.1109/ECCE.2011.6063780

Nguyen, M. K., Lim, Y. C. & Kim, Y. J. (2012). A modified single-phase quasi-Z-source ac-ac converter. *IEEE Transactions on Power Electronics, 27*(1), 201–210. https://doi.org/10.1109/TPEL.2011.2157362

Parikh, J. & Parikh, K. (2012). Growing pains: Meeting India's energy needs in the face of limited fossil fuels. *IEEE Power Energy Magazine, 10*(3), 59–66.

Peng, F. Z. (2003a). Z-source inverter. *IEEE Transactions on Industry Applications, 39*(2), 504–510. https://doi.org/10.1109/TIA.2003.808920

Peng, F. Z. (2003b). Z-source inverter. *IEEE Transactions on Industry Applications, 39*(2), 504–510. https://doi.org/10.1109/TIA.2003.808920

Prudente, M., Pfitscher, L. L., Emmendoerfer, G., Romaneli, E. F., & Gules, R. (2008). Voltage multiplier cells applied to non-isolated DC-DC converters. *IEEE Transactions on Power Electronics, 23*(2), 871–887. https://doi.org/10.1109/TPEL.2007.915762

Qian, W., Peng, F. Z. & Cha, H. (2011). Trans-Z-source inverters. *IEEE Transactions on Power Electronics, 26*(12), 3453–3463. https://doi.org/10.1109/TPEL.2011.2122309

Rosas-Caro, J. C., Peng, F. Z., Cha, H. & Rogers, C. (2009). Z-source-converter-based energy-recycling zero-voltage electronic loads. *IEEE Transactions on Industrial Electronics, 56*(12), 4894–4902. https://doi.org/10.1109/TIE.2009.2026374

Shen, M., Wang, J., Joseph, A., Peng, F. Z., Tolbert, L. M. & Adams, D. J. (2006). Constant boost control of the Z-source inverter to minimize current ripple and voltage stress. *IEEE Transactions on Industry Applications, 42*(3), 770–778. https://doi.org/10.1109/TIA.2006.872927

Tang, Y., Fu, D., Wang, T. & Xu, Z. (2015). Hybrid switched-inductor converters for high step-up conversion. *IEEE Transactions on Industrial Electronics, 62*(3), 1480–1490. https://doi.org/10.1109/TIE.2014.2364797

Tang, Y., Wang, T. & He, Y. (2014). A Switched-Capacitor-Based Active-Network. *IEEE Trans. Power Electron, 29*(6), 2959–2968.

Tang, Y., Zhang, C. & Xie, S. (2007). Z-source AC-AC converters solving commutation problem. *IEEE Trans. Power Electron, 22(*6), 2146–2154. https://doi.org/10.1109/PESC.2007.4342440

Transactions, I. & Electronics, P. (2015). A Novel High step-up converter with a quasi active switched-inductor structure for renewable energy systems. IEEE Transactions on Power Electronics, 8993. https://doi.org/10.1109/TPEL.2015.2480115

Tsai, J. C., Chen, C. L., Lee, Y. H., Yang, H. Y., Hsu, M. S. & Chen, K. H. (2011). Modified hysteretic current control (MHCC) for improving transient response of boost converter. *IEEE Transactions on Circuits and Systems I: Regular Papers, 58*(8), 1967–1979. https://doi.org/10.1109/TCSI.2011.2106231

Vinnikov, D. & Roasto, I. (2011). Quasi-Z-Source-based isolated DC/DC converters for distributed power generation. *IEEE Transactions on Industrial Electronics, 58*(1), 192–201. https://doi.org/10.1109/TIE.2009.2039460

Wei, J., Tang, Y. & Xie, S. (2010). Grid-connected PV system based on the series Z-Source inverter. *In Proceedings of 5th IEEE Conference on Industrial Electronics and Applications, ICIEA* (pp. 532–537). https://doi.org/10.1109/ICIEA.2010.5517096

Wijeratne, D. S. & Moschopoulos, G. (2012). Quadratic power conversion for power electronics: Principles and circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers, 59*(2), 426–438. https://doi.org/10.1109/TCSI.2011.2163976

Wildrick, C. M., Lee, F. C., Cho, B. H. & Choi, B. (1995). A method of defining the load impedance specification for a stable distributed power system - Power Electronics, *IEEE Transactions on. Power, 10*(3), 280–285.

Yilmaz, M. & Krein, P. T. (2013). Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles. *IEEE Trans. Power Electronics, 28*(5), 2151–2169.

Zhang, G., Member, S., Zhang, B. & Li, Z. (2014). A 3-Z-Network Boost Converter. *IEEE Transactions On Industrial Electronics, 46*(c), 1–11. https://doi.org/10.1109/TIE.2014.2326990