ZUHER R. KHALIFA ABOJELA

DESIGN AND SIMULATION OF Z-SOURCE BASED HALF-BRIDGE INVERTER

NEU 2019

DESIGN AND SIMULATION OF Z-SOURCE BASED HALF-BRIDGE INVERTER

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

By
ZUHER R. KHALIFA ABOJELA

In Partial Fulfilment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

NICOSIA, 2019

DESIGN AND SIMULATION OF Z-SOURCE BASED HALF-BRIDGE INVERTER

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

By
ZUHER R. KHALIFA ABOJELA

In Partial Fulfilment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

NICOSIA, 2019

ZUHER R.KHALIFA ABOJELA: DESINE AND SIMULATION OF Z-SOURCE BASED HAFE- BRIDGE INVERTER

Approval of Director of Graduate School of Applied Sciences

Prof. Dr. Nadire CAVUS

We certify this thesis is satisfactory for the award of the degree of Master of Science in Electrical and ElectronicEngineering

Examining Committee in Charge:

Assist. Prof. Dr. Sertan Kaymak	Committee Chairman, Department of Electrical and Electronic Engineering, NEU
Prof. Dr. Ebrahim Babaei	Supervisor, Department of Electrical and Computer Engineering, University of Tabriz-Iran
Assist. Prof. Dr. Parvaneh Esmaili	Co-Supervisor, Department of Electrical and Electronic Engineering, NEU
Assist. Prof. Dr. Ali Serener	Department of Electrical and Electronic Engineering, NEU
Assist. Prof. Dr. Lida Ebrahimi Vafaei	Department of Mechanical Engineering, NEU

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name: Zuher R. Khalifa Abojela

Signature:

Date:

ACKNOWLEDGEMENTS

I would like to express my deep and sincere gratitude to my research supervisor, Prof. Dr. Ebrahim Babaei, Near East University, Northern Cyprus, for giving me the opportunity to conduct this research by providing invaluable guidance throughout the process. His dynamism, vision, sincerity and motivation have deeply inspired me. He has taught me the methodology to carry out the research and to present the research works as clearly as possible. It was a great privilege and honor to work and study under his guidance. I am extremely grateful for what he has offered. I would also like to thank him for his friendship, empathy, and great sense of humor.

I would also like to take the time to thank my friends and family for their immense contribution, suggestions and moral support. I would also like to thank my examination committee for taking their time to review my thesis.

I am extremely grateful to my parents for their love, prayers, caring and sacrifices while educating and preparing me for my future. Also, I will like to express my thanks to my brothers and sister, for their support and valuable prayers.

To my parents…

ABSTRACT

Half-bridge inverters are suitable for many power electronics applications due to their simple structure, ease of control, versatility, and ability to produce high gain and efficiency. However, in some applications such as electromechanical power supplies for electroplating products there are special requirements to provide very high voltage gain and wide range of outputs such as symmetrical and asymmetrical voltages. The use of conventional half-bridge inverters in such applications is affected by current shoot-through problem, limited output voltage and unbalance voltage between input capacitors. This thesis focuses on the analysis and simulation of a Z-source based half-bridge inverter to address the limitations of the conventional HBI and make it capable for lots more applications. The equations of currents and voltages of all the components are derived, in order to find the minimum values of passive components (capacitors and inductors).

This inverter circuit is built upon the conventional half-bridge converter circuit by adding an impedance LC network known as Z-source between the source and the converter. A comprehensive description and steady state analysis of the inverter circuits are presented. In order to complement the theoretical analysis a simulation is conducted on the inverter circuits using PSCAD/EMTDC package.

The theoretical and simulation results show that the inverter circuit can solve the unbalance midpoint input voltage problem in addition to solving the issues of current shoot-through and limited output voltage. It also provides an improved efficiency compared to the two-LC network Z-source half-bridge converter since only one LC network is used here. It also produces a wide range of output voltage with reduction in component count, size, weight and cost. The inverter can satisfy the special requirements of the electromechanical power supplies used in electroplating technologies and many more applications.

***Keywords*:** Half-bridge inverter; Z-source; Z-source HBI; PSCAD/EMTDC package

ÖZET

Yarım köprü evirgeçler; basit yapıları, kontrol kolaylıkları, çokyönlülükleri ve yüksek kazanım ile etkinlikleri dolayısıyla birçok güç elektroniği uygulamaları için uygundur. Bununla birlikte, elektrolitik kaplama ürünleri için elektromekanik güç kaynakları gibi bazı uygulamalarda, çok yüksek voltaj kazanımı ve simetrik ile asimetrik voltajlar gibi geniş yelpazeli çıktıların temin etmek için özel gereksinimler vardır. Bu uygulamalarda konvansiyonel yarım köprü evirgeçlerin kullanımı; akımın gitme probleminden, girdi kapasitörleri arasındaki sınırlı çıktı voltajı ile dengesiz voltajdan etkilenir. Bu bitirme tezi, konvansiyonel HBI'ın kısıtlamalarını ele almak ve daha fazla uygulamaları yetenekli kılmak için Z-kaynak tabanlı yarım köprü evirgeç tasarım ve simülasyonu üzerinde odaklanmıştır.

Bu evirgeç elektrik devresi, kaynak ile değiştirici arasında Z-kaynak olarak bilinen bir empedans LC şebekesi ilave etmek suretiyle konvansiyonel yarım köprü değiştirici elektrik devresi üzerine kurulmuştur. Evirgeç devrelerin kapsamlı bir açıklaması ve durağan durum analizi sunulmuştur. Kuramsal analizi tümlemek için, PSCAD/EMTDC paket program kullanılarak evirgeç devreler üzerinde bir simulasyon yapılmıştır.

Kuramsal ve simülasyon sonuçları; akımın gitmesi ve sınırlı çıktı voltajı sorunlarının çözümüne ilaveten, evirgeç devrenin, dengesiz orta-nokta girdi voltajı problemini de çözebileceklerini göstermektedir. Ayrıca bu; iki-LC şebeke Z-kaynak yarım köprü değiştirici ile karşılatırıldığında, burada bir-LC şebeke kullanılmasından dolayı, etkinlikte bir gelişme sağlamaktadır. Bu ayrıca; bileşen sayısı, büyüklüğü, ağırlığı ve maliyetinin azaltılmasıyla da, geniş yelpazeli çıktı voltajı üretmektedir. Evirgeç, elektrolitik kaplama teknolojilerinde ve daha birçok uygulamalarda kullanılan elektromekanik güç kaynaklarının özel gereksinimlerini tatmin edebilir.

***Anahtar kelimeler*:** Yarım-köprü evirgeç; Z-kaynak; Z-kaynak HBI; PSCAD/EMTDC paket programı

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

DC:	Direct Current
AC:	Alternating Current
L-C:	Inductor-Capacitor
HBI:	Half-Bridge Inverters
ZSI:	Z-Source Inverter
ZS-HBI:	Z-Source Half-Bridge Inverter
ZCS:	Zero Current Switching
ZVC:	Zero Voltage Switching
PWM:	Pulse Width Modulation
PSCAD:	Power System Computer Aided Design

CHAPTER 1
INTRODUCTION

1.1 Overview

Power converters are frequently used in numerous applications to provide a desired power supply for many electronic equipment. Popular applications of inverters include in servomotor derives, renewable power systems, home appliances, office equipment, telecommunication devices, electrochemical power suppliers and many more. Power converters gives a regulated output higher than a given unregulated input for boost converters or lower output for buck inverters (Wen, Deng, Mao, & Batarseh, 2005). Half-bridge converters are prominent among the power inverter topologies, this is resulting from its simple structure, ease of control, versatility, small component count, and it's potent for producing high efficiency. These features have made them to be widely used in power electronics applications. (Win, Baba, Hiraki, Tanaka, & Okamoto, 2012). Moreover, half-bridge structures suitable for applications requiring medium-level power. Half-bridge dc-dc converters are traditionally control using complementary (asymmetric) control and symmetric control strategies, even though, introduction of Z-source network has pave a way for more flexible and efficient methods have (Vinnikov, Chub, & Liivik, 2015).

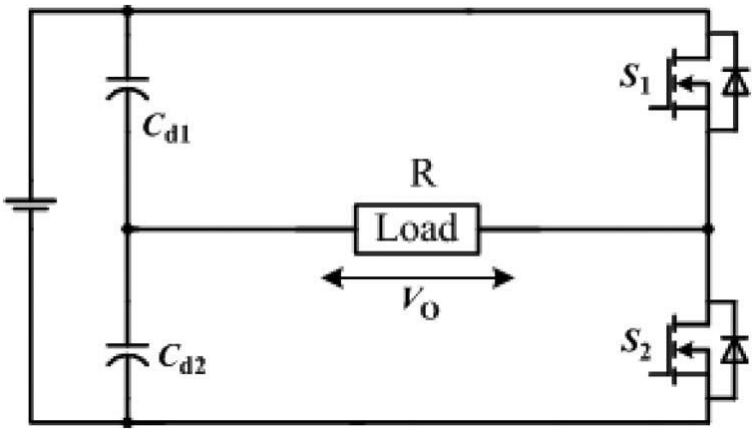


Figure 1.1: Conventional half-bridge inverter (Zhang et al., 2014)

Despite the aforementioned advantages of the half-bridge inverters the conventional topology has the following problems. 1) Current shoot-through problem, 2) Limited output-voltage problem, and 3) Unbalance voltage between input capacitors. As shown in Figure1.1, switches of conventional half-bridge inverters are arranged in series, the turn on and off of the switches cannot occur instantaneously, an interval occur within which both the switches are turned on and they are said to be operating in shoot-through mode, because of the occurrence of shoot-through heavy current flow through the switches which may destroy them, eventually affecting the inverter's reliability (Zhao, Yu, Leng, & Chen, 2012). Moreover, stability of the system is affected by unbalance between input capacitors that increases stress across semiconductor device and increases ripples (Hung, Shyu, Lin, & Lai, 2003; Z. Liu, Liu, Duan, & Kang, 2012).

There is a good number of proposed solutions in the literature for these problems. Boroyevich et al. invented a protection strategy to handle the shoot through problem. However, a special design process is required for the switches (Lai et al., 2010). Moreover, a digital signal processor (DIP) based protection scheme (Zhilei, Lan, & Yangguang, 2009) has been established, but their method considered only adding a control circuit to the inverter which added cost, complexity and affected the overall system stability. In order to address the limited output-voltage issue, two strategies have been used in (Kamli, Yamamoto, & Abe, 1996), using in parallel between the source and the output section, a step-up transformer or a boost circuit, the problem of this technique is that because of the fixed transformer turn-ratio the converter output voltage is also fixed. Extended power control algorithm was presented, to take care of the unbalanced voltage of the input capacitors (Joaquın, Santiago, & Jose, 2008). Also hybrid active-power quality compensator and voltage balancer circuit have been introduced in (Tanaka, Ishibashi, Ishikura, & Hiraki, 2010) and (Win et al., 2012) to solve the unbalanced midpoint issue.

In 2003 Peng (Peng, 2003) invented an impedance source inverter known as Z-network based inverter. ZSI has brought about a change that resolves many of the limitations of conventional current-source and voltage-converters.

Figure 1.2 shows a Z-source based half-bridge inverter, integrating Peng's Z-network with traditional HB inverter (Loh, Gao, Blaabjerg, Feng, & Soon, 2007), since two input capacitors served as dc-sources in the circuit, and one Z-source should be coupled with each input source, two impedance Z-source network are required in this topology as shown.

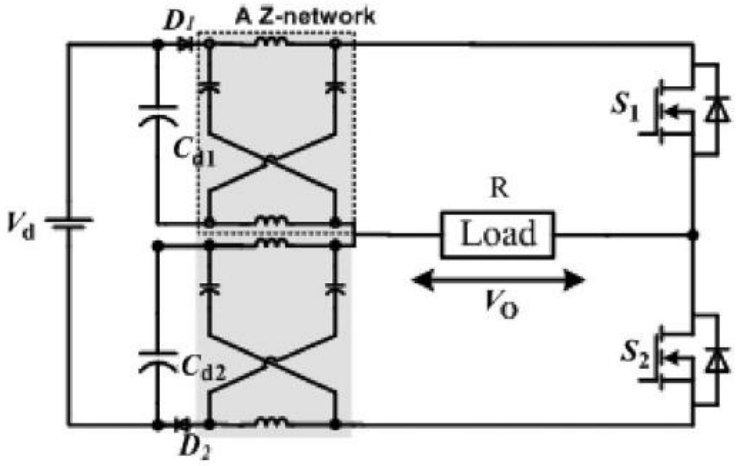


Figure 1.2: Z-source half-bridge converter with two Z-networks (Loh et al., 2007)

Both problems of output ac voltage limitation and current shoot-thrrough could be alleviated by using Z-network based half-bridge inverter. Nevertheless, additional circuits are introduced by using two LC networks, thereby increasing size, cost plus weight. Furthermore, for applications like electrochemical power supply, were several waveforms of different shapes with wider range of output voltage are necessary, the range of Z-source inverter can not satisfy such special requirements.

This thesis presents an improved version of Z-source based half-bridge inverter where only one impedance network is used. This new inverter is capable of solving the unbalance between input capacitors in addition to solving the issues of output voltage limitation and current shoot-through. Moreover, this inverter topology provides an improved efficiency compared to the two-LC network Z-source half-bridge inverter.

1.2 Thesis Objectives and Significance

The main objective of this thesis is to analyse and simulate a Z-source based half-bridge inverter. PSCAD software used for simulation, support theoretical result. This inverter differs from conventional HB inverter, and two-LC network Z-source based half-bridge inverters from sense that only one LC network is used. The inverter under study resolve solving the unbalance between input capacitors, issues of output voltage limitation and current shoot-through sufferd by conventional HB inverters. When compared to other Z-source inverters it provided much broader output voltage range with reduction in component count, size, weight, cost and efficiency. It can satisfy the special needs of electrochemical power supplies used in electroplating products which requires a broad range of outputs, with different waveforms including saw-tooth, square, step waves and recurrent pulses.

1.3 Scope and Limitations

For simplicity the analysis considered ideal components conditions and ignored freewheeling diodes in switches. The thesis is limited to simulation only, no prototype or experimental results are presented.

1.4 Structure of Thesis

Chapter 1: This chapter gives a general background on the thesis topic including the problem description, motivation and objectives.

Chapter 2: Provides a comprehensive review on conventional, soft-switching and Z-source based half-bridge inverters proposed in literature.

Chapter 3: Presents the power circuit description, mathematical analysis, equivalent circuits, converter operational modes and simulation results.

Chapter 4: Conclusion and recommendation.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

The function of power electronics converter is to condition electrical power taken from a power source to the form suitable for user loads, and therefore serves as an interface between user loads and the source. Depending on the type of input and output (alternative current (ac) or direct current (dc)) they operate on, power electronics converters are classified into ac-ac, ac-dc, dc-ac and dc-dc converters. Power electronics converters, that converts a dc input source into an ac output are referred to as inverters.

Power inverter circuits are construct are often constructed as either full-bridge or half-bridge depending on the number of switches used. Full-bridge inverters operates with four transistor switches for input signal, and there is also simultaneous conduction of the two switches and simultaneous cutting of the other this makes signal processing in full-bridge inverters complex and cumbersome. On the other hand, half-bridge inverter circuits utilize just two switches for input signal, and therefore it operates with one switch conducting when the other one is off. In this way, signal processing is easier and simpler (Win et al., 2012).

Half-bridge inverters are prominent among the power converter topologies, this is resulting from its simple structure, ease of control, versatility, small component count, and it's potent for producing high efficiency. These features have made them to be widely used in power electronics applications (Win et al., 2012). Moreover, half-bridge structures suitable for applications requiring medium-level power.

Half-bridge inverters are traditionally control using complementary (asymmetric) control and symmetric control strategies. Conventional half-bridge inverters have three major problems; because of having their input switches in series, current shoot-through occurs which may damage the whole inverter, limitation in the output ac voltage level which hinders its usage in many applications where high output voltage is a must and finally the unbalance midpoint input voltage which leads to instability in the inverter (Zhang et al., 2014).

However introduction of Z-source network has pave a way for more flexible and efficient methods of inverter design and have offered a solution to this problems (Vinnikov et al., 2015).

In line with that, this chapter presents a review of some of the most significant half-bridge inverter topologies existing in the literature. For the purpose of this review, three classes of half-bridge inverters are considered; the classical half-bridge inverters, the soft-switched half-bridge inverters and Z-source half bridge inverters as shown in figure 2.1. A number of articles are reviewed under each category.

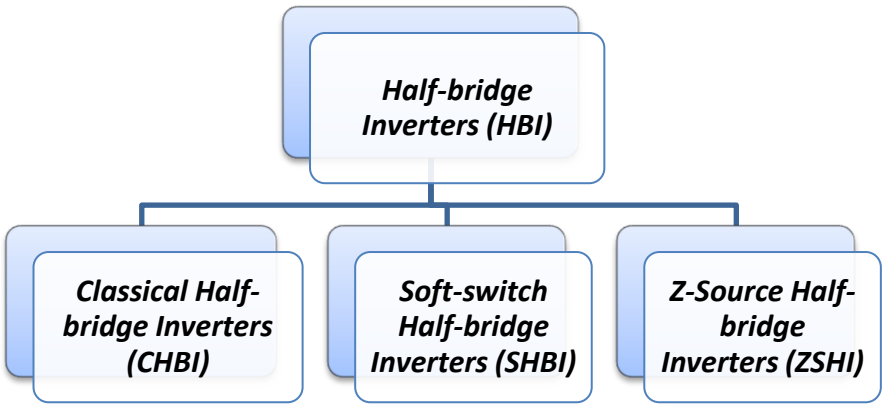


Figure 2.1: Classification of Half-bridge Inverters

2.2 Classical Half-bridge Inverters (CHBI)

Figure 2.2 shows the circuit diagram of classical half-bridge inverter which comprise of two transistor switches (IGBTs), a dc-voltage source, a load and two input capacitors. Despite the aforementioned advantages of the half-bridge inverters the classical topology has the following problems. 1) Current shoot-through problem, 2) Limited output-voltage problem, and 3) Unbalance voltage between input capacitors. As shown in figure 2.2, switches of conventional half-bridge inverters are arranged in series, the turn on and off of the switches cannot occur instantaneously, an interval occur within which both the switches are turned on and they are said to be operating in shoot-through mode.

Because of the occurrence of shoot-through heavy current flow through the switches which may destroy them, eventually affecting the converter's reliability (Zhao et al., 2012). Moreover, stability of the system is affected by unbalance between input capacitors that increases stress across semiconductor device and increases ripples (Hung et al., 2003; Z. Liu et al., 2012).

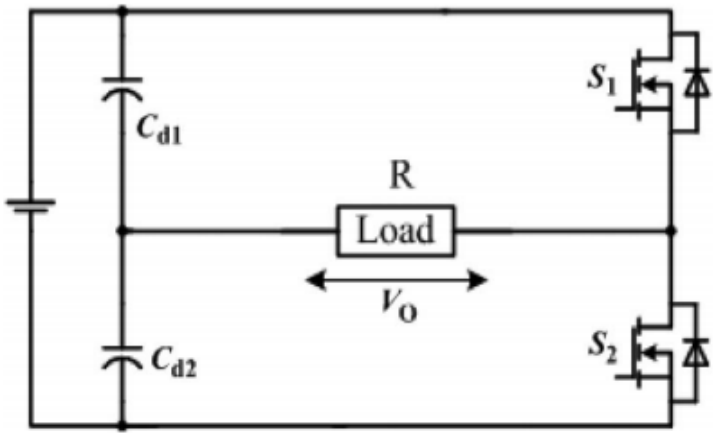


Figure 2.2: Conventional half-bridge inverter (Zhang et al., 2014)

There is a good number of proposed solutions in the literature for the above problems. Boroyevich et al. invented a protection strategy to handle the shoot through problem. The protection idea is shown in figure 2.3. To detect the shoot-through problem bidirectional switches consisting of relay and IGBT is inserted in the dc link. Shoot-through problem is identified in the converter and cleared. However, a special design process is required for the switches (Lai et al., 2010).

Moreover, a digital signal processor (DIP) based protection scheme (Zhilei et al., 2009) has been established, but their method considered only adding a control circuit to the inverter which added cost, complexity and affected the overall system stability.

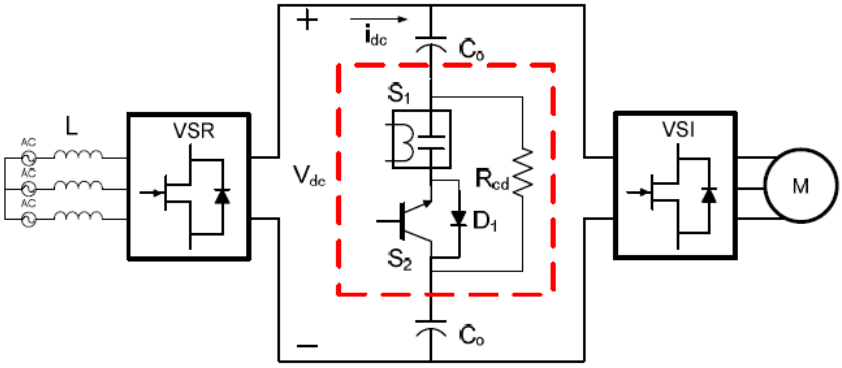


Figure 2.3: Protection Circuit proposed in (Lai et al., 2010)

In order to address the limited output-voltage issue, two strategies have been used in (Kamli et al., 1996), using in parallel between the source and the output section, a step-up transformer or a boost circuit, the problem of this technique is that because of the fixed transformer turn-ratio the inverter output voltage is also fixed.

Extended power control algorithm was presented, to take care of the unbalanced voltage of the input capacitors, in (Joaquın et al., 2008) and shown in figure 2.4. Also hybrid active-power quality compensator and voltage balancer circuit have been also introduced in (Tanaka et al., 2010) to solve the unbalanced midpoint issue of the input capacitors.

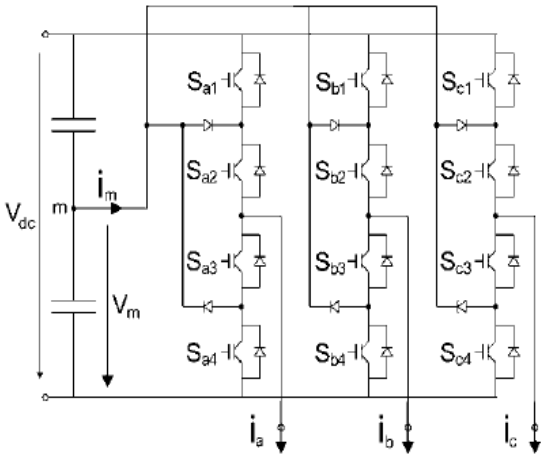
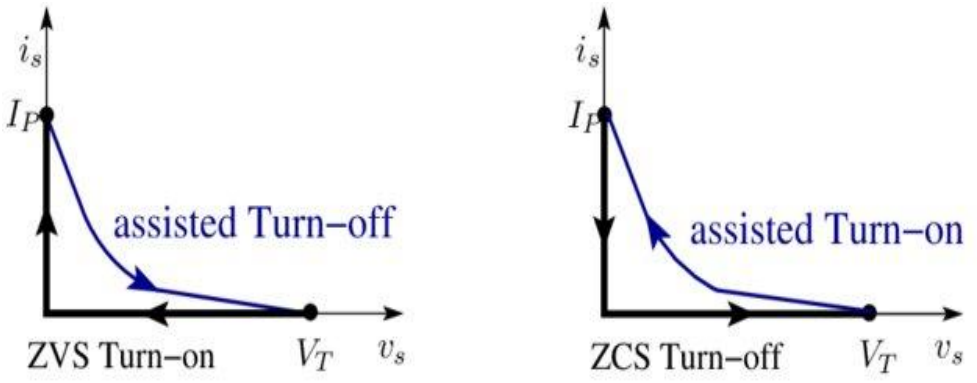


Figure 2.4: Neutral point clamped (NPC) V-source inverter (Joaquın et al., 2008)

2.3 Soft Switching of HBC

Hard change is opposed to progressive change. When we produce software switching circuits, we start with a hardware switching circuit, and then add circuits (power components) to make it flexible. Flexible support for smooth voltage / current transitions when switching. Under the "difficult change" it simply means that a special diet is not added to smooth the pattern. To achieve smooth transitions, the basic principle of all soft switching methods is the switching of zero voltage and zero current in the main switching devices. At high switching frequency, soft switching technologies (ZVS or ZCS) are used to achieve good performance and lower switching voltage. When switching with zero voltage (ZVS), the voltage on the device is zero just before switching it on. On the other hand, at zero current switching (ZCS), the current flowing through the device is zero just before the output. Figures 2.5 (a) and (b) illustrate the switching paths of the ZVS and ZCS.



(a) ZVS Trajectory (b) ZCS Trajectory

Figure 2.5: Switching trajectory of ZVS and ZCS (Neelam et, al 2011)

The switching or dynamic behavior of power semiconductor devices attracts the most attention from the fastest due to several reasons: optimal unity, power dissipation, electromagnetic and radio frequency interference problems and switching support networks. Changing software is another opportunity to reduce losses in electronic circuit breakers. In fact, the operation of electronic power switches in ZVS (zero voltage) or ZCS (zero current) mode is called “soft switching”. Software switching methods in recent years are of great interest for power switching applications. for high-power IGBT applications, preferably strong MOSFETs, with much higher conductivity losses. The Figure 2.7 shows

the circuit diagram of soft switching and the salient element is the nonlinear reactor, shown enclosed in a box with constant secondary bias current.

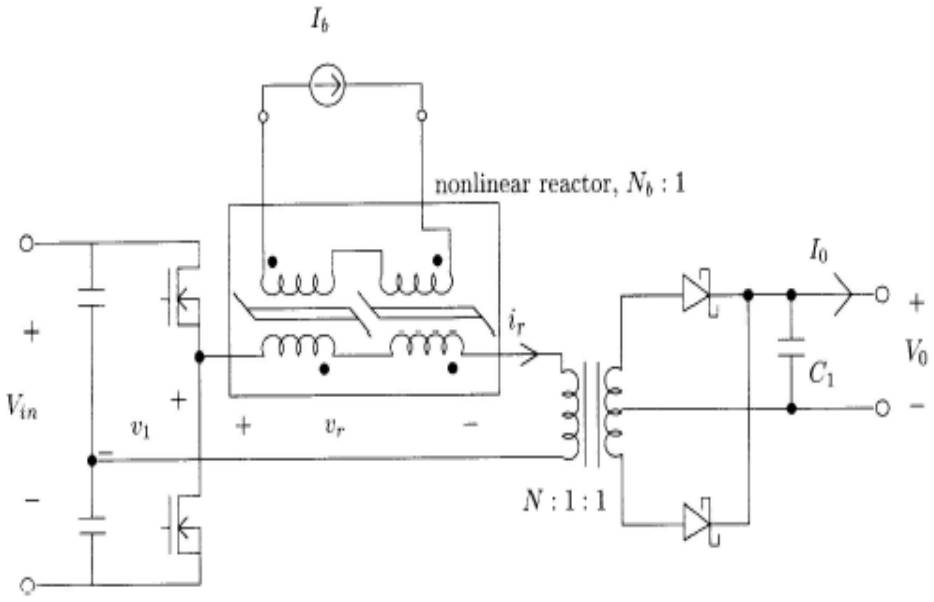


Figure 2.6: Soft switching circuit diagram (Al-Saffar, Ismail, & Sabzali, 2013)

2.4 Z-Source Inverters

As there exist two traditional converters which are voltage source and current source converters. But these converters have the following common problems; they are either a boost or a buck converter and cannot be a buck-boost converter. That is, their obtainable output voltage range is limited to either greater or smaller than the input voltage, their main circuits cannot be interchangeable. In other words, neither the V-source converter main circuit can be used for the I-source converter and nor vice versa and they are vulnerable to EMI noise in terms of reliability.

To solve the aforementioned problems related with the traditional voltage source and voltage source converters an impedance source power converter (Z-Source converter) is introduced in (Peng, 2003), after the introduction of the Z-source inverter (ZSI) various topologies have been introduced by modifying and utilizing this circuit. This include ac-to-dc, dc-to-ac, dc-to-dc and ac-to-ac, converter operations, as well as full-bridge and half-bridge conversions.

The ZSI has interesting and unique properties like single-stage conversion, high voltage gains and buck-boost capability. It uses a specially designed $LC - Network$ to couple the inverter source to the main inverter circuit and boost the input voltage. This greatly enhance the reliability of the inverter and make it suitable for many applications. Many ZSI structures have been discussed in literature (Ellabban & Abu-Rub, 2016).

Figure 2.7 shows the basic circuit of ZS converter. This circuit comprises of a dc source or load which may be a current-source or voltage-source or loads. the source is connected to the main circuit through an "X-shape" $LC - network$ to provide the impedance source. This dc network contains capacitors C_1 and C_2 along with two inductors L_1, and L_2.

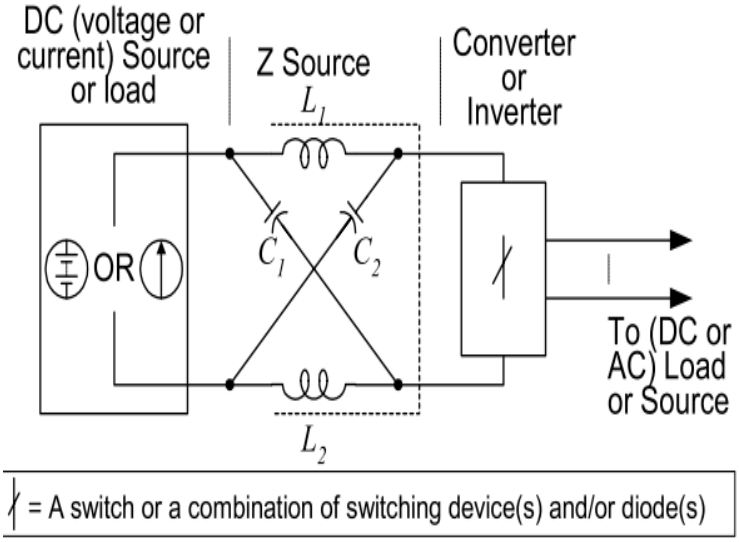


Figure 2.7: General Structure of ZS Converter (Ellabban & Abu-Rub, 2016)

For instance, the dc input source may be a fuel cell, thyristor-converter as a source, diode rectifier, battery source, a capacitor or inductor or any of their combination. A series or anti-parallel combination of switches and diodes can be used as shown in Figure 2.8 and Figure 2.9 respectively.

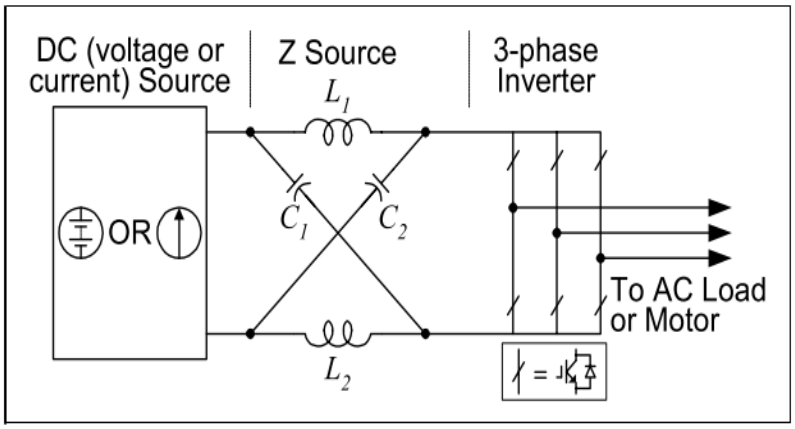


Figure 2.8: ZS converter with anti-parallel combination of diodes and switches (Abu-Rub et al, 2016)

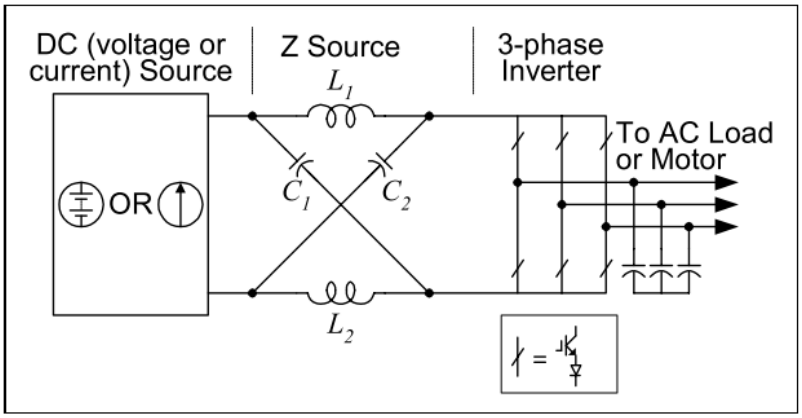


Figure 2.9: ZS converter with anti-parallel combination of diodes and switches (Ellabban & Abu-Rub, 2016)

Nevertheless, above ZSI circuits have some shortcomings and challenges. Such as high starting current inrush, inability to handle heavy load, input current discontinuity, power flow in one direction, reduced efficiency, to mention some. Therefore, numerous improvements have been proposed in the literature to alleviate these shortcomings of classical ZS converter topology.

To cite some examples, Figure 2.10 Shows an improved version of ZSI obtained by modifying classical ZSI structure. In this topology the connections of the input diodes are

reversed and then interchange their location with the inverter bridge. The number of components used is equal to those in classical ZSI structure. It solved the problem of current inrush while maintaining the voltage conversion gain. It also significantly decreases the voltage stress (Yu Tang, Shaojun Xie, Chaohua Zhang, & Zegang Xu, 2009). Lower current inrush and voltage stress is also achieved in (Wei, Tang, & Xie, 2010) by connecting the impedance networks in cascade.

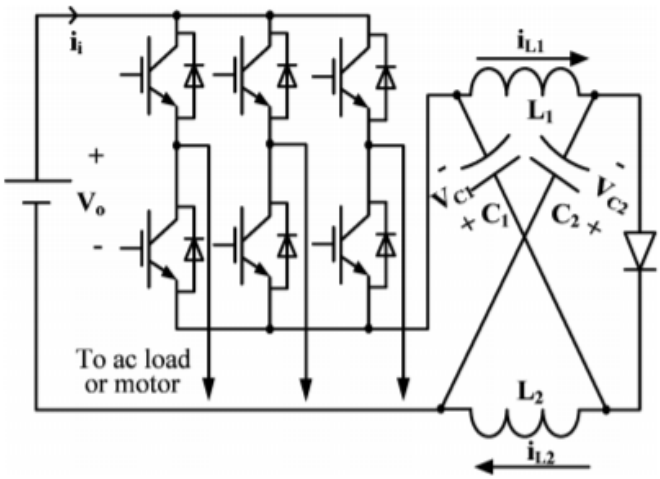


Figure 2.10: Improved ZSI (Wei et al., 2010)

Another modification of the ZSI is presented in (Y. Liu, Abu-Rub, & Ge, 2014). This converter called "quasi-ZSI (QZSI)" is shown in Figure 2.11, it has discontinuous input current, and hence provide numerous advantages compared with classical ZSI structure. This include less noise since common earthing is use for input and the dc-link, and reduces the ratings of the impedance network components. Further modification based on similar passion is presented in (Anderson & Peng, 2008) and (Ge et al., 2013) as shown in Figure 2.12. Here, continuous current is used in the input and it provides an additional advantage of reduced stress in the source.

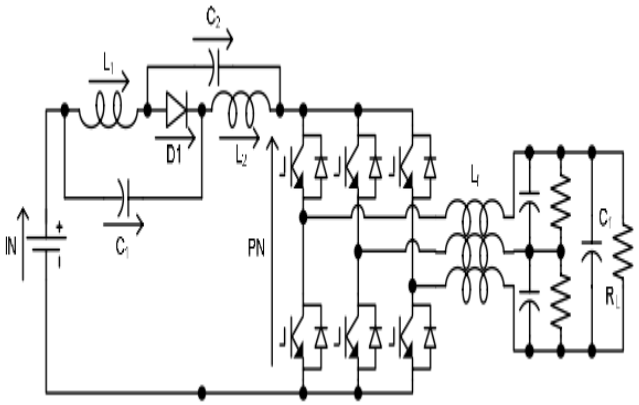


Figure 2.11: QZSI with discontinuous input current (Y. Liu et al., 2014)

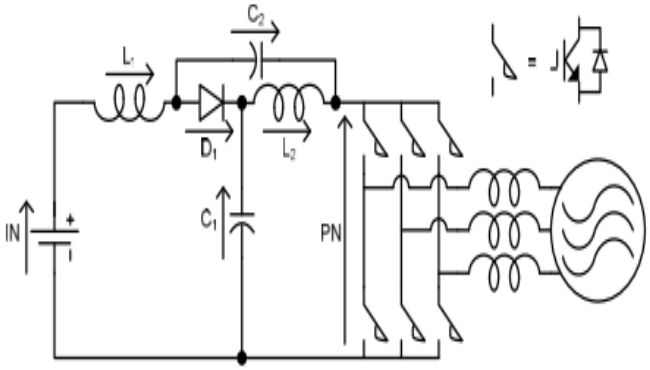


Figure 2.12: QZSI with continuous input current (Ge et al., 2013)

Figure 2.13, shows a "Quasi-resonant soft-switching Z-source inverter (QRSSZSI)" designed to achieve a soft switching in ZSI. The circuit is produced by adding a "quasi-resonant" circuit with a single complementary switch to a classical ZSI structure. With this topology zero voltage switching (ZVS) is achieved for all the inverter bridge switches. Due to the soft-switching higher efficiency is attained (Zhu, Chen, Lee, & Tsutomu, 2012).

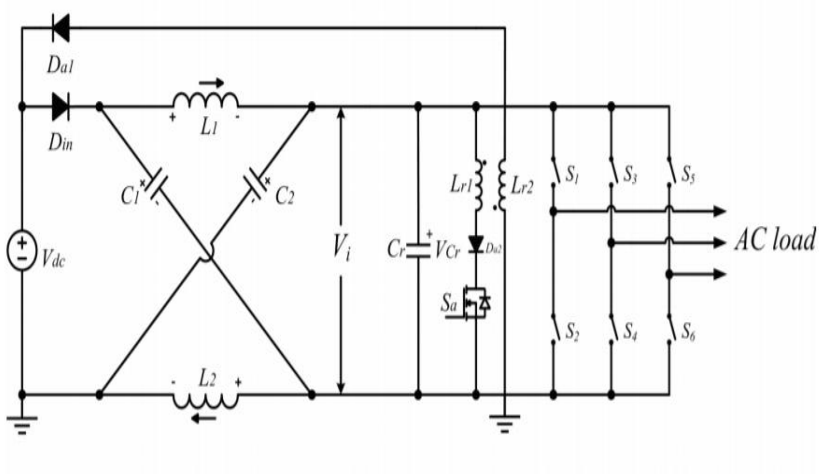


Figure 2.13: Quasi-resonant soft-switching ZSI (Zhu et al., 2012)

2.4.1 Z-source Half-bridge Inverter

There is a good number of proposed inverter topologies produced by integrating Peng's Z-network with traditional half-bridge inverter. By using this technology Z-source based half-bridge converters are obtained.

In (Zhao et al., 2012) Zhao et al presented a new Z-source based switched dc-dc converter with isolation transformer. Two Z-networks are used to connect the input source to the main converter and the load to the main converter circuit. This converter topology is shown in Figure 2.14 , a high frequency transformer (HFT) is used to provide an isolation. It is composed of two half-bridge converters one in the primary part and the other in the secondary of the HFT. Two Z-networks are used, one to connect the input source to the main converter and the second one to connect the load to the main converter circuit.

In comparison with classical IBC, this topology provides a better voltage regulation, can operate on both voltage and current dc sources. Because of the isolation there is increase in efficiency. Furthermore, the presence of impedance network makes the converter more reliable, since it can handle the problem of current shoot through which limits the reliability of conventional half-bridge converter.

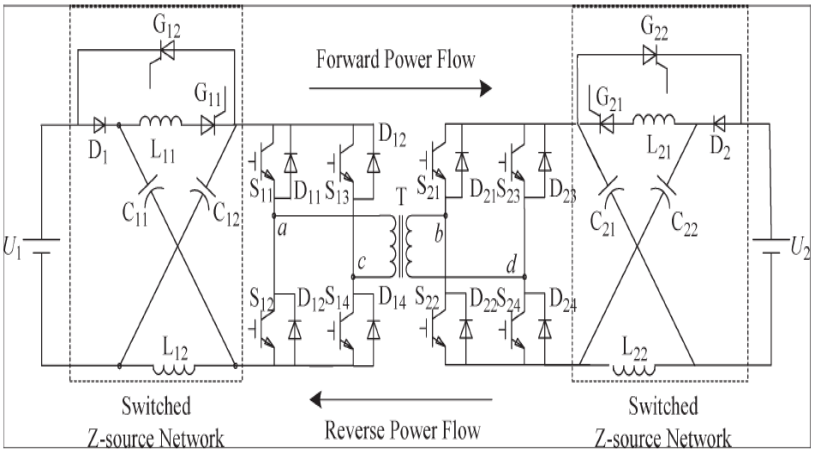


Figure 2.14: SZSIB dc-dc converter (Zhao et al., 2012)

Figure 2.15 shows a Z-source based half-bridge inverter, formed by integrating Peng's Z-network with traditional HB inverter (Loh et al., 2007). Since two input capacitors served as dc-sources in the circuit, and one Z-source should be coupled with each input source, two impedance Z-source network are required in this topology.

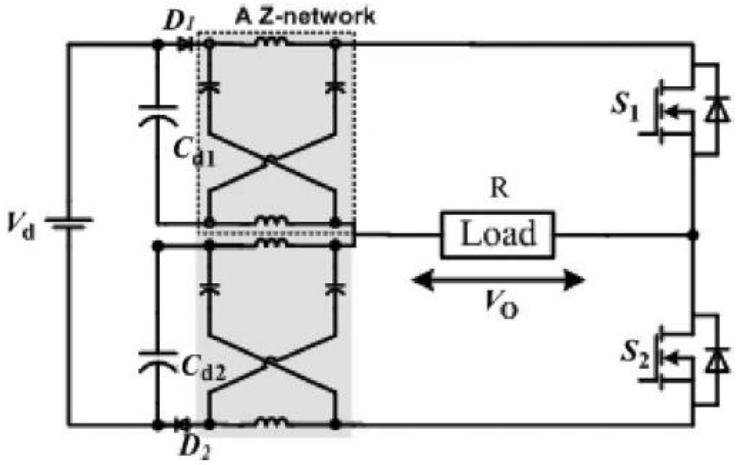


Figure 2.15: Z-source half-bridge converter with two Z-networks (Loh et al., 2007)

Both problems of output ac voltage limitation and current shoot-through could be alleviated by using Z-network based half-bridge inverter. Nevertheless, additional circuits are introduced by using two LC networks, thereby increasing size, cost plus weight. Furthermore, for applications like electrochemical power supply, were several waveforms

of different shapes with wider range of output voltage are necessary, the range of Z-source inverter cannot satisfy such special requirements.

Babaei et al (Babaei, Asl, & Babayi, 2016) present and analysed a unique half-bridge inverter circuit shown in Figure 2.16, this converter employs active circuit components instead of passive, replacing the inductors and capacitors with switches and diodes. When compared with the inverter in (Loh et al., 2007) this inverter provides a decrease in size, weight and significantly reduced the cost.

Furthermore, the new inverter topology has the advantage of creating zero output-voltage level. It provides a higher voltage gain compared to traditional counterpart; it possesses the capability of removing short circuit issues associated with the inverter leg. A detailed analysis of the inverter circuit in steady-state was presented. The experimental and theoretical results confirmed the significance of this topology. To further ascertain the advantages a comparison was made with classical inverter types.

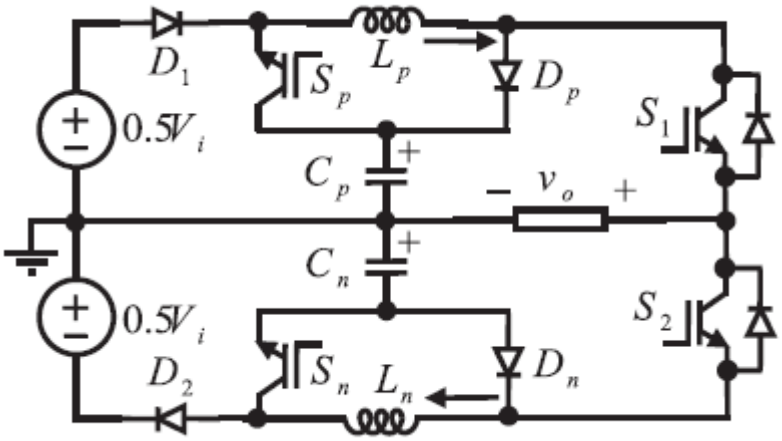


Figure 2.16: Power circuit of the proposed inverter (Babaei et al., 2016)

An improved version of Z-source based Half-bridge inverter where only one impedance network is used is also proposed (Zhang et al., 2014). This new inverter is capable of solving the unbalance between input capacitors in addition to solving the issues of output voltage limitation and current shoot-through. Moreover, this inverter topology provides an improved efficiency compared to the two-LC network Z-source half-bridge inverter.

The circuit arrangement of the inverter circuit is depicted in Figure 2.17 As shown, traditional half-bridge inverter consisting two switches S_1 and S_2, a diode D and two capacitors C_{d1} and C_{d2} is combined with an impedance LC network comprising inductors L_1 and L_2, and capacitors C_1 and C_2. The additional Z-source circuit is to protect the inverter dc source from current flow back. The inductors used in the Z-source are to handle the inverter shoot-through currents.

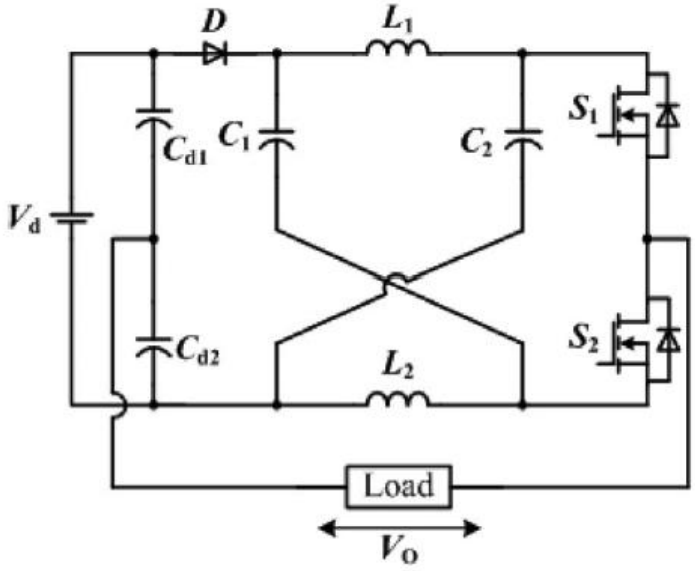


Figure 2.17: ZSI with single Z-network (Zhang et al., 2014)

This inverter differs from conventional HB inverter, and two-LC network Z-source based half-bridge inverters from sense that only one LC network is used. The inverter resolves the unbalance between input capacitors, issues of output voltage limitation and current shoot-through suffered by conventional HB inverters. When compared to other Z-source inverters it provided much broader output voltage range with reduction in component count, size, weight, cost and efficiency. It can satisfy the special needs of electrochemical power supplies used in electroplating products which requires a broad range of outputs, with different waveforms including saw-tooth, square, step waves and recurrent pulses.

Further attempt is made by Kumar and Veerachary to handle the deficiencies associated with two-Z-network inverters. They present an improved version of ZSHB converter suitable for applications where broad range of outputs, with different waveforms including saw-tooth, square, step waves and recurrent pulses, and variation in output voltage are

required. In comparison to conventional type, this topology provides a significant decrease in voltage stress across the capacitor and the switch.

In terms of circuit structure this converter circuit as shown in Figure 2.18 It interchanged the connection between the load and the impedance network contrary to the arrangement in traditional ZSHBC (Kumar & Veerachary, 2017).

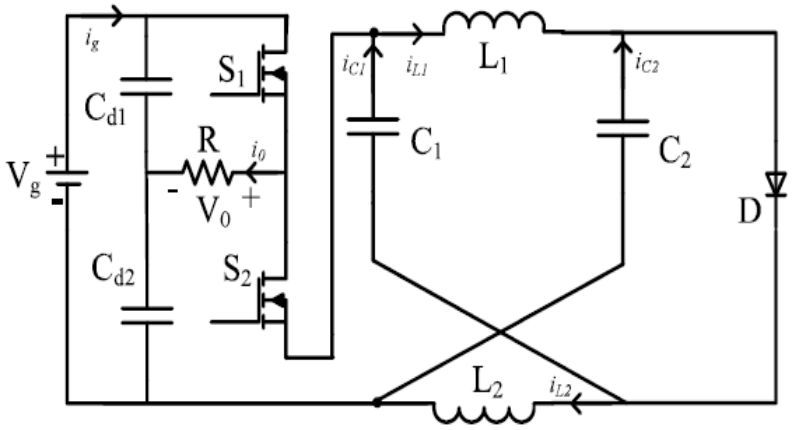


Figure 2.18: Z-source half-bridge converter (Kumar & Veerachary, 2017)

In a similar manner, a different Z-source based inverter structure; named "High-Voltage Gain Half-Bridge Z-Source Inverter With Low-Voltage Stress on Capacitors" is introduced in (Babaei & Asl, 2017). In this topology only one z-network (LC network) is employed.

The circuit arrangement for this inverter is depicted in Figure 2.19 As shown, the circuit consist of traditional half-bridge inverter consisting two switches S_1 and S_2, two diodes D_1 and D_2, two inductors L_1 and L_2, and capacitors C_1 and C_2. A dc-voltage source and a load. The additional Z-source circuit is to protect the inverter dc source from current flow back. The inductors used in the Z-source handles the inverter shoot-through currents (Babaei & Asl, 2017).

Contrary to traditional half-bridge inverter, this inverter circuit is capable of producing zero output-voltage level. It can as well provide a higher stabilized output-voltage with different range. It can work with nominal capacitor voltage rating with decrease stress and cost. Using mathematical analysis technique and experimental analysis are carried out to validated the performance. For the analysis in steady state two operation modes are

considered based on the diode's states; referred asynchronous and synchronous diodes operation modes.

To provide more reduction in weight, size and cost while increasing the voltage conversion gains, the impedance networks are connected in series. A correlation analysis between this inverter and previous one shows the exceptional performance of this inverter.

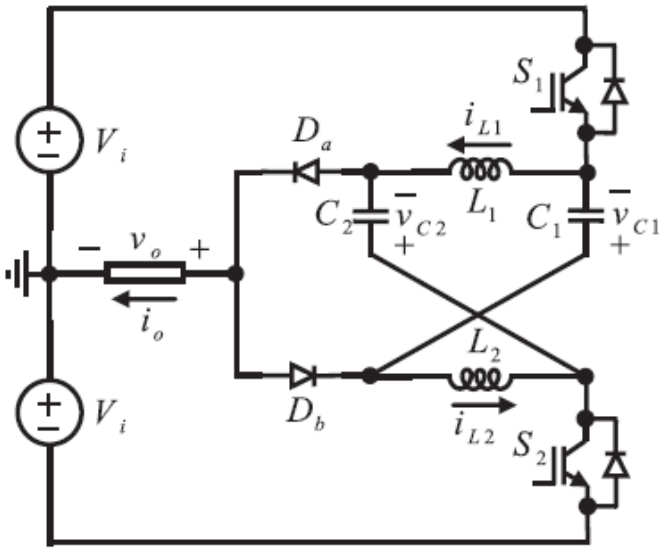


Figure 2.19: Power circuit of the proposed topology (Babaei & Asl, 2017)

2.4.2 Application of ZSHBI

Classical half-bridge inverters and Z-network HBI have many applications in several areas (Jangwanitlert & Sanaj, 2007; Lee et al., 2011; Silvestre, Pedro, & Quinta, 2008; Wu, Sun, Zhu, & Xing, 2016; Zhilei et al., 2009). To stress the importance of combining classical HBI with Z-network, a detailed discussion on potential application of ZSHBI in electro-chemical power supply conversion system is discussed in this sub-section.

A potential application where the use of ZSHBI is necessary is electro-chemical power system, because of its special requirements and characteristics. This power supply is required to produce a variety of output voltage waveforms, such as variable negative or positive output-voltages with varied rate ratios among the positive and negative voltages.

To realize this, engineers have to incorporate many series sub-circuits with complicated control strategies to create an overlapping waveform with multiple output voltages. Nevertheless, using these traditional approaches it's the output-voltage stabilization and control is cumbersome, and the additional sub-circuits used results in an increased in cost, size, components power losses, and the structure become bulky and leads to system instability.

One of the popular examples of electro-chemical supply system is electroplating technology. Figure 2.20 shows the basic diagram representing the principle of operation of electroplating process. This process works based on redox reaction (transfer of electrons), as shown the process consist of dc-voltage source, a solution and opposite charged electrodes. The aim is to force the metal ions to smoothly and evenly cover the negative (-ve) electrode surface. Unfortunately, direction of the dc source and current density have to be adjusted occasionally. In order to achieve that complex designs are required depending on the processes and products (HuY, PuZhiyuan, LingZhiyuan, & Yin, 2009).

The continues increase in applications that requires electro-chemical-based power supplies has made the demand on the electroplating product to increase exponentially. However, the recent advances in the design and implementation of Z-network based inverter circuit have responded well and the existing circuits discussed here can satisfy the special needs of electrochemical power supplies used in electroplating products which requires a broad range of outputs, with different waveforms including saw-tooth, square, step waves and recurrent pulses.

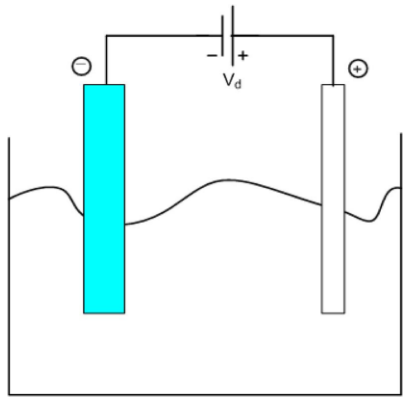


Figure 2.20: Diagram of electroplating (HuY et al., 2009)

2.5 Comparison between Conventional, Soft Switching and Z- Source Half Bridge Converter

The comparison of proposed converter with ZSHBC is presented in this section. The proposed converter has load voltage equal to ZSHBC and lesser than HVHBZSI, with least capacitor voltage stress and same switch voltage stress, without any additional component (Kumar et al., 2017). Table 2.1 represents the comparison based on number of components. The detailed comparison based on the voltage gain and voltage stress across the switches is presented in Table 2.2.

Table 2.1: Comparison Based on Number of Components

Relationship	**Conventional HBC**	**Soft Switching HBC**	**Z-Source HBC**
Input Voltage	V_d	V_{in}	V_d
Capacitors	2	3	4
Inductors	0	4	2
Diodes	2	2	3
Switches	2	2	2

Table 2.2: Comparison based on voltage gain and Voltage Stress across the switch.

	Conventional HBC	**Soft Switching HBC**	**Z-Source HBC**
Voltage Gain	$\frac{1}{2}(\frac{n_2}{n_2})\frac{1}{1-D}$	$\frac{4n+D}{1-D}$	$\frac{1-D}{1-2D}$
Voltage stress across the switch	V_{in}	$\frac{V_o}{4n+1}$	

2.6 Conclusion

This chapter presented a review on conventional half bridge converter. A conventional half bridge converter is not suitable due to the fact that it is associated with shoot through, limited voltage problems, ripples (unbalanced midpoint problems). A z-source half bridge converter is proposed to give a solution to these problems. And it shows that a z-source converter is more stable than the traditional half bridge.

CHAPTER 3
CONVERTER CIRCUIT ANALYSIS AND THE SIMULATION RESULTS

3.1 Introduction

This chapter discussed the circuit analysis and simulation for the Z-Source based half-bridge inverter (Zhang et al., 2014). Circuit description of converter and analysis in section 3.2, two cases are considered, case 1 and case 2 in which the converter is in shoot-through and otherwise respectively. To express the converter capability of producing different output voltage waveforms by controlling the switches duties, two conditions are exemplified, first to produce a symmetric output voltage and second to produce asymmetric output voltage. This is followed by a simulation conducted using PSCAD software.

3.2 System Development and Analysis

This section explains the circuit development, steady-state operational analysis, equivalent circuits and key waveforms of the inverter.

3.2.1 Circuit Development

The circuit arrangement of the inverter circuit is depicted in figure 3.1. As shown, traditional half-bridge inverter consisting two switches S_1 and S_2, a diode D and two capacitors C_{d1} and C_{d2} is combined with an impedance LC network comprising inductors L_1 and L_2, and capacitors C_1 and C_2. The additional Z-source circuit is to protect the inverter dc source from current flow back. The inductors used in the Z-source are to handle the converter shoot-through currents.

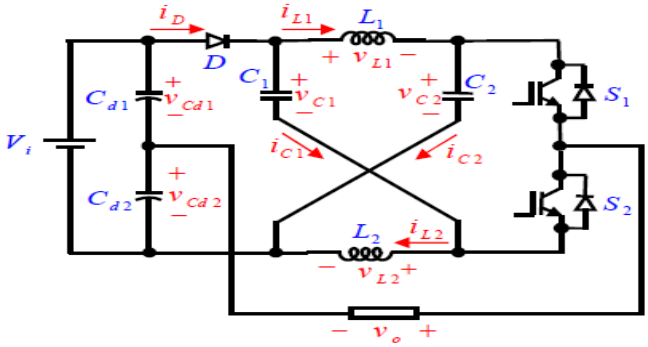


Figure 3.1: Z-source half-bridge inverter

3.2.2 Steady State Analysis

Following assumptions and notations are adapted in the analysis:

1)The inverter components operate in ideal mode; 2) In the LC network, capacitors $C_1 = C_2$ and inductors $L_1 = L_2$; 3) Switching pulses dead time and switches freewheeling diodes are neglected; 4) Large value of capacitance of the capacitors C_{d1}, C_{d2}, C_1 and C_2. 5) D_1 and D_2 represent the duty cycles of the switches S_1 and S_2 respectively. The inverter operates distinctively in two different cases based on the combination of switches duties: $D_1 + D_2 \leq 1$ and $D_1 + D_2 > 1$.

A. Case I: $\boldsymbol{D_1 + D_2 \leq 1}$.

Here, the circuit does not operate in the shoot-through since the switches S_1 and S_2 never turn on simultaneously. The process is exactly the same as in traditional half-bridge inverter. Depending on the switches states in this case we have three distinct operating modes in this case. Switches state $S_1 \rightarrow on$, $S_2 \rightarrow off$ correspond to mode 1, equivalent circuit for this mode is shown in Figure 3.2 (a). Therein, as indicated by arrows current flow from source-diode- Z-network-S_1, finally flows into source. During the second mode which correspond to $S_1 \rightarrow off$, $S_2 \rightarrow off$, the equivalent circuit is shown in Figure 3.2 (b). Therein, as indicated by arrows, current flow from the source, via the diode, through the Z-network, and finally flows back to source. Similarly, mode 3 occur when $S_1 \rightarrow off$, $S_2 \rightarrow on$. As shown in the equivalent circuit Figure 3.2 (c), negative voltage appears across the diode and therefore turn-off. The current flow from source, via R_L, through the switch S_2, then Z-network, finally flows into source again.

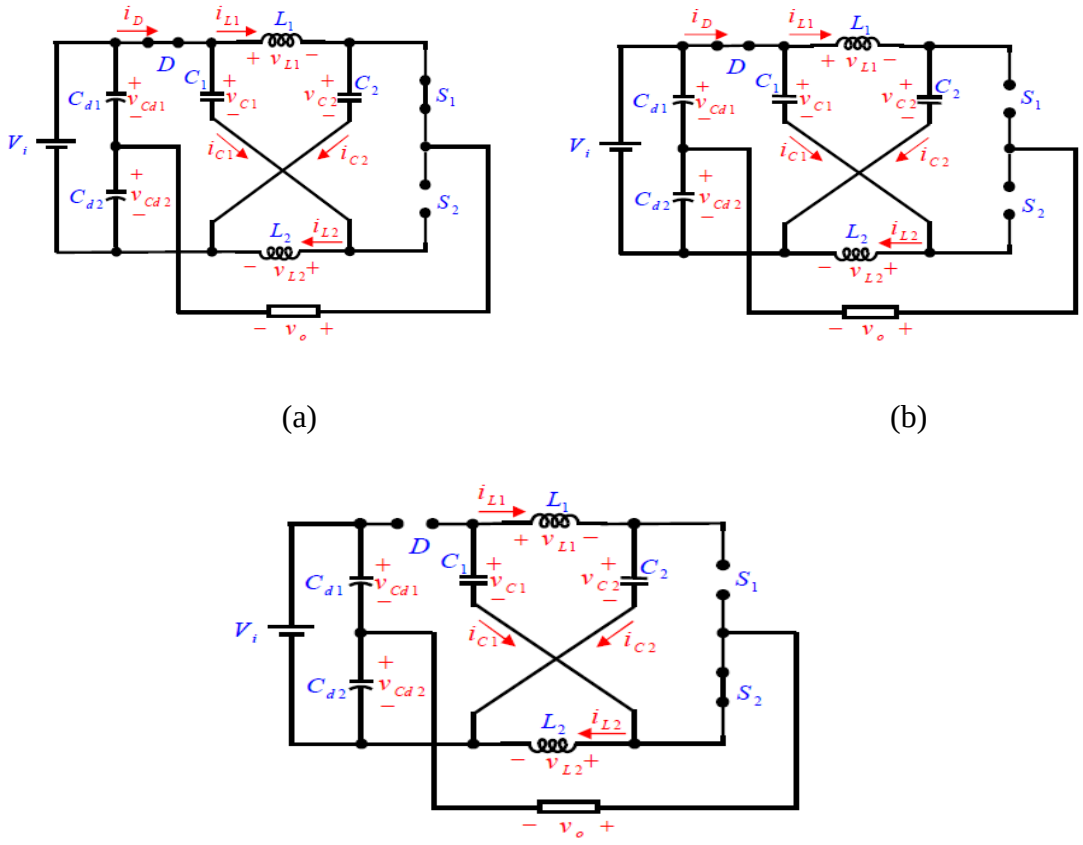
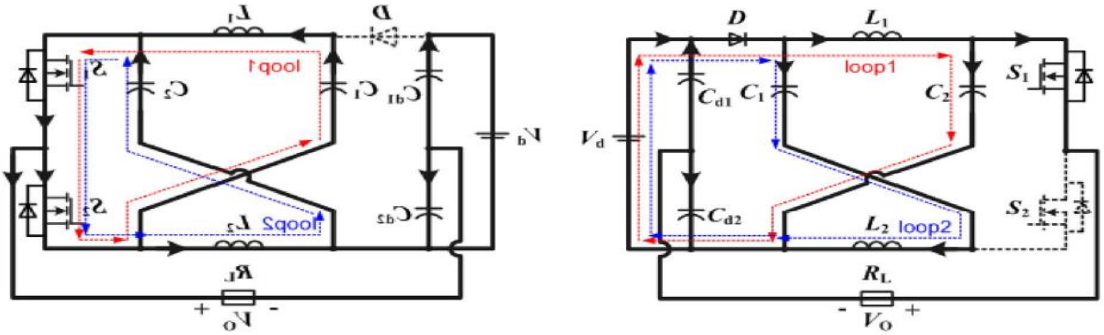


Figure 3.2: Case I: $D_1 + D_2 \leq 1$ equivalent circuits. (a) $S_1 \rightarrow on$, $S_2 \rightarrow off$. (b) $S_1 \rightarrow off, S_2 \rightarrow off$. (c) $S_1 \rightarrow off, S_2 \rightarrow on$.

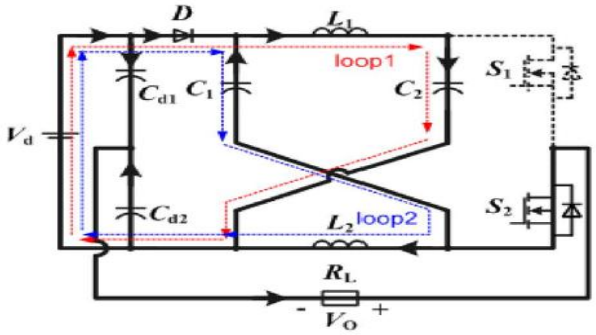
B. Case II: $D_1 + D_2 > 1$

There are three operational modes in this case, based on the states of the switches over the period T. Mode 1: $S_1 \rightarrow on$, $S_2 \rightarrow on$, mode 2: $S_1 \rightarrow on$, $S_2 \rightarrow off$, and mode 3: $S_1 \rightarrow off, S_2 \rightarrow on$. The equivalent circuits for these modes are shown in fig. 3.3 (a), 3.3(b) and 3.3(c) for mode1, mode 2 and mode 3, respectively.

For the steady state operation analysis let t_o to represent the starting of a period, t_1 mode transition from mode1 to mode 2 given as $t_1 = t_o + (D2 + D1 - 1)T$, t_2 transition interval from mode 2 to mode 3; $t_2 = t_1 + (1 - D2)T$ and $t_3 = T$ is the end of period. The goal here is to obtain the equation for the output-voltage from every mode.



(a) (b)



(c)

Figure 3.3: Case II: $D_1 + D_2 > 1$ equivalent circuits. (a) mode 1: $S_1 \rightarrow on$, $S_2 \rightarrow on$. (b) mode 2: $S_1 \rightarrow on$, $S_2 \rightarrow off$. (c) mode 3: $S_1 \rightarrow off$, $S_2 \rightarrow on$.

Mode 1: $t \in [t_0, t_1]$: This is shown in Figure 3.3(a), $S_1 \rightarrow on$, $S_2 \rightarrow on$, there are two loops; loop 1 and loop 2 marked with red and blue colours respectively. Within the loops, energy is discharged from the capacitors C_1 and C_2 to L_1 and L_2 inductors. Subsequently, the energy is stored in L_1 and L_2 and therefore inductor currents i_{l1} and i_{l2} increased. Accordingly, we have:

$$\begin{cases} v_{L_1} = v_{C_1} \\ v_{L_2} = v_{C_2} \end{cases} \tag{3.1}$$

Where $v_{L1}, v_{L2}, v_{C1}, v_{C2}, i_{l1}$, and i_{l2} are the voltages of L_1, L_2, C_1, and C_2 and currents of L_1, L_2 respectively.

Meanwhile diodes D carry negative voltage $-(v_{C1} + v_{C2} - V_d)$ it therefore turns off. The capacitor C_2 deliver energy C_{d2} and load R_L, therefore C_{d2} charges while C_{d1} discharges. Considering loop $C_2 \rightarrow R_L \rightarrow C_{d2}$, the inverter output voltage is obtained as

$$v_o = v_{C2} - v_{Cd2} \tag{3.2}$$

Mode 2: $t \in [t_1, t_2]$: This is shown in Figure 3.3(b), $S_1 \rightarrow on$, $S_2 \rightarrow off$. There are two loops; loop 1 and loop 2 marked with red and blue colours respectively. Within loop 1, energy is discharged from the source V_d and inductor L_1 to the capacitor C_2, and therefore v_{C2} increased. Within loop 2, energy is discharged from the source V_d and inductor L_2 to the capacitor C_1, and so that v_{C1} increased. Subsequently, capacitor C_2 deliver energy C_{d2} and load R_L, therefore C_{d2} charges while C_{d1} discharges. Considering loop 1 we have

$$v_{L1} = V_d - v_{C2} \tag{3.3}$$

Considering loop $C_2 \rightarrow R_L \rightarrow C_{d2}$, the inverter output voltage is equal to (3.2).

Mode 3: $t \in [t_2, t_3]$: This is shown in Figure 3.3(c), $S_1 \rightarrow off$, $S_2 \rightarrow on$. There are two loops; loop 1 and loop 2 marked with red and blue colours respectively. Within loop 1, energy is discharged from the source V_d and inductor L_1 to the capacitor C_2, and therefore v_{C2} increased. Within loop 2, energy is discharged from the source V_d and inductor L_2 to the capacitor C_1, and so that v_{C1} increased. Subsequently, energy stored in L_2 and C_{d2} is discharged to R_L, therefore C_{d1} charges while C_{d2} discharges. Considering loop 1 we have similar equation as in (3.3)

Considering loop $V_d \rightarrow D \rightarrow C_1 \rightarrow R_L \rightarrow C_{d2}$, the inverter output voltage v_o is obtained as

$$v_o = -(v_{Cd2} + v_{C1} - V_d) \tag{3.4}$$

Using volt-second property of L_1, we have

$$\int_0^T v_{L1} dt = 0 \tag{3.5}$$

Using (3.1) and (3.2) in (3.5)

$$\int_{t_0}^{t_1} v_{C1}\, dt + \int_{t1}^{t_2} (V_d - v_{C2})\, dt = 0 \tag{3.6}$$

$$(D_2 + D_1 - 1)Tv_{C1} + (2 - D_2 - D_1)T(V_d - v_{C2}) = 0 \quad (3.7)$$

Since the impedance network is symmetric i.e. $L_1 = L_2$ and $C_1 = C_2$ equation (3.7) can be written as

$$v_{C1} \approx v_{C2} = \frac{2-D_2-D_1}{3-2(D_1+D_2)} V_d \quad (3.8)$$

On the other hand, considering the ampere-sec characteristics of capacitor C_{d2}

$$\int_0^T i_{C_{d2}} dt = 0 \quad (3.9)$$

It is observed from the equivalent circuits Figure 3.3 that

$$V_d = v_{Cd1} + v_{Cd2}$$

Let the errors of the voltages v_{Cd1} and v_{Cd2} be represented as Δv_{Cd1} and Δv_{Cd2}, respectively. Since the source voltage V_d is constant, then

$$\Delta v_{Cd1} = -\Delta v_{Cd2}$$

And it follows that

$$i_{Cd1} = i_{Cd2}.$$

Furthermore, from the equivalent circuit its apparent that

$$i_o = i_{Cd1} + i_{Cd2}$$

Subsequently,

$$i_{Cd2} = {}^{i_o}/_2 \quad (3.10)$$

By using (3.6) in (3.5) we got

$$\int_0^T {}^{i_o}/_2 \, dt = 0 \quad (3.11)$$

Using (3.2) and (3.4) in (3.7)

$$\int_{t_0}^{t_1} \frac{(v_{C2}-v_{Cd2})}{2R_L}\, dt + \int_{t2}^{t_3} \frac{-(v_{Cd2}+v_{C1}-V_d)}{2R_L}\, dt = 0 \quad (3.12)$$

$$\frac{(v_{C2}-v_{Cd2})}{2R_L} D1T + \frac{-(v_{Cd2}+v_{C1}-V_d)}{2R_L}\,(1-D1)T = 0 \quad (3.13)$$

Which leads to

$$v_{Cd2} = (2v_{C2} - V_d)D1 - v_{C2} + V_d \quad (3.14)$$

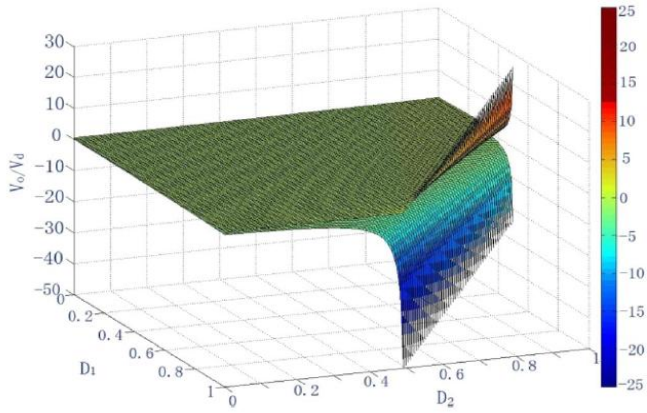
To find the inverter positive output-voltage by considering situation when S_1 is on using equations (3.8) and (3.14) in (3.2) we have

$$v_p = v_o = v_{C2} - v_{Cd2} = \frac{(1-D_1)}{3-2(D_1+D_2)} V_d \quad (3.15)$$

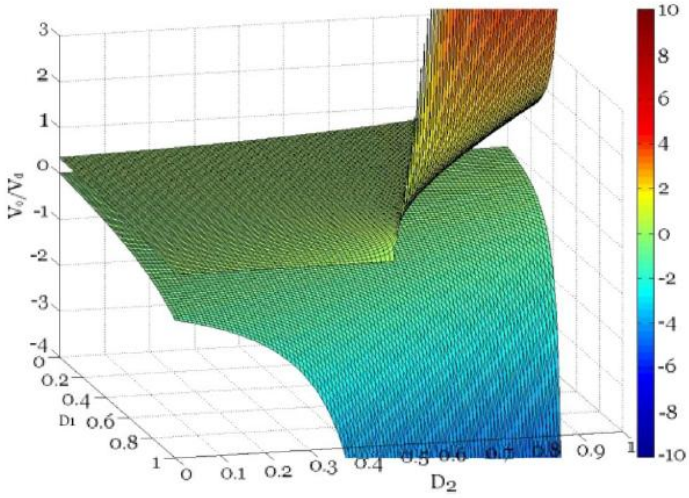
In the same way to find the inverter negative output-voltage we consider situation when S_2 is on using equations (3.8) and (3.14) in (3.4) we have

$$v_n = v_o = v_d - v_{C2} - v_{Cd2} = -\frac{D_1}{3-2(D_1+D_2)} V_d \quad (3.16)$$

Using equation (3.15) and (3.16), relationship between the switches duties D1, D2 and the inverter gain $^{v_o}/_{V_d}$ is plotted in figure 3.4 (a) and zoomed figure 3.4 (b). It can be observed from these figure that the voltage gain increases rapidly, this implies that by properly adjusting the duties D1 and D2 wide output-voltage is obtained from this inverter.



(a)



(b)

Figure 3.4: (a) Relationship figure of *D1*, D2 and $^{v_o}/_{V_d}$. (b) Zooming in of (a)

Different output-voltage such as asymmetric and symmetric, buck and boost, positive and negative peaks can be obtained by adjusting the duty of the switches D1 and D2. Moreover, the inverter work as a buck-boost, it would work as boost when the gain $^{v_o}/_{V_d} \geq 1$, and act as a buck when $^{v_o}/_{V_d} < 1$.

Figure 3.5 shows the inverter waveform under case 2 with $D1 = 0.5$ and $D2 = 0.7$. Therein, G_{S1} and G_{S2} are the switching voltages for S_1 and S_2, respectively. i_{l1} and i_{l2} are the currents of inductors L_1 and L_2, respectively; i_d diode D current; v_{C1}, v_{C2}, v_{Cd1}, and v_{Cd2} represent the voltages of capacitors C_1, C_2, C_{d1} and C_{d2} respectively; and finally the output-voltage is v_o. For the conventional inverter the output voltage limit when $D1 = 0.5$

and $D2 = 0.7$ is indicated as $0.5V_i$ and $-0.5V_i$ and it can be seen that the voltage of the Z-network converter can go beyond the limit.

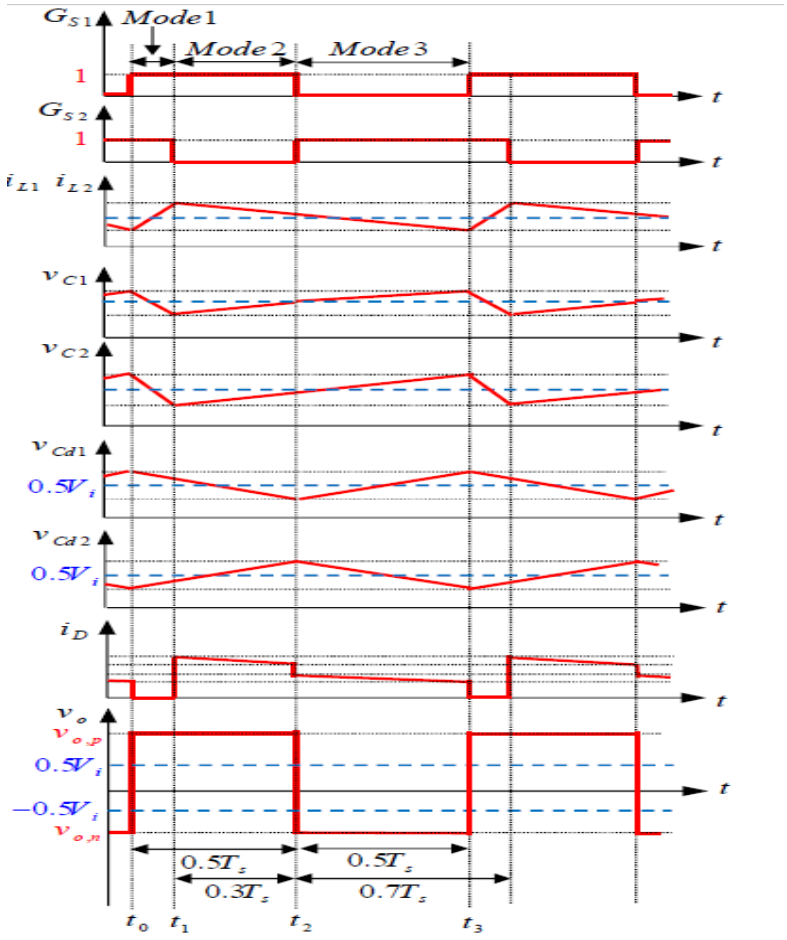


Figure 3.5: Waveforms of the Z-network half-bridge inverter when $D1$ = 0.5 and $D2$ = 0.7.

Figure 3.6 shows the converter waveform under case 2 with $D1 = 0.7$ and $D2 = 0.5$. from the output waveform it can be clearly observed that the output voltage is asymmetric unlike in Figure 3.5 this prove the assertion that different output voltage waveforms can be achieved, which is the requirement of applications such as electrochemical supply.

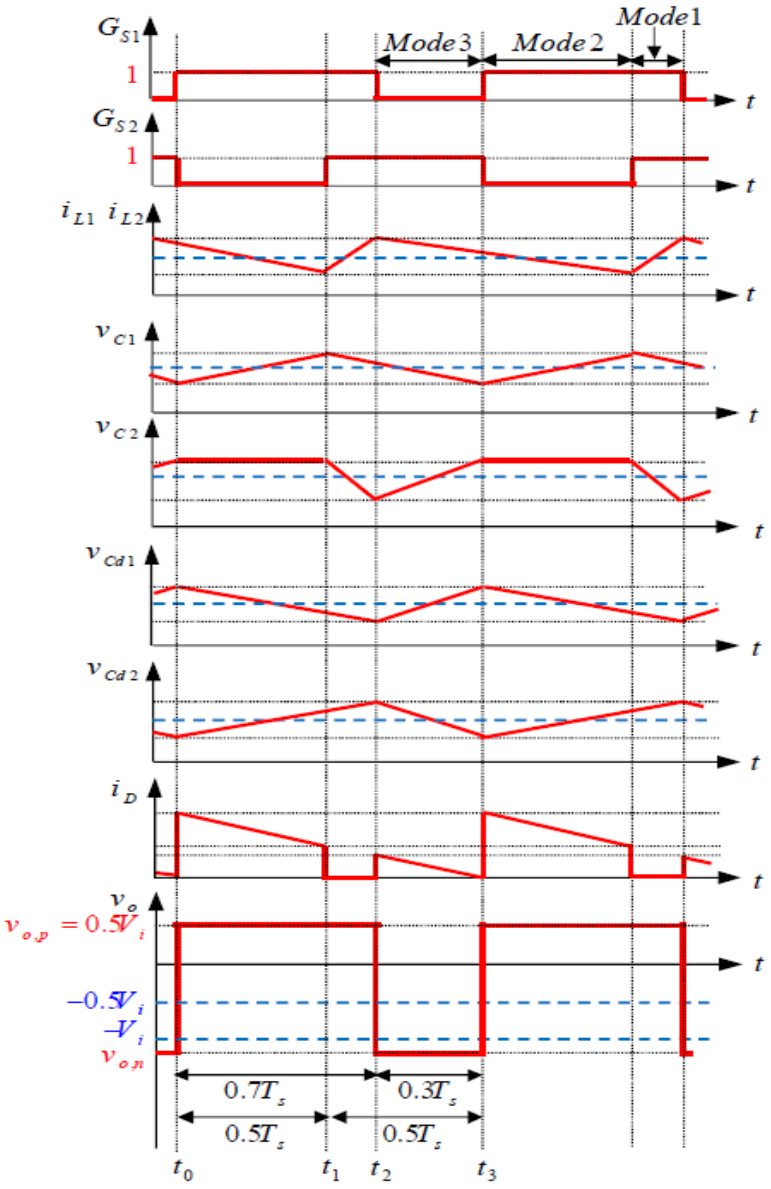


Figure 3.6: Waveforms of the Z-network half-bridge inverter when $D1 = 0.7$ and $D2 = 0.5$.

The converter efficiency can be express as

$$\eta = \frac{P_{out}}{P_{in}} \tag{3.17}$$

where the output power

$$P_{out} = \frac{D_1 v_p{}^2 + (1-D_1) v_n{}^2}{R} \tag{3.18}$$

And the input power

$$P_{in} = V_d I_{av} \tag{3.19}$$

I_{av} is the average input current.

Using (3.18) and (3.19) in (3.17), we have

$$\eta = \frac{\frac{D_1 {v_p}^2 + (1 - D_1){v_n}^2}{R}}{V_d I_{av}}$$

$$= \frac{D_1 {v_p}^2 + (1 - D_1){v_n}^2}{R V_d I_{av}}$$

Substituting for v_p and v_n

$$= \frac{D_1(1-D_1)V_d}{(3-2(D_1+D_2))^2 R I_{av}} \tag{3.20}$$

3.3 Midpoint Voltage

Considering the equivalent circuits shown in Figure. 3.7 (a) and (b); these circuits are obtained by regarding the inverter input part as a dc voltage source or a dc current source and the output side of the Z-network as a dc current source, the current of the constant source is given by;

$$I_p = C_{d2} \frac{dv_{C_{d2}}}{dt} \tag{3.21}$$

From (3.21)

$$v_{C_{d2}}(t) = V_{C_{d2}0} + \int \frac{I_p}{C_{d2}} dt. \tag{3.22}$$

Let the maximal fluctuation of $v_{C_{d2}}$ in this inverter be represented as ΔV_Z, using (3.22), one has

$$\Delta V_Z = \int_0^{D_1 T} \frac{I_p}{C_{d2}} dt = D_1 T \frac{I_p}{C_{d2}} \tag{3.23}$$

Using KVL in the circuits we obtained

$$I_p R = V_d - V_{C_{d2}0} - V_{I_p}$$

$$I_p = \frac{V_d - V_{C_{d2}0} - V_{I_p}}{R} \tag{3.24}$$

And therefore (3.23) become

$$\Delta V_Z = D_1 T \frac{V_d - V_{C_{d2}0} - V_{I_p}}{C_{d2} R} \tag{3.25}$$

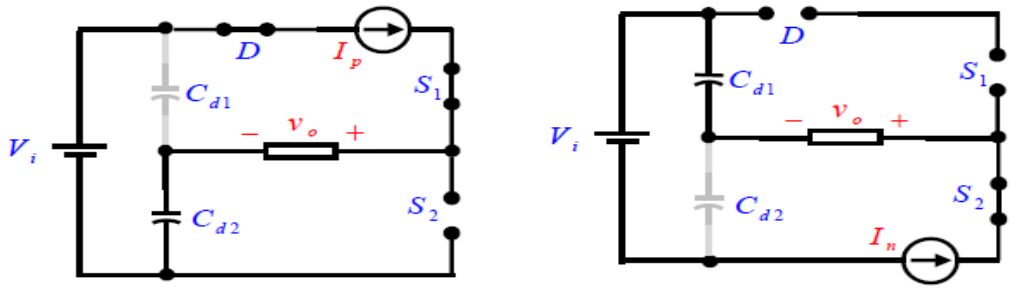
Taking the ratio of the maximal fluctuation of $v_{C_{d2}}$ in this inverter ΔV_Z to the one in conventional inverter ΔV as given in

$$\Delta V = \frac{D_1 T}{C_{d2} R}(V_d - V_{C_{d2}0}) \tag{3.26}$$

We have,

$$\frac{\Delta V_Z}{\Delta V} = \frac{V_d - V_{C_{d2}0} - V_{I_p}}{(V_d - V_{C_{d2}0})} x100\% \tag{3.27}$$

From (3.27) it can be seen that the stability can be enhance by proper design of V_{I_p} which can be done proper selection of the Z-network parameters. As shown in the equation the ratio $\Delta V_Z / \Delta V$ become smaller if V_{I_p} is positive and approaches zero as V_{I_p} approaches the value of $(V_d - V_{C_{d2}0})$.



(a)mode 1: $S_1 \rightarrow on, S_2 \rightarrow of$ (b)mode 1: $S_1 \rightarrow off, S_2 \rightarrow on$

Figure 3.7: Equivalent circuit of Z-source inverter

3.4 Components Design and Simulation Results

This section presents the simulation result for the inverter, carried out using PSCAD software. The first stage is components design, to obtain the optimal values of the impedance network capacitors and inductors.

The capacitance of the capacitor C_2 is given by the equation

$$C_2 = \frac{I_{C2} dt_{C2}}{dv_{C2}} \tag{3.28}$$

Where $dt_{C2} \approx (D_1 + D_2 - 1)T$, is the time when the switch is on, and dv_C is capacitor voltage ripple which can be express in terms of the allowable fluctuation factor $x_C\%$ and the maximum capacitance range $v_{C2,max}$.

$$V_{C2} = \frac{2-D_1-D_2}{D_1} V_o \quad when\ (S_1, S_2) = (on, off) \tag{3.29}$$

$$V_{C2} = \frac{2-D_1-D_2}{1-D_1} V_o \quad when\ (S_1, S_2) = (off, on) \tag{3.30}$$

Applying KCL in the equivalent circuits shown in figure 3.3 we get

$$i_{L2} = i_{C1} + i_o \quad when\ (S_1, S_2) = (on, on)$$

$$i_{L1} = i_{C2} + i_o \quad when\ (S_1, S_2) = (on, off)$$

$$i_{L2} = i_o - i_{C1} \quad when\ (S_1, S_2) = (off, on) \tag{3.31}$$

And subsequently, from (3.31) we get

$$i_{C2,rms} \approx i_{L2,rms} = \frac{I_o}{2} \tag{3.32}$$

The range of v_{C2} voltage is determined by using the equations (3.29) and (3.30), the maximum voltage for safe operation the voltage should be between $1.5v_{C2,max}$ and $2v_{C2,max}$. The voltage ripple dv_C can therefore be given as

$$dv_C = x_C\% v_{C2,max} \tag{3.33}$$

By using equations (3.32) and (3.33) along with expression for dt_{C2} in to (3.28)

$$C_2 = \frac{I_o(D_1+D_2-1)T}{2x_C\%V_{C2,max}} \tag{3.34}$$

using the same procedure the capacitance of the capacitor C_1 is given as

$$C_1 = C_2 = \frac{I_o(D_1+D_2-1)T}{2x_C\%V_{C2,max}} \tag{3.35}$$

Similarly, for the inductor design, the inductance of the inductor L_2 is given by the equation

$$L_2 = \frac{V_{L_2}dt_{L2}}{di_{L_2}} \tag{3.36}$$

Where $dt_{L2} \approx (D_1 + D_2 - 1)T$, is the time when the switch is on, and the inductor ripple current di_{L2} can be express in terms of the allowable inductance fluctuation factor $x_L\%$ and inductor current I_{L2} as

$$di_L = x_L\%I_{L2} \tag{3.37}$$

Substituting for I_{L2} from equation (3.32), dt_{L2} and V_{L_2} following expression is obtained

$$L_2 = \frac{2V_{C2,max}(D_1+D_2-1)T}{x_L\%I_o} \tag{3.38}$$

Meanwhile

$$L_1 = L_2 = \frac{2V_{C2M}(D_1+D_2-1)T}{x_L\%I_o} \tag{3.39}$$

Where x_c is capacitor allowed fluctuation range, x_L is inductor allowed fluctuation range of the inductor, T is the switching period, I_o is the desired output current rms value, and V_{C2M} the maximal rated voltage of C_2.

For the purpose of our simulation the preassigned values for the allowed capacitor and inductor fluctuation range x_c and x_L are selected to be 1% and 10% respectively, $V_{in} = 48\,V$, $V_o = 100\,V$, $I_o = 10\,A$.

The selected parameters for the simulation are summarized in table 3.1.

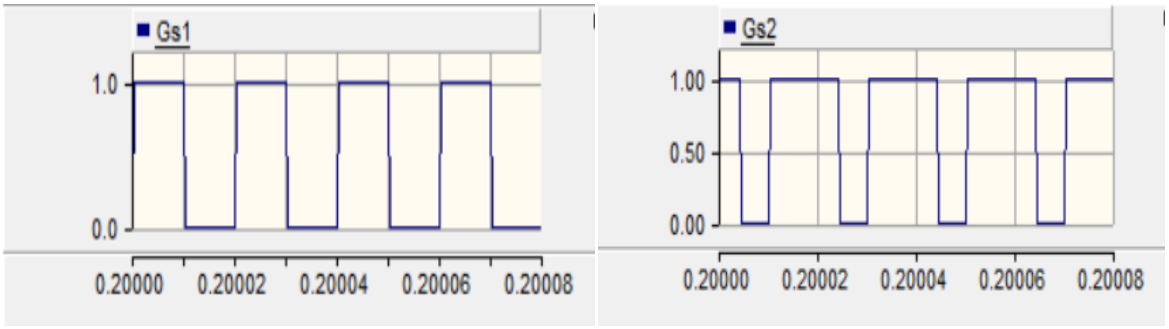
Table 3.1: Selected Parameters for Simulation

V_{in}	$48V$
$L_1 = L_2$	$100\ \mu H$
$C_1 = C_2 = Cd_1 = C_{d2}$	$470\ \mu F$
R_L	$470\ \Omega$
f_s	$50\ kHz$

3.4.1 Symmetric output voltage Simulation Result

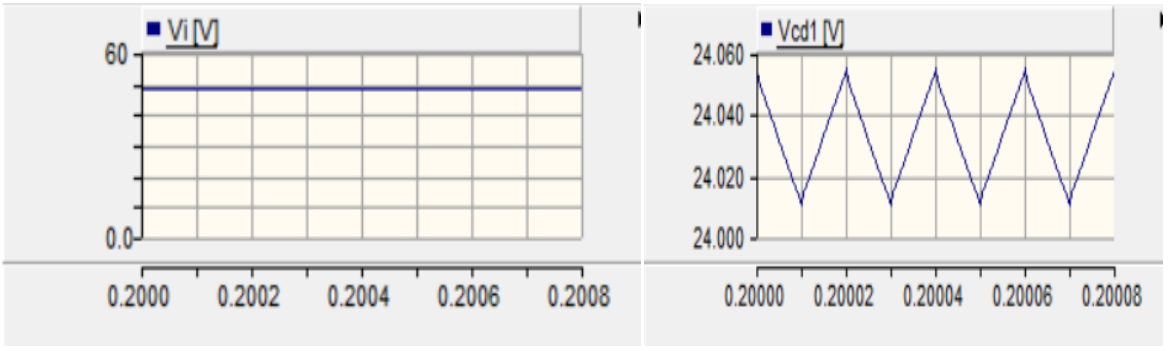
Fig. 3.8 shows the simulation result for the inverter symmetrical output voltage. Figure 3.8 (a) shows the trigger pulse with for switch S_1 with a duty ratio $D_1 = 0.5$, and Figure 3.8 (b) shows the switching pulses for switch S_2 with a duty ratio $D_1 = 0.7$, the duties are selected to be equal to those in Figure 3.5 that produces a symmetrical output. The input voltage is selected to be equal to $48V$ as shown in Figure 3.9 (a). The waveform for the two input capacitor voltages v_{cd1} and v_{cd2} are shown in Figure 3.9 (b) and 3.10 (a) respectively, according to these figures, the total voltages of the two capacitors is equal to the value of source voltage. Figure 3.10 (b) shows the current flowing through the diode D, according to this figure, when the switches S_1 and S_2 are simultaneously on, the diode current is zero and the diode is off, otherwise, the diode current is positive and the diode is on. Figure 3.11 (a) and 3.11 (b) show the current flows through the inductors L_1 and L_2, i_{L1} and i_{L2} respectively. It can be seen that the average values of i_{L1} and i_{L2} are equal. The shape of the voltages of the two capacitors C_1 and C_2 is shown in Figure 3.12 (a) and 3.12 (b) respectively, from these figures the average voltage of the two capacitors peak is

63.9 $volts,$ which is approximately equal to the calculated value of 64 $volts$, calculated using equation (3.8). Finally, fig. 3.12 (c) shows the output voltage which is consistent with the theoretical waveform of Figure 3.5. Furthermore, from the figure the positive and negative output voltages are 40 and -40 volts which is approximately equal to 39.9 and $-$ 39.8 volts, calculated using equations (3.15) and (3.16).



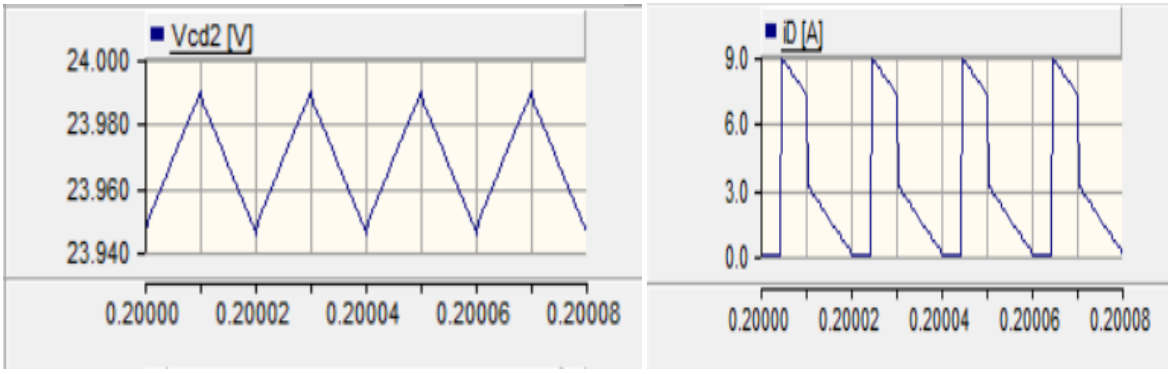
(a) (b)

Figure3.8: Simulation Result in case of symmetric output; (a) $GS1$ Switch 1 triggering pulses (b) $GS2$ Switch 2 triggering pulses



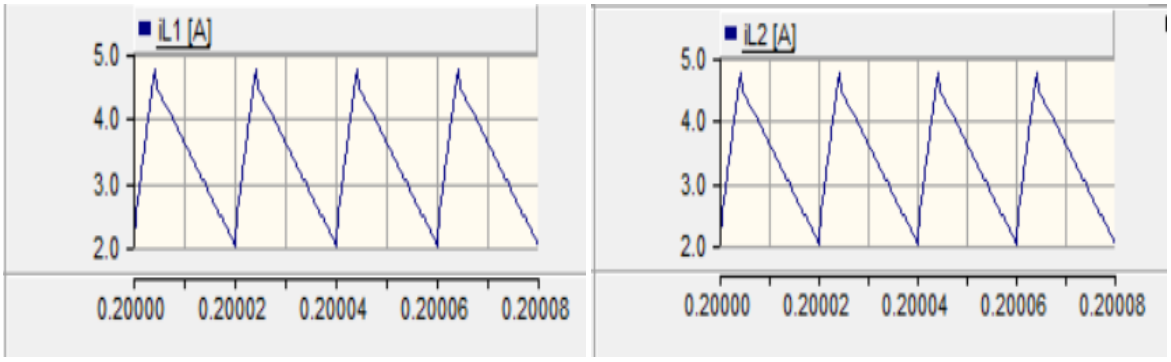
(a) (b)

Figure 3.9: Simulation Result in case of symmetric output; (a) source voltage V_{in} (b) input capacitor C_1 voltage v_{cd1}



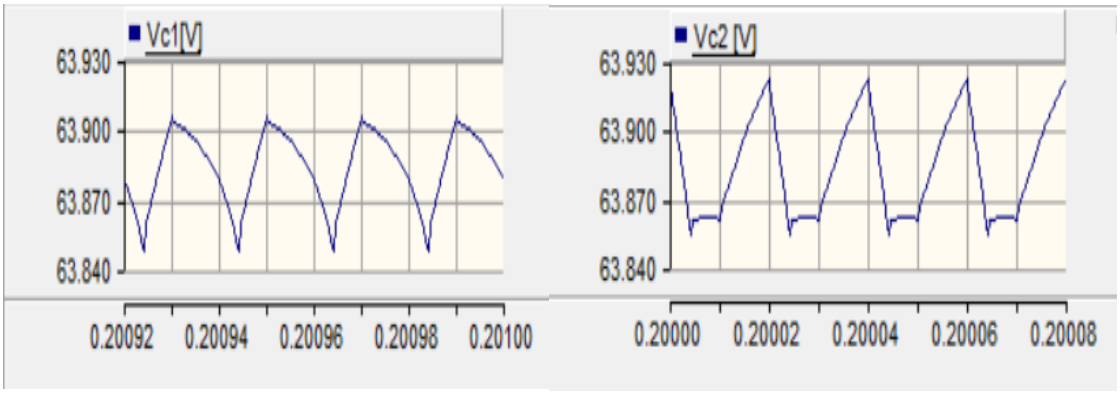
(a) (b)

Figure 3.10: Simulation Result in case of symmetric output; (a)Input capacitor C_2 voltage v_{cd2} (b) diode current i_D

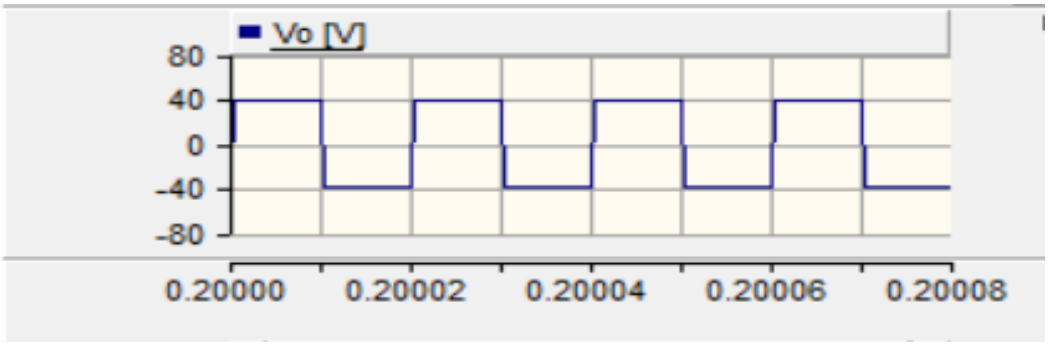


(a) (b)

Figure 3.11: Simulation Result in case of symmetric output; (a) L_1 inductor current i_{L1} (b) L_2 inductor current i_{L2}



(a) (b)



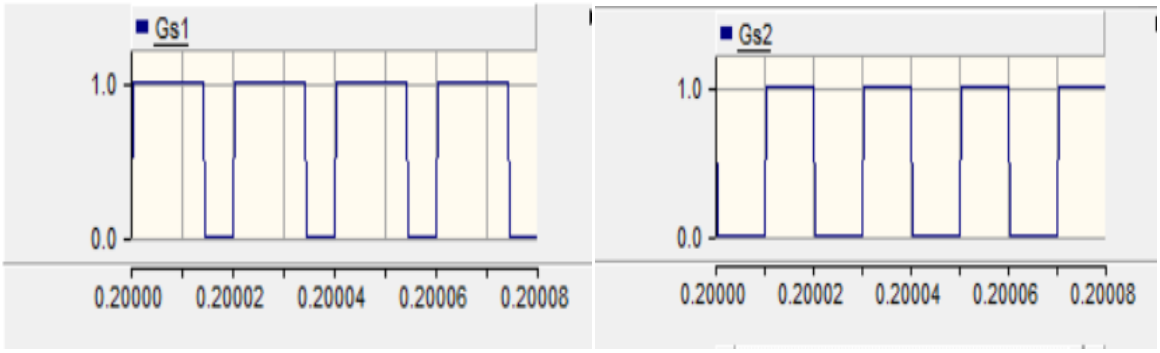
(c)

Figure 3.12: Simulation Result in case of symmetric output; (a) C_1 Capacitor voltage v_{c1} (b) C_2 Capacitor voltage v_{c2} (c) Output Voltage V_o.

3.4.2 Asymmetric output voltage Simulation Result

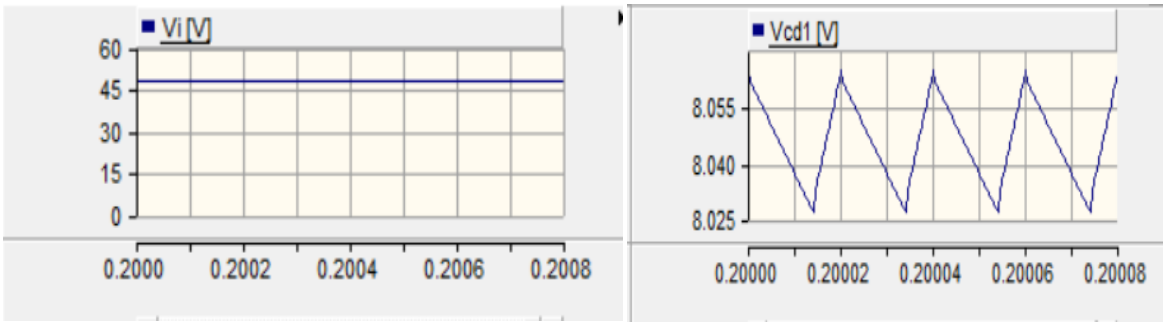
Figure 3.13 shows the simulation result for the inverter asymmetric output voltage. Figure 3.13 (a) shows the trigger pulse with for switch S_1 with a duty ratio $D_1 = 0.7$, and Figure 3.13 (b) shows the switching pulses for switch S_2 with a duty ratio $D_1 = 0.5$, the duties are selected to be equal to those in fig. 3.6 that produces asymmetrical output. The input voltage is selected to be equal to $48V$ as shown in Figure 3.14 (a). The waveform for the two input capacitor voltages v_{cd1} and v_{cd2} are shown in Figure 3.14 (b) and 3.15 (a) respectively, similarly the algebraic sum of voltages from the two capacitors is equal to the value of the source voltage. Figure 3.15 (b) shows the current flowing through the diode D, also according to this figure, when the switches S_1 and S_2 are simultaneously on, the diode current is zero and the diode is off, otherwise, the diode current is positive and the diode is on. Figure 3.16 (a) and 3.16 (b) show the current flows through the inductors L_1 and L_2, i_{L1}

and i_{L2} respectively. It can also be observed that the average values of i_{L1} and i_{L2} are equal. The shape of the voltages of the two capacitors C_1 and C_2 is shown in Figure 3.17 (a) and 3.17 (b) respectively, from these figures the average voltage of the two capacitors peak is $63.9\,volts,$ which is approximately equal to the calculated value of $64\,volts,$ calculated using equation (3.8). Finally, Figure 3.17 (c) shows the output voltage which is consistent with the theoretical waveform of Figure 3.6. Furthermore, from the figure the positive and negative output voltages are 23.9 and -55.8 volts which is approximately equal to $24\ and\ -56$ volts, calculated using equations (3.15) and (3.16).



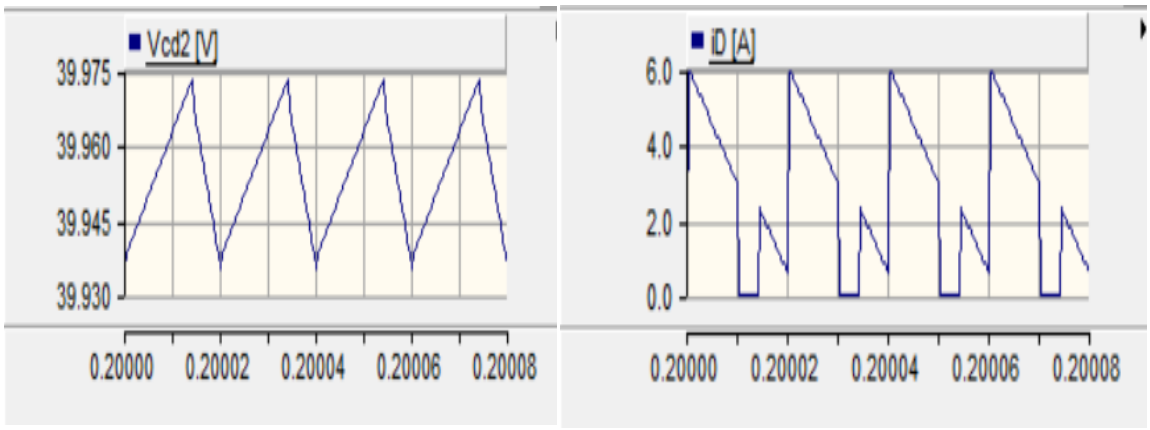
(a) (b)

Figure 3.13: Simulation Result in case of asymmetric output; (a) $GS1$ Switch 1 triggering pulses (b) $GS2$ Switch 2 triggering pulses



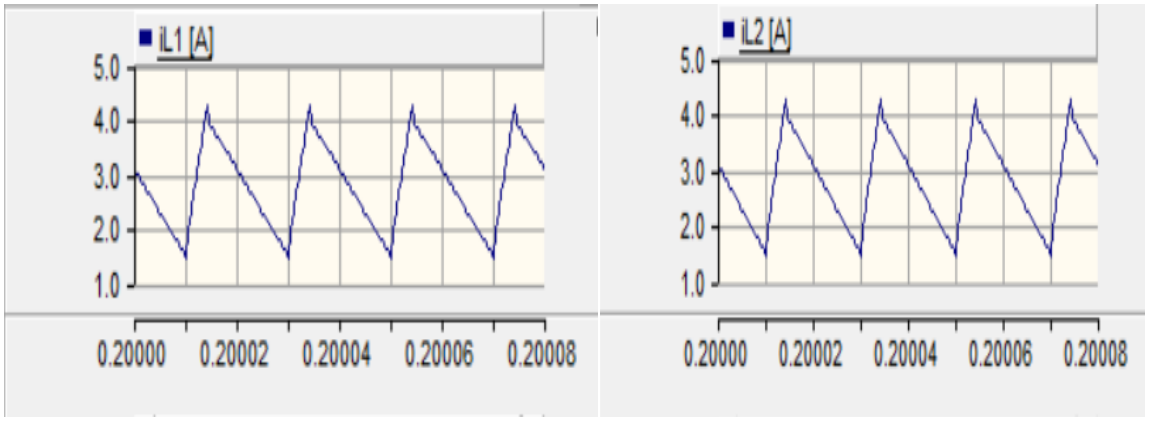
(a) (b)

Figure 3.14: Simulation Result in case of asymmetric output; (a) source voltage V_{in} (b) input capacitor C_1 voltage v_{cd1}



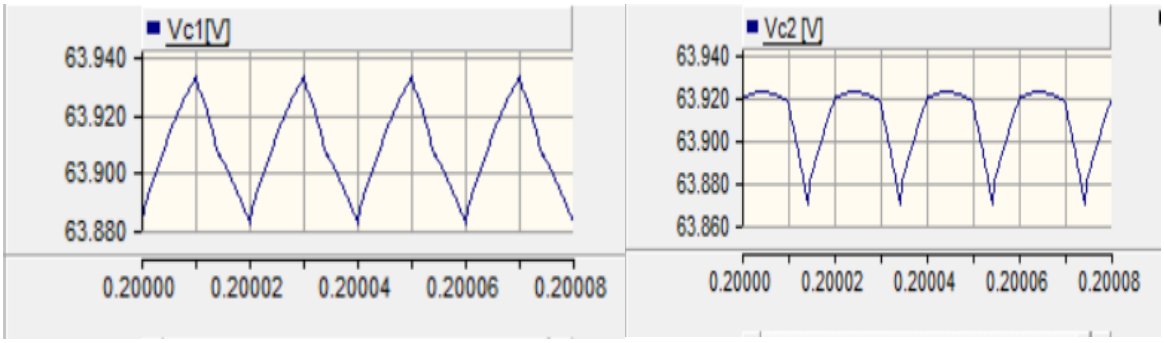
(a) (b)

Figure 3.15: Simulation Result in case of asymmetric output; (a)Input capacitor C_2 voltage v_{cd2} (b) diode current i_D

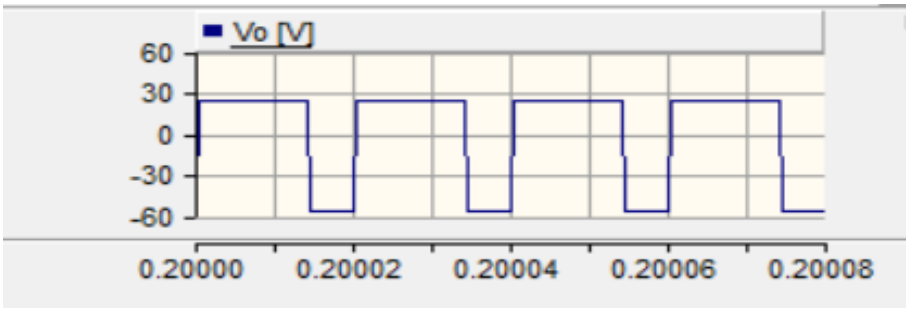


(a) (b)

Figure 3.16: Simulation Result in case of asymmetric output; (a) L_1 inductor current i_{L1} (b) L_2 inductor current i_{L2}



(a) (b)



(c)

Figure 3.17: Simulation Result in case of asymmetric output; (a) C_1 Capacitor voltage v_{c1} (b) C_2 Capacitor voltage v_{c2} (c) Output Voltage V_o.

3.5 Conclusion

This chapter has presented the development and analysis of the Z-source based half-bridge inverter. Two operational cases were considered corresponding to non-shoot through and shoot through modes, in either case the inverter performance was established. Theoretical result has shown that the converter is capable of handling the shoot-through situation and the output voltage limitation problem is also solved. To validate the theoretical result a simulation is conducted using PSCAD which satisfies all the theoretical claims.

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1. Conclusion

In this thesis, analysis and simulation of a Z-source based half-bridge inverter has been presented. The equations of currents and voltages of all the components are obtained, to find the minimum values of passive components (capacitor and inductor). This inverter circuit is built upon the conventional half-bridge inverter circuit by adding an impedance LC network known as Z-network between the source and the converter. With this arrangement a robust inverter capable of handling conventional converter limitations is realized.

The steady state analysis of the novel Z-source half-bridge inverter has been discussed, depending on the combination of duty ratios of the two switches two operational cases are considered, case one corresponds to the inverter operation in a non-shoot-through mode and case two where shoot-through mode may occur. In both cases the relation between the responses of the various components are established by using appropriate equivalent circuits. The capacitor voltages and output voltage were derived using volt-second characteristics of the input inductor. Subsequently, the voltage gain and efficiency of the inverter are obtained, the gain is plotted against the duty ratios of the two switches, which indicated that the inverter produces a high efficiency and high gain. To show the capability of the inverter in producing range of different output voltage waveforms by controlling the switches duties, two examples are shown, one to produce a symmetric output voltage and the other to produce asymmetric output voltage.

To support the theoretical results, a simulation is carried out using PSCAD software. To show how the inverter can be used to produce different output voltages and overcome the ac output voltage limitation. In all the scenarios and for all the components the simulation results approximately fulfill the theoretical result. Both theoretical and simulation results have shown a clear indication that the inverter is capable of handling the shoot-through situation and alleviate the output voltage limitation problem is also solved.

Because of the many advantages offered by half-bridge inverters has made them to be widely used in many applications, despite the advantages which include simple structure, ease of control, versatility, small component count, and it's potent for producing high efficiency, they have three major problems; current shoot-through which may damage the whole converter, limitation in the output ac voltage level which hinders its usage in many applications where high output voltage is a must and finally the unbalance midpoint input voltage which leads to instability in the inverter.

One of the most successful solutions to these problems was obtained by integrating Peng's Z-network with the traditional inverter forming a Z-networked based half-bridge inverter. However, two LC impedance network were used to couple each of the two input capacitors with one Z-source network. This topology has made it possible to resolve the issues of limited output-voltage and current shoot-through. Nevertheless, additional circuit components are introduced by using two LC networks, that means increasing the weight, size and cost.

Despite the above advantages of this inverter it cannot satisfy some applications. Particularly, the electromechanical power supplies used in special applications such as electroplating technologies have peculiar requirements, such requirements include a varied output voltage with varied ratio between the positive and negative voltages. With increased demand on electroplating product along with numerous different specifications there are needs for electromechanical supplies that can provide different output waveforms such as square waves, triangular waves, step waves, saw-tooth waves, symmetrical and asymmetrical positive and negative voltages.

Meanwhile, the improved version of Z-source Half-bridge inverter discussed in this thesis will satisfy the special needs of the electromechanical power supplies used in electroplating technologies and many more applications. Furthermore, since only one LC network is used, this inverter topology provides an improved efficiency compared to the two-LC network Z-source half-bridge inverter. When compared to other Z-source inverters it provided much broader output voltage range with reduction in component count, size, weight and cost.

4.2. Future Work

The efficiency can be improved by using soft-switching techniques to reduce switching stress and losses. To further evaluate the performance of the inverter an experiment should be conducted to actualized the theoretical and simulation result.

REFERENCES

Axelrod, B., Berkovich, Y. & Ioinovici, A. (2003). Transformerless DC-DC converters with a very high DC line-to-load voltage ratio. *In Proceedings of the 2003 International Symposium on Circuits and Systems. 3 ISCAS'03*. (pp. III-III). IEEE.

Babaei, E. & Asl, E. S. (2017). High-voltage gain half-bridge Z-source inverter with low-voltage stress on capacitors. *IEEE Transactions on Industrial Electronics, 64*(1), 191-197.

Bernardon, D. P., Mello, A. P. C., Pfitscher, L. L., Canha, L. N., Abaide, A. R. & Ferreira, A. A. B. (2014). Real-time reconfiguration of distribution network with distributed generation. *Electric Power Systems Research, 107*, 59-67.

Bradaschia, F., Cavalcanti, M. C., Ferraz, P. E., Neves, F. A., dos Santos, E. C. & da Silva, J. H. (2011). Modulation for three-phase transformerless Z-source inverter to reduce leakage currents in photovoltaic systems. *IEEE Transactions on Industrial Electronics, 58*(12), 5385-5395.

Dehghan, S. M., Mohamadian, M., Yazdian, A. & Ashrafzadeh, F. (2010). A dual-input–dual-output Z-source inverter. *IEEE Transactions on power electronics, 25(*2), 360-368.

Eloy-Garcia, J., Arnaltes, S. & Rodriguez-Amenedo, J. L. (2007). Extended direct power control for multilevel inverters including DC link middle point voltage control. *IET Electric Power Applications, 1*(4), 571-580.

Eloy-Garcia, J., Arnaltes, S. & RodriguezAmenedo, J. L. (2008). Extended direct power control of a three-level neutral point clamped voltage source inverter with unbalanced voltages. *In 2008 IEEE Power Electronics Specialists Conference IEEE.* (pp. 3396-3400).

Emadi, A. (2014). Advanced electric drive vehicles. CRC Press.

Ge, B., Lei, Q., Qian, W. & Peng, F. Z. (2012). A family of Z-source matrix converters. *IEEE Transactions on Industrial Electronics*, *59*(1), 35-46.

Hsieh, Y. P., Chen, J. F., Liang, T. J. & Yang, L. S. (2012). Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques. *IEEE Transactions on Industrial Electronics*, *59*(2), 998-1007.

Hu, X., Ling, Z. Y., He, X. H. & Chen, S. S. (2009). Controlling transmission spectra of photonic crystals under electrochemical oxidization of aluminum. *Journal of The Electrochemical Society*, *156*(5), C176-C179.

Huang, Y., Shen, M., Peng, F. Z. & Wang, J. (2006). $ Z $-Source Inverter for Residential Photovoltaic Systems. *IEEE Transactions on Power Electronics, 21(*6), 1776-1782.

Hung, Y. C., Shyu, F. S., Lin, C. J. & Lai, Y. S. (2003, November). New voltage balance technique for capacitors of symmetrical half-bridge converter with current mode control. *In The Fifth International Conference on Power Electronics and Drive Systems,* PEDS 2003. (Vol. 1, pp. 365-369). IEEE.

Kamli, M., Yamamoto, S. & Abe, M. (1996). A 50-150 kHz half-bridge inverter for induction heating applications. *IEEE Transactions on Industrial Electronics, 43*(1), 163-172.

Kayatri, S., Vengatesh, R. P. & Rajan, S. E. (2016). Investigation of 3-Z-network boost converter for photovoltaic power generation system using MPPT control strategies. *In 2016 International Conference on Circuit, Power and Computing Technologies* (ICCPCT) (pp. 1-8). IEEE.

Kumar, M., Ansari, F. & Jha, A. K. (2011). Maximum power point tracking using perturbation and observation as well as incremental conductance algorithm. *International Journal of Research in Engineering and Applied Sciences*, *1*(4), 19-31.

Kumar, P. & Veerachary, M. (2017). Analysis of modified impedance-network half-bridge converter. In 2017 6th International Conference on Computer Applications In Electrical Engineering-Recent Advances (CERA) (pp. 415-420). IEEE.

Lai, R., Wang, F., Burgos, R., Boroyevich, D., Zhang, D. & Ning, P. (2010). A shoot-through protection scheme for converters built with SiC JFETs. *IEEE Transactions on Industry Applications, 46*(6), 2495-2500.

Li, W. & He, X. (2011). Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications. *IEEE Transactions on Industrial Electronics*, *58*(4), 1239-1250.

Li, Y., Jiang, S., Cintron-Rivera, J. G. & Peng, F. Z. (2013). Modeling and control of quasi-Z-source inverter for distributed generation applications. *IEEE Transactions on Industrial Electronics, 60*(4), 1532-1541.

Liu, Z., Liu, B., Duan, S. & Kang, Y. (2012). A novel DC capacitor voltage balance control method for cascade multilevel STATCOM. *IEEE Transactions on Power Electronics, 27*(1), 14-27.

Loh, P. C., Gao, F., Blaabjerg, F., Feng, S. Y. C. & Soon, K. N. J. (2007). Pulsewidth-Modulated $ Z $-Source Neutral-Point-Clamped Inverter. *IEEE Transactions on Industry Applications*, *43*(5), 1295-1308.

Luo, F. L. & Ye, H. (2004). Positive output multiple-lift push-pull switched-capacitor Luo-converters. *IEEE transactions on industrial electronics, 51*(3), 594-602.

Musavi, F., Edington, M., Eberle, W. & Dunford, W. G. (2012). Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies. *IEEE Transactions on Smart Grid, 3(*1), 413-421.

N. S. González-Santini, H. Zeng, Y. Yu, F. Z. Peng, (2016). "Z-source resonant converter with power factor correction for wireless power transfer applications", *IEEE Trans. Power Electron. 31* (11), pp. 7691-7700, Nov.

Norris, D. J., Arlinghaus, E. G., Meng, L., Heiny, R. & Scriven, L. E. (2004). Opaline photonic crystals: how does self- assembly work?. *Advanced Materials, 16*(16), 1393-1399.

Parikh, J. & Parikh, K. (2012). Growing pains: Meeting India's energy needs in the face of limited fossil fuels. *IEEE Power and Energy Magazine, 10*(3), 59-66.

Peng, F. Z., Joseph, A., Wang, J., Shen, M., Chen, L., Pan, Z. & Huang, Y. (2005). Z-source inverter for motor drives. *IEEE transactions on power electronics, 20*(4), 857-863.

Peng, F. Z., Shen, M. & Holland, K. (2007). Application of Z-source inverter for traction drive of fuel cell—Battery hybrid electric vehicles. *IEEE Transactions on Power Electronics, 22*(3), 1054-1061.

Peng, F. Z., Yuan, X., Fang, X. & Qian, Z. (2003). Z-source inverter for adjustable speed drives. *IEEE power electronics letters, 1*(2), 33-35.

PRASAD, J. S. (2012). Half bridge ZVS DC-DC converter with DCS PWM active clamp technique. *International Journal of Power Electronics and Drive Systems (IJPEDS), 2*(4).

Prudente, M., Pfitscher, L. L., Emmendoerfer, G., Romaneli, E. F. & Gules, R. (2008). Voltage multiplier cells applied to non-isolated DC–DC converters. *IEEE Transactions on Power Electronics, 23*(2), 871-887.

Rosas-Caro, J. C., Peng, F. Z., Cha, H. & Rogers, C. (2009). Z-source-converter-based energy-recycling zero-voltage electronic loads. *IEEE Transactions on Industrial Electronics, 56*(12), 4894-4902.

Shen, M., Joseph, A., Wang, J., Peng, F. Z. & Adams, D. J. (2004, October). Comparison of traditional inverters and Z-source inverter for fuel cell vehicles. *In Power Electronics in Transportation (IEEE Cat. No. 04TH8756)* (pp. 125-132). IEEE.

Shen, M., Wang, J., Joseph, A., Peng, F. Z., Tolbert, L. M. & Adams, D. J. (2006). Constant boost control of the Z-source inverter to minimize current ripple and voltage stress. *IEEE transactions on industry applications, 42*(3), 770-778.

Stout, P. J. & Zhang, D. (2002). High-power magnetron Cu seed deposition on 3-D dual inlaid features. *IEEE transactions on plasma science, 30*(1), 116-117.

Tanaka, T., Ishibashi, K., Ishikura, N. & Hiraki, E. (2010). A half-bridge inverter based active power quality compensator for electrified railways. *In The International Power Electronics Conference-ECCE ASIA-* (pp. 1590-1595). IEEE.

Tran, Q. V., Chun, T. W., Ahn, J. R. & Lee, H. H. (2007). Algorithms for controlling both the DC boost and AC output voltage of Z-source inverter. *IEEE Transactions on Industrial Electronics, 54*(5), 2745-2750.

Vinnikov, D. & Roasto, I. (2011). Quasi-Z-source-based isolated DC/DC converters for distributed power generation. *IEEE Transactions on Industrial Electronics, 58*(1), 192-201.

Vinnikov, D., Chub, A. & Liivik, L. (2015, June). Asymmetrical quasi-Z-source half-bridge dc-dc converters. *In 2015 9th International Conference on Compatibility and Power Electronics (CPE)* (pp. 369-372). IEEE.

Wai, R. J. & Duan, R. Y. (2005). High step-up converter with coupled-inductor. *IEEE transactions on power electronics, 20*(5), 1025-1035.

Walker, G. R. & Sernia, P. C. (2004). Cascaded DC-DC converter connection of photovoltaic modules. *IEEE transactions on power electronics, 19*(4), 1130-1139.

Wang, J., Wu, B., Xu, D. & Zargari, N. R. (2013). Phase-shifting-transformer-fed multimodular matrix converter operated by a new modulation strategy. *IEEE Transactions on Industrial Electronics, 60*(10), 4329-4338.

Wen, Y., Deng, S., Mao, H. & Batarseh, I. (2005). Unified steady-state and dynamic modeling for symmetric and asymmetric half-bridge DC-DC converters with current doubler rectifiers. *In Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 3*. (pp. 1525-1530). IEEE.

Win, T. S., Baba, Y., Hiraki, E., Tanaka, T. & Okamoto, M. (2012, June). A half-bridge inverter based active power quality compensator using a constant dc capacitor voltage control for electrified railways. *In Proceedings of The 7th International Power Electronics and Motion Control Conference* (Vol. 1, pp. 314-320). IEEE..

Win, T. S., Baba, Y., Okamoto, M., Hiraki, E. & Tanaka, T. (2011, December). A half-bridge inverter based active power quality compensator with a DC voltage balancer for electrified railways. *In 2011 IEEE Ninth International Conference on Power Electronics and Drive Systems* (pp. 185-190). IEEE.

Yao, Z., Xiao, L. & Yan, Y. (2009). Control strategy for series and parallel output dual-buck half bridge inverters based on DSP control. *IEEE Transactions on Power Electronics, 24*(2), 434-444.

Zhang, G., Li, Z., Zhang, B., Qiu, D., Xiao, W. & Halang, W. A. (2014). A Z-source half-bridge converter. *IEEE Transactions on Industrial Electronics, 61*(3), 1269-1279.

Zhang, W., Deng, M., Pei, Y. & Wang, Z. (2010). Design and optimization of high current power supply for electrochemistry. *In The 2010 International Power Electronics Conference-ECCE ASIA*- (pp. 86-91). IEEE.

Zhao, B., Yu, Q., Leng, Z. & Chen, X. (2012). Switched Z-source isolated bidirectional DC–DC converter and its phase-shifting shoot-through bivariate coordinated control strategy. *IEEE Transactions on Industrial Electronics*, *59*(12), 4657-4670.

Zhu, M., Li, D., Loh, P. C. & Blaabjerg, F. (2010, December). Tapped-inductor Z-source inverters with enhanced voltage boost inversion abilities. *In 2010 IEEE International Conference on Sustainable Energy Technologies* (ICSET) (pp. 1-6). IEEE.