ANALYSIS OF QUASI Z-SOURCE BASED FIVE-LEVEL INVERTER

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF

NEAR EAST UNIVERSITY

By
RASHEED ADEBAYO ADEGBOYEGA

In Partial Fulfilment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

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Approval of Director of Graduate School of Applied Sciences

Prof. Dr. Nadire CAVUS

We certify this thesis is satisfactory for the award of Masters of Science in Electrical and Electronic Engineering

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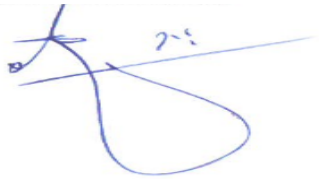

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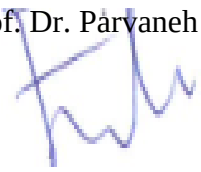

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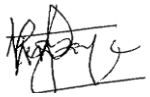
Signature: 

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ABSTRACT

The demands for electricity is ever risen as the technological advancement move along the same pace. With industrial development and domestic necessity of life, much emphasis have to be placed on latest trends on technology based on power electronics which provides power at higher output, lower losses and better quality.

This paper is an important novelty, proposed single-phase Q-ZS that analyzed different inverters at higher steps. The improved topology is fine-tuned by modulation and duty cycle variations which yield a better high energy with good quality. The proposed analysis reduces the current stress thereby reducing losses on the switches. This paper also elucidate the effects of more turns in inductor and so also the increase size of capacitor area that bring a desired energy. The performances of both the proposed inverter is well analyzed by calculation, modulation methods, simulation software and interpreted by experiments.

Keywords: Alternative phase opposition disposition; modulation technique; quasi-Z-source; impedance network; dc-dc boost converter

ÖZET

Teknolojik gelişme aynı hızda ilerledikçe, elektrik talepleri de artmıştır. Endüstriyel gelişme ve evsel yaşam gereksinimi ile, güç elektroniğine dayanan teknolojideki son eğilimlere daha çok önem verilmelidir. Bu makale, invertör üç seviyeli çıkış voltajını artırmak için yeni bir modifiye yarı-Z-kaynaklı (MqZS) invertör ile tek fazlı simetrik hibrit üç seviyeli invertör kombinasyonunu önermektedir. Önerilen tek fazlı MqZS hibrit üç seviyeli invertör, daha yüksek bir destek kabiliyeti sağlar ve hem tek fazlı üç seviyeli sinir noktası kelepçeli (NPC) qZSI hem de tek faz ile karşılaştırıldığında kaynak empedansındaki indüktör sayısını azaltır yarı-Z kaynaklı basamaklı çok seviyeli invertör (CMI). Ek olarak, iki üç seviyeli PWM anahtarlama hücresini ayrı bir MqZS ve dc kaynağıyla basamaklandırmak suretiyle dokuz seviyeli bir çıkış voltajı elde etmek için genişletilebilir, burada tek fazlı MqZS kademeli hibrit beş seviyeli invertör (MqZS-CHI olarak adlandırılır)). DC-link voltajını artırmak ve MqZS'nin iki seri kapasitör voltajını dengelemek için ateşleme durumunu etkin bir şekilde kontrol etmek için alternatif bir faz karşıt yerleştirme (APOD) şemasına dayanan bir modifiye modülasyon tekniği önerilmektedir. Önerilen MqZS-CHI ve modülasyon tekniklerinin performansları simülasyon ve deneysel sonuçlarla doğrulanmıştır. Dizin

Anahtar Kelimeler: Basamaklı evirici; karma beş; seviyeli evirici; modülasyon tekniği; yarı-Z kaynağı

To my parents...

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LIST OF ABBREVIATIONS

AC:	Alternating Current
BJT:	Bipolar Junction Transistor
C:	Capacitor value
CCM:	Continuous Conduction Mode
D:	Duty cycle
DC:	Direct Current
DCM:	Discontinuous Conduction Mode
E:	Energy stored in the inductor
IGBT:	Insulated Gate Bipolar Transistor
L:	Inductor value
LCD:	Liquid Crystal Display
MOSFET:	Metal–Oxide–Semiconductor Field-Effect Transistor
P:	Power Switching loss
PV:	Photo-Voltaic
S:	Switch
SMPS:	Switching-Mode Power Supply
T:	Total time period
t:	Time period
$\mathbf{C_o}$**:**	Output Capacitor
$\mathbf{C_1}$**:**	The First Capacitor value
$\mathbf{C_2}$**:**	The Second Capacitor value
$\mathbf{D_o}$**:**	Output Diode
$\mathbf{D_1}$**:**	Diode number One
$\Delta\mathbf{I_L}$:	the variation Inductor current
$\Delta\mathbf{I_{Loff}}$**:**	the variation Inductor current during off-state
$\Delta\mathbf{I_{Lon}}$**:**	the variation Inductor current during on-state
$\mathbf{f_s}$**:**	Switching Frequency

IGBT:	insulated-gate bipolar transistor
$\mathbf{I_{Co}}$**:**	Output Capacitor Current
$\mathbf{I_D}$**:**	Diode Current
$\mathbf{I_L}$**:**	Inductor Current
$\mathbf{I_{L1p}}$**:**	Parallel Currant during Inductor number One
$\mathbf{I_{L2p}}$**:**	Parallel Currant during Inductor number Two
$\mathbf{I_{Lmax}}$:	Maximum inductor current
$\mathbf{I_S}$**:**	Switch Current
$\mathbf{L_1}$**:**	Inductor number One
$\mathbf{L_2}$**:**	Inductor number Two
R:	The value of Output Resistant
$\mathbf{S_1}$**:**	Switch number One
$\mathbf{S_2}$**:**	Switch number two
∂**:**	Constant
$\mathbf{t_0}$**:**	Time at the start point
$\mathbf{t_1}$**:**	Time at the point One
$\mathbf{t_2}$**:**	Time at the point One
$\tau_{\mathbf{LB}}$**:**	The Inductor Time constant for Boundary Condition
$\mathbf{T_1}$**:**	Switch constant time
$\mathbf{V_i}$**:**	Input Voltage
$\mathbf{V_O}$**:**	Output Voltage

CHAPTER 1
INTRODUCTION

The modern technology of energy conversion is important especially to the safety and sustainability of the creature. For many years power electronic converters laid the foundation of energy conversion chain. These converters play very important role in advancing modern technology through numerous means such as renewable energy system, industrial machineries and home appliances (Mao and Batarseh, 2005)

The olden days inverters, the Ac output voltages are less than the dc input voltage due to poor understanding of inversion methods.

Several researchers contribute hugely in introducing different topologies of these converters. Recent research has examined combinations of basic converter configurations, for instance, that which could bring about huge energy at the output terminal by the use of impedance networks.
Therefore, in other to have better output and quality signals with little or free harmonics, the number of this converter has to be increased.

1.1 Thesis Problem

The proposed topology has many benefits as stated but in the application of it faces the challenges of high current stress, conversion problems and addition of the interfering inverters and irrational duty ratio reduce the overall performance of the system.

These are two inverter connected together in series. The output of one unit is connected to the input of the other. This brings about increase in the output voltage of the overall inverters.

With all the advantages and applications of these converters, the combination of two different voltage sources and addition of an impedance network in the circuitry will bring about a boost in energy at the output terminal. This additional combination of different inverters is cumbersome, heavier, space demanding and costly. These have been replaced by alternating network, with less components and effective.

Moreover, it suppresses overall conversion efficiency and the problem of power losses across the switches that becomes severe under this condition.

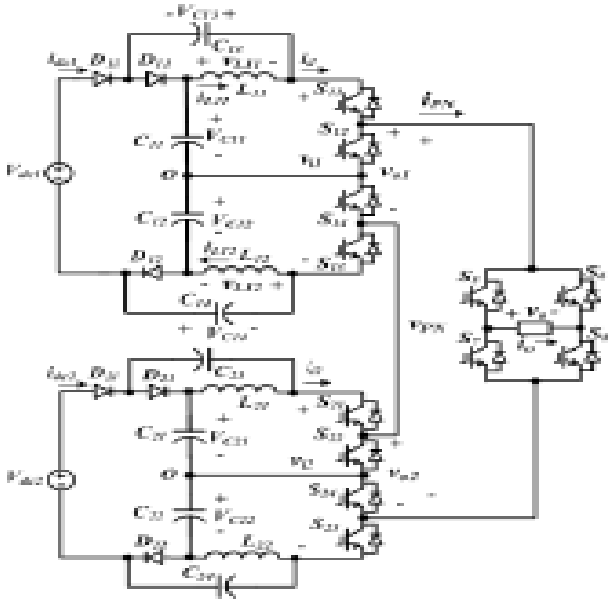

Figure 1.1: A cascaded inverters

1.2 Aim of the Thesis

The aim of this thesis research is to analysis, design and modified different kinds of single phase inverters that can produce a higher output voltage with limited switches and components. In recent years (Berkovich and Loinovici 2008) introduced modified dc-dc converter by using capacitor-switch and inductor-switch for design transformer less converter. Likewise is another researcher who worked on three switches high voltage converter (Pietkiewicz and Cuk, 1999)

The methods of integration of Z- source energy conversion idea is to vary the modulation indices as theduty cycle changes.

1.3 Importance of the Thesis

This work will also come up with latest converter that can solve the problems of switching mechanism, inductance leakage that produce high voltage stress to the components. Moreover, the overall conversion efficiency of this converter would be very reliable and the switches voltage stresses will be very low compare to traditional converters.

1.4 Limitations of the Study

For accuracy of the investigation all the components are considers as ideal, the capacitors, inductors, diodes, resistors and inductors are considered adequately good to have the constant voltage. Simulation will be done using PSCAD software throughout the research.

1.5 Overview of the Thesis

This thesis has four chapters as follows.

Chapter I of this thesis introduces general background, outlines the challenges and drawbacks inherited by traditional inverters, poor performances and proposed ways to minimize them.

Chapter II discusses the fundamental background, investigates the relevant theories, characteristics and comprehensive literatures review and recent achievements on various Quasi Z-source of different levels against the traditional inverters and their vast importance.

Chapter III introduces different components arrangement, tabular analysis, further analysis on Quasi Z-source Inverters and multiple simulation of results using PSCAD software to prove the higher voltage gain performances of the inverter.

Chapter IV focuses on conclusions and summary of the thesis. General recommendations and identifies the areas to advance the work in the future will also be presented.

1.6 Ethical Consideration

Considering the standard ethical feature and preparation of research procedures, the standard research procedures are implemented throughout the thesis. Moreover, the appropriate considerations and credit were given during the use of other people`s words or ideas by proper citing.

CHAPTER 2

RELATED RESEARCH

2.1 A Conventional Multilevel Inverters

This is a device with source of supply of voltage in one side and the modified output voltage from the other side as controlled by the switching devices of the system. The inverter is majored in 3 types:

a) The Bridged-cascading;

b) Neutral point-clamped and

c) FLC inverter.

2.1.1 Bridged-cascading inverter

In cascaded multilevel inverters, the arrangement of the switches, discrete components, solid state elements such as diodes are arranged in H or Bridge shape. The four switches of each unit of the inverter join each other by emitter-collector connection of switch 1 to 3 and that of switch 2 to 4 for a unit cell. The collector leg of one transistor is then connected to the emitter leg through a source of supply. And from the center of the first pair switch S1 and S3, a terminal connection is made out the same is repeated for switch S2 and S4. This form the output terminal of the multilevel as appeared in the diagram below:

Increase the output produce by this inverter, it is then connected in cascading. This is a process by which the each unit of the inverter are added together in series. Each separate unit has its own source of input values.

Voltage generated is a function of number, level, which equally depends on the unit cell. The value gotten at the output terminal of the system is in manifold as compared to the initial primary source. (F. Z. Peng, 2003)

Cascaded multilevel inverter comes in different forms depending on the needs and purpose to which it is to serve. Various CMI come with the integration of diodes, capacitors, inductors etc

It is used in many domestic and industrial applications because it is easier duplicating and cost effective.

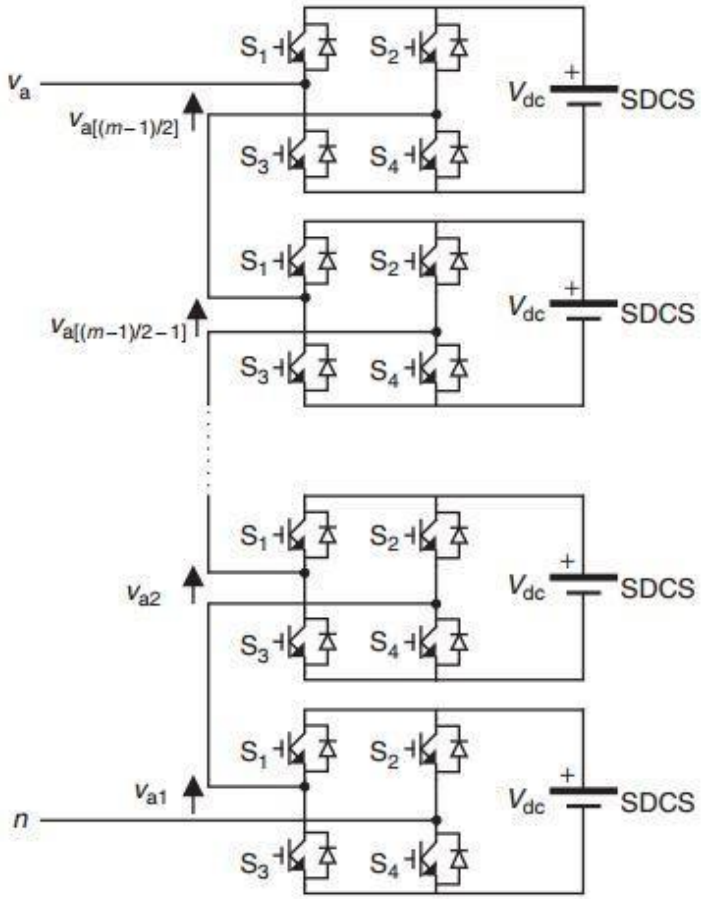

Figure 2.1: Structure of a multilevel CH-BI

2.1.2 Neutral point CMI

The other type device, the Diode clamped multilevel inverter. In its connection are the diodes joining one switch to the other. That is one diode is connecting with two switches by taking in signal and the other returning it for a perfect circuitry. The center of this two diodes connected to the four switches are center-tapped and clamped at the input source.

NPC device has applicable areas especially where high demands of voltage is required as in HV dc line and in FACT. We equally make use of it in the industries where higher torque is needed to rotate electrical machines at different speeds.

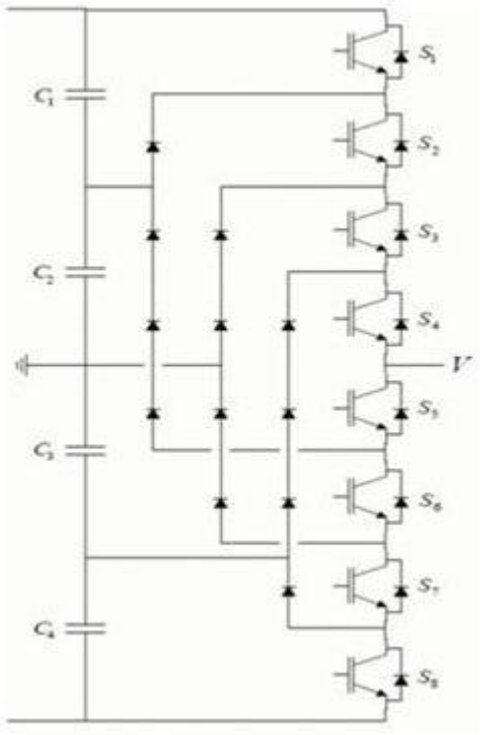

Figure 2.2: Seven level DCI

2.1.3 FLC Inverter

In flying capacitor multilevel inverter, it has the same similarity with the position of diode clamped only that the center of the two opposing switches are connected with capacitor, fig. 2.3, and the four switches are tapped at the middle and earthed. Equally the emitter and collector are connected to the input source for powering the inverter. And two series capacitors connected across the switches are center tapped to the ground at the input side. FCMI can work for a longer period because of the numbers of capacitors that continually storing charge energy. It has a vast application in industries in taking charge of both active and reactive power (M. Shen and D. J. Adam, Jul. 2007).

Part of its demerit is the bulkiness of the capacitors and the number one would have to attain in making a higher valued voltage.

The same connection is repeated three times for three phase inverter for the practical purposes.

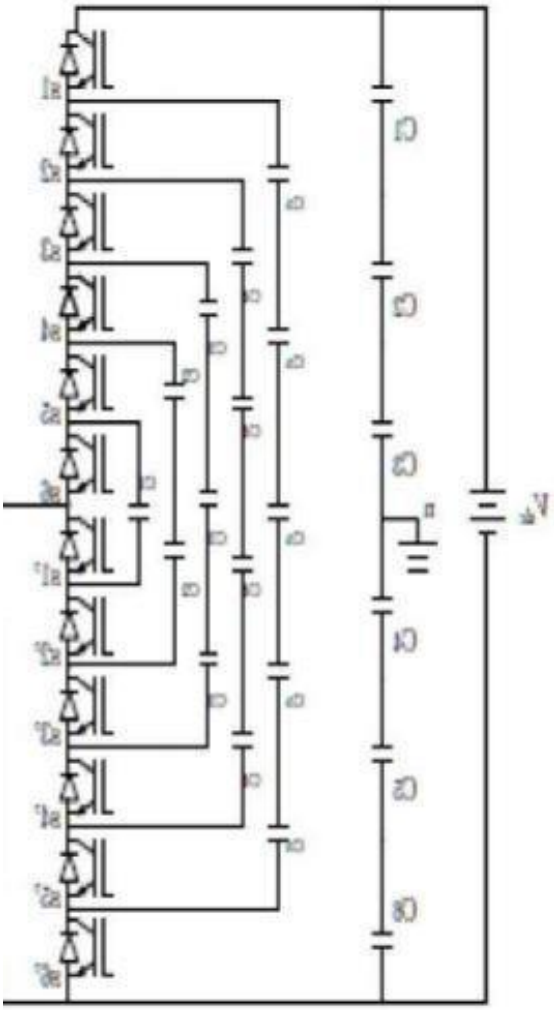

Figure 2.3: Seven level capacitor clamped inverter

2.2 A Reduction in Switches Quantity

The idea behind this topology arose as a result of reducing the bulkiness of inverters and cost effectiveness. Though some of the components are not expensive like diodes and capacitors but, switches are very costly and fragile in handling. With latest in technology, system are coming handy and portable. That is why the incorporation of diode-clamp and H-bridge circuit are made to bring about the reduction in switches. The diode clamped will produce a stair-shaped sinusoidal graph while the H-bridge produce the needed Ac signal having

negative and positive poles. In addition we make use of capacitors to separate the DC-link voltage to different levels depending on the exigence of demand. The voltage eso formed from the capacitor, Vc can be added to get a stair-shaped graph. This is shown in the diagram below:

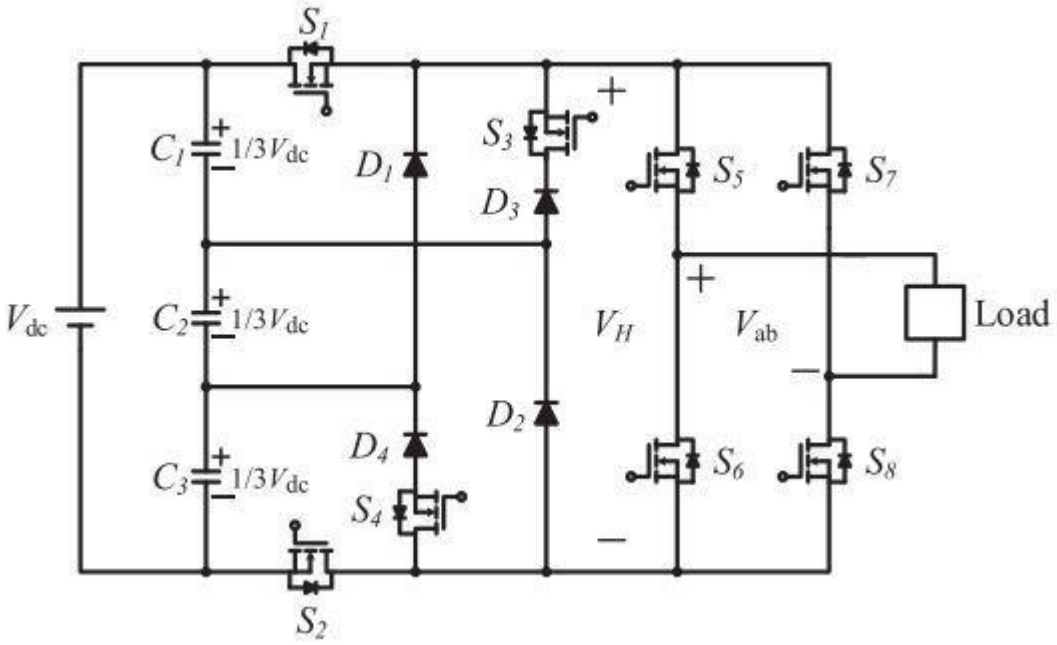

Figure 2.4: Switches Reduction 7-level inverter

2.3 Analysis of a Steady-State and Impedance Structure in Network of ZSIs

As seen in the figure 2.5 below is a topology of a symmetrical impedance network having diode D_s in series with the primary source of supply while the Z-source come between the conventional inverters and input source impedance network comprise of two capacitors and inductors arranged to bring about a boosting value. The impedance network changes the circuit behavior from the initial input source characteristics to a boosting character for the inductors and capacitors being a storage device act as an alternate source of supply. This would now operate as shoot-through with the same inverter leg with input source at the same axis.

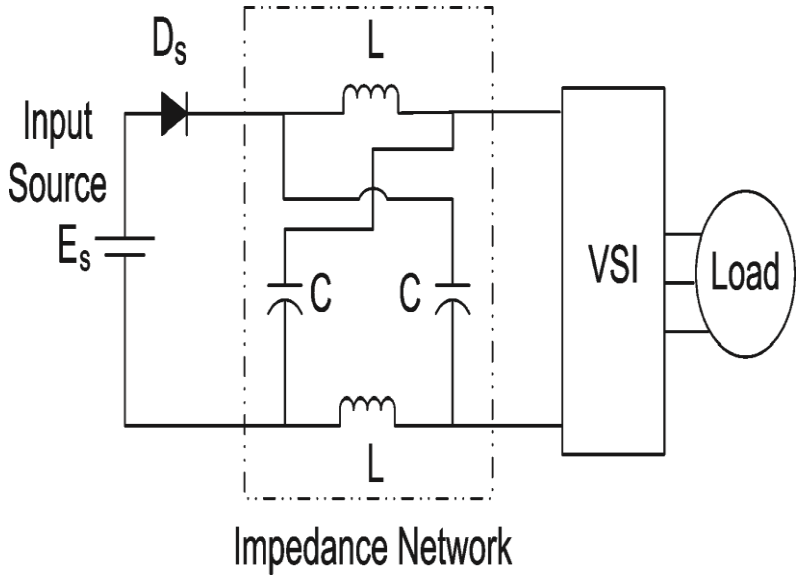

Figure 2.5: ZSI with a symmetrical impedance network

This topology has a vast of merits both at the domestics and industrial usage for a lot of application that demand higher power qualities. These include fuel cell vehicles, residential solar system, motor drives, UPS, distributed generators etc.

2.4 Principle of Operation of Stationary mode of ZSI

Looking at figure in 2.6, we see the arrangement of the circuitry as the Ds is in series with the supply voltage of the circuit. It is the primary source of supply such as photovoltaic cell and the inductors and capacitors in parallel connection between the source voltages. The source inverter between output terminal and the input source and act as a regulatory component for the analysis.

The diode Ds from the input been a unidirectional has an ON and OFF state for switching while Voltage source inverter VSI has three regulating terminals at the its output. It source out voltage developed from the storing components which is boosted within it to a larger value. The three terminals on the VSI are representing the switching state of the system as state–one, state-two, and state–three.

The mode of operation is that when the diode Ds is closed, current Is pass through the through the inductor and build an inductive voltage, V_l within. The same effect is manifested at the capacitor by building V_c. Both are storing devices and an impedance network between the

input and the output of the inverter. With this type of topology, it is the input for the VSI. The voltage built up are fed to the inverter as dc/dc booster. During the period Ds is put ON is the active state of the inverter. As soon as the Ds is put OFF, the voltages developed by the storing devices are then consumed by the circuit for inversion processes.

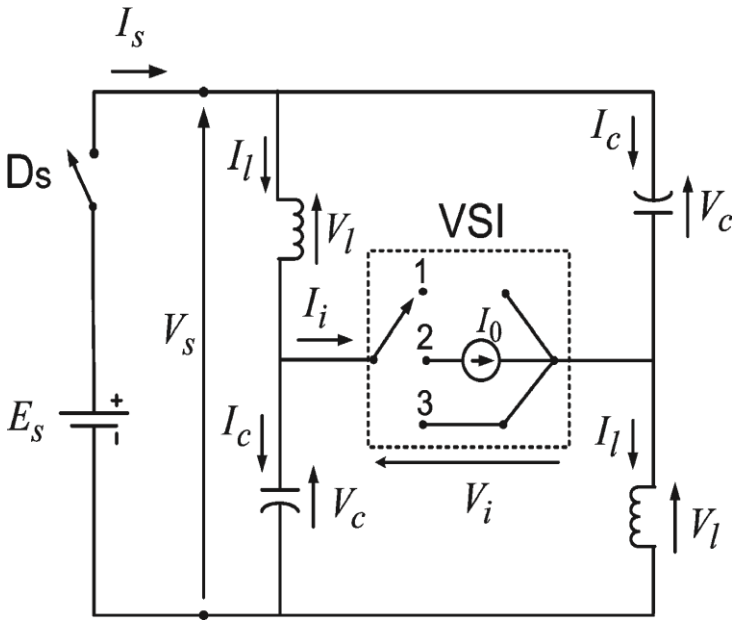

Figure 2.6: switching equivalent of ZSI

The switching operates in three mode form; the Alert, Active and the Shoot-through.

This is the active state of the inverter and when it when the diode is put at OFF, the impedance network is remained active. Likewise when the diode Ds is at open mode, the stored energy during active periods "t" are used up by the components and load in the circuitry. The third input stage, that represent "SH-TH" stage (F. Z. Peng, 2003.) is presented below:

Table 2.1: Possible operating stages of the Z- network

VSI	ACTIVE	ALERT	SH-TH
D2	Active Inactive	Active Inactive	Inactive Active Sh-Th-II
Z-network Alert-1 Alert- II	Active-I Active-II	Sh-Th-I	

It is however to be noted that the Alert-I, Alert-I, with Sh-Th-I needed stages for real life usages. They are the state that are real to practical handlings and application but, Alert-II, Alert-II, for Sh-Th-II stages, riot to desirability of practical purposes.

The mathematical analyzes between the V∞ I for all the listed stages are equated below:

$$Io_c = C(dV_c/dt)\ , \quad V_{lnput} = L(dI_l/dt) \tag{2.1}$$

$$Vs_{upply} = Vc + Vl, \qquad Is = Ic + Il \tag{2.2}$$

$$Ii = Il - Ic, \qquad Vi_{nput} = V_c - V_l \tag{2.3}$$

Then for Alert-I state equations:

$$E_{sending} = V_{supply} \qquad I_{in} = 0. \tag{2.4}$$

Putting (2.4) into (2.1)–(2.3), then Vc across and Ic can become:

$$\frac{d^2V_c}{dt^2} + \frac{V_c}{LC} = \frac{E_s}{LC}$$

$$V_c = E_s + X_O \sin(\omega t + \Phi_O) \tag{2.5}$$

$$I_c = I_l = I_s/2 = X_O \omega C \cdot \cos(\omega t + \Phi_O) \tag{2.6}$$

Where,

$$\omega = 1/\sqrt{LC} \tag{2.7}$$

$$X_O = \sqrt{(V_{ciO} - E_s)^2 + [I_{liO}/(C\omega)]^2} \tag{2.8}$$

$$\Phi_O = \tan^{-1}\left((V_{ciO} - E_s)\omega C/I_{liO}\right) \tag{2.9}$$

When considering Alert-I stage by V_{cap} and I_{lind}, by evaluating its positive sizes, V_{cap} and I_{lind}, varying from the starting angle $\Phi_0 = 0$ to 180 related thus:

$$V_{inp} = 2V_{cap} - E_{supply}\ ; \qquad V_{ind} = E_{supply} - V_{cap}\ . \tag{2.10}$$

By varying the angular disposition from 0 to 180, the capacitive voltage gain maximum size, while inductive value tends to 0. But if the system is subjected to work under Alert stage above the ranging period while Ds is OFF and current flows in opposition. Then Alert-I would stop while stage of Alert-II starts.

Alert-II stage, Ds is in the in active stage and the system Alert stage then, the stage relating expression goes thus:

$$I_{inpt} = 0 \quad ; \quad I_{supply} = 0. \tag{2.11}$$

And as input is the same as

$$I_{lfO} > 0 \tag{2.12}$$

Active state I

In active state-I, the main changes in Alert-I, Active-I stages is the availability of the stable current generated from the source to the inverter as presented in given diagram 2.

The equations for Active-I stage

$$I_{inp} = I_0\text{ut.} \quad ; \quad V_{supply} = E_{supply} \tag{2.13}$$

By putting (2.13) inside (2.1)–(2.3), arrived:

$$V_c = E_s + X_A \sin(\omega t + \Phi_A) \tag{2.14}$$

$$X_A \omega C \cdot \cos(\omega t + \Phi_A) = I_{cap} = I_{ind} - I_0 = (I_{supply} - I_0)/2 \tag{2.15}$$

$$X_A = \sqrt{(V_{ciA} - E_s)^2 + [(I_{liA} - I_0)/(C\omega)]^2} \tag{2.16}$$

$$\Phi_A = (\tan)^{-1}((V_{ciA} - E_{supply})\, \omega C/(I_{liA} - I_0)) \tag{2.17}$$

And this is the same for the Active -I stage.

In equation (15), the current through the diode I_s is observed to turn 0 while Ds remain at off position.

Then,

$$I_{ind} = -I_{cap} = I_0/2.$$

Worthy of maximizing end value parameters expressed as

$$V_{cfA} = E_s + X_A \sin(\omega t_A + \Phi_A) \quad (2.18)$$

$$I_{lfA} = I_0 + X_A \omega C \cdot \cos(\omega t_A + \Phi_A). \quad (2.19)$$

For Active-II Stage,

$$I_{input} = I_0 \quad I_{supply} = 0. \quad (2.20)$$

By putting equation (2.20) in (.2.2) and (2.3),

$$I_{ind} = -I_{cap} = I_0/2$$

$$I_{lfA} > I_0/2. \quad (2.21)$$

And in SH-TH-I Stage,

$$I_{supply} = 0, \qquad V_{inp} = 0. \quad (2.22)$$

Putting equation (22) inside the capacitive voltage and current euations, we arrived at:

$$V_c = V_l = V_s/2 = X_S \sin(\omega t + \Phi_S) \quad (2.23)$$

$$I_c = -I_l = X_S \omega C \cdot \cos(\omega t + \Phi_S) \quad (2.24)$$

Where,

$$X_S = \sqrt{(V_{ciS})^2 + (-I_{liS}/C\omega)^2} \quad (2.25)$$

$$\Phi_S = \tan^{-1}(-V_{ciS}\omega C/I_{liS}) \quad (2.26)$$

The voltage source inverter appears equation (2.23), is observed with ts period with other two state parameters as equated thus

$$V_{cfS} = X_S \sin(\omega t_S + \Phi_S) \quad (2.27)$$

$$I_{lfS} = -X_S \omega C \cdot \cos(\omega t_S + \Phi_S). \quad (2.28)$$

The last Stage is the Sh-Th-II, here:

$$E_{supply} \; ; \; V_{supply} \qquad V_{input} = 0. \quad (2.29)$$

By equating (2.29) in (2.1)–(2.3), it is observed thus:

$$V_{cap} = V_{ind} = E_{supply}/2$$

Therefore,

$$I_c = 0$$

Then, equation (2.30) below proffers necessary condition to be met in preventing damage to the system, VSI as the hike in inductor current I_l corresponding to $E_s/(2L)$

$$V_{cfS} > E_s/2. \quad (2.30)$$

2.5 General Overviewing of Operating States/ Stages

By inferring on the overall work, we obviously see Alert-II, Active-II, and Sh-Th-II stages have no impact to the conversion processes. That is the reason they are inactive as could be seen in this thesis. But the modern converters at real life operate in stages of the Alert-I, Active-I and Sh-Th-I stages. This is tagged a "moving states." And the erratic behavior of storing devices towards unbalanced voltage and current conditions led to equations (2.12), (2.21), and (2.30).

Therefore, it is imperative to correct the size of the capacitor and the number of turns in inductor to reduce the harmonics and improve the power quality through their values.

Therefore, emphasis has to be put on the consideration of the sizes of the capacitors and the turn ratio of the inductors to prevent voltages and current erratic behavior in design.

CHAPTER 3

CIRCUIT PRESENTATION, MATHEMATICAL ANALYSIS AND SIMULATION

3.1 The Three- level Z-source Diode Clamped Inverter

The inverter has low cost as a result of lower components and voltage source. It uses the same voltage source and the impedance network to operate.(F. Gao, and F. Blaabjerg, 2007). The working analysis of the modulation methods used PD, which has higher signals and with lower harmonics. All these are achieved by period of the oscillation from the reference. The control of the load current and voltage are determined by the inductors and capacitors. And which is at the same time subjected to the arrangement of the switches in line with these components.

Equally, a three-level neutral point clamp (NPC) quasi-ZSI is discussed in (Bayhan, M. Trabelsi, 2015) where an impedance network of proposed topology combined with an NPC system. This provides multilevel output voltage and continuous Dc current source. And the boost factor remain the same despite the two are symmetrical..

Likewise by using photovoltaic (PV) as primary source of energy, the control and analytical design of a quasi-Z-source can be enhanced. And with this minimum energy, current and voltage balance control can be achieved, (M. Sahoo and S. Keerthipati, 2017). Each solar panel connects to a separate inverter. The more the number of the solar panel, the more the generated input source which consequently lead to more output voltage.

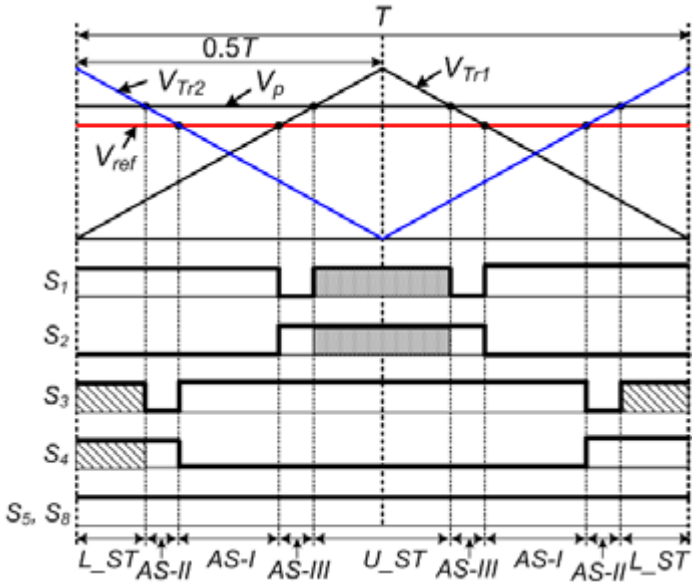

Figure. 3.1: A proposed topologies Result

3.2 The Single-phase Modified Quasi-Z- source Hybrid Three-level Inverter

This inverter has its two inductor removed. There is a connection of a diode across the voltage supply at the upper network. This added with a similar inverter that is hybrid. (H. Abu-Rub, and R. S. Balog 2015). The Z-source network is linking the switches and the primary source. A boosting circuit that comprise of the storing device, capacitor and inductors are connected across the diode in series. And two capacitors are connected in series and join with the storing device parallel to the mess connection. At the output terminal are the four different switches which modified the inverter in parallel connection with the switches.

3.2.1 Mode of operations.

It operates using a full bridge single phase inverter. It is a three-level inverter that has a switching pattern as S5 and S8. This is paired to work as S5/S8 and S6/S7 when it is put to ON position do that positive polarity and negative can be generated as the output signals. Then S1 and S4 are switched to generate high output voltage as shown below:

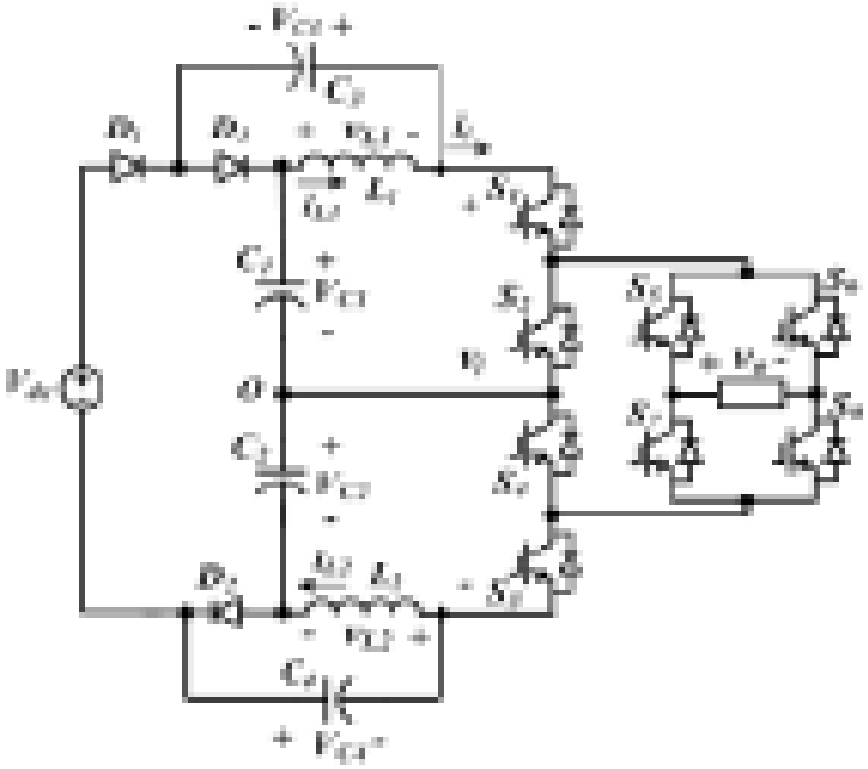

Figure 3.2: 3-Level hybrid inverter

This is a modified quasi hybrid inverter. As we can see that the network circuitry consists of two parallel capacitors between the output source and the switches. Another capacitor is connected the diode D1 and D2 across the inductors L1 and L2 respectively. Though this arrangement the input voltage can be increased in double.

Assuming:

Vc1 = Vc2

Vc3 = Vc4

That analysis the symmetric of the impedance network.

We have two operational mode for the hybrid inverter:-

a) The shoot-through state SH-TH;
b) The non-shoot-through state N-SH-TH.

The output voltage determine the operation methods.

a) The shoot-through state, SH-TH.

There are two states for the inverter, the upper and the lower:-

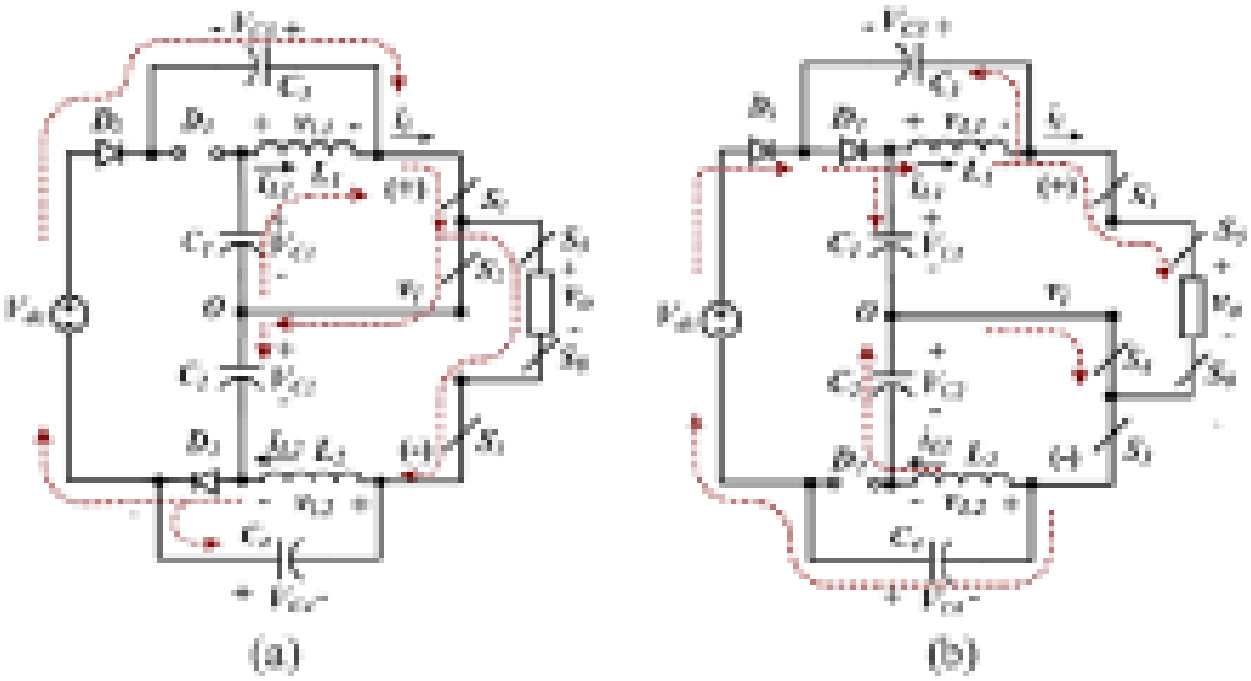

Figure 3.3: (a and b) Equivalent circuits of hybrid inverter

There is a middle point between the two centre capacitors. In the first diagram, the diode D1 is open circuit after input source charged the storing devices, capacitor and inductors, this bring about upper and the lower by stored energy acquired are then discharged through diode D2 in other as equated below:

$$VL1 = -Vdc - Vc3 + Vc1 + Vc2 \quad (3.1)$$

$$VL2 = -Vc4 \quad (3.2)$$

$$Vi = Vc2 + Vc4$$

With the diode D1 and D2 the invertrs are turn ON and OFF at the level of lower- shoot through whe the diode D2 is OFF.

$$VL1 = -Vc3 + VL2 = -Vdc - Vc4 + Vc1 + Vc2 = Vc2 \quad (3.3)$$

$$Vi = Vc1 + V3 \quad (3.4)$$

b) Non-shoot-through state, N-SH-TH.

At Ta in this stage, D1, D2 are placed Active while diode Di is OFF. We have four divisions in stage:

i. Active N-St-TH stage I,
ii. Active N-St-TH stageII
iii. Active N-St-TH stage III
iv. Stage of 0

In active stage I, at maximum input voltage Vi, the switching devices S1 and S3 are turned ON fig. (a)

Energy is transferred to the inverter in active stage II, L1, C1 as shown in fig. (b)

Likewise in active N-St 3, as L2 and capacitor C2 transfer stored energy to the inverter. It is however worth noting that in the two stages, Vi is transfered output. And inductors and capacitors do the effective charging of the circuitry.

But in the zero state, there is no voltage at the load terminal.

These are shown with the equivalent circuit diagrams as presented in the figures 3 (a,b,c and d) behind this page:

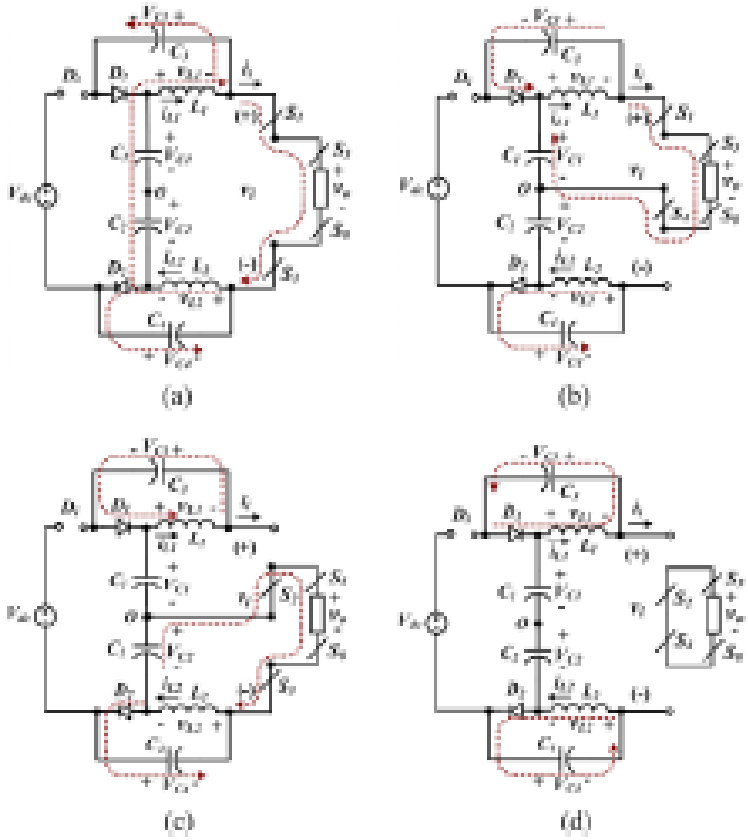

Figure 3.4: All the operating states

VL1 = -Vc3, VL2 = -Vc4 (3.5)

V1 = Vi = Vc1 + Vc2 + Vc3 + Vc4 (3.6)

Vo = Vc1 +Vc2 + Vc3 + Vc4 = Vi for active state I (3.7)

Vo = Vc1 + Vc3 = 0.5Vi state II (3.8)

Vo = Vc2 + Vc4 = 0.5Vi state III (3.9)

Vo = 0 active state 0 (10)

c) Boost Factor

By using formula, L1 and L2 in equations (3.1), (3.3) and (3.5)

VC1 =VC2 and VC3 =VC4 then the equations relates with duty ratio and shoot period as thus:

$$Vc1 = Vc2 = \frac{1-\frac{Tsh}{T}}{1-2\left(\frac{Tsh}{T}\right)}, \quad Vdc = \frac{1-D}{1-2D} Vdc \tag{3.11}$$

$$Vc3 = Vc4 = \frac{D}{1-2D} Vdc \tag{3.12}$$

where Tsh = shoot-through period T, and

D = Tsh/T = duty ratio.

By substituting (3.11) and (3.12) into (3.6),

we have equation:

$$B = \frac{Vi}{Vdc} = \frac{2}{1-2D} \tag{3.13}$$

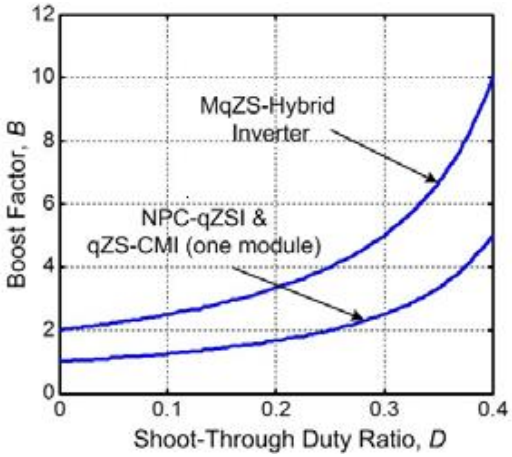

Figure 3.5: Boost factor against duty ratio

d) Difference with Existing Topologies

In comparing proposed performance topology, it is observed that the performance has a better output quality with less components. Its boost factor is higher with traditional inverters but has less harmonics. qZS-CMI (L.Ben-Brahim, and F. Z. Peng, 2014).

Looking at table 3.1, it expresses different inverters with different components needed to give five-level output voltage. The demands of individual inverter to components fixture differs so also is the characteristics. The hybrid inverter is two inductors less than other traditional inverter. And all has the same number of capacitors and switches. It is equally observed that the diodes reduces in the proposed topology by half while its by one third in the cascaded inverter. In the traditional inverters, the current stress increases as the voltage gain of ac increases. But for Neutral point quasi-source, the current stress remain constant with varing ac gain at output current of 1.5 and likewise, when the output current (RMS) drop to a reasonable value, the Hybrid inverter at this [point maintain a steady constant of output current at a varying AC voltage gain.

Table 3.1: Quantities of Elements to produce five-level output voltage

Descrete Elements	**H- I**	**Diode-clamp Inverter**	**Cascaded I**
L	2	4	4
C	4	4	4
Switches	8	8	8
Diodes	3	6	2
Pry. source of supply	1	1	2

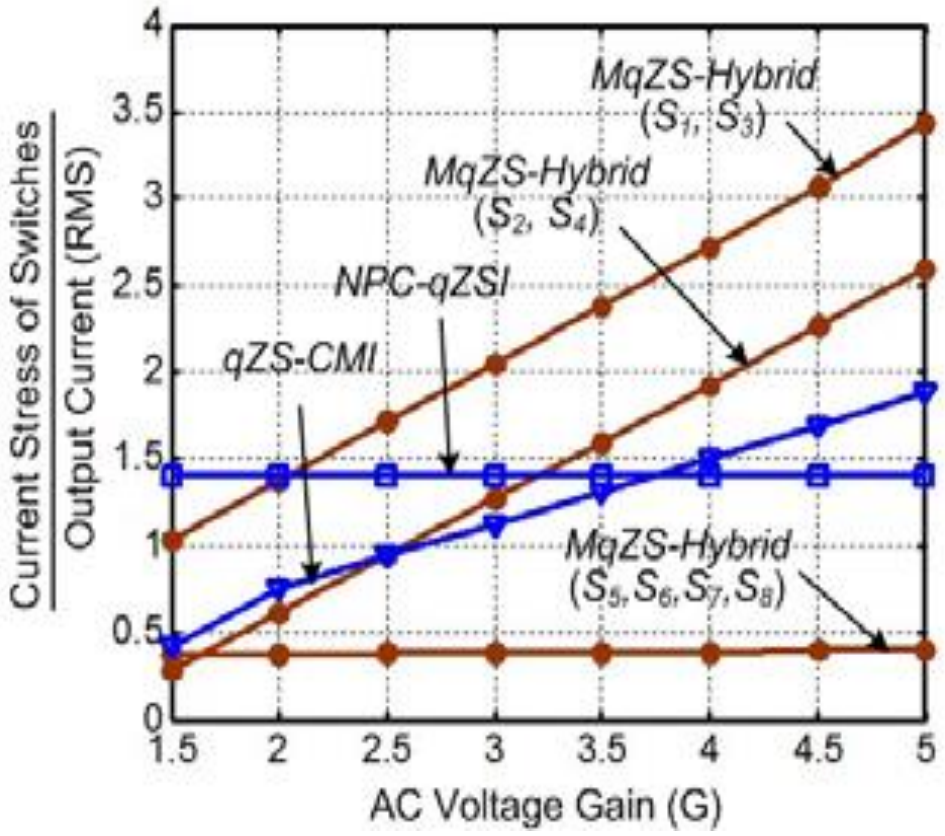

Figure 3.6: Current stress against ac voltage

Also, table 3.2 analyses the behavior of the switches, diodes and all other components to the root mean square of the alternating output voltage.. We can observed that other traditional inverters have lower voltage stress.

Table 3.2: Analysis of voltage stress

Elements		**H- I**	**Diode Clamp**		**Cascaded I**	
Switches	S1-S4 S5-S8	$1/\mathbf{1/\sqrt{2}(1-D)}$		$\mathbf{1/\sqrt{2}(1-D)}$		$\mathbf{1/\sqrt{2}(1-D)}$
		$\frac{\sqrt{2}}{1-D}$				
Cs	C1,C2	$\mathbf{1/\sqrt{2}}$	C1C4	$\mathbf{1/\sqrt{2}}$	C1	$\mathbf{1/\sqrt{2}}$

	C3,C4	$\mathbf{1/\sqrt{2}\ v/(1-v)}$	C2,C3	$\mathbf{1/\sqrt{2}\ \frac{D}{1-D}}$	C2	$\mathbf{1/\sqrt{2}\ \frac{D}{1-D}}$
Ds		$\mathbf{1/\sqrt{2}(1-D)}$		$\mathbf{1/\sqrt{2}(1-D)}$		$\mathbf{1/\sqrt{2}(1-D)}$

In table 3.2, it analysis the relationship that exist between the switching devices and the descrete components, diode and capacitor. At S1 to S4, all the inverters have the same switching pattern. The three inverter have the same current stress. But as bsoon as the switch S5 to S8 are toggled the current stress is doubled in hybrid inverter than the other topology.

At capacitor C,C4, the duty ratio is doubled as the capacitors are varied for output maximum voltage. The hybrid has the higher current stress with switches S2 and S4

Table 3.3: Analysis of current stress

Descrete elements	**H- I**	**Diode clamp**	**Cascaded I**
Ls	L1-L2 $\frac{\sqrt{2(1-D)}}{1-2D}$	L1-L4 $\frac{1-D}{\sqrt{2(1-2D)}}$	L1-L4 $\frac{1-D}{\sqrt{2(1-2D)}}$
Ds	Di $\frac{1-D}{\sqrt{2D(1-2D)}}$	D1,D2 $\frac{1-D}{\sqrt{2(1-2D)}}$	D1,D2 $\frac{1}{\sqrt{2(1-2)}}$
	D1D2 $\frac{1-D}{\sqrt{2(1-2D)}}$	D3-D6 0.25	

3.3 Boost Modulation Technique

This is the method by which the carrier and reference signal of the inverters are modulated. It is the appropriate way of changing the output signal by varying the reference signal. Likewise to control the output frequency, it is enough to change the reference signal frequency. The switching losses increases as the number of pulses increases. We should consider Fc not to be more than Fr. The more Fc the more the losses and the more the costfor filters.

Fc ≥ fr, fc ≥ fo where fo is the fundamental frequency of the system.

In most application in industries, fc is always 1Khz to 10Khz.

But when fc is greater than fr, there is higher cost, high losses and less energy.

And when fc is lower than fr, there is lower cost, low losses and higher filter. The designer design the value of fc to meet the output voltage and cost. The ratio of the reference signal to carrier signal is called the index modulation of the system.

3.4 Analyzing of SPHB Modified Quasi-Z-source Cascaded Five-level Inverter

Three separate units of a Quasi-Z-source cascaded Hybrid, modified forms a number of levels inverter. Each unit has the same similarities as the other. The similarities in terms of input voltage,Vi to the system, discrete elements like capacitors and inductors, the solid state elements like diodes, the switches and the snubbers etc.

Taking a unit for a description purpose, it is observed that the input voltage, Vi is in series with inductor L and Diode Di. These are connected to four switches. And at the negative polarity of the is connected to the two emitter legs.in between the input voltage and switches are the impedance network that interface between the input signal and control of the system, different designers have different arrangement/ combination of their impedance components. And sometimes it equally depends on what is expected of the impedance source to perform. In some cases, it could be inductive L, capacitive C arrangement, and in some it could be diodes, inductor and capacitor arrangement placed in-between the input source and switches.

So also, Quasi is the modified circuit which are attached to the impedance network to fine-tune the performance of whole inversion. It is always placed above in parallel arrangement with Z-source network. Then there comes a connection of a capacitor that bridge the collector-emitter legs in split or H arrangement. All these form a single robust unit of an inverter.

To increase the voltage at the output, the Z-source network, a booster regulates to a desired value that commensurate with the output demand. The diode regulate intake current to the circuit against damage of the switches. But there is limitation to the regulation of the boosting circuit, more cells have to be connected in series a phenomenon called cascading. With this, more voltage can be generated at the output of the inverter.

In the institution of cascading, we have a Symmetrical multilevel inverter and asymmetrical multilevel inverter. In symmetrical arrangement, all the organs of the circuit in a particular

cell or unit appear the same with one another but, in asymmetric cascaded, there are differences in the configuration of the units.

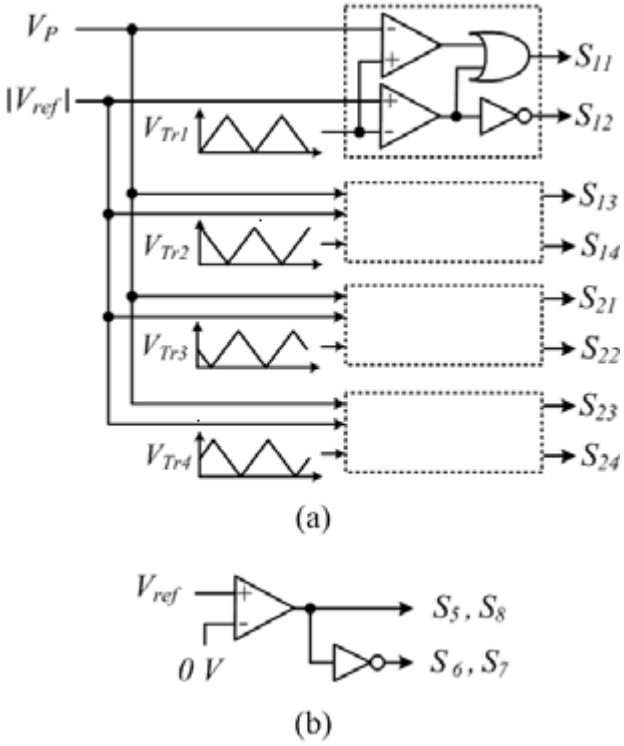

Figure 3.7: Modified inverter logic

3.5 Simulation and Analytical Results

Simulation is done out on proposed circuit using PSCAD software which delivered a very accurate results. The results are presented in the table as shown behind:

Table 3.4: Elements used for simulation and experiments

Elements	**Type/ Value**
DSP	TMS320F2835/32bit, 150MHz
Switches	IGBT SKM 100GB 12T4/ 1200V, 150A
Diodes	STTH200L 06TC/ 600V, 30A
Capacitors C_{11}…..C_{22}	DCMC 102 T450/ 1000µF
Inductors L_{11}.....L_{22}	1mH
LC_{output}	L_f = 1.2mH, C_f =2.5 µF
RL	R_L =50ohm, L_l =10.7mH

The underline figure has vPN. It is a graphical representation of modulation at 80% when the duty cycle is 20%. The output voltage is almost three times increment using the single phase full bridge five-level inverter.

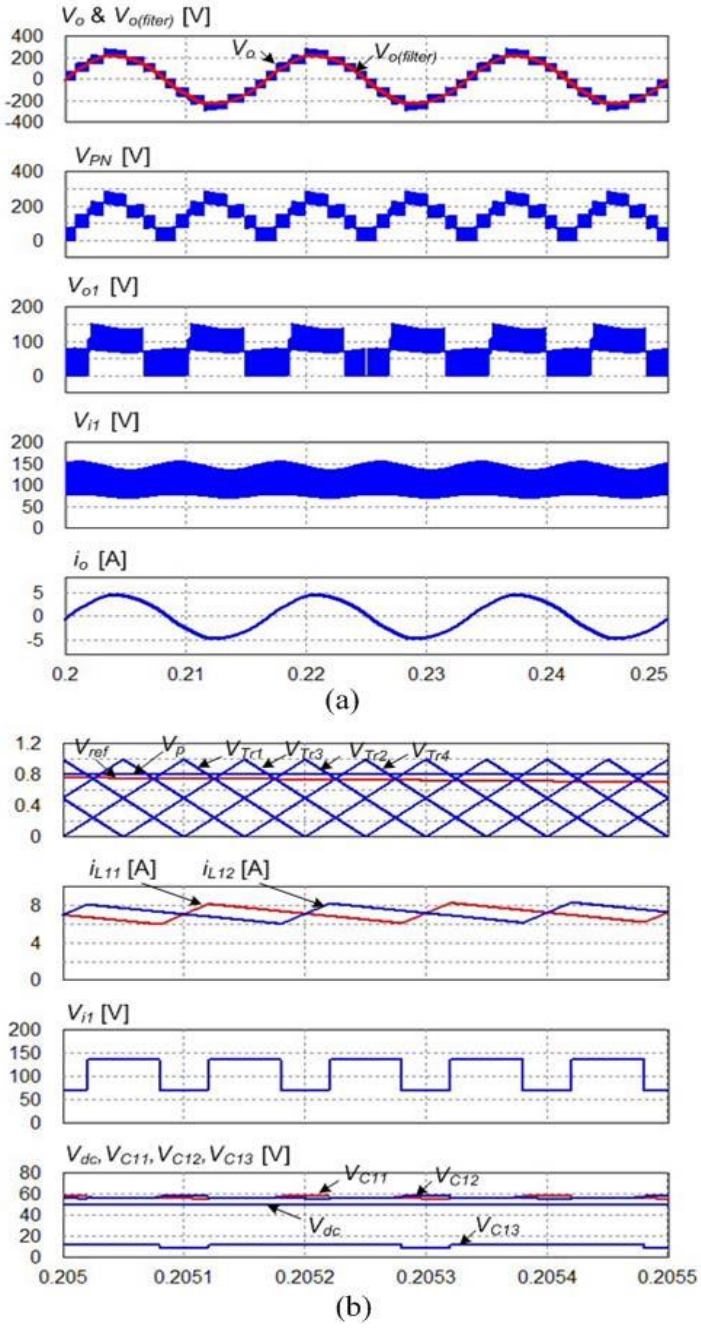

Figure 3.8: Simulation results M = 0.8 and D = 0.2

Altering the indices and the duty cycles, all other output variable are changed as showing in another simulation as diagramed.

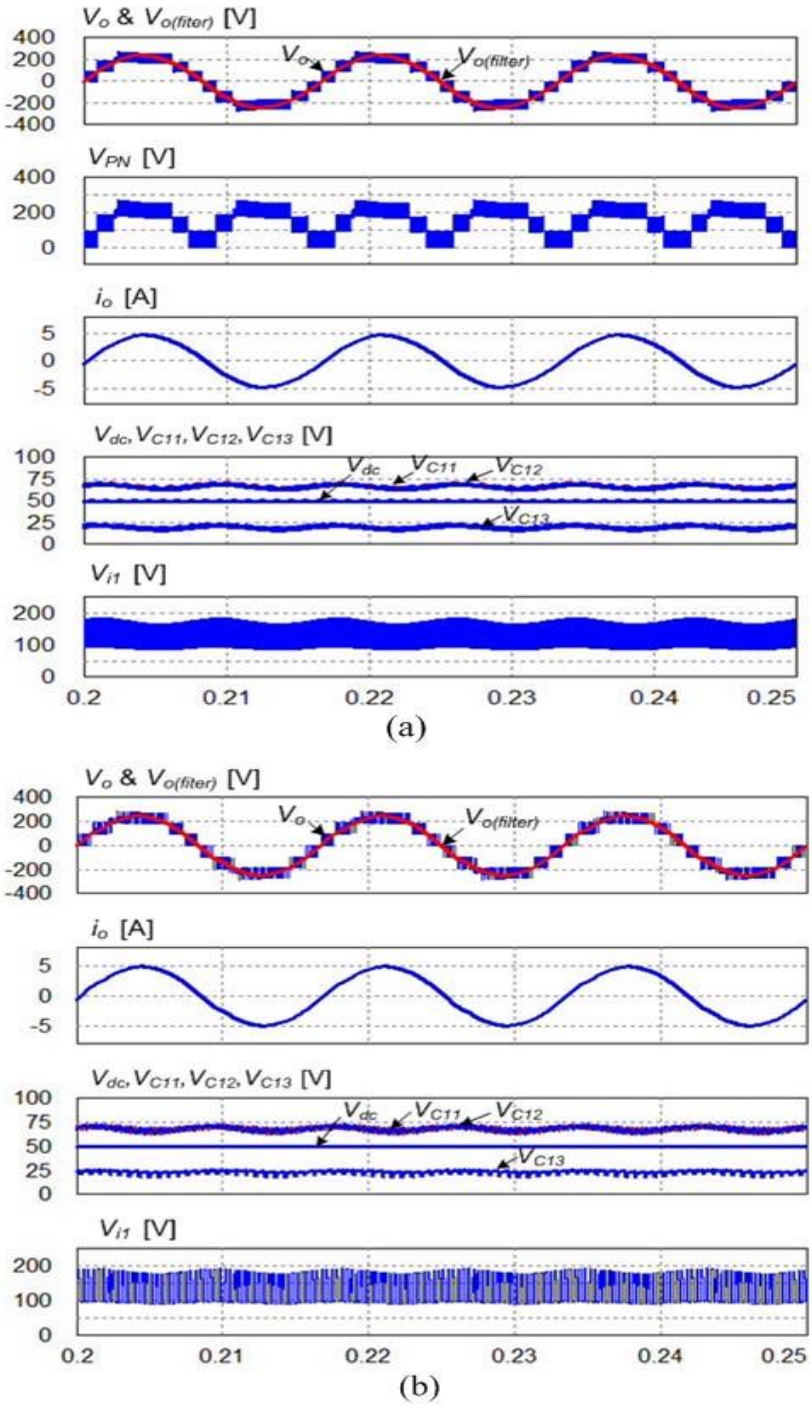

Figure3.9: Graphical results of the proposed inverter when M = 0.7, D = 0.25

The Figure 3.10 below is with modulation of 0.8 and duty circle of 0.2. The chart as simulated below.

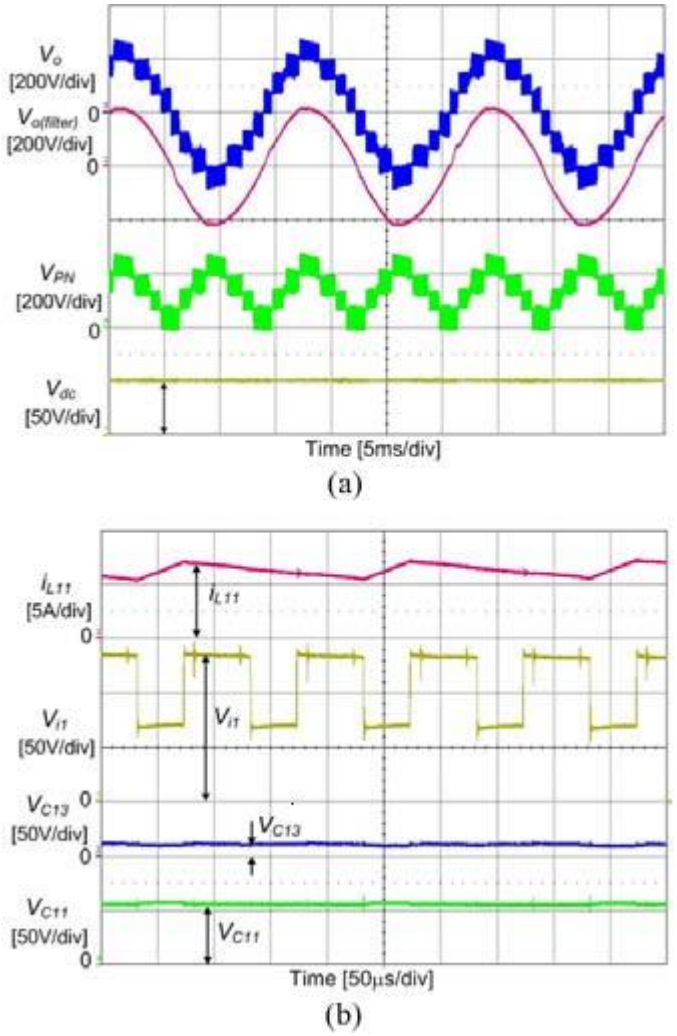

Figure. 3.10: Analyzed results on a Cascaded inverter M= 0.8, D= 0.2

This figure above has the same identity with figure 3.8 with same operating conditions.

In Figure 3.11, the experimental result is changed by reducing the Modulation to a reasonably value and the duty cycle is maintained.

From Fig. 13 (b), for the inductor currents at upper shoot state increase

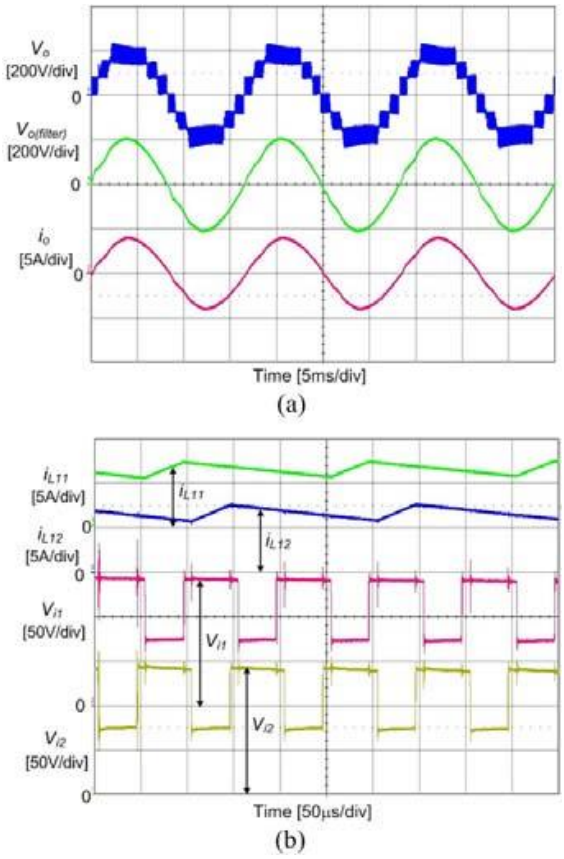

Figure 3.11: A cascaded inverter at M= 0.7, D= 0.2

The analyzed simulation is further adjusted by increasing D to 0.25 while maintaining M to 0.7. With this, the increased output voltage as observed in the figure 3.12 below:

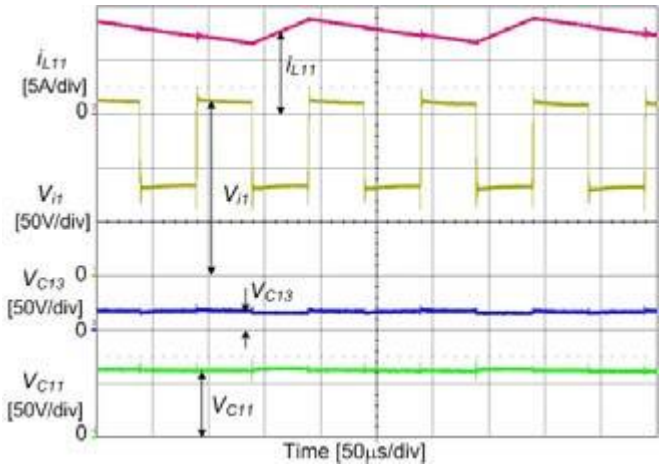

Figure 3.12: At M= 0.7, D= 0.25

The figure below express the characteristics associated with pulse width modulated expressing inverter at sequential order, operates at the lower stage and the upper stage during half switching time as can be observed at 60Hz. And in one switching cycle, the PWM patterns are symmetrical.

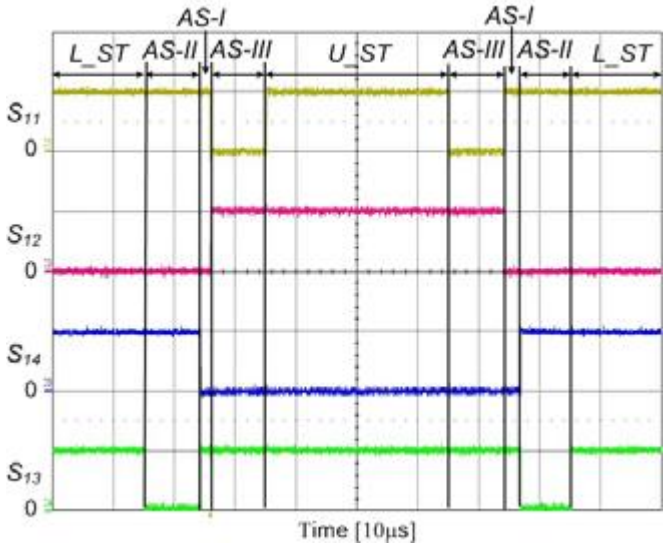

Figure 3.13: Switches variation with time of cell 1

The cascaded inverter changes when varied as illustrated below. The efficiency is between 85% and 92%

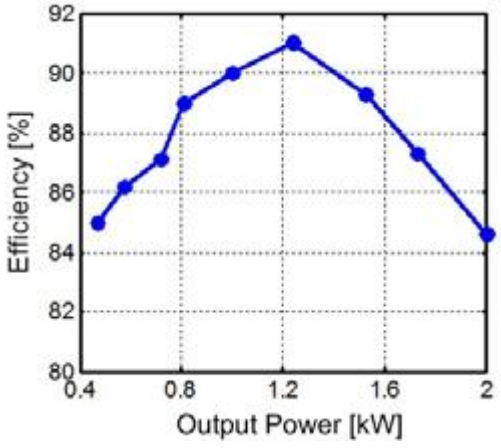

Figure 3.14: Efficiency against output power at M = 0.8 and D = 0.15

And figure 3.10 shows the analysis of modulation index of cascaded inverter expressed as:

Voltage gain = Vo/Vi (RMS)

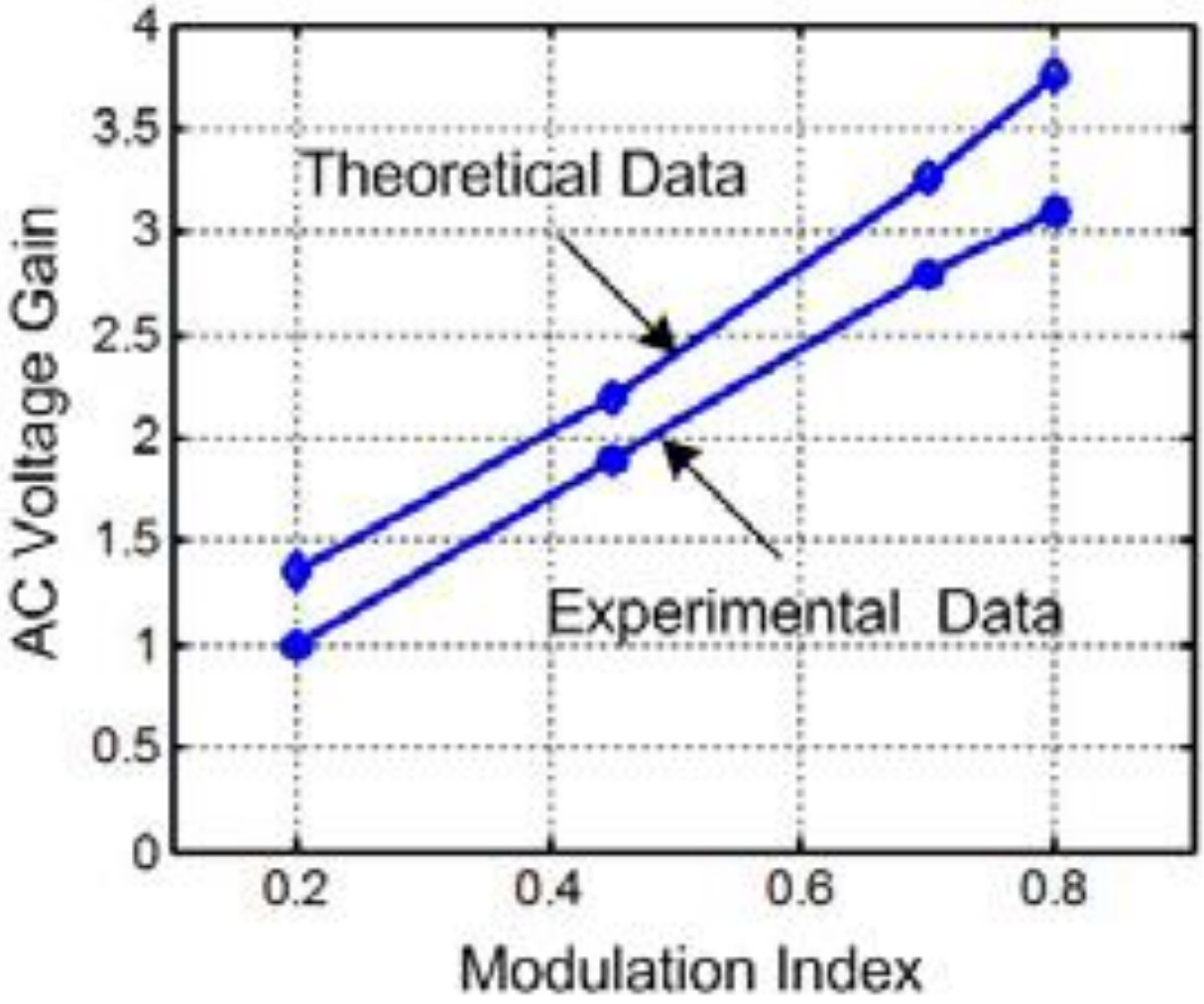

Figure 3.15: AC voltage gains against modulation index

Figure 3.15 gives the relationship that exist between the theoretical data collected and practical data. It is a variation of Ac voltage (gain) against modulation index. We observed that the theoretical analysis goes in line with experimental data. The modulation index increases as Ac voltage gain increases.

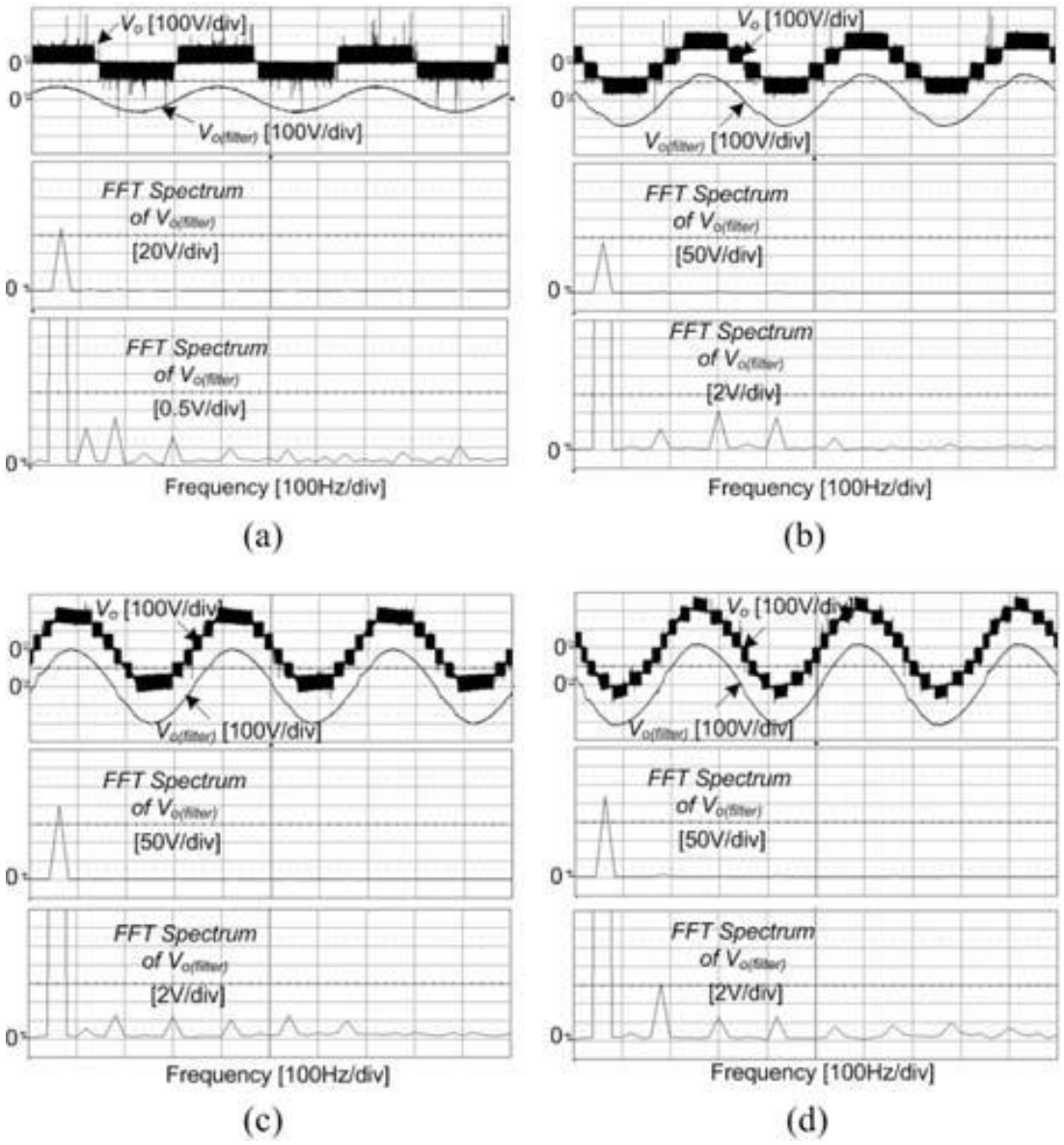

Figure 3.16: A Fast Fourier Transformer, FFT graph at various modulation.

And figure 3.17 express relationship between modulation indexes of a system and the Total Harmonic Distortion.

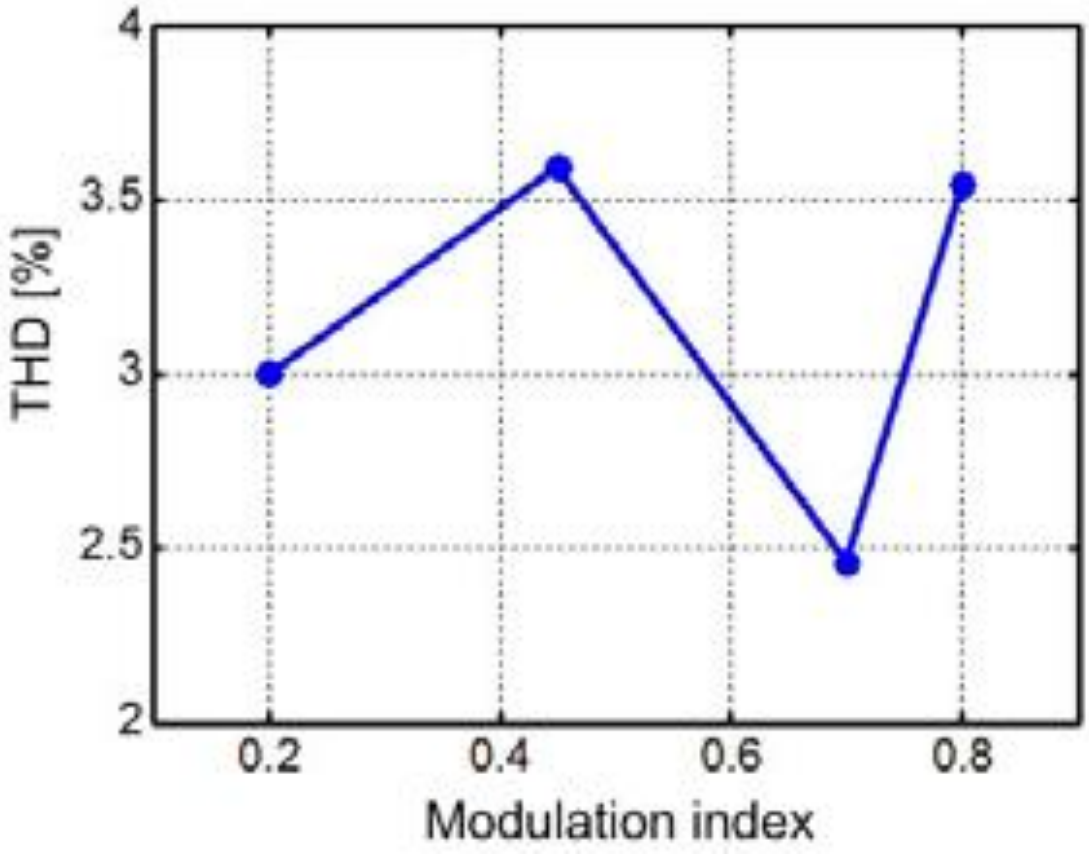

Figure 3.17: THD against Modulation index

CHAPTER 4

CONCLUSION AND RECOMMENDATION

4.1 Conclusion

This thesis has studied a topology for a better energy supply. It combines ideologies from earlier topologies to address current stress. This reduces the losses reasonably and the output voltage is raised up to 155Vrm from primary source of supply. The method provides easier applicability and the objectives are accomplished.

The working principles, the performance and analysis of high step-up voltage ratio under different operating conditions at steady state have been discussed. The achievement of the higher voltage conversion ratio with minimum voltage stresses across the active capacitors and diodes extremely low duty cycle as well as low level of on-state resistance leads to low voltage rating and low building cost of the inverter.

The output capacitor designed is to be very large to avoid over voltage. And output voltage derived successfully using the volt–second balance of the source in an inductor. In each case, different equivalent circuits and wave forms have been presented and outputs under the various condition have been reported appropriately. The output result obtained from the inverters comprises of voltages gains and duty ratios were tabulated and compared.

The simple structures and low rating of the components has made the inverter better for producing high energy conversion and equally easy to design and control. The importance of this studies also include the capabilities of the proposed inverter to generate low ripple current, minimum magnetization current and less inductor leakage current.

The high conversion ratio and the power quality of the inverter draw the attention to nowadays designs to frequently use the inverter especially in the renewable energy (photovoltaic and fuel cell) areas where the high demand of power is concernly required. Also at the industries, several equipment and machineries such as dc motors and so many modern technologies like electric vehicles as well as telecommunications equipment have to be powered!

With all these aforementioned applications, the inverter has some limitations that needs appropriate improvements which could have set some drawbacks that generally decreases the overall inverting efficiency and virtually increases the building cost. But these have been

worked upon as a result of reduced number of components used. Low duty cycle is used for better improvement. The problem of voltage stress was properly addressed and appropriately minimized. Finally, the inverter performed excellently well by generating higher efficiency. To prove the performance of the designed inverter the result was simulated using PSCAD software and both the design and theoretical results are relatively corresponded to each other and proved the higher voltage conversion ratio with extreme low duty cycle. In this regard, the major objectives of this research have been achieved perfectly.

4.2 Recommendations

The operation modes in this thesis covered only covered multilevel inverters and modes of operations. . A future research objective from this work is to design inverter topology that would have a steady output parameters and can operate in dynamic period which will not be affected by voltage, current unbalance. To have this steady state, the size of capacitors have to be increased likewise the inductor coil be increased in turn from the practical point of view. Moreover, I also think of designing the same inverter with the same topology but with higher steps like nine level topology. I am sure this will produce better quality energy, higher power and very low harmonics.

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APPENDICES

APPENDIX 1

ETHICAL CONTRACT FORM

YAKIN DOĞU ÜNİVERSİTESİ

ETHICAL APROVAL DOCUMENT

Date: 15/01/2020

To the **Graduate School of Applied Sciences**

The research project titled "..ANALYSIS OF QUASI Z-SOURCE BASED FIVE-LEVEL INVERTER....."
has been evaluated. Since the researcher(s) will not collect primary data from humans, animals, plants or earth, this project does not need to go through the ethics committee.

Title: ANALYSIS OF QUASI Z-SOURCE BASED FIVE LEVEL INVERTER

Name Surname: Prof. Dr. Ebrahim Babaei

Signature:

Role in the Research Project: Supervisor

Title:

Name Surname:

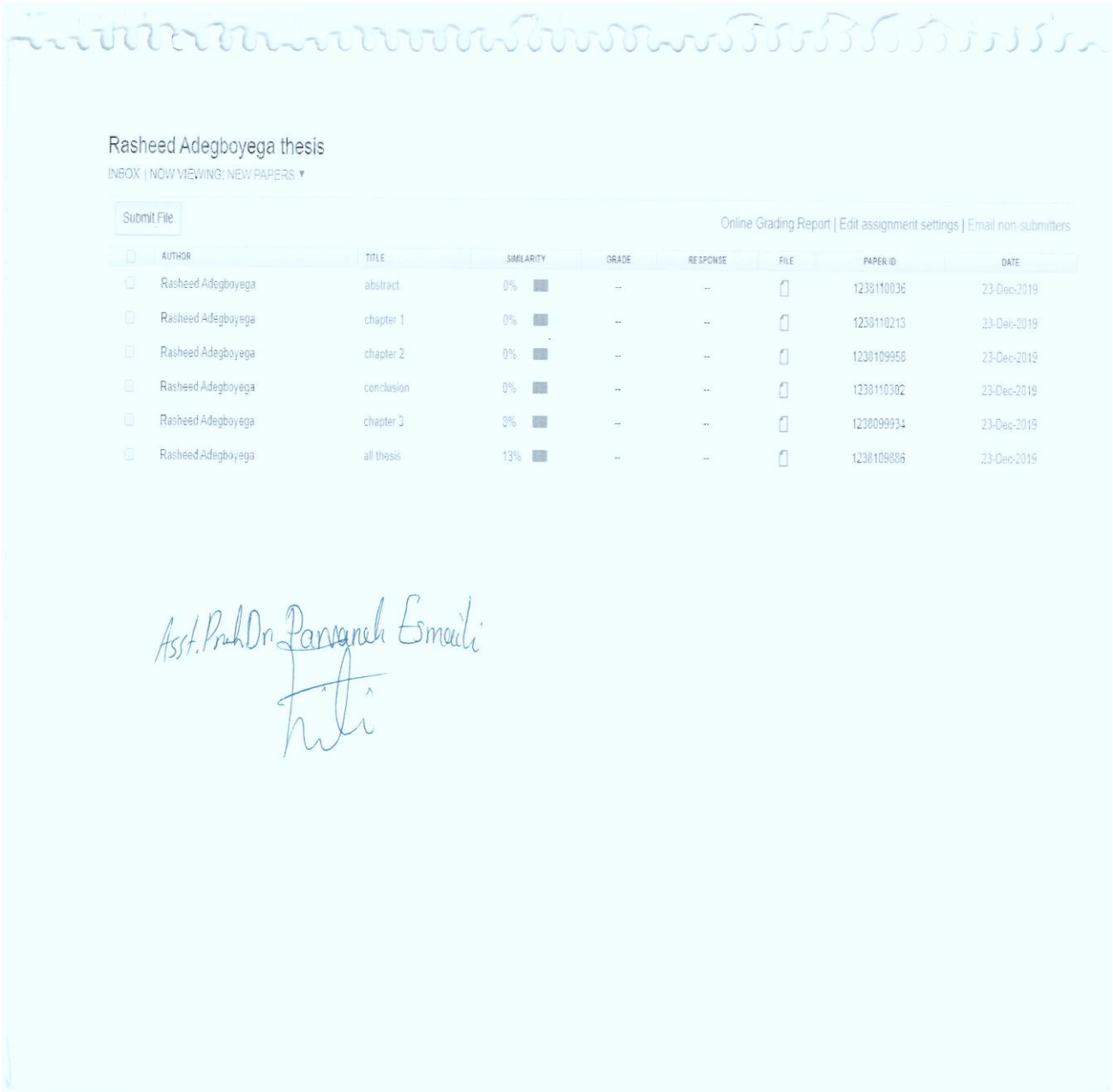
Signature:

Role in the Research Project: Co-Supervisor

APPEDIX 2

SIMILARITY REPORT

SIMILARITY 1 (Before Defense)



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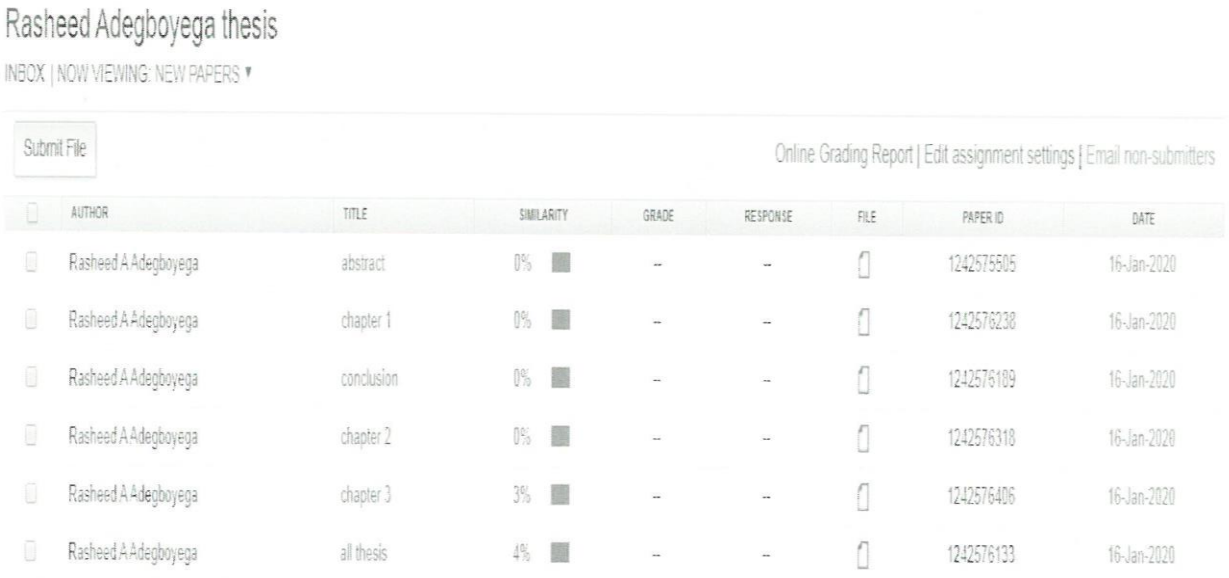

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