MORAD ALI KH ALMANSURI

A MULTIPLE-INPUT DC-DC CONVERTER TOPOLOGY

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A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

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In Partial Fulfilment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

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Approval of Director of Graduate School of Applied Sciences

Prof. Dr. Nadire Çavuş

We certify this thesis is satisfactory for the award of the degree of Master of Science in Electrical and Electronic Engineering

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Assist. Prof. Dr. Lida Ebrahimi Vafaei	Department of Alternative Energy Resources Technology, NEU

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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Signature:

Date: 23.01.2021

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My endless appreciation to my siblings who despite their distance have always been a source of empowerment and strength for me. Also, to my closest and dearest friends.

To my parents…

ABSTRACT

A novel hybrid multi-input dc-dc converter topology is presented in this research. The presented topology has hybrid energy conversion capabilities thereby diversifying the converters input voltage sources to a variety of energy sources. There are no restrictions to input voltage sources with varying current-voltage characteristics. All these properties are achieved with minimum component number and bidirectional capabilities. When compared to previous multi-input buck-boost converter, the presented topology has the following advantages; transformers are not required to produce positive output voltages, bidirectional capabilities and independent operation in the various categories of buck-boost.

Keywords: Multi-input dc-dc converter; bidirectional; buck; boost and buck-boost.

ÖZET

Bu araştırmada yeni bir hibrit çok girişli dc-dc dönüştürücü topolojisi sunulmuştur. Sunulan topoloji, hibrit enerji dönüştürme yeteneklerine sahiptir, bu nedenle dönüştürücülerin giriş voltaj kaynaklarını çeşitli enerji kaynaklarına çeşitlendirir. Değişken akım-voltaj özelliklerine sahip giriş voltaj kaynakları için herhangi bir kısıtlama yoktur. Tüm bu özellikler, minimum parça sayısı ve çift yönlü yeteneklerle elde edilir. Önceki çok girişli buck-boost dönüştürücü ile karşılaştırıldığında, sunulan topoloji aşağıdaki avantajlara sahiptir; Transformatörlerin, çeşitli buck-boost kategorilerinde pozitif çıkış voltajları, çift yönlü yetenekler ve bağımsız çalışma üretmesi gerekli değildir.

Anahtar Kelimeler: çok girişli dc-dc dönüştürücü; çift yönlü; buck; boost ve buck-boost.

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LIST OF ABBREVIATIONS

DC:	Direct Current
HVDC:	High Voltage Direct Current
MIC:	Multi-Input Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
CCM:	Continuous Conduction Mode
DCM:	Discontinues Conduction Mode
PSCAD:	Power Systems Computer Aided Design

CHAPTER 1
INTRODUCTION

1.1 Overview

The use of power electronic converters in the last decade has witnessed rapid increase and this can largely be attributed to the major improvements that have been chalked in the power electronics based industry. These various converters now come with minimum size, less weight, less cost, higher efficiency and are more reliability. The term converters is a broad name which is used to classify all the various topologies of power electronic converters. Basically converters are semiconductor based devices which are used in conditioning or altering the state of power to some more desirable characteristics.

DC-DC converters are the simplest topologies of power electronics converters. They are widely used in almost all electronics systems and high power systems such as electric vehicles, HVDC, wielding and plating systems etc. By connecting a transformer to the DC-DC converter, it can be used as an isolating system. A variety of DC-Dc topologies exist; the commonest topologies are the buck topology, boost topology and buck-boost topology; these classes of converters are differentiated based on the relationship between the input voltage and the output voltage. These common topologies have less number of components especially the semiconductor switches and. They mostly have one or two switches. On the other hand, there are complex DC-DC topologies where the quantity of switches increases and the general topology is complex. In other to minimize the switching losses, application of resonant techniques or soft switching techniques are employed.

The buck converter of the DC-DC topology is able to provide an output voltage with magnitude less than the magnitude of the input voltage whiles the boost converter topology of the DC-DC converter has the capabilities to generate output voltages with magnitude always greater than the magnitude of the input voltage. The buck topology is also referred to as step-down converter whiles step-up converter is used describe the boost topology. Figure 1.1 shows the general buck

converter; the structure is composed of four main components, one switch, one inductor, one capacitor and one diode. The buck-boost topology combines the characteristics of the buck and the boost topology; it able to generate output voltage with magnitude greater than, equal to or less than the magnitude of the input voltage.

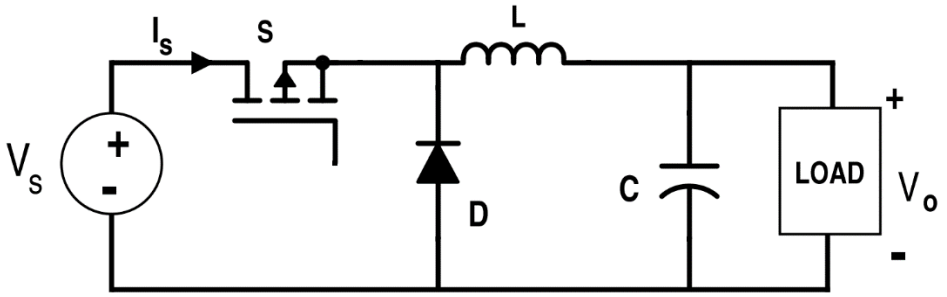

Figure 1.1: Buck converter

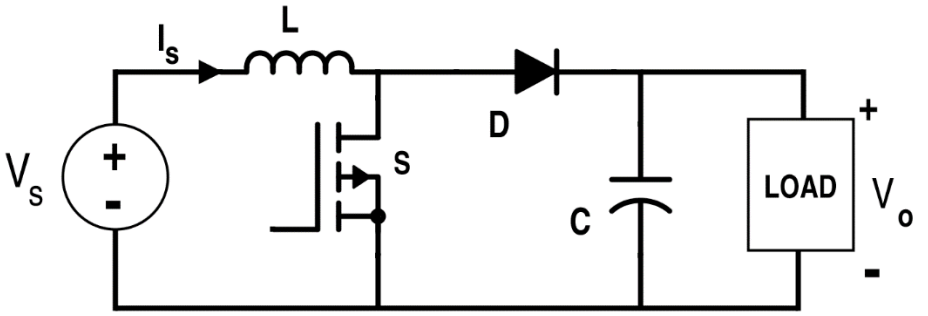

Figure 1.2: Boost converter

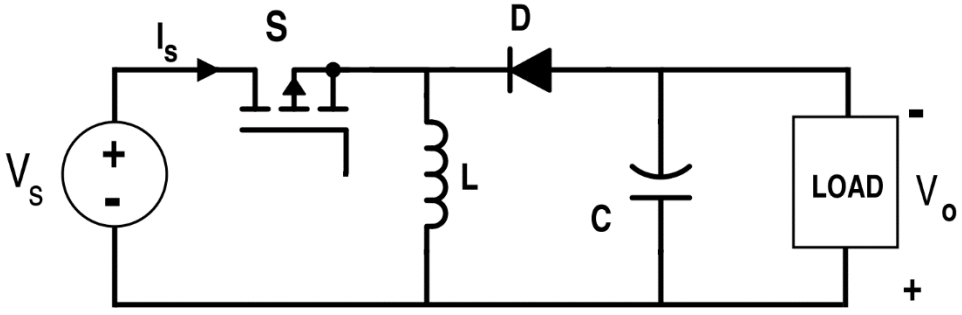

Figure 1.3: Buck-Boost converter

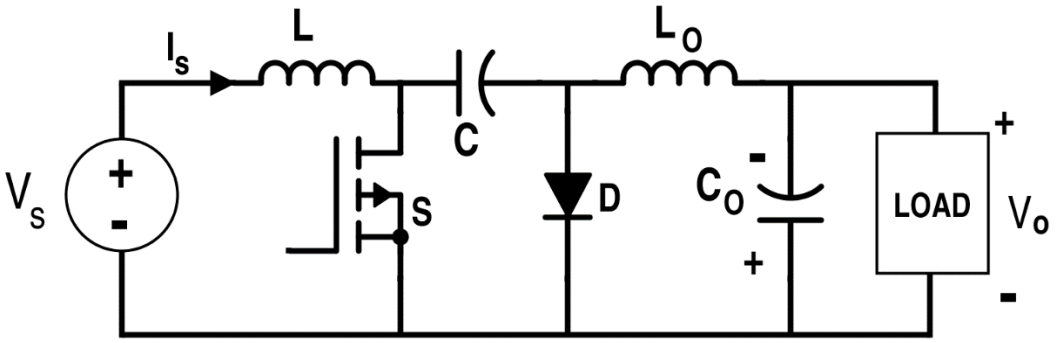

Figure 1.4: Cuk converter

The structure of the boost topology is shown by Figure 1.2. The component count is the same as that of the buck topology, the only difference is the position of the switch and inductor. Similarly, the buck-boost topology has the same component count when compared to the two previous structures; buck and boost topologies. The Cuk converter is another type common DC-DC converter which has buck-boost functionality.

Multi-input based systems especially converters have the capabilities to harness energy from multi sources. They make use of multiple energy sources hence are able to combine the merits of these various sources such as PV systems, wind energy, batteries, capacitor based sources, fuel cells etc. multi-input converters have received a lot of research of the past three decades and they are very suitable for use in microgrids, grid connected systems, telecommunication systems, uninterrupted power supplies etc. Several multi-input systems are able to combine voltages with different features characteristics as the source of converters, some examples of such useful topologies can be found in (Matsuo et al., 2004; Montali, 2010; Solero et al., 2005, 1996). These topologies however have some limitations; multiple energy supply from the source to load is not possible, one source is able to provide power to the load at one time, concurrent power supply is not possible, this is done in other to prevent the effects of power coupling. The solutions to these limitations are provided in (Di Napoli et al., 2002).

In the case of current source multi-input converters, concurrent supply of power from the source to the load is permissible and this achieved by the connection of transformer (multi winding type). Although this topology provides useful application of the multi-input system, the structure of the converter is bulky and very expensive because of the use of two inductances in each topology of the parallel connection. Multi-input DC-DC topology with buck-boost functionality, the component count in this topology is less however the output voltage has a negative reference. Reversing of the output will require the application of a transformer which increases the cost and size of the topology. Also it's unable to provide bidirectional path for the current hence extra converters are needed to perform this function. Application of multi-input converters provide efficient applications of varied power sources especially renewable energy; these converters are not limited to specific locations by virtue of the type of energy source, they can easily be utilized in locations with more solar irradiations and can adapt easily to locations with cheaper utility. An example of a multi-input DC-DC converter is shown in Figure 1.4. This topology is an illustration of the way multiple power source sources can be used in feeding a DC-DC converter.

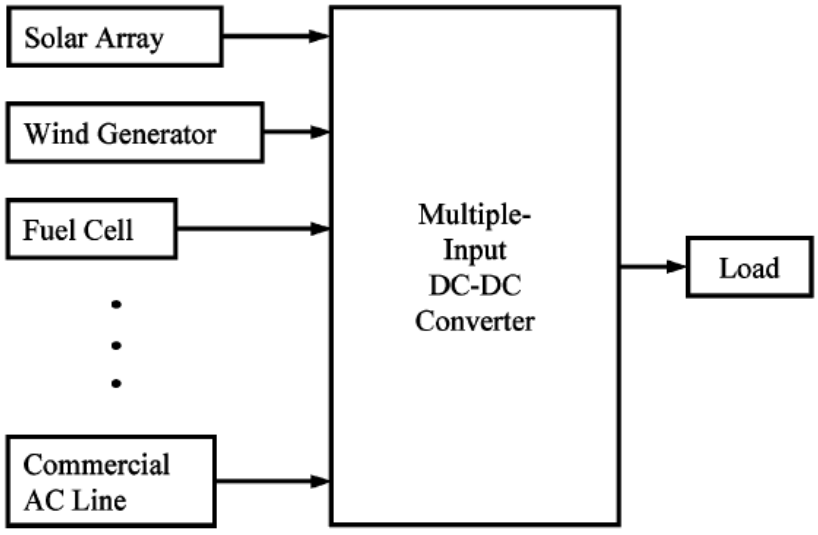

Figure 1.5: Illustration of multi-input dc-dc converter

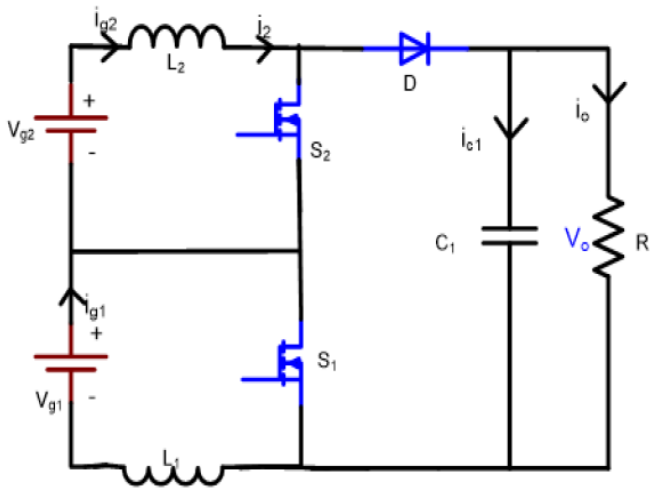

Figure 1.6: Multi-input integrated converter

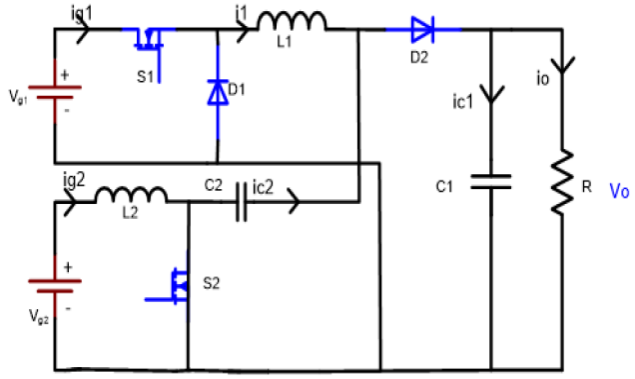

Figure 1.7: Multi-input septic converter

1.2 Thesis Problem

Single input converters are good and efficient but have limitations to the kind of power they accept at the input or source. If the characteristics of the input voltage for which they were designed for changes, the converter will not be able to function as desired. Hence they are not suitable for multi-source functions. Multi-input converters with unidirectional power flow also have limitations; they cannot provide bidirectional power flow, power is only transferred from the source to load but cannot be flowed from the load to the source in cases of regeneration, this

causes power loss which leads to increased cost and reduced efficiency. Finally, converters without buck-boost functionality require extra converters to achieve the functions of buck-boost hence the cost of the system increases and the efficiency reduces.

1.3 The Aim of the Thesis

The goal of this thesis is to design a converter capable of resolving the above numerated problems. A multi-input converter is proposed, this converter has the ability to function with different input sources this leads to application of multi renewable energy sources which leads to improving the environments. The proposed converter accepts multi-input power sources with different characteristics of voltage and current. The proposed converter also provides multi or bidirectional power flow from the source to the load and vice versa. Buck-boost mode or functionality is provided by the proposed converter; also transformers are not required in generating positive voltage at the output.

1.4 The Importance of the Thesis

The proposed converter performs the functions of multiple converters hence the importance of the proposed topology can be summarised below as:

- Minimum converter or system cost
- Reduced converter losses
- Maximum converter efficiency
- Less component count
- Less space required for the converter
- Mobility functionality irrespective of the power characteristics

1.5 Limitation of Study

This research investigation was successfully done with the barest or minimum limitation. The major limitations of this research is that only simulation of the proposed topology can be done due to the absence of a well-equipped or standard laboratory facility where

experimental results can be generated in other to validate the simulation outputs, nevertheless PSCAD software provides the minimum differences between simulation output and experimental outputs.

1.6 Overview of the Thesis

The body of the thesis is segmented into the following categories:

Chapter 1: Introduction, Thesis Problem, Aim of the Thesis, The importance of the Thesis, Overview of the Thesis.

Chapter 2: Literature Review of DC-DC Converters

Chapter 3: Proposed Topology and Simulation Results

Chapter 4: Conclusion and Recommendation

CHAPTER 2
DC-DC CONVERTER REVIEW

2.1 Introduction

DC-DC converters have long been in existence and are considered as the pioneer and simplest power electronic conditioning device. They are used in almost all spheres of human life such as power supply systems, communication establishments, military, academia, health services, transportation systems (air, sea and land) and electronic devices (mobile phones, laptops and computers) and wielding and plating. DC-DC converters can also be utilized as an isolation device when a transformer coupled to the converter (Forsyth & Mollov, 1998). Classification of DC-DC converters is shown by Figure 2.1 where Linear, hard switching and Soft switching modes forms the initial stage of categorization. The most common topologies can be found under hard switching mode which is constituted by isolated and non-isolated topologies. A review of selected DC-DC converter topologies with emphasis on isolated and no-isolated topologies will be carried out this chapter. The selected topologies for review are:

- Buck topology
- Boost topology
- Buck-Boost Topology
- Cuk Topology
- Multi-input Topology

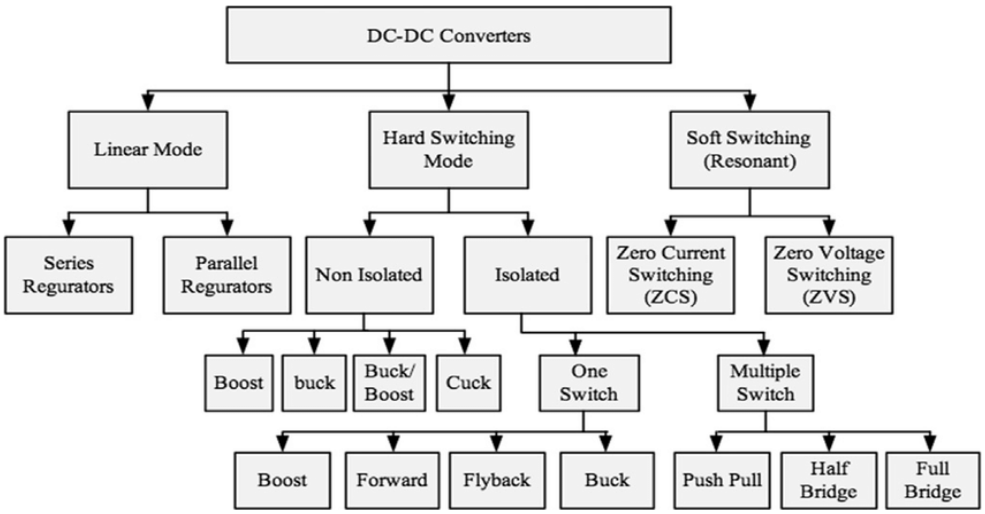

Figure 2.1: DC-DC converter classification

2.2 Buck DC-DC Topology

The buck dc-dc converter is illustrated by Figure 2.2. This topology of dc–dc converter has this main characteristic where the magnitude of the output voltage always being less than the value of magnitude of the input voltage. This is because the switching architecture (diode and power switch) cuts (chops) the input voltage Vi. This is why this topology of converter is also referred to as a chopper. It is also known as a stepdown dc-dc converter. The power circuit of the buck converter is made up of six components namely source voltage **Vi**, diode, the semiconductor switch **S** (let's assume MOSFET), and inductor **L**, a capacitor (filter) **C** and the load is represented by $\mathbf{R_L}$. the diode is given a multiple of nomenclature such as:

a. Catch diode

b. Flywheel diode

c. Freewheeling diode

PWM control technique is used in operating the power switch for the turn-on and turn-off states by virtue of the switching frequency f_s and duty cycle D which are represented by equations (2.1-2.4). Two states of power switch control exist and these are ***on-state*** represented by Figure 2.3 and ***off-state*** represented by Figure 2.4.

$$f_s = \frac{1}{T_s} \tag{2.1}$$

$$D = \frac{t_{on}}{T} \tag{2.2}$$

$$D = \frac{t_{on}}{t_{on}+t_{off}} \tag{2.3}$$

$$D = f_s t_{on} \tag{2.4}$$

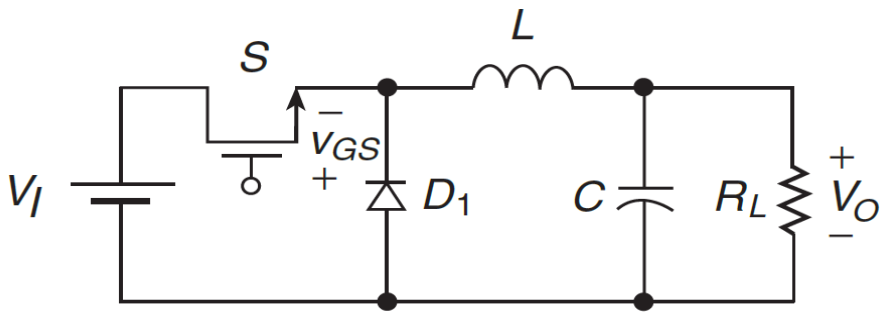

Figure 2.2: Buck DC-DC converter

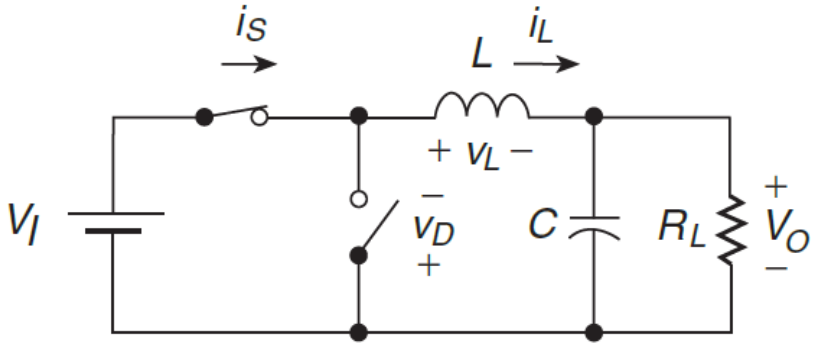

Figure 2.3: On-state

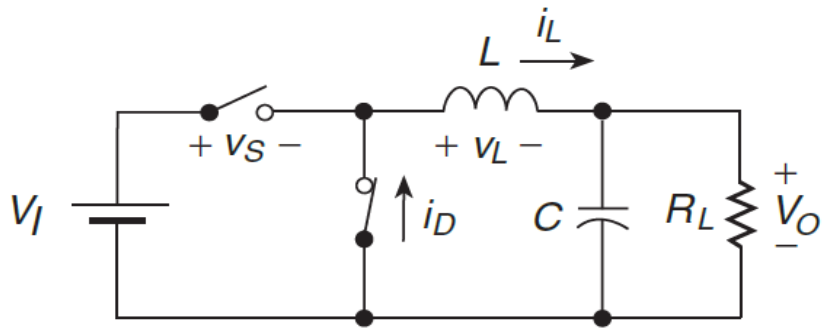

Figure 2.4: Off-state

The converter as a whole has two modes of operation CCM (continues conduction mode) and DCM (Discontinues conduction mode). These two modes are differentiated by the period of conduction of the inductor current. The inductor current conducts for the complete cycle whiles during the CCM state whiles the inductor current only conducts for a period of the cycle and terminates at zero f or a period of time in the DCM state. The boundary of operation for the DCM and CCM is referred to as critical mode.

Referring to Figure 2.3, that is when the switch is closed or the switch is on-state mode, the diode is reversed biased and the inductor current is equivalent to the switch current. The following mathematical expressions are developed for this mode specifically for CCM:

The diode voltage v_D is given by:

$$v_D = -V_i \tag{2.5}$$

The inductor voltage v_L and inductor current i_L are given below where V_o is the output voltage

$$v_L = V_i - V_o \tag{2.6}$$

$$i_{L\,(slope)} = \frac{V_i - V_o}{L} \tag{2.7}$$

$$i_L = i_S \tag{2.8}$$

The output waveforms for this period of conduction from 0 to DT are shown by Figure 2.5 and during this period the inductor, capacitor and load receives energy from the dc voltage source,

the second state which is the ***off-state*** starts by turning off the power switch at time DT. When the switch is off, the inductor current is given by:

$$i_{L(slope)} = \frac{-V_o}{L} \tag{2.9}$$

$$v_L = -V_o \tag{2.10}$$

$$v_s = V_i \tag{2.11}$$

$$i_D = -\frac{V_o}{L}(t - DT) + i_L(DT) \tag{2.12}$$

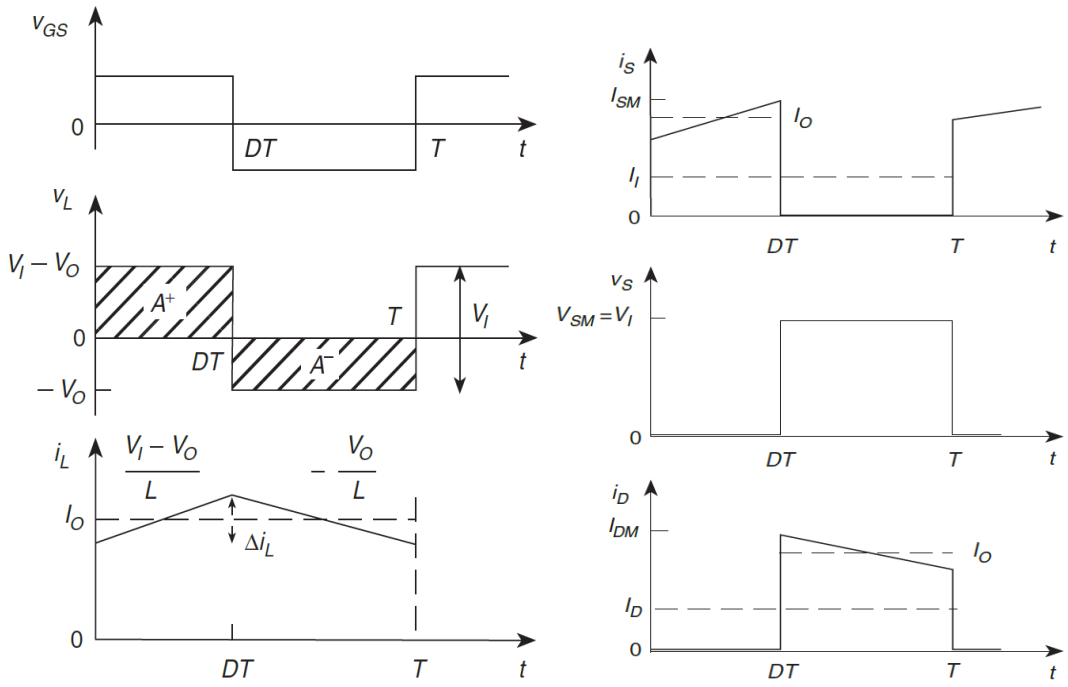

Figure 2.5: Output waveforms (Varesi et al., 2017)

Figure 2.6 shows the critical mode for the period $0 < t \leq DT$ and its expressed by the expression below:

$$i_L = t\frac{V_i - V_o}{L} \tag{2.13}$$

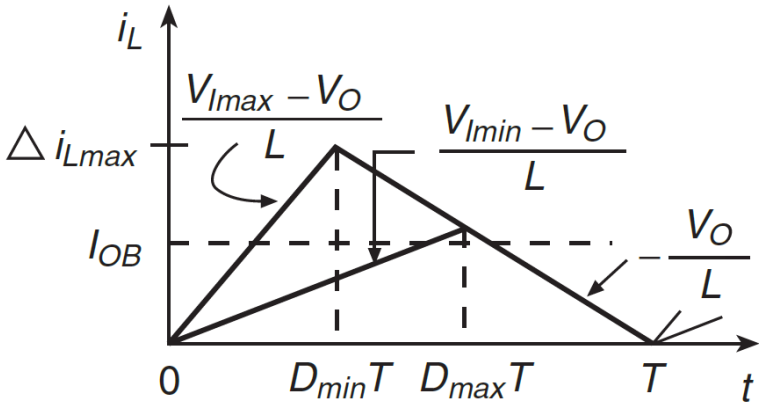

Figure 2.6: Critical mode for CCM buck converter

The CCM state maximum stress on the diode and power switch for current (I_{Smax}) and voltage (V_{Smax}) are expressed below where I_{omax} is the maximum output current and V_{imax} is the maximum input current.

$$I_{Smax} = \frac{(1-D_{min})V_o}{2f_sL} I_{omax} \tag{2.14}$$

$$V_{smax} = V_{imax} \tag{2.15}$$

The buck converter circuit with parasitic components are illustrated by Figure 2.7. These parasitic components are defined below as:

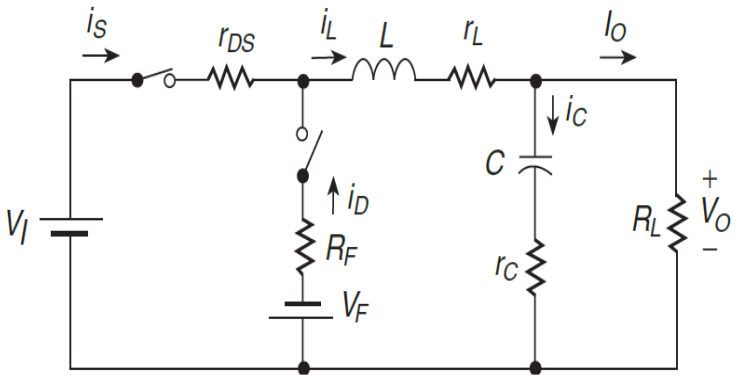

Figure 2.7: Buck converter with parasitic components

r_{ds} = On resistance of power switch (MOSFET)

R_F = Forward resistance the diode

V_F = Threshold voltage of the diode

r_L = Inductor ESR (equivalent series resistance)

r_C = Capacitor ESR (equivalent series resistance)

The converter power losses and efficiency are expressed below assuming the transistor has a linear output capacitance C_o. therefore the switching power loss P_{SPL} and maximum switching power loss $P_{SPL(max)}$ are given by:

$$P_{SPL} = C_o f_s V_I^2 \tag{2.16}$$

$$P_{SPL(\max)} = C_O f_s V_{i(\max)}^2 \tag{2.17}$$

R_F power loss is given by:

$$P_{RF} = R_F I_{Drms}^2 \tag{2.18}$$

V_F power loss is given by:

$$P_{VF} = V_F I_D \tag{2.19}$$

The total conduction loss of the diode is given by:

$$P_D = P_{RF} + P_{VF} \tag{2.20}$$

r_L power loss and maximum power loss are given by:

$$P_{rL} = r_L I_{Lrms}^2 \tag{2.21}$$

$$P_{rLmax} = r_L I_{omax}^2 \tag{2.22}$$

r_C power loss and maximum power loss are given by:

$$P_{rC} = r_C I_{Crms}^2 \tag{2.23}$$

$$P_{rCmax} = \frac{1}{12} r_C \Delta i_{Lmax} \tag{2.24}$$

MOSFET conduction power loss P_{MOSFET} is given by:

$$P_{MOSFET} = r_{DS} I_{Srms}^2 \tag{2.25}$$

Therefore, the total power loss of the converter is given by:

$$P_{TOTAL} = P_{rC} + P_{MOSFET} + P_{rL} + P_{SPL} + P_D \tag{2.26}$$

Hence the converter efficiency is given by:

$$Efficiency\ \eta = \frac{Power\ output\ P_o}{Power\ input\ P_i} = \frac{P_o}{P_o + P_{TOTAL}} \tag{2.27}$$

Analysis of the converter during the discontinuous conduction mode is given below. There are three states of operations in the DCM state which are represented by Figure 2.8 to Figure 2.11. Figure 2.8 is the power circuit, Figure 2.9 shows the first state when the semiconductor switch is conducting (ON) whiles the diode is reverse biased (OFF). Figure 2.10 shows the reverse state

of Figure 2.9, the diode forward biased whiles the semiconductor switch is non-conducting. Finally, in the last state, both the diode and the switch are not conducting.

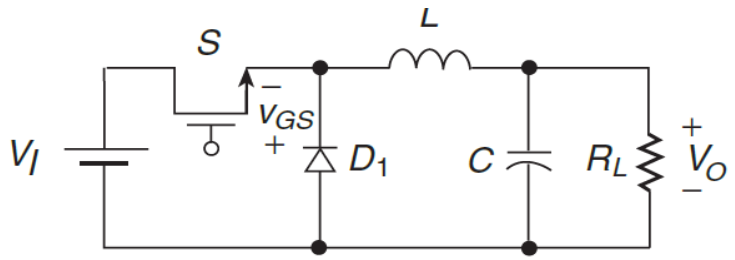

Figure 2.8: Power circuit

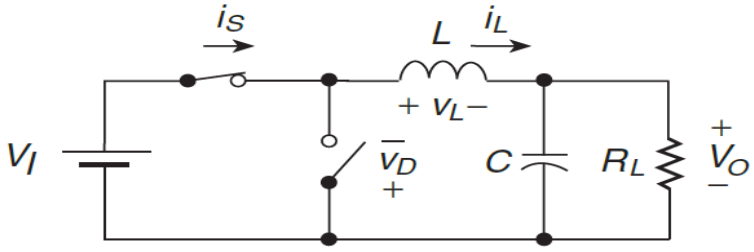

Figure 2.9: DCM first state

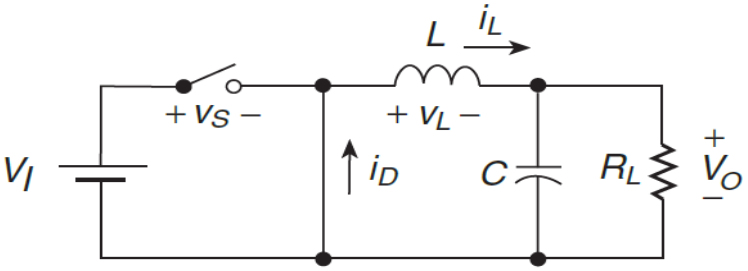

Figure 2.10: DCM second state

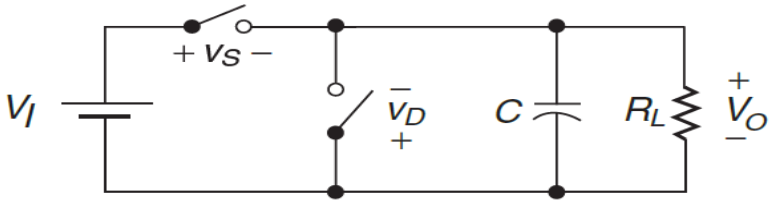

Figure 2.11: DCM third state

These three states of DCM operation are given below in terms of the period of conduction of the various waveforms.

- State 1: $0 < t \leq DT$
- State 2: $DT < t \leq (D + D_1)T$
- State 3: $(D + D_1)T < t \leq T$

The voltage and current waveform for these periods are shown below

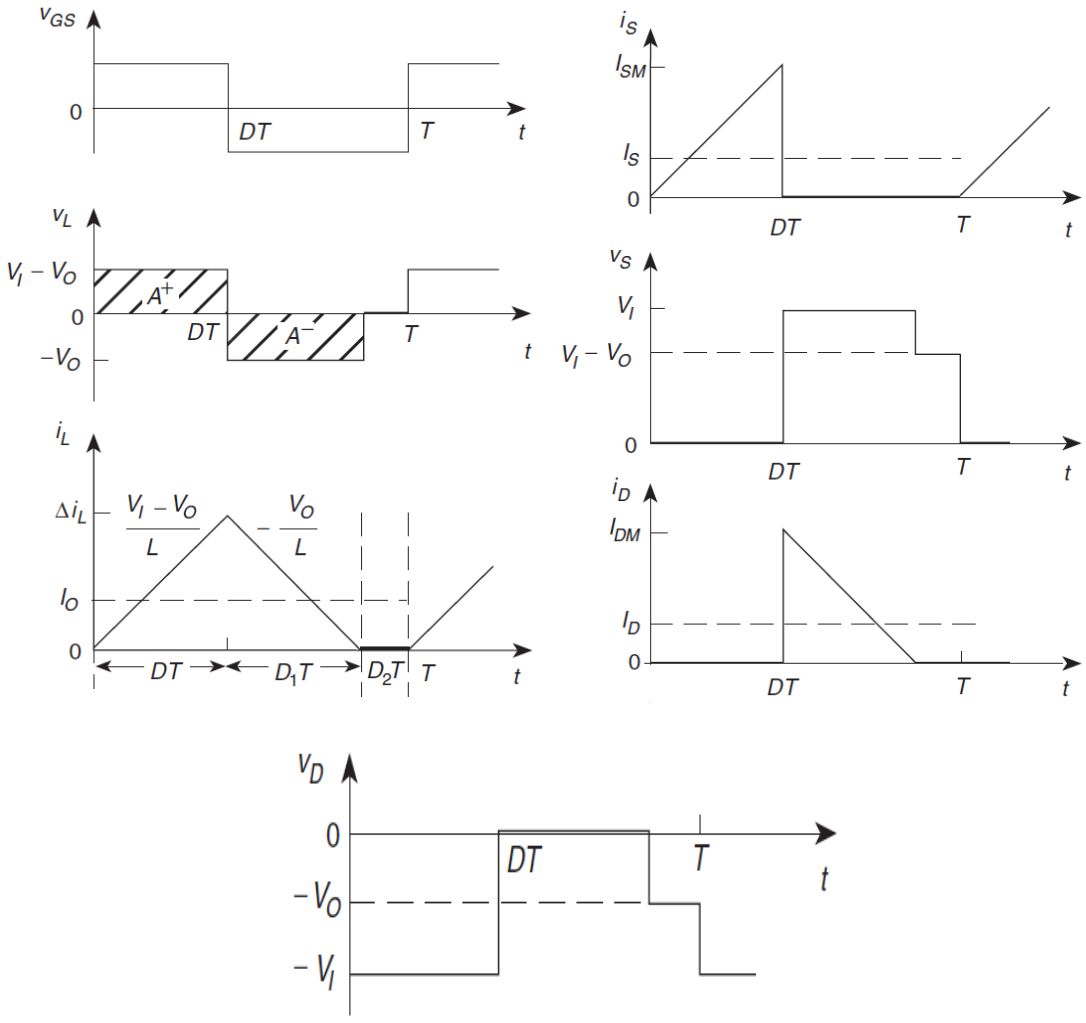

Figure 2.12: Output waveforms

The following expressions are developed in the first state for the time inverter $0 < t \leq DT$:

$$v_L = V_i - V_O \tag{2.28}$$

$$V_D = -V_i \tag{2.29}$$

$$i_L = i_s = t\frac{V_i - V_o}{L} \tag{2.30}$$

The following expressions are developed in the second state for the time inverter $DT < t \leq (D + D_1)T$:

$$v_L = L\frac{di_L}{dt} = -V_O \tag{2.31}$$

$$i_L = i_D \tag{2.32}$$

$$V_i = V_{SM}(maximum\ switch\ voltage) \tag{2.33}$$

The following expressions are developed in the third state for the time inverter $(D + D_1)T < t \leq T$:

$$v_S = V_i - V_o \tag{2.34}$$

$$v_D = -V_o \tag{2.35}$$

The DCM state maximum stress on the diode and power switch for current (I_{Smax}) and voltage (V_{Smax}) are expressed below where I_{omax} is the maximum output current and V_{imax} is the maximum input current.

$$I_{Smax} = D_{min}\frac{(V_{Imax} - V_o)}{f_s L} \tag{2.36}$$

$$V_{smax} = V_{imax} \tag{2.37}$$

MOSFET conduction power loss P_{MOSFET} is given by:

$$P_{MOSFET} = r_{DS}I_{Srms}^2 \tag{2.38}$$

Switching power loss P_{SPL} and maximum switching power loss $P_{SPL(max)}$ are given by:

$$P_{SPL} = C_o f_s V_I^2 \tag{2.39}$$

$$P_{SPL(\max)} = C_O f_s V_{i(\max)}^2 \tag{2.40}$$

MOSFET total power loss

$$P_{MOSFET(TOTAL)} = P_{rDS} + \frac{P_{SPL}}{2} \tag{2.41}$$

R_F power loss is given by:

$$P_{RF} = R_F I_{Drms}^2 \tag{2.42}$$

$$I_D = I_o(1 - M_{VDC}) \tag{2.43}$$

V_F power loss is given by:

$$P_{VF} = V_F I_D \tag{2.44}$$

The total conduction loss of the diode is given by:

$$P_D = P_{RF} + P_{VF} \tag{2.45}$$

r_L power loss and maximum power loss are given by:

$$P_{rL} = r_L I_{Lrms}^2 \tag{2.46}$$

Therefore, the total power loss of the converter is given by:

$$P_{TOTAL} = P_{MOSFET} + P_{rL} + P_{SPL} + P_D \tag{2.47}$$

Hence the converter efficiency is given by:

$$Efficiency\ \eta = \frac{Power\ output\ P_o}{Power\ input\ P_i} = \frac{P_o}{P_o + P_{TOTAL}} \tag{2.48}$$

2.3 Boost DC-DC Converter Topology

The boost converter of DC-DC topology is shown by Figure 2.13. This topology of DC-DC converter has the main characteristic of input voltage source which is always less when compared to the magnitude of the output voltage during steady state operation of the converter; this is why the converter is referred to as Boost converter. Four components constitute this topology of converter, these are one diode, one semiconductor switch, one inductor and one capacitor (filter). Operation of the power switch depends on the switching frequency f_s and duty cycle D. The turn on time or period is given by t_{on}.

$$f_s = \frac{1}{T_s} \tag{2.49}$$

$$D = \frac{t_{on}}{T} \tag{2.50}$$

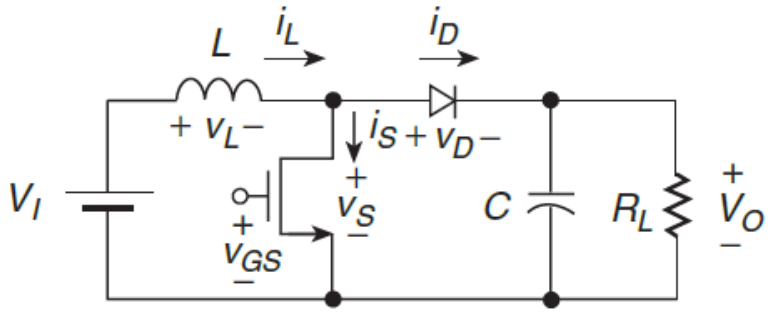

Figure 2.13: Boost DC-DC converter

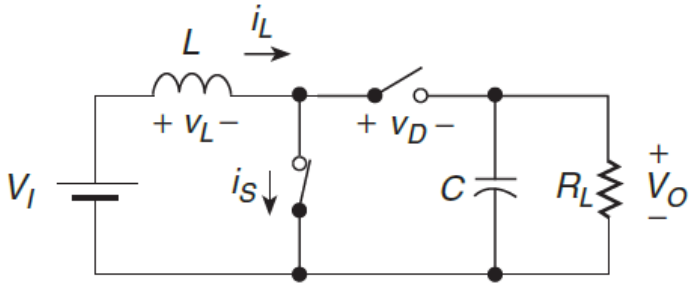

Figure 2.14: Equivalent circuit when switch is off

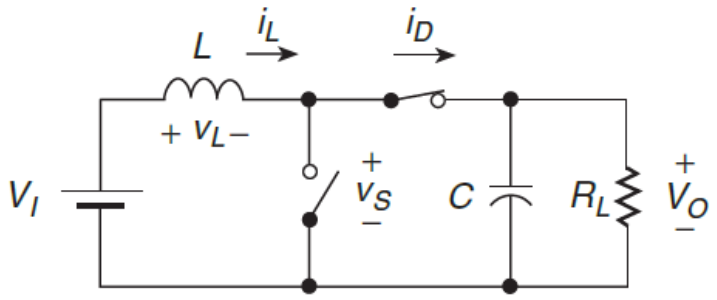

Figure 2.15: Equivalent circuit when diode is reverse biased

The boost converter can also be operated in two modes, the CCM (continuous conduction mode) and the DCM (discontinuous conduction mode) however, in the CCM mode, the converter cannot be operated when the load value is infinity (∞). Analysis of the boost topology in CCM mode is investigated using Figure 2.13 to Figure 15. The first state of the CCM mode is shown by Figure 2.14, where the switch conducts whiles the diode is reverse biased, this occurs during the period $0 < t \leq DT$. The following equations are developed for CCM state during the period of $0 < t \leq DT$ for the boost topology of DC-DC converter:

$$v_D = -V_O \tag{2.51}$$

$$v_L = V_i \tag{2.52}$$

$$v_L = L\frac{di_L}{dt} \tag{2.53}$$

$$i_L(slope) = \frac{V_i}{L} \tag{2.54}$$

$$i_s = i_L + \frac{V_i}{L} \tag{2.56}$$

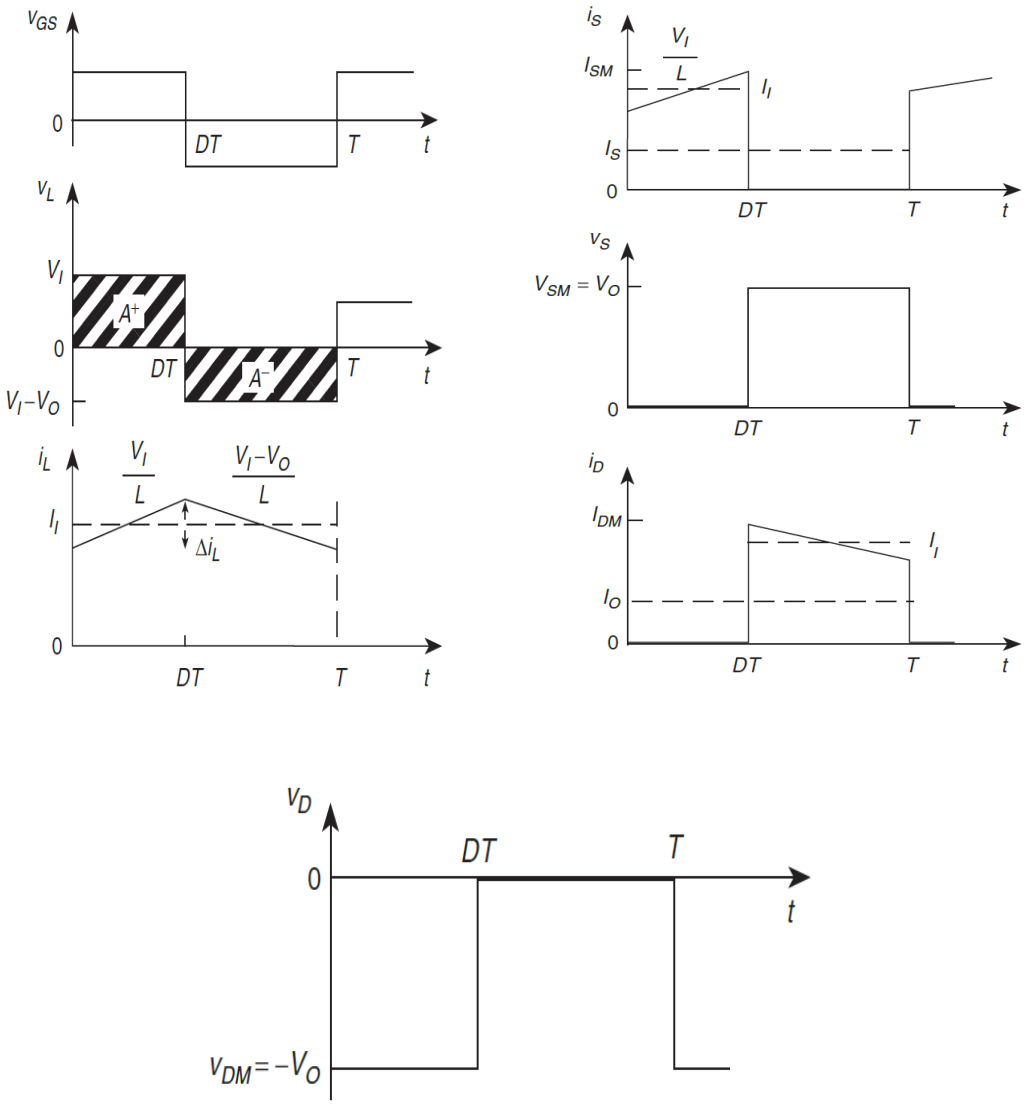

Figure 2.16: CCM state output waveforms

The following expressions are developed during the period $DT < t \leq T$ where the diode is forward biased and the switch is in non-conducting state. This period of converter mode is shown by Figure 2.16. The diode voltage and the switch current are both zero in this state and also the inductor releases the stored energy during this period.

The following expression are developed by analysing the circuit of Figure 2.16:

$$v_D = 0 \tag{2.57}$$

$$i_s = 0 \tag{2.58}$$

$$v_L = V_i - V_o \tag{2.59}$$

$$i_D = i_L(DT) + (t - DT)\frac{V_i - V_o}{L} \tag{2.60}$$

$$v_s = V_o \tag{2.61}$$

$$v_s = V_{SM} \tag{2.62}$$

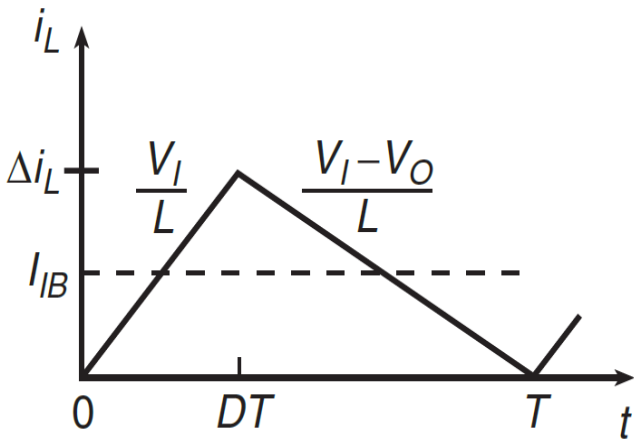

Figure 2.17: Critical mode for CCM boost converter

With parasitic elements, the power loss of the boost converter due to switching of Figure 2.17 is given by (2.63) where C_o is the capacitance at transistor output and P_o is the output power:

$$P_{SW} = P_O f_s C_o R_L \tag{2.63}$$

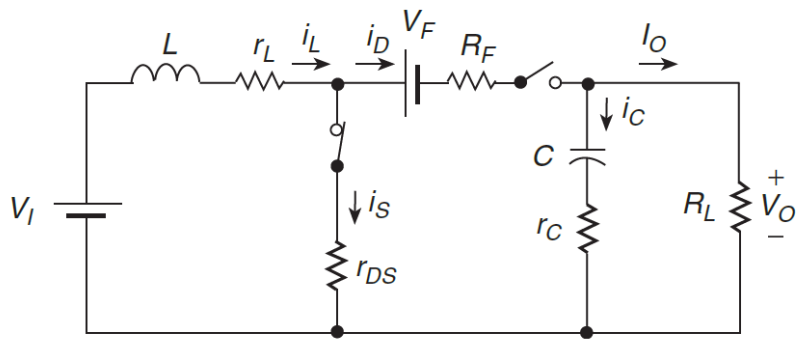

Figure 2.18: Boost converter with parasitic components

The conduction losses of the MOSFET switch is given by:

$$P_{MOSFET} = r_{DS} I_{Srms}^2 \tag{2.64}$$

The losses due to the capacitor:

$$P_{rc} = rC I_{Crms}^2 \tag{2.65}$$

The losses due to the inductor:

$$P_{rL} = r_L I_{Lrms}^2 \tag{2.66}$$

RF losses:

$$P_{RF} = R_F I_{Drms}^2 \tag{2.67}$$

Diode losses:

$$P_D = \frac{I_O^2 R_F}{1-D} I_o V_F \tag{2.68}$$

The total converter losses and efficiency are expressed by:

$$P_{TOTAL} = P_{MOSFET} + P_D + P_{RF} + P_{rC} + P_{SW} \tag{2.69}$$

$$\text{Efficiency } \eta = \frac{P_o}{P_o + P_{TOTAL}} \tag{2.70}$$

Analysis of the boost converter during the discontinuous conduction mode is given below. There are three states of operations in the DCM state which are represented by Figure 2.19 to Figure 2.22. Figure 2.19 is the power circuit; Figure 2.20 shows the first state when the semiconductor switch is conducting (ON) whiles the diode is reverse biased (OFF). Figure 2.21 shows the reverse state of Figure 2.20; the diode is forward biased whiles the semiconductor switch is non-conducting. Finally, in the last state of Figure 2.22 both the diode and the switch are not conducting.

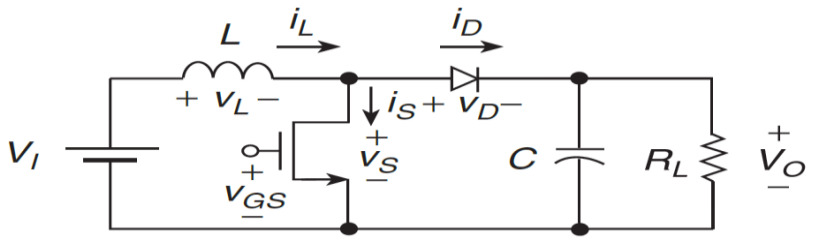

Figure 2.19: Boos t converter

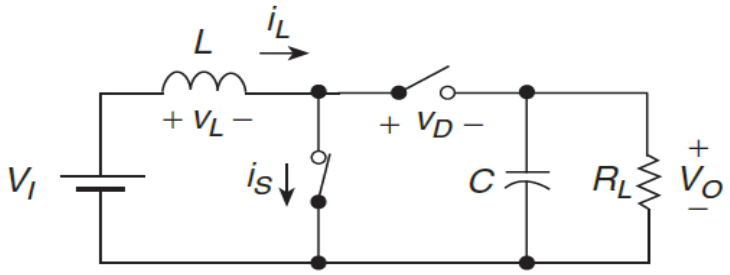

Figure 2.20: DCM first state

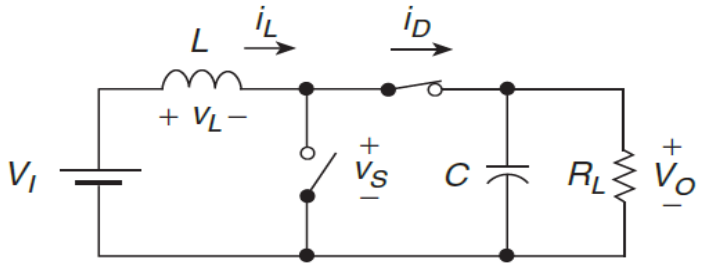

Figure 2.21: DCM second state

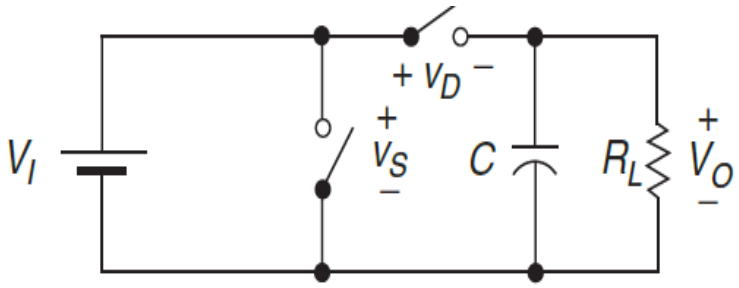

Figure 2.22: DCM third state

The output waveforms for these time intervals are represented below, during the period of $0 < t \leq DT$, its circuit is shown by Figure 2.20. On the other hand, Figure 2.21 illustrates the period of conduction for $DT < t \leq (D+_1)T$. The finally period of $(D + D_1)T < + \leq T$ represents Figure 2.22. The components output waveforms during these periods are shown by Figure 2.23. The major components illustrated by the output waveforms are:

- Input voltage
- Switch current
- Inductor current
- Inductor voltage
- Diode current
- Diode voltage
- Source voltage

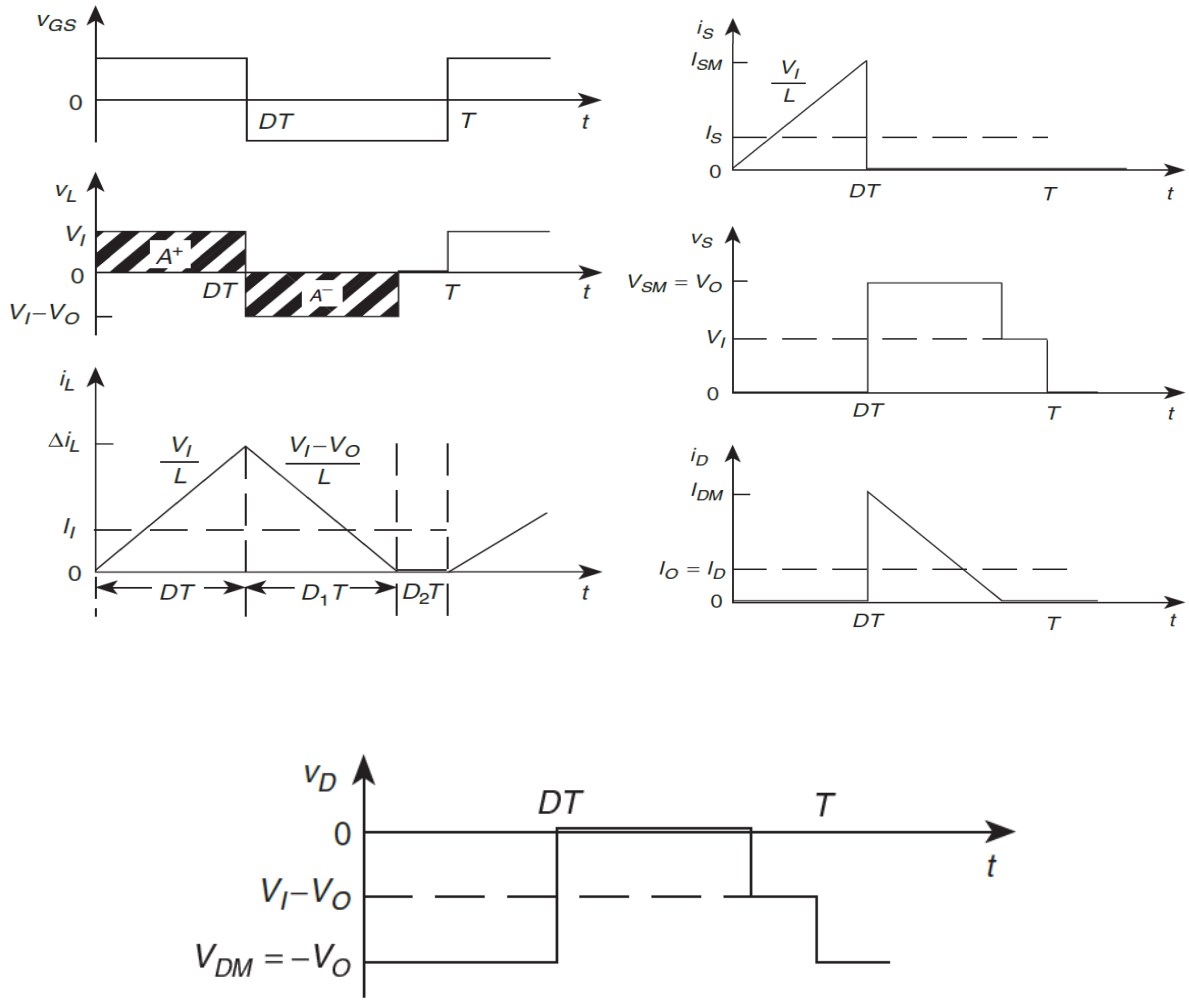

Figure 2.23: DCM boost converter output waveforms

The following expressions are developed during the period of $0 < t \leq DT$, its circuit is shown by Figure 2.20.

$$v_L = V_i \tag{2.71}$$

$$V_i = L\frac{di_L}{dt} \tag{2.72}$$

$$i_s = \frac{V_i}{L}t \tag{2.73}$$

Maximum switch current:

$$I_{SM} = \frac{DV_i}{Lf_s} \tag{2.74}$$

The following expressions are developed during the period of $DT < t \leq (D + D_1)T$, its circuit is shown by Figure 2.21:

$$v_s = V_o \tag{2.75}$$

Maximum diode current:

$$I_{DM} = \frac{D_1(V_0 - V_i)}{Lf_s} \tag{2.76}$$

$$v_i = V_i - V_o \tag{2.77}$$

$$i_D = \frac{V_i DT}{L} + (t - DT)\frac{V_i - V_o}{L} \tag{2.78}$$

The following expressions are developed during the period of $(D + D_1) < t \leq T$, its circuit is shown by Figure 2.21:

$$v_s = V_o \tag{2.79}$$

$$v_D = V_i - V_o \tag{2.80}$$

2.4 Selected Buck Topologies

A buck multiphase dc-dc converter is presented in (Gordillo & Aguilar, 2017) which provides equal output current sharing capabilities thereby ensuring equality in thermal stresses and power losses. Several current sharing methodologies have been presented over the years and these methods require a sensing circuit which eventually increases the total cost of the system and also increases the complexity of the control system however, the presented method in this paper does not require a sensing circuit and it's a simple technique. This technique determines the

parasitic resistance for each phase and the calculations for the duty cycles are determined which are useful in current sharing methodology. Analog to digital converters are not required when using the control loop technique. The five phase buck converter is shown by Figure 2.25. The power circuit is composed of the following:

- 10 MOSFET switches
- 5 RL load
- One capacitor and one resistance

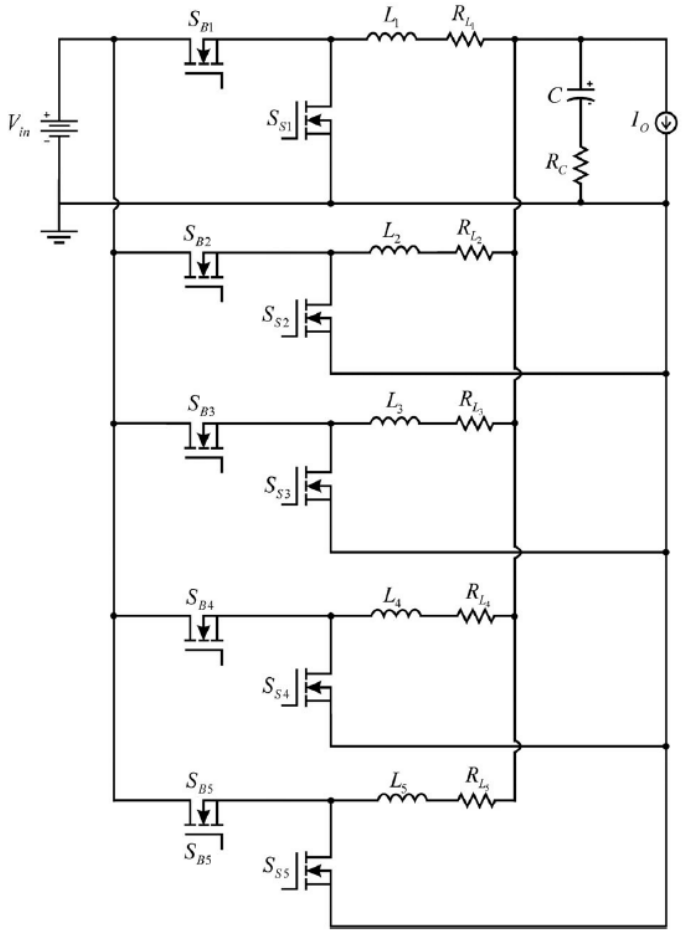

Figure 2.24: Synchronous 5-phase buck converter

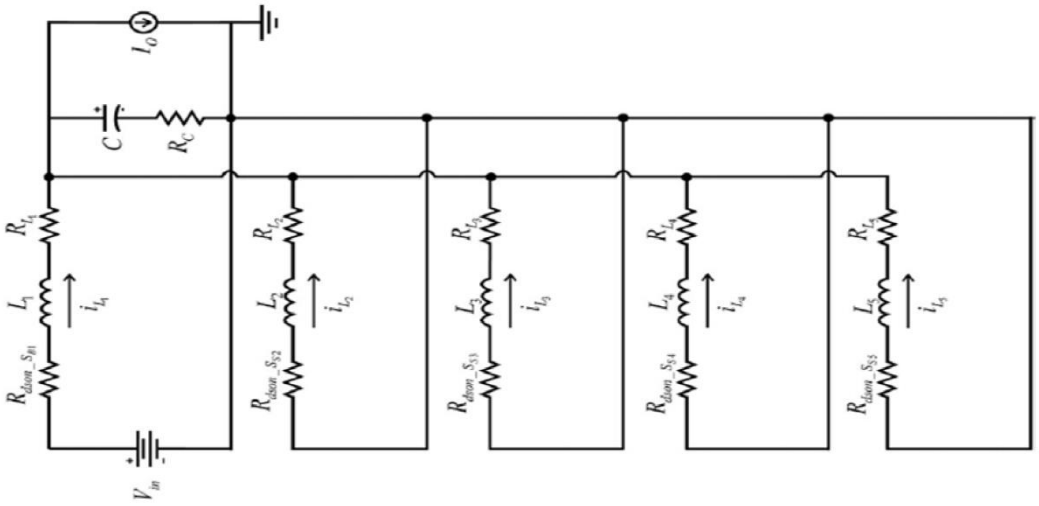

Figure 2.25: D_1T_s interval equivalent circuit

A two cell buck converter is presented in (El Aroudi et al., 2008) where its modelling and design are investigated. The presented buck converter power circuit is shown in Figure 2.26. The circuit contains the following components: 2 power switches, 2 diodes, input voltage V_{in}, output voltage v_o, one capacitor and one inductor. Balancing the voltage across the cells will provide minimum semiconductor stresses and this is achieved by using a controlled source voltage. The controlled voltage source is achieved by incorporating a capacitor to the topology and controlled by power switches S_1 and S_2. The two diodes conduct by a complimentary manner with respect to the switches. When switch S_1 conducts, D_2 is forward biased and D_1 is reverse biased. When switch S_2 conducts D_1 is forward biased and diode D_2 is reverse biased.

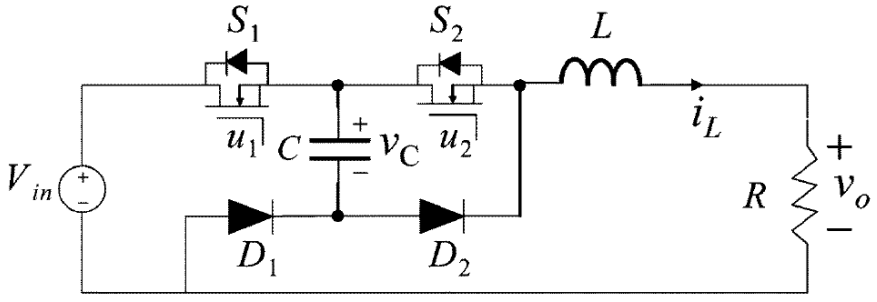

Figure 2.26: Two-cell buck converter

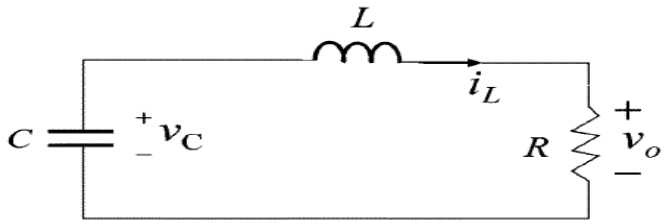

Figure 2.27: Equivalent circuit when S_1 is off and S_2 is on.

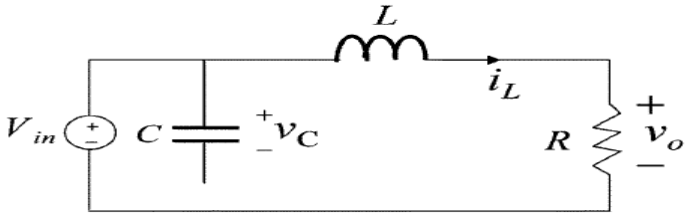

Figure 2.28: Equivalent circuit when S_1 is on and S_2 is on.

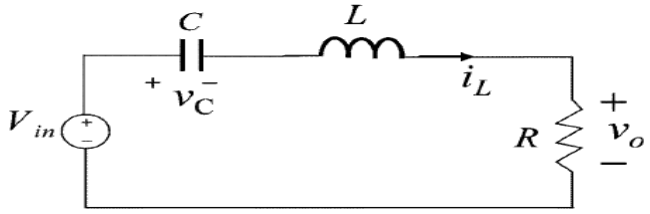

Figure 2.29: Mode of operation when S_1 is on and S_2 is off.

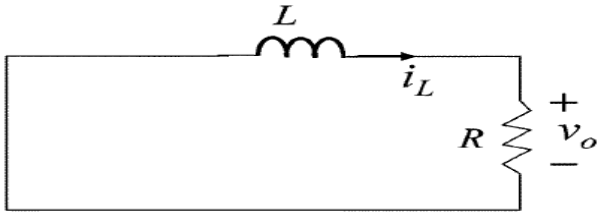

Figure 2.30: Mode of operation when S_1 is off and S_2 is off.

An improved non-isolated buck converter is presented in (Varesi et al., 2017). This topology of buck converter also has multi-input capabilities which enables independent power transfer or simultaneous power transfer. This topology is released with less number of components which directly translates to reduced losses, increased efficiency, minimum size and volume and finally

reduced converter cost. by adding a battery to the structure, bidirectional power flow is enabled. This feature makes the converter suitable for application in hybrid systems. The power circuit of the presented topology is given by Figure 2.31 whiles Figure 2.32 shows the modes of operations.

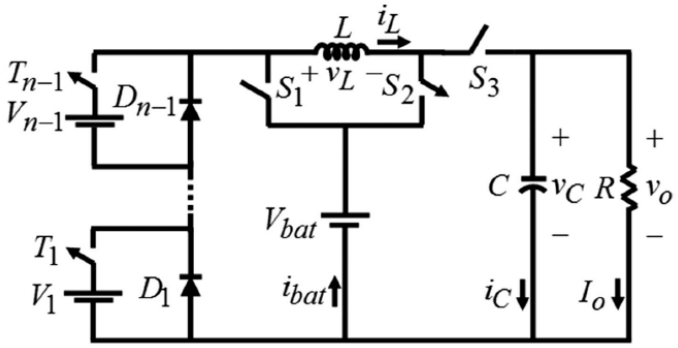

Figure 2.31: Improved non-isolated topology

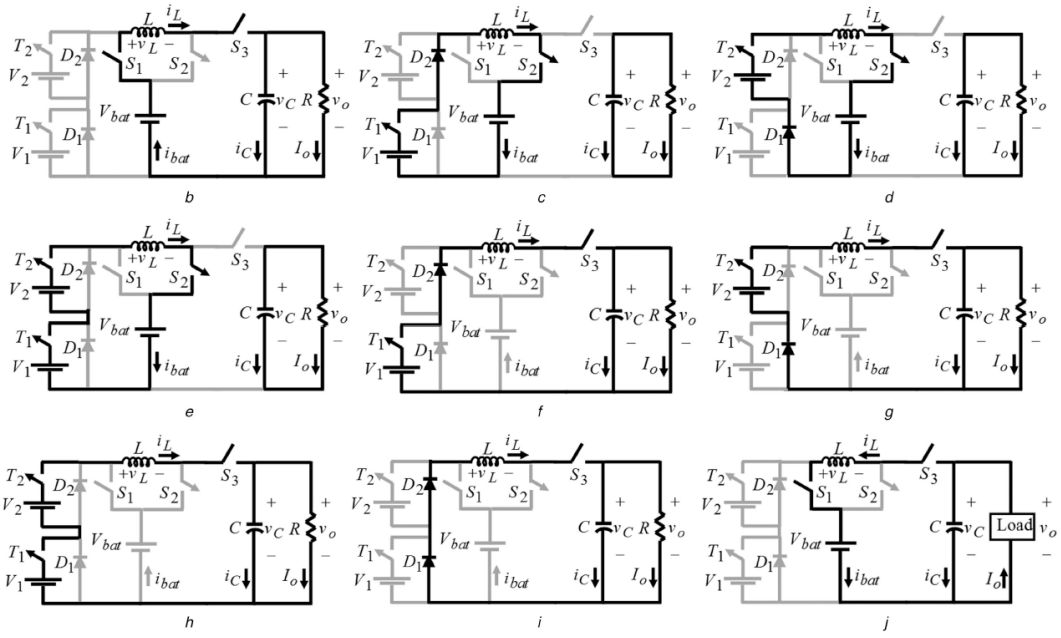

Figure 2.32: Modes of operation

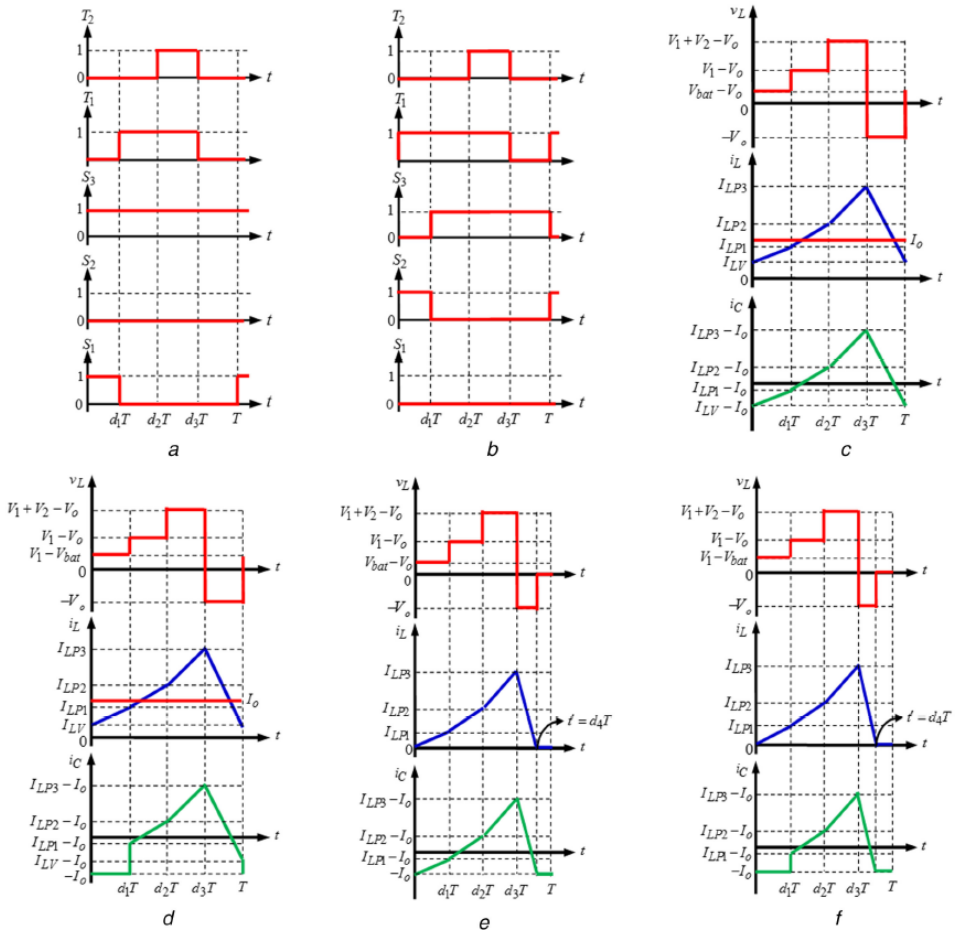

Figure 2.33: Output waveforms

A buck converter topology derived from amalgamation of existing topologies is presented in (Dc et al., 2019). These existing topologies which are used in presenting the new topologies are a) interleaved b) series-capacitor and finally c) tapped topologies or transformer based topologies. Figure 2.34. Shows the series-capacitor topology, Figure 2.35 shows two circuit of the series-capacitor tapped topology and finally the hybrid transformer based topology is shown by Figure 2.36. Each topology has its corresponding output waveform.

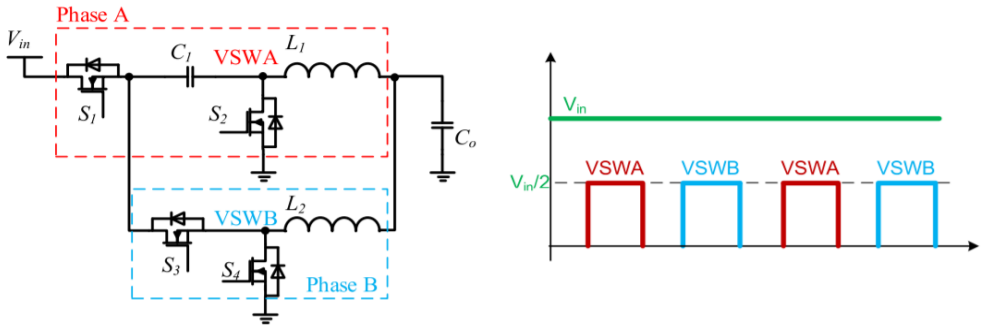

Figure 2.34: Series-capacitor topology.

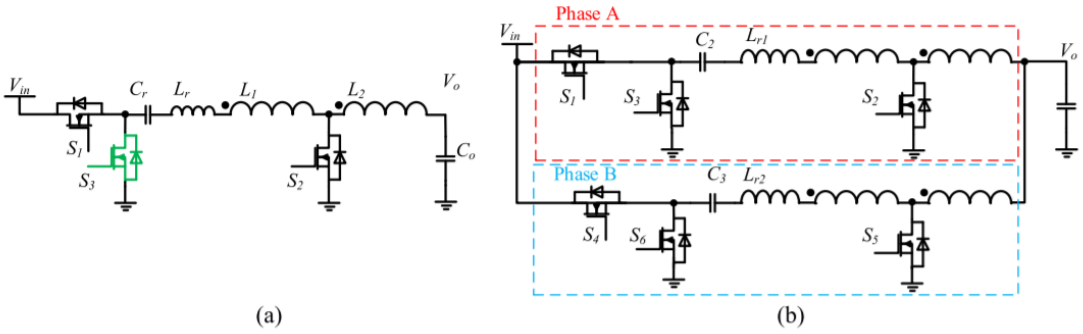

Figure 2.35: Series-capacitor tapped topologies

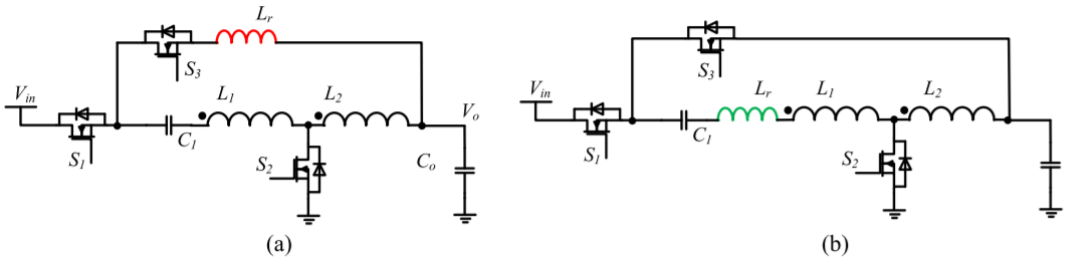

Figure 2.36: Hybrid transformer topologies

The presented topology of Figure 37 is amongst several topologies of buck converters that provide improved performance a feature which is absent in the conventional buck topology. the

above mentioned topologies are part of these topologies that provide improved performance and the presented topology combines the advantages of the amalgamated topologies.

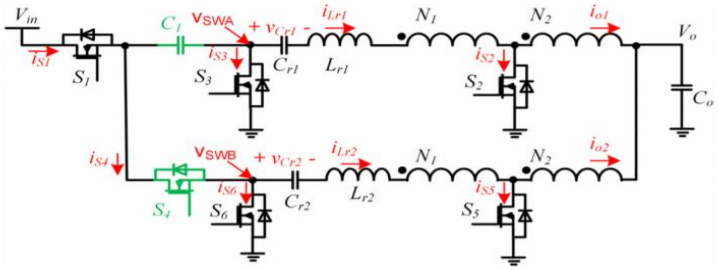

Figure 2.37: Interleaved SC-Ta buck converter.

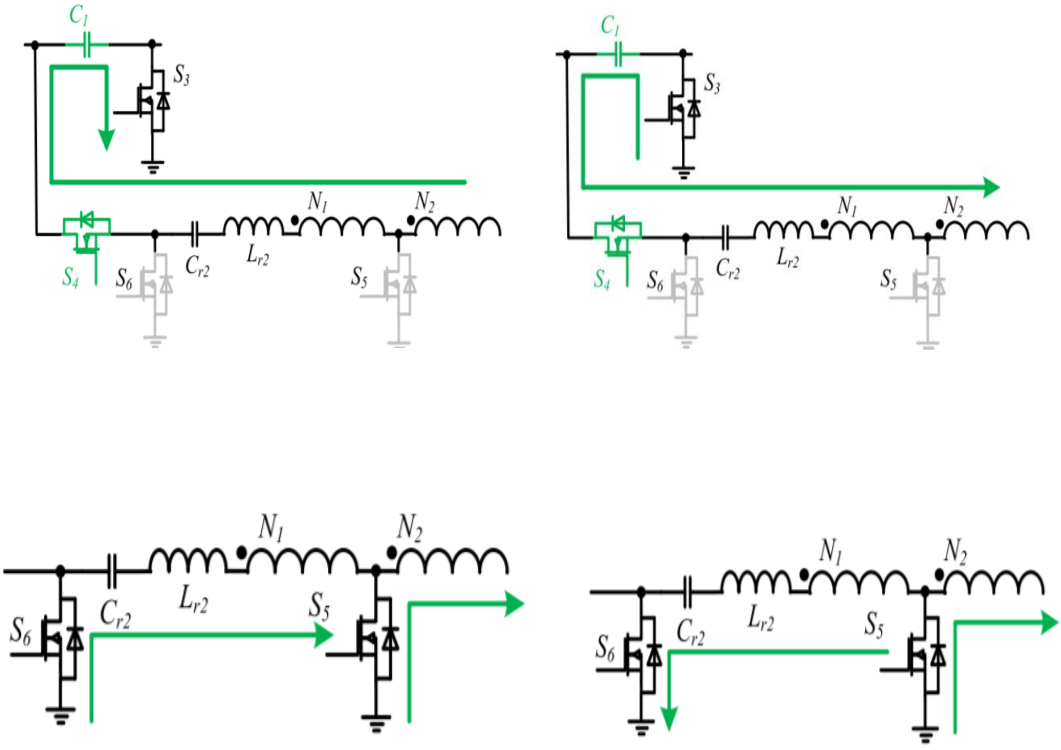

Figure 2.38: Modes of operation

2.5 Selected Buck Topologies

An improved novel boost dc-dc converter (Sahin & Umaz, 2019) is reviewed in this section. This reviewed topology of dc-dc boost converter has less magnitude of voltage across the filter capacitor. when compared to other traditional boost dc-dc converters, this presented topology provides the advantages of higher power density and minimum converter cost because of the use of lower rated capacitor. Also there's less complexity in its design because of its simple structure. Figure 2.39 shows the power circuit of the presented topology. Its composed one inductor, one capacitor, one switch, one diode and input and output sources. Two modes of operational capabilities exist in the presented topology, the power circuit of these modes of operation are shown by Figure 2.40a and Figure 2.40b.

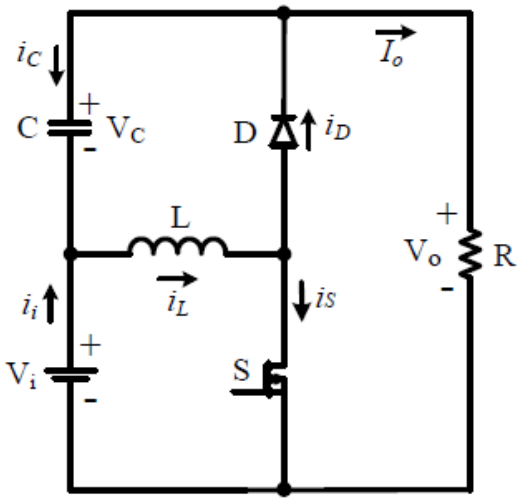

Figure 2.39: Boost dc-dc converter

The first mode of operation is given by Figure 40a where the diode is forward biased and the power switch is non-conducting, this occurs before the turning on signal is applied to the power switch, basically the first mode starts when the power switch is conducting and the diode is reverse biased. The inductor energy increases during this period whiles its current flows through the switch, when the switch is turned off, this mode ends and the second mode begins, the following expressions are developed for this mode:

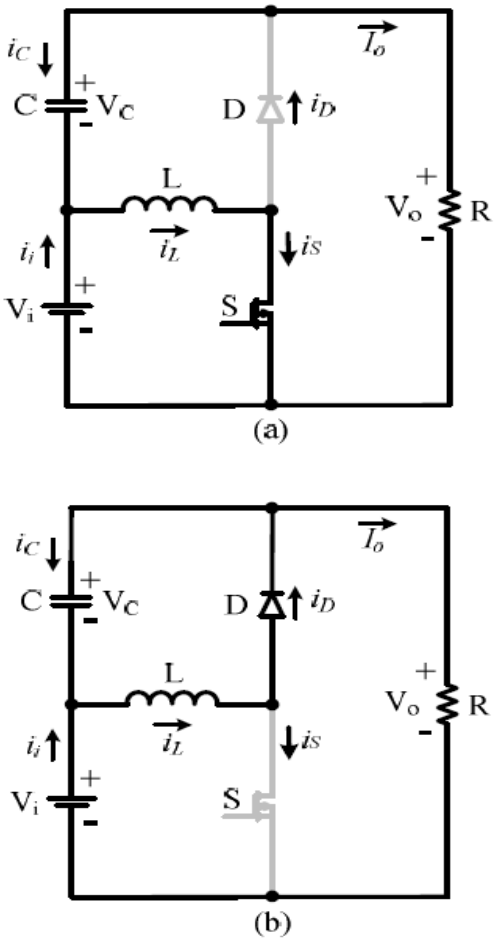

Figure 2.40: Modes of operation

$$\Delta i_L = \frac{V_i T_{on}}{L} \tag{2.81}$$

$$\Delta i_c = \frac{V_o T_{on}}{R} \tag{2.82}$$

$$\frac{dv_c}{dt} = \frac{V_o T_{on}}{RC} \tag{2.83}$$

$$\Delta v_c = -\frac{V_o T_{on}}{RC} \tag{2.84}$$

The second mode is shown by Figure 2.40b and this starts when the switch is turned off thus the diode becomes forward biased because of the positive voltage across its terminals. The inductor energy minimises in this state and the following expressions are developed for this mode.

$$v_L = v_c \tag{2.85}$$

$$\Delta i_L = \left(\frac{V_o - V_i}{L}\right) T_{off} \tag{2.86}$$

$$\Delta i_C = \left(I_L - \frac{V_o}{R}\right) T_{off} \tag{2.87}$$

$$V_O = \frac{V_i}{1-D} \tag{2.88}$$

A new topology of quadratic boost converter (Veerachary, 2018) is reviewed in this part. This topology of boost converter is a fifth order topology. analysis of the presented topology is done with respect to steady state and time domain analysis. The main advantage of this topology is its capability to provide higher voltage boosting than conventional quadratic topologies. Figure 41 shows the power circuit of the presented topology. its made-up of one power switch, three capacitors, four diodes, two inductors and input and output sections. It's actually derived by adding one diode and one capacitor to the conventional quadratic topology. two modes of operation exist, in the first mode shown by Figure 42, the switch and two diodes (D2 and D3) conducts whiles the remaining diodes are reverse biased. In the second mode shown by Figure 43, diodes D1 and D4 conducts whiles the switch and diodes (D2 and D3) are non-conducting.

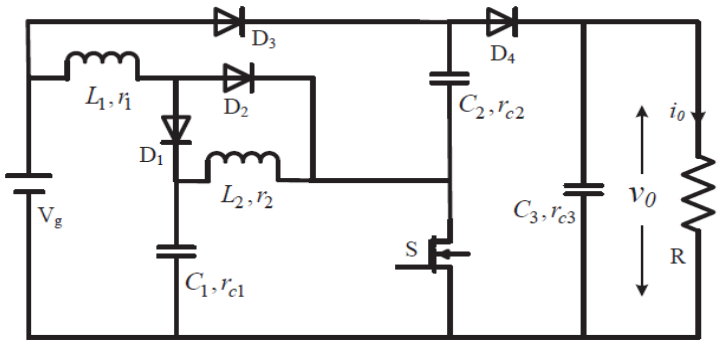

Figure 2.41: 5th order boost converter

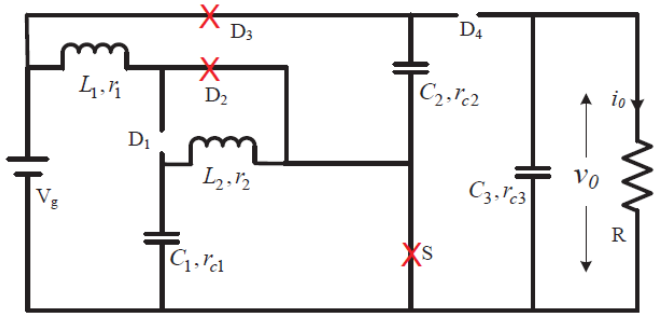

Figure 2.42: 1st mode of operation

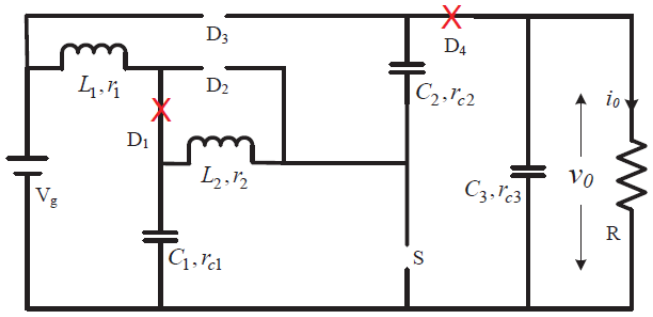

Figure 2.43: 2nd mode of operation

Mode 1:

$$v_{L1} = V_g \tag{2.89}$$

$$v_{L2} = v_{C1} \tag{2.90}$$

Mode 2:

$$v_{L1} = V_g - v_{C1} \tag{2.91}$$

$$v_{L2} = (v_{c1} + v_{c2}) - V_o \tag{2.92}$$

Using volt-sec method:

$$DV_g + (v_g - v_{C1})(1 - D) = 0 \tag{2.93}$$

$$Dv_{c1} + (1 - D)v_{c1} = (1 - D)(V_o - v_{c2}) \tag{2.94}$$

Voltage gain:

$$G = \frac{2+D^2-2D}{(1-D)^2} \tag{2.95}$$

A review of a non-isolated boost converter presented by (Shahir & Azar, 2018) is carried out in this part. The new boost converter is derived by utilizing the LV (voltage lift) technique. Analysis of the new converter is done during CCM state of operation where the its voltage gain is obtained. Figure 2.44 shows the power circuit of the presented boost dc-dc converter topology which is made up of 2 power switches, two inductors, three capacitors and three diodes. Two modes of operation are possible as indicated by Figure 2.45a and 2.45b. These modes occur between two time intervals:

a. $0 \leq t \leq T_{on}$
b. $T_{on} \leq t \leq T_{off}$

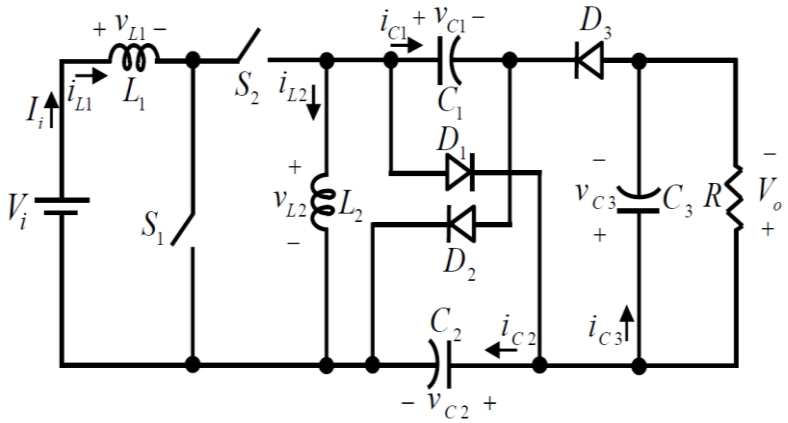

Figure 2.44: Boost converter

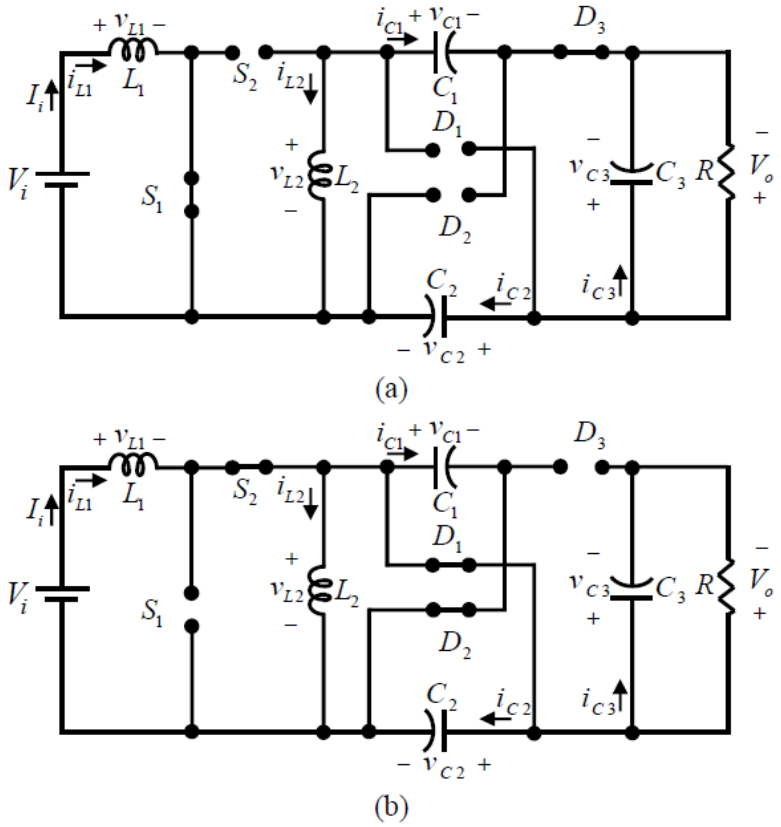

Figure 2.45: Modes of operation

The first mode of operation (Figure 2.45a) occurs during $0 \leq t \leq T_{on}$ time interval, switch S_1 and diode D_3 conducts, whiles switch S2 and diodes D_1 and D_2 are non-conducting. The inductor energy increases during this period and its current also has maximum exponential increase. Also there's a series connection between the load, all three capacitors and the inductor L2. In the second state of operation (Figure 2.45b), switch S1 and diode D3 are not conduction while the remaining active switches are conducting. Some selected expression for CCM state of operations are shown below:

$$v_{L1} = V_i \tag{2.96}$$

$$v_L = L\frac{di_L}{dt} \tag{2.97}$$

$$V_i = L_1 \frac{di_{L1}}{dt} \tag{2.98}$$

$$i_{L1} = \frac{tV_i}{L_1} + I_{LV1} \tag{2.99}$$

$$v_{L1} = V_i - V_{c1} \tag{2.100}$$

$$D = \frac{T_{on}}{T} \tag{2.101}$$

$$v_{C1} = V_i \frac{1}{1-D} \tag{2.102}$$

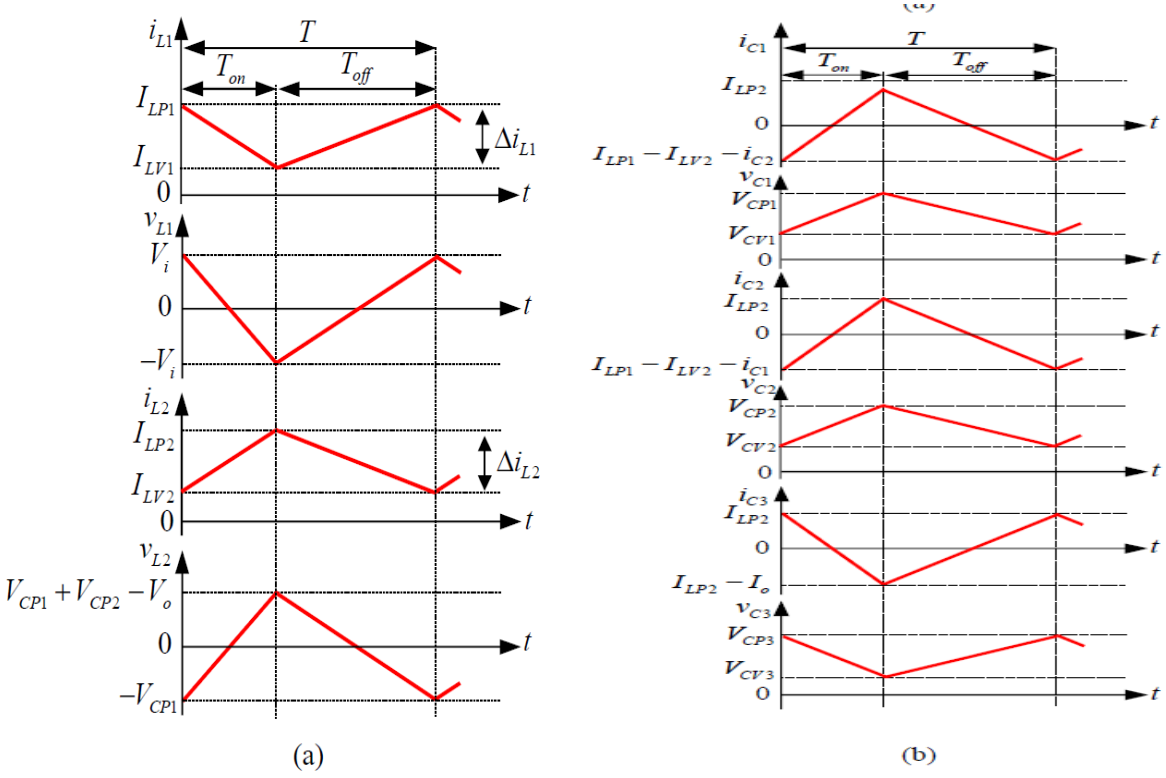

Figure 2.46: Output waveforms: inductor (a) and capacitors (b)

2.6 Buck-Boost DC-DC Topology

The buck-boost topology of the dc-dc converter combines the advantages of the buck and boost topologies thus it's able to provide stepup and stepdown capabilities without introducing extra converter structure. Figure 2.47 shows the power circuit which is made-up of one diode, one power switch, one inductor and one capacitor. Analysis of this circuit in the CCM state is shown by Figure 2.48 where the switch is closed and the diode is reverse biased and Figure 2.49 where the switch is opened and the diode is forward biased.

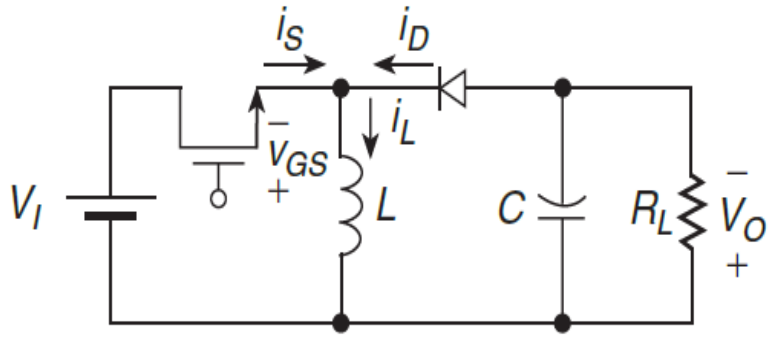

Figure 2.47: Buck-boost converter

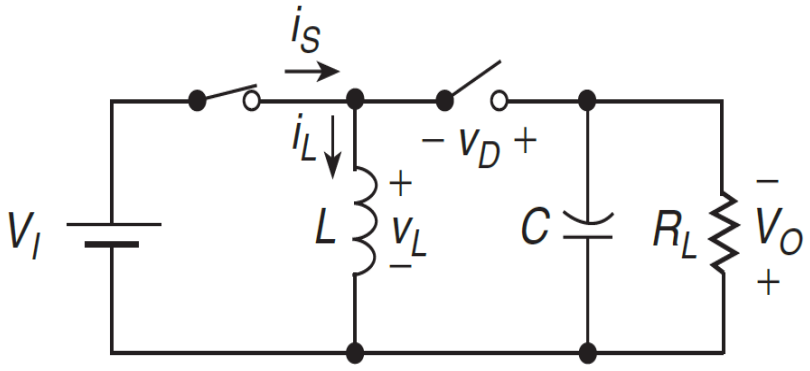

Figure 2.48: Mode of operation

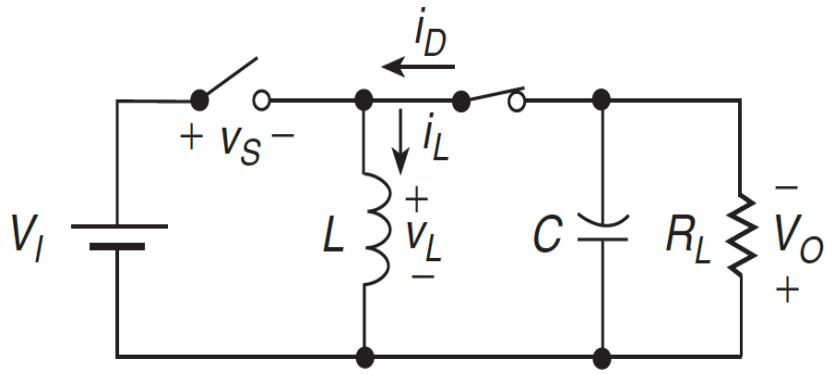

Figure 2.49: Mode of operation

The ideal output waveforms for these modes of operation are shown by Figure 50. The first mode of operation of Figure 48 last for the time interval $0 < t \leq DT$. In this interval the diode is reverse biased whiles the switch conducts. The following expressions are developed for this time interval:

$$v_D = -(V_i + V_o) \tag{2.103}$$

$$v_s = 0 \tag{2.104}$$

$$i_D = 0 \tag{2.105}$$

$$v_L = V_i \tag{2.106}$$

$$i_s = i_L + \frac{V_i}{L} \tag{2.107}$$

$$v_D = -\frac{V_i}{L} \tag{2.108}$$

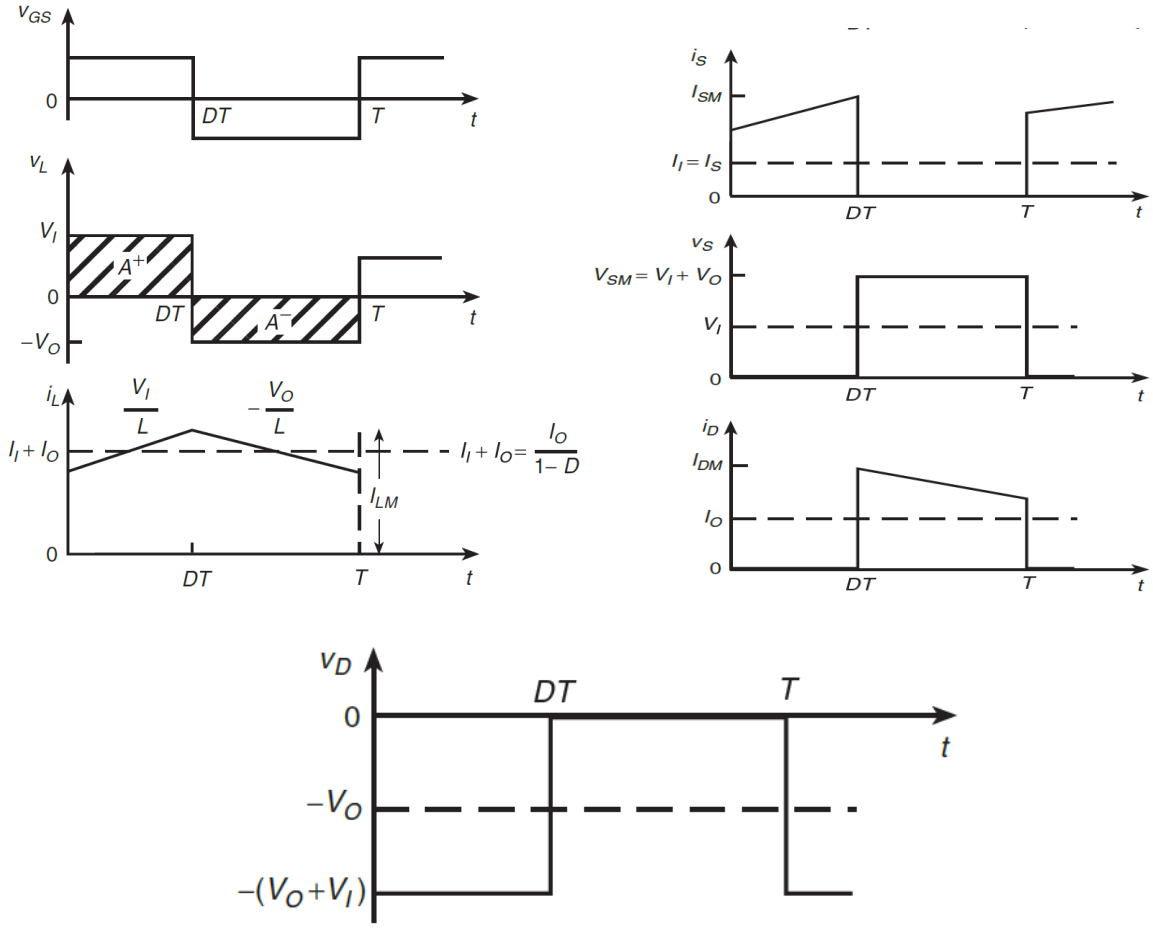

Figure 2.50: Ideal output waveforms for CCM state

The second mode of operation of Figure 2.49 last for the time interval $DT < t \leq T$. In this interval the diode is forward biased whiles the switch does not conduct. The following expressions are developed for this time interval:

$$i_s = 0, v_D = 0 \tag{2.109}$$

$$v_L = L\frac{di_L}{dt} \tag{2.110}$$

$$i_D = i_L + \frac{DV_i}{Lf_s} - \frac{V_o}{L}(t - DT) \tag{2.111}$$

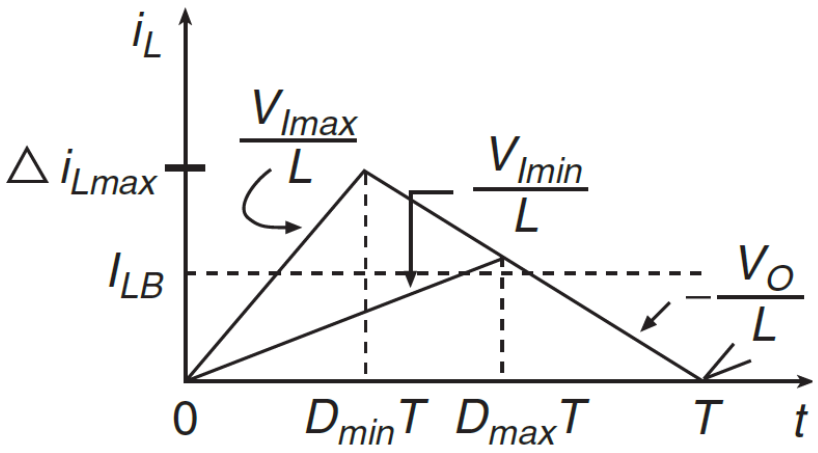

Figure 2.51: Buck-boost critical angle for CCM

The buck-boost converter power losses are explained below suing Figure 2.52 which contains parasitic components. Switching power losses P_{SPL}.

$$P_{SPL} = \frac{P_o f_s C_o R_L (1+M_{VDC})}{M_{VDC}^2} \tag{2.112}$$

$$P_{rC} = \frac{P_o D_{rc}}{R_L(1-D)} \tag{2.113}$$

$$P_{rL} = \frac{P_o r_L}{R_L(1-D)^2} \tag{2.114}$$

$$P_D = P_O(\frac{V_F}{V_o} + \frac{R_F}{R_L(1-D)} \tag{2.115}$$

MOSFET conduction power loss P_{MOSFET} is given by:

$$P_{MOSFET} = \frac{P_O D_{rDS}}{R_L(1-D)^2} \tag{2.116}$$

Therefore, the total power loss of the converter is given by:

$$P_{TOTAL} = P_{rC} + P_{MOSFET} + P_{rL} + P_{SPL} + P_D \tag{2.117}$$

Hence the converter efficiency is given by:

$$Efficiency\ \eta = \frac{Power\ output\ P_o}{Power\ input\ P_i} = \frac{P_o}{P_o + P_{TOTAL}} \tag{2.118}$$

Analysis of the buck-boost converter during the discontinuous conduction mode is investigated by using the power circuit of Figure 2.52. There are three states of operations in the DCM state which are represented by Figure 2.53 to Fig 2.55. Figure 2.53 shows the first state when the semiconductor switch is conducting (ON) whiles the diode is reverse biased (OFF). Figure 2.54 shows the reverse state of Figure 2.53; the diode is forward biased whiles the semiconductor switch is non-conducting. Finally, in the last state of Figure 2.55 both the diode and the switch are not conducting. The three modes of operation of the converter exists in the following time intervals:

$0 < t \leq DT$ represented by Figure 2.53.

$DT < t \leq (D + D_1)T$ represented by Figure 2.54.

$(D + D_1)T < t \leq T$ represented by Figure 2.55.

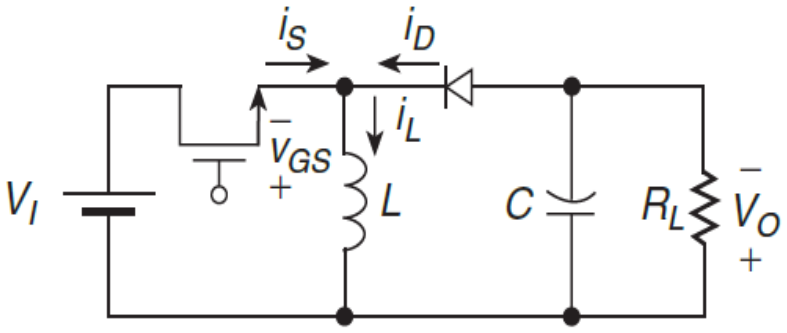

Figure 2.52: Buck-boost converter

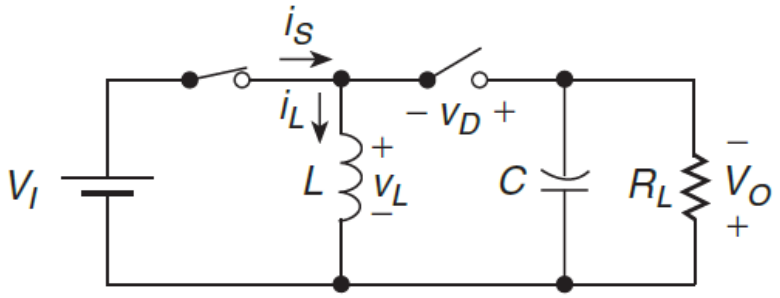

Figure 2.53: Mode of operation

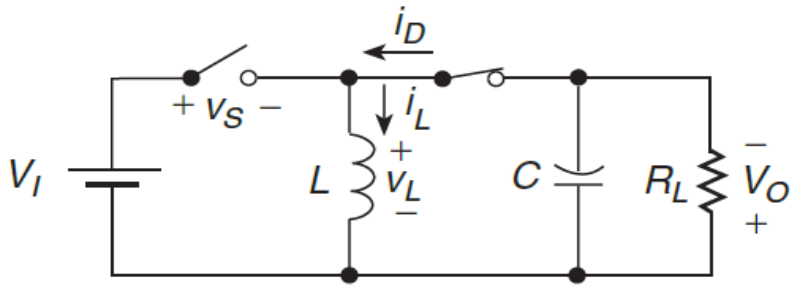

Figure 2.54: Mode of operation

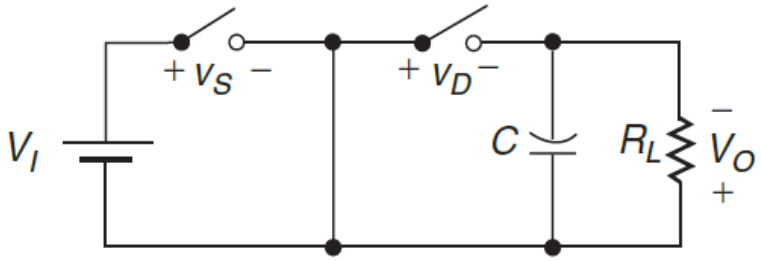

Figure 2.55: Mode of operation

The mathematical expression developed for the following time intervals are given below:

$0 < t \leq DT$ represented by Figure 2.53:

$$v_s = 0 \tag{2.119}$$

$$i_D = 0 \tag{2.120}$$

$$v_L = L\frac{di_L}{dt} \tag{2.121}$$

$$v_L = V_i \tag{2.122}$$

$$i_s = t\frac{V_i}{L} \tag{2.123}$$

$$v_D = -V_i + V_o \tag{2.124}$$

$DT < t \leq (D + D_1)T$ represented by Figure 2.54:

$$v_D = 0 \tag{2.125}$$

$$i_s = 0 \tag{2.126}$$

$$v_L = L\frac{di_L}{dt} \tag{2.127}$$

$$v_L = -V_o \tag{2.128}$$

$$i_D = -\frac{V_o}{L}\ (t - DT) + \frac{V_i DT}{L} \tag{2.129}$$

$(D + D_1)T < t \leq T$ represented by Figure 2.55:

$$v_D = -V_o \tag{2.130}$$

$$v_s = V_i \tag{2.131}$$

$$i_s = 0 \tag{2.132}$$

$$i_D = 0 \tag{2.133}$$

$$i_L = 0 \tag{2.134}$$

$$v_L = 0 \tag{2.135}$$

Converter power losses and efficiency are derived by:

$$P_{SW} = f_s C_o V_{sm}^2 \tag{2.136}$$

$$P_{rDs} = P_o M_{VDC} * \frac{2_{rDs}}{3} \sqrt{\frac{2}{R_L L f_s}} \tag{2.137}$$

The losses due to the inductor:

$$P_{rL} = r_L I_{Lrms}^2 \tag{2.138}$$

$$P_D = P_o \left(\frac{V_F}{V_o} + \frac{2R_F}{3} \sqrt{\frac{2}{R_L L f_s}}\right) \tag{2.139}$$

The total converter losses and efficiency are expressed by:

$$P_{TOTAL} = P_D + P_{rL} + P_{rDs} + P_{SW} \tag{2.140}$$

$$\text{Efficiency } \eta = \frac{P_o}{P_o + P_{TOTAL}} \tag{2.141}$$

2.7 Selected Buck-Boost Topologies

A novel buck-boost converter referred to as negative output KY is reviewed in this section (Hwu & Yau, 2009). The presented topology of converter has bilinear features. Figure 2.56 shows the power circuit of the presented topology, it has two mode of operations which are represented by Figure 2.57 and Figure 2.58. The power circuit is composed of four unidirectional power switches, two diodes, two capacitors and a low pass output filter. In the first mode of operation (Figure 2.57), the lower switches of S_2 and S_4 are gated on whiles the upper switches remains off. The following expressions are developed for this mode:

$$L_o \frac{di_o}{dt} = 2V_i - V_o \tag{2.142}$$

$$C_o \frac{dV_o}{dt} = -\frac{V_o}{R_o} + i_o \tag{2.143}$$

$$i_o = i_{b2} \tag{2.144}$$

$$i_i = i_{b1} \tag{2.145}$$

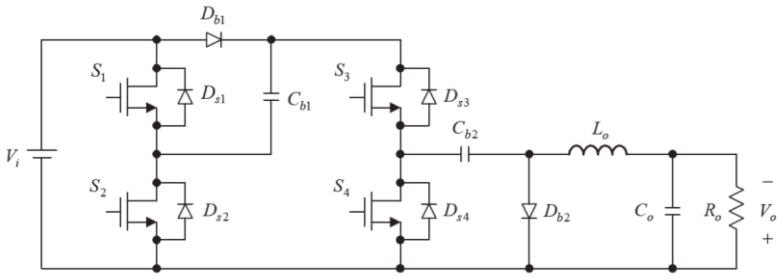

Figure 2.56: Negative output KY converter

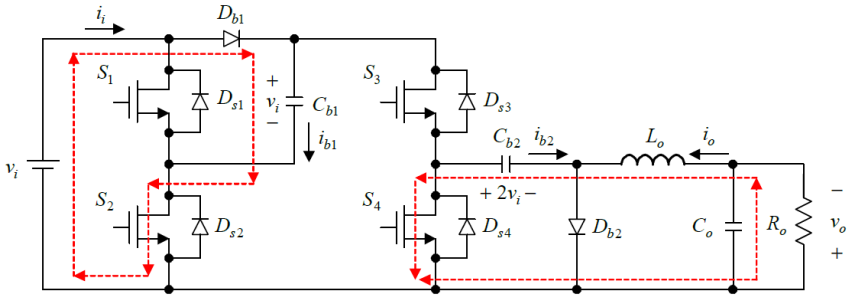

Figure 2.57: Mode 1 operational state

The following expressions are developed for the second mode of operation where the upper switches of S1 and S3 are gated on whiles the lower switches are gated off.

$$L_o \frac{di_o}{dt} = V_o \tag{2.146}$$

$$C_o \frac{dV_o}{dt} = -\frac{V_o}{R_o} + i_o \tag{2.147}$$

$$i_i = i_{b1} \tag{2.148}$$

$$i_i = i_{b2} \tag{2.149}$$

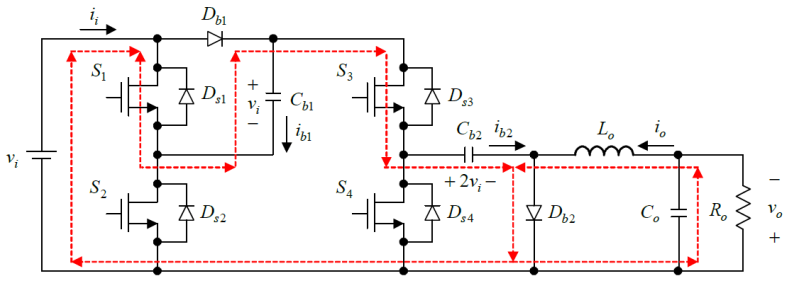

Figure 2.58: Mode 2 operational state

Another type of KY topology of buck-boost is presented in (Hwu et al., 2009). This topology of converter has better rapid responses when compared to the conventional buck-boost topologies. It also has the feature of output current which is non-pulsating which means that the stress on the output capacitor is minimised and also the ripples in the output voltage are reduced. Two types of KY structures are presented and they will be reviewed individually in this section. The first topology is shown by Figure 2.59 whiles Figure 2.62 shows the second topology. The first topology has one diode, one capacitor, four switches and an output filter, however, the second topology has two input voltage sources, four switches one capacitor, one diode and an output filter. The modes of operation of the first topology are shown by Figure 2.60 and Figure 2.61.

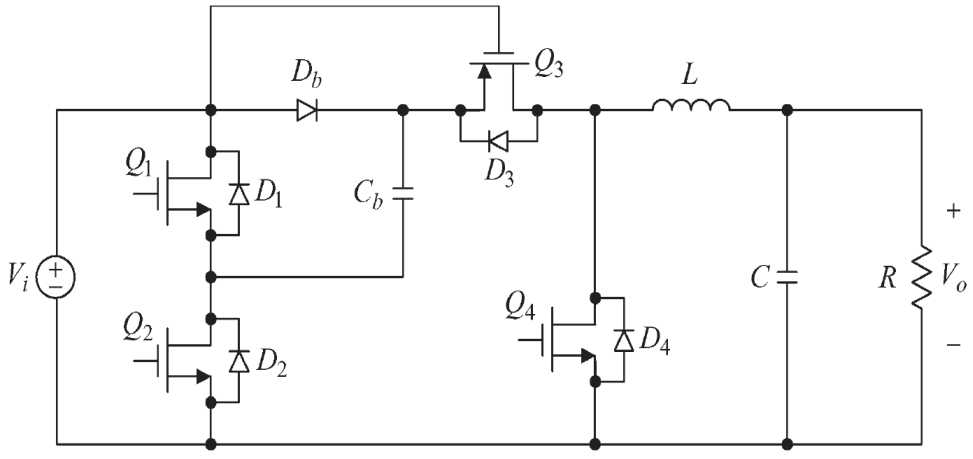

Figure 2.59: First topology of KY

Mode 1 of Type 1:

$$\frac{Ldi}{dt} = 2V_i - V_o \tag{2.150}$$

$$\frac{CdV_o}{dt} = i - \frac{V_o}{R} \tag{2.151}$$

$$i = i_. \tag{2.152}$$

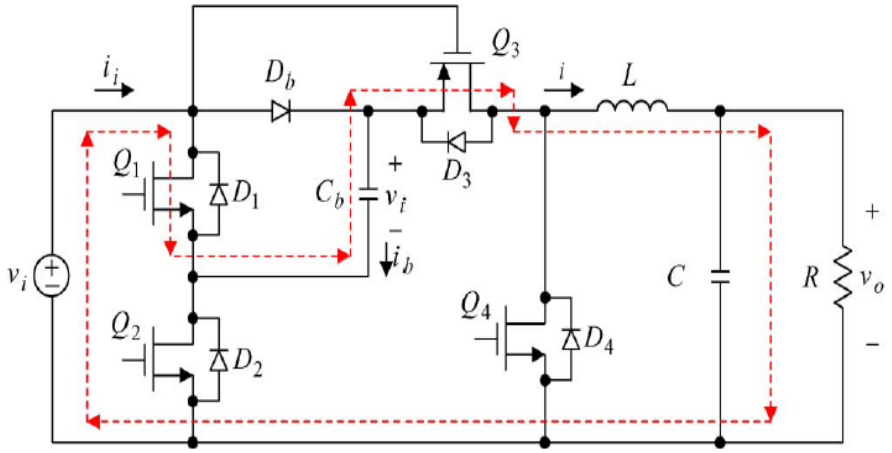

Figure 2.60: Mode 1 operation for first topology

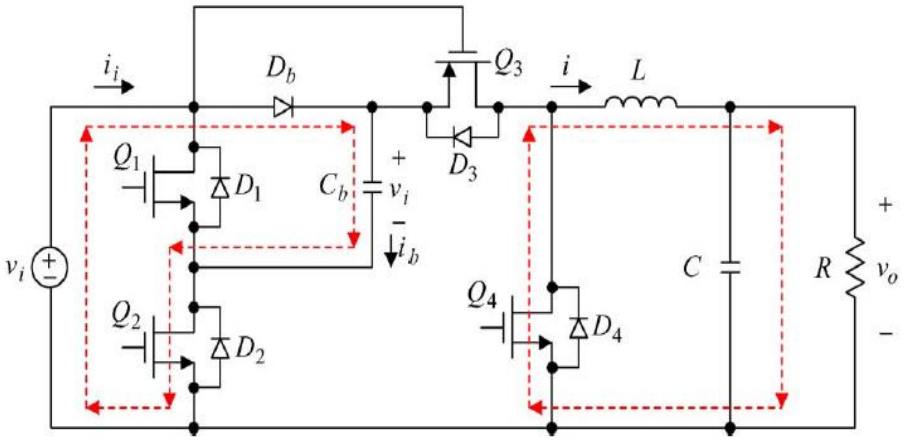

Figure 2.61: Mode 2 operation for first topology

Mode 2 of Type 1:

$$v_{L1} = V_i \tag{2.153}$$

$$v_{L2} = V_i + v_{c1} - v_{c2} - v_{c3} \tag{2.154}$$

$$v_{L3} = v_{c1} + V_i - V_o \tag{2.155}$$

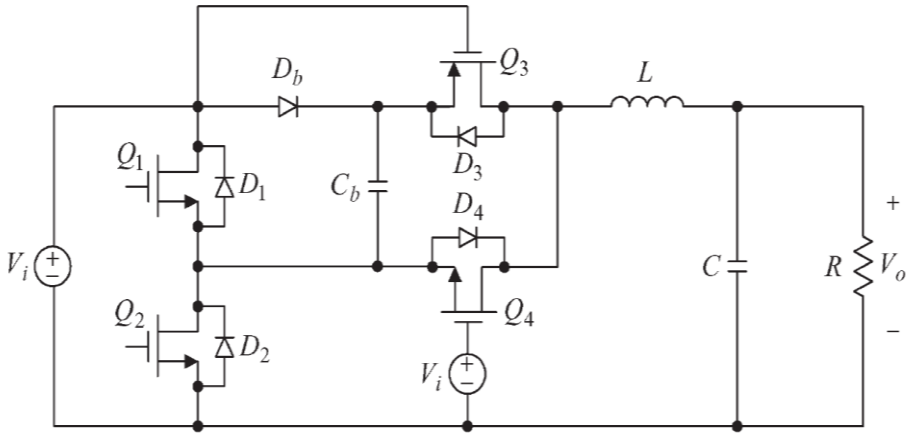

Figure 2.62: Second Topology of KY

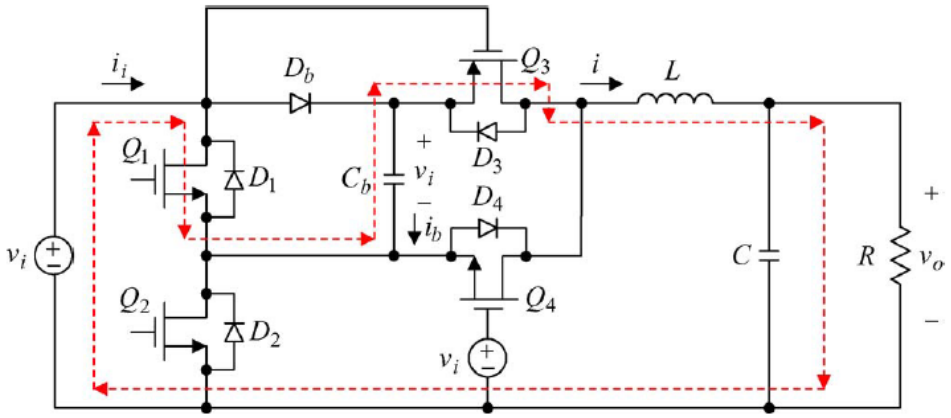

Figure 2.63: Mode 1 operation for second topology

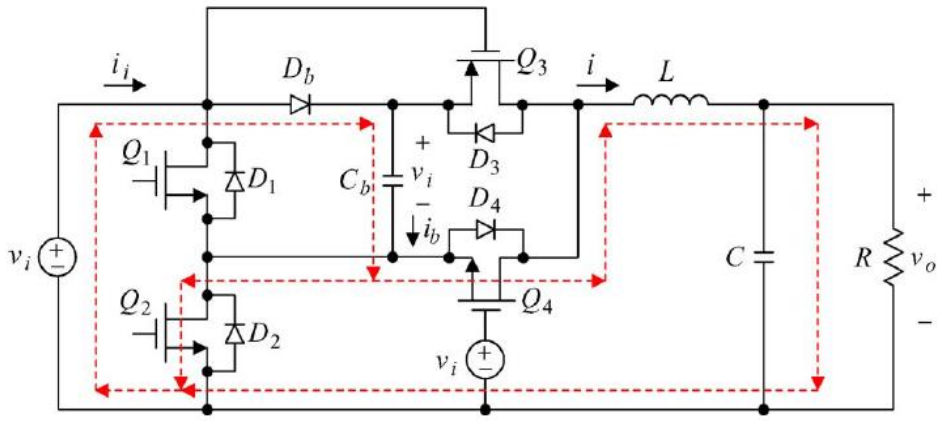

Figure 2.64: Mode 2 operation for second topology

A new topology of buck-boost converter (non-isolated) with high efficiency is presented in (Banaei & Bonab, 2020), this converter is derived from the Zeta topology therefore it inherits all the advantages of the Zeta topology; dc insulation for the input and output sections, buck-boost abilities and uninterrupted flow of output current. The presented topology uses only one power switch with low voltage stress and has higher voltage gain when compared to traditional Zeta structures. Figure 2.65 shows the power circuit of the presented topology and it contains two inductors, three capacitors, two diodes, one switch and an output filter. There are two modes of operation. The first mode is represented by Figure 2.66 whiles the second mode is represented by Figure 2.67.

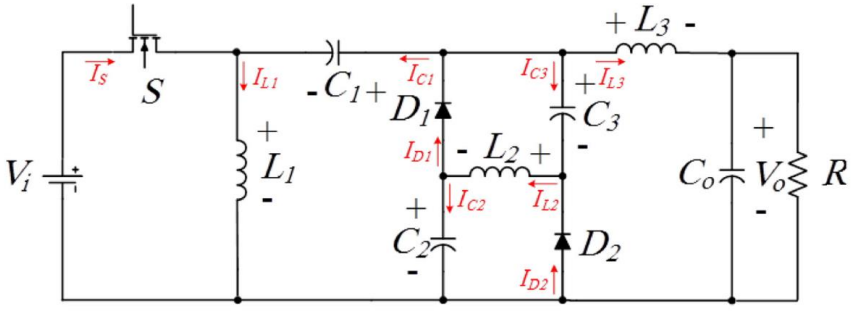

Figure 2.65: Non-isolated buck-boost converter

Both CCM and DCM states of operation are possible in the presented topology however, CCM state is used in operations. In the first mode which last for the time interval of DT_s, the switch is gated on, the diodes D1 and D2 becomes reverse biased because of the negative source voltage across its terminal. The following expressions are developed for this state:

$$v_{L1} = V_i \tag{2.156}$$

$$v_{L2} = V_i + v_{c1} - v_{c2} - v_{c3} \tag{2.157}$$

$$v_{L3} = v_{c1} + V_i - V_o \tag{2.158}$$

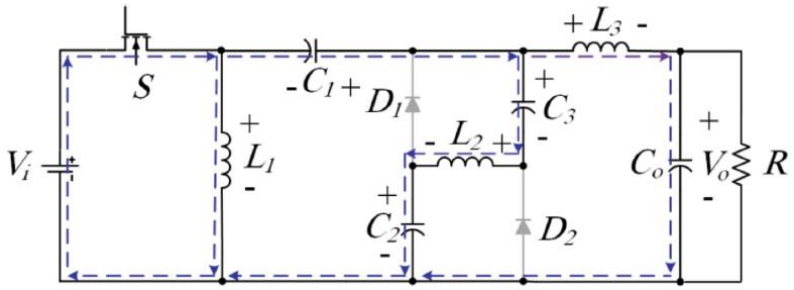

Figure 2.66: Mode 1 operation

In the second mode which last for the time interval of $(1\text{-}D)T_s$, the switch is gated on, the diodes D1 and D2 becomes reverse biased because of the negative source voltage across its terminal. The following expressions are developed for this state:

$$v_{L1} = v_{c2} - v_{c1} \tag{2.159}$$

$$v_{L2} = -v_{c2} = -v_{c3} \tag{2.160}$$

$$v_{L3} = v_{c3} - V_o \tag{2.161}$$

Voltage gain is given by:

$$G = \frac{2D}{1-D} \tag{2.162}$$

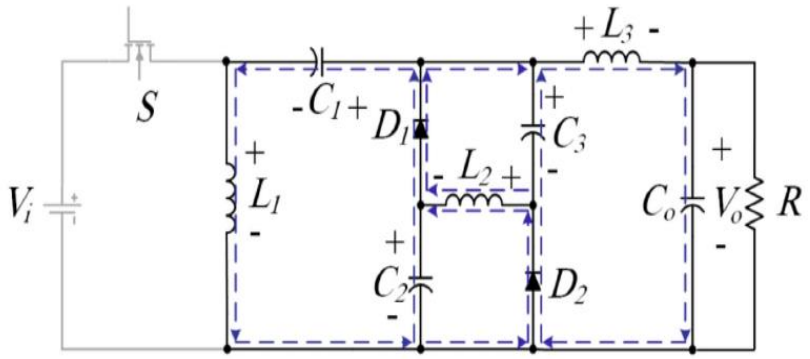

Figure 2.67: Mode 2 operation

2.8 Cuk Topology

The power circuit of the Cuk converter is shown by Figure 2.68. The Cuk converter has the buck-boost functionality and its most applied in controlled dc supplies. The power circuit is composed one power switch, one inductor, one capacitor, one diode and an output filter. Apart from buck-boost functionality, the Cuk converter is able to provide output voltage with inversed characteristics. The voltage gain or transfer ratio is given by:

$$G = \frac{D}{1-D} \tag{2.163}$$

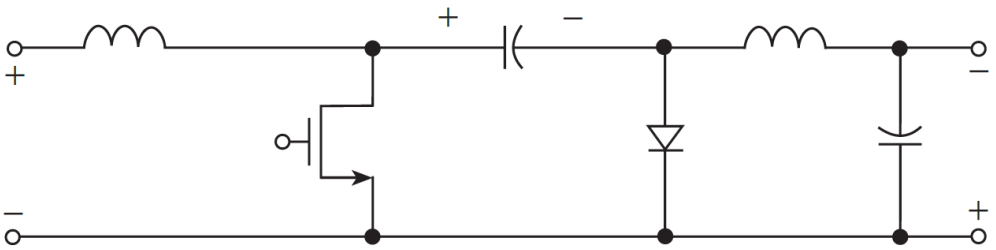

Figure 2.68: Cuk Converter

There are two states of operations of the Cuk converter, the first state or mode is when the power switch is closed and the second mode is when the power switch is off. In one period or cycle, the switch is opened for a specific duration and turned off for the remaining duration thus the on and off periods are determined by the duty cycle. Analysis of the operating is for CCM mode

which simply means that inductor current doesn't fall to zero during the period of operation. The following expressions are developed during the operations of the Cuk converter in CCM mode.

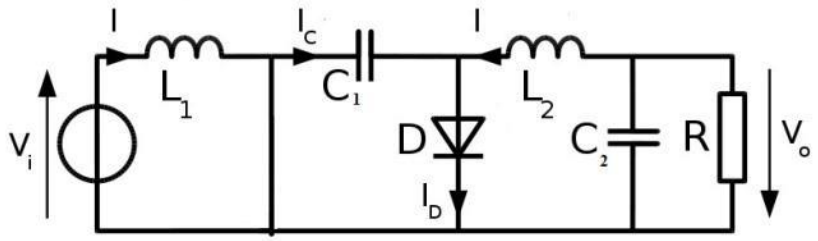

Figure 2.69: Mode 1 operating state

$$\frac{di_{L1}}{dt} = \frac{v_i}{L_i} \tag{2.164}$$

$$\frac{dv_{c1}}{dt} = \frac{i_{L2}}{c_1} \tag{2.165}$$

$$\frac{di_{L2}}{dt} = \frac{(v_{c1} - v_o)}{L_2} \tag{2.166}$$

$$\frac{dv_o}{dt} = \frac{1}{C_o}(i_{L2} - \frac{V_o}{R}) \tag{2.167}$$

$$i_{s1} = i_{L1} + i_{L2} \tag{2.168}$$

In the second state of Figure 2.70 when the switch is opened and the diode is forward biased, the following expressions are produced:

$$\frac{di_{L1}}{dt} = \frac{v_i - v_c}{L_1} \tag{2.169}$$

$$\frac{dv_c}{dt} = \frac{i_{L1}}{C} \tag{2.170}$$

$$\frac{di_{L2}}{dt} = -\frac{v_o}{L_2} \tag{2.171}$$

$$\frac{dv_o}{dt} = \frac{1}{C}\left(i_{L2} - \frac{V_o}{R}\right) \tag{2.172}$$

$$i_{D1} = i_{L1} + i_{L2} \tag{2.173}$$

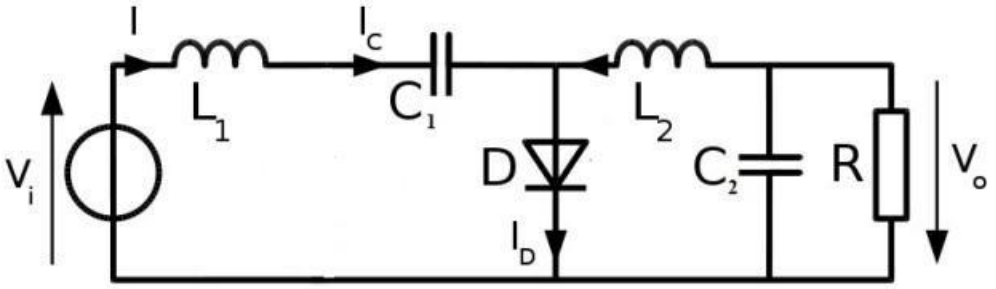

Figure 2.70: Mode 2 operating state

Three state of operation exist for the DCM mode. These state of operations are represented below.

State 1: Power switch is on; diode is reverse biased

State 2: Power switch is off, diode is forward biased

State 3: Power switch off, diode is reverse biased

State 1 expressions:

$$\frac{di_{L1}}{dt} = \frac{v_i}{L1} \tag{2.174}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L2}}{C_1} \tag{2.175}$$

$$\frac{di_{L2}}{dt} = \frac{v_{C1}}{L2} - \frac{v_o}{L2} \tag{2.176}$$

$$\frac{dv_o}{dt} = \frac{i_{L2}}{C_o} = \frac{v_o}{C_o R} \tag{2.177}$$

$$i_{s1} = i_{L1} + i_{L2} \tag{2.178}$$

State 2 expressions:

$$\frac{di_{L1}}{dt} = v_i - \frac{v_{C1}}{L_1} \tag{2.179}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1} \tag{2.180}$$

$$\frac{di_{L2}}{dt} = -\frac{v_o}{L_2} \tag{2.181}$$

$$\frac{dv_O}{dt} = \frac{1}{C_o}\left(i_{L2} - \frac{v_o}{R}\right) \tag{2.182}$$

$$i_{D1} = i_{L1} + i_{L2} \tag{2.183}$$

State 3 expressions:

$$i_{L1} = i_{L2} \tag{2.184}$$

$$v_{L1} + v_{L2} = v_i + v_o + v_{c1} \tag{2.185}$$

2.9 Selected Cuk Topologies

Static high gain Cuk converter is presented in (De Souza et al., 2015). This topology of converter has the characteristics of current for the input and output sections and also allows the integration of second stage section with more components. Its suitable for application in grid-tied or connected systems and also for photovoltaic systems. Multiple control techniques have been proposed for the control of these types of converter (Axelrod et al., 2008; Li & He, 2011; Meneses et al., 2013; Pop-Calimanu et al., 2019; Prudente et al., 2008; Tang et al., 2015; Yang et al., 2009; Zhou et al., 1999). Figure 2.71 shows the power circuit of the presented of topology which is made up of the following components: two inductors, one switch, three capacitors and

three diodes and an output filter. There are two stages of operation of this converter which are presented by Figure 2.72 and Figure 2.73.

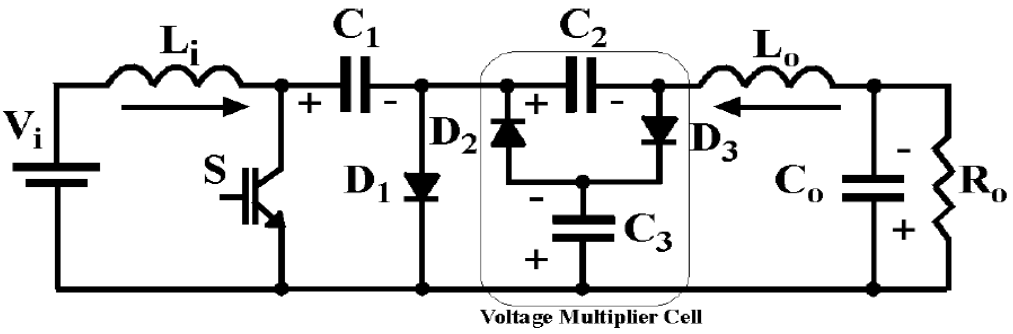

Figure 2.71: High gain Cuk converter

In the first state of operation, the switch is off and diode D_2 is reverse biased, the capacitor obtains energy from the inductor, the output inductor serves as a freewheeling device for this section. The function of the inductor L_s is a resonant tank thus the energy transfer involving this inductor is a resonant energy transfer.

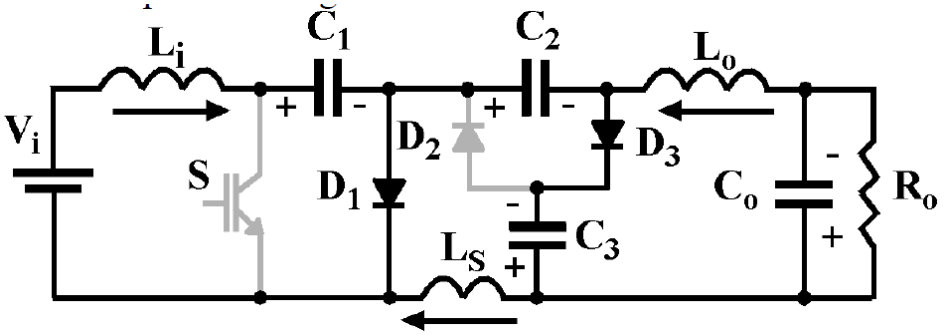

Figure 2.72: First mode of operation

In the second state of operation shown by Figure 2.73, the switch is gated on whiles diodes D_1 and D_3 are reverse biased. During this mode of operation, the energy stored by capacitor C_1 is transferred to capacitor C_3 whiles the inductor L_i charges during this period.

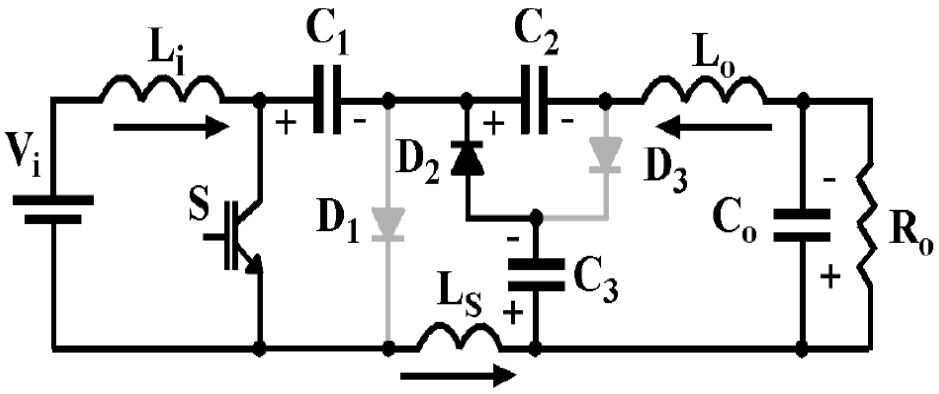

Figure 2.73: Second mode of operation

The capacitor voltages are determined by:

$$V_{C1,C2,C3} = V_i \frac{1}{1-D} \tag{2.186}$$

The converter gain G is expressed below where n is the number of stages in the converter

$$G = \frac{n+D}{1-D} \tag{2.187}$$

A new topology of hybrid Cuk converter (Pop-Calimanu et al., 2019) is reviewed in this section. This novel converter boast of the following advantages:

- Inverse output voltage polarity
- Buck-boost capabilities
- Wide range conversion ratio.

The power circuit is shown by Figure 2.74. It is composed of three diodes, two inductors, one power switch, one capacitor and an output filter. The simplified circuit of the presented converter is shown below.

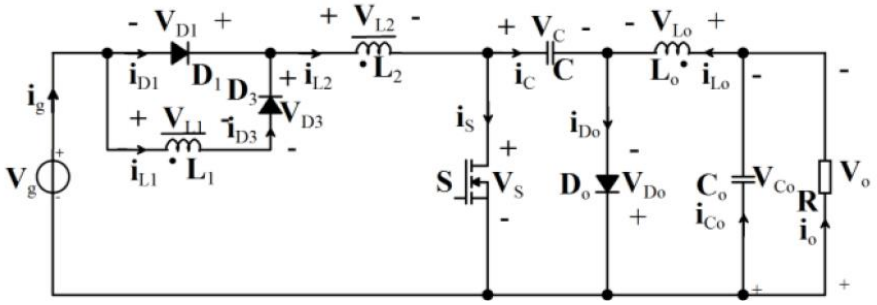

Figure 2.74: Hybrid cuk converter

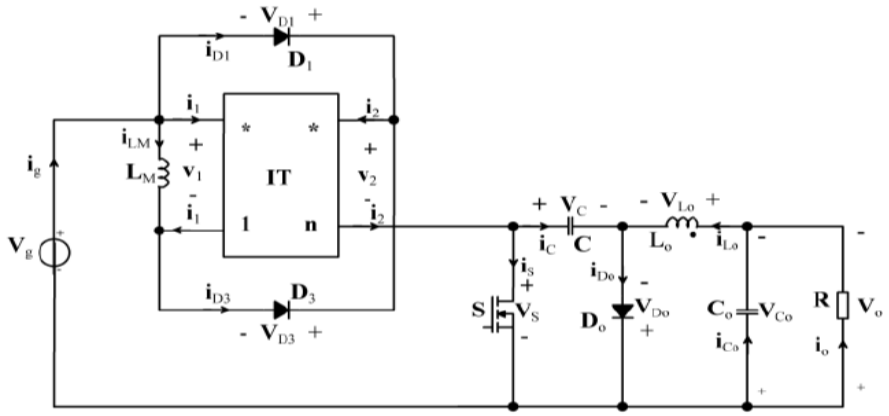

Figure 2.75: Simplified topology

The hybrid cuk converter also has two states of operations; in the first state, the power switch is gated on whiles its gated off in the second state. The voltage conversion ratio is expressed below as:

$$M = \frac{D^2+nD}{n-nD} \tag{2.188}$$

A self-lift cuk converter (Zhu & Luo, 2009) is reviewed in this section. This converter employs the voltage lift methodology in the design of a new cuk converter. The new VL Cuk converter when compared to the conventional Cuk converter provides the following merits higher boosting gain, positive output voltage, negative output voltage, reduced component count, reduced output ripples. Below is the proposed self-lift converter and its modes of operation, a)

is the power circuit, b) is the mode of operation when the switch is on, c) mode of operation when the power switch is gated of and d) DMC mode of operation.

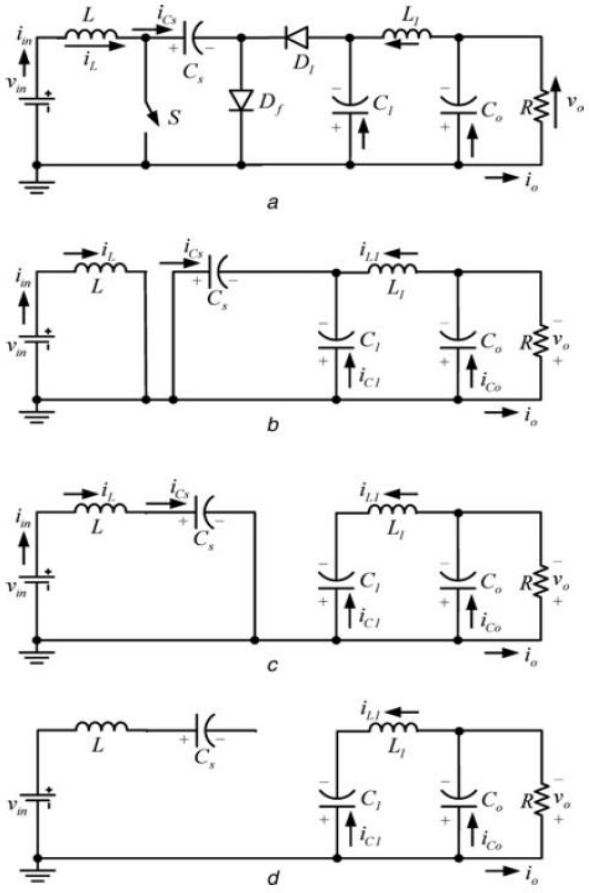

Figure 2.76: Self-lift Cuk converter

2.10 Control strategies of TB

In a broader perspective, there are several topologies of multi-input converter. these type of converter seeks to employ different and multiple dc sources as the input of the converter. This makes it suitable to harness variety of energy sources especially from renewable energy (Blaabjerg et al., 2004; González et al., 2007; Jain & Agarwal, 2007; Xue, Chang, et al., 2004; Yang et al., 2009). Basically multi-input converters provide hybridization of energy sources thereby increasing efficiency, reliability and reducing losses. Advantages of the multi-input converter is reliability of the source because in the absence or failure of one source, the others

will function without difficulty. A multi-input converter basically is a converter with multiple dc voltage sources at the input. The converter input/source can be arranged in series or parallel as desired by the designer. Various research into the application of multi-input converter can be found as follows:

PV-Wind (Crescimbini et al., 1996; Solero et al., 1996).

PV-Utility (Kobayashi et al., 2006; Matsuo et al., 2004).

Hybrid Vehicle (Di Napoli et al., 2002; Jain & Agarwal, 2007).

Other applications (Benavides & Chapman, 2005; Chen et al., 2006; Chiu et al., 2005; Dobbs & Chapman, 2003).

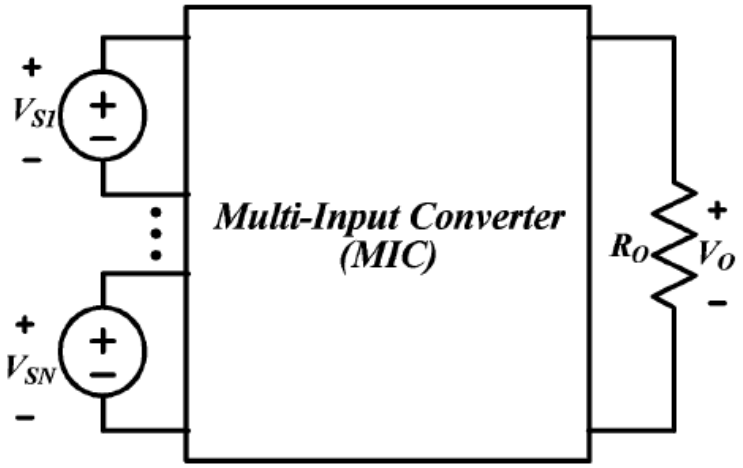

Figure 2.77: General structure of multi-input converter

Some examples of multi-input converters for dc-dc applications can be found in the following published literatures (Dobbs & Chapman, 2003; Kwasinski, 2009; Liu & Chen, 2009).

2.11 Conclusion

Review of dc-dc converters was investigated in this section of my research/thesis. Selected topologies were extensively reviewed with respect to the categorization of dc-dc converters, the modes of operation and also the type of conduction i.e. CCM or DCM with respect to the inductor current, various mathematical expressions were reviewed for the various modes of operation, finally the applications areas of the selected topologies were reviewed. Emphasis was placed on the following selected topologies:

- Buck Topology
- Boost Topology
- Buck-Boost Topology
- Cuk Topology
- Multi-input Topology

CHAPTER 3
PRESENTED CONVERTER AND SIMULATION RESULTS

3.1 Introduction

DC-DC converters have long been in existence and are considered as the pioneer and simplest power electronic conditioning device. They are used in almost all sectors of human life such as power supply systems, communication establishments, military, academia, health services, transportation systems (air, sea and land) and electronic devices (mobile phones, laptops and computers) and wielding and plating. DC-DC converters can also be utilized as an isolation device when a transformer coupled to the converter (Solero et al., 2005).

Multi-input converter seeks to employ different and multiple dc sources as the input of the converter and this makes it suitable to harness variety of energy resources especially from renewable energy. A multi-input converter basically is a converter with multiple dc voltage sources at the input. Primarily, multi-input converters provide hybridization of energy sources thereby increasing efficiency, reliability and reducing losses. Advantages of the multi-input converter is a high reliability of the source, this is because in the absence or failure of one source, the others will function without difficulty.

3.2 Presented Converter

The presented converter topology for investigations is the multi-input dc-dc converter represented by Figure 3.1. The circuit is composed of multi-input voltages with corresponding unidirectional switches, two diodes and an output *LC* filter. From the power circuit, the following parameters are defined as:

- Input current i is expressed by $i = 1, 2, 3, 4 \ldots$
- The input voltage is V_i
- The inductor current is i_L
- Inductor voltage is v_L

- Capacitor voltage is v_C
- Input and output voltage and current is given by V_o and I_o accordingly
- The switch number is S_i

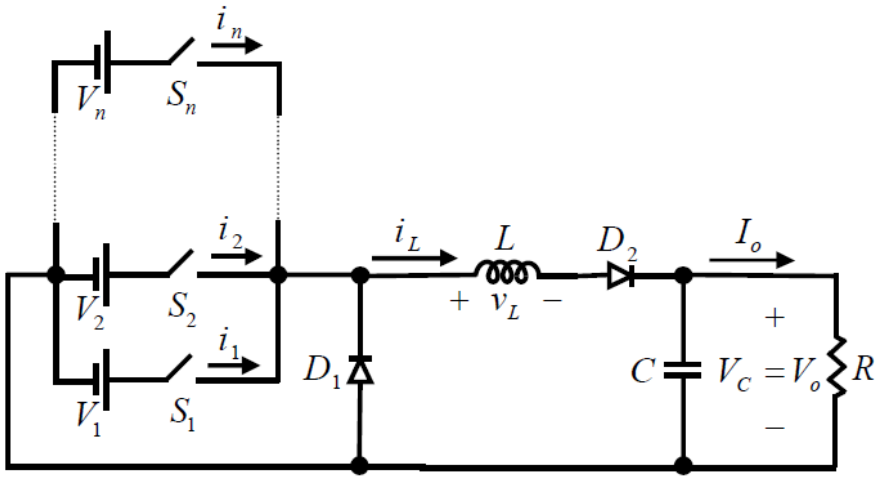

Figure 3.1: Multi-input dc-dc converter

Analysis of the presented converter will be investigated using Figure 3.2 where two voltage sources are applied. The corresponding switching waveform is given Figure 3.3 where the periods of switching for switches S_1 and S_2 are indicated. One period of conduction is segmented into three parts:

$$\begin{cases} 0 \le t \le D_1 T \\ D_1 T \le t \le D_2 T \\ D_2 T \le t \le T \end{cases} \tag{3.1}$$

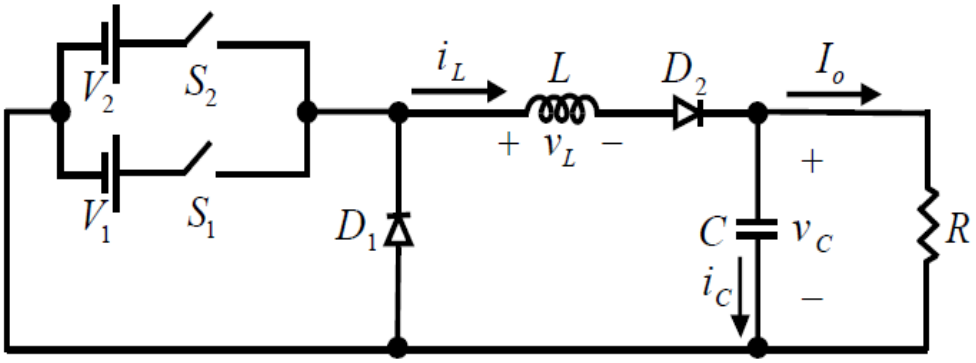

Figure 3.2: Two voltage multi-input converter

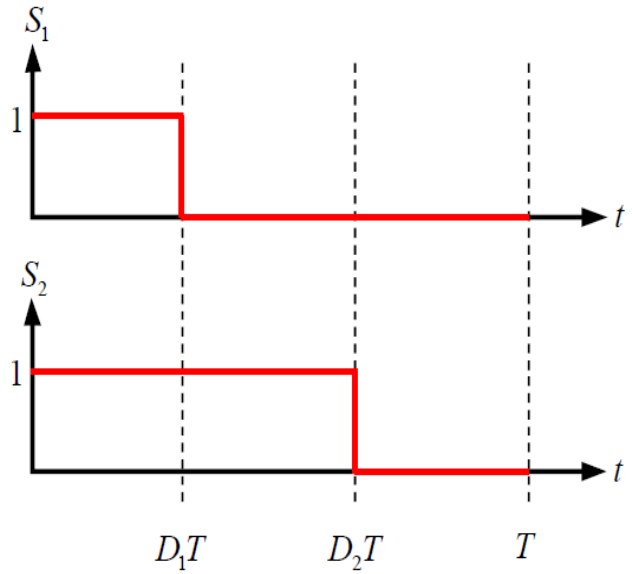

Figure 3.3: Switching waveform

The switching waveform for the two switches of Figure 3.2 is illustrated by Figure 3.3. the first switch S_1 is turned on for the period $0 \leq t \leq D_1T$ and is turned on for the remaining period of $D_1T \leq t \leq D_2T$ and $D_2T \leq t \leq T$. The second switch S_2 performs the opposite switching states of the first switch in terms of duration of switching. S2 is switched on for the period of $0 \leq t \leq D_1T$ and $D_1T \leq t \leq D_2T$ and it's switched off for the remaining period $D_2T \leq t \leq T$.

$0 \leq t \leq D_1T$ Switching state:

In this state, the required energy is obtained when switch S_1 is switched on (as shown by Figure 3.34) and the input voltage is given by $V_1 > V_2$ and the inductor voltage is given by $V_1 - V_o > 0$. Positive voltage will be supplied to the load. There is a linear exponential increase of the inductor current (I_{LV1}) and its magnitude is less than the load current hence the capacitor provides energy in the time interval ($0 \leq t \leq t_1$). However, during the period of ($t_1 \leq t \leq D_1T$), the capacitor discharges its voltage and the inductor current is also less. All these waveform characteristics are represented in Figure 3.7.

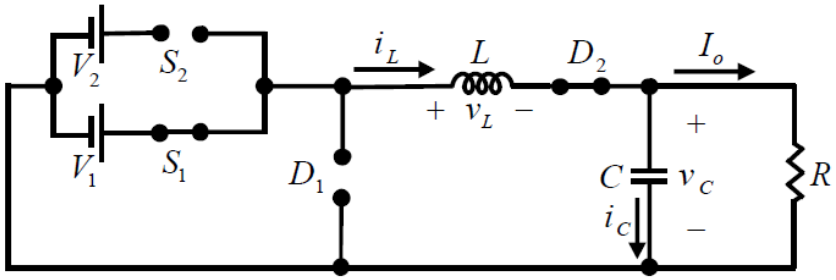

Figure 3.4: Switch S_1 closed

$D_1T \leq t \leq D_2T$ Switching state:

In this state, switch S2 is closed whiles switch S1 and diode D1 are in no-conducting state. The circuit equivalence of this state is indicated by Figure 3.5. The inductor voltage is expressed as $V_2 - V_0$. Also there is a linear increase in the inductor current from I_{LP1} and I_{LP2}, similarly the capacitor current increases from $I_{LP1} - I_O$ to $I_{LP2} - I_O$. The inductor current is greater than the load current during this state of operation. The capacitor voltage increases or the capacitor charges in this state of operation. All these waveform characteristics are represented in Figure 3.7.

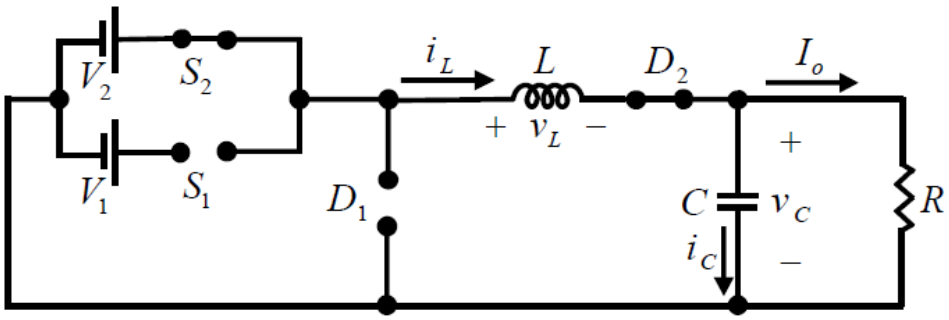

Figure 3.5: Switch S_2 closed

$D_1T \leq t \leq D_2T$ Switching state:

In this state or time interval, the switches are opened whiles diodes D_1 and D_2 are forward biased. Applying KVL to the circuit will produce the expression below where v_{D1} is the voltage across the diode D_1. This diode (D_1) conducts because of the positive voltage place across it. Both the inductor and capacitor currents decrease linearly to I_{LV} and $I_{LV} - I_O$ respectively. The inductor current is greater than the load current for the interval $D_2T \leq t \leq t_2$. All these waveform characteristics are represented in Figure 3.7.

$$v_{D1} = -L\frac{di_L}{dt} - V_o$$

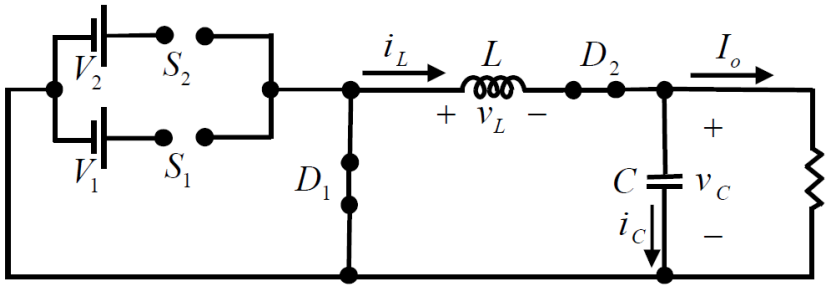

Figure 3.6: Diode D_1 is forward biased

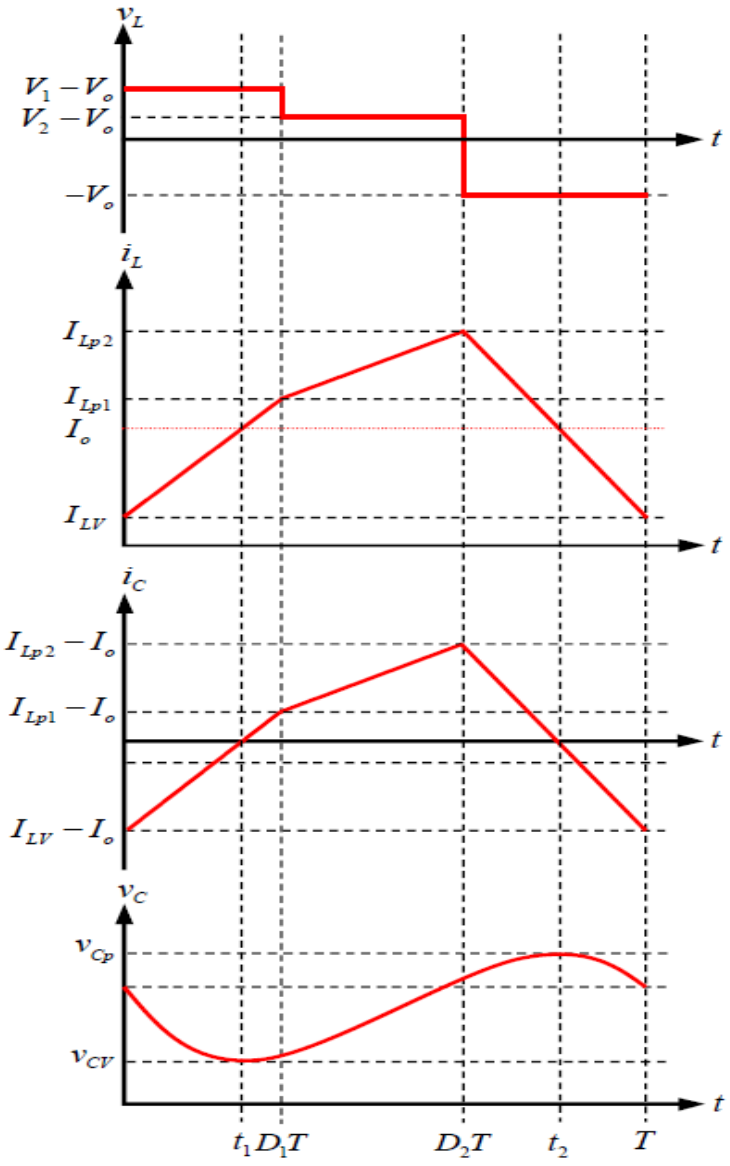

Figure 3.7: Voltage and current waveforms

Analysis of the presented topology during CCM mode of operation is provided below where critical values of voltages and currents provided theoretically. The input voltages are different in terms of magnitude V_1 is greater than V_2 and there's a 2% difference between them.

The period and frequency relates by:

$$T = \frac{1}{f} \tag{3.2}$$

Applying KCL during the period of $0 \leq t \leq D_1 T$

$$i_C = i_L - I_O \tag{3.3}$$

Inductor voltage:

$$v_L = L\frac{di_L}{dt} \tag{3.4}$$

The inductor for the time interval $0 \leq t \leq D_1 T$:

$$v_{L1} = V_1 - V_o \tag{3.5}$$

It implies the corresponding inductor current and capacitor current are given by:

$$i_{L1} = \frac{V_1 - V_0}{L} t + I_{LV} \tag{3.6}$$

$$i_{C1} = \frac{V_1 - V_O}{L} t + (I_{LV} - I_O) \tag{3.7}$$

During $D_1 T \leq t \leq D_2 T$, the following expressions are developed:

$$v_{L2} = V_2 - V_O \tag{3.8}$$

$$i_{L2} = \frac{V_2 - V_O}{L} t + I_{LP1} \tag{3.9}$$

$$i_{C2} = \frac{V_2 - V_O}{L} t + (I_{LP1} - I_O) \tag{3.10}$$

During $D_2 T \leq t \leq T$, the following expressions are developed:

$$v_{L3} = -V_O \tag{3.11}$$

$$i_{L3} = \frac{-V_O}{L}t + I_{LP2} \tag{3.12}$$

$$i_{C3} = \frac{-V_O}{L}t + (I_{LP2} - I_O) \tag{3.13}$$

$$I_{LP1} = (D_1 T + I_{LV})\frac{V_1 - V_0}{L}$$

$$I_{LP2} = I_{LP1} + (D_2 - D_1)T(\frac{V_2 - V_0}{L}) \tag{3.14}$$

$$I_0 = \frac{V_0}{R} \tag{3.15}$$

$$L_C = \frac{R}{2f}\left[(-D_1^2 + 2D_1)\frac{V_1}{V_0} + (-D_2^2 + D_1^2 - 2D_1 + 2D_2\frac{V_2}{V_0} - 1\right] \tag{3.16}$$

$$V_0 = D_1 V_1 + V_2(D_2 - D_1) \tag{3.17}$$

When the number of dc sources (V_1, V_2 *and* V_3) is increased to three, the power circuit is presented below in Figure 3.8. The power switches also increases to three (S_1, S_2 *and* S_3).

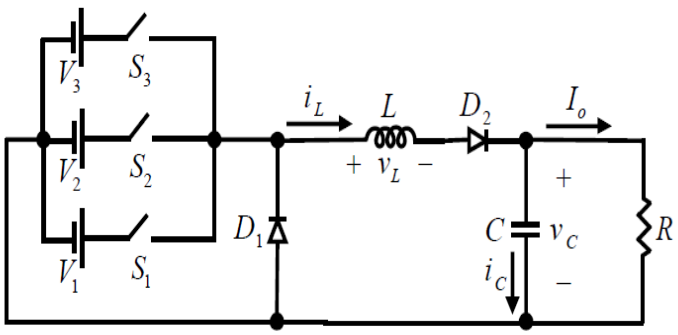

Figure 3.8: Three dc source dc-dc converter

The mode of operation of this converter is represented by Figure 3.9 to Figure 3.12. These figures correspond to the following modes of time intervals $0 \leq t < D_1T$, $D_1T \leq t < D_2T$, $D_2T \leq t < D_3T$, $D_3T \leq t < T$ accordingly. The voltage and current waveforms are given by Figure 3.13.

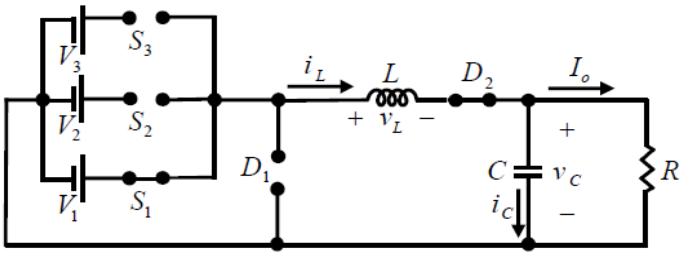

Figure 3.9: $0 \leq t < D_1T$

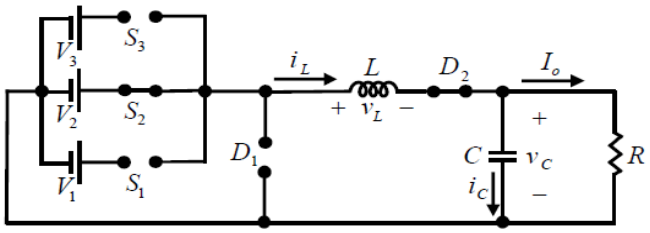

Figure 3.10: $D_1T \leq t < D_2T$

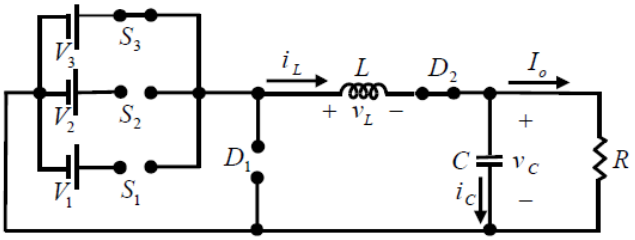

Figure 3.11: $D_2T \leq t < D_3T$

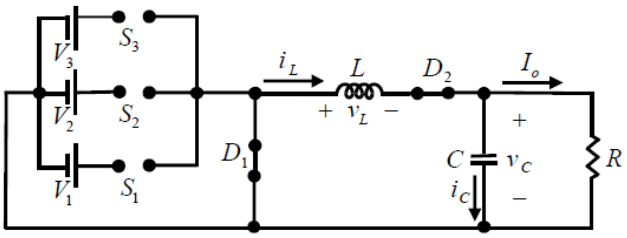

Figure 3.12: $D_3T \leq t < T$

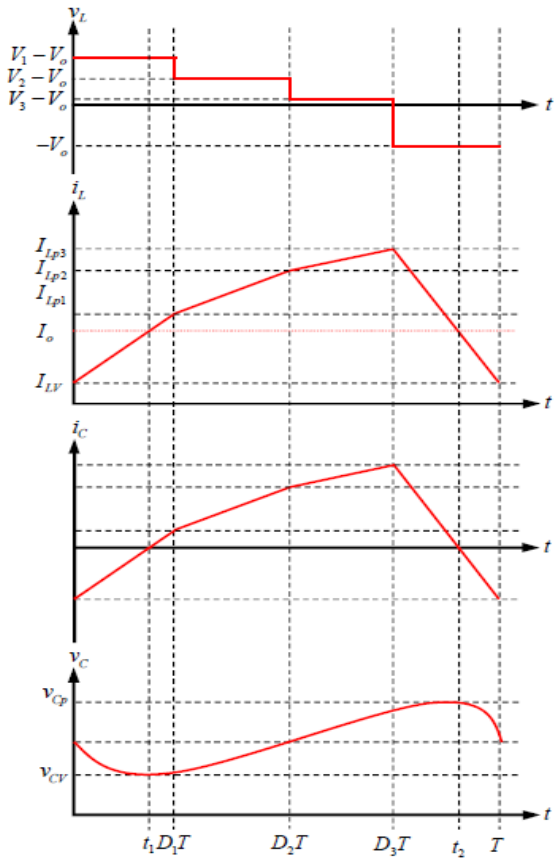

Figure 3.13: Voltage and current waveforms

Mathematical analysis of this circuit is similar to the case study of two dc sources, KVL and KCL is utilized to produce the desired equations. Only the fourth parameter equations are developed in this section:

$$T = \frac{1}{f} \tag{3.18}$$

Applying KCL during the period of $0 \leq t \leq D_1 T$

$$i_C = i_L - I_O \tag{3.19}$$

Inductor voltage:

$$v_L = L\frac{di_L}{dt} \tag{3.20}$$

The inductor for the time interval $0 \leq t \leq D_1 T$:

$$v_{L1} = V_1 - V_o \tag{3.21}$$

It implies the corresponding inductor current and capacitor current are given by:

$$i_{L1} = \frac{V_1 - V_0}{L} t + I_{LV} \tag{3.22}$$

$$i_{C1} = \frac{V_1 - V_O}{L} t + (I_{LV} - I_O) \tag{3.23}$$

During $D_1 T \leq t \leq D_2 T$, the following expressions are developed:

$$v_{L2} = V_2 - V_O \tag{3.24}$$

$$i_{L2} = \frac{V_2 - V_O}{L} t + I_{LP1} \tag{3.25}$$

$$i_{C2} = \frac{V_2 - V_O}{L} t + (I_{LP1} - I_O) \tag{3.26}$$

During $D_2 T \leq t \leq T$, the following expressions are developed:

$$v_{L3} = -V_O \tag{3.27}$$

$$i_{L3} = \frac{-V_O}{L} t + I_{LP2} \tag{3.28}$$

$$i_{C3} = \frac{-V_O}{L} t + (I_{LP2} - I_O) \tag{3.29}$$

$$I_{LP1} = (D_1 T + I_{LV}) \frac{V_1 - V_0}{L}$$

$$I_{LP2} = I_{LP1} + (D_2 - D_1) T (\frac{V_2 - V_0}{L}) \tag{3.30}$$

$$I_0 = \frac{V_0}{R} \tag{3.31}$$

$$L_C = \frac{R}{2f} \left[(-D_1^2 + 2D_1) \frac{V_1}{V_0} + (-D_2^2 + D_1^2 - 2D_1 + 2D_2 \frac{V_2}{V_0} - 1 \right] \tag{3.32}$$

$$V_0 = D_1 V_1 + V_2 (D_2 - D_1) \tag{3.33}$$

Similarly, when the dc sources are increased to four, the power circuit is indicated by Figure 3. 14.

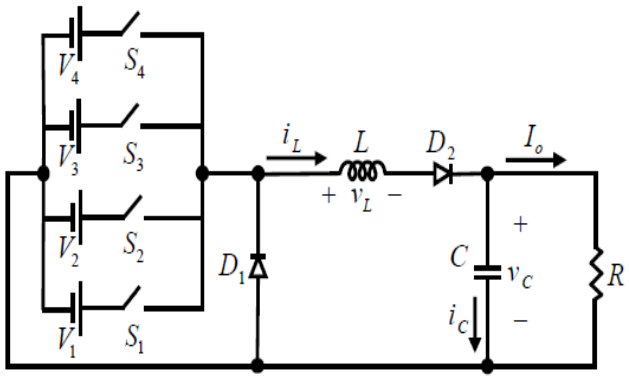

Figure 3.14: Four dc source dc-dc converter

The corresponding equivalent circuits for the sates of operations are indicated by Figure 3.15 to Figure 3.19. These states occur during $0 \leq t < D_1T$, $D_1T \leq t < D_2T$, $D_2T \leq t < D_3T$, $D_3T \leq t < D_2T$, $D_4T \leq t < T$ respectively.

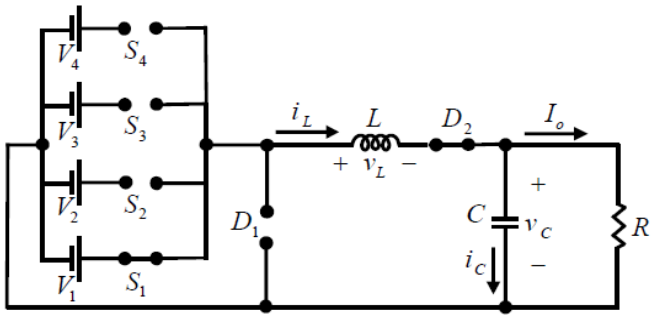

Figure 3.15: $0 \leq t < D_1T$

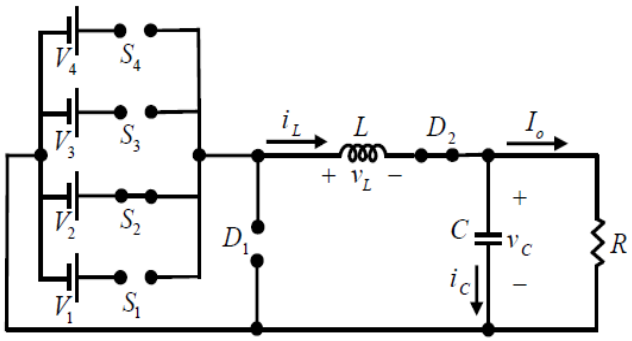

Figure 3.16: $D_1T \leq t < D_2T$

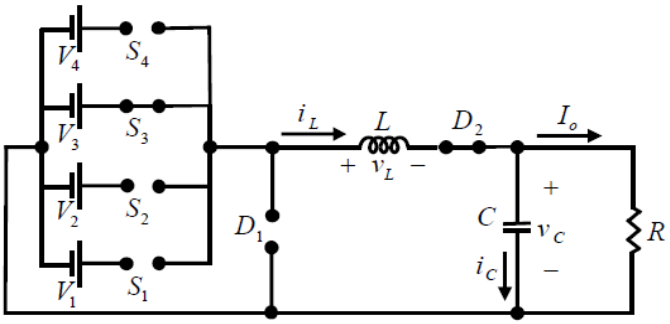

Figure 3.17: $D_2T \leq t < D_3T$

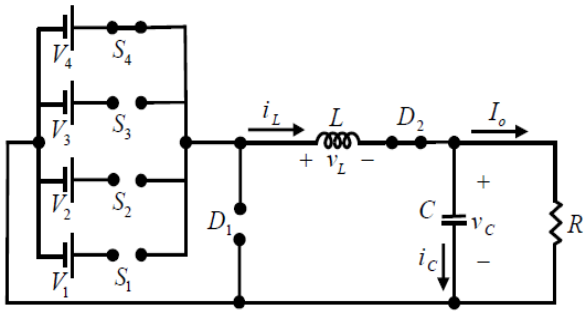

Figure 3.18: $D_3T \leq t < D_4T$

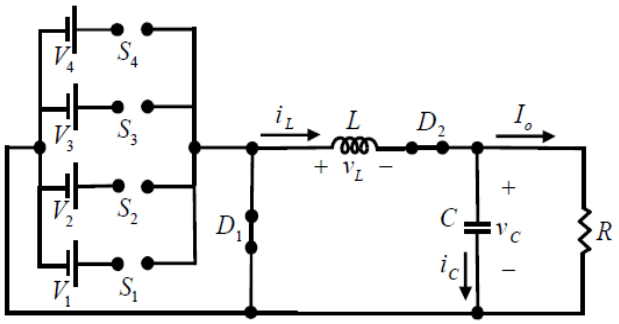

Figure 3.19: $D_4T \leq t < T$

The voltage and current waveforms are given by Figure 3.20.

$$V_{L4} = -V_0 \tag{3.34}$$

$$i_{L4} = \frac{-V_o}{L}t + (I_{LP3} - I_0) \tag{3.35}$$

$$i_{C4} = \frac{-V_0}{L}t + (I_{LP3} - I_0) \tag{3.36}$$

$$L_C = \frac{R}{2f}\left[(-D_1^2 + 2D_1)\frac{V_1}{V_0} + (-D_2^2 + D_1^2 - 2D_1 + 2D_2\frac{V_2}{V_0}) + (D_2^2 - D_3^2 - 2D_2 + 2D_3\left(\frac{V_3}{V_0}\right) - 1\right] \tag{3.37}$$

$$V_0 = D_1V_1 + V_2(D_2 - D_1) + (D_3 - D_2)V_3 \tag{3.38}$$

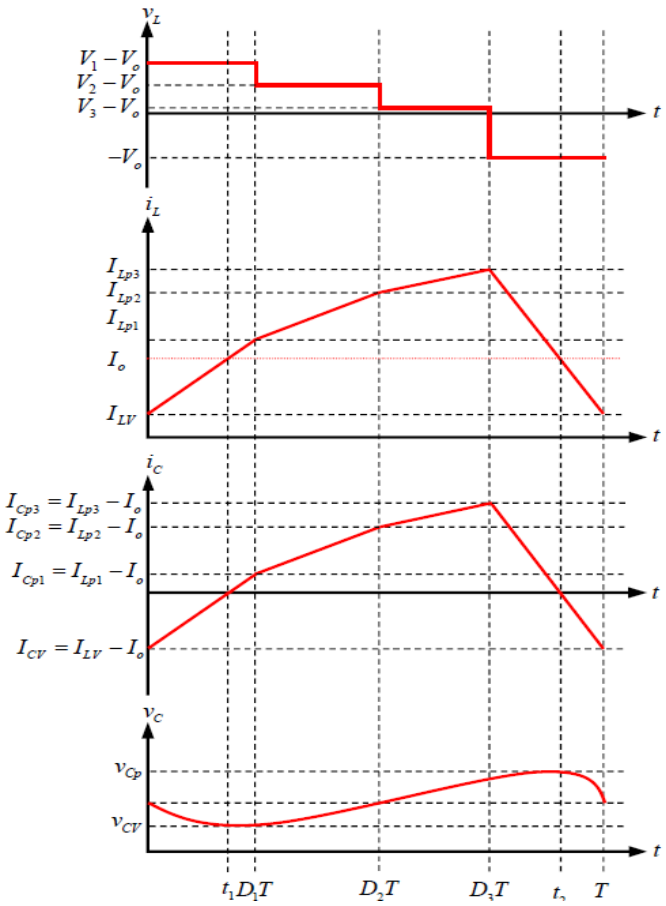

Figure 3.20: Voltage and current waveforms

3.3 Simulation Results

Simulation results for the presented multi-input dc-dc converter is produced by building the various topologies in PSCAD software. Simulation results are produced for three case scenarios when the input voltage is two (V_1 *and* V_2), when the input voltage is three (V_1, V_2 *and* V_3) and finally when the input voltage is four (V_1, V_2, V_3, *and* V_4). The structure of the circuit remains the same in all cases however, the component number is increased; the number of dc sources and the power switches increases together. Furthermore, the load power is the same in all the cases as 9 Watts. The values of the various components utilized in generating the output

waveforms are indicated in tables below where Table 3.1 corresponds to a two input converter, Table 3.2 corresponds a three input converter and Table 3.3 corresponds to a five input converter. The critical inductance (L_C) values are determined with respect to the number of applied dc sources.

Table 3.1: Two inputs converter simulation parameters

Component	Value
First voltage value V_1	$10V$
Second voltage value V_2	$7V$
Switching frequency f	$50kHz$
Load resistance R_L	5Ω
Filter capacitance C	$680\mu F$
Switch S_1 duty cycle D_1	0.5
Switch S_2 duty cycle D_2	0.7

Table 3.2: Three inputs converter simulation parameters

Component	Value
First voltage value V_1	$10V$
Second voltage value V_2	$9V$
Third voltage value V_3	$8V$
Switching frequency f	$50kHz$
Load resistance R_L	5Ω
Filter capacitance C	$680\mu F$
Switch S_1 duty cycle D_1	0.5
Switch S_2 duty cycle D_2	0.6
Switch S_3 duty cycle D_3	0.7

Table 3.3: Five inputs converter simulation parameters

Component	Value
First voltage value V_1	$10V$
Second voltage value V_2	$9V$
Third voltage value V_3	$8V$
Fourth voltage value V_4	$7V$
Fifth voltage value V_5	$6V$
Switching frequency f	$50kHz$
Load resistance R_L	5Ω
Filter capacitance C	$680\mu F$
Switch S_1 duty cycle D_1	0.4
Switch S_2 duty cycle D_2	0.5
Switch S_3 duty cycle D_3	0.6
Switch S_4 duty cycle D_4	0.7
Switch S_5 duty cycle D_5	0.8

The output waveforms of Figure 3.21 to Figure 3.25 are the applied waveforms of the two input converter and are generated by utilizing the parameters of Table 3.1. The waveforms of the input voltages are illustrated by Figure 3.21. the values of these inputs are $V_1 = 10V \; and \; V_2 = 7V$.

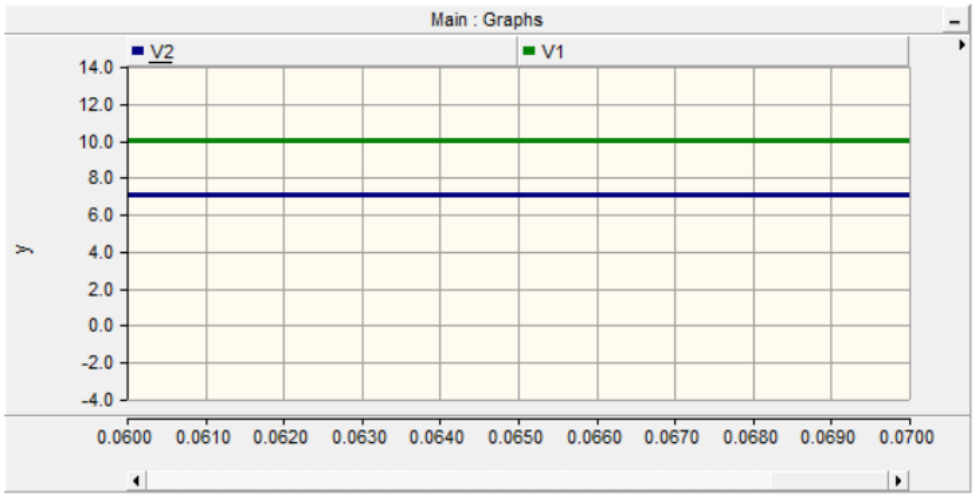

Figure 3.21: Input dc voltages

The inductor and capacitor current waveforms are illustrated by Figure 3.22 and Figure 3.23 respectively. The nature of these waveforms corresponds the theoretically presented waveforms. The inductor current alternates only in the positive polarity region of the graph whiles the capacitor current alternates in both polarity regions of the graph.

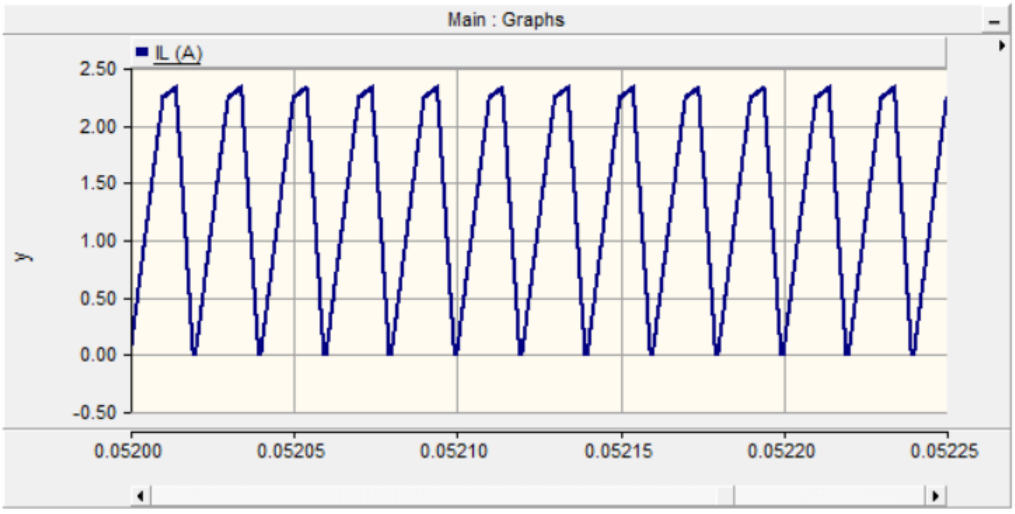

Figure 3.22: Inductor current waveform

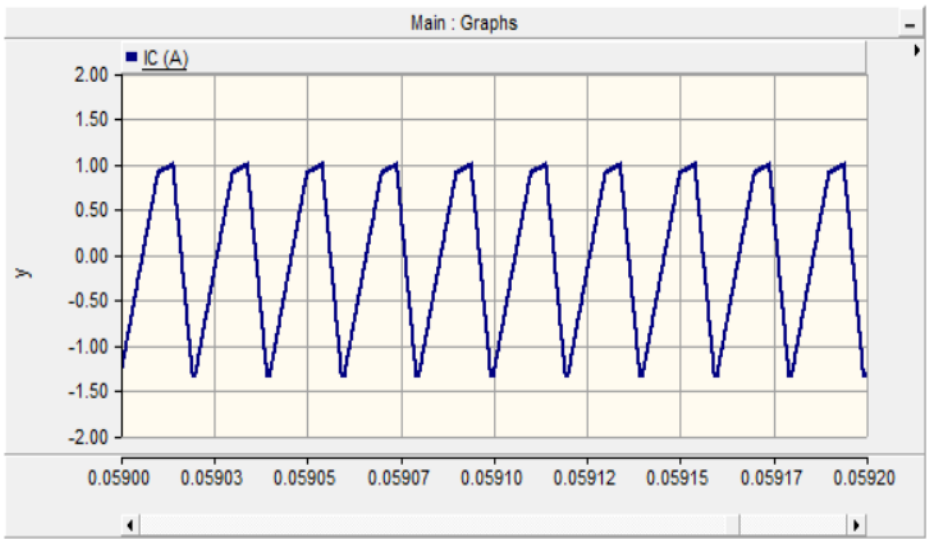

Figure 3.23: Capacitor current waveform

The load current and load voltage waveforms are illustrated by Figure 3.24 and Figure 3.25. The presented waveforms occur during the steady states of the converter operation. The magnitude the load current and load voltage are $i_o = 1.4A$ and $V_0 = 7V$ respectively.

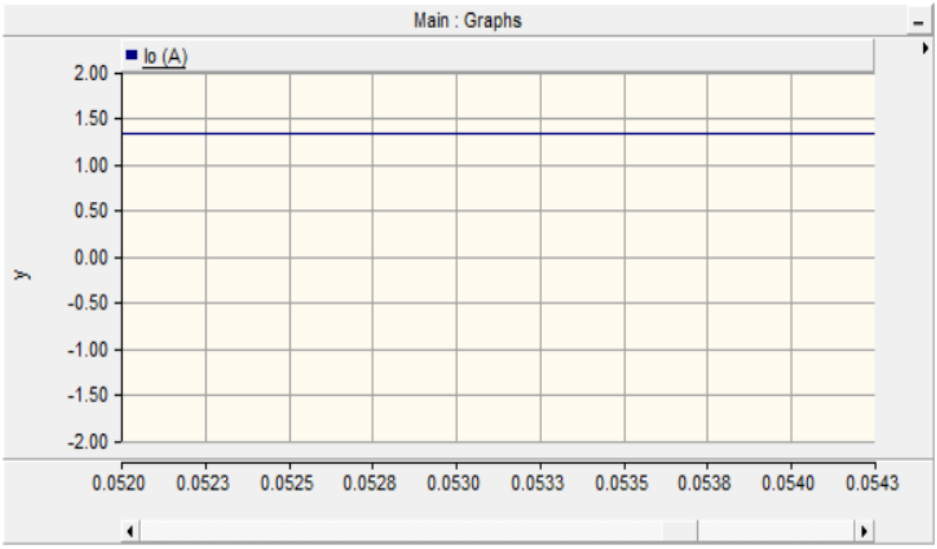

Figure 3.24: Load current waveform

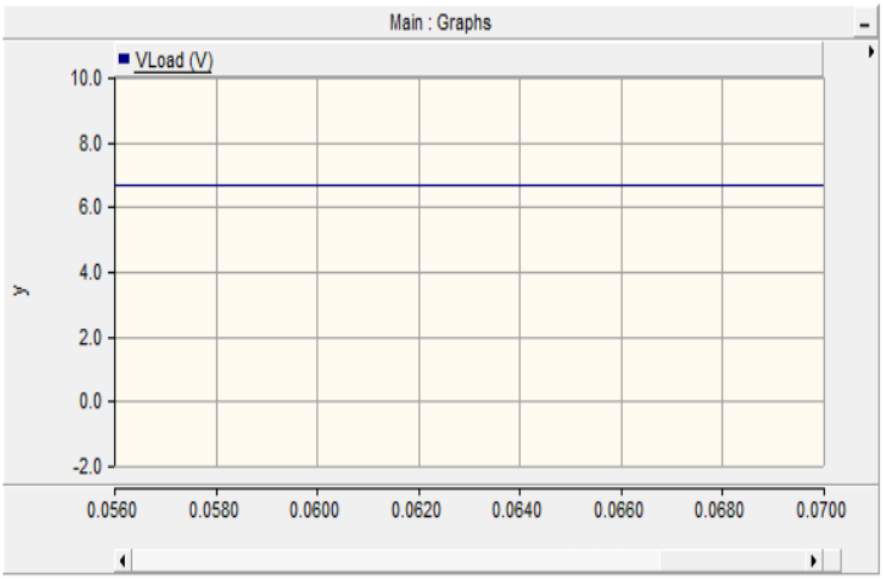

Figure 3.25: Load voltage waveform

The output waveforms of Figure 3.26 to Figure 3.31 are the applied waveforms of the three input converter and are generated by utilizing the parameters of Table 3.2.

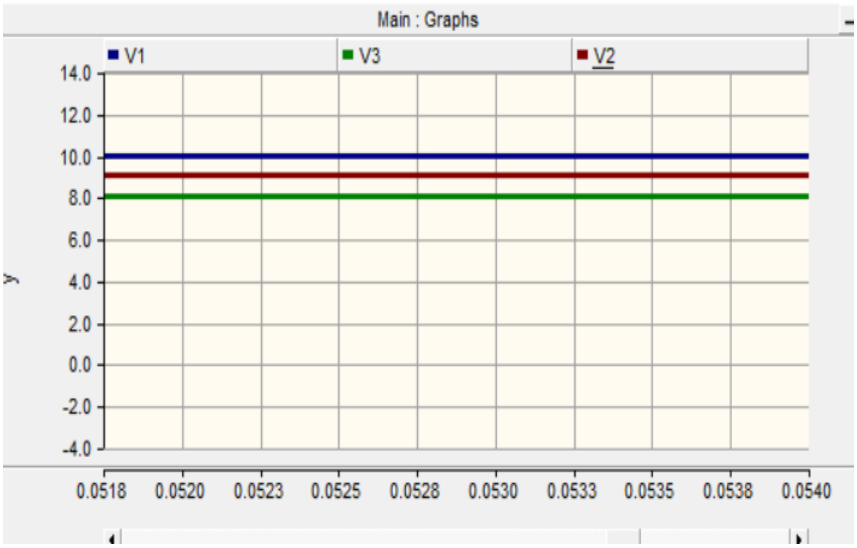

Figure 3.26: Input dc voltages

The waveforms of the input voltages are illustrated by Figure 3.26. the values of these inputs are $V_1 = 10V, V_2 = 9V \; and \; V_3 = 8V$. The capacitor and inductor current waveforms are illustrated by Figure 3.27 and Figure 3.28 respectively. The nature of these waveforms corresponds the theoretically presented waveforms. The inductor current alternates only in the positive polarity region of the graph whiles the capacitor current alternates in both polarity of the graph.

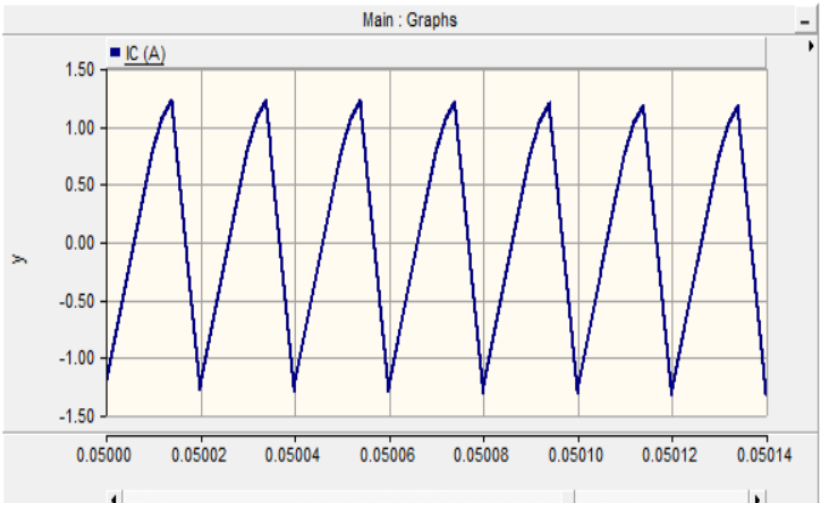

Figure 3.27: Capacitor current waveform

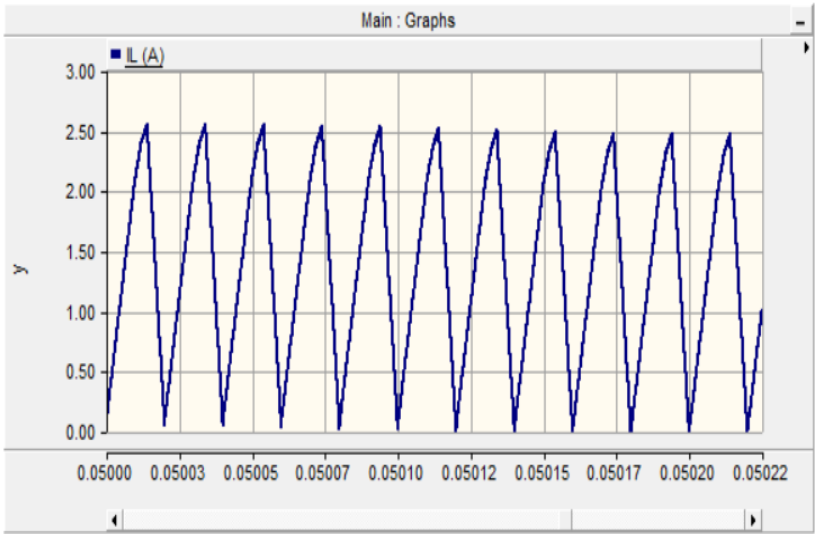

Figure 3.28: Inductor current waveform

The load current and load voltage waveforms are illustrated by Figure 3.29 and Figure 3.31 accordingly. The presented waveforms occur during the steady states of the converter operation. The magnitude the load current and load voltage are $i_o = 1.3A$ and $V_0 = 7V$ respectively. The inductor voltage for the three input converter is indicated by Figure 3.30. The various generated waveforms correspond to the theoretically produced waveforms.

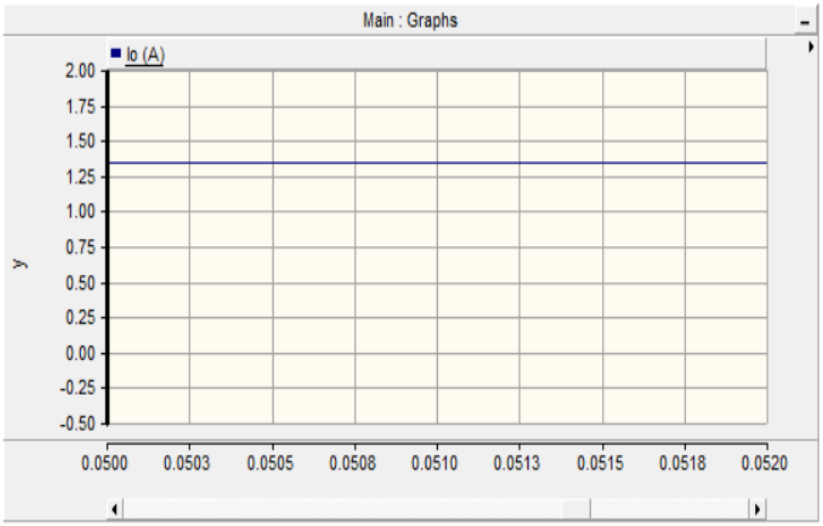

Figure 3.29: Load current waveform

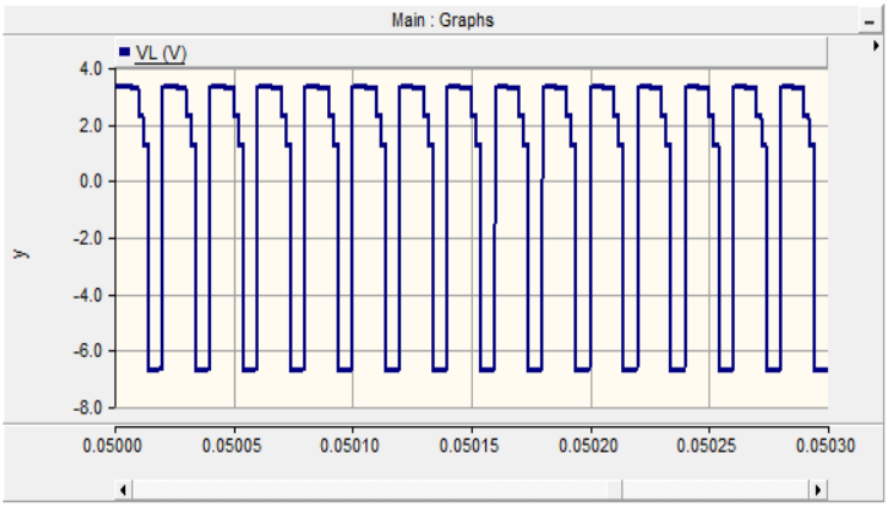

Figure 3.30: Inductor voltage waveform

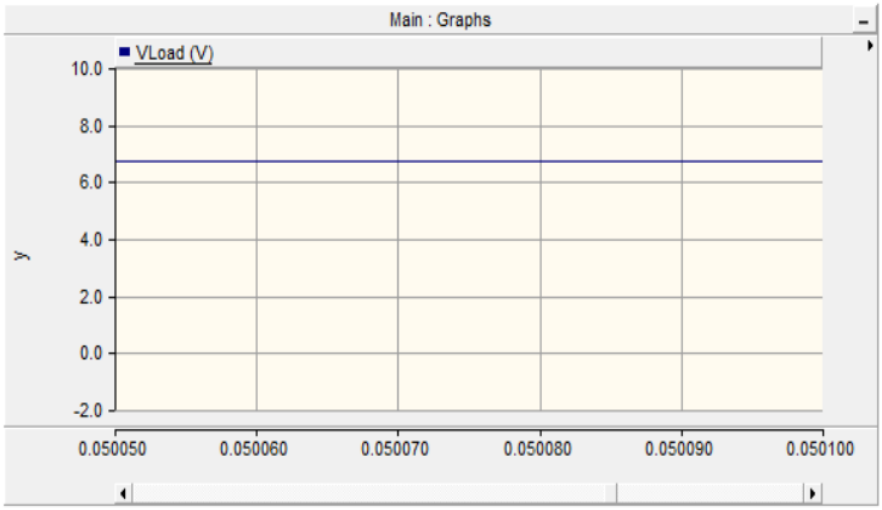

Figure 3.31: Load voltage waveform

The output waveforms of Figure 3.32 to Figure 3.37 are the applied waveforms of the five input converter and are generated by utilizing the parameters of Table 3.3.

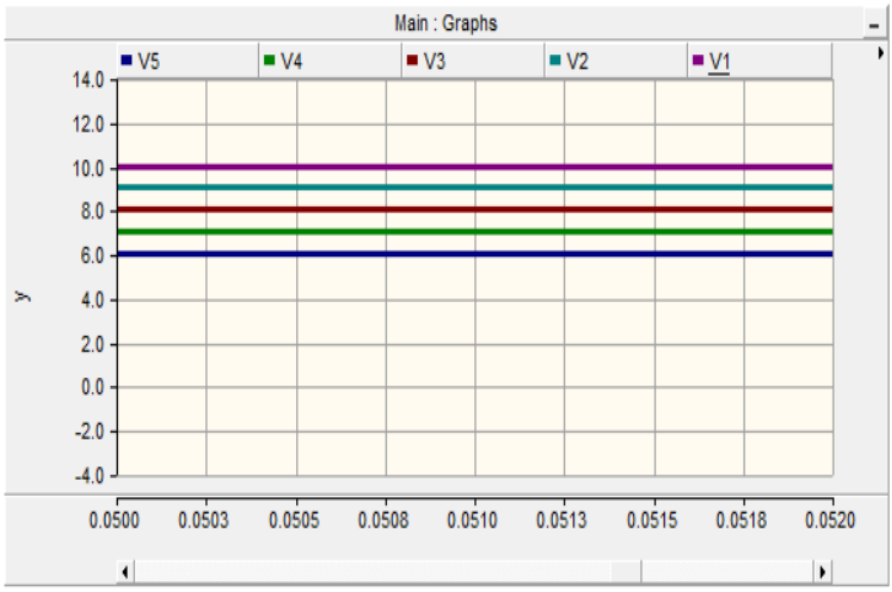

Figure 3.32: Input dc voltages

The waveforms of the input voltages are illustrated by Figure 3.32. The values of these inputs are $V_1 = 10V$, $V_2 = 9V$, $V_3 = 8V$, $V_4 = 7V$ *and* $V_5 = 6V$. The capacitor and inductor current waveforms are illustrated by Figure 3.33 and Figure 3.34 respectively. The nature of these waveforms corresponds the theoretically presented waveforms. The inductor current alternates only in the positive polarity region of the graph whiles the capacitor current alternates in both polarity regions of the graph.

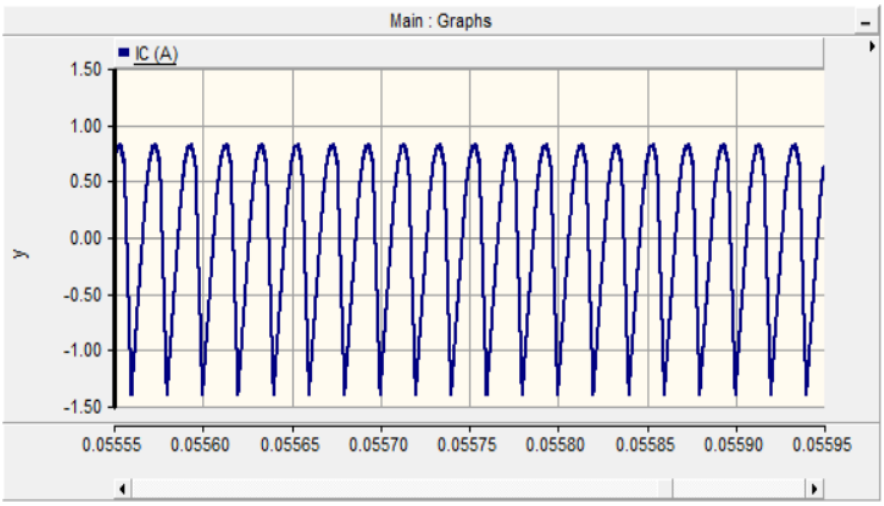

Figure 3.33: Capacitor current waveform

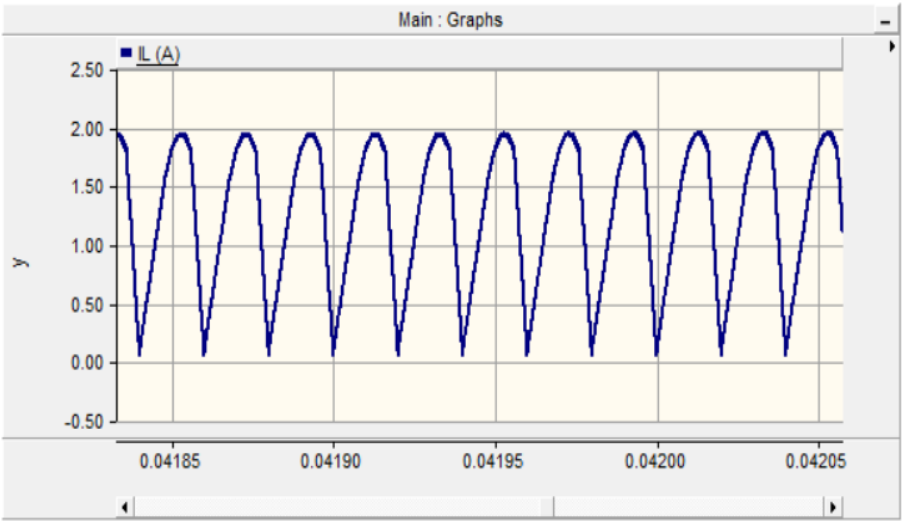

Figure 3.34: Inductor current waveform

Finally, the load current and load voltage waveforms are illustrated by Figure 3.35 and Figure 3.37 accordingly. The presented waveforms occur during the steady states of the converter operation. The magnitude the load current and load voltage are $i_o = 1.3A$ and $V_0 = 7V$ respectively. The inductor voltage for the three input converter is indicated by Figure 3.36. The various generated waveforms correspond to the theoretically produced waveforms.

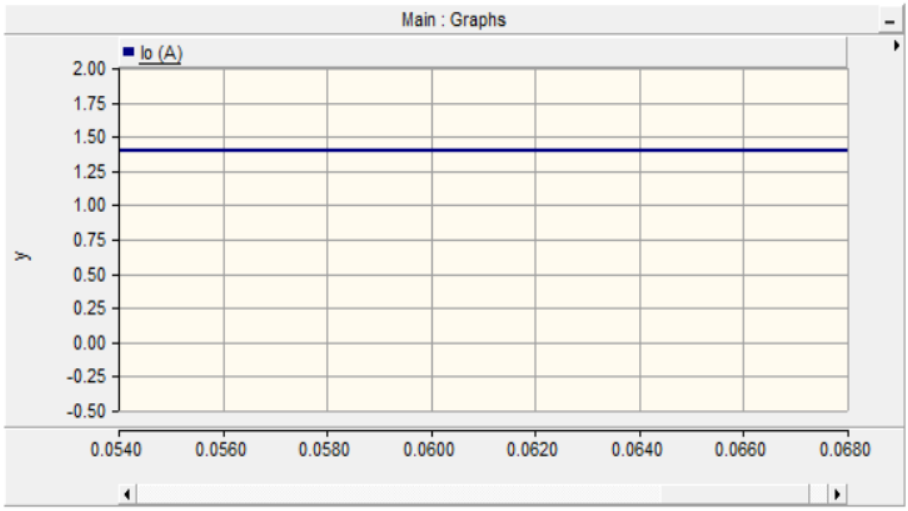

Figure 3.35: Load current waveform

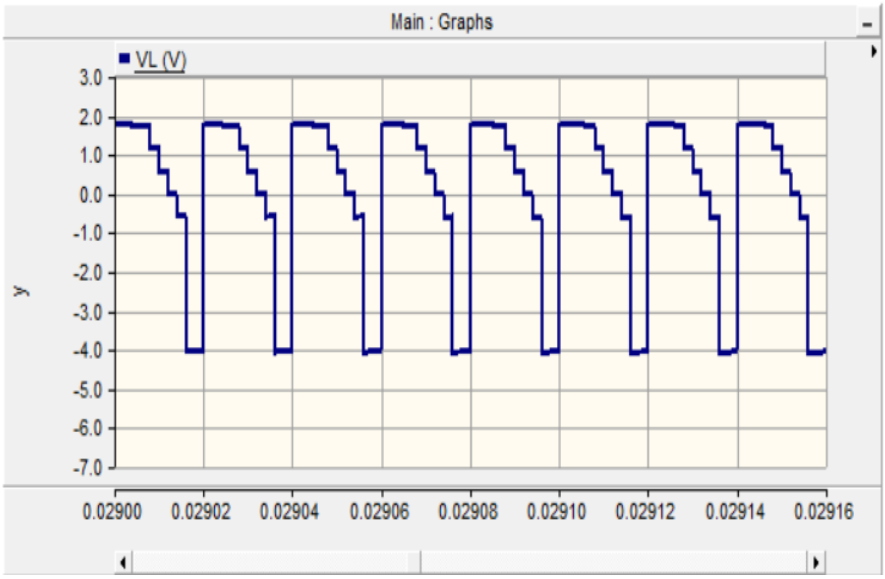

Figure 3.36: Inductor voltage waveform

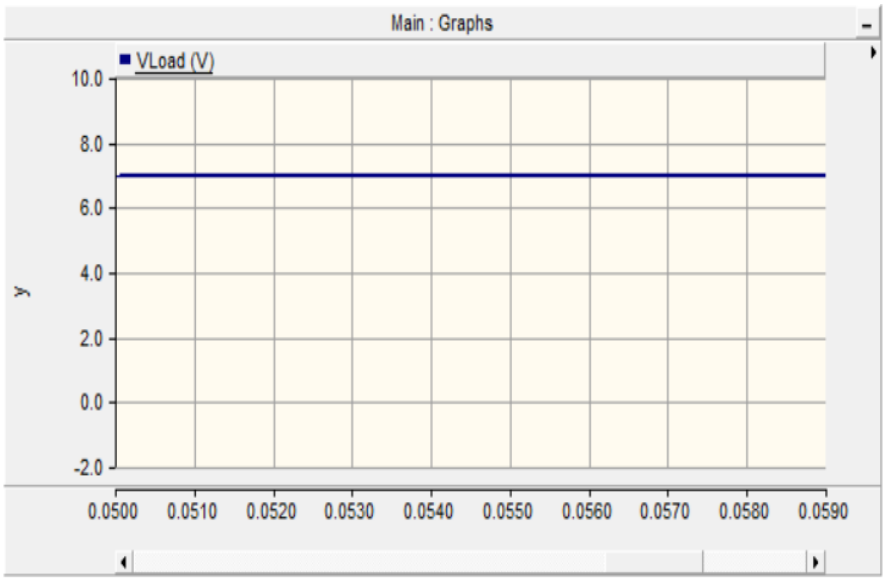

Figure 3.37: load voltage waveform

3.4 Conclusion

The presented multi-input dc-dc converter was investigated by building and simulating the power circuit in PSCAD software. Three different case scenarios of input values were analyzed and waveforms generated for the various inputs; in the first case, two voltage inputs were applied, in the second case three voltage inputs were applied whiles in the third case five voltage inputs were applied. The magnitude of the applied voltage was different but they had the same polarities. The load resistance value R_L was maintained constant in all three case scenarios however, the duty cycles were varied. The simulated output waveforms for inductor and capacitor currents, inductor and capacitor voltages, load current and load voltage conforms to the theoretically provided waveforms.

CHAPTER 4

CONCLUSION AND RECOMMENDATIONS

4.1 Conclusion

As stated in the introduction of chapter one of this research, application of power electronic converters in the last decade has witnessed rapid increase and this can largely be attributed to the major improvements that have been chalked in the power electronics based industry. Power switches with fast response, higher ratings and minimum power losses have been introduced. The current trajectory of electric power systems shows that the application of power electronic converters will continue to increase even though they are largely being applied in various areas of industry.

DC-DC converters are considered as the simplest converter topology in the broader converter family of power electronics converters. They are widely used in most electric power system from home electronics systems to satellite systems and everything in-between such as electric vehicle charging, communications systems and military applications. A multi-input dc-dc converter is presented in this research. Literature review of dc-dc converters was investigated based on the conventional topologies of buck, boost, buck-boost, cuk and multi-input converters. Theoretical analysis of the presented multi-input converter was also investigated where the mathematical equations governing the various parameters were provided. Finally, the presented topology's output waveforms were produced by constructing the converter's power circuit for three different case scenarios of two voltage input, three voltage input and five voltage input in PSCAD software and simulations were conducted. The generated output waveforms conform to the predicted waveforms in the theoretical analysis hence it can be said that the presented research was a success. The major advantage of the presented topology is its ability of energy diversification i.e. the application of various energy sources with different characteristics and also the converters ability to produce the desired magnitude of load voltage

and load current values irrespective of the number of input sources, this is evident from the simulated results of chapter three.

4.2 Recommendations

The idea of a multi-input source has been applied in multilevel converters but not extensively. Analyses of this concept in multilevel converters especially asymmetric topologies is worth investigating. This is a recommendation for future works.

The thesis is limited to the design and simulation of the multi-input converter. Hence, the detail characteristics of the energy sources have not been considered for brevity. Meanwhile, the performance of the developed converter to handle multiple energy sources was evaluated by using different values of the dc voltages to mimic the various energy inputs. The converter can successfully operate even when one or more sources is disconnected. However, the converter efficiency is higher when all the inputs are available. The future work will consider the detailed analysis about the lifetime of the specific energy sources, optimal inputs combination for higher efficiency.

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APPENDIX 1

ETHICAL APPROVAL LETTER

TO GRADUATE SCHOOL OF APPLIED SCİENCES

REFERENCE: MORAD ALI KH ALMANSURI (20183514)

I would like to inform you that the above candidate is one of our postgraduate students in Electrical and Electronics Engineering department he is taking thesis under my supervision and the thesis entailed: **A MULTIPLE-INPUT DC-DC CONVERTER TOPOLOGY.** The data used in his thesis does not require any ethical report.

Please do not hesitate to contact me if you have any further queries or questions.

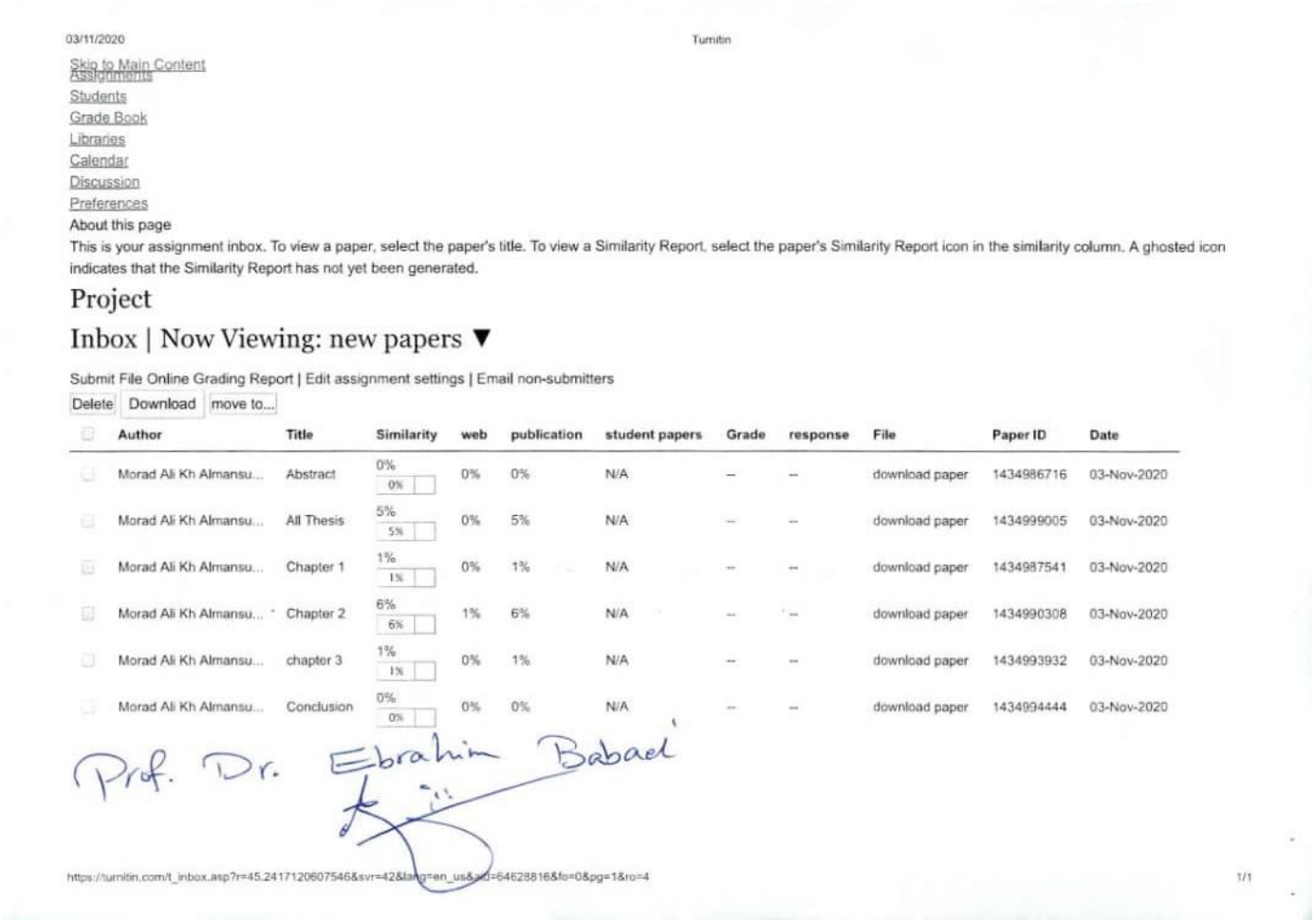
Thank you very much indeed.

Best Regards,

Prof. Dr. Ebrahim Babaei
Electrical and Electronics Engineering Department,
Faculty of Engineering,
Near East Boulevard, ZIP: 99138
Nicosia / TRNC, North Cyprus,
Mersin 10 – Turkey.
Email: parvaneh.esmaili@neu.edu.tr

APPENDIX 2

SIMILARITY REPORT



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