A NOVEL MULTILEVEL INVERTER BASED DYNAMIC VOLTAGE RESTORER DESIGN FOR MITIGATING THE VOLTAGE DISTURBANCES ON SENSITIVE LOADS

A THESIS SUBMITTED TO THE

GRADUATE SCHOOL OF APPLIED SCIENCES

OF

NEAR EAST UNIVERSITY

By
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In Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy
in
Electrical and Electronic Engineering

NICOSIA, 2021

Samuel Nii Tackie: A Novel Multilevel Inverter Based Dynamic Voltage Restorer Design for Mitigating Voltage Disturbances on Sensitive Loads.

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ACKNOWLEDGMENT

I would like to sincerely thank my supervisor Prof. Dr. Ebrahim Babaei for his understanding, patience, and guidance throughout my graduate studies at Near East University. His supervision was paramount in providing a well-rounded experience in projecting my long-term career goals. He encouraged me to be confident in everything I do. I graciously thank you for all you have done for me Prof. Dr. Ebrahim Babaei.

I would also like to thank Prof. Dr. Bulent Bilgehan, Dean and Chairman of Electrical and Electronic Engineering Department, my course Advisor Assist. Prof. Dr. Ali Serener, Thesis monitoring jury members; Prof. Dr. Senol Bektas and Prof. Dr. Sezai Dincer, all the lecturers in Electrical and Electronic Engineering Department and Faculty of Engineering at large for their immense guidance and attention.

Furthermore, I would like to thank my mom Theresa Ansah for her immense love, support and continuous prayer. Lastly, I want to thank all friends and colleagues for their consistent support.

ABSTRACT

An improved three-phase multilevel inverter, developed from H-bridge is proposed by this thesis. 13-level line voltage and phase voltage of 7-level are generated by the proposed inverter. The proposed three-phase multilevel inverter is made-up of less component count; 18 semiconductor switches of lower voltage ratings, 4 dc-source voltage and 18 driver circuits. Galvanic isolation is enabled when 3 single-phase transformers are incorporated. This makes the proposed inverter suitable for application in three-phase power systems such as dynamic voltage restorer (DVR). The proposed three-phase inverter is simple to control using fundamental frequency control technique and less complex structurally. Comparative investigation of the proposed three-phase inverter and other recently published three-phase multilevel inverters regarding total component quantity, dc voltage count, standing voltage, output voltage level count and driver circuit count is analyzed. Comprehensive explanation of the applied control technique is provided. Lastly, functionality of proposed three-phase multilevel inverter is validated by experimental prototype and EMTDC/PSCAD software based simulation.

Keywords: Three-phase multilevel inverter, standing voltage, multilevel inverter, component count, three-phase inverter, dynamic voltage restorer.

ÖZET

Bu tezde, H-köprüsünden geliştirilen üç fazlı çok seviyeli evirici önerilmiştir.Önerilen evirici tarafından 13 seviyeli hat gerilimi ve 7 seviyeli faz gerilimi üretilir.Önerilen üç fazlı çok seviyeli evirici, daha az bileşen sayısından oluşmaktadır; Daha düşük gerilim değerlerine sahip 18 adet yarı iletken anahtar, 4 adet doğru akım kaynak gerilimi ve 18 adet sürücü devresi.Üç tek fazlı transformatör dahil edildiğinde galvanik izolasyon etkinleştirilir.Bu, önerilen eviriciyi, dinamik gerilim yenileyici (DVR) gibi üç fazlı güç sistemlerinde uygulamanması için uygun hale getirmektedir.Önerilen üç fazlı evirici, temel frekans kontrol tekniğini kullanarak kontrol etmek basittir ve yapısal olarak daha az karmaşıktır.Önerilen üç faz evirici ile diğer son yayınlanan üç fazlı çok seviyeli eviricilerin, toplam bileşen miktarı, doğru akım gerilim sayısı, sabit gerilim, çıkış gerilim seviyesi sayısı ve sürücü devre sayısı ile ilgili karşılaştırmalı incelemesi analiz edilir.Uygulanan kontrol tekniğinin kapsamlı açıklaması verilmiştir. Son olarak, önerilen üç fazlı çok seviyeli eviricinin işlevselliği deneysel prototip ve EMTDC / PSCAD yazılım tabanlı simülasyon ile doğrulanır.

Anahtar Kelimeler: Üç fazlı çok seviyeli evirici, sabit gerilim, çok seviyeli evirici, bileşen sayısı, üç faz evirici, dinamik gerilim yenileyici.

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LIST OF ABBREVIATIONS

AC	Alternating Current
ANPC	Active Neutral Point Clamped
APOD	Alternate Phase Opposition Disposition
CD	Carrier Disposition
DC	Direct Current
DVC	Dynamic Voltage Compensator
DVR	Dynamic Voltage Restorer
ESS	Energy Saving System
FACTS	Flexible Alternating Current Transmission System
FC	Flying Capacitor
FFT	Fast Fourier Transform
GTO	Gate Turn-off Thyristor
HB	H-bridge
HFT	High frequency transformer
IEC	International Electro-technical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LC	Inductance Capacitance

LFT	Line Frequency Transformer
PCC	Point of Common Coupling
PD	Phase Disposition
PLL	Phase Locked Loop
POD	Phase Opposition Disposition
PQ	Power Quality
PV	Photovoltaic
PWM	Pulse Width Modulation
PS	Phase Shift
SV-PWM	Space Vector Pulse Width Modulation
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
TCT	Tap Changing Transformers
TDVR	Transformerless Dynamic Voltage Restorer
THD	Total Harmonic Distortion
TCR	Thyristor Controlled Reactor
TSC	Thyristor Switched Capacitor
MLI	Multilevel Inverter

MMLI	Modular Multilevel Inverter
MVA	Megavolt Amperes
NPC	Neutral Point Clamped
UPS	Uninterruptible Power Supply
VAR	Volt-ampere Reactive
WT	Wavelet Transform
WFFT	Wavelet Fast Fourier Transform
ZS	Z-Source

CHAPTER 1

INTRODUCTION

1.1 Overview

Application of Power electronic converters has rapidly increased in the past few years because of changes in the dynamics of electric power generation and also the utilization of more energy efficient devices. The world is gradually shifting from the use of fossil fuel for electric power generation to more sustainable methods such as renewable energy sources/resources. Developed countries such as Germany, USA China etc. generates substantial (Gigawatts) amount of electric power from renewable energy sources as a wind and solar. As a policy direction, renewable energy based electric power is increased yearly in these countries, China tops the group with respect to amount of power generated from PV systems. Renewable energy based methods of electric power generation require the use of power electronic converters for conditioning purposes. Generally, power electronic converters encompass the various electric power conditioning circuit such as cycloconverters, inverters, rectifiers and choppers (DC-DC). An inverter is a device composed of power electronic components (mostly semiconductor switches) which is used to change the characteristics of voltage i.e. from direct current voltage into alternating current voltage and also magnitude variations. Inverters are categorized according to several factors such as application; standalone or grid-tied for PV systems, low, medium and high power inverters, phase type; single, three or six phase, type of switching; soft or hard, source type; voltage or current source etc. Multilevel inverter, a class of inverters was first developed over 35 years ago.

Multilevel inverter (MLI) utilizes several number of direct current (DC) voltage sources at the input of the inverter power circuit to generate levels (steps) of voltage waveform at the output. Application of suitable number of dc voltage, semiconductor based switches and an appropriate control scheme will generate stepped output voltage waveforms which is similar to sinusoidal waveforms at the inverter's output. An almost perfect sinusoidal-like waveform has the following advantages; high quality output voltage waveform, minimum total harmonic

distortion (THD), inverter size is greatly reduced because filter size is minimized or eliminated in certain cases, lower switching losses, acceptable electromagnetic interference, less voltage stress on switches and reduced cost of inverter. These attribute makes MLI the preferred alternative when compared to other inverters most especially the two-level inverter. The main component in MLIs is the semiconductor power switch and its driver circuit. The switch type is selected with respect to the voltage medium and the application for which it's to be used. Power switches are either unidirectional or bidirectional from voltage and current point of view. Each unidirectional switch (voltage) is composed of one IGBT connected to a diode in an antiparallel style. Bidirectional switches are built from any of the following configurations; common-emitter, common collector, diode bridge, anti-parallel connected transistors and RB IGBT configuration. Appropriate control scheme is chosen to turn-on and turn-off the switches to generate the desired output waveform. In the absences of filters, semiconductor switches are the major components that determine the cost, size, volume and efficiency of the inverter. Utilizing minimum switch quantity and also lower rated switches reduces the cost, volume and size of inverter thereby increasing the efficiency of inverter. Series and parallel connections of switches provide *new* high rated switches which are commercially unavailable.

Multilevel inverters are generally classified into three categories, the first in this category is the Cascaded H-bridge MLI (Baker and Bannister 1975). The succeeding topology in this category is the Diode clamped MLI (DC MLI) (Nabae et al., 1981), which uses several diodes for clamping purposes and also series connected capacitors, finally the third member in the MLI category is Flying capacitor MLI (FC MLI) where capacitors float instead of having series connection (Meynard and Foch, 1992). Fig. 1 illustrates this classification and also a further classification based on single and multiple dc sources. Cascaded H-bridge MLI are mostly utilized in industrial applications for integration of renewable energy integrations (Patel and Hoft 1974). This is mainly because the architecture is easily scalable and there's no capacitor voltage-balancing challenges; a major challenge present in the other two topologies (DC MLI and FC MLI). Several topologies of cascaded MLI have been published in literature with the principal of increasing the stepped output voltages which significantly improves the waveform quality and also minimize the overall component quantity especially semiconductor switches.

These variations in topology are categorized into symmetric and asymmetric, with the latter having varying multiple magnitude dc sources. Reduced component count is highly realized with this topology but not suitable for high power utility systems due to lack of modularity and unbalanced voltage distribution. A solution is proposed in (Babaei and Hosseini, 2007) to resolved unbalanced voltage challenges. The symmetric topology has uniform voltage magnitude across the various unit in the cascaded architecture. The major drawback here is the higher component quantity (dc sources and switches) required for high number of stepped output voltage, however it boast of modularity, uncomplicated control scheme and equal voltage magnitudes.

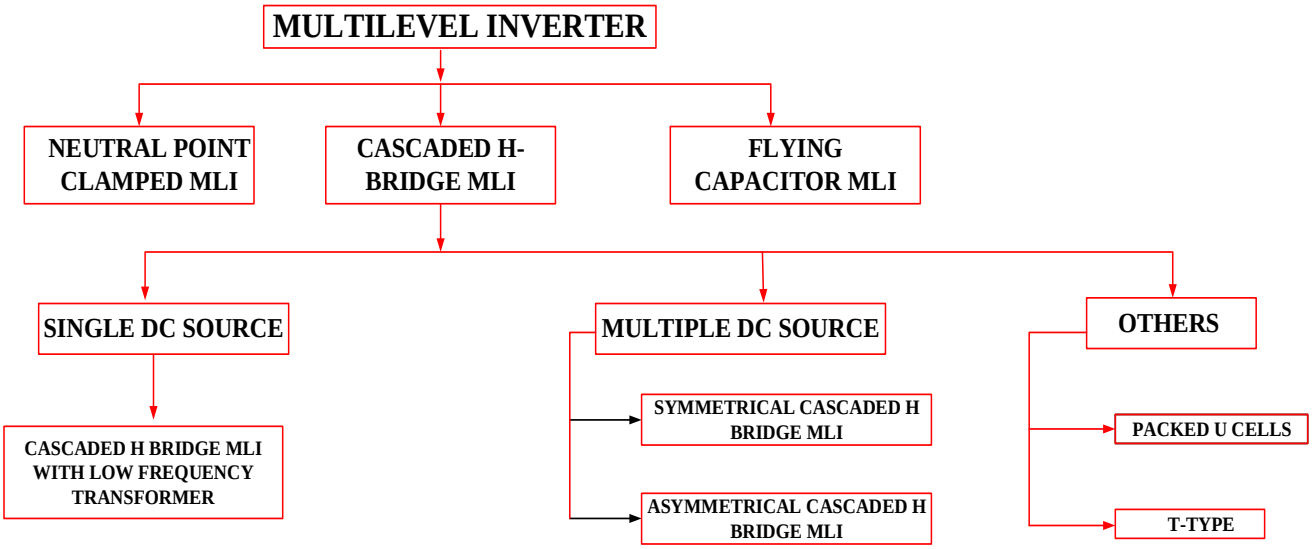

Figure 1.1: Classification of multilevel inverter

Voltage disturbance, made-up of voltage dip, voltage swell, flickers, unbalances and harmonics is one of the frequently faced power quality (PQ) problems by utility providers (Elnady et al.,2005). Voltage disturbances when not appropriately mitigated will lead to the destruction of critical and sensitive loads located in hospitals, factories and office buildings (Jimichi et al., 2008), also it can cause the disruption of production lines which may result in huge financial loss or possibly the loss of vital information (Chan and Milanović 2015; Trindade et al., 2013; IEEE, 2005). The demand for sensitive load protection is on the rise likewise is the usage of

devices responsible for the pollution of distribution lines. The definition of voltage dip according IEEE 1159 and 1346 standards is a reduction in the RMS (root mean square) ac voltage from 10% to 90% of nominal voltage at the utility's frequency for a period of half cycle to 60 seconds (IEEE, 1995, 1998). An abrupt connection of large loads, start-up of large rated induction motors and short circuit faults are major causes of voltage swell (Farhadi-Kangarlu et al., 2017) Also voltage dip can be defined according to IEC 61000-2-1 standards by two characteristics; an abrupt ***drop*** and ***recovery*** of voltage in power systems for a period lasting not more than half cycle to 60 seconds. Voltage swell is also defined according to IEEE benchmark as a rise in the RMS source voltage from 110% to 180% of the nominal voltage at the utility's frequency for a period not exceeding half cycle to 60 seconds. Disconnecting large loads such as inductive loads, switching of large capacitors and energizing of heavy capacitor banks are the major causes of voltage swell (Babaei and Farhadi Kangarlu 2009). Some effects of voltage swell are breakdown of industrial devices as a result of tripping and overheating of relays, surge arresters and ac motors (Bollen 2000; Arrillaga et al., 2000). Contamination of power lines with harmonics is a drawback for sensitive loads since their control relies on two factors; maximum value and zero crossing of the source voltage. These factors are affected by harmonic distortion (Awad 2004).

Different solutions have been proposed to resolve effects of voltage disturbances on sensitive loads. Custom power devices have been the most desired solutions to mitigate against voltage disturbances due to their effectiveness, fast response and flexibility. Custom power devices are power electronic based compensators and are classified into three categories; series compensators, parallel compensators and series-parallel compensators (Kazmierkowski 2007; Ghosh and Ledwich 2002). Series compensators which encompasses Dynamic Voltage Restorers (DVR), Dynamic Voltage Compensators (DVC) and Static Series Compensators (SCC) are considered cost effective way of resolving voltage disturbances. These compensators may vary from each other with respect to purpose and control mechanism but are similar in terms of power circuit structure and principles of operation. Other devices used in voltage sag and swell corrections are STATCOM (static compensators), tap changing transformers, UPS

(uninterruptable power supply) and flywheel (Najafi and Yatim 2011). The first installed DVR is located in a rug manufacturing company in North Carolina (Woodley et al., 1999).

Dynamic voltage restorer is a power electronic based device whose principal function is to protect critical and sensitive loads from voltage disturbances emanating from the supply side. DVRs are coupled to the distribution line via series connection and has the potential of absorbing and generating reactive and real powers. With respect to energy storage systems (ESS) DVRs are categorized into these groups: with ESS and without ESS. DVR topologies with ESS are sub-divided into capacitor based topologies and an external ESS. DVR topologies without ESS also subdivided into two; shunt based topologies and ac-ac based topologies. The shunt based topologies are also subdivided into source side connection and load side connection.

1.2 Problem Statement

Power electronic converter are regarded as integral component in all electric power generation systems (fossil fuel and renewable energy systems) and electric power conversion systems. Their usefulness is undoubtedly very important however, they are bedeviled with a number of drawback which are being addressed in both industry and academia by researchers. These drawbacks are high inverter cost, huge installation area as a result of increased size and volume, high inverter losses and reduced efficiency. The above mentioned drawbacks are directly caused by high component quantity most especially power switches and dc sources. Reducing the quantity of semiconductor switches and dc sources significantly improves or eliminates these drawbacks. The most common method of designing three-phase MLI is to replicate one single-phase three times to achieve three-phase MLI systems. This methodology increases the overall component quantity, a phenomenon that we wish to eliminate. A novel methodology will be implemented to reduce the overall component count, most importantly dc voltage source count. The use of power electronic gadgets in electric power generation, transmission and distribution has brought to the fore the problem of power quality issues such as voltage sag and swell, spikes and harmonics. These power quality related disturbances cause destruction of sensitive loads leading to huge financial burden to the consumer and utility provider.

1.3 The Aim of the Thesis

The aim of this research is to significantly reduce or eliminate the limitations enumerated above (in section 1.2). This is achieved by proposing a novel developed three-phase multilevel inverter composed of less component quantity i.e. semiconductor power switches and dc sources. The proposed three-phase topology has 18 power switches and 4 dc sources. “Extension technique” is applied to the single-phase topology to derive three-phase structure. This technique reduces the overall component count which leads to an improved three-phase ML inverter with less cost, minimum installation area, reduced inverter loss hence improved efficiency and finally highly reliable inverter. So as to make the proposed topology suitable for DVR (dynamic voltage restorer) applications, three single-phase transformers are connected to the topology. Also the proposed topology is capable of providing galvanic isolation because of the transformers.

1.4 The Importance of the Thesis

Because power electronic converters (inverters) are integral components of power generation and conversion systems, it’s imperative to significantly minimize or eliminate limitations which bug these inverters. In view of this, the proposed three-phase ML inverter has the following merits:

- Reduced dc source count
- Reduced inverter size
- Reduced inverter volume
- Minimum area of installation
- Less quantity of semiconductor switches
- Improved reliability
- Reduced inverter cost

On the other hand, applying the proposed three-phase ML inverter in DVR systems for voltage compensations will generally lead to protection of sensitive loads in factories, hospitals etc. Generally, some advantages of DVR systems are reduce cost of replacing damaged devices, lifesaving and reduced production losses.

1.5 Limitation of the Study

Generally, a number of limitations were encountered during the implementation of this research, significant amongst these limitations was the travel restrictions due to COVID 19. However, these limitations were overcome by the guidance and support of my supervisor, chairman and course advisor of electrical and electronics engineering department.

1.6 Overview of the Thesis

This section describes the arrangement of the thesis. This work of research is segmented into the following chapters:

Chapter 1: introduction

- Introduction
- Problem Statement
- Aim of the thesis
- The importance of the thesis
- Limitations of the study
- Overview of the thesis

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- Introduction
- Cascaded H-Bridge MLI
- Flying Capacitor MLI
- Neutral Point Clamped MLI
- Comparative analysis of Cascaded H-Bridge and Flying Capacitor
- Comparative analysis of Cascaded H-Bridge and Neutral Point Clamped
- Application of MLI
- Cascaded MLI Topologies
- MLI Control Techniques
- Conclusion

Chapter 3: investigation of multilevel inverter based dynamic voltage restorers.

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- DVR Components
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- Application of DVR
- DVR Topologies
- Conclusion

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- Proposed Three-phase Multilevel Inverter
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- Comparative Investigation
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- Introduction
- Simulation Results
- Experimental Results
- DVR Simulation
- Conclusion

Chapter 6: conclusion

CHAPTER 2
LITERATURE REVIEW OF MULTILEVEL INVERTERS

2.1 Introduction

Multilevel inverters (MLI) are inverters that produce several levels of load voltages by employing single or multiple dc source voltage at the input side. The concept of multilevel inverter was proposed over 35 years ago. Diode Clamped MLI was the first functional multilevel inverter introduced in 1980 by (Nabae et al., 1981). Basically, any inverter capable of producing three or more levels of output voltage is considered to be a multilevel inverter. The conventional two-level inverter precedes the multilevel inverter. MLIs are the appropriate devices for high voltage and high power applications because the synthesized output waveforms contain acceptable harmonic spectrum, also lower rated switches are used to synthesize high voltages (Manjrekar et al., 1999). Generally, multilevel inverters produce better quality output waveforms when the number of output levels is increased. This characteristic makes the MLI topology a better alternative to the two level inverter. Higher levels of output waveforms mean the magnitude of the output step voltages are small hence power switches of lower ratings are utilized. Lower rated switches reduce power losses hence increases the efficiency of the inverter. Other advantages of MLI are minimum harmonic content, reduced dv/dt stress and application of low speed semiconductor switches.

2.2 Cascaded H-Bridge

Cascaded H-bridge inverter is derived by series connection of two or more H-bridge structures. Each H-bridge inverter (cell) in the series connection has a separate dc-link or source. The number of voltage levels that can be generated by the cascaded structure is determined by the number of H-bridges in the cascaded structure and the magnitude of the dc-links. For evenly distributed dc-link magnitudes, the output voltage level is computed by $2n + 1$ where n represents the number of H-bridge cells in the series connection. Increasing the number of cells in the cascaded H-bridge topology will result in higher number of output voltage levels. The

simplicity of the H-bridge topology makes it convenient for deriving a cascaded topology unlike other types of multilevel inverters. An example of a cascaded topology made of two H-bridge cells is shown in Fig. 2.1. The switching pattern of this cascaded structure used in generating the desired output voltage (V_0) is shown in Table 2.1. *E* is the input voltage for each cell. It should however be noted that not all switching states in Table 1 are required. Switching states which produce short circuit of switches and dc-link as well as open circuit of the load should be avoided.

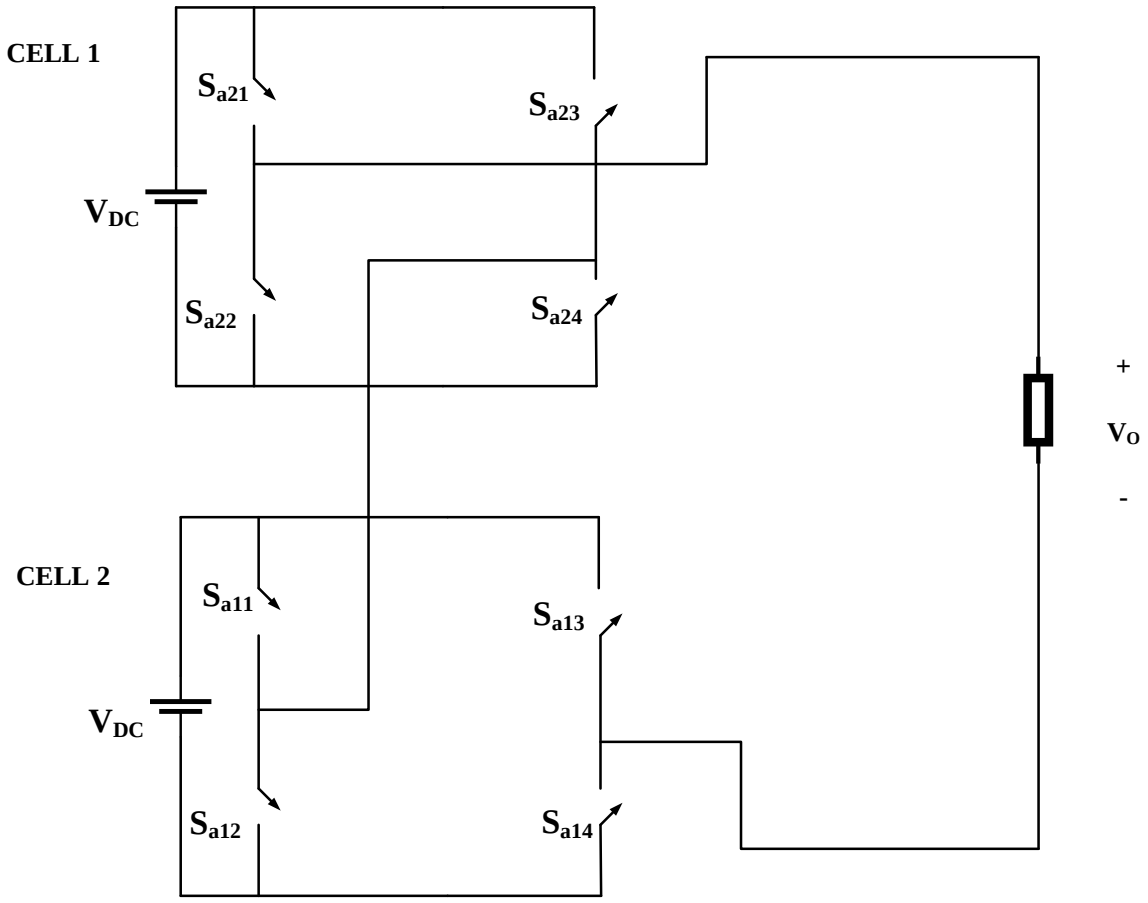


Figure 2.1: 5-levels Cascaded H bridge inverter

S_a21 to S_a24 are the switches for "cell 1" H-bridge where the input and output voltages are V_{DC} and V_A respectively. S_a11 to S_a14 are the switches for "Cell 2" H-bridge where the input and output voltages are V_{DC} and V_N respectively. Pulsewidth modulation control techniques can be

applied to the cascaded H-bridge multilevel converter. Some advantages of the cascaded converter are: less number of components is required, snubber circuit not needed because soft switching is applicable, each layout has same number of component making it simple to package, high power-high voltage application, and the disadvantage of the cascaded multilevel inverter lies in the separate dc source required and as such makes gives the cascaded converter limited application (Lai and Peng 1996), a new topology was presented in (Soto et al., 2003) where a single dc source was used to developed 5-levels cascaded H-bridge inverter by utilizing interface inductors between the series chain.

Table 2.1: Switching Pattern for 5-levels cascaded converter. (Chiasson et al., 2003).

S_a21	S_a23	S_a22	S_a24	S_a11	S_a13	S_a12	S_a14	V_A	V_B	V_O
1	0	0	1	1	0	0	1	$+V_{DC}$	$+ V_{DC}$	$+2V_{DC}$
1	0	0	1	1	1	0	0	$+ V_{DC}$	0	$+ V_{DC}$
1	0	0	1	0	0	1	0	$+ V_{DC}$	0	$+ V_{DC}$
1	0	0	1	0	1	1	0	$+ V_{DC}$	$- V_{DC}$	0
1	1	0	0	1	0	0	1	0	$+ V_{DC}$	$+ V_{DC}$
1	1	0	0	1	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
1	1	0	0	0	1	1	0	0	$- V_{DC}$	$- V_{DC}$
0	0	1	1	1	0	0	1	0	$+ V_{DC}$	$+ V_{DC}$
0	0	1	1	1	1	0	0	0	0	0
0	0	1	1	0	0	1	0	0	0	0
0	0	1	1	0	1	1	0	0	$- V_{DC}$	$- V_{DC}$
0	1	1	0	1	0	0	1	$- V_{DC}$	$+ V_{DC}$	0
0	1	1	0	1	1	0	0	$- V_{DC}$	0	$- V_{DC}$
0	1	1	0	0	0	1	0	$- V_{DC}$	0	$- V_{DC}$
0	1	1	0	0	1	1	0	$- V_{DC}$	$- V_{DC}$	$-2 V_{DC}$

2.2.1 Symmetrical and Asymmetrical CHB

Cascaded multilevel inverters are categorized into two types, namely symmetrical cascaded multilevel inverter and asymmetrical cascaded multilevel inverter. It has already been established that cascaded multilevel inverter is the series connection of multiple H-bridge inverters. Basically, the difference between the two types of cascaded multilevel inverter lies in the magnitude of dc voltage at the input. When the magnitude of dc voltage for all H-bridges in the series connection are equal, then the multilevel inverter is known as symmetrical cascaded multilevel inverter.

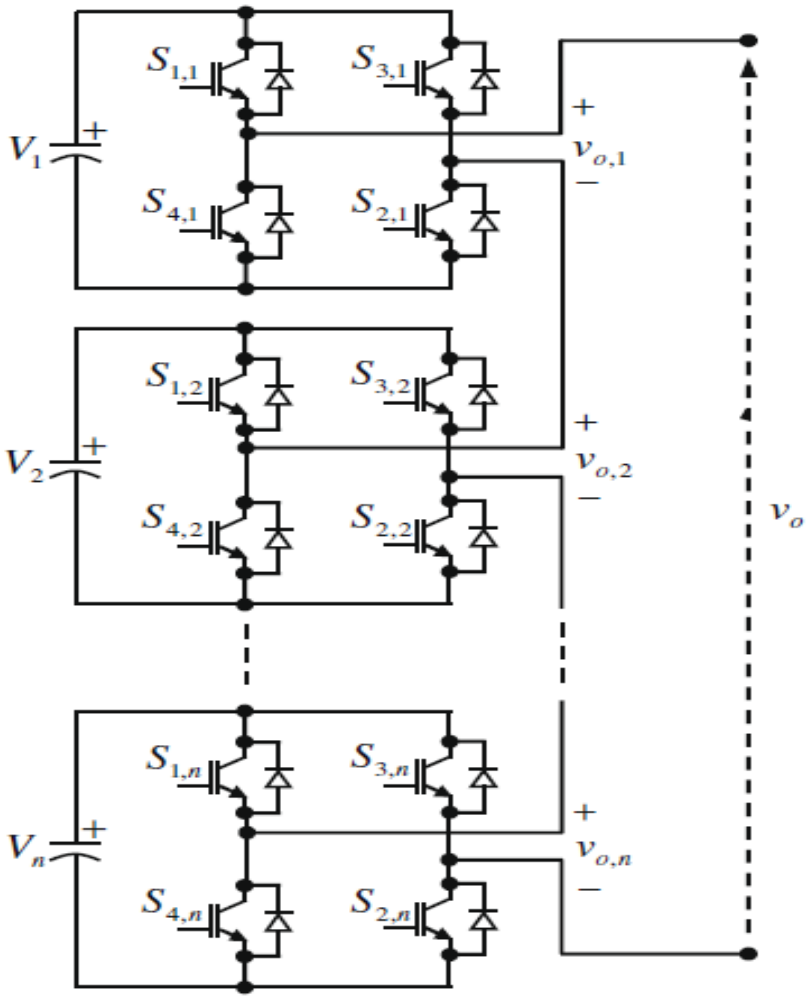


Figure 2.2: *n*-level cascaded H-Bridge converter

However, if there's a difference in the magnitude of the dc voltage of at least one H-bridge in the series chain, then the multilevel is known as asymmetrical cascaded multilevel inverter (Manjrekar and Lipo 1998; Schibli 2000; Rufer et al., 1999). Although there are other factors which differentiate symmetrical and asymmetrical converters; these factors will be explained in later sections, our considerations now will be on the magnitude of the input dc voltage. Based on the magnitude of the input dc voltage, symmetrical and asymmetrical inverters cannot be limited to cascaded H-bridge inverters only as symmetrical and asymmetrical diode clamped inverters have been presented in (Song-Manguelle and Rufer 2001).

Fig. 2.2 shows limitless level (n-level) of cascaded multilevel converter. For symmetrical cascaded multilevel inverter, the number of levels or steps that can be generated at the output is expressed by equation (2.1) where n in the equation is the number of H-Bridge modules in the series connection.

$$\text{Number of steps (n)} = 2n + 1 \tag{2.1}$$

For example, if 3 H-bridge modules are connected in series to form cascaded bridge inverter, then the maximum steps that can be generated at the output is 7-level for symmetrical H-bridge provided $V_1 = V_2 = V_3$ where V_1, V_2, and V_3 represents the input voltage for the individual H-bridge modules in the series connection. Also the maximum voltage that can be generated by 7-level cascaded symmetrical multilevel is given by equation (2.2), where V_{dc} is the voltage across any H-bridge in the series connection.

$$Vmax = nVdc \tag{2.2}$$

As stated above, if the voltage value (V_{dc}) of any H-bridge module in the series connection is different i.e. $V_1 \neq V_2 = V_3$, the series connection is classified as asymmetrical; two types exist for the asymmetrical converter; ***binary*** and ***trinary*** cascaded asymmetrical inverter. Table 2.2 shows the difference between symmetrical and asymmetrical converter with respect to no of output levels, maximum output voltage, number of input voltage and number of semiconductor switches required (Babaei et al., 2007; Babaei and Hosseini 2008). The difference between binary and trinary asymmetrical multilevel inverter is the number of output voltage levels and

the ratio of dc voltage between H-bridges in the series chain. In the binary cascaded H-bridge multilevel inverter, the input voltage ratio is 1:2 whiles its 1:3 for the trinary cascaded H-bridge multilevel inverter, these ratios are valid provided they have the same number of input voltage and H-bridges in the series connection.

If two H-bridge modules are cascaded for asymmetrical multilevel inverter, the number of output voltage steps will be 7-level and 9-level for ***binary*** and ***trinary*** asymmetrical multilevel inverter respectively. IGBTs and diodes are the principal components in all multilevel inverters, asymmetrical cascaded have equal quantity of switches but are able to generate more levels of load voltage. from the perspective of technical and economic significance of power dissipation, using lower voltage rated switches reduces the cost and losses. Losses which occur in converters because of power semiconductor switches are categorized into three set; switching losses, off-state losses and conduction losses (Aghdam and Fathi 2005).

Table 2.2: Symmetrical and Asymmetrical converter comparison

	Symmetrical Inverter	**Asymmetrical Inverter**	
		Binary	**Trinary**
Number of output steps	2n + 1	$2^{n+1}-1$	3^n
Number of dc sources	n	n	n
Number of switches	4n	4n	4n
Maximum output voltage	n	2n - 1	$\frac{3^n-1}{2}$

One major disadvantage of the cascaded H-bridge multilevel inverter is the huge number of semiconductor power devices required as the number of output steps are increased; this results in increased number of gate driver circuits and protection circuits thus increased cost of device and maintenance cost. Asymmetrical cascaded H-bridge inverter has the advantage of increased number of output steps when compared to the symmetrical H-bridge which corresponds to small

device size, reduced device cost, and easy control technique. Despite the considerable advantages of asymmetrical multilevel inverter over symmetrical multilevel inverter, some disadvantages exist as well. Difference in magnitude of input voltage results in differences in the life-span of the voltage sources therefore increased cost due to increased battery evaluation and substitution, power losses increases due to higher voltage rated semiconductor devices. To solve the problem of high number of semiconductor devices required in the cascaded multilevel inverter, several new topologies in (Babaei et al., 2007; Babaei and Hosseini 2008) have been introduced which can produce higher voltage output steps with limited number of semiconductor switches.

2.3 Flying Capacitor Multilevel Inverter

A 5-level Flying capacitor single phase inverter is shown by Fig. 2.3. In the Flying capacitor inverter which is also known as capacitor clamped inverter, clamping diodes are not required which is an added impetus when compared to NPC inverter, also one dc source is enough because of switching redundancy (Lai and Peng 1996). Each capacitor in a different leg is charged to a different value from other capacitors, and the capacitors which are connected in series determine the level of output voltage. The series connection of the capacitors as shown in Fig. 2.3 determines the level of V_{dc} output from the point of clamping. The switching pattern for the Flying capacitor converter is shown by Table 2.3. The use of multilevel inverters means that ac voltage in power systems could be increased without the utilization of transformers and lower order harmonics can be cancelled which means reduced component cost because the ac inductance size is greatly minimized. The Flying capacitor converter has numerous advantages such as: minimization of harmonics thus cost saving because the need for filters are eliminated, reduced number of diodes when compared to NPC, suitable for high voltage transmission system because reactive power can be controlled, capacitors serve as storage units, phase redundancy in Flying capacitor over line to line redundancy in the NPC inverter. Disadvantages are: lager number of capacitors are required, in high power systems efficiency is reduced because switching losses are increased thus control of the inverter becomes complex (Lai and Peng 1996).

Table 2.3: Switching pattern for 5-level flying capacitor inverter

Output Voltage	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = \frac{3}{4}V_{dc}$	1	1	1	0	1	0	0	0
$V_3 = \frac{1}{2}V_{dc}$	1	1	0	0	1	1	0	0
$V_2 = \frac{1}{4}V_{dc}$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

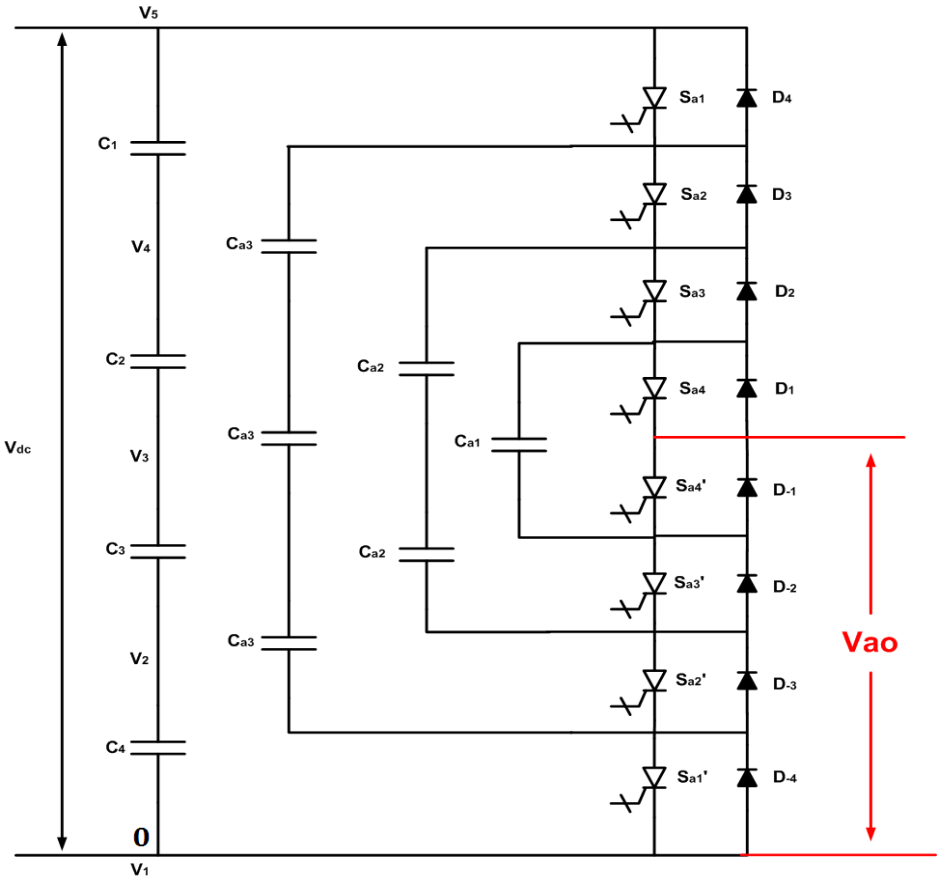


Figure 2.3: Five level flying capacitor converter

2.4 Neutral Point Clamped Multilevel Inverter

Another type of multilevel inverter which has contributed significantly to the development of quality output waveform is the Neutral Point Clamped Inverter (NPC). Fig. 2.4 shows the circuit diagram of the NPC inverter for three-phase topology, the neutral point of the circuit with respect to direct voltage source is the zero (0) point. There are two types of switches in the circuit, main switches and auxiliary switches. The main transistor switches have the responsibility or function of pulse width modulation controller and the purpose of the auxiliary transistor switches is to clamp the potentials of the output terminals to the zero point with the aid of diodes D_1 to D_6. The main switches are S_{a1}, S_{a4}, S_{b1}, S_{b4}, S_{c1}, S_{c4} (upper and bottom horizontal switches) and the auxiliary switches are S_{a2}, S_{a3}, S_{b2}, S_{b3}, S_{c2}, and S_{c3}. All conventional pulsewidth modulation control techniques can easily be applied to this inverter which makes NPC-PWM inverter versatile in terms of control methodology (Nabae et al., 1981).

The NPC inverter shown in Fig. 2.4 is a three phase 5-level inverter; it's possible to generate line-to-line voltage between the phases available and also possible to generate phase voltage for either phases a, b or c. The switching pattern for a-phase is similar to the switching pattern of Table 2.4. Several other topologies of neutral point clamped inverter have been developed; these topologies are derived by changing the structure of the conventional NPC. Examples of these newer NPC inverters are:

a. Active NPC
b. T-Type NPC

The active NPC inverter is developed by substituting the clamping diode in the NPC inverter with an active switch. The T-type NPC also known as switch clamp is derived by connecting the output point together with the neutral point via bidirectional switches. Figure 2.5a, 2.5b and 2.5c shows the ANPC and T-type NPC derived from 3-level diode clamped inverter. Single phase NPC-PWM inverter is shown in Fig. 2.6 (Nabae et al., 1981). The single NPC inverter is described as 3-state NPC inverter because of its ability to generate 3 different dc voltages at the output; 0, E, and 2E. As explained in the 3-phase NPC inverter, switches S_1, S_2, S_7, and S_8 are

the main switches and switches S_3, S_4, S_5, and S_6 are the auxiliary switches; their function is to complement the main switches to derive desired output voltage. Table 2.4 shows the switching pattern for the single phase NPC inverter.

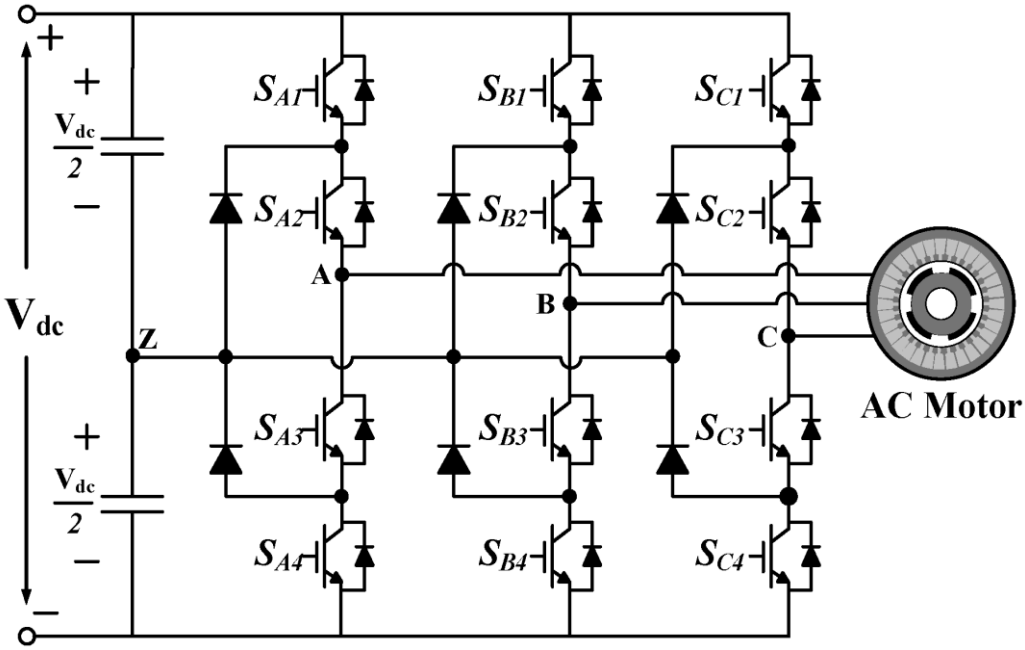
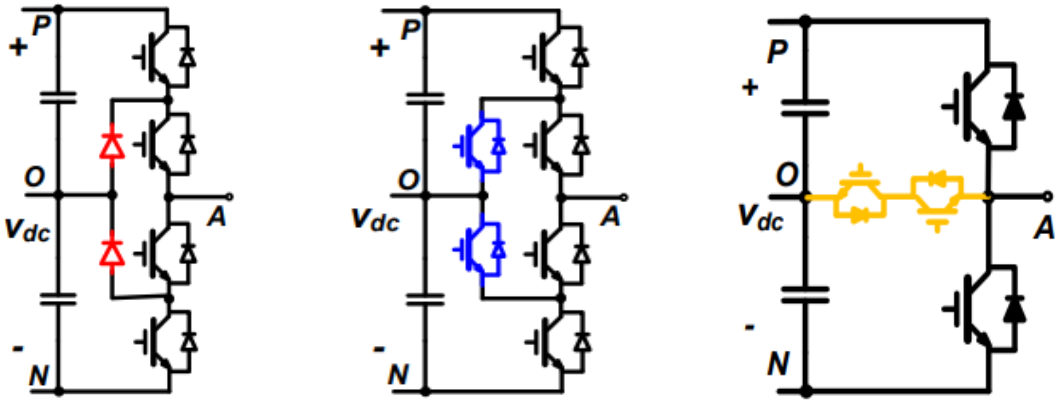


Figure 2.4: Neutral point clamped inverter



(a) (b) (c)

Figure 2.5: (a) NPC (b) ANPC (c) T-type NPC

During any switching pattern, the maximum blocking voltage across each semiconductor switches must be equivalent to half the dc supply. Proper controlling of the inverter to avoid abrupt alterations between E and -E will produce lower harmonics and prevent simultaneous turning on and off of two switches. Some advantages of NPC are: harmonic elimination at higher levels, higher efficiency due to fundamental frequency switching, control of reactive power, simple control techniques and the demerits are: large number of diodes are required for higher levels, real power flow control is difficult for individual converters (Lai and Peng 1996).

Table 2.4: Single Phase NPC Inverter Switching Pattern

	Switches				
State	**S_1**	**S_7**	**S_2**	**S_8**	**Output Voltage**
I	1	0	0	1	2E
	1	0	0	0	
II	0	0	0	1	E
	1	0	1	0	
III	0	0	0	0	0
	0	1	0	1	
	0	0	1	0	
IV	0	1	0	0	-E
V	0	1	1	0	-2E

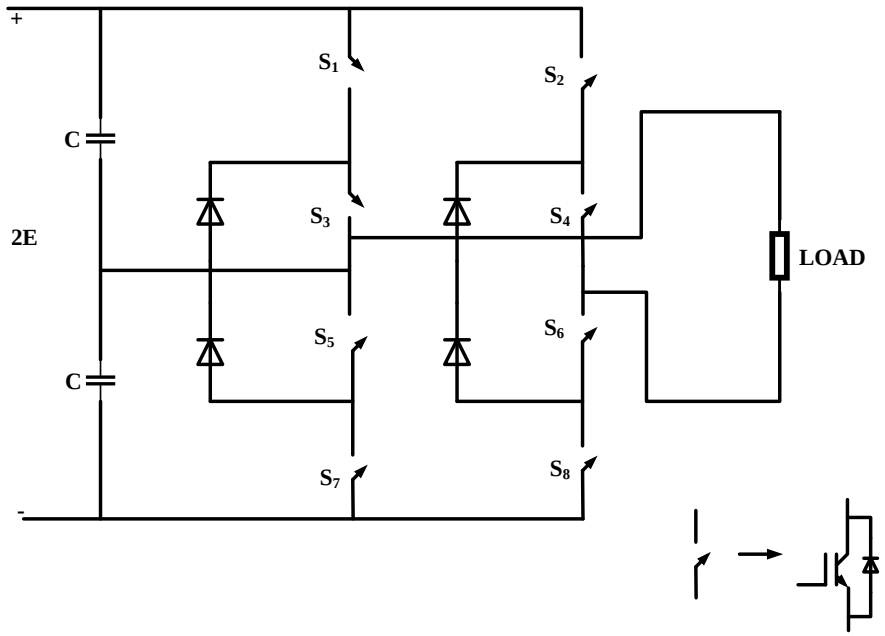


Figure 2.6: Single phase NPC- PWM inverter

2.5 Comparative Analysis of Cascaded H-Bridge and Flying Capacitor.

Although the cascaded H-bridge and Flying capacitor inverters are all categories of multilevel inverters; there are a couple of differences between them; these differences can be mainly traced to the circuit structure. Fig. 2.1 and Fig. 2.3 shows the circuit diagrams of the two inverters having 5-level output voltage, these inverter circuits are that of cascaded H-bridge and Flying capacitor inverters respectively. The number of diodes and power switches in both circuits are equal but the Flying capacitor has 10 capacitors more than cascaded H-bridge. From the power source pint of view, the cascaded H-bridge inverter is made up two dc source and the Flying capacitor inverter has only one dc source. Capacitor voltage levels in the latter topology can be balanced by phase redundancies technique. The power ratings of power switches in the Flying capacitor inverters are different. This is because different levels of power ratings are applied to different switches but in the case of the cascaded H-bridge the voltage ratings are the same, these differences cause difficulties in the blocking voltage analysis of the Flying capacitor

inverter. The blocking voltage or standing voltage of converters have become an important point of reference when determining the reliability of the converter. Standing voltage is directly linked to the cost, size and efficiency of any proposed converter (Babaei et al., 2014). Control of the Flying capacitor is complicated because each leg has different voltage ratings of capacitors hence different voltage levels; discharging and discharging period becomes problematic. The cascaded H-bridge inverter control is less problematic as compared to Flying capacitor inverter; the same number of components in the first cell/module is repeated in the next cell/module hence its control is simple, also no capacitors required in the main topology structure. Due to the large number of capacitors required in the Flying capacitor topology, the structure of the system becomes bulky and heavy, not to talk about increased cost and reduced efficiency. Increasing the output voltage level will result in uneven package/layout but the cascaded H-bridge topology has modularized structure making the model or packaging less difficult (Lai and Peng 1996). Comparative analysis of the two topologies with respect to the number of component and the type of component utilized in the main inverter circuit is shown in Table 2.5. Cascaded H-bridge inverter has the following advantages over the Flying capacitor inverter;

a. simple control technique
b. very reliable irrespective of the desired levels of output voltage hence high modularity
c. Uniform blocking voltage
d. Reduced cost, simple structure and increased efficiency (Babaei and Laali 2015).

Table 2.5: Analysis of CHB and FC inverters

No. of Components	Cascaded HB	Flying Capacitor
Capacitor	-	10
Switch	8	8
Source	2	1
Diode	8	8
Total	18	27

2.6 Comparative Analysis of Cascaded H-Bridge and NPC

Cascaded H-bridge inverter and the NPC inverter are similar when analyzed with respect to the level of output voltage. Fig. 2.1 and Fig 2.6 show the single phase circuit diagram of cascaded H-bridge and NPC inverter respectively. These topologies are referred to as 5-level inverters because of the steps (5-level) of output voltage that can be generated.

The number of components required in the two topologies are not equal; the cascaded H-bridge requires 8 switches (antiparallel connection of a transistor and a diode) and two dc sources to generate 5-steps of output voltage whiles the NPC topology requires 8 switches (antiparallel connection of a transistor and a diode), two capacitors, four diodes and one dc source to generate the same level of output voltage as the cascaded H-bridge topology. Comparing the NPC topology to the conventional inverter will exhibit superior advantages for the NPC topology but when compared to the cascaded H-bridge topology, the latter topology exhibits more advantages than the former. The main advantages of the NPC inverter are derived when it's compared to the traditional inverter, some advantages are reduced harmonic content, quality output waveform and minimum switch stress caused by high voltage. Also it should be noted that NPC converter is mostly suitable for renewable energy application. Due to complex nature of the topology, increasing the output voltage beyond 5-level becomes complicated hence the 3-level NPC inverter has received lots of applications (Nabae et al., 1981).

Table 2.6: Analysis of CHB and NPC inverters

No. of Components	Cascaded HB	NPC
Capacitor	-	2
Switch	8	8
Source	2	1
Diode	8	12
Total	18	23

From Table 2.6, the following deductions can be made about the two topologies; cascaded H-bridge and NPC. The number of switches utilized in the two topologies are the same, 8 bidirectional switch with respect to current for each topology. However, the NPC topology has two capacitors connected to the dc source and four diodes for voltage blocking purposes. The output voltage of the NPC inverter is dependent on the voltage ratings of the two capacitors; however, the voltage ratings of these capacitors are the same. Therefore, the input voltage is shared equally between the capacitors.

Again cascaded H-bridge inverter exhibits superior advantages over NPC inverter with the following advantages; reduced number of components, simple structure hence increasing the output levels is less complicated, modularity of the structure is easily achieved, quality output waveform, reduced loses and increased efficiency. Some advantages of NPC are: harmonic elimination at higher voltage levels, higher efficiency due to fundamental frequency switching, control of reactive power, simple control techniques and the demerits are: large number of diodes are required for higher levels, real power flow control is difficult for individual converters (Lai and Peng 1996). During any switching pattern, the maximum blocking voltage across each semiconductor switches must be equivalent to half the dc supply. Proper controlling of the inverter to avoid abrupt alterations between E and -E will produce lower harmonics and prevent simultaneous turning on and off of two switches.

2.7 Application of Multilevel Inverters

One major application of the multilevel inverter in the early 1990s to late 1990s is VAR compensation technique in high power transmission lines; FACTS. Reactive power control popularly known as VAR is an integral component in power systems which increases the power transmission capabilities of the system, reduce power losses due to transmission and stabilizes system (Peng and Lai 1997). Due to the MVA requirements of the power systems and the low power ratings of GTOs available, parallel connection of multilevel units or modules to achieve higher currents rating were proposed in (Schauder et al., 1995; Mori et al., 1993); this topology

did not require an increase in the GTO power ratings which was a problem at that time but lower order harmonics could be minimized with an appropriate control technique.

Application of multilevel converter in the compensation area of power systems ranges from VAR to SVC, ASVC, STATCOM (Mwinyiwiwa et al., 1997; Chen and Ooi 1996;). The various reactive power compensators such SVC, ASVC etc. have come to replace the traditional method of VAR compensation; TCR and TSC (Peng and Lai 1997; Schauder et al., 1994; Mori et al., 1993). Basically, multilevel converter are important devices in controlling the various components of flexible ac transmission system as reported in (Mwinyiwiwa et al., 1997; Mori et al., 1993; Schauder et al., 1995; Gyugyi 1995). One limitation of the GTO is the low switching frequency medium in which it can operate (Damiano et al., 1997) but IGBTs with high power-high switching frequency capabilities were reported in (Hiyoshi et al., 1995; Brunner et al., 1996). Some applications of multilevel converters reported in (Damiano et al., 1997) are: compensation of reactive power (Waltrich and Barbi 2009). Large induction motor drives (Menzies et al., 1994) and active filtering (Damiano et al., 1997).

Other application of multilevel converters in areas of electric drives as reported in (Sinha and Lipo 1997); an inverter/converter is required in adjustable speed drives due to the variable voltage and frequency capabilities of converters. Problems due to traditional adjustable speed drives as opposed to multilevel speed drives are reported in (Sinha and Lipo 1997). Multilevel converter based unified power flow controller application in (Chen et al., 2000), STATCOM application using chain converters. Grid Photovoltaic system using single phase multilevel converter induction motor application, AC drive application, universal power conditioner application.

2.8 Cascaded MLI Topologies

This section will focus on reviewing cascaded MLI topologies. Analysis will be done with respect to newer or different topologies that have been presented in past recent years with focus on the number of components utilized, the number of dc source used, permissible levels of output voltage that can be generated, type of control method used and finally compare

advantages of the various topologies reviewed. It worth mentioning at this point that the various topologies of cascaded MLI been investigated comes in different categories; some do not include the H-bridge structure whiles others include, mostly the ones without H-bridge are unable to produce negative step voltages. Also there are topologies which by design are only able to generate positive step voltages.

2.8.1 Single-phase Cascaded MLI Topologies

Conventional multilevel inverter topologies; Flying capacitor, cascaded H-bridge and NPC can be formed into a cascaded topology. A cascaded topology simply means connection of several units of the fundamental topology into a series chain. Because cascaded H-bridge topology has already been presented above, only new cascaded MLI topologies will be discussed from this point forward. To achieve higher efficiency, reduced cost and less component size, a new cascaded MLI structure is introduced by (Aalami et al., 2018) with minimum number of components. The basic structure of the proposed inverter is shown in Fig. 2.7. The structure is made up of 2 dc sources and 10 power switches. The proposed inverter is a further development of the conventional H-bridge structure to increase the number steps generated at the output. The number of steps generated at the output is seven (7); which is an improvement of the conventional H-bridge structure. The cascaded topology of the presented inverter is achieved by utilizing only one H-bridge structure with several units of designed topology consisting of one dc source and two power switches. The required level of output voltage determines the number of units of the designed topology which are combined with the H-bridge inverter.

Two switches are connected in the upper and lower sections of the bridge inverter to provide bidirectional power flow for both section of the bridge inverter. Fig. 2.8 show the circuit diagram of cascaded topology which is capable of generating *n* levels of output voltage. Five different methods or algorithms are proposed to determine the magnitude or level of the dc source voltage and also to determine the following crucial parts of the converter: a. blocking voltage, b. maximum output voltage, c. number of possible output steps of voltage, d. number of variety of the converter.

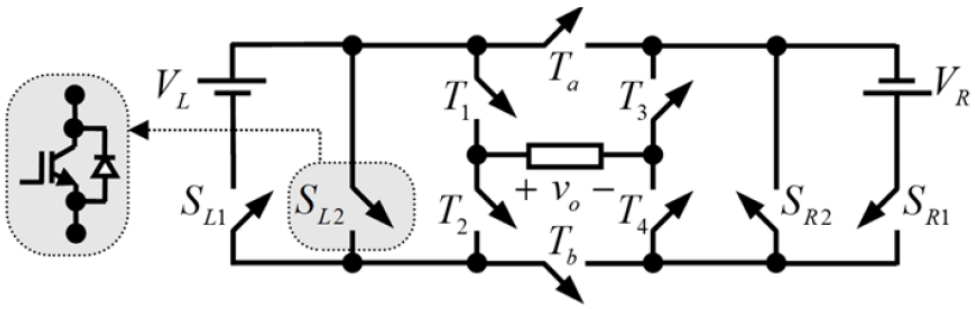


Figure 2.7: H-bridge based MLI (Aalami et al., 2018)

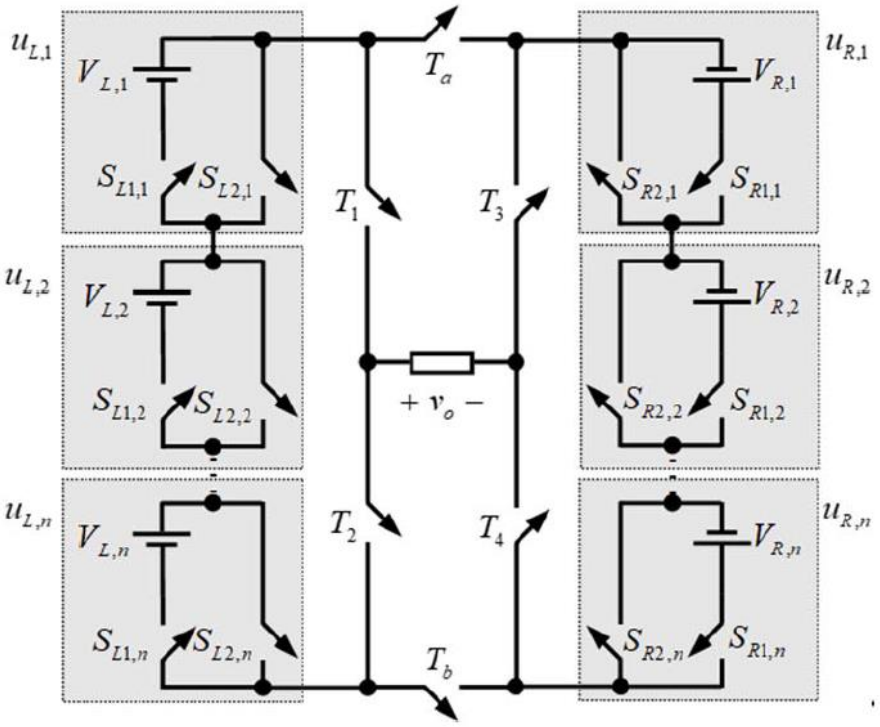


Figure 2.8: H-bridge based cascaded MLI (Aalami et al., 2018)

A new topology of cascaded MLI which has features of producing higher steps of output voltage whiles using limited number of components is presented in (Shahir and Babaei 2016). This topology has the ability to generate 16 steps of output voltage whiles maintaining less number of components as possible. The presented topology is able to generate only positive values of output voltage hence H-bridge structure is added to the topology to produce negative output

voltage. 16 steps of output voltage are generated without using the H-bridge structure. 4 dc source and 8 switches (two bidirectional switches and 6 switches) are harnessed in generating 16 positive steps at the inverter output. One major advantage of the proposed inverter is that; conduction losses is not really high due to the fact that only three switches are ON during generation of any level of output voltage which means that the switching losses will not be very high. Thirty-one steps of output voltages are generated when the H-bridge structure is incorporated in the basic unit. Fig. 2.11 show the basic unit of the proposed structure whiles Fig. 2.9 and Fig. 2.10 shows two cascaded structure of newly proposed topologies. 31-level output voltage of the same topology can be achieved with little changes to the basic unit. The presented topology when compared to previously published papers shows more advantages for the presented inverter in (Shahir and Babaei 2016).

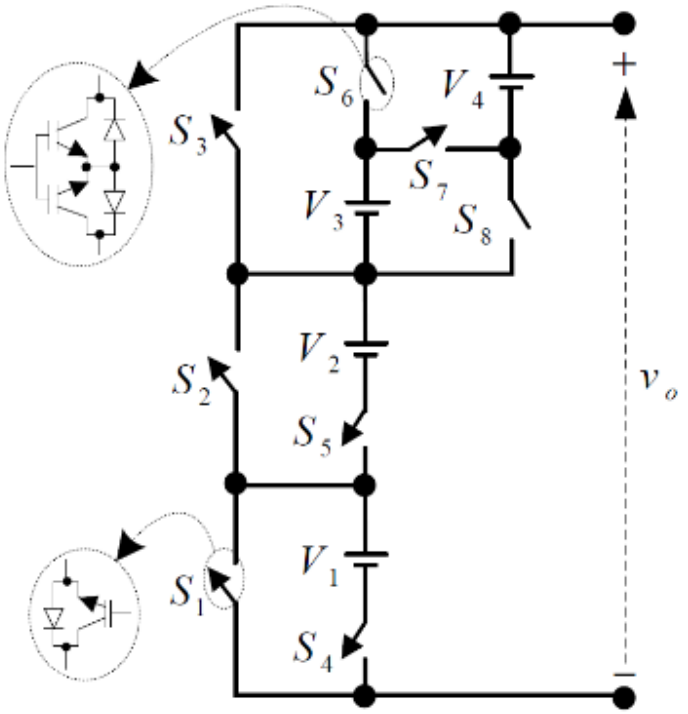


Figure 2.9: Basic unit of positive16-level MLI (Shahir and Babaei 2016).

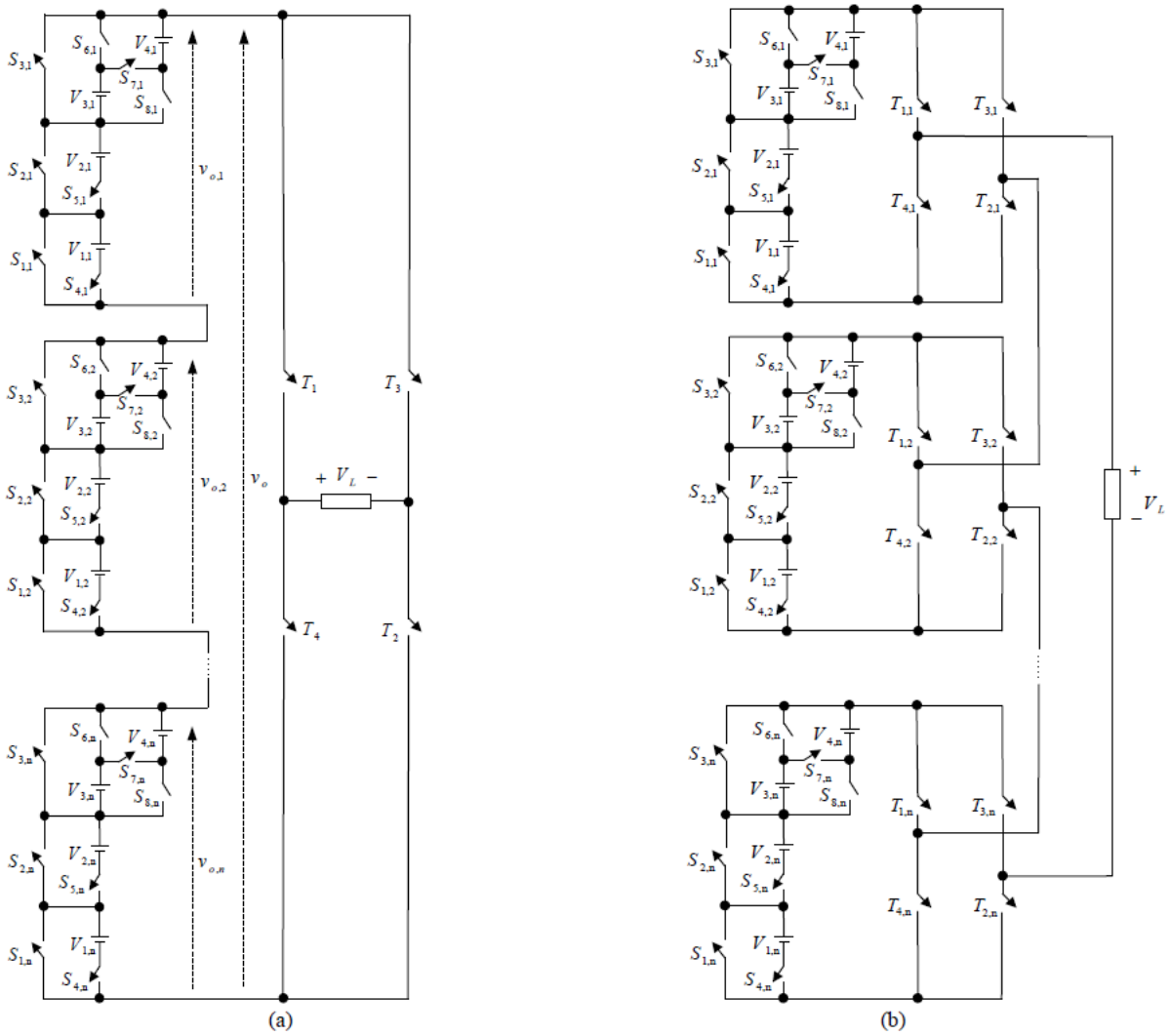


Figure 2.10: 31-level cascaded MLI (Shahir and Babaei 2016).

A new cascaded MLI with analysis from symmetric and asymmetric features utilizing reduced number of components is presented in (Babaei et al., 2016). The presented cascaded MLI has the capacity to generate 10 steps of output voltage by using 7 switches and 3 dc sources which are unequal in magnitude. One feature of the presented topology is the ability to generate only positive voltages, hence H-bridge inverter is required when negative output voltages are required to be generated. Fig. 2.11a and Fig. 2.11b shows the basic structure of the proposed inverter and output waveforms respectively. Two topologies are produced when the H-bridge

structure is added to the basic unit to derive the cascaded structure. The two proposed connections of the H-bridge are shown by Fig. 2.12a and Fig. 2.12b respectively. The basic unit is able to generate 19-steps of output voltage; this is possible due to connection of the basic unit and the H-bridge structure.

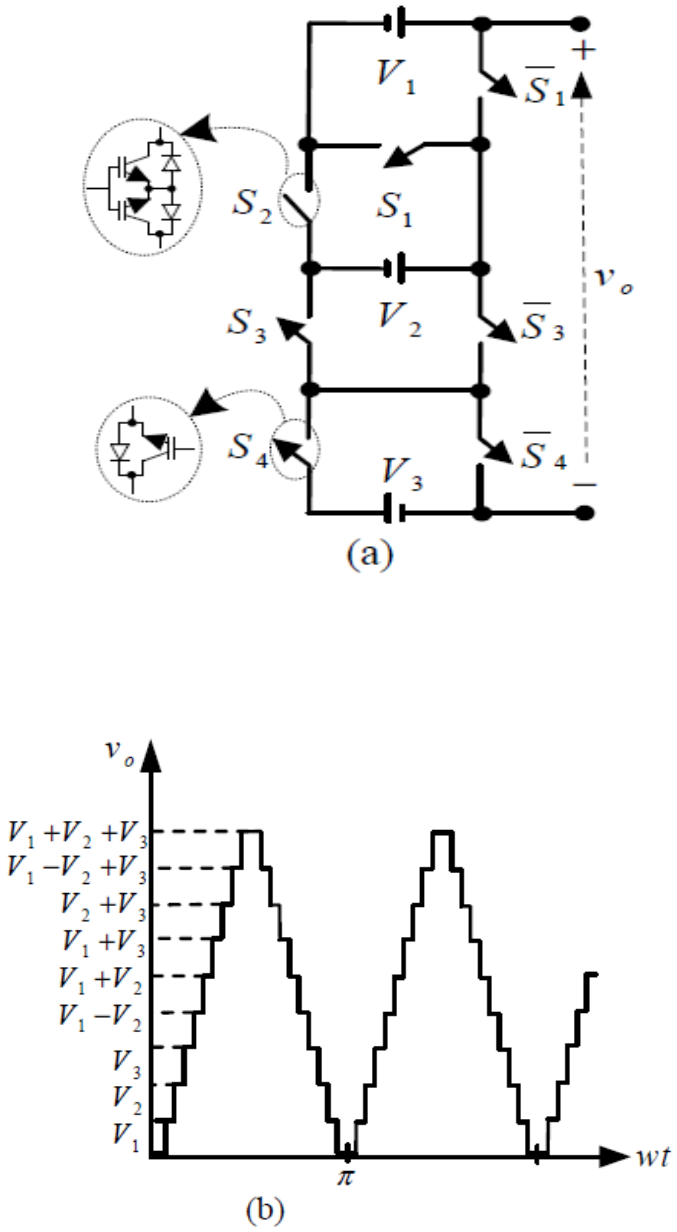


Figure 2.11: Positive 10-level inverter (Babaei et al., 2016).

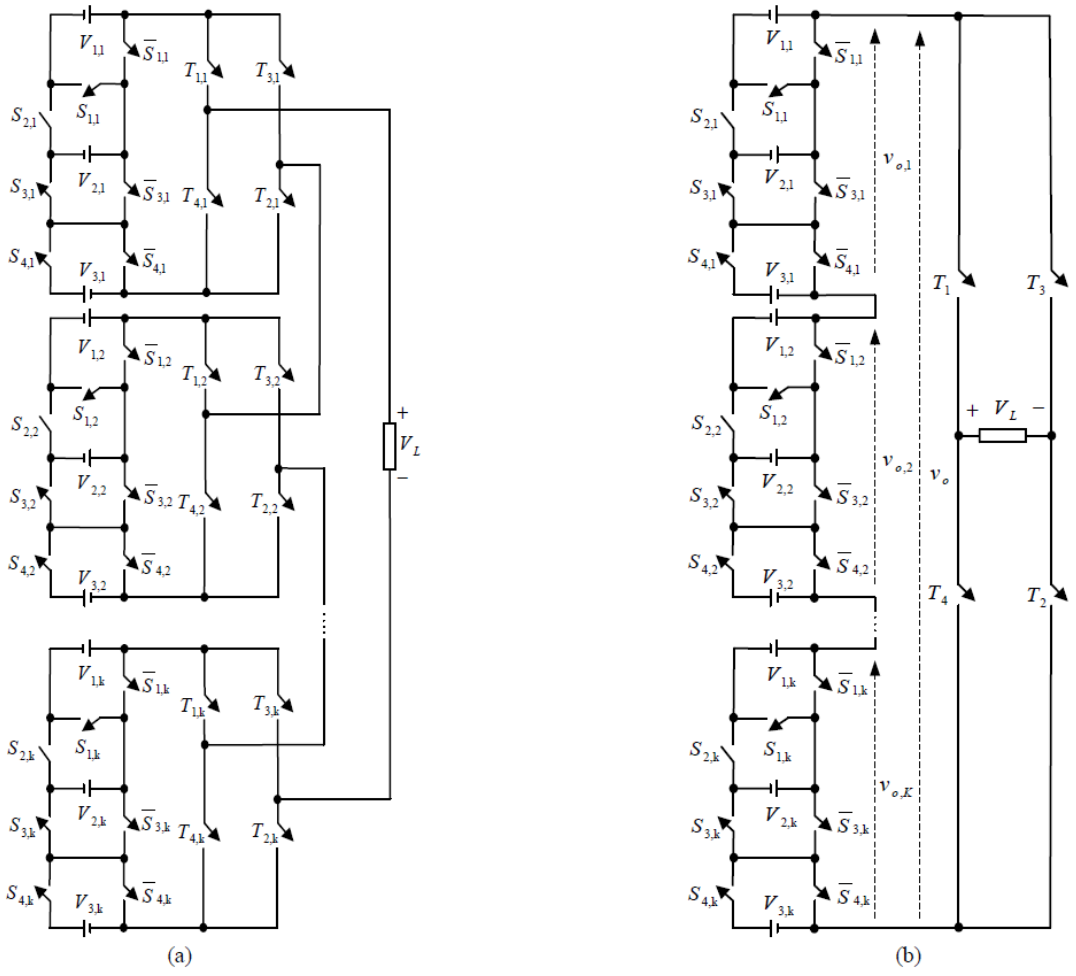
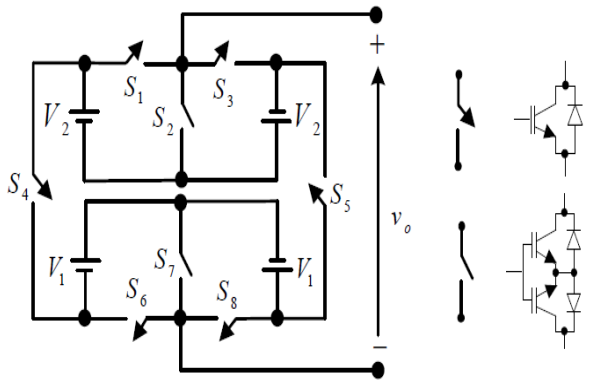


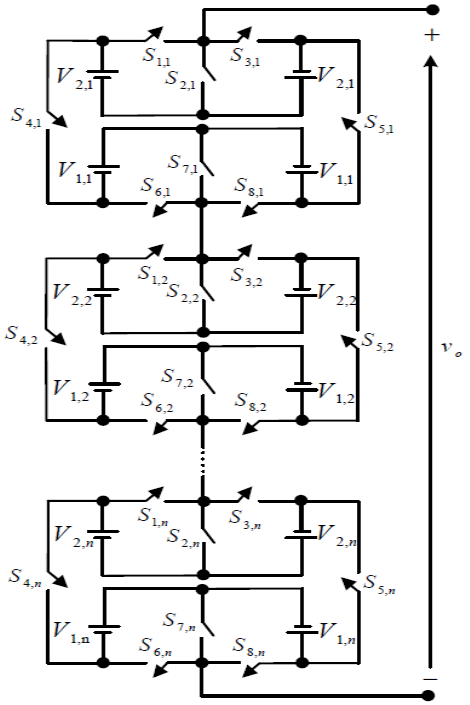
Figure 2.12: Cascaded multilevel inverter (Babaei et al., 2016).

A new topology of cascaded MLI was presented by (Sarbanzadeh et al., 2016). This topology combines bidirectional switches and unidirectional switches to generate the desired level of output power. 17-level of output voltage are generated by this proposed inverter; 4 input dc voltage and 8 switches are utilized to achieve the desired maximum output voltage. Fig. 2.13a shows the basic structure of the presented MLI topology. Fig. 2.14 shows all requisites switching states of the proposed inverter. Fig. 2.13b shows cascaded structure of the same presented inverter where several units of the basic structure are connected in series to achieve a certain level of output voltage. The results of comparison between the proposed topology and other presented topologies such as (Manjrekar and Lipo 1998; Alishah et al., 2015) are presented in

the paper (Sarbanzadeh et al., 2016). This presented topology is able to achieve higher levels of output voltage and also generate negative voltage at the output without using the H-Bridge structure.



(a)



(b)

Figure 2.13: Bidirectional and unidirectional switch based MLI (Sarbanzadeh et al., 2016)

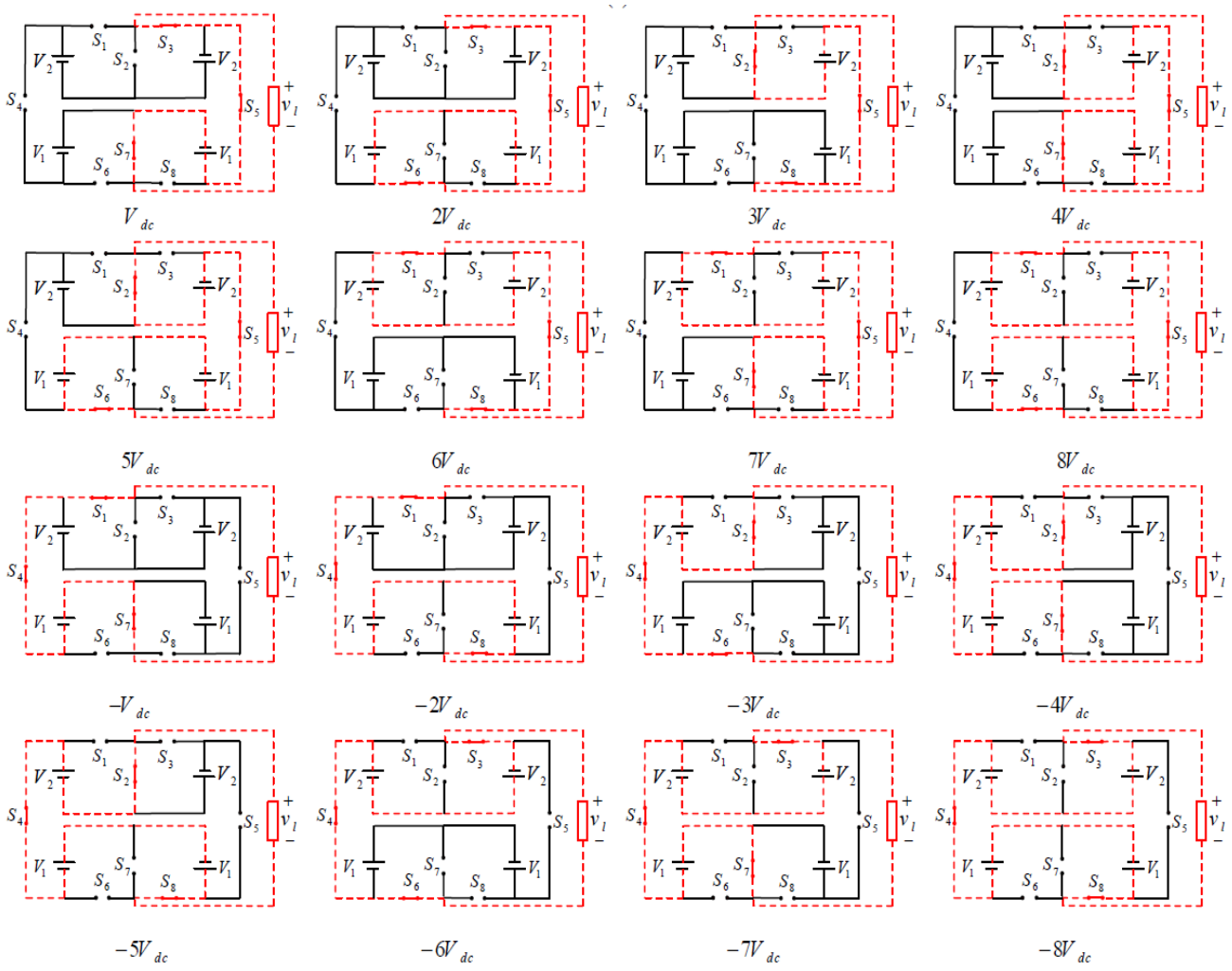


Figure 2.14: Switching states of presented MLI (Sarbanzadeh et al., 2016)

Two topologies of multilevel inverters which are dissimilar from the conventional multilevel inverter structures are presented in (Laali and Babaei 2016) and (Salehahari et al., 2017). In the topology presented in (Laali and Babaei 2016), a capacitor based basic unit structure is presented. The sources of the proposed topology are composed of one dc source and one capacitor, each connected to a separate unit of structure having two switches. In all, the overall structure is composed two sources and four switches and it's able to generate 3 steps of output voltage. In the topology of (Salehahari et al., 2017), 9-steps of output voltage are possible by the use of a coupled inductors, one dc source and 8 switches. The basic unit of the presented

hybrid coupled inductor MLI is represented by Fig. 2.15. Cascaded topology of the hybrid coupled inductor MLI is illustrated by Fig. 2.16.

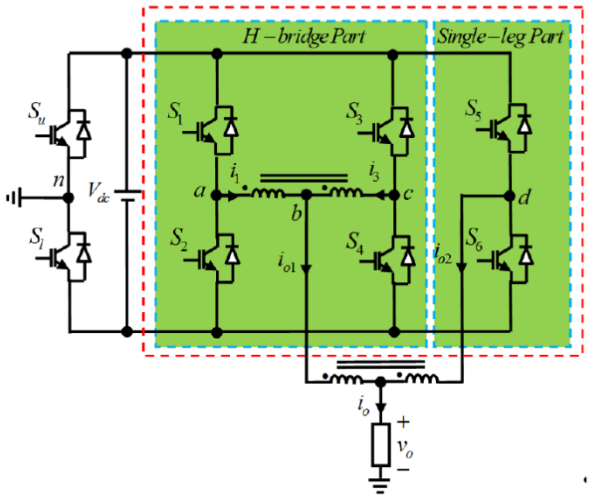


Figure 2.15: Hybrid coupled inductor MLI (Salehahari et al., 2017)

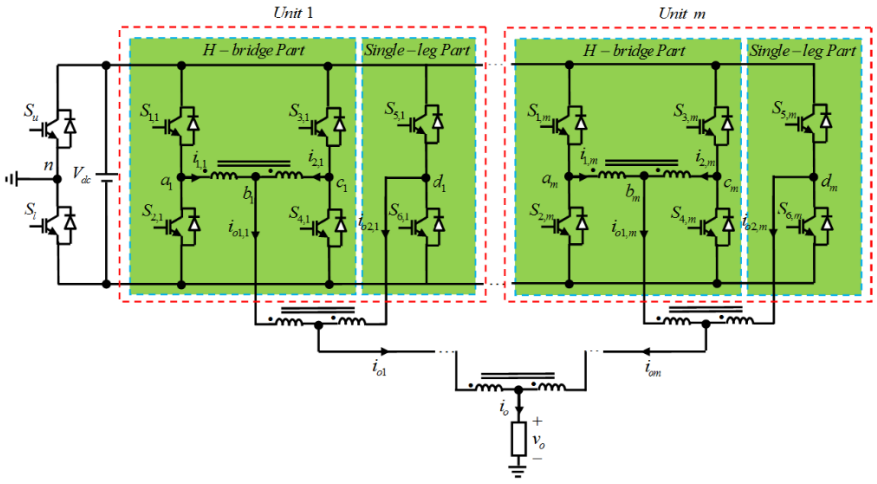


Figure 2.16: Cascaded hybrid coupled inductor MLI (Salehahari et al., 2017)

Another topology of cascaded MLI cable of generating 15-levels of output voltage utilizing less number of components is presented in (Babaei and Laali 2016). The proposed topology uses four dc inputs and eight switches in deriving the desired steps of output voltage. Extension of the 15 steps from the basic structure to a possible 71-steps in a cascaded structure is possible

and also represented in (Babaei and Laali 2016). The circuit of the basic structure of the proposed topology is given by Fig. 2.17 whiles the circuit diagram of the 71-steps is represented by Fig. 2.18. The topology of 15-level and 71-level output voltage is compared with other topologies (Laali et al., 2010; Hinago and Koizumi 2010; Waltrich and Barbi (2009). The following factors are used in the comparisons; capacity of the dc input voltage, the number of components used, and the standing voltage of the inverter, also the symmetric and asymmetric functionality of the source voltage.

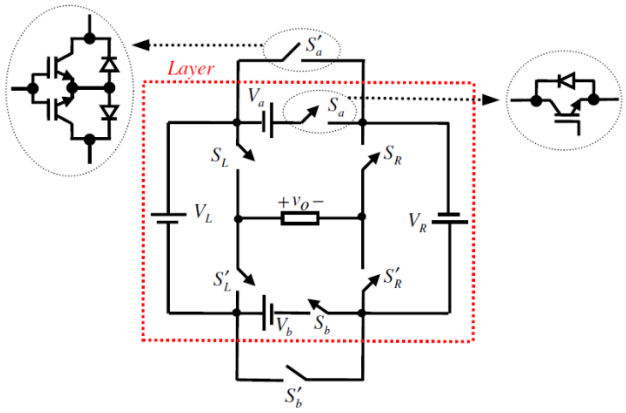


Figure 2.17: 15-level H-bridge inverter (Babaei and Laali 2016)

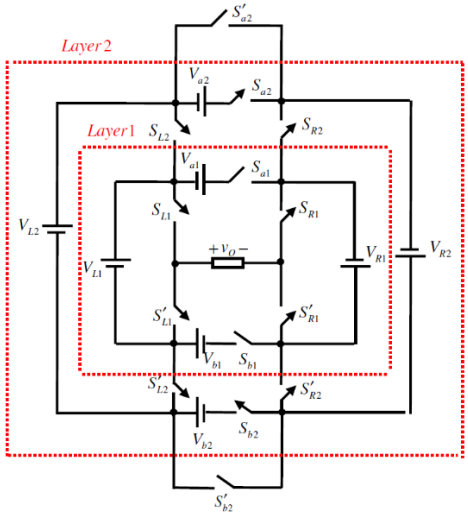


Figure 2.18: 71-level H-bridge inverter (Babaei and Laali 2016)

A further developed H-bridge multilevel inverter is presented by (Alilu et al., 2013). This topology is derived by including two switches and one dc source to conventional H-bridge topology; this results in a 7-level inverter. In all, the presented topology is composed of two dc sources and six power switches. Changing the polarity connection of one of the dc sources will results in the derivation of two topologies; these topologies are represented by Fig. 2.19a and Fig. 2.19b respectively. From the same presented MLI, 31-level and 127-level topologies are derived and represented by Fig. 2.20a and Fig. 2.20b respectively.

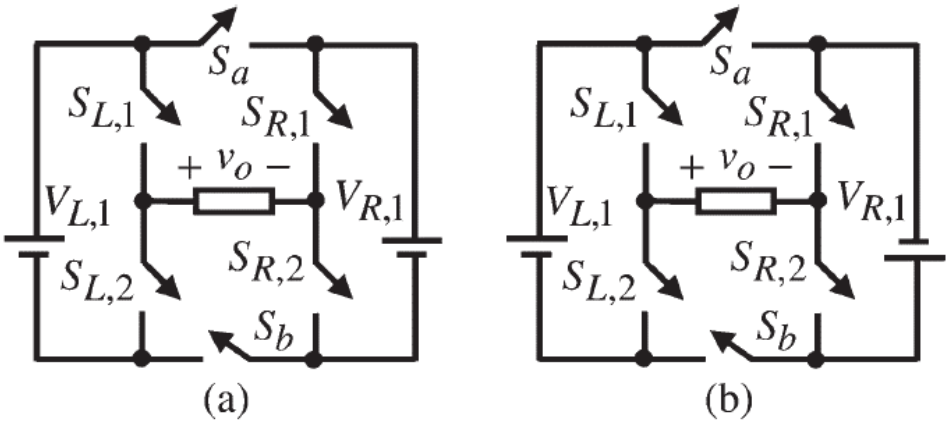


Figure 2.19: Fundamental multilevel inverter topology (Alilu et al., 2013)

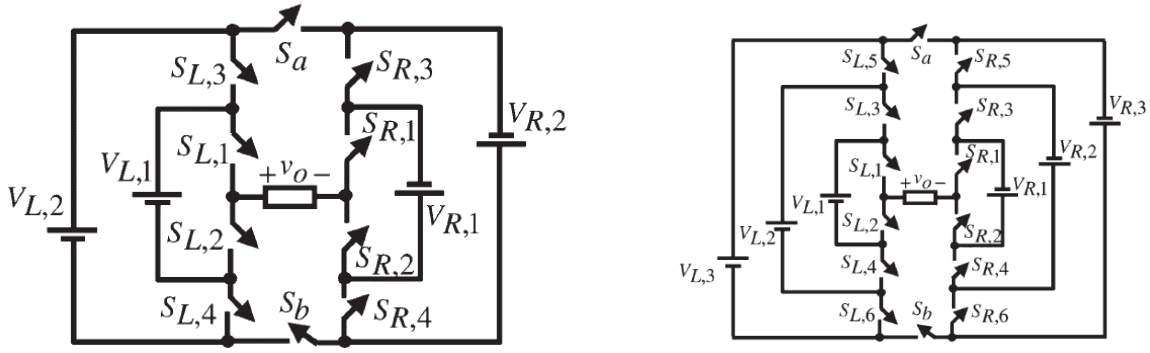


Figure 2.20: 31-level and 127-level developed H-bridge (Alilu et al., 2013)

In (Alishah et al., 2016), the presented topology is derived by linking sub units of multilevel topologies. This topology just as the previously reviewed topologies achieves better efficiency by utilizing the less amount of components, minimum blocking voltage across the switches, and minimum number of dc sources but generates higher steps of output voltage. The fundamental unit of the proposed topology is given by Fig. 2.21 whiles the cascaded unit is derived by cascading the basic unit. The fundamental unit of the proposed topology in (Alishah et al., 2016) is able to produce 17-steps at the output voltage. This topology is also a further development of the H-bridge structure, hence without considering H-Bridge structure, the following equations valid in determining the component count for the following: IGBTs, driver circuit and dc sources. N is the number of units in the sub-multilevel.

$$N_{IGBT} = 4n + 4 \tag{2.3}$$

$$N_{driver} = 2n + 6 \tag{2.4}$$

$$N_{dc} = 2n \tag{2.5}$$

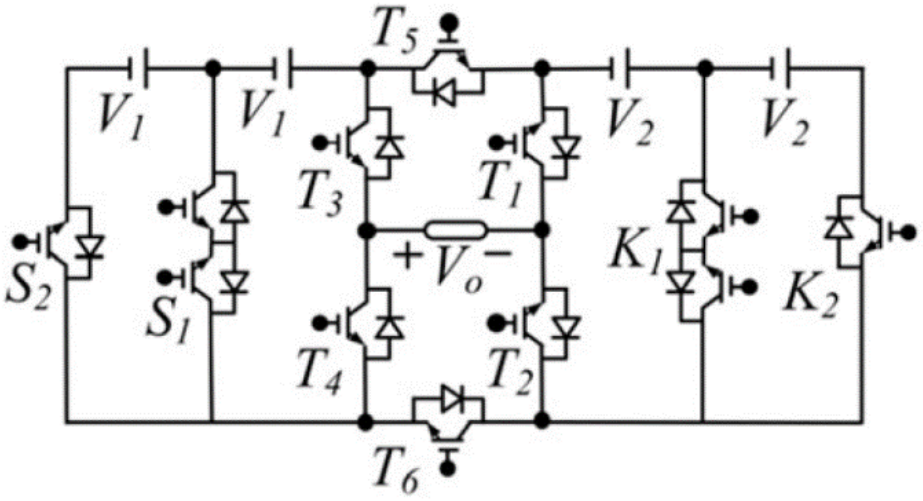


Figure 2.21: 17-level single-phase inverter (Alishah et al., 2016)

2.8.2 Three-phase Cascaded MLI Topologies

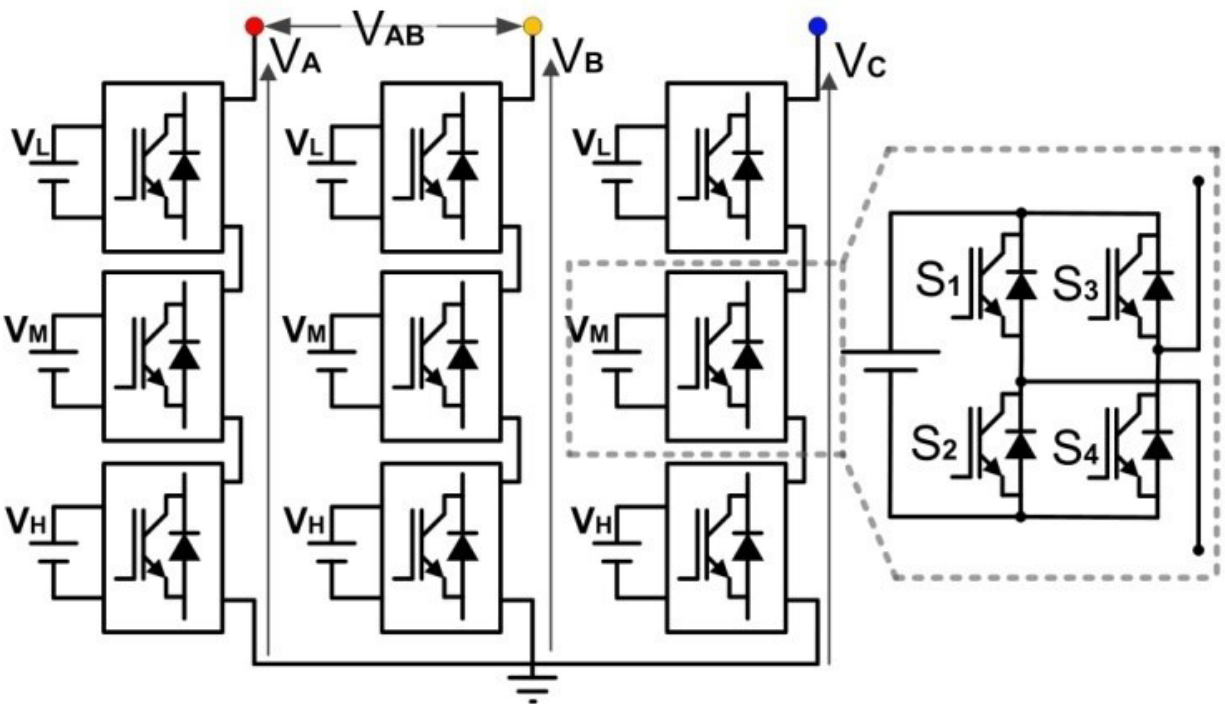


Figure 2.22: Three-phase cascaded H-bridge MLI (Chattopadhyay and Chakraborty 2015).

All three conventional multilevel inverters; cascaded H-bridge, NPC and Flying capacitor topologies can be presented in either single or three phase topology. Preference will however be given to cascaded MLI topologies in three-phase form at this juncture of my research. Fig. 2.22 shows three-phase conventional cascaded H-bridge topology; the three-phase topology inherits all the advantages of the single-phase topology. Symmetric or asymmetric topologies can also be derived in the three-phase topology. The three-phase topology is basically three units of the single-phase structure. The number of output step is determined by either the number of basic structure used or the nature of the dc sources applied (symmetric or asymmetric). Analysis of asymmetric topology is presented in (Chattopadhyay and Chakraborty 2015). Cascade H-bridge three-phase MLI structure is one of the most commonly used inverter in industry and academia. Fig. 2.23 shows a 9-level three-phase NPC MLI. Comparing the two topologies of Fig. 2.22 and Fig. 2.23 yields the following results: 48 switches are used by both topologies; the cascaded H-bridge uses 12 dc sources whiles the NPC topology uses only one dc source but requires 8

capacitors to achieve multilevel functionality. Also the NPC topology requires 63 extra diodes for voltage clamping purposes; a feature which is absent in the cascaded H-bridge topology. The component count in the NPC topology is quite higher than cascaded H-bridge topology. Therefore, the price, size and volume of NPC is more than that of cascaded H-bridge.

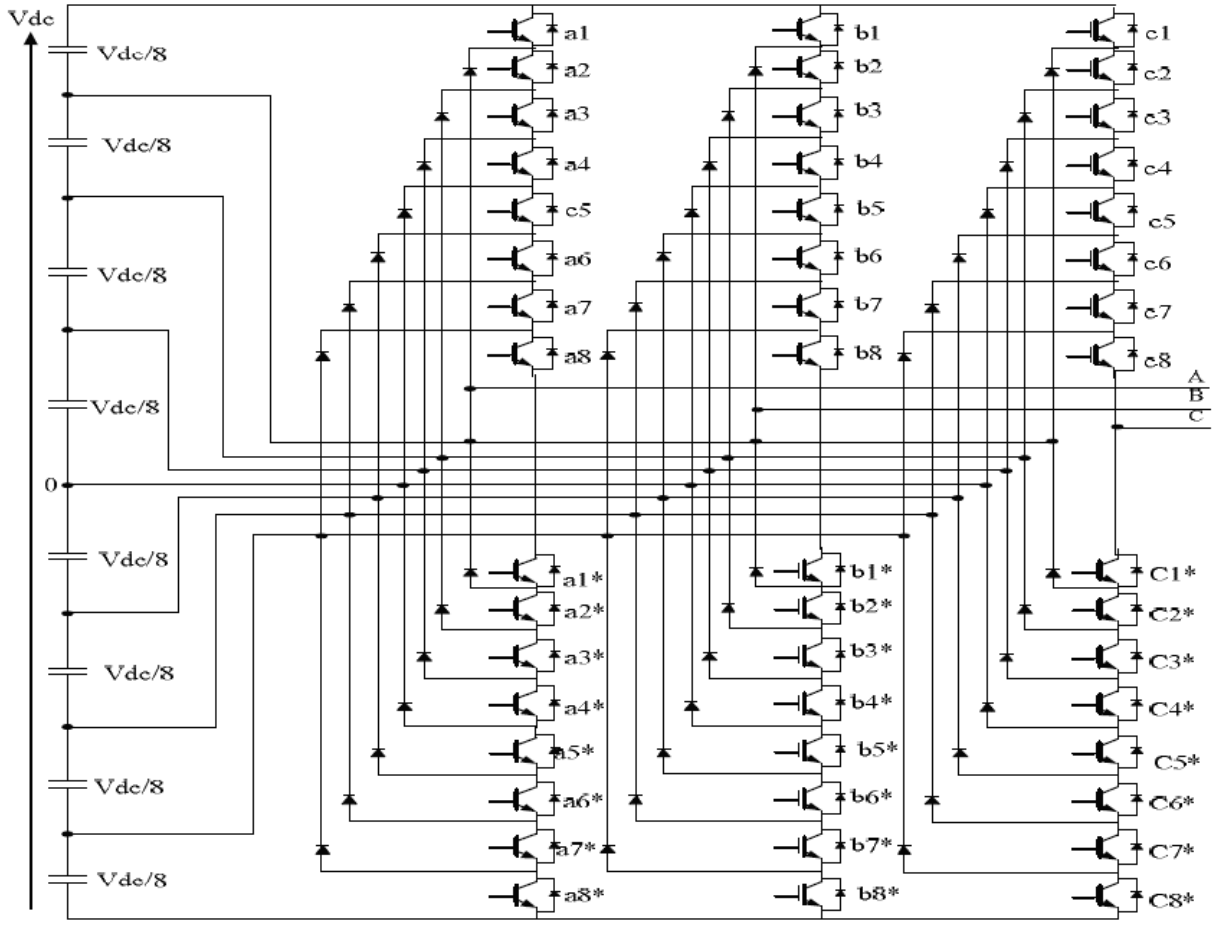


Figure 2.23: Three-phase NPC MLI (Chattopadhyay and Chakraborty 2015).

A novel topology of three-phase cascaded MLI is presented by (Waltrich and Barbi 2009). Compared to the conventional cascaded H-bridge topology, the proposed topology utilizes power cells and half bridge inverter legs to achieve the desired level of output voltage. The structure of the presented topology is presented in Fig. 2.24. The cost, size and losses of the presented topology is greatly reduced because less number of switches are utilized. A modified

version of the cascaded H-bridge MLI topology is presented in (Uthirasamy et al., 201). This topology is a three-phase inverter of 7-level output voltage which is applied in photovoltaic systems. The presented topology is a combination of sub modules and H-bridge structure, when compared to the conventional cascaded H-Bridge topology, the proposed topology utilizes less number of semiconductor switches hence reduced losses, minimum volume and size, simpler control methods and structure (Kangarlu and Babaei 2013; Ebrahimi et al., 2012). Fig. 2.24 represents the circuit diagram of the proposed topology.

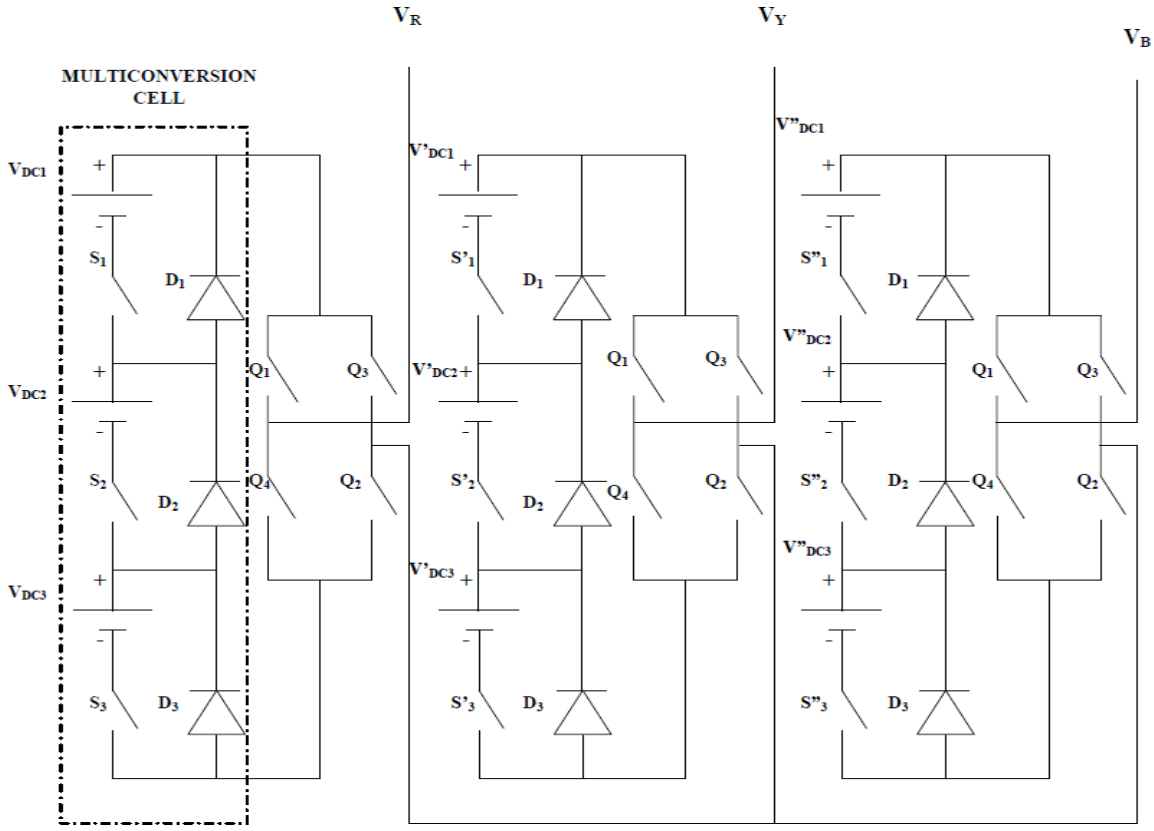


Figure 2.24: Full and Half H-bridge three-phase MLI (Uthirasamy et al., 2014).

In (Liu et al., 2014), impedance structure which is popularly known as Z-source but specifically a quasi ZS is combined with H-bridge inverter topology to achieve the desired topology known as quasi ZS cascaded MLI. This topology is quite different than the previously presented topology because the ZS structure which is embedded between the source and H-bridge structure

provides enormous advantages which is absent in all conventional MLI. Buck-boost functionality, better immunity to effects of EMIs, input voltage fluctuation capabilities and most importantly higher boost factor or voltage gain are some of the advantages of the presented structure because of the impedance network (Peng et al., 2003). Due to its capability to accept voltage fluctuations at the input, the proposed topology is ideal for photovoltaic system applications.

In (Fernão Pires et al., 2016), the quasi ZS structure is combined with T-type inverter to form a new topology for three-phase system. The presented topology combines advantages of quasi ZS and multilevel inverters. The quasi ZS topology has the advantage of reduced component stress due to the application of power switches with lower voltage ratings. Also constant input current can be provided by the source. The proposed topology has fault tolerance capabilities and the circuit is made up two quasi ZS circuits having symmetric features; one for the upper part and the other for the lower part as shown in Fig. 2.25.

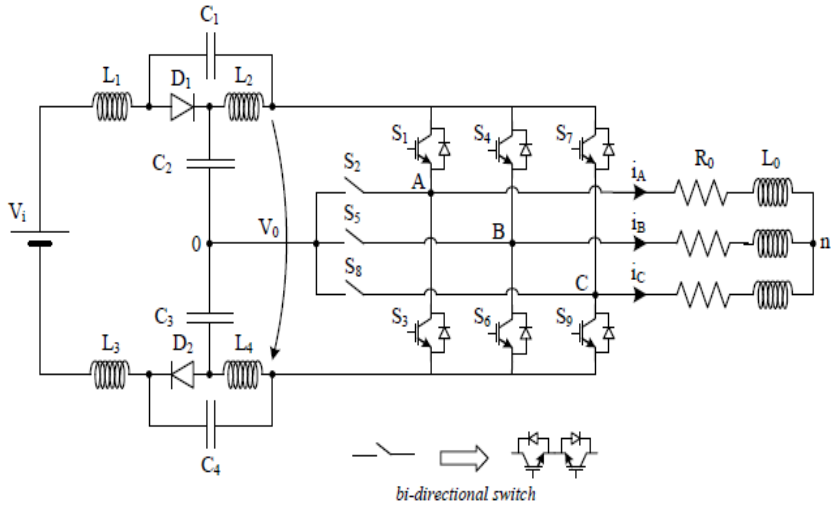


Figure 2.25: T-type ZS MLI (Fernão Pires et al., 2016).

In (Krishnan et al., 2018), a cascaded MLI inverter is presented; the basic unit of the presented topology is composed of four and two unidirectional and bidirectional switches respectively. Also the basic unit is powered by two dc sources. Analysis of symmetric and asymmetric functionality of the presented inverter is investigated experimentally. Fig. 2.46 shows the three-

phase connection of the presented topology whiles Fig. 2.26 shows the cascaded connection of one of the three phases. For symmetric functionality, the presented inverter is able generate 5 steps and 7 steps of output voltage when using one and two modules of the proposed inverter structure whiles its produces 9 steps and 15 steps of output voltage for asymmetric functionality.

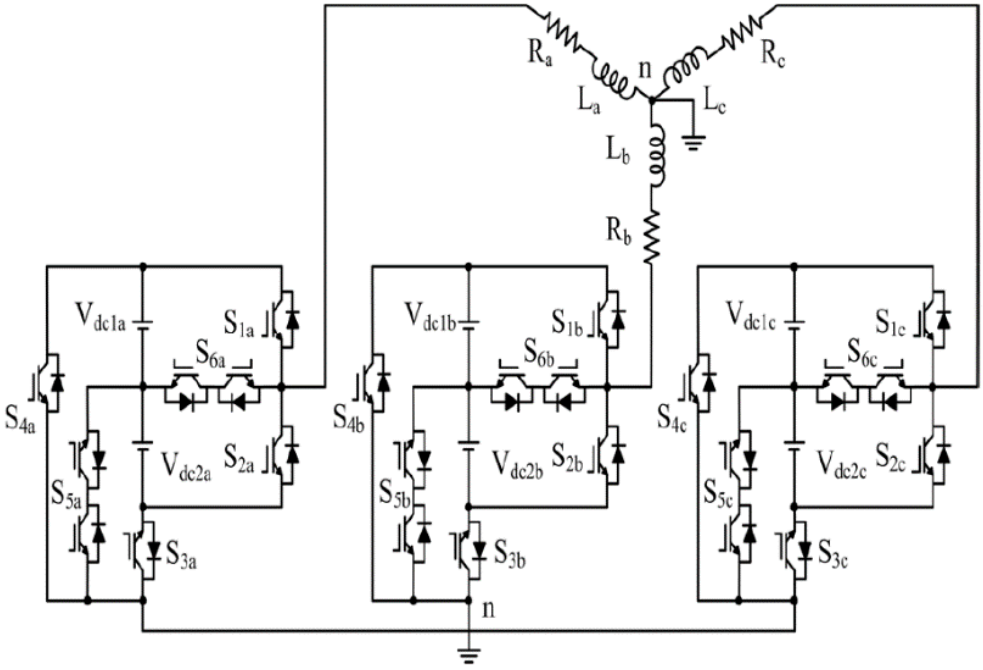


Figure 2.26: Three-phase cascaded inverter (Krishnan et al., 2018)

Modular multilevel inverters (MMLI) was first introduced by (Friedrich 2010). The main advantage of MMLI is the application of minimum number of components to achieve the desired level of output voltage. However, MMLIs have higher voltage stress on the switches. A new type of three-phase MLI is introduced in (Salem et al., 2015), this topology is modular in nature and exhibits all the characteristics of MMLI. The authors in (Salem et al., 2015) achieved higher steps of output voltage whiles utilizing minimum number of components and dc sources. A new feature called FC/L is introduced which is used to determine the number of components desired based on the pole of the voltage steps. The circuit diagram of the proposed MMLI in (Salem et al., 2015) is represented by Fig. 2.28. Each phase of the three phase topology has a unit which is made up of one source voltage and two switches, two switches are used for isolation purpose

and one dc source is shared by all phases. Fig. 2.27 shows the cascaded topology of the presented MMLI in (Salem et al., 2015).

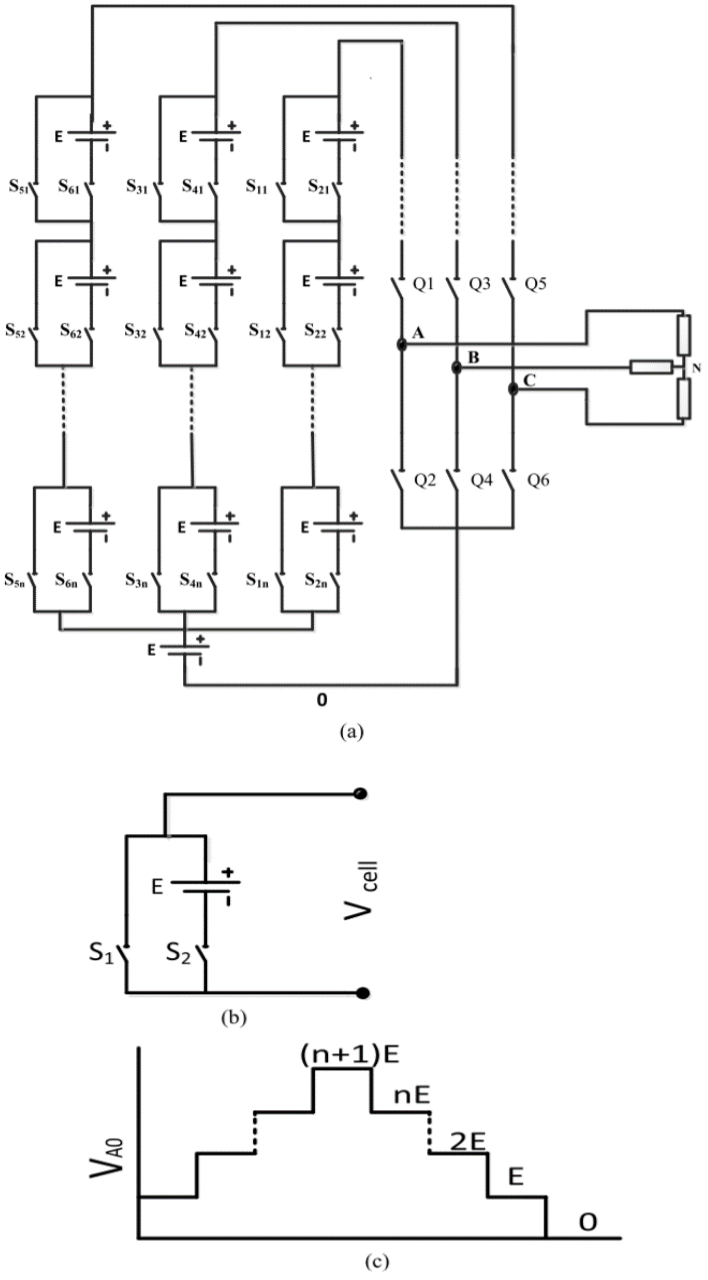


Figure 2.27: (a) Cascaded modular MLI (b) Basic unit (c) Output waveform (Salem et al., 2015)

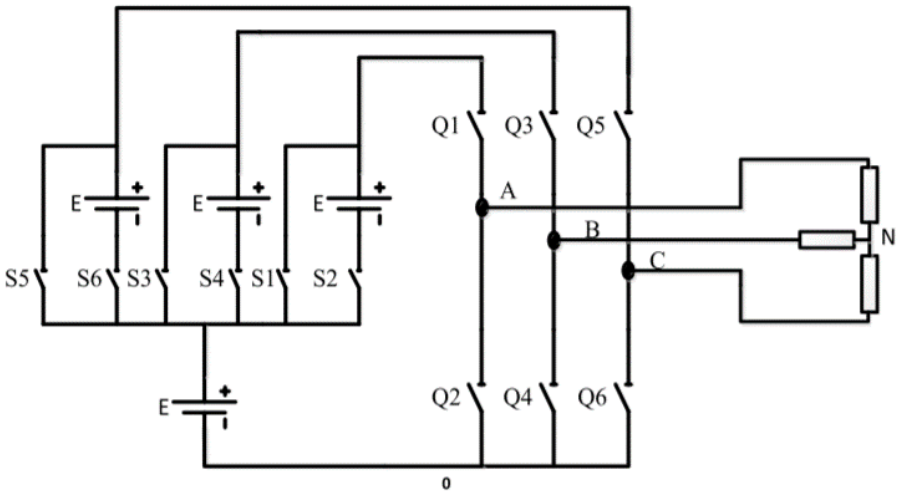


Figure 2.28: Three-phase modular MLI (Salem et al., 2015)

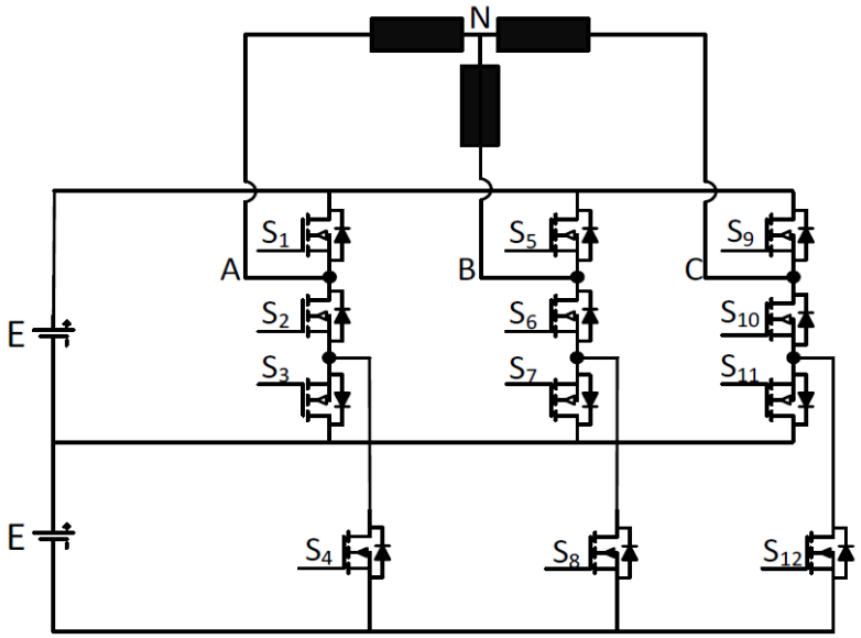


Figure 2.29: Modular multilevel inverter (Salem et al., 2015).

A novel topology of cascaded MLI is presented in (Hasan et al., 2018). This topology achieves multilevel functionality by employing half-bridge structures whiles the required polarity is generated by conventional H-bridge structure. Basically the structure of the presented topology is composed H-bridge and half bridge circuits. To provide isolation between the load and the

Table 2.7: Comparison study of selected topologies

Reference Topology	Output Voltage Level	Power Switch Quantity	Power Switch Type	DC Voltage Quantity	Other Components	Boosting Capabilities	Phase Type
Aalami et al., 2018	7	10	Uni	2	-	No	Single-phase
Shahir and Babaei 2016	16	8	Uni and Bi	4	-	No	Single-phase
Babaei et al., 2016	10	7	Uni and Bi	3	-	No	Single-phase
Sarbanzadeh et al., 2016	17	8	Uni and Bi	4	-	No	Single-phase
Salehahari et al., 2017	9	8	Uni	1	-	No	Single-phase
Babaei and Laali 2016	15	8	Uni and Bi	4	-	No	Single-phase
Alilu et al., 2013	7	6	Uni	2	-	No	Single-phase
Alishah et al., 2016	17	10	Uni and Bi	4	-	No	Single-phase
Chattopadhyay and Chakraborty 2015	9	36	Uni	9	-	No	Three-phase
Uthirasamy et al., 2014	7	21	Uni	9	9 Diodes	No	Three-phase
Fernão Pires et al., 2016	7	9	Uni and Bi	1	4 Capacitors 2 Diodes 4 Inductors	Yes	Three-phase
Krishnan et al., 2018	7	18	Uni and Bi	6	-	No	Three-phase
Salem et al., 2015	5	12	Uni	4	-	No	Three-phase

Note: Uni = Unidirectional Switch

Bi = Bidirectional Switch

grid, three-phase transformer is employed. The presented topology provides the following advantages when compared to similar topologies; less number of switches, easily scalable, minimum number of dc sources, simple control techniques.

2.9 Multilevel Inverter Control Techniques.

Using an appropriate control technique significantly contributes to achieving the required aim of having an efficient working converter/inverter. Several control schemes have been presented by researchers and majority of these control techniques fall within the ambit of the popular method known as pulse-width modulation (PWM) techniques which was first introduced by (Bhagwat and Stefanovic 1983).

According to (Josh et al., 2011), MLI modulation techniques can be categorized into the following sub groups:

a. PWM techniques
b. Non-PWM techniques

Further categorization of these groups is represented by Fig. 2.30, representing categorization of MLI modulation techniques proposed by (Babaei et al., 2007) whiles the detailed classification of MLI modulation techniques is presented by the authors in (Josh et al., 2011).

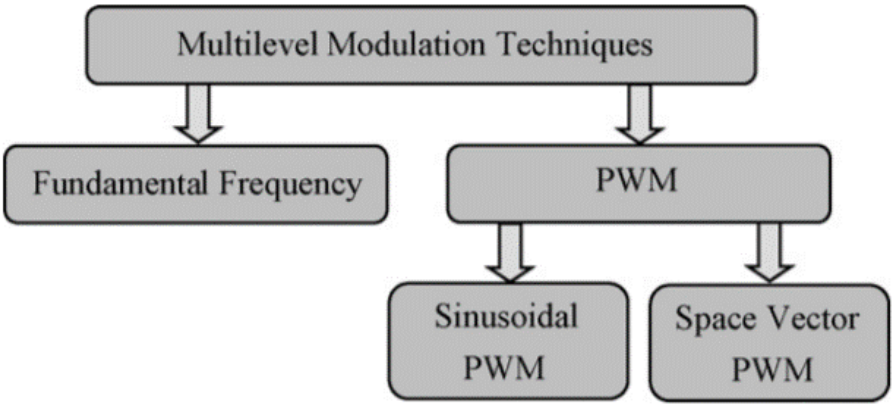


Figure 2.30: MLI modulation classifications (Babaei et al., 2007)

To understand the various PWM control methods, the following basic parameters should be explained mathematically:

$$m_f = \frac{f_c}{f_o} \tag{2.6}$$

$$m_a = \frac{A_0}{A_{CPP}} \tag{2.7}$$

$$m_a = \frac{A_0}{4A_{CPP}} \tag{2.8}$$

From equation (2.6), m_f is the modulating frequency whiles f_c and f_o are the carrier signal frequency and reference signal frequency respectively. From equation (2.7) and (2.8), m_a is the amplitude modulation index, A_{cpp} is the maximum or peak value of the carrier signal and A_o is the reference signal's amplitude. Equation (2) is the m_a formula for PS method and equation (3) is the m_a formula for CD method (Calais et al., 2001).

2.10 Conclusion

Multilevel inverters are classified into three main categories; cascaded H-bridge, Diode clamped and Flying capacitor topologies. Each topology has its own advantages and disadvantages. Cascaded topology however has received more literature review, development and application than the other two topologies. This due to its enormous merits such as simple structure, reduced number of components, modularity and unlimited output voltage levels, minimum size and weight, least cost of purchase and operation etc. The main disadvantage of this topology is the multiple number of dc sources required.

Multilevel inverters can be designed and operated either as single-phase or three-phase topologies without much difficulty; most three phase systems are obtained from three single-phase systems operated as one unit with 120^0 phase shifting. However, there are other three-phase systems which are not obtained from three single-phase units. Over the last decade, researchers are challenged to develop new MLI topologies which have at least one or more of the following advantages; reduced component count with higher levels of output voltage, reduced size, weight and volume, increased efficiency, high reliability and most importantly

reduced inverter cost and minimum cost of operation. Comparative study of the selected topologies has been presented in Table 2.7 on page 47, these topologies are juxtaposed with to each other with respect to several parameters of comparison such the level of output voltage, the type of switch, phase type etc.

The control of MLI can easily be achieved with any PWM based control techniques. However, other control techniques which are not part of PWM methods such as fundamental frequency can be applied. The desired quality output waveform of MLI topologies are always a trade-off between high switching and low switching frequencies. High switching frequencies provide quality output waveforms but increases the switching losses but low switching frequencies provide minimum switching losses but reduced output waveform quality.

CHAPTER 3

INVESTIGATION OF MULTILEVEL INVERTER BASED DYNAMIC VOLTAGE RESTORERS

3.1 Introduction

In recent years, the quality of power supplied to utility consumers by utility providers is of great concern. This is mainly because of load types used by power consumers and also utility providers. Voltage disturbances made-up of voltage dip, voltage swell, flickers, unbalances and harmonics are the frequently faced power quality (PQ) problems by utility providers. Voltage disturbances when not appropriately mitigated leads to destruction of critical and sensitive loads located in hospitals, factories and office buildings. Sensitive loads in power systems are very susceptible to the quality of electric power. Several devices which have been proposed or are currently being used to mitigate or resolve the drawbacks in power systems. These PQ mitigating devices are classified into two categories; series compensators and shunt compensator. In protecting sensitive loads, quality of supplied voltage is of outermost importance. Voltage and current compensation in low and medium power systems require series and shunt based compensating devices. Some power quality compensating devices have been listed below:

- DVR
- UPS
- TCT
- Flywheel
- DVC

The drawbacks which causes the quality of power to deteriorate can be traced to but not limited to the following (Moravej et al., 2009; Baggini, 2008; Sankaran, 2002):

- Voltage sag
- Unbalances
- Voltage swells
- Spike

- Harmonics
- Fluctuation

In the opinion of IEEE 1346 (IEEE 1998) standards, the definition of voltage sag is explained as a sudden or momentarily reduction in the nominal voltage provided by the utility and this reduction usually occurs for a short period of 1 minute and the percentage reduction usually ranges from 10% to 90%. On the hand, voltage swell is defined according to IEEE 1159 (IEEE 2019) standards as a sudden rise in the nominal voltage provided by the utility, period of the rise is also for a maximum of 1 minute and the percentage increase ranges from 110% to 180%. The following factors causes voltage dip (sag) (Kangarlu et al., 2017): short circuit faults, starting of motors, and sudden connection of large loads. Some negative effects of voltage swell are destruction of electrical appliances in factories such as motors, relays, and surge arresters (Babaei et al., 2010).

The number of sensitive loads being utilized in today's powers system has seen a drastic increase, this can be attributed to the increase use of smart or technologically advanced devices such as converters, computers and other devices which use microprocessor (Subasi et al., 2011). Therefore, it is imperative to provide high quality power and balanced (Babaei et al., 2010) in terms of amplitude and frequency to protect sensitive loads. Dynamic voltage restorer, abbreviated as DVR is a power electronic gadget, connected close to the load and in series to power supply at distribution level at PCC (point of common coupling) and used to resolve power quality disturbances mentioned above. In 1996, the first DVR topology was designed and installed by Westinghouse (Woodley et al., 1999). DVR's are considered economical device for voltage compensation because of its numerous advantages (Roncero-Sanchez and Acha 2009). Voltage magnitude, phase and frequency are three vital components in voltage restoration technique. This is achieved by injecting positive or negative voltage into the line to maintain the desired voltage levels. By commutation process, reactive power is injected into the lines whilst real power is injected by energy sources. Usually, DVR's are cited close to the load to reduce losses and increase efficiency. Basically the function of a DVR is to feed voltage into a transmission line with required voltage difference with the right magnitude, frequency and phase angle to compensate for the sag or swell (Marquard (1982). In practical systems, DVR can

produce up to 50% of the required nominal voltage to be injected into the lines but within a short time period of 0.1s but voltage swell and sag are far less than 50% of nominal voltages. DVR serves as a guard against damaging effects or power quality problems. Fig. 3.1 shows the simplified structure of DVR located in a power system and its mode of operation. More detailed discussions of published papers on various topologies of DVR's are found in the following (Praveen et al., 2004; Jing et al., 2008; Nielsen and Blaabjerg 2005).

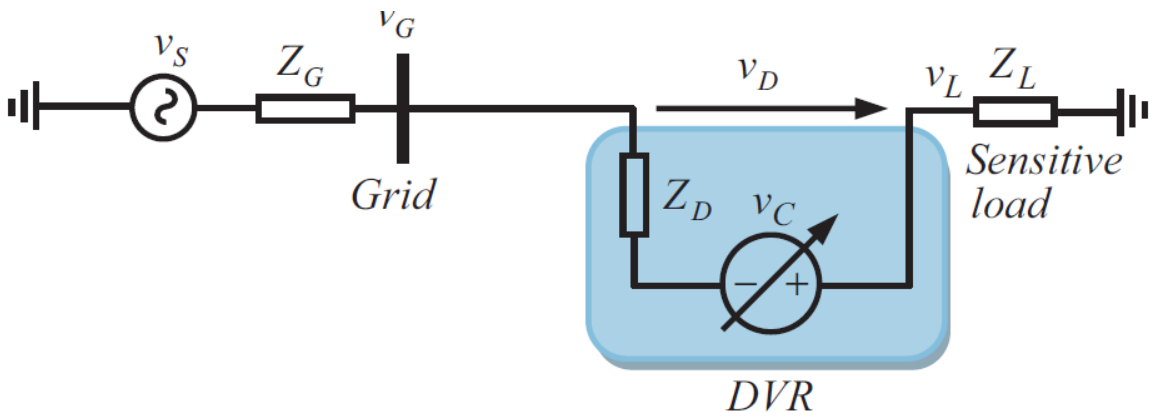


Figure 3.1: DVR equivalent circuit (Kangarlu et al., 2017)

V_s - supply voltage

Z_G - grid impedance

v_G - grid voltage

Z_D - DVR impedance

v_D - DVR voltage

v_L - load voltage

Z_L - Load impedance

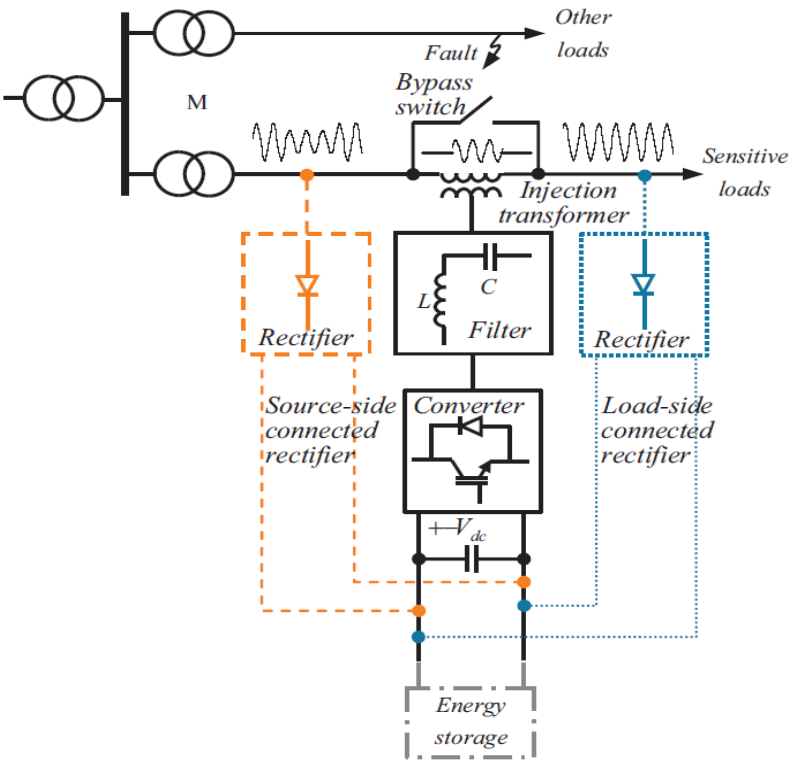


Figure 3.2: DVR location and mode of operation (Nielsen and Blaabjerg 2005)

Fig. 3.2 shows the general structure of the DVR topology. From the figure, the following components can be derived or DVR topology is mainly composed of the following four major parts or components:

- Converter
- LC filter
- Injection Transformer
- DC- Link

The DVR can be located either at the source side or at the load side as illustrated by Fig. 3.2. In this type of DVR, the compensating voltage is derived from the supply lines hence rectifier circuits are required to convert the ac voltage into dc voltage as the input voltage for the MLI.

3.2 DVR Components

The main components which constitute the DVR structure have been listed above. The central component is the converter; its basic function is to generate variable voltage to mitigate the disturbance of the power system. The type converter is dependent on the type of DVR structure

employed. Various converter topologies have been proposed and these ranges from single phase to three phase, MLI topologies, and impedance based topologies etc.

High frequency based harmonics can been found in the output voltage of converters which employ high switching frequencies. To reduce or eliminate these frequencies, a filter; LC is usually used to achieve this purpose of harmonic attenuation (Choi et al., 2002; Li et al., 2001). The mode of filter connection can be done in two ways:

- Converter side (Choi et al., 2002)
- Grid side (Li et al., 2001).

Both methods of filter connection have their merits and disadvantages, in the case of the converter side connection, the following merits are gained (Farhadi Kangarlu et al., 2017):

- Maximum harmonic content is eliminated because the filter position is close to the source of harmonic generation.
- Transformer ratings are not affected because high order harmonics cannot flow into the transformer.
- The voltage stress on the transformer is minimized.

Because DVR is series custom device, it functions as a series load with respect to the system source. Hence the filter inductor will introduce the following problems when connected at the converter side:

- Series transformer will experience voltage drop.
- Magnitude difference in fundamental components.
- Phase difference in the fundamental components.

The function of injection transformer is to connect or transfer the output of the DVR to distribution system and acts as isolation device to separate the DVR topology from power system when desired power quality is attained. Low frequency transformers are used as injection transformer; this increases the weight and cost of the overall structure. To resolve this, high frequency converters are used to replace low frequency transformers (Goharrizi et al., 2012; Jimichi et al., 2009). Not all DVR topologies have injection transformers; these DVR topologies are referred to as Transformerless DVR (TDVR) (Ansal et al., 2016; Visser et al., 2002). TDVR do not experience the following problems associated.

- Saturation currents.
- Inrush currents.

Also TDVR have the following advantages (Farhadi Kangarlu et al., 2017):

- Reduced weight.
- Reduced volume.
- Reduced cost.

ESS are required by some DVR topologies to provide needed power/voltage to mitigate against voltage sag. Using ESS will require inverter devices to provide the needed inversion process. Some ESS utilized in DVR topologies are:

- Fly wheels (Babaei et al., 2014; Babaei et al., 2010)
- Batteries (Li et al., 2008; Omar and Rahim 2012; Somayajula and Crow 2015)
- Superconductors (Wang and Venkataramanan 2007; Perez et al., 2006)
- Supercapacitors (Babaei etal., 2010; Lozano et al., 2010)

Between the distribution feeder and DVR topology is a device called bypass switch which is activated to link or isolate the DVR topology from the circuit. In event of high quality power, the switch is closed to isolate the DVR but it's opened when there's the need to provide compensation to increase the quality of the feed (Farhadi Kangarlu et al., 2017).

3.3 DVR Operational Range

Applying KVL to Fig. 3.1 will yield the equation below:

$$\overrightarrow{V_L} = \overrightarrow{V_G} + \overrightarrow{V_D} \quad (3.3)$$

Where:

$\overrightarrow{V_L}$ is the vector load voltage.

$\overrightarrow{V_G}$ is the vector grid voltage.

$\overrightarrow{V_D}$ is the vector DVR voltage.

Relationship between the vector DVR voltage, modulation index (M) and the dc input voltage (V_{dc}) and the converter side transformer turns ratio (a) is expressed by:

$$\left|\overrightarrow{V_D}\right| = aMV_{dc} \quad (3.3)$$

Voltage sag per-unit value with respect to rated value of base load voltage is expressed by:

$$\mathrm{PU_{sag}} = \frac{|\mathrm{V_{L,rated}}|-|\mathrm{V_G}|}{|\mathrm{V_{L,rated}}|} = 1 - \left|\mathrm{V_{G,pu}}\right| \quad (3.3)$$

For in-phase voltage sag compensation:

$$|\mathrm{V_L}| = |\mathrm{V_G}| + |\mathrm{V_D}| \quad (3.3)$$

$$1 = \left|\mathrm{V_{G,pu}}\right| + \left|\mathrm{V_{D,pu}}\right| \quad (3.3)$$

Combining the above equations will yield:

$$\mathrm{PU_{sag}} = \mathrm{aMV_{dc,pu}} \quad (3.3)$$

The maximum voltage sag compensation value when maximum modulation index of 1 is given by:

$$\mathrm{PU_{sag}} = \mathrm{aV_{dc,pu}} \quad (3.3)$$

When the dc source voltage V_{DC} equals to the grid voltage V_G, then the maximum voltage sag compensation is expressed by:

$$\mathrm{PU_{sag}} = \mathrm{a}\left|\mathrm{V_{G,pu}}\right| \quad (3.3)$$

The volt-ampere ratings ($\mathrm{VA_{rated}}$) of the DVR is computed by:

$$\mathrm{VA_{rated}} = \left|\mathrm{V_{D,rated}}\right|\left|\mathrm{I_{L,rated}}\right| \quad (3.3)$$

Where $\mathrm{I_{L,rated}}$ is the load current ratings.

3.4 DVR Classification

The presented topology is a generalized topology hence does not constitute the only structure of DVR topologies available. Classification of DVR's can be done according to either the type of phase (single or three phase) or the conventional classifying method which based on the type of converter utilized. From the converter point of view classification, DVR's are categorized into the following groups:

- ac-ac
- ac-dc-ac

The difference between the above categories is the inclusion of energy storage system (ESS) to the latter group. Fig. 3.3 shows the classification of DVR based on ESS.

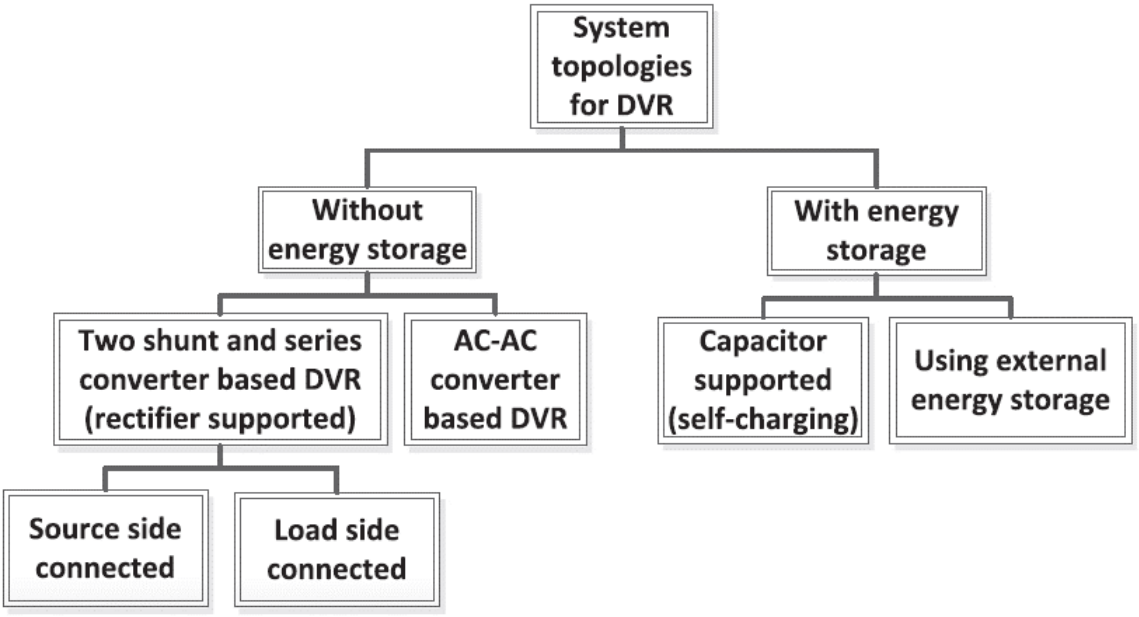


Figure 3.3: DVR classification based on ESS (Farhadi-Kangarlu et al., 2017)

ac-ac DVRs are topologies which do not need energy saving system. The power used to resolve compensations is derived from the supply line via a shunt active converter. The utilized shunt converter is not always a diode rectifier but active converter is most utilized. These type of DVR topologies without ESS are mostly used in power systems where the percentage decrease in nominal voltage during voltage dip is not high hence the supply side can provide the needed power to compensate voltage dip. This method however causes the DVR to draw more current from the power systems hence affecting other loads connected along the line. Contrarily, this method provides cost saving without using ESS (Farhadi-Kangarlu et al., 2017). Examples of ac-ac based DVR are found in the following topologies: matrix converter, impedance based topologies and direct and indirect converters (ac-ac) (Babaei et al., 2010; Perez et al., 2006). Fig. 3.4 shows DVR topology without ESS but with a shunt active converter. DVR based ac-ac topology has the following advantages: reduced cost, reduced size and weight, fast response time, unlimited compensation period. Impedance based topologies have high boosting capabilities. However, ac-ac based DVR topology has some demerits such as increased number of switches hence increased switching losses; ac-ac converters require bidirectional switches.

Also ac-ac topologies have complex structure and control techniques and also require special commutation techniques.

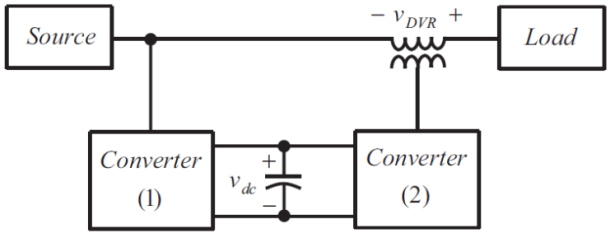


Figure 3.4: DVR without ESS connected at supply end (Farhadi Kangarlu et al., 2017).

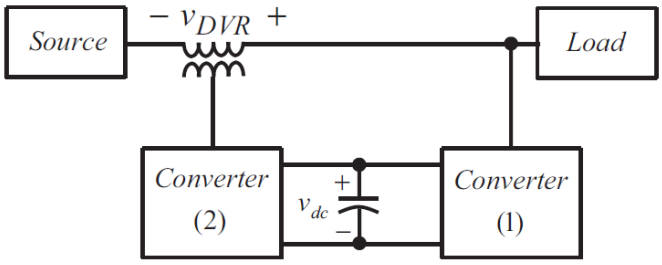


Figure 3.5: DVR without ESS connected at load end (Farhadi Kangarlu et al., 2017).

On the other hand, ac-dc-ac based DVR topologies require ESS. The power utilized for compensation is derived from the supply lines and stored in the ESS, also the compensating power can be derived from an external source; either ESS or dc-link. Fig. 3.5 shows the DVR topology with two stages of power conversion ie ac to dc and dc to ac, also the location of injcetd power is close to the load however, the topology in Fig. 3.6 is a single stage converter based DVR and its compensation energy is taken from ESS connected to a dc-link.

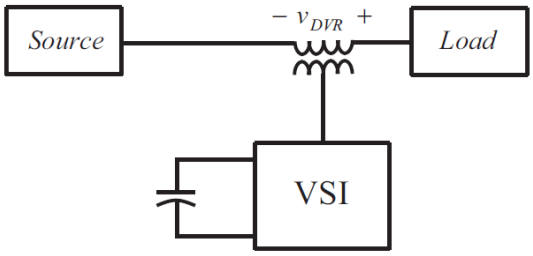


Figure 3.6: DVR with a dc-link (Farhadi-Kangarlu et al., 2017).

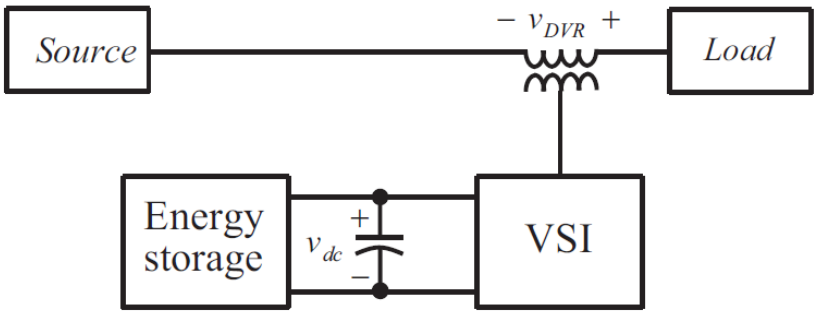


Figure 3.7: DVR with ESS (Farhadi-Kangarlu et al., 2017).

Multilevel inverter topologies are suitable for DVR based high power system because of the following merits: lower harmonic content, higher quality output power due to lower level of output steps, better electromagnetic functionality and finally lower losses.

There are three conventional MLI topologies; NPC, FC and cascaded H-bridge. Amongst these topologies, cascaded H-bride topology is frequently utilized because higher levels of output voltage can be produced with limited components, simple structure and control technique.

However, each basic unit in the cascaded chain requires its own dc source; this will no longer be a disadvantage because of the increased application of renewable energy especially solar energy. Also injection transformers are not required in cascaded topology when isolated dc sources are used; this results in a DVR topology with reduced size, reduced volume and reduced cost (Farhadi-Kangarlu et al., 2017). Fig. 3. 9 shows DVR topology based on cascaded H-Bridge with one and multiple dc sources. Hence there's a trade of between multiple dc sources and injection transformer. There are merits and demerits for the two cases.

MLI based DVR topologies have major limitation during voltage compensations. There is a major difference between the DVR output voltage and the required voltage during voltage dip compensations; this can be attributed to the wide difference in step output voltages of the DVR. Hence the desired magnitude of voltage required for compensation is not produced by the DVR and also the quality of the produced voltage is not the desired quality. A review of this problem is investigated by (Babaei et al 2014), to resolve this issue, dc-dc converter with adjustable dc link is proposed by (Babaei et al 2014). Comparative analysis of the 3-Ø DVR is presented in

(Farhadi-Kangarlu et al., 2017) each presented topology has its own advantages and disadvantages.

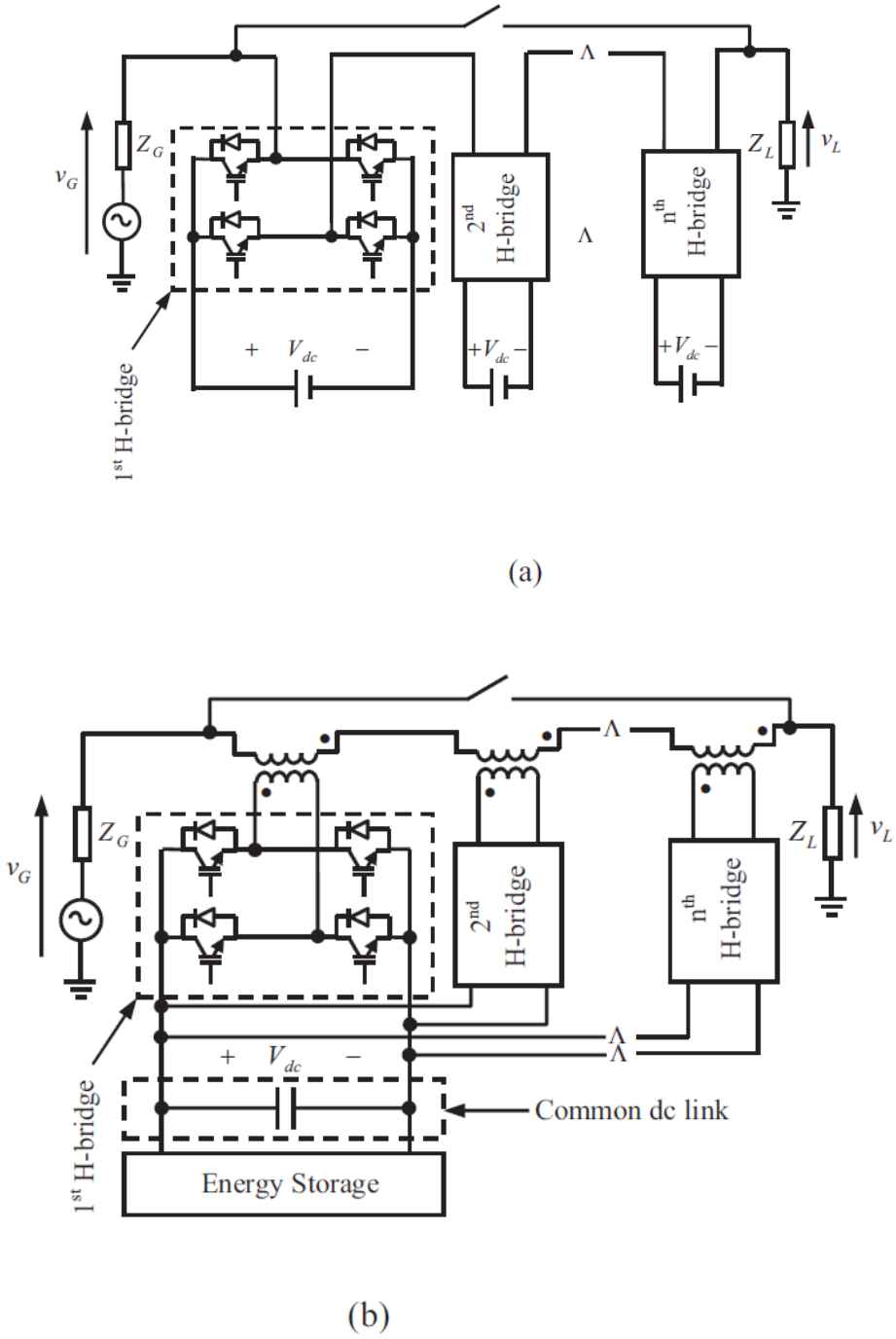


Figure 3.8: Cascaded H-bridge based DVR: (a) multiple dc sources (b) Single dc source (Farhadi Kangarlu et al., 2017)

3.5 DVR Control System

The block diagram illustrating the various stages in the control of DVR structure is represented by Fig. 3.10. The control system receives measured data from the supply side of the DVR. Swift detection of voltage disturbances is a critical function of the DVR; this will enable a quick response of protecting sensitive loads from the supply side disturbances. Several methods have been proposed for voltage dip diagnosis, a review of these techniques have been presented below (Bollen 2000; Fitzer et al., 2004; Saleh et al., 2008).

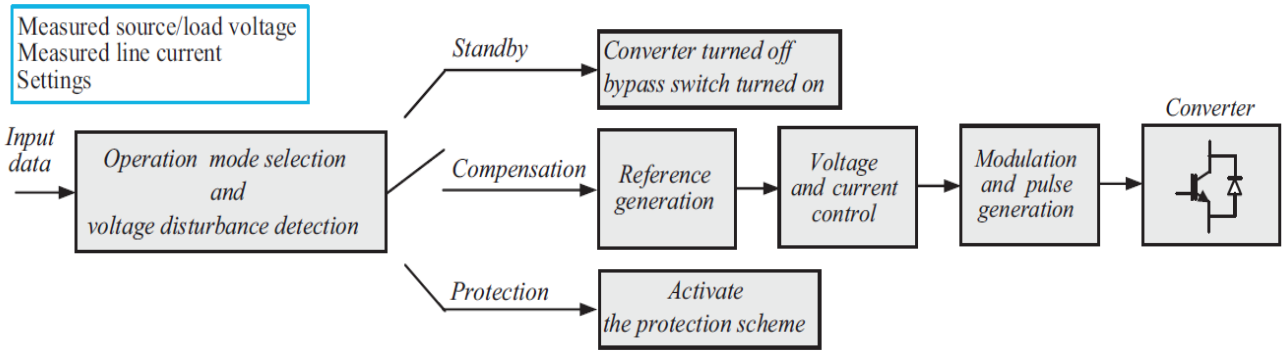


Figure 3.9: DVR control block diagram (Farhadi Kangarlu et al., 2017).

From the block diagram of Fig. 3.10, the control components of DVR are grouped into the following main categories:

- Detection of supply disturbance
- Generation of reference value
- Voltage and current controller
- Compensation techniques

RMS method of voltage disturbance detection is the most straightforward technique; this method works by comparing a reference value to the measured rms value, the difference is then compared to the acceptable range, if it's more than the threshold value, either voltage sag or voltage swell is observed. This method is simple to implement and apply but not satisfactory for DVR application due to low speed.

The second method is abc-dq transformation technique; here also, a reference value is compared to a measured value v_d to determine the presence of voltage sag or swell. This method is composed of reference producing system and is a core component of the DVR structure. This method has the advantage of fast response time and simple to implement. However, during the period of unbalanced voltage dip and swell compensation, the reliability of this technique is questionable due to the presence of dq components (Farhadi-Kangarlu et al., 2017; Fitzer et al., 2004). Authors in (Ciobotaru et al., 2006) proposes a technique of DVR control under unbalanced conditions.

Another control technique is the Fourier transform method. This method is also suitable for voltage dip and swell detection. This method is able to provide information about the level of:

- Swell/dip
- Harmonic
- Phase difference

However, it has the disadvantage of slow response hence not suitable for DVR application. This method (Fourier Transform) is used in monitoring the grid and providing information for each phase of the grid. To account for the presence of all frequencies, WFFT technique is most suitable and it's implemented digitally.

Finally, a quick technique for phase voltage disturbance detection is the WT (wavelet transform) technique. This method is gaining popularity as the desired technique for supply-side disturbance detection due to its numerous advantages such as quick response time and ease of implementation. The DVR core component is composed of the voltage controller and reference value generation system. The output voltage of the DVR required for the reference value should contain phase and amplitude. The compensation voltage produced by the voltage controller will have opposite polarity of amplitude and opposite angle with respect to the reference value; this is due to the type of compensation required. The type of compensation can either be phase and amplitude compensation or only one of them (phase or amplitude) compensation. Fig. 3.11 shows a conventional reference generation technique.

The main aim of DVR is to compensate the disturbances caused by the supply, this is done by injecting the desired power with required amplitude or magnitude and phase angle. Power or voltage compensation by DVR is achieved by three main techniques known as (Vilathgamuwa et al., 1999; Choi et al., 2000; Nielsen et al., 2001; Vilathgamuwa et al., 2003):

- Pre-sag
- In-phase
- Minimum energy

Also a hybrid technique which is derived from the combination of any of the above methods can also be used in power compensation. Compensation techniques and reference generation are dependent on each other, which is to say that injected power is dependent on the two factors. PLL is used in implementing the compensation of DVR hence the output of the PLL is heavily contingent on the compensation technique utilized.

In the case of pre-sag, PLL is latched onto phase angle of the grid voltage. The amplitude of the inject voltage much higher than the other techniques. Also significantly higher active power is injected during compensation which affects the capacity and duration of ESS or the drawn power from the supply line. Minimum energy (dc-link) is drawn during this method. Pre-sag technique is mostly suitable for cases where the load is highly sensitive to variations in the phase angle of the supply voltage. Hence the pre-sag method is suitable for cases where the load is not sensitive to phase angle variations. The pre-sag technique is best explained as maintaining the amplitude and phase angle of both pre-sag voltage and the load voltage (Nielsen et al., 2001). Fig. 3.12 shows the pre-sag compensation technique.

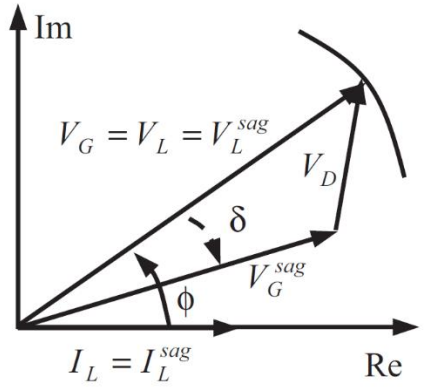


Figure 3.10: Pre-sag compensation (Farhadi Kangarlu et al., 2017).

However, in the case of in-phase compensation, phase angle derived from PLL output is a real-time measurement of the phase angle of the grid voltage. Minimum voltage is injected by this technique hence ESS and the supply line are not affected by drawn power. There is phase synchronization of the injected voltage and the supply voltage. Injection of active power is minimized in this technique however compensation of phase angle is not possible in this technique (Farhadi Kangarlu et al., 2017). Fig. 3.13 shows the in-phase compensation technique.

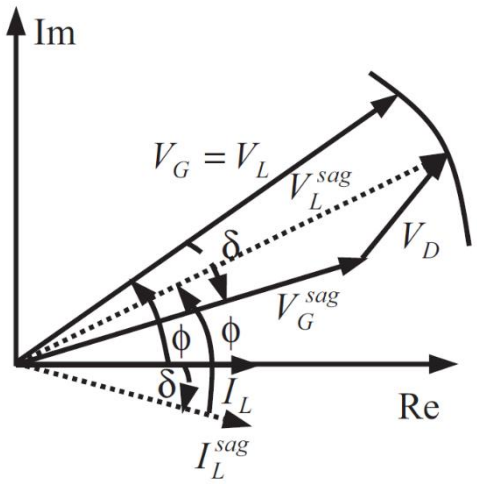


Figure 3.11: In-phase compensation technique

In the case of minimum energy technique (Vilathgamuwa et al., 1999), PLL output voltage is the sum of two factors namely: a) phase angle of the grid voltage and b) minimization equation. In this method the goal is to use reactive power for voltage dip compensation. Using this method will minimize the quantity of energy required from the dc-link because the desired reactive power for compensation is drawn from the supply line. Compensation periods are unlimited in cases where voltage dip is quite shallow (Farhadi-Kangarlu et al., 2017). Two major advantages of this technique can be found in (Farhadi-Kangarlu et al., 2017).

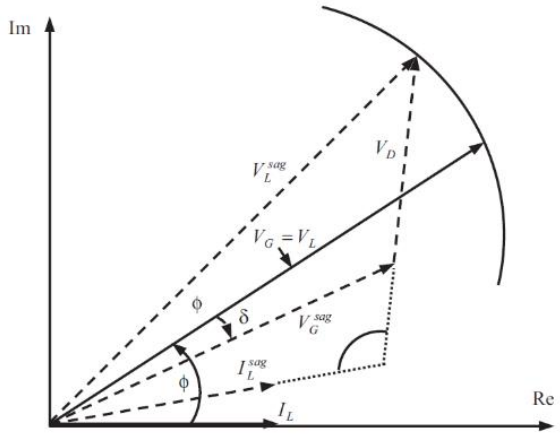


Figure 3.12: Minimum energy compensation technique

The final technique is the combination of the above techniques (hybrid) (Meyer et. Al., 2008). The major advantage of this technique is that the desired characteristics of the hybrid technique is obtained from the already existing methods; it also comes with the advantages but its limitations are mostly limited.

One of such hybrid technique is called optimized control method. The goal of this technique is to reduce distortions of the grid and also compensate long voltage dips using large phase jumps whiles reducing the stress on the dc-link. Hence the major components of the optimize control technique are small phase steps (jumps) and reduced voltage amplitude. Detailed explanation of this technique is found in (Farhadi-Kangarlu et al., 2017).

3.6 Application of DVR

The principal function of the DVR is to compensate voltage dip and swells caused by the supply-side disturbances. However, research has proven that DVR topologies can be used to resolve or perform function in the following case scenarios:

- Compensation of voltage harmonics (Newman et al., 2005)
- Flicker compensation (Sadigh et al., 2010; Ramirez et al., 2012)
- Compensation of frequencies (Jindal et al., 2008)
- Compensation of reactive power (Wu and Pei 2011)

The DVR topology should have protection against downstream fault current because these currents can cause destruction of the DVR structure (Axente et al., 2006). Bypass switches can

be used to achieve this aim or fault limiting techniques for DVR topologies can be applied; these methods are addressed in (Ajaei et al., 2011; Shuai et al., 2015). In the case of downstream fault current detection, the DVR topology injects voltage of negative polarity in series to the supply hence the fault current receives very minimum voltage thereby curbing the fault current significantly. The existence region in single-phase DVR can be reduced by sliding mode control (SMC) technique (Biricik and Komurcugil 2016) whiles time-varying and constant switching frequency SMC is applied in three-phase DVR (Komurcugil and Biricik 2017).

3.7 DVR Topologies

Conventional quasi ZS ac-ac converter is applied in DVRs as component of the DVR topology (Ahmed et al., 2016). The quasi ZS topology has the following advantages over the conventional ZS converter (a) reduced inrush current, (b) better reliability, (c) minimum harmonic content, (d) wide range input current functionality.

The presented converter topology requires isolating transformer for safety and isolation purposes. The type of transformer commonly used is known as line frequency transformer (LFT) and it has the following disadvantages: expensive, increased size and weight, increased losses, inrush current during starting and saturation. High frequency transformer (HFT) coupled with the quasi ZS topology overcomes the above mentioned limitations of LFT. Fig. 3.21 shows the presented converter of qausi ZS functionality.

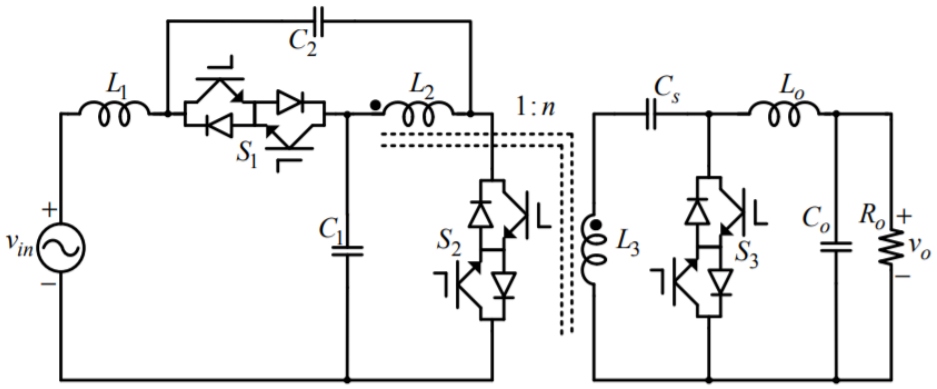


Figure 3.13: Quasi topology with HFT (Ahmed et al., 2016).

A half bridge ZS converter is presented by (Babaei and Shokati 2016). The presented converter structure is achieved by combination of impedance network and half bridge structure. One major advantage of the presented converter is the symmetric and asymmetric functionality for both positive and negative amplitudes. Also the presented topology has shoot-through functionality; a feature which is absent in the conventional half bridge structure. The presented converter has wide variety of industrial applications such as:

- Residential
- Electroplating
- Electrochemical

Although the presented converter is not applied in DVR topology, its numerous advantages makes it suitable for DVR application hence the mention of it by this research.

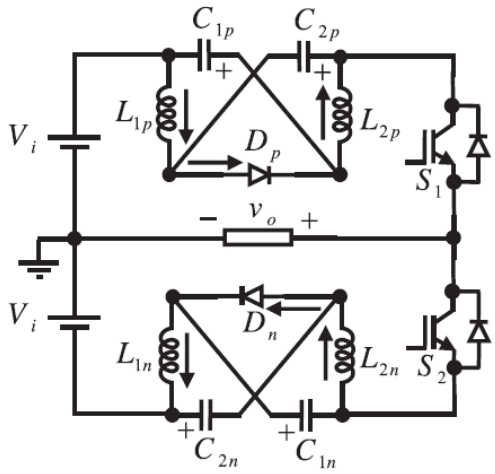


Figure 3.14: Half-Bridge ZS converter in (Babaei and Shokati 2016).

Cascaded ZS inverter based DVR is presented in (Banaei and Dehghanzadeh 2010). The presented system combines advantages of a cascaded structure and impedances based network. Some advantages of cascaded structures are high quality output waveforms, increased output amplitude whiles the merits of ZS are buck-boost capabilities, better protection against EMIs etc. A novel topology of DVR based on matrix converter is presented in (Lozano et al., 2010); this topology is able to compensate for supply side disturbances by taken power from the supply itself hence the need for ESS is not required therefore there's cost saving. Control of the matrix converter is achieved by SVM method. Also a 2 *x* 2 matrix converter based DVR topology is

presented in (Santoyo Anaya et al., 2011); this presented system has the ability to compensate disturbances having shorter and longer periods, also disturbances having high amplitudes can be compensated by the presented system. AC chopper based DVR topology is presented in (Parmar and Yadav 2016); feedforwad and feedback control techniques are employed in the control of the presented DVR topologies.

A DVR topology based on parallel connection of diode-clamped MMC is presented in (Lv et al., 2017). There's an automatic balancing of the capacitor voltage without applying any control method hence the need for capacitor voltage sensors in the sub module of the MMC is not required. A new method of compensation is also proposed. Fig. 3.23 illustrates the presented converter circuit of (Lv et al., 2017),

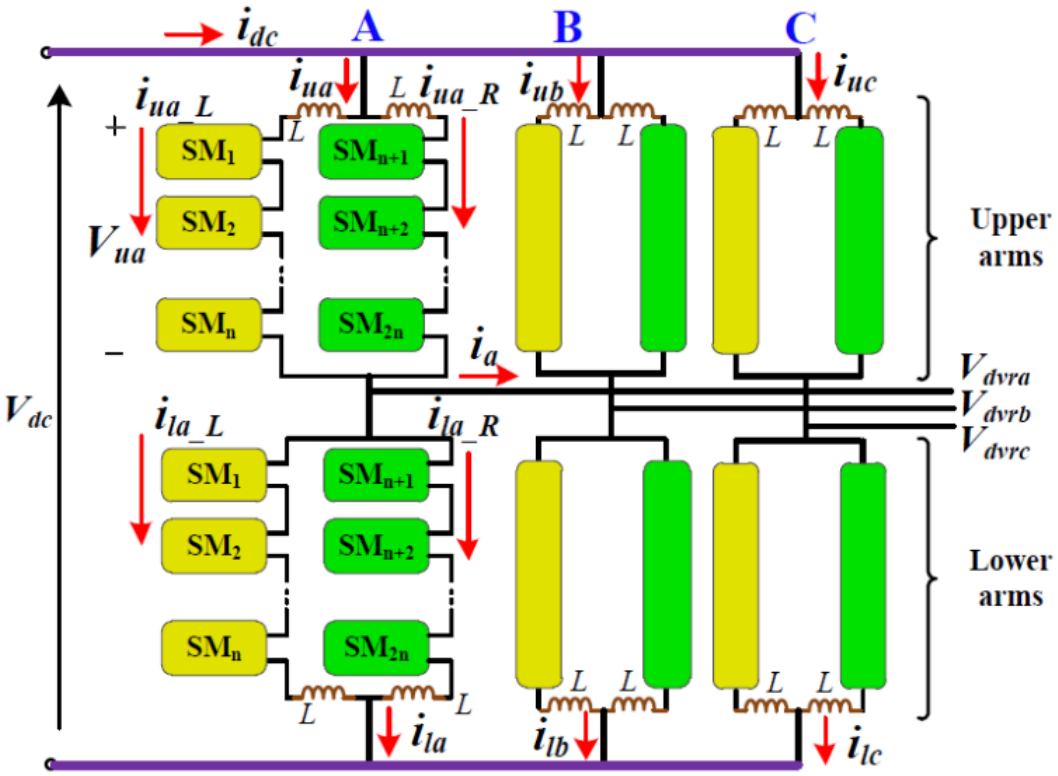


Figure 3.15: Parallel MMC (Lv et al., 2017)

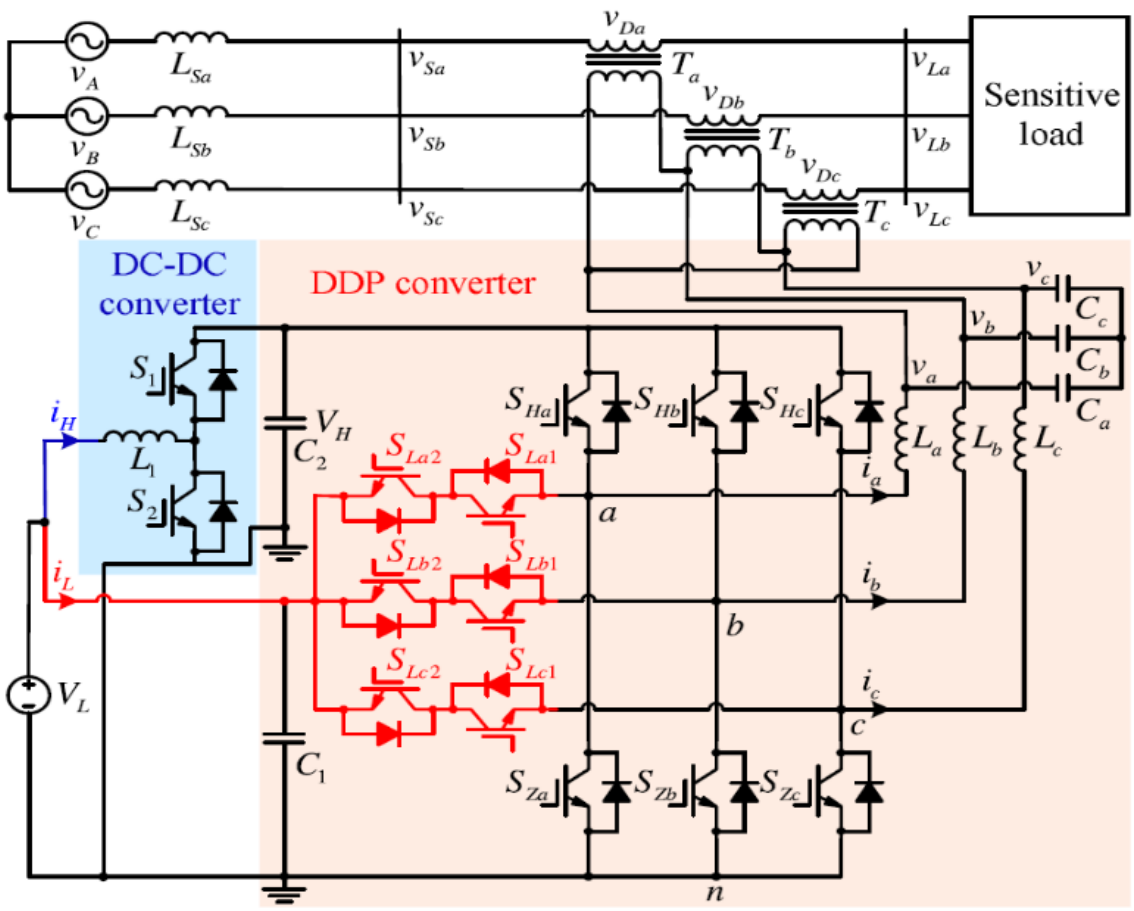


Figure 3.16: DVR topology based on DDP (Wang et al., 2019).

A single phase cascaded MLI topology derived from switching cell coupled with an inductor is applied in DVR structure (Kim et al., 2017). The presented converter is an ac-ac converter and has the ability to operate in open and closed circuits without destroying circuit components such as semiconductor switches. The presented ac-ac converter does not require a commutation circuit or a snubber circuit; hence the reliability of the DVR topology made of the composed ac-ac converter is safeguarded. Using cascaded structure can generate higher magnitudes of output voltages whiles limiting the ratings of the components. Cascaded topologies produce quality output waveforms. Filter size is minimized because of the use PS-PWM. Fig. 3.26 shows single-phase circuit of multilevel inverter applied in the DVR topology.

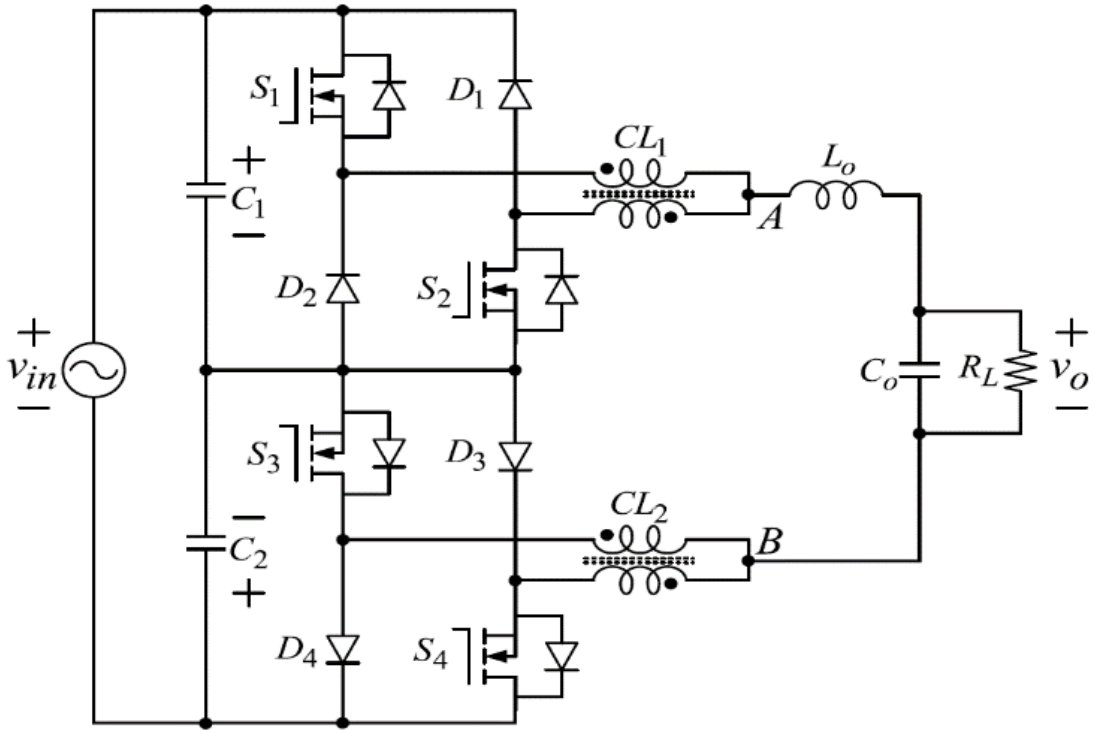


Figure 3.17: Phase one of switching cell MLI (Kim et al., 2017).

Two topologies of direct DVR structures are presented in (Babaei et al., 2010). These topologies of DVR do not require ESS therefore power for compensation is derived directly from the supply line. The absence of ESS means the DVR topology has the following characteristics; reduced size, minimum weight and reduced cost. The presented topologies have longer periods of voltage dip compensation capabilities. In the case of outage in a single-phase, presented topologies have the ability to compensate for outages. Unbalanced voltage dip/swell can be compensated by the presented topologies due to independence of each structure. The two designs are shown by Fig. 3.27a and Fig. 3.27b.

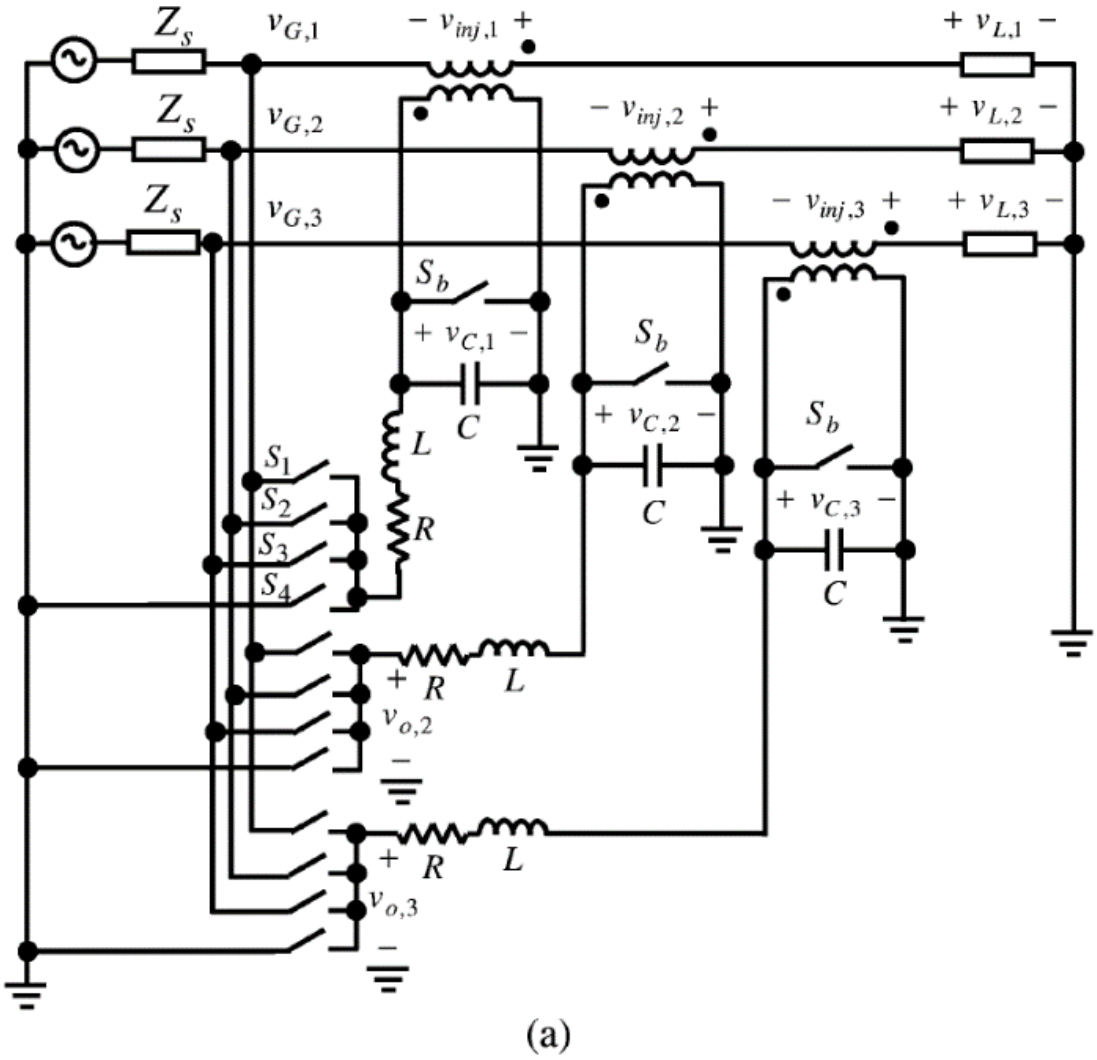


Figure 3.18: (a) First design of presented DVR (Babaei et al., 2010).

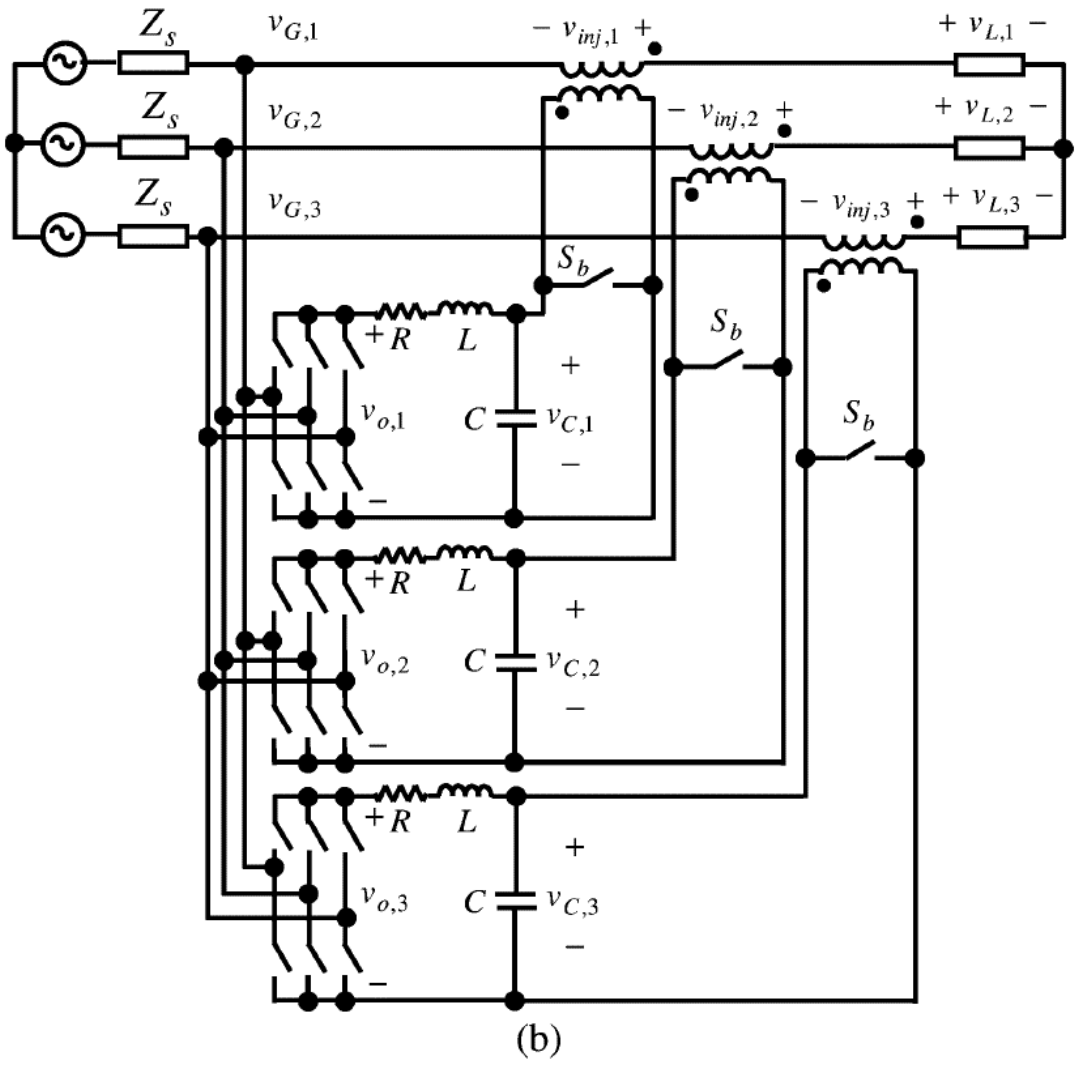


Figure 3.18: (b) Second design of presented DVR (Babaei et al., 2010).

A single phase direct power conversion DVR topology is presented in (Babaei and Kangarlu 2011). This presented DVR has less number of components in the converter structure and also does not require the use of ESS. The size, weight volume and cost of the presented structure are minimized due to the absence ESS. The compensation capabilities are heavily dependent on the turn's ratio of the injection transformer. Also the proposed topology is able to compensate voltage dip/swell, elimination or reduction of harmonics and flickers concurrently without the addition of any other component; a feature not common in the conventional DVR. The capability of increasing the number of phases for the presented converter is possible and compensate for

voltage under both unbalanced and balanced conditions. A fictitious DC source converter suitable for three-phase is presented as the converter component of DVR structure in (Babaei, and Kangarlu 2011). The use of the fictitious dc link eliminates the need for ESS, also the compensation power is derived directly from the grid. Fig. 3.28 shows the power circuit of the presented topology.

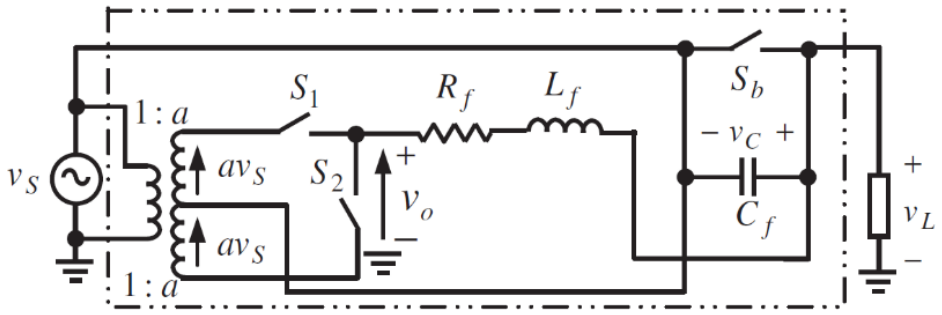


Figure 3.19: Single phase DVR (Babaei and Kangarlu 2011).

A three-phase ac-ac converter based DVR is presented in (Babaei and Farhadi-Kangarlu 2013). This topology inherits all the advantages of ac-ac based DVRs and it's also possible to compensate voltage dip for a phase by drawing power from the other two healthy phases. In the event of outage in one phase, the presented DVR topology is able to provide three-phase power to the sensitive until power is restored in the phase experiencing power outage. The presented topology is referred to as cross phase DVR. Fig. 3.29 shows the structure of the proposed DVR topology.

Simulation of selected multilevel inverter based dynamic voltage restorers are presented in this section. These topologies have been already published, simulative investigation will equip me with the requisite skills to effectively simulate our proposed DVR topology. Fig. 3.20 shows the simulation waveforms of voltage sag and voltage swell conditions for the presented topology in Fig. 3.19. This topology is an ac-ac converter therefore obtains the compensating voltage directly from the supply, bidirectional switches are used in this topology to provide to and fro current paths. As depicted in Fig. 3.20, waveforms have been provided for sag and swell, converter output voltage, DVR output and load voltage.

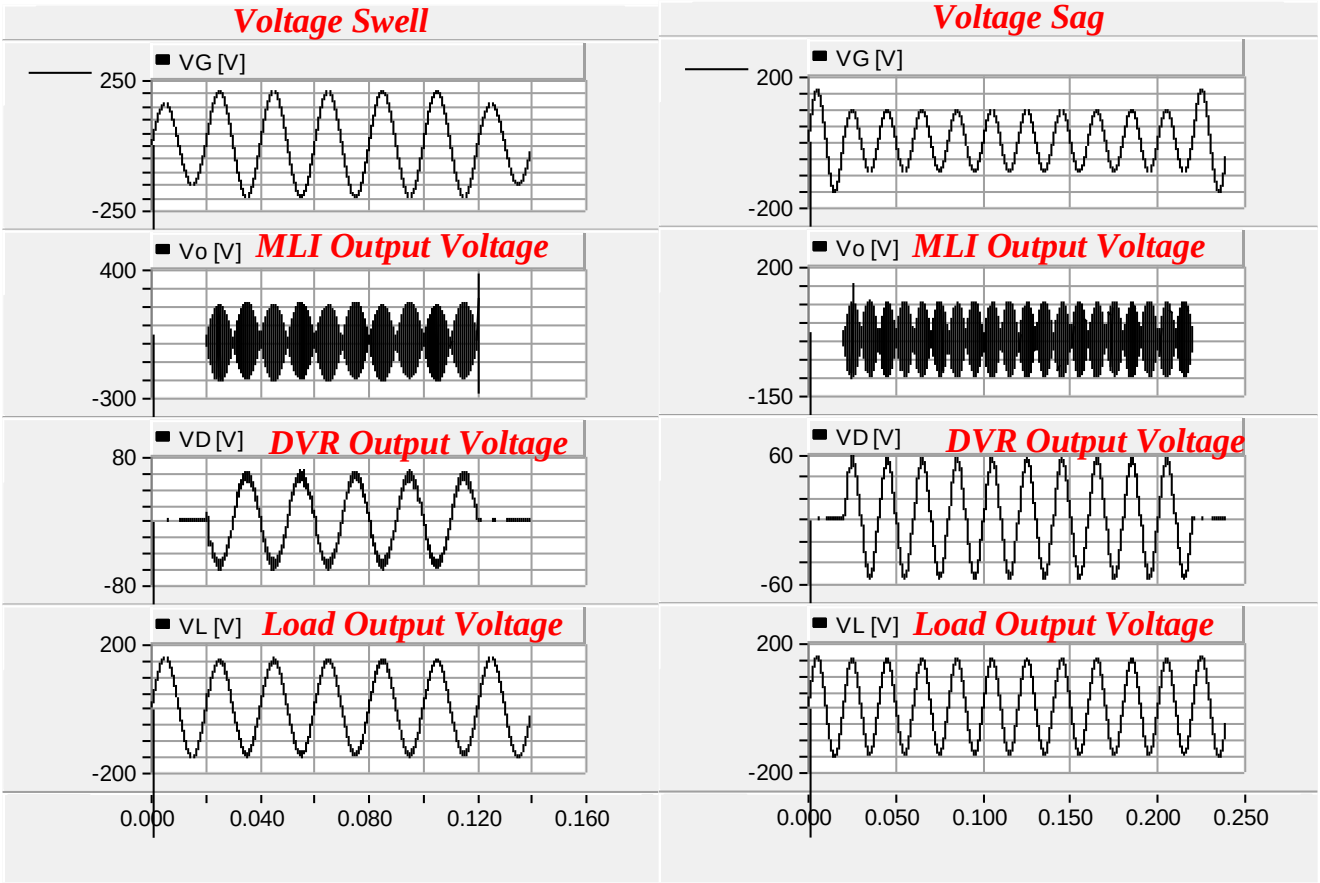


Figure 3.20: Single-phase ac-ac converter DVR waveform

Fig. 3.21 illustrates the DVR output waveforms of Fig. 2.18 using a three-phase ac-ac converter. As in the case of all ac-ac dynamic voltage restorers, the voltage used for compensation is derived from the supply line. The advantage of this technique is the elimination of double energy conversion which causes losses and reduced efficiency and also the need for dc sources and sometimes energy storage systems. The grid voltages of the three-phase lines are denoted by V_{G1}, V_{G2} and V_{G3}, the corresponding compensation voltage (injected voltage) are also denoted by $V_{inj,1}$, V_{inj2}, and V_{inj3} respectively. The load voltages V_{L1}, V_{L2} and V_{L3} after resolving the sag and swell conditions are shown exhibiting perfect sinusoidal waveform.

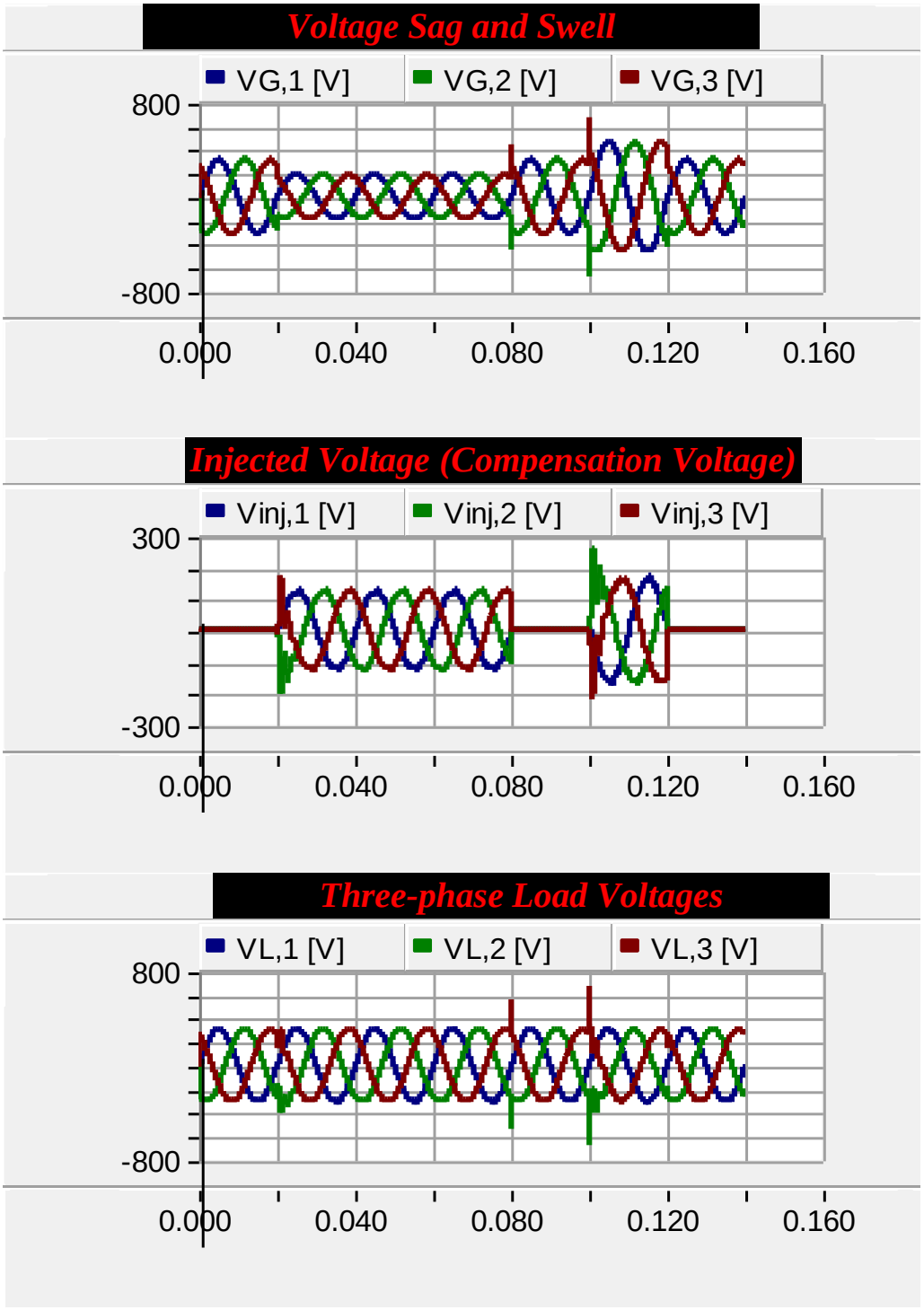


Figure 3.21: Single-phase ac-ac converter DVR waveform

3.8 Conclusion

DVR is a power electronic device which is suitable for resolving power quality disturbances produced by the supply side. The use power electronic based loads such as converters, computers etc. contributes to the generation of these supply side disturbances. It's very critical to mitigate these problems so as to protect loads of sensitive nature. The cost saving to both power producer and power consumer is or enormous magnitude when these disturbances are resolved. DVR topologies are broadly grouped into two main categories; topologies with ESS (ac/dc/ac) and topologies without ESS (ac-ac). Siting of the DVR is mostly on low to medium power systems and very close the load. DVR fault detection and compensation are the critical stages in the operation of the DVR; several control techniques have been presented for fault detection and also suitable control method is needed during compensation periods. MLI converters are mostly the suitable converter topology for generation of the desired compensation voltage or current; this can be attributed to its high power application with components of lower rating.

CHAPTER 4

PROPOSED THREE-PHASE MLI BASED DYNAMIC VOLTAGE RESTORER

4.1 Proposed Three-Phase MLI

The proposed improved H-bridge three-phase MLI is illustrated by Fig. 4.3. The proposed topology is a modified architecture of the presented topology in (Babaei et al., 2014). Two switches and one dc voltage source are added to the conventional H-bridge to obtain this topology. Fig. 4.1 shows the structure of the conventional single-phase inverter. One dc voltage source is added to the right-side of the H-bridge architecture and one switch is placed on the upper and lower section of the structure, this new structure, illustrated by Fig. 4.2 constitutes the fundamental architecture of the proposed three-phase MLI. A novel technique known as the "extension technique" is utilized to obtain the new three-phase MLI with reduced dc voltage source quantity. The dc voltage source count in the proposed topology is 4.

However, 6 dc voltage sources are required for the same three-phase MLI with independent single-phase units. 18 unidirectional power switches and 18 driver circuit are used in the proposed three-phase MLI, 6 switches, 6 driver circuit and 2 dc voltage sources are required for each phase. Individual phases are capable of generating 7-levels of load voltage. Two topologies of the proposed three-phase MLI are presented, Fig. 4.1a shows the proposed three-phase MLI with independent loads whiles Fig. 4.1b shows the proposed three-phase MLI with three single-phase transformers; this topology is suitable systems that require galvanic isolation such as DVR (dynamic voltage restorer). To the maximum number of output voltage levels that a multilevel inverter can generate, the general expression $\mathbf{2^s}$ is used. Where *s* represent the quantity of power switches used the proposed multilevel inverter. However, two important factors have to be considered, they are guidelines used in protecting the power switches and load, these factors are:

1. Avoid short-circuit of dc sources and power switches unless shoot-through conditions are required.
2. Avoiding open circuit of the load (with inductive element).

Considering the above factors, the proposed multilevel inverter is capable of generating maximum output voltage of 7-levels with 8 switching states, zero (0) output voltage can be generated with two different switching states.

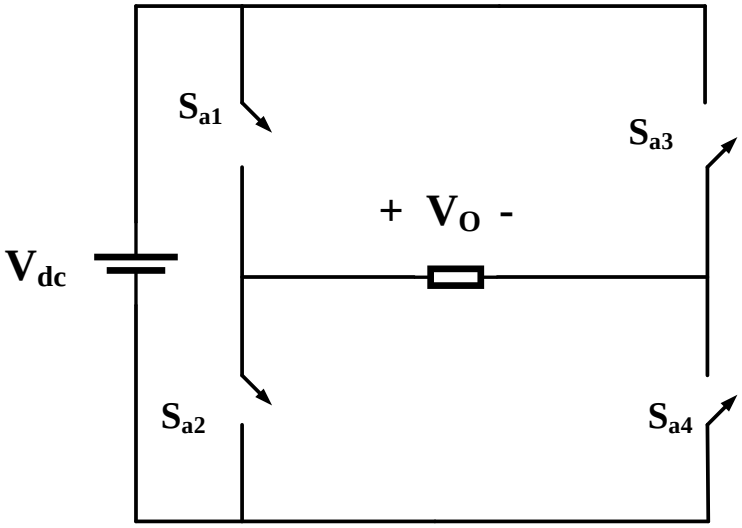


Figure 4.1: Conventional H-bridge MLI

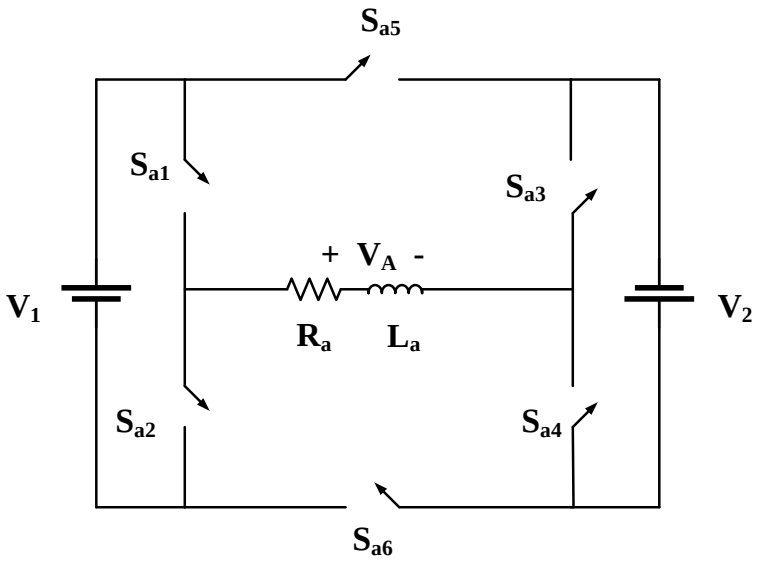
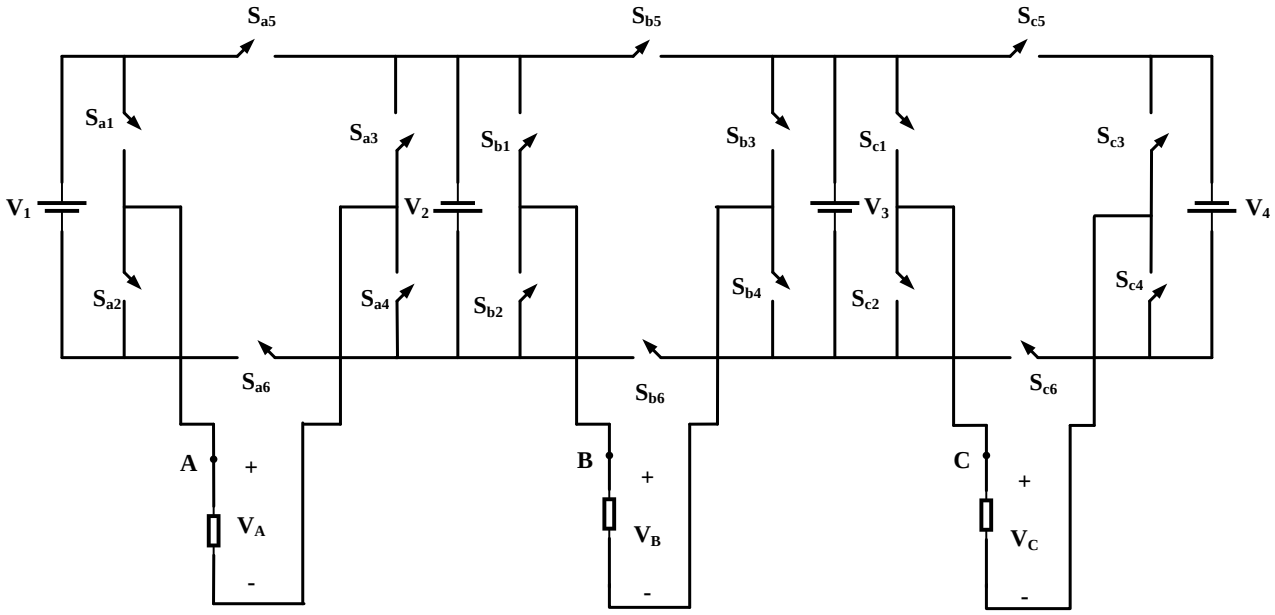
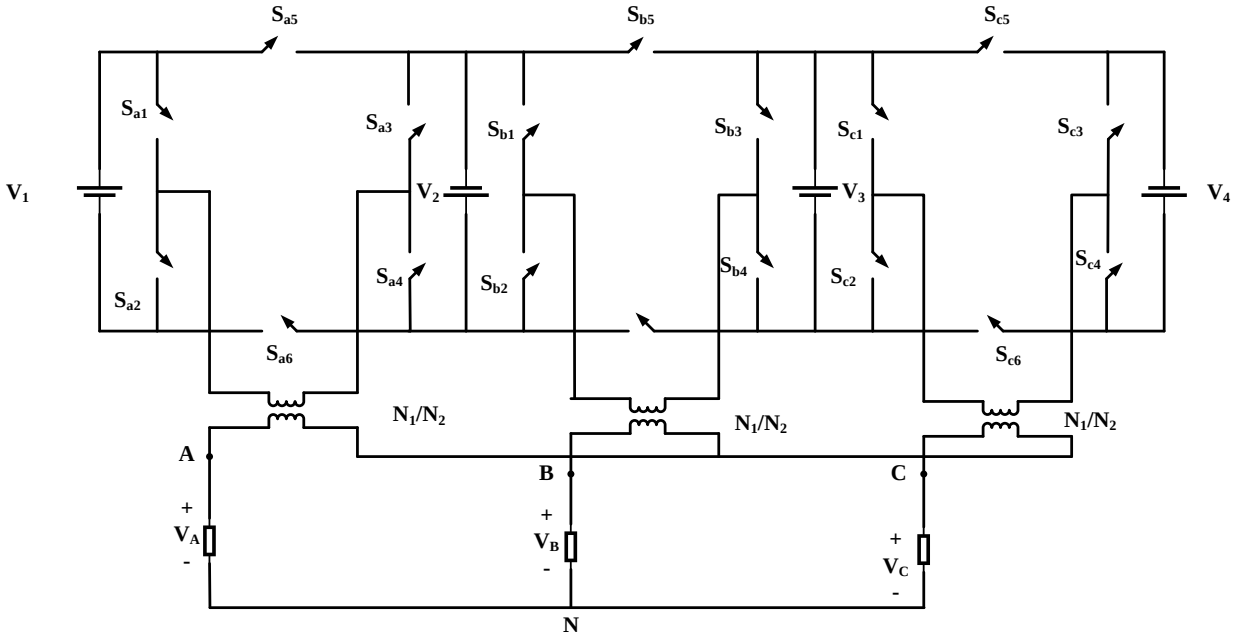


Figure 4.2: Single-phase structure of proposed MLI



(a)



(b)

Figure 4.3: Proposed three-phase multilevel inverter; (a) Three independent loads; (b) Three-phase load connected in Y configuration.

All switches in Phase A contain letter A in the subscript whiles Phases B and C have letters B and C in the subscript respectively. There are two dc voltage sources for each phase, the magnitude of these sources differ hence the proposed topology is an asymmetric inverter. This condition provides much higher stepped load voltage. If symmetric voltage source conditions are applied to the inverter, less stepped load voltage will be generated compared to the asymmetric condition i.e. only 5-levels of load voltage is generated. Similarly, it's important to connect the dc voltages for each phase in a series manner so as to generate high levels of load voltage. As illustrated in Fig. 4.3, the various phase load voltages of A, B and C are given by V_A, V_B and V_C respectively. Also the following represents the line-to-line voltages; V_{AB}, V_{BC} and V_{CA}. These features of Phase A are repeated in each phase i.e. there is symmetric features amongst individual phases of the inverter.

The dc voltage sources of the proposed three-phase MLI are related by the equation:

$$\begin{aligned} V_2 &= V_4 = V_{dc} \\ V_1 &= V_3 = 2V_{dc} \end{aligned} \tag{4.1}$$

The component count of the proposed topology is expressed by:

$$\begin{aligned} N_{switches} &= 18 \\ N_{Driver} &= 18 \\ N_{DC-Source} &= 4 \\ N_{Level} &= 7 \end{aligned} \tag{4.2}$$

Where $N_{switches}$, N_{Driver}, $N_{DC\text{-}Source}$ and N_L represents switch q, driver circuit count, dc source count and number of levels accordingly. The pole voltages at V_{AN}, V_{BN} and V_{CN} for Fig. 4b are determined below by the equations:

$$\begin{aligned} V_{AB} &= V_{AN} - V_{BN} \\ V_{BC} &= V_{BN} - V_{CN} \\ V_{CA} &= V_{CN} - V_{AN} \end{aligned} \tag{4.3}$$

Finally, it's evident from Fig. 4b that:

$$\begin{aligned} V_{AN} &= V_A \\ V_{BN} &= V_B \\ V_{CN} &= V_C \end{aligned} \tag{4.4}$$

The maximum phase output voltages and stepped voltages are given by:

$$V_A = V_B = V_C = \pm 3V_{dc} \ (0, \pm V_{dc}, \pm 2V_{dc}, \pm 3V_{dc}) \tag{4.5}$$

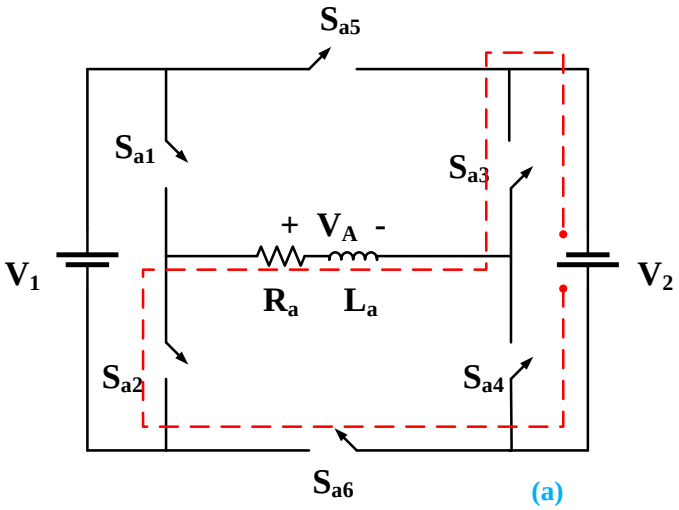
The maximum the line to line output voltages stepped voltages are given by:

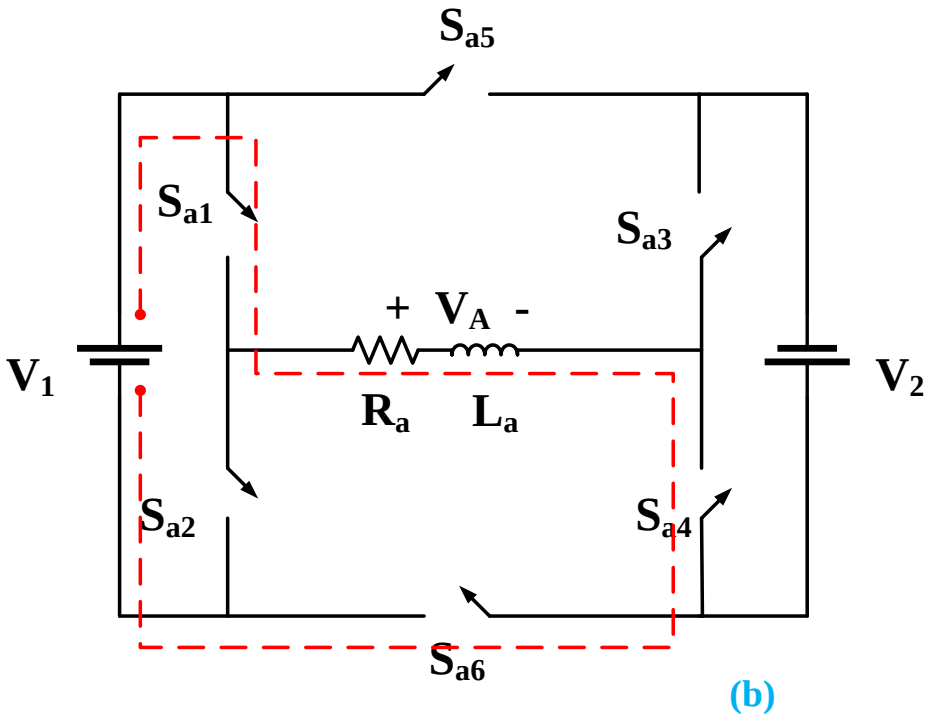
$$V_{AB} = V_{BC} = V_{CA} = 6V_{dc}(0, \pm V_{dc}, \pm 2V_{dc}, \pm 3V_{dc}, \pm 4_{dc}, \pm 5V_{dc}, \pm 6V_{dc}) \tag{4.6}$$

Table 4.1: Phase switching pattern

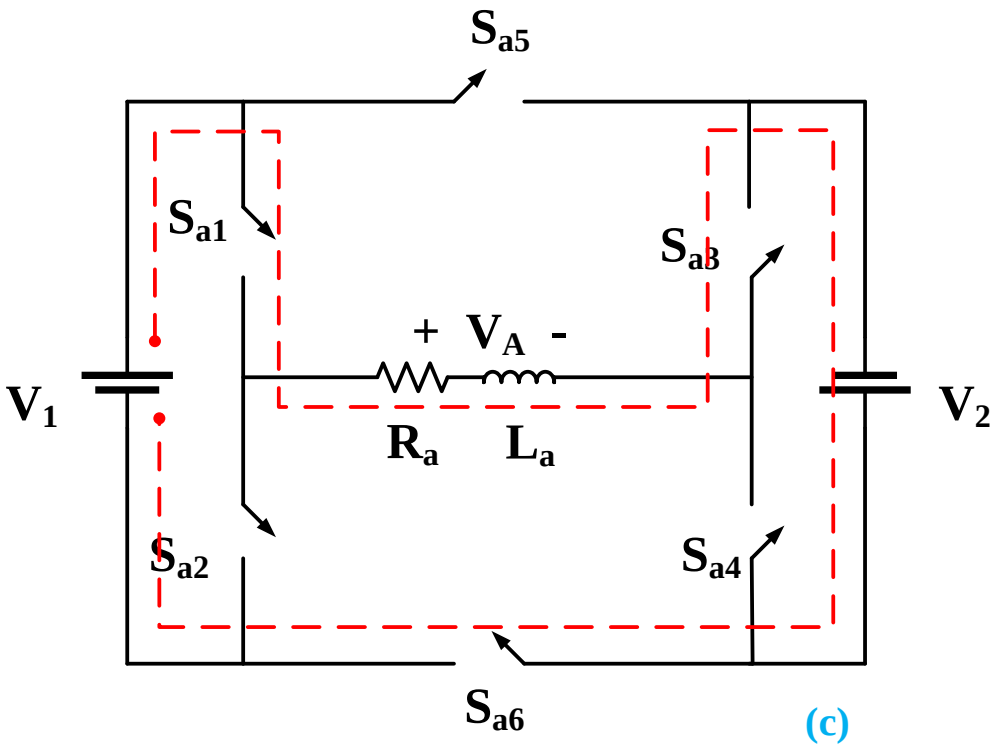
State	**Switches**	**V_A**	**Switches**	**V_B**	**Switches**	**V_C**
I	S_{a2}, S_{a3}, S_{a6}	V_{dc}	S_{b2}, S_{b3}, S_{a5}	V_{dc}	S_{c2}, S_{c3}, S_{c6}	V_{dc}
II	S_{a1}, S_{a4}, S_{a6}	$2V_{dc}$	S_{b1}, S_{b4}, S_{a5}	$2V_{dc}$	S_{c1}, S_{c4}, S_{c6}	$2V_{dc}$
III	S_{a1}, S_{a3}, S_{a6}	$3\ V_{dc}$	S_{b2}, S_{b4}, S_{a5}	$3\ V_{dc}$	S_{c1}, S_{c3}, S_{c6}	$3V_{dc}$
IV	S_{a1}, S_{a3}, S_{a5} S_{a2}, S_{a4}, S_{a6}	0	S_{b1}, S_{b3}, S_{a5} S_{b2}, S_{b4}, S_{a6}	0	S_{c1}, S_{c3}, S_{c5} S_{c2}, S_{c4}, S_{c6}	0
V	S_{a1}, S_{a4}, S_{a5}	$-V_{dc}$	S_{b1}, S_{b4}, S_{a6}	$-V_{dc}$	S_{c4}, S_{c1}, S_{c5}	$-\ V_{dc}$
VI	S_{a2}, S_{a3}, S_{a5}	$-2V_{dc}$	S_{b2}, S_{b3}, S_{a6}	$-2\ V_{dc}$	S_{c2}, S_{c3}, S_{c5}	$-2V_{dc}$
VII	S_{a2}, S_{a4}, S_{a5}	$-\ 3V_{dc}$	S_{b1}, S_{b3}, S_{a6}	$-\ 3\ V_{dc}$	S_{c2}, S_{c4}, S_{c5}	$-\ 3V_{dc}$

The working principle of the proposed three-phase MLI is equivalent to operations of an H-bridge inverter. When switches are gated ON diagonally in each phase, the generated output voltage is positive or negative value of each isolated dc source, to generate the sum of dc voltage source in each phase, different gating methodology is employed. Table 4.1 shows the switching pattern of Phase for the proposed three-phase MLI. Phase A is used to explain the mode of operation of the proposed inverter. To produce zero output voltage, two sets of switches are gated ON independently; Sa_1, Sa_3, Sa_5 or Sa_1, Sa_3, Sa_5. Positive V_{dc} is generated when Sa_2, Sa_3, Sa_6 are gated ON simultaneously, to generate Negative V_{dc}, concurrent conduction of Sa_1, Sa_4, Sa_5 is required. Positive $2V_{dc}$ is generated by concurrent gating ON Sa_1, Sa_4, Sa_6 switches, also negative $2V_{dc}$ is generated by gating ON Sa_2, Sa_3, Sa_5 switches concurrently. Positive $3V_{dc}$ is produced when Sa_1, Sa_3, Sa_6 switches conduct simultaneously whiles negative $3V_{dc}$ is produced when Sa_2, Sa_4, Sa_5 switches conducts simultaneously. During each conduction state of the inverter, the remaining switches are in voltage blocking mode. This conduction methodology is repeated for each phase to generate the same stepped load voltage. In other to differentiate switches of individual phases, subscript A, B and C are included in the numbering to indicate the phase each switch belongs. Fig. 4.4 shows the various conducting and non-conducting power switches during each switching state in phase A. In Fig. 4.4, positive V_2 is generated when switches S_{a2}, S_{a3} and S_{a6} conducts whiles the remaining switches maintain blocking mode. This switching mode is equivalent to the generation of V_{dc} during the first state shown in Table 4.1.

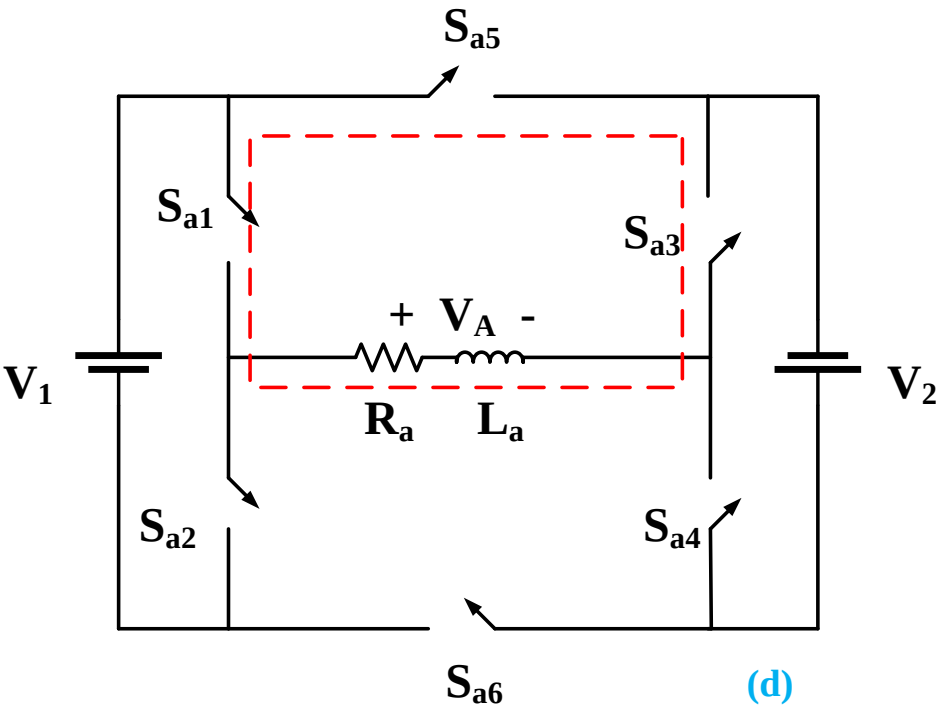



S_{a5}
S_{a1}
S_{a3}
+ V_A -
V_1
V_2
R_a
L_a
S_{a2}
S_{a4}
S_{a6}

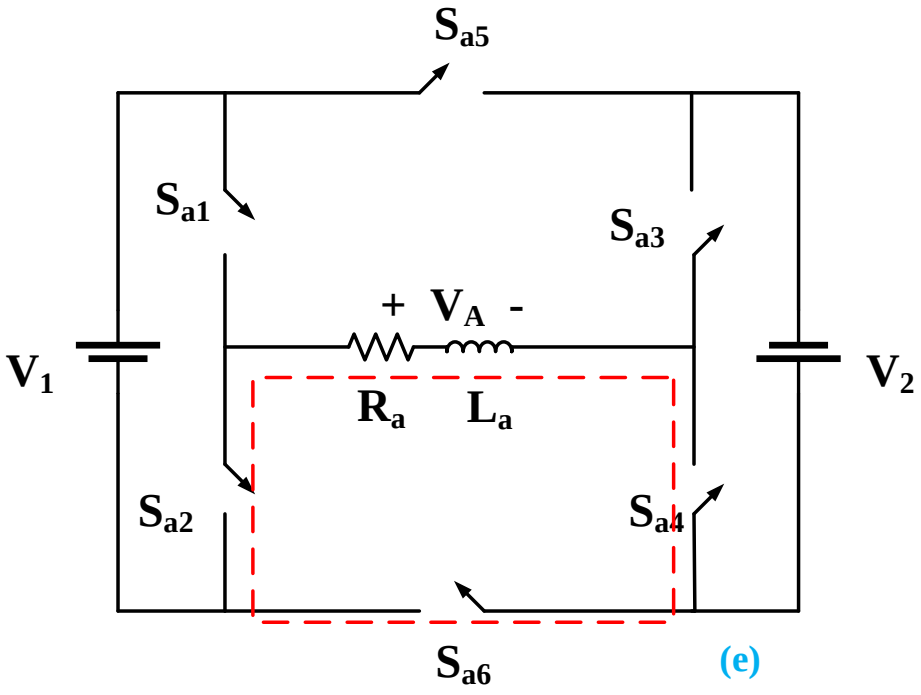
(b)


S_{a5}
S_{a1}
S_{a3}
+ V_A -
V_1
V_2
R_a
L_a
S_{a2}
S_{a4}
S_{a6}

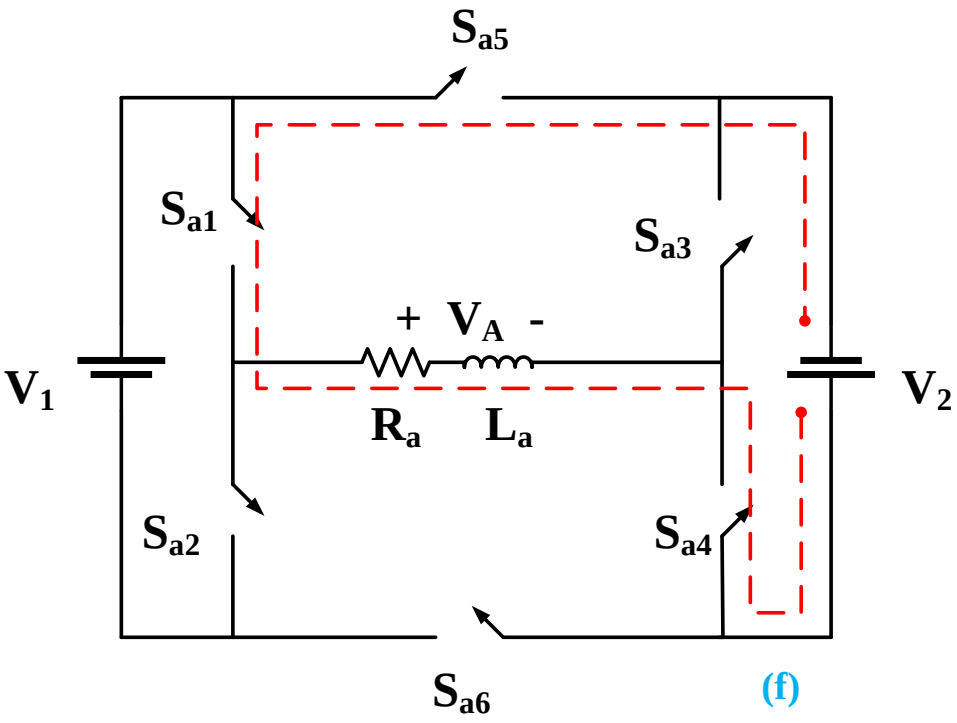
(c)


S_{a5}
S_{a1}
S_{a3}
+ V_A -
V_1
V_2
R_a
L_a
S_{a2}
S_{a4}
S_{a6}

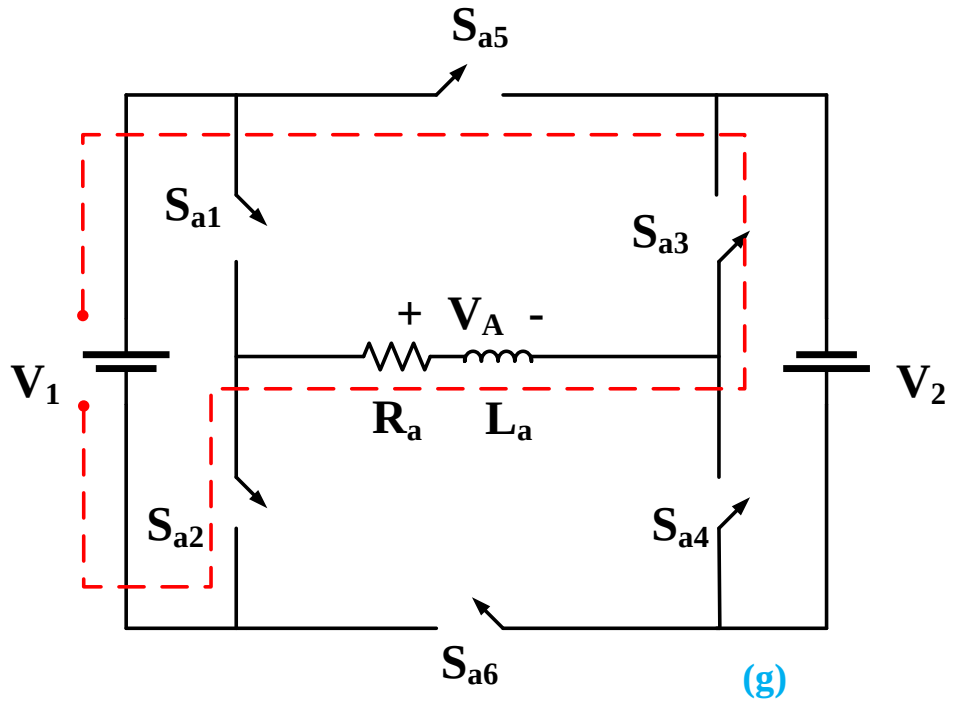
(d)


S_{a5}
S_{a1}
S_{a3}
+ V_A -
V_1
V_2
R_a
L_a
S_{a2}
S_{a4}
S_{a6}

(e)


Sa5
Sa1
Sa3
+ VA -
V1
V2
Ra
La
Sa2
Sa4
Sa6

(f)


Sa5
Sa1
Sa3
+ VA -
V1
V2
Ra
La
Sa2
Sa4
Sa6

(g)

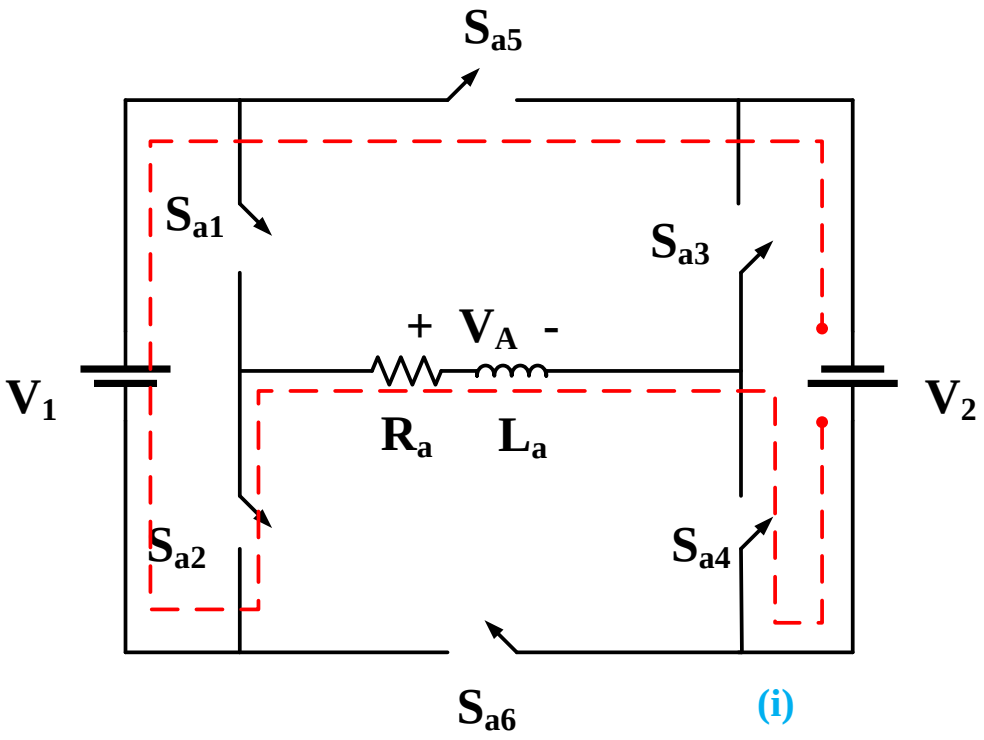


Figure 4. 4: Conducting switches in each switching state in phase A.

4.2 Proposed MLI Control

Fundamental frequency control method (FFCM) also known as NLC (nearest level control) technique is used in controlling proposed three-phase multilevel inverter. Fig. 4.5 illustrates the concept of FFCM technique in controlling multilevel inverters. The waveform (Fig. 4.5) shows stepped load voltage and reference voltage of single-phase structure of the proposed three-phase inverter. Comparing the reference voltage to the stepped voltage helps in selecting the closest (nearest) voltage level that should be produced by the MLI. With appropriate switching, the nearest stepped voltage is generated by the inverter. For the three-phase inverter, each phase is controlled independently with the usual phase difference of 120^0. FFCM technique is much simplified with respect to the algorithm when compared to NVC (nearest vector control) because selecting the closest value is simple.

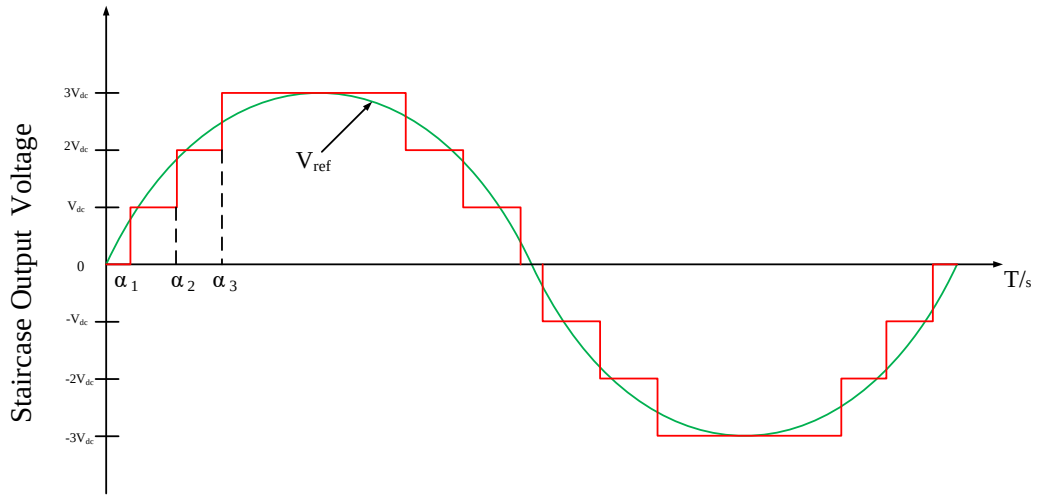


Figure 4. 5: Fundamental Frequency Control Method (FFCM)

The inverter output voltage level based on NLC technique is expressed below as:

$$V_{Closest} = V_{dc} f_{round} \quad (4.7)$$

Where:

V_{dc} is step voltage (incremental value)

f_{round} is the rounded closest integer.

Normalization of the reference voltage (V_{ref}) is achieved by the use of incremental stepped voltage Vdc. This normalize value is estimated to the nearest integer (f_{round}) which is multiplied by Vdc to determine the nearest voltage level with respect to the reference voltage (V_{ref}). The multilevel inverter produces this level of output voltage. FFCM technique is not a modulation technique because there no reference tracking by time average synthesis between two levels. FFCM method is not suitable for converters with minimum load voltage levels. The main advantages of FFCM are simple to implement, conceptuality and better efficiency. Step by step implementation of the proposed control technique for the three-phase MLI in PSCAD is given in appendix 1 of this thesis. Table 4.2 shows the gate signal switching derived after implementing the proposed three-phase MLI in PSCAD software. For example, to generate positive 3Vdc output voltage, switches S_{a1}, S_{a3} and S_{a6} are gated on whiles the remaining

switches are gated off. This procedure is carried out for other levels of output voltage using the appropriate switches.

Table 4.2. Gate signal switching states

Error	**Switching States**						**V_o**
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	V_A
MP3	1	0	1	0	0	1	$3V_{dc}$
MP2	1	0	0	1	0	1	$2V_{dc}$
MP1	0	1	1	0	0	1	V_{dc}
	1	0	1	0	1	0	
MP0	0	1	0	1	0	1	0
MN1	1	0	0	1	1	0	$-V_{dc}$
MN2	0	1	1	0	1	0	$-2V_{dc}$
MN3	0	1	0	1	1	0	$-3V_{dc}$

4.3 Blocking Voltage

When semiconductor power switches are not conducting i.e. in OFF-STATE, they are regarded to be in voltage blocking mode. The magnitude of voltage they block depends on source voltage magnitude which also determines the voltage ratings of the switch. It imperative to keep the voltage ratings of switch as low as possible because higher rated switches are much expensive therefore increases the cost of inverter and replacement cost, also higher voltage rated switches increase losses of the converter. Blocking voltage of power switches is the maximum voltage across the switch when it's not-conducting. Since there are two equal voltage sources for each phase, the blocking voltage will be determined for one phase and multiplied by three to determine the maximum blocking voltage of the proposed three-phase MLI.

The blocking voltage of switches S_{a1} and S_{a2} is computed by:

$$V_{S_{a1}} = V_{S_{a2}} = V_1 \tag{4.8}$$

The blocking voltage of switches S_{a3} and S_{a4} is computed by:

$$V_{S_{a3}} = V_{S_{a4}} = V_2 \tag{4.9}$$

The maximum blocking voltage for each phase is computed by:

$$V_{1\phi,Block} = 4(V_1 + V_2) \tag{4.10}$$

The maximum blocking voltage of the proposed three-phase MLI is computed by:

$$V_{3\phi,Block} = 3V_{1\phi,Block} = 12(V_1 + V_2) \tag{4.11}$$

4.4 Calculation of Inverter Losses

Power losses of an inverter are mainly associated with the semiconductor switches. Three types of power losses are produced by the semiconductor switches; these power losses are:

- Conduction power losses
- Switching power losses
- Blocking voltage power losses (this is however ignored because off-state currents of power switches are negligible)

4.4.1 Conduction Power Losses

Unidirectional switch made-up of one IGBT and one diode connected antiparallel together constitute the switch type in the proposed three-phase MLI. Therefore, the conduction losses of proposed topology are determined for individual power switches during the period of ON-state of those switches. Conduction power losses P_C is composed of IGBT power losses $P_{C,T}$ and the diode power losses $P_{C,D}$. The resistive component in the IGBT and diode are represented by R_T and R_D accordingly. The voltage component of IGBT and diode are given by V_T and V_D accordingly. The average conduction power losses are derived by integration of initial $P_{C,T}$ and $P_{C,D}$ equation for a cycle or a period. Considering the control mechanism and load characteristics will alter the conduction power losses equation.

$$P_{C,T}(t)=[V_T+R_T i(t)]i(t) \quad (4.12)$$

$$P_{C,D}(t)=[V_D+R_D i(t)]i(t) \quad (4.13)$$

$$P_{C,T}=\frac{1}{2\pi}\int_0^{2\pi} n_T(t)[V_T+R_T i(t))i(t)]d(\omega t) \quad (4.14)$$

$$P_{C,D}=\frac{1}{2\pi}\int_0^{2\pi} n_D(t)[(V_T+R_D i(t))i(t)]d(\omega t) \quad (4.15)$$

$$P_C=P_{C,T}+P_{C,D} \quad (4.16)$$

4.4.2 Switching Power Losses

Switching power losses of the proposed three-phase multilevel inverter occur during the period of *turn-on* and *turn-off*. These power losses are determined as energy power losses during the turn-on and turn-off of the power switches. The turn-on energy losses are represented by E_{on} and the turn-off energy losses are represented by E_{off}. The total switching energy losses is represented by P_{SW}. The voltage across the switch during the OFF period is represented by V_{SW}, the switch current during the turn-on period is I and the switch current during turn-off period is Ì. The turn-on and turn-off times are given by t_{on} and t_{off} accordingly.

$$E_{on,k}=\int_0^{t_{on}} v(t)i(t)dt=\int_0^{t_{on}}\left[\left(\frac{I'}{t_{on}}t\right)\left(-\frac{V_{sw,k}}{t_{on}}(t-t_{on})\right)\right]dt=\frac{1}{6}V_{sw,k}I't_{on} \quad (4.17)$$

$$E_{off,k}=\int_0^{t_{off}} v(t)i(t)dt=\int_0^{t_{off}}\left[\left(\frac{V_{sw,k}}{t_{off}}\right)\left(-\frac{I}{t_{off}}(t-t_{off})\right)\right]dt=\frac{1}{6}V_{sw,k}It_{off} \quad (4.18)$$

$$P_{SW} = f_s \sum_{k=1}^{N_{switch}} \left(\sum_{i-1}^{N_{on,k}} E_{on,k} + \sum_{i=1}^{N_{off,k}} E_{off,k} \right) \quad (4.19)$$

Power losses of the proposed inverter are computed below as:

$$P_{Loss} = P_{sw} + P_C \quad (4.20)$$

Efficiency (η) of the proposed inverter is determined by:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{Loss}}{P_{in}} \quad (4.21)$$

4.5 Comparative Investigation

Comparative analysis of the proposed three-phase multilevel inverter and other recently published topologies as well as conventional topologies of cascaded H-bridge (CHB), Flying capacitor (FC) and Diode-clamped (DC) MLI is presented in this section. This comprehensive comparison is carried out with respect to component quantities utilized i.e. dc voltage sources, IGBTs, driver circuits, transformers, capacitors and diodes. Only one of the selected topologies for comparison has 9-levels of load voltage, the remaining topologies generate 7-levels of load voltage. Detailed comparison is presented in Table 4.3 where it's evident that the proposed three-phase multilevel inverter utilizes the least component quantity (N_{TOTAL}). The presented topology in [17] can generate 7-levels for single phase inverter. Here, by using 14 switches, one DC voltage source and three capacitors, it is possible to supply a single phase load. To apply the presented topology in three-phase system, it will require 42 switches, 3 DC voltage sources, and 9 capacitors. However, the quantity of dc voltage sources in the proposed topology is higher than other topologies including the two conventional topologies. Table 4.3 illustrates the equations of comparison between the proposed three-phase MLI and other references. Equations are utilized in plotting the graphs of comparison shown by Fig. 4.6 to Fig. 4.9. From Table 4.4 three equations N_{IGBT}, N_{Driver}, N_{DC} and N_{TOTAL} are used individually against N_{LEVEL} to plot the graphs. all references and proposed topology generates 7-levels of load voltage.

Table 4.3: Comparative investigation of proposed topology and other presented topologies

Topology	N_{level}	N_{IGBT}	N_{DC}	N_{Driver}	N_{MD}	N_{CD}	N_{CF}	N_{C}	N_{T}	N_{Total}
Proposed	7	18	4	18	18	0	0	0	0	58
[11]	7	36	1	36	36	0	0	6	1	116
[12]	7	36	2	36	36	0	0	9	0	119
[13]	7	54	1	54	55	0	0	17	0	181
[14]	7	30	3	30	30	0	0	0	1	94
[15]	7	30	6	30	30	0	0	0	0	96
[16]	7	24	1	24	30	0	0	9	0	88
[17]	7	14	3	14	12	0	0	3	0	46
[18]	7	30	2	30	30	0	0	9	0	101
[19]	7	18	6	18	18	0	0	0	0	60
[20]	9	24	4	24	24	0	0	8	0	84
[21]	7	24	1	24	24	0	0	8	0	81
[22]	7	18	6	18	36	0	0	0	0	78
[23]	7	24	1	24	24	0	0	5	0	78
NPC	7	36	1	36	36	90	0	6	0	205
FC	7	36	1	36	36	0	45	6	0	160
CHB	7	36	9	36	36	0	0	0	0	117

Note: N_{level}: Number of levels, N_{IGBT}: Number of IGBT, N_{DC}: Number of dc sources, N_{driver}: Number of driver circuits, N_{MD}: Number of main diodes, N_{CD}: Number of clamping diodes, N_{CF}: Number of clamping capacitors, N_{C}: Number of capacitors, N_{T}: number of transformers, N_{TOTAL}: Total number of components.

Fig. 4.6 illustrates the variation graph of load voltage level count (N_{LEVEL}) vs IGBT quantity (N_{IGBT}) between selected references and proposed topology of Table 4.4. From the graph, the proposed topology (Y) as well two other topologies (Y8 and Y11) utilize the least quantity of IGBT in generating a load voltage of 7-levels. Proposed three-phase topology and the other reference topologies use unidirectional switches hence the IGBT and diode count are equal in individual topologies except for DC MLI topology where clamping diodes are required.

Table 4.4: Equations of comparison

Topology	N_{IGBT}	N_{Driver}	N_{MC}	N_{DC}	N_{Total}
Y [Proposed]	$2(n + 2)$	$2(n + 2)$	-	$n - 3$	$(8n + 3)$
Y1 [11]	$6(n - 1)$	$6(n - 1)$	$n - 7$	$n - 6$	$(16n + 6)$
Y2 [12]	$6(n - 1)$	$6(n - 1)$	$n + 3$	$n - 5$	$17n$
Y3 [13]	$(10n – 15) - 1$	$(10n – 15) - 1$	$2n + 3$	$n – 6$	$(27n – 8)$
Y4 [14]	$3(2n – 4)$	$3(2n – 4)$	-	$n – 4$	$(13n + 3)$
Y5 [15]	$3(2n – 4)$	$3(2n – 4)$	-	$n – 1$	$(13n + 5)$
Y6 [16]	$3n + 3$	$3n + 3$	$n + 3$	$n - 6$	$(12n + 4)$
Y7 [18]	$3(2n – 4)$	$3(2n – 4)$	$n + 3$	$n – 5$	$(14n + 3)$
Y8 [19]	$2(n + 2)$	$2(n + 2)$	-	$n – 3$	$3(2n + 4) + 6$
Y9 [20]	$3n + 3$	$3n + 3$	$n + 1$	$n – 3$	$12n$
Y10 [21]	$3n + 3$	$3n + 3$	$n + 1$	$n – 6$	$3(4n – 1)$
Y11 [22]	$2(n + 2)$	$2(n + 2)$	-	$n - 1$	$3(4n – 2)$
Y12 [23]	$3n + 3$	$3n + 3$	$n - 2$	$n – 5$	$3(4n -6)$
Y13 [NPC]	$6(n - 1)$	$6(n - 1)$	$n - 1$	$n – 5$	$6(5n + 1) - (n +4)$
Y14 [CHB]	$6(n - 1)$	$6(n - 1)$	$n - 1$	$n – 5$	$(22n + 6)$
Y15 [FC]	$6(n - 1)$	$6(n - 1)$	-	$n +3$	$3(6n - 2) - 3$

In Fig. 4.7, the graph represents the voltage level count (N_{LEVEL}) vs quantity of driver circuits (N_{Driver}). Since no bidirectional switches are utilized in proposed topology and reference topologies, the IGBT count is equivalent to the driver circuit count. That's is to say that each switch (whether unidirectional or bidirectional) will require individual driver circuits. Hence the diagram of N_{LEVEL} vs N_{Driver} is equivalent to the graph of N_{LEVL} vs N_{IGBT}. Therefore, the proposed topology (Y) and the reference topologies of (Y8 and Y11) utilizes the least driver circuit count. The driver circuit count in the cascaded H-bridge topology will be much higher

especially when high levels of load voltage are generated. The graph depicting variations with respect to (N_{LEVEL}) and dc voltage source quantity (N_{DC}) between the proposed topology and reference topologies is illustrated by Fig. 4.8. The proposed topology requires more dc voltage sources compared to other references, however, the dc voltage count in the cascaded H-bridge topology increases when the load voltage levels increases. Even though Diode clamped and Flying capacitor MLI requires one dc source each, the number of capacitors are high hence there's a trade-off between the dc voltage source quantity and the capacitor quantity. The proposed topology does not require capacitors therefore uses much simple control technique. The references used for comparison in Table 4.3 and Table 4.4 are used listed in appendix 3 of this thesis.

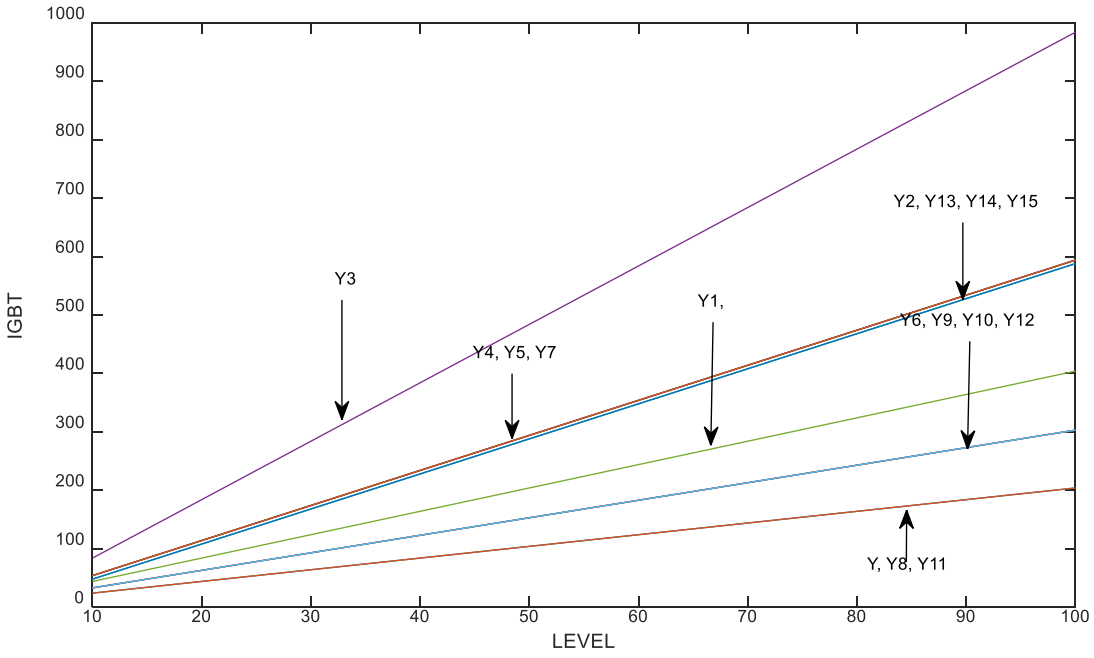


Figure 4.6: Graph of N_{IGBT} versus N_{LEVEL}.

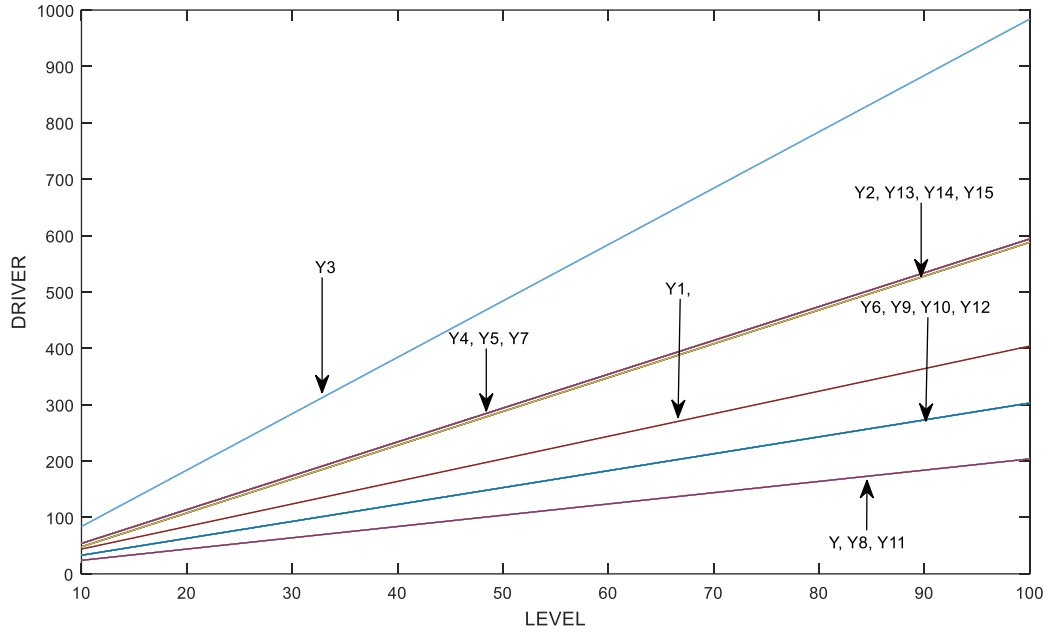


Figure 4.7: Graph of N_{DRIVER} versus N_{LEVEL}.

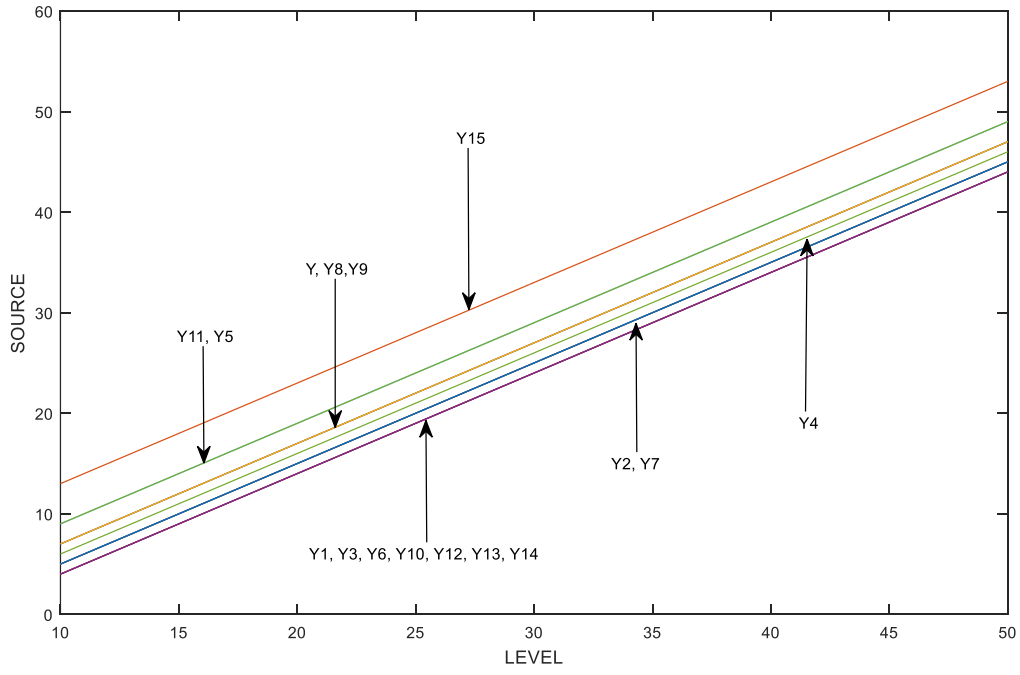


Figure 4.8: Graph of $N_{DC\text{-}SOURCE}$ versus N_{LEVEL}.

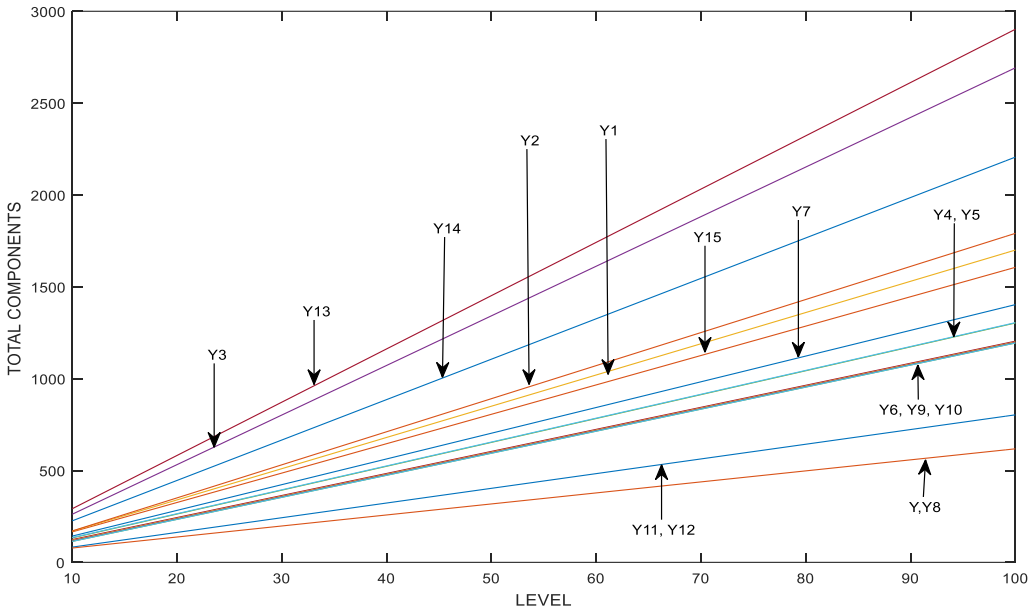


Figure 4.9: Graph of N_{TOTAL} versus N_{LEVEL}.

Finally, the graph depicting variations with respect to (N_{LEVEL}) and total component quantity (N_{TOTAL}) is illustrated by Fig. 4.9. From this diagram of comparison, the proposed three-phase inverter requires a total of 59 components whiles reference (Y8) requires a total of 60 components. The graph lines are same for both topologies because the negligible differences between the two topologies with respect to component quantity. The highest component count can be found in the three traditional MLI topologies. From the four graphs of comparison, the proposed three-phase MLI offers the best trade-off between the desired load voltage of 7-levels and investments compared to the other references.

4.6 Total Harmonic Distortion of Proposed MLI

Generally, total harmonic distortion (THD) is an estimation of the level of distortion or deviation of the voltage and current waveforms from sinusoidal waveforms. Nonlinear loads are the best culprits in causing pollution of power lines with high harmonics. Examples of nonlinear loads are computers, UPS, devices with rectifier circuits, telecommunication devices, battery charges. Low percentage THD levels are acceptable but very high levels causes problems such as equipment disturbances and heated power lines. THD levels differ from country to country,

IEEE 519 provides the acceptable levels in the USA. The general formula for calculating the THD of voltage is expressed below.

$$THD = \frac{\sqrt{(V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + \ldots V_n^{\,2}}}{V_1} \qquad (4.22)$$

V_1, V_2, V_3 and V_4 are the voltage magnitude of the first, second, third and fourth harmonics. V_n is the voltage magnitude of the nth harmonic. In general, multilevel inverters produce voltage with reduced the total harmonic distortion content. The generated frequency spectrum of Fig. 4.10 shows elimination of the even harmonics and minimum levels of odd harmonics such as 5^{th}, 7^{th} and 9^{th} harmonics in comparison to the 1^{st} harmonic. THD of the output voltage is 12% as shown by Fig. 4.11. To eliminate selected harmonics, several methods such as the use of filters or appropriate control techniques such SHE (selective harmonic elimination) can be applied.

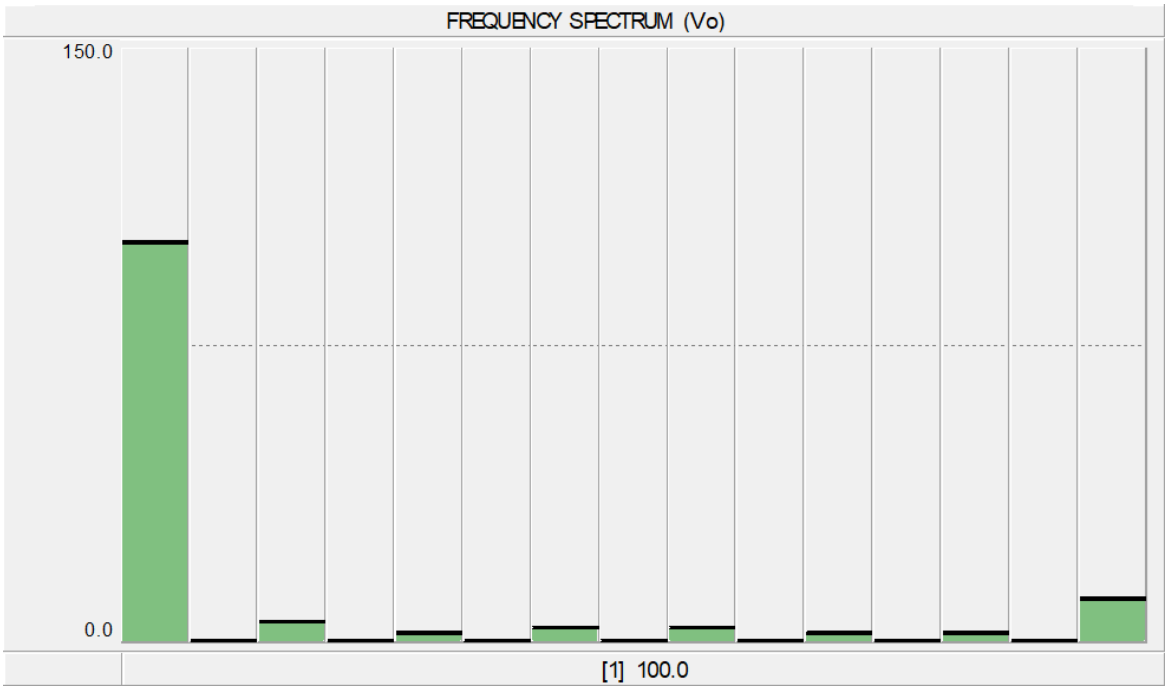


Figure 4.10: Frequency spectrum

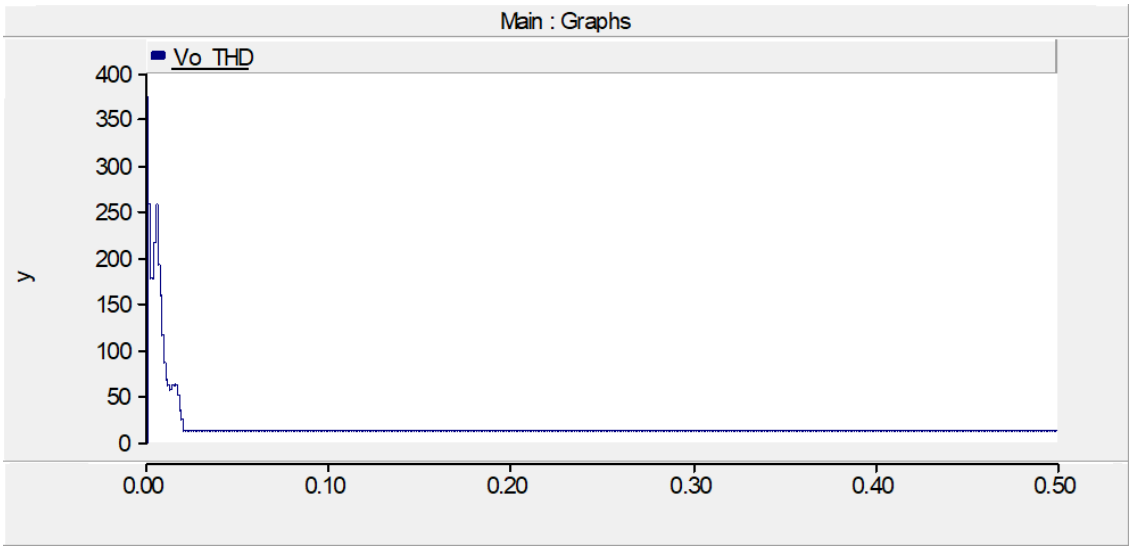


Figure 4.11: THD waveform of output voltage

4.7 Proposed Three-phase MLI based DVR

Under grid disturbances, the quality of voltage deteriorates thereby causing destruction of sensitive loads mostly located in hospitals, factories etc. Voltage sag and swell are some of the negative effects due to these disturbances. The proposed three-phase MLI based DVR is a suitable topology to resolve these disturbances via voltage compensations. Fig. 4.12 shows architecture of the proposed DVR. The proposed three-phase MLI based DVR is composed three main parts namely the supply, main DVR topology and loads (sensitive). The proposed DVR uses external energy source (from the inverter dc source voltage) to compensate voltage sag or swell conditions. As shown by Fig. 4.12, proposed three-phase multilevel is imbedded into the generalized structure of three-phase DVR constituting proposed topology. Pictorial evidence of implemented proposed three-phase multilevel inverter based DVR in PSCAD software is illustrated in appendix 2 of this thesis.

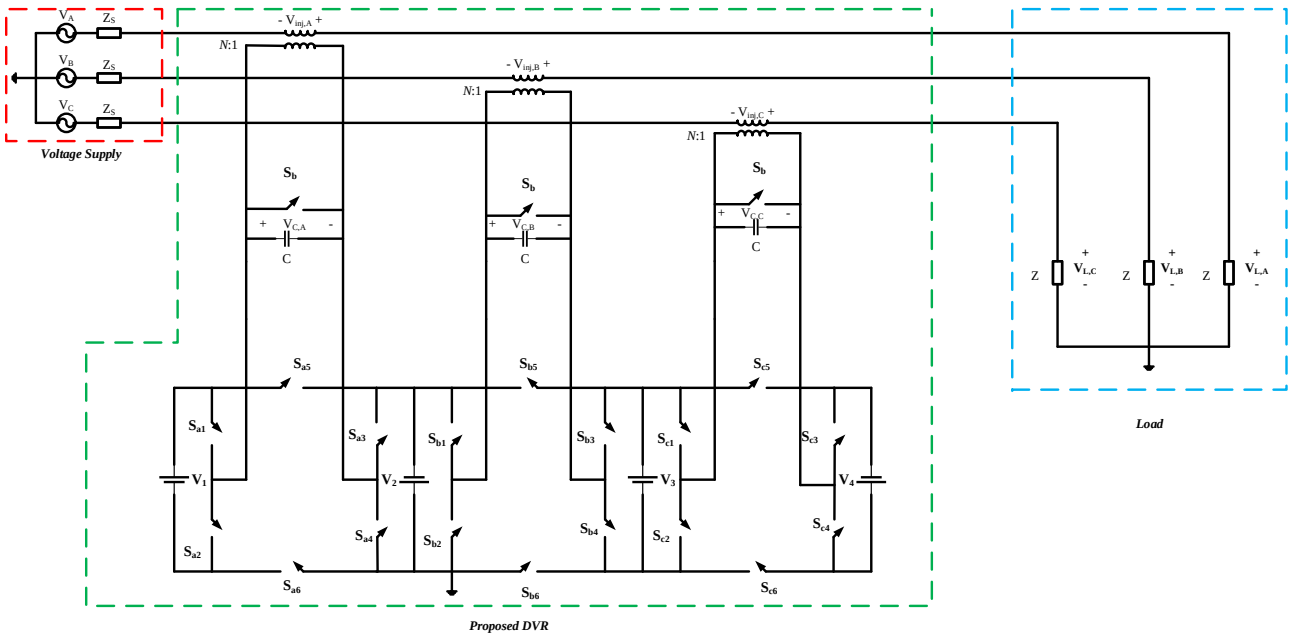


Figure 4.12: Proposed MLI based DVR

4.8 Limitation of Proposed MLI Based DVR

The proposed multilevel inverter based DVR has a few drawbacks with respect to the magnitude of compensating voltage and the stepped injecting voltage from the multilevel inverter. The duration of compensations is not a major issue because several dc sources such as photovoltaic systems can be used in compensating voltage sag and swell conditions. The voltage values for the proposed multilevel inverter DVR topology are V_{dc} and $2V_{dc}$ for each phase of the MLI, this corresponds to 10V and 20V respectively. With these voltage magnitudes, the proposed DVR is able to inject a maximum compensating voltage of 30V into the lines for each phase and 50V for line-to-line voltages. The three-phase load voltage rating of the line is 310V, therefore the proposed DVR will be able to compensate 9.68% of the load voltage using input voltages of 10V and 20V.

Table 4.5: Limitation analysis of the proposed three-phase MLI based DVR

CASE	MLI Input Voltage	Maximum DVR Output Voltage	Incremental Voltage Levels	Load Voltage	Compensating Percentage (%)
I	V_1 = 10V, V_2 = 20V	30V	10V	310V	9.68%
II	V_1 = 15V, V_2 = 30V	45V	15V	310V	14.52%
III	V1 = 30V, V2 = 30V	60V	30V	310V	19.36%
IV	V_1 = 25V, V_2 = 50V	75V	25V	310V	24.19%
V	V_1 = 50V, V_2 = 100V	150V	20V	310V	48.39%
VI	V_1 = 25V, V_2 = 75V	75V	25V	400V	18.75%

Also the incremental voltage levels for compensations are 10V, 20V and 30V. This is to say that, voltage sag or swell conditions without these incremental values will not be compensated for appropriately. However, the input voltage of the proposed MLI can be varied to provide the required compensating voltage. Table 4.5 shows analysis of the proposed MLI DVR with varying input voltages. As indicated in the table, minimum input voltage magnitudes are capable of compensating less percentage of voltage sand swell condition conditions. In case I, the maximum phase out voltage is 30V whiles the load voltage is 310V, therefore the maximum compensating percentage is 9.05%, in case II, the maximum phase out voltage is 45V whiles the load voltage is 310V, therefore the maximum compensating percentage is 14.52% and in

case V, the maximum phase out voltage is 150V whiles the load voltage is maintained at 310V, therefore the maximum compensating percentage is 48.39%.

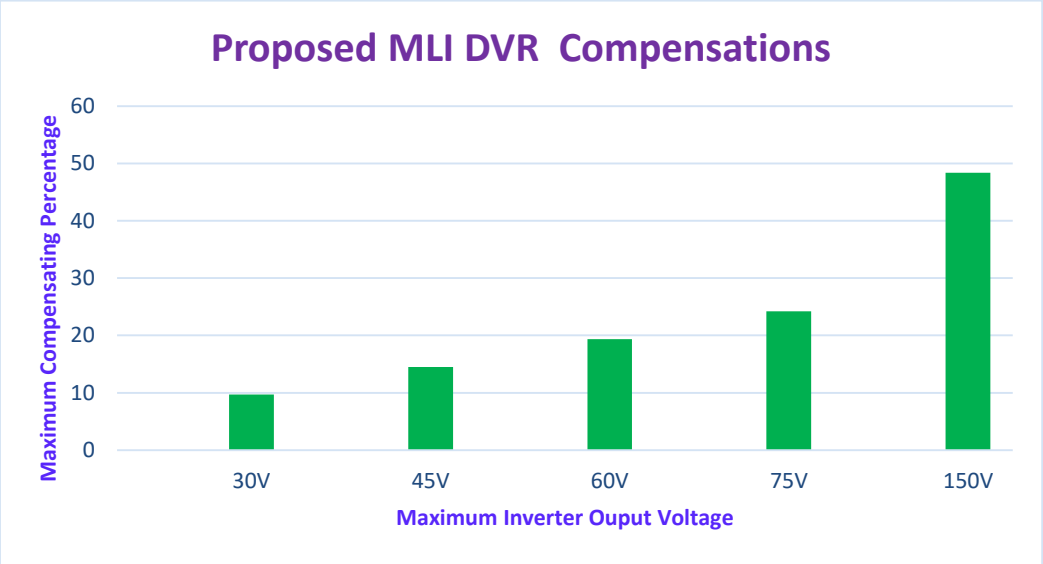


Figure 4.13: Compensation percentage of proposed DVR

Fig. 4.13 shows a graph of the maximum DVR output voltage and the maximum compensating percentage. If the load varies whiles the DVR output voltages are maintained, the compensating percentage will vary. The compensating percentage will increase if the load voltage is reduced from its current value of 310V, however, the compensating percentage will reduce if the load voltage is increased. These analyses are only valid if the input voltages are maintained as shown in Table 4.5. Simulation results for some selected maximum inverter output voltages of Table 4.5 are illustrated by Fig. 5.20 to Fig. 5.22 using 150V, 75V and 30V inverter output voltages for each case respectively.

4.9 Conclusion

In this section, the proposed three-phase multilevel inverter is presented and analyzed. Two power circuits of the proposed topology are presented; the first topology has three independent loads whiles the second topology utilizes three single-phase transformers to provide galvanic isolation. The modes of operation and inverter power losses calculations are comprehensively

presented, conduction and switching losses constitute the power losses of the inverter. Finally, comprehensive investigation of the proposed topology and selected references are presented using four graphs where it's clear the proposed topology requires less components to generate same levels of load voltage. This means the proposed inverter cost is reduced, the volume and size are also reduced and also simple control technique is used because no capacitors are used in the proposed topology.

CHAPTER 5
SIMULATION AND EXPERIMENTAL RESULTS

5.1 Introduction

In this section, the results of simulations and experiments are provided to show the workings or practicability of the proposed three-phase multilevel inverter. Firstly, simulation results of the proposed three-phase are provided, subsequently the experimental results are provided then finally simulation results of proposed MLI based DVR is provided.

5.2 Simulation Results

In other to provide the simulation results, the proposed topology is developed in PSCAD/EMTDC software by building its power circuit as illustrated by Fig. 5.1. The proposed three-phase is connected to a three-phase *RL* (resistance-inductance) Y configured load. Three single-phase transformer are used to provide galvanic isolation. The turns ratio of the transformers are $\frac{N_1}{N_2} = 1$. To fully execute the switching pattern of Table 4.1, an appropriate control technique is required. The basic function of switching methods is to reduce the harmonic content, minimize the switching losses and generate high quality load waveforms (Pan et al., 2005). Switching losses of fundamental frequency modulation is less when compared to PWM control techniques such as sinusoidal PWM hence its selected to control the switching states of Table 4.1. Simulation and experimental parameters are indicated by Table 5.1.

Table 5.1: Simulation and Implementation Parameters

Parameters	Value
Input voltage V_{dc}	$V_1 = V_3 = 20V$, $V_2 = V_4 = 10V$
Output Resistance *R*	100Ω
Output Inductance *L*	55mH
Switching Frequency f_s	4kHz
Output Frequency f_o	50Hz
Modulation Index	1

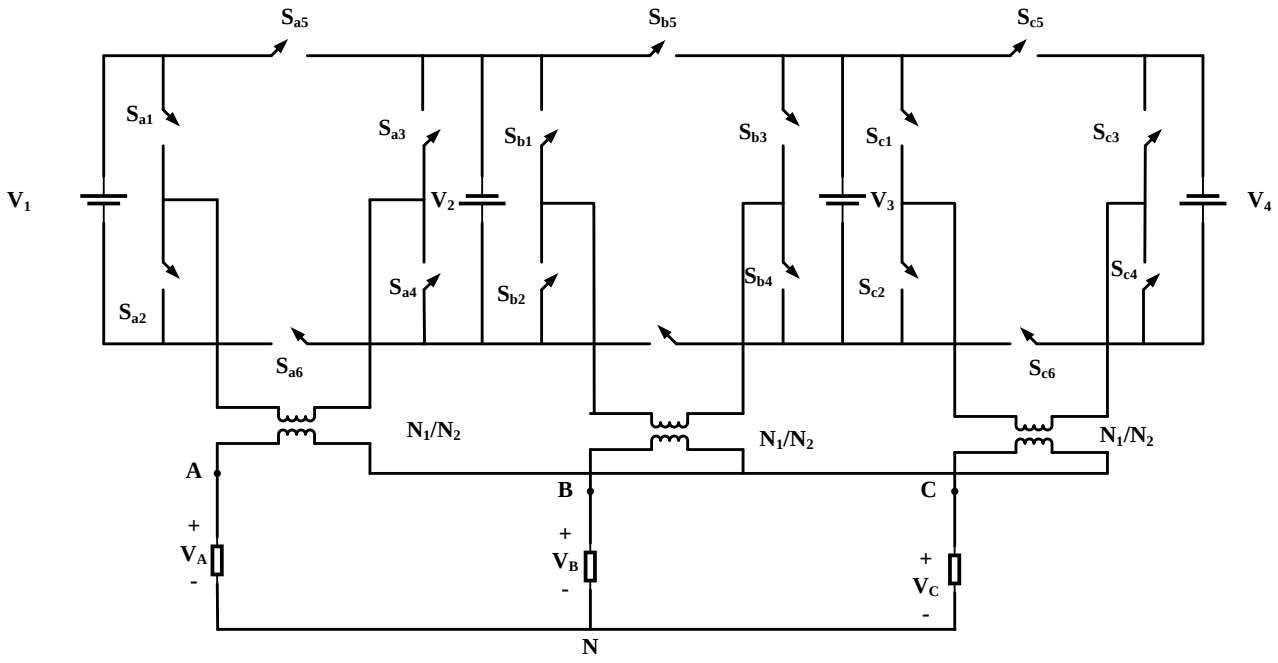


Figure 5.1: Proposed three-phase MLI load connected in Y configuration.

Three categories of load waveforms are generated from simulation, these waveforms are individual phase voltage waveforms, phase current waveforms and line-to-line voltage waveforms. Phase voltage, phase current and line-to-line current waveforms are illustrated by Fig. 5.2 to Fig. 5.11, Fig. 5.55 to Fig. 5.5 and Fig. 5.7 to Fig. 5.9 respectively. Each phase load voltage is generated against the reference sine waveform (va/Refa, vb/Refb and vc/Refc).

The perfect superimposition of the two waveforms clearly indicates better quality load waveforms which attest to the practicability of the proposed topology and the applied modulation technique. The maximum load voltage for each phase is $\pm 30V$ with incremental voltage levels (steps) of $\pm 10V$.

The load current waveform of Fig. 5.5 to Fig. 5.6 are the phase currents for phases A, B and C accordingly. The peak to peak current magnitude for each phase is 300mA. Fig. 5.3 to Fig. 55 shows the line-to-line voltages. The incremental levels in the line-to-line load voltage is also $\pm 10V$ with peak to peak voltage of $\pm 50V$. this means 13-levels of load voltage are generated for the line-to-line system. Line voltages vab, vbc and vca are generated against the reference

signals of Refab, Refbc and Refca accordingly. Fig. 5.11 shows the blocking voltage of the various switches in phase. Theoretical and simulation analysis of the blocking voltage of the power switches yield the same results, equations 4.7 and 4.8 and Fig. 5.11 produce the same magnitudes of Blocking voltage. The blocking voltage of the lower and upper switches of Phase A is 30V, the right and left side switches blocks 20V and 10V accordingly. The total blocking voltage for each phase is 120V whiles the total blocking voltage for the proposed three-phase topology is 360V.

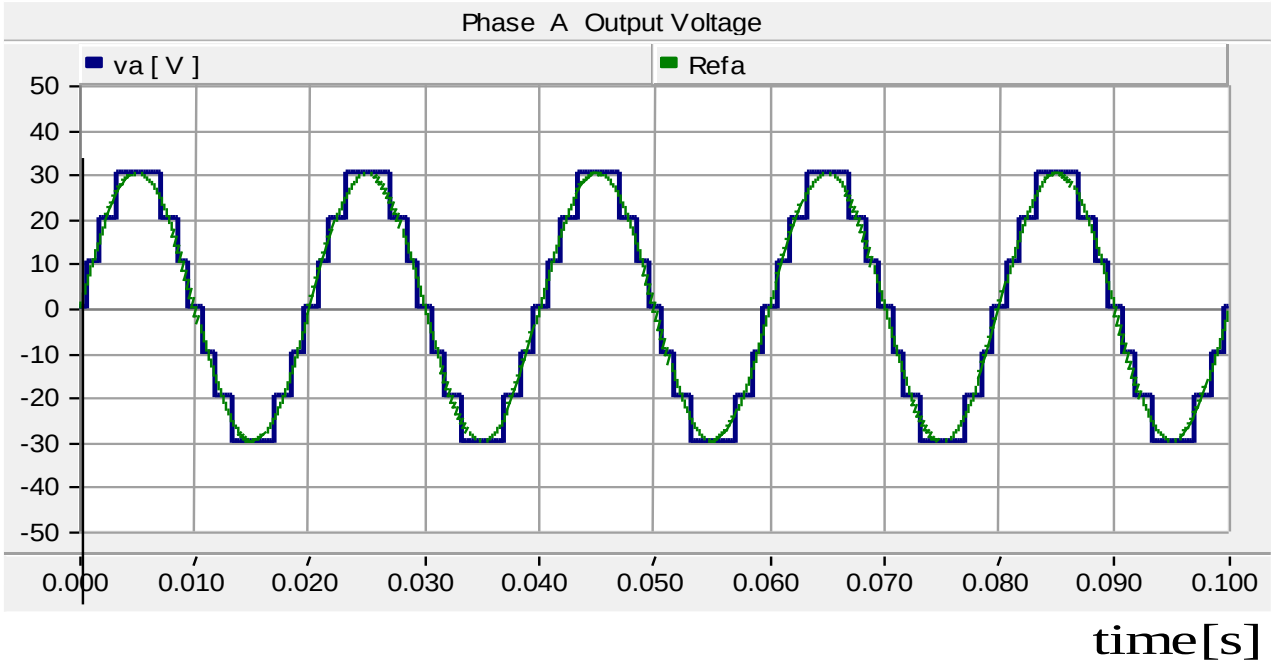


Figure 5.2: Phase A load voltage and reference signal

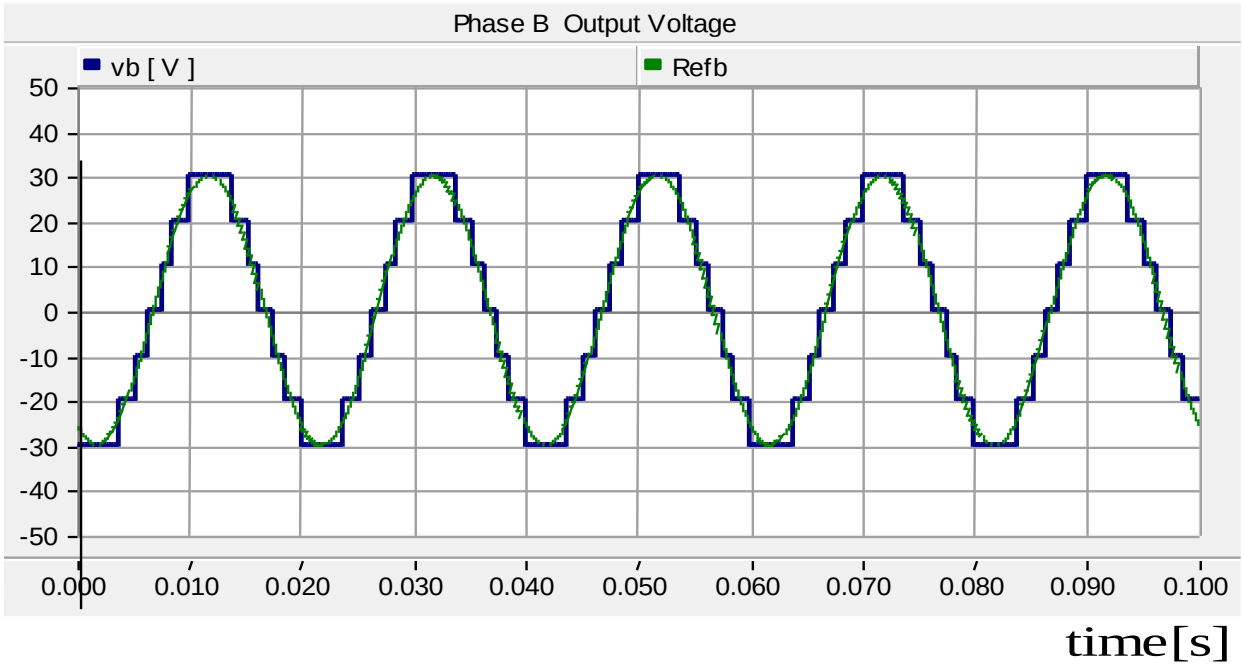


Figure 5.3: Phase B load voltage and reference signal

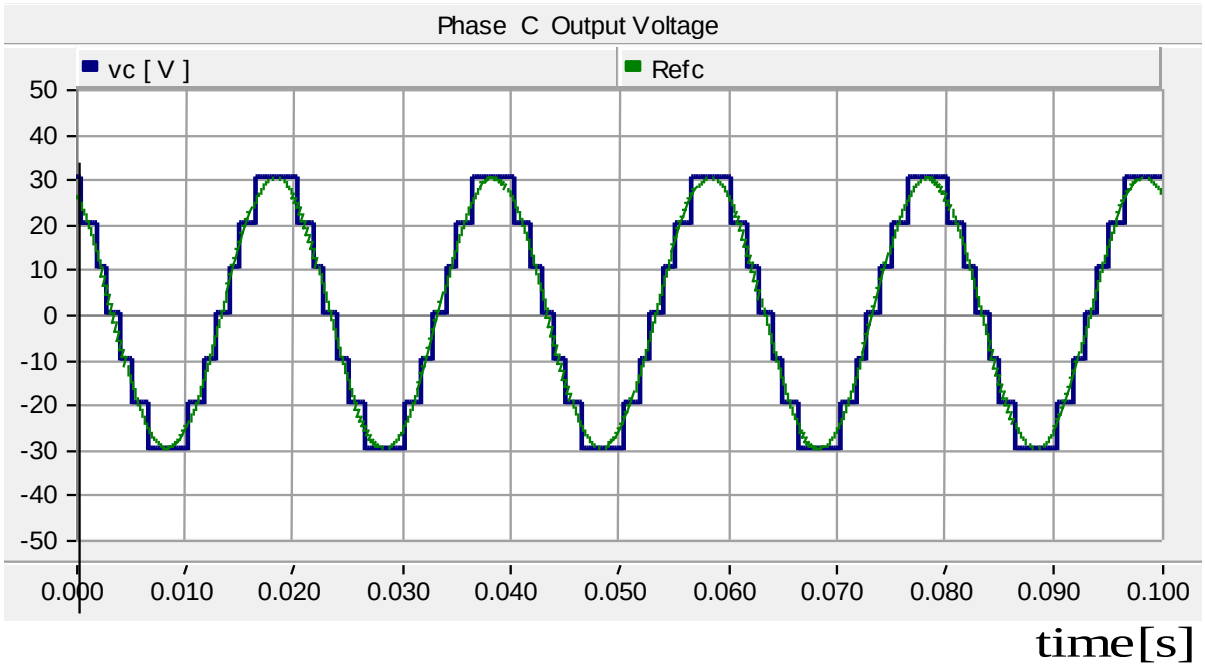


Figure 5.4: Phase C load voltage and reference signal

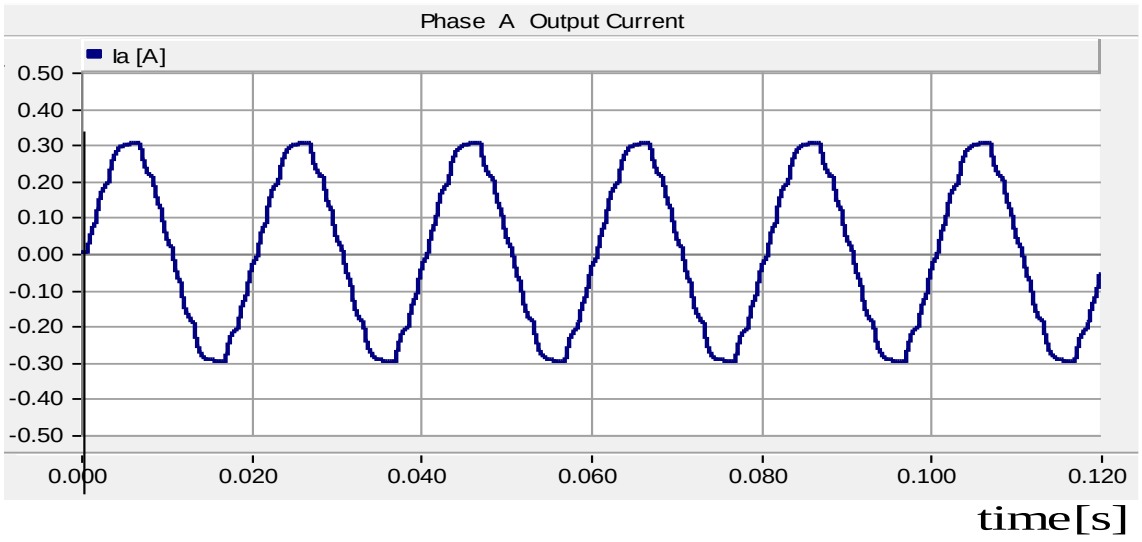


Figure 5.5: Phase A load current waveform

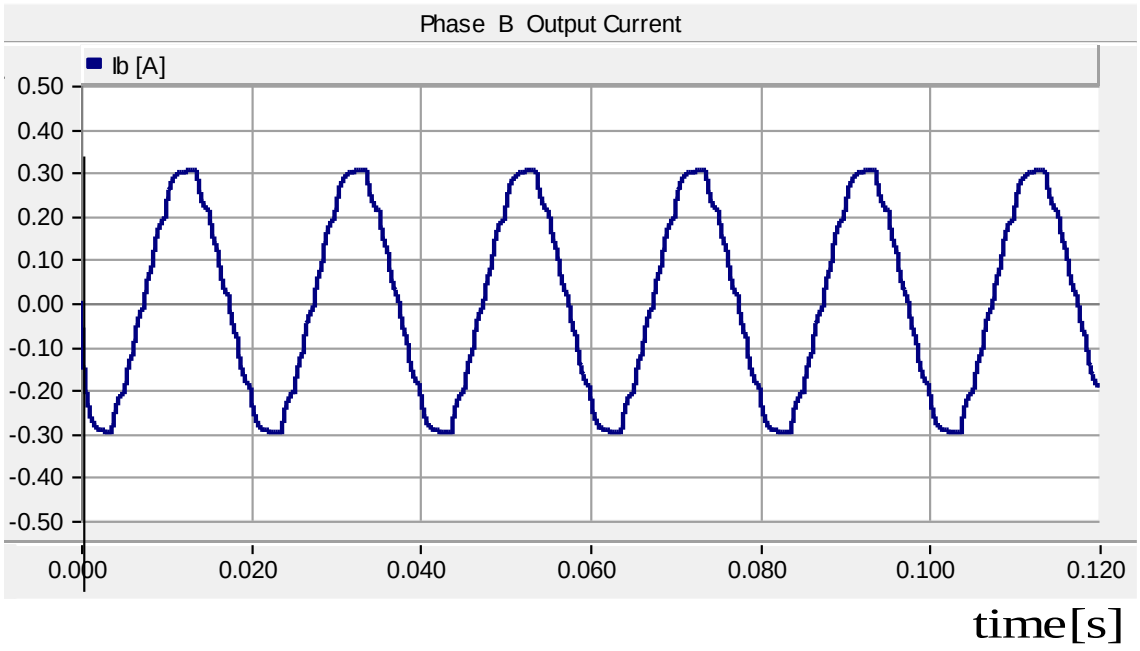


Figure 5.6: Phase B load current waveform

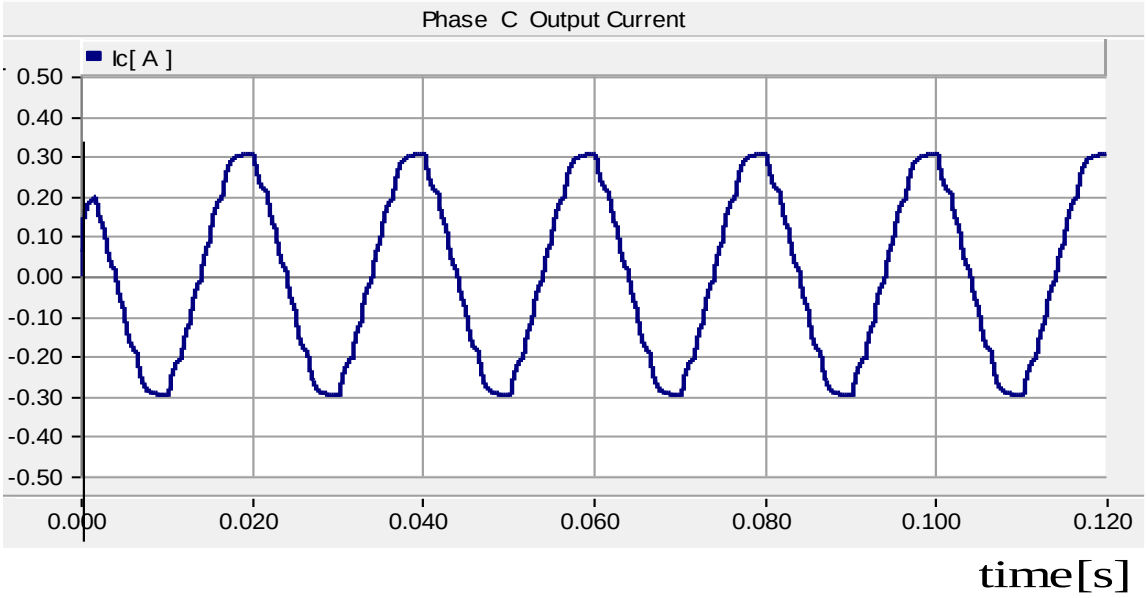


Figure 5.7: Phase C load current waveform

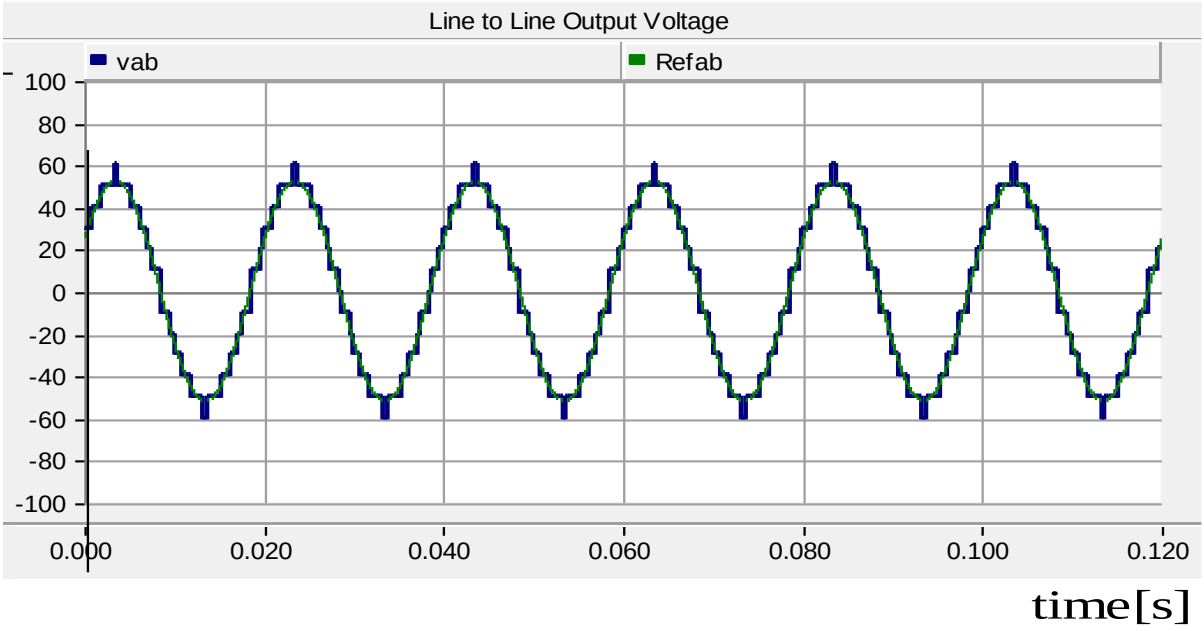


Figure 5.8: Phase AB line-to-line load voltage waveform

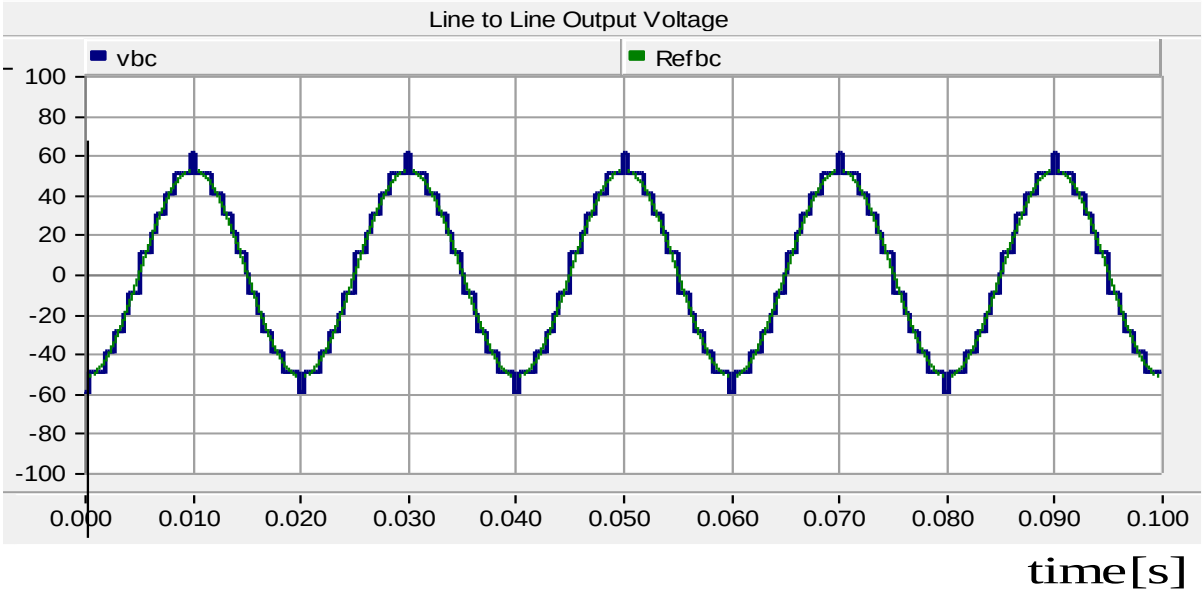


Figure 5.9: Phase BC line-to-line load voltage waveform

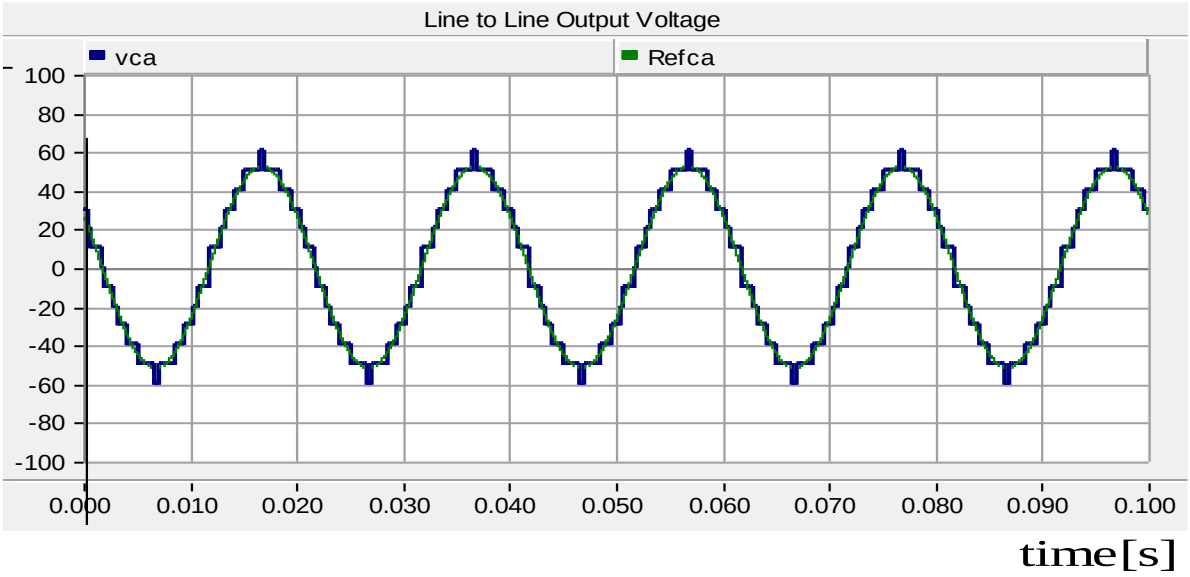


Figure 5.10: Phase CA line-to-line load voltage waveform

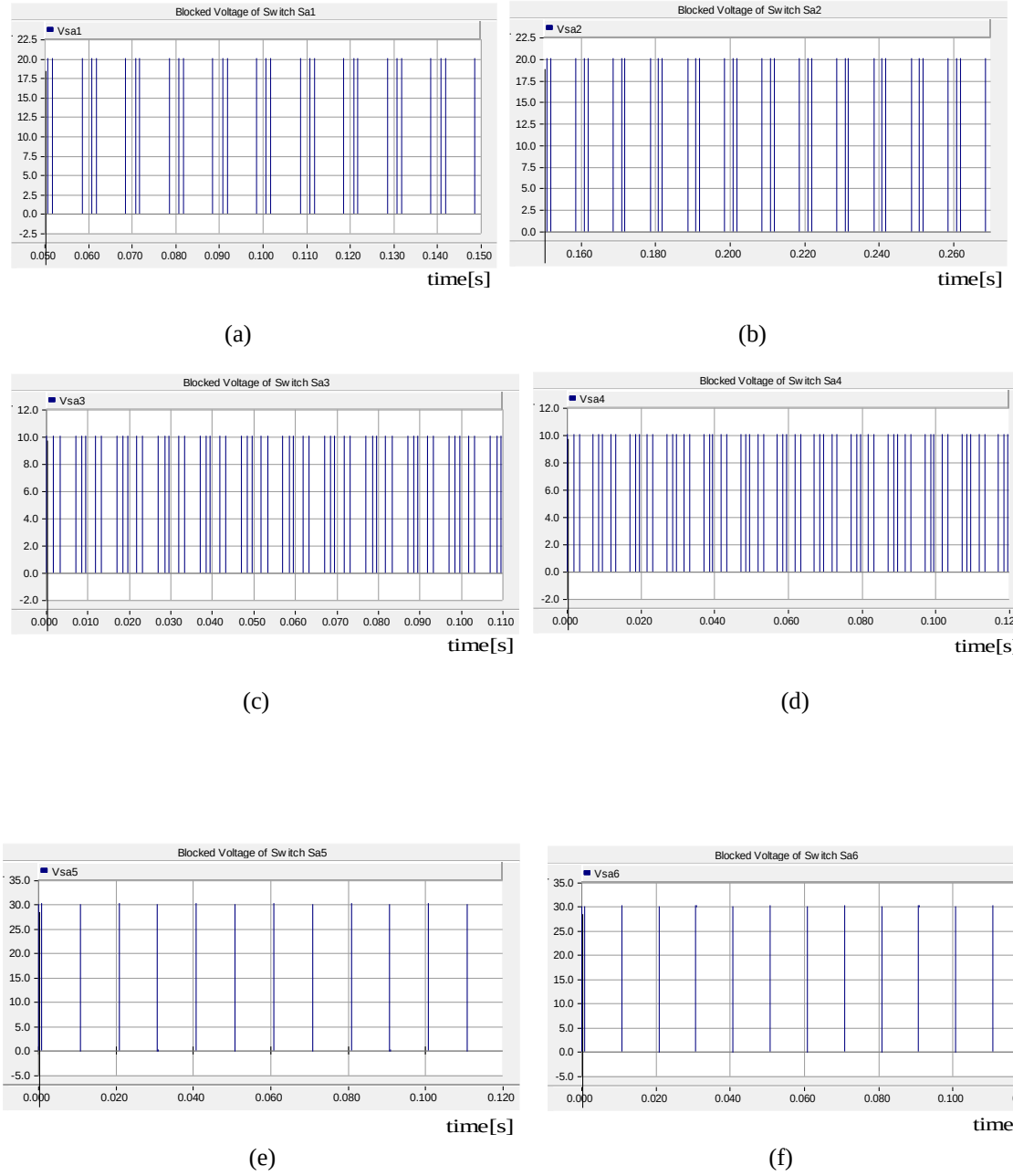


Figure 5.11: Blocked voltage of switches in Phase A. (a) Blocked voltage of switch Sa1; (b) Blocked voltage of switch Sa2; (c) Blocked voltage of switch Sa3; (d) Blocked voltage of switch Sa4; (e) Blocked voltage of switch Sa5; (f) Blocked voltage of switch Sa6.

Table 5.2 shows the simulation parameters of diodes and switches which are used in calculating the efficiency of the proposed multilevel inverter. Efficiency of the proposed inverter is determined for three case scenarios with varying input and output voltages. In the first case

illustrated by Table 5.3, the input voltage is 20V and the output voltage is 60V, the corresponding input and output powers are 54.65W and 54.305W respectively. The total power losses are 0.343W. Efficiency of the inverter with these data is 99.36%. Varying the input voltage from 20V to 50V and 100V provides 99.37% and 99.36% efficiency accordingly as indicated in Table 5.4 and Table 5.5 respectively.

Table 5.2: Parameters used in the simulation to calculate losses

V_F (Diode)	r_d (Diode)	C_p (Diode)	V_F (switch)	r_d (switch)	C_P (switch)
0.7V	0.1Ω	$4\mu F$	1.1V	0.2Ω	$500\mu F$

Table 5.3: Loss distribution results in the simulation when $V_{in} = 20V$

V_{in} = 20V			V_{out} (peak) = 60V	
P_{in} = 54.65W			P_{out} = 54.305W	
P_{rd} (Diodes) 0.0017W	P_{rd} (Switches) 0.322W	P_{VF} (Diodes) 0.001W	P_{VF} (switches) 0.001W	P_{CS} 0.002W
			η = 99.36%	

Table 5.4: Loss distribution results in the simulation when $V_{in} = 50V$

V_{in} = 50V			V_{out} (peak) = 150V	
P_{in} = 341.557W			P_{out} = 339.436W	
P_{rd} (Diodes) 0.093W	P_{rd} (Switches) 2.03822W	P_{VF} (Diodes) 0.002W	P_{VF} (switches) 0.002W	P_{CS} 0.002W
			η = 99.37%	

Table 5.5: Loss distribution results in the simulation when $V_{in} = 100V$

V_{in} = 100V			**V_{out} (peak) = 300V**	
P_{in} = 1366.32W			P_{out} = 1357.78W	
P_{rd} (Diodes) 0.43W	P_{rd} (Switches) 8.1W	P_{VF} (Diodes) 0.003W	P_{VF} (switches) 0.002W	P_{CS} 0.002W
			η = 99.37%	

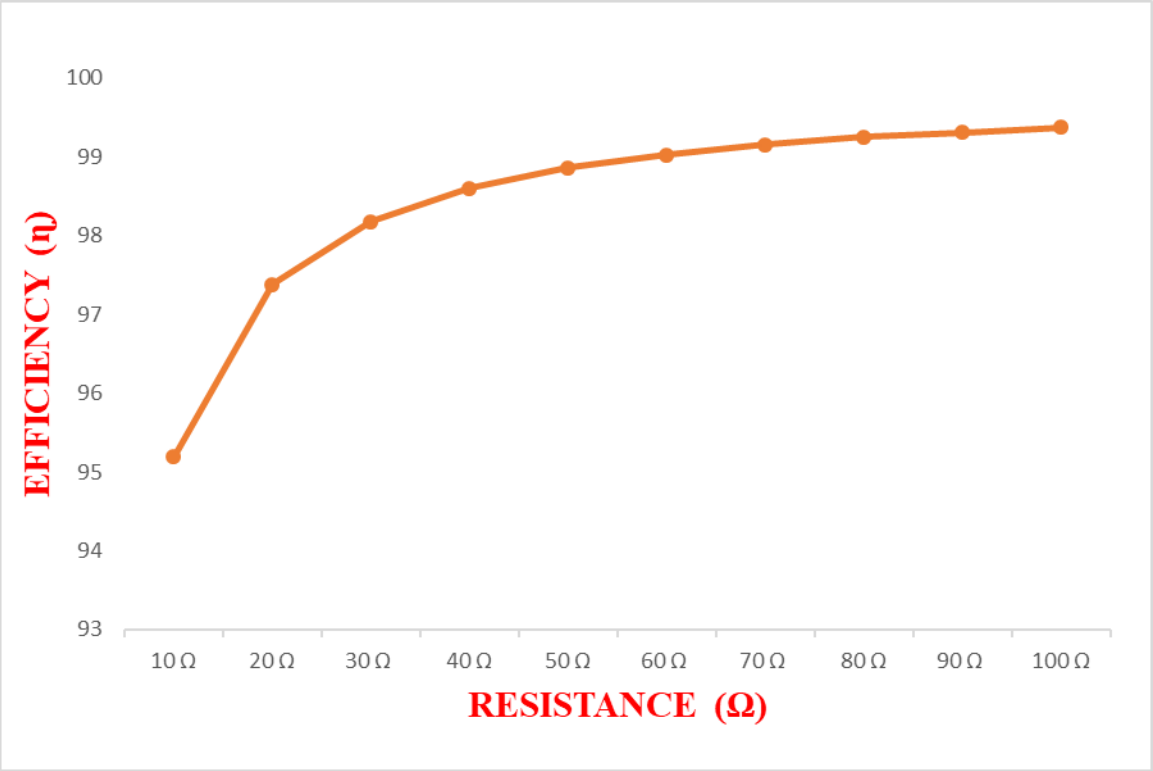


Figure 5.12: Efficiency curve with constant input voltage (100V)

Fig. 5.12 illustrates efficiency curve with constant input voltage of 100V magnitude but varying load resistances. The efficiency curve was generated by simulation, varying the input voltage produces equivalent efficiency values as shown by the graph. The load resistance are varied between 10Ω and 100Ω.

5.3 Experimental Results

Laboratory setup of the proposed topology is built using the parameters of Table 5.6. This is done so as to validate the results obtained from simulation using the same parameters of Table 5.1. Because of the symmetric nature of all phases of the proposed topology, experimental results are produced for Phase A only. The laboratory setup of the proposed three-phase topology is illustrated by Fig. 5.13. Experimental load voltage and load current waveforms of Phase A are illustrated by Fig. 5.14. Experimental blocking voltage waveforms of selected switches in Phase are shown Fig. 5.15. Laboratory prototype result affirms the results obtained from simulation. The practicability of the proposed three-phase MLI is validated by results of laboratory prototype and simulation.

Table 5.6: Simulation and Implementation Parameters

Parameters	**Value**
Input voltage V_{dc}	$V_1 = V_3 = 20V$, $V_2 = V_4 = 10V$
Output Resistance R	100Ω
Output Inductance L	55mH
Switching Frequency f_s	4kHz
Output Frequency f_o	50Hz
Modulation Index	1

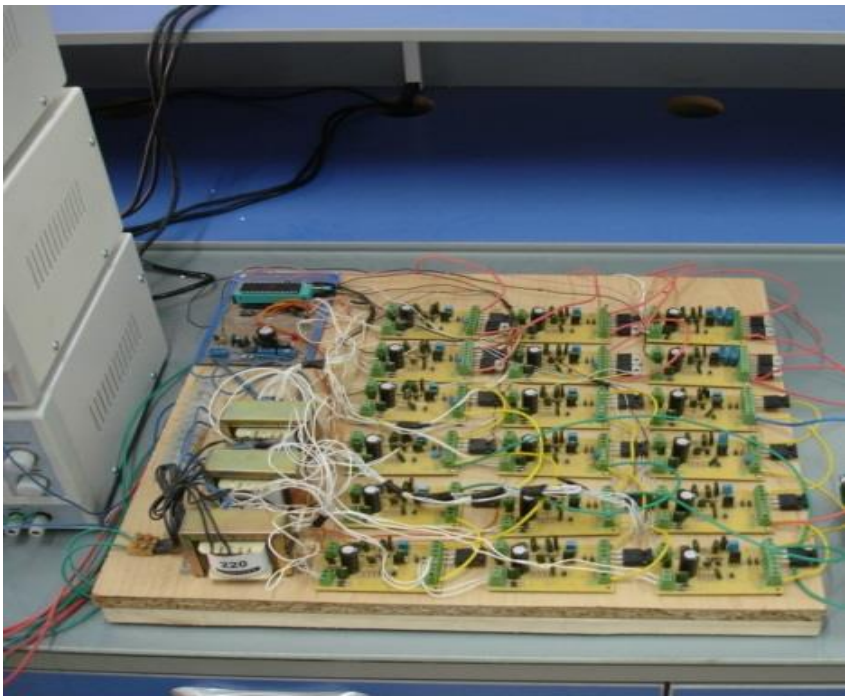


Figure 5.13: Experimental prototype.

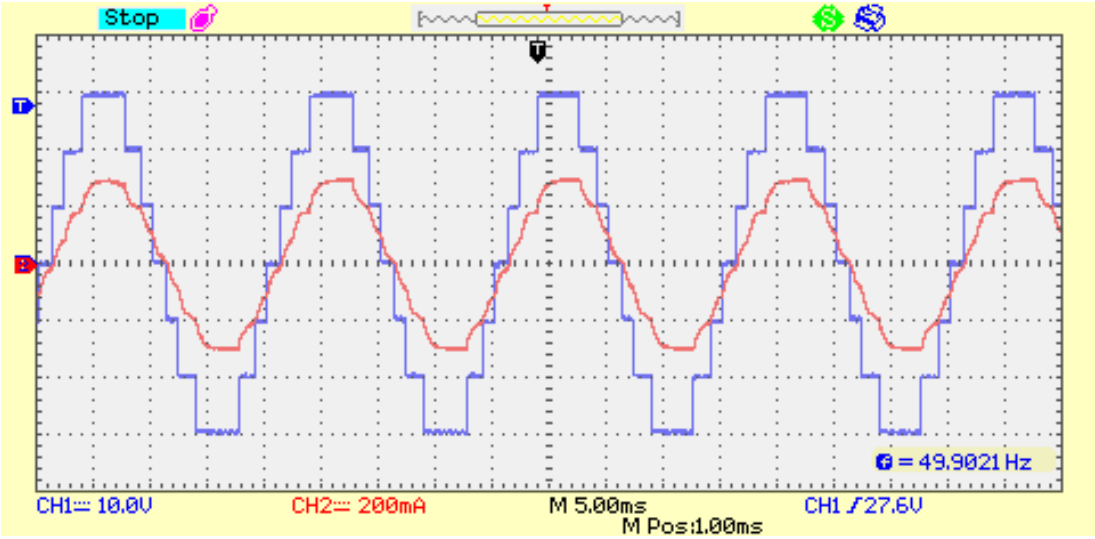
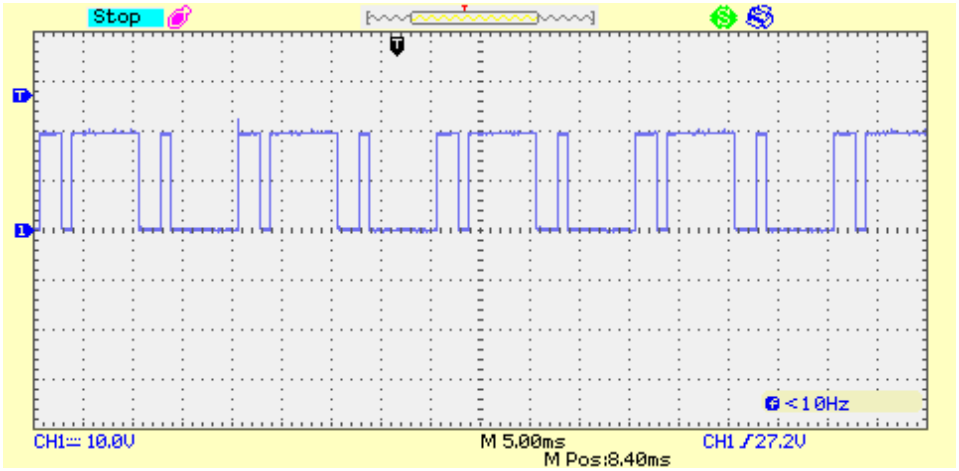
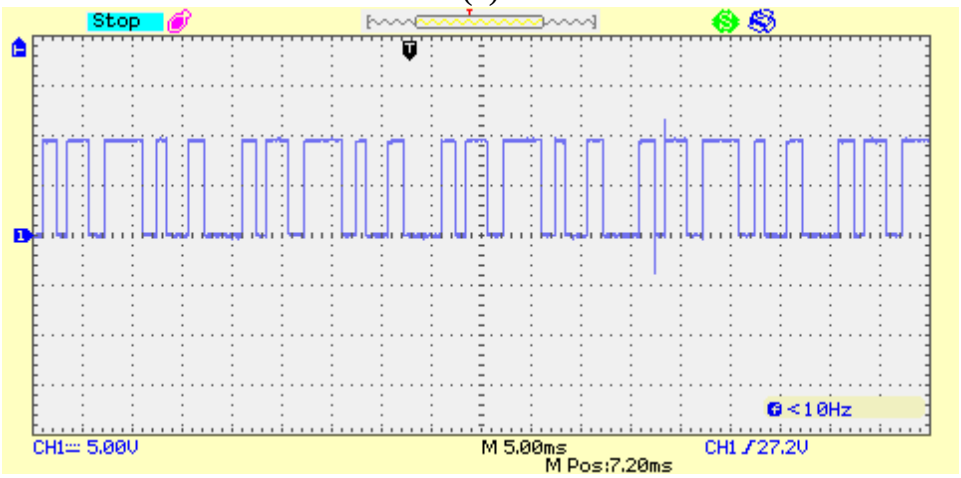


Figure 5.14: Phase A voltage and current **e**xperimental waveforms

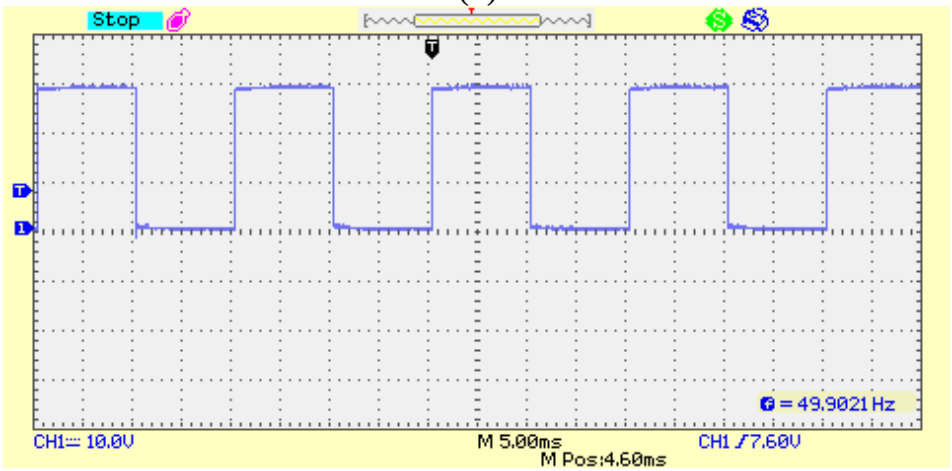
The load output waveform derived experimentally for phase A load voltage and current are illustrated by Fig. 513, the current waveform is depicted by red color whiles the voltage waveform is depicted by blue color, the magnitude of these parameters are 200mA and 49.9V respectively.



(**a**)



(**b**)



(**c**)

Figure 5.15: Blocked voltage of switches in Phase A. (a) Blocked voltage of switch Sa_1; (b) Blocked voltage of switch Sa3; (c) Blocked voltage of switch Sa5

5.4 Multilevel Inverter Based DVR Simulation

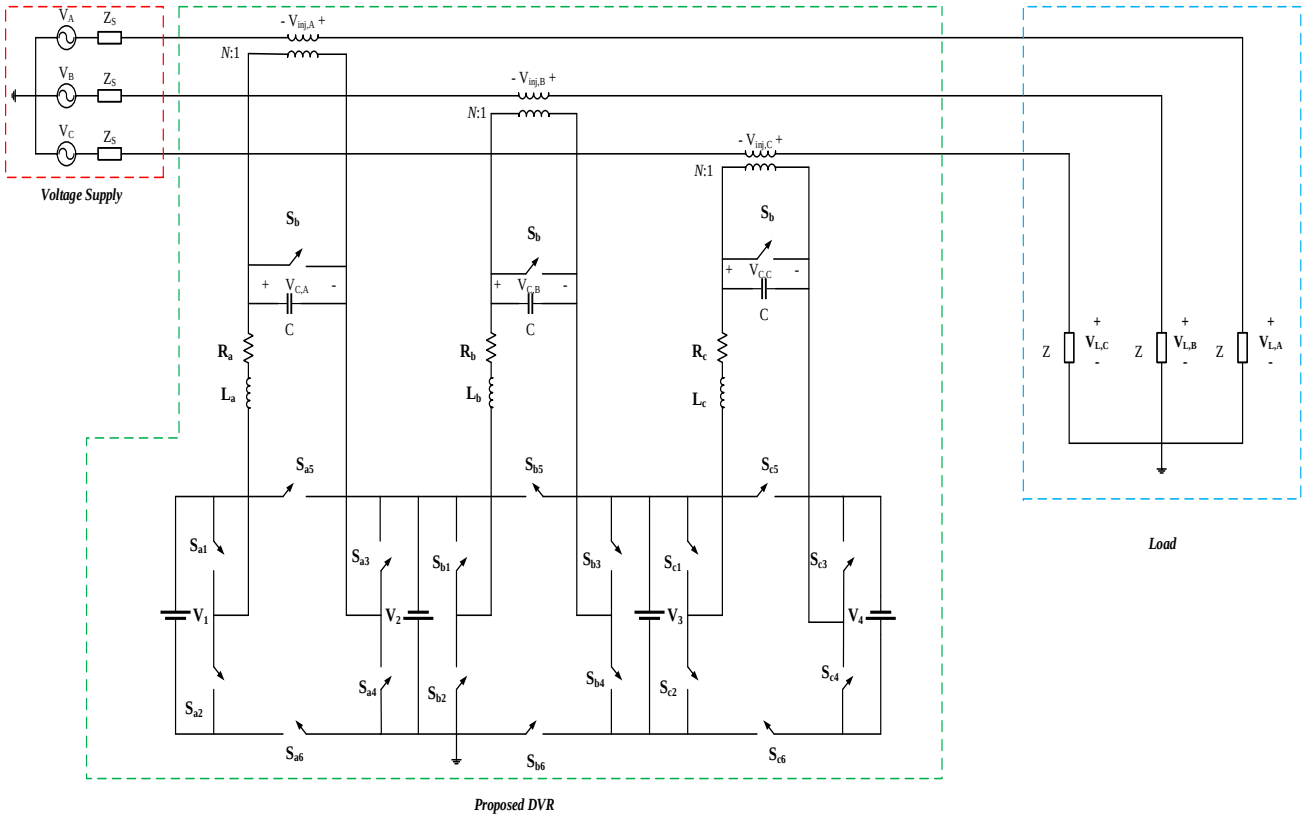


Figure 5.16: Proposed DVR Topology

The proposed three-phase MLI DVR system is illustrated by Fig. 5.16. The proposed DVR system is composed of three main parts namely; (a) voltage supply, (b) proposed DVR and (c) sensitive load. Implementation of the proposed three-phase MLI based DVR in PSCAD software is illustrated in appendix 2 of this thesis.

Under grid disturbances, the quality of voltage deteriorates thereby causing destruction of sensitive loads mostly located in hospitals, factories etc. Voltage sag and swell are some of the negative effects due to these disturbances. The proposed three-phase MLI DVR is utilized to overcome these drawbacks. Figure 5.17 (upper section) shows three-phase voltage sag and swell disturbances in the grid. The duration of the voltage sag is 0.1s (0.2s – 0.3s) whiles the voltage swell duration is 0.1s (0.4s – 0.5s). The lower part of Fig. 5.17 shows the same grid voltage after

using the proposed three-phase MLI DVR to compensate the voltage sag and swell. Fig. 5.18 to Fig. 5.20 shows the grid voltage for phases A, B and C for the following cases:

- Before voltage sag
- Before voltage swell
- During Voltage sag and swell
- After compensation of voltage sag and swell

The voltage sag disturbance in the supply is corrected by injecting positive voltage of equivalent magnitude and phase into the supply, therefore positive 60V was injected by DVR for sag compensations, similarly, negative 60V was injected by the DVR to compensate for swell disturbances. This procedure is repeated for all phases of the supply.

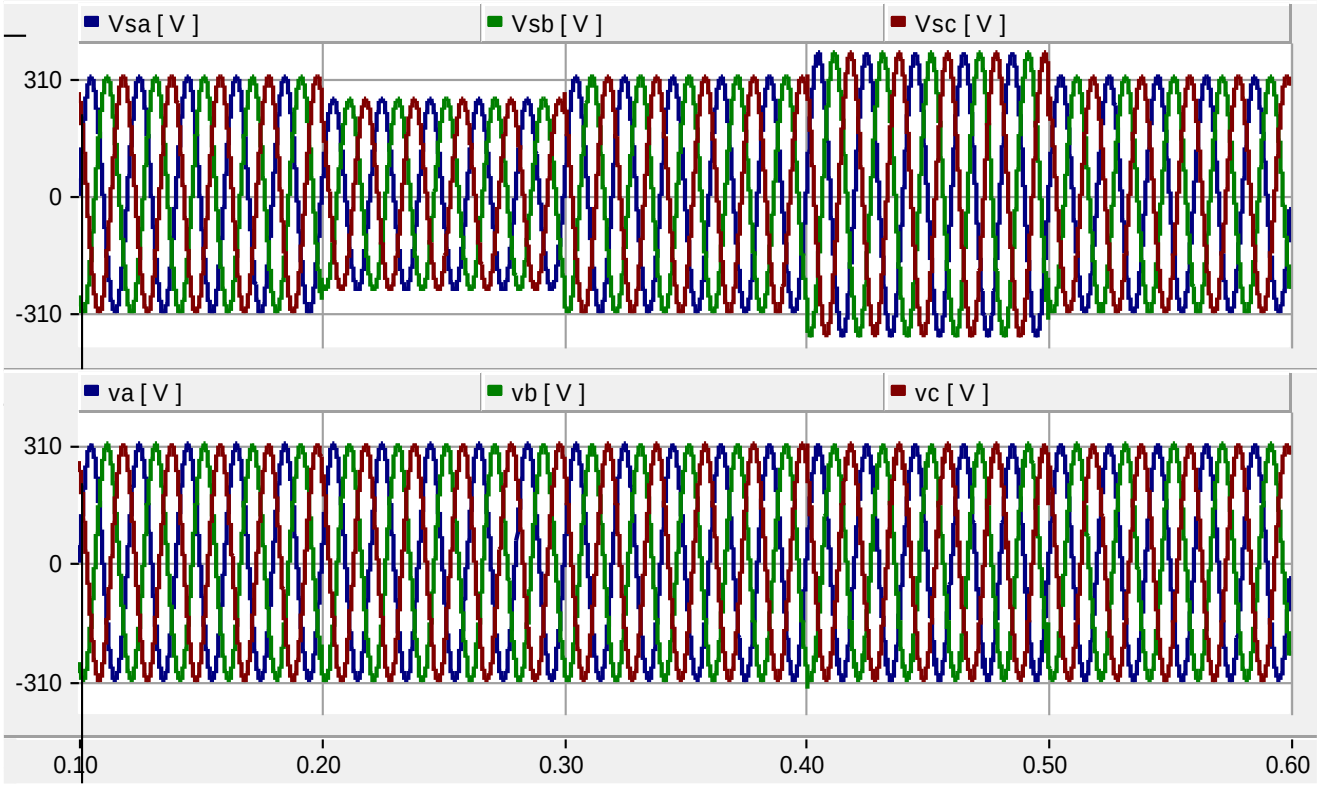


Figure 5.17: Three-phase input and output voltage waveforms under grid disturbances

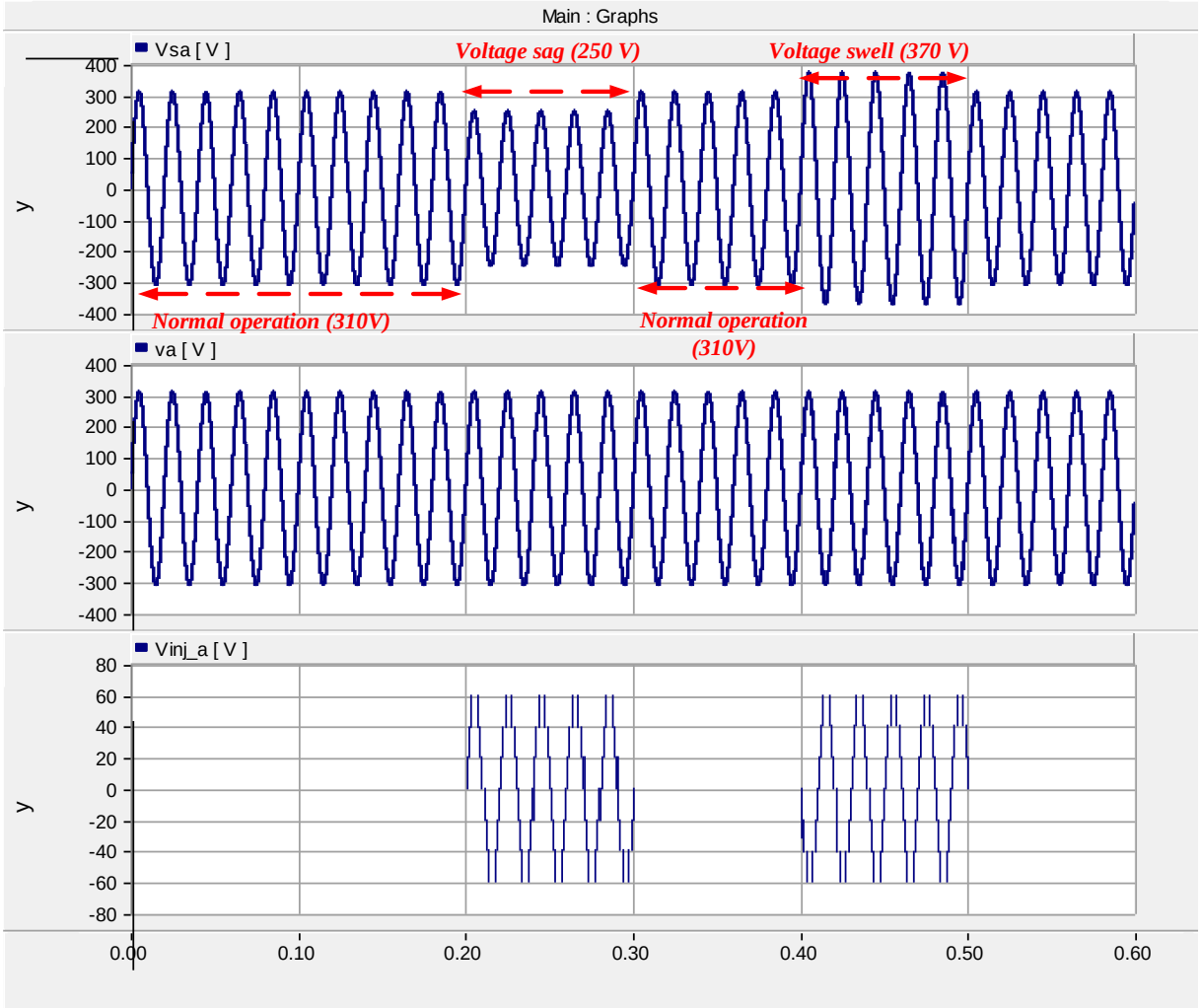


Figure 5.18: Waveform of input and output voltages of phase "A" and voltage injected by DVR (top to bottom input voltage of phase "A", load voltage of phase "A" and voltage injected in phase "A", respectively)

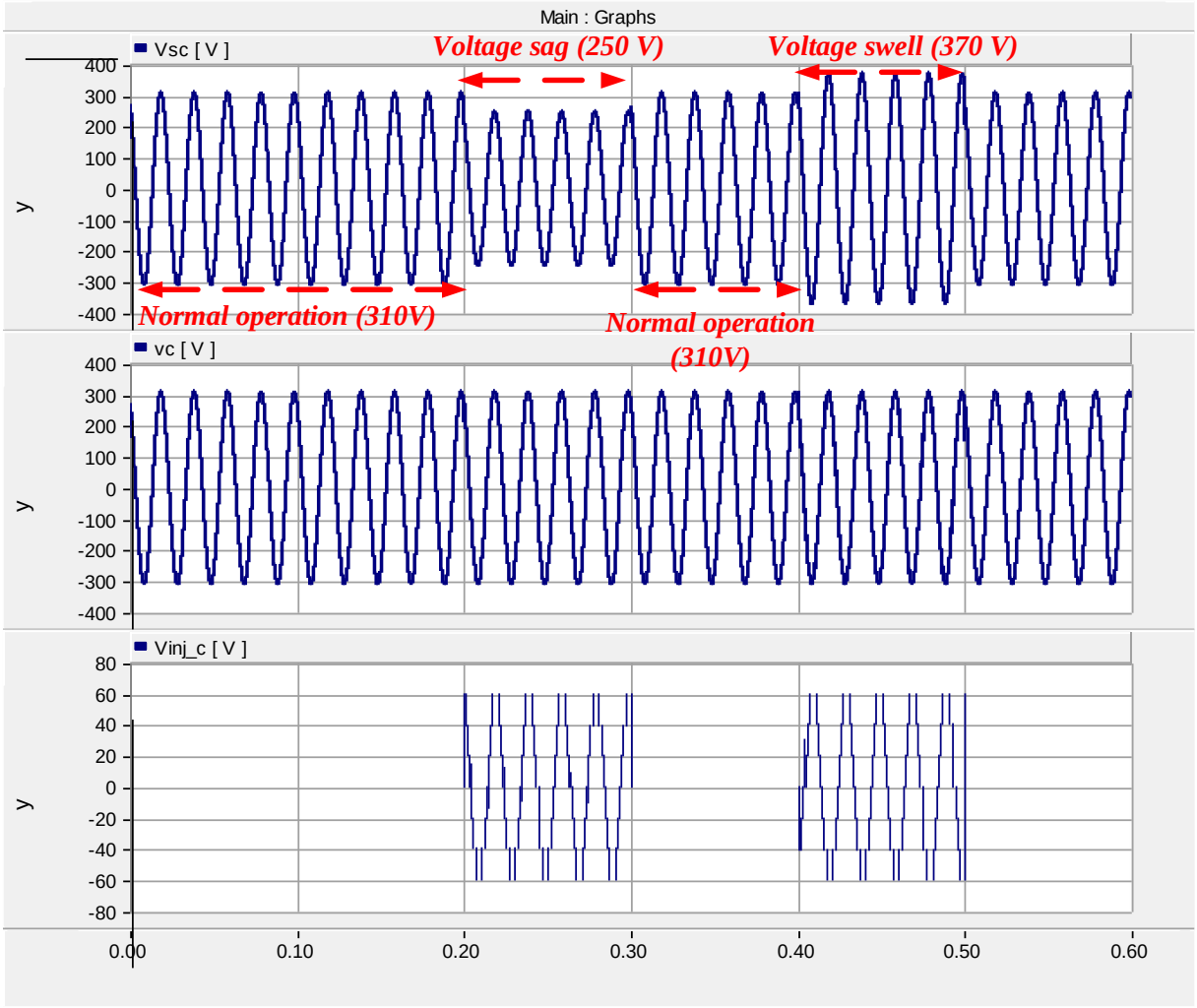


Figure 5.19: Waveform of input and output voltages of phase "B" and voltage injected by DVR (top to bottom input voltage of phase "B", load voltage of phase "B" and voltage injected in phase "B", respectively)

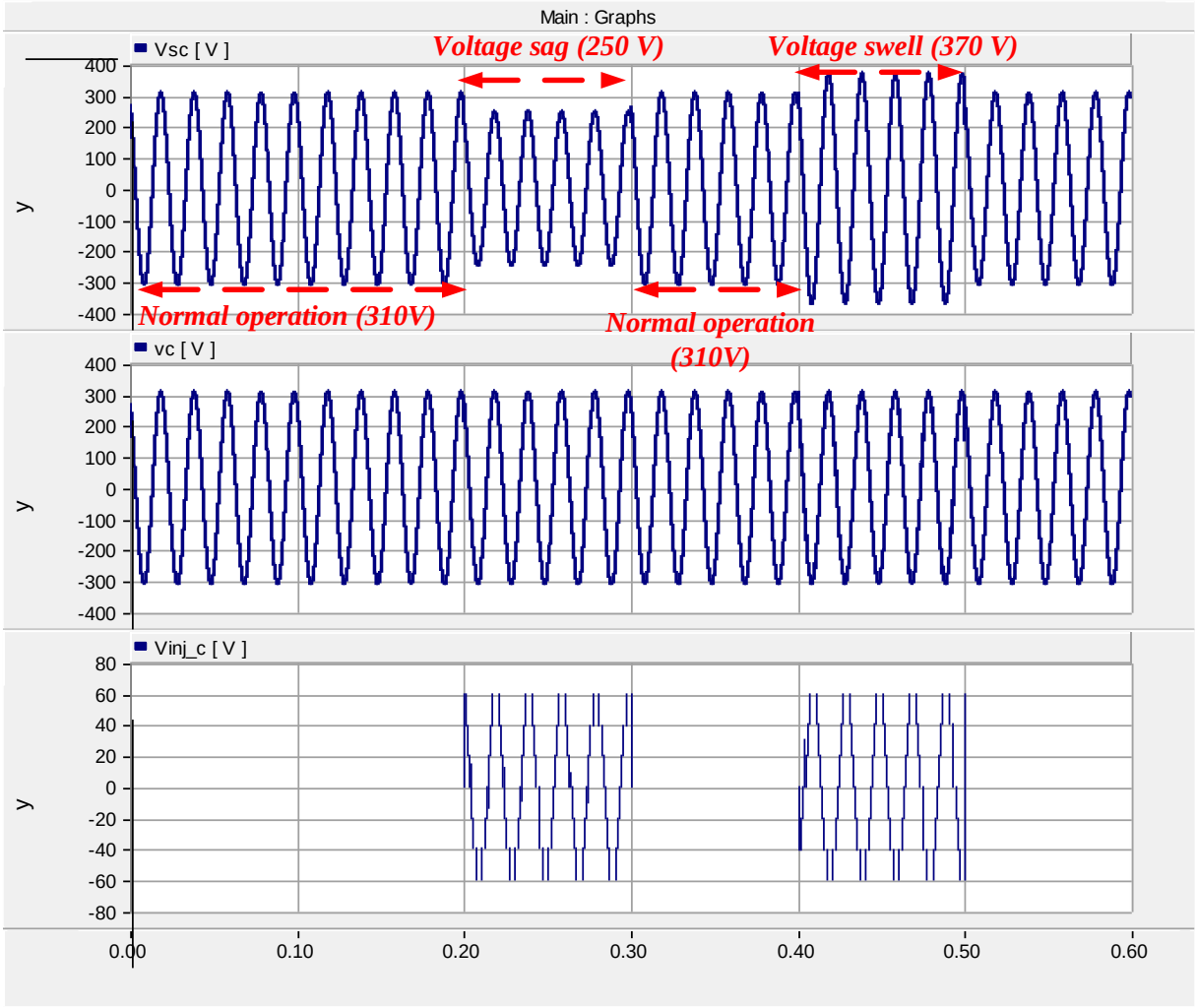


Figure 5.20: Waveform of input and output voltages of phase "C" and voltage injected by DVR (top to bottom input voltage of phase "C", load voltage of phase "C" and voltage injected in phase "C", respectively).

5.5 DVR Simulation Results with Varying Voltage Sag and Swell Values

This section provides simulation waveforms for various voltage sag and swell values and the appropriate compensating voltage values. Fig. 5.21 shows a 310V load voltage system with 160V voltage sag condition and 460V voltage swell condition. 150V compensating voltage was injected by the DVR to resolve these disturbances. The input voltage of the MLI in the DVR topology during this condition is 50V for both isolated dc sources in each phase. Therefore, the maximum phase output voltage of the multilevel inverter is 150V. Due to the symmetry nature of the MLI, only phase A output waveforms are illustrated in this section.

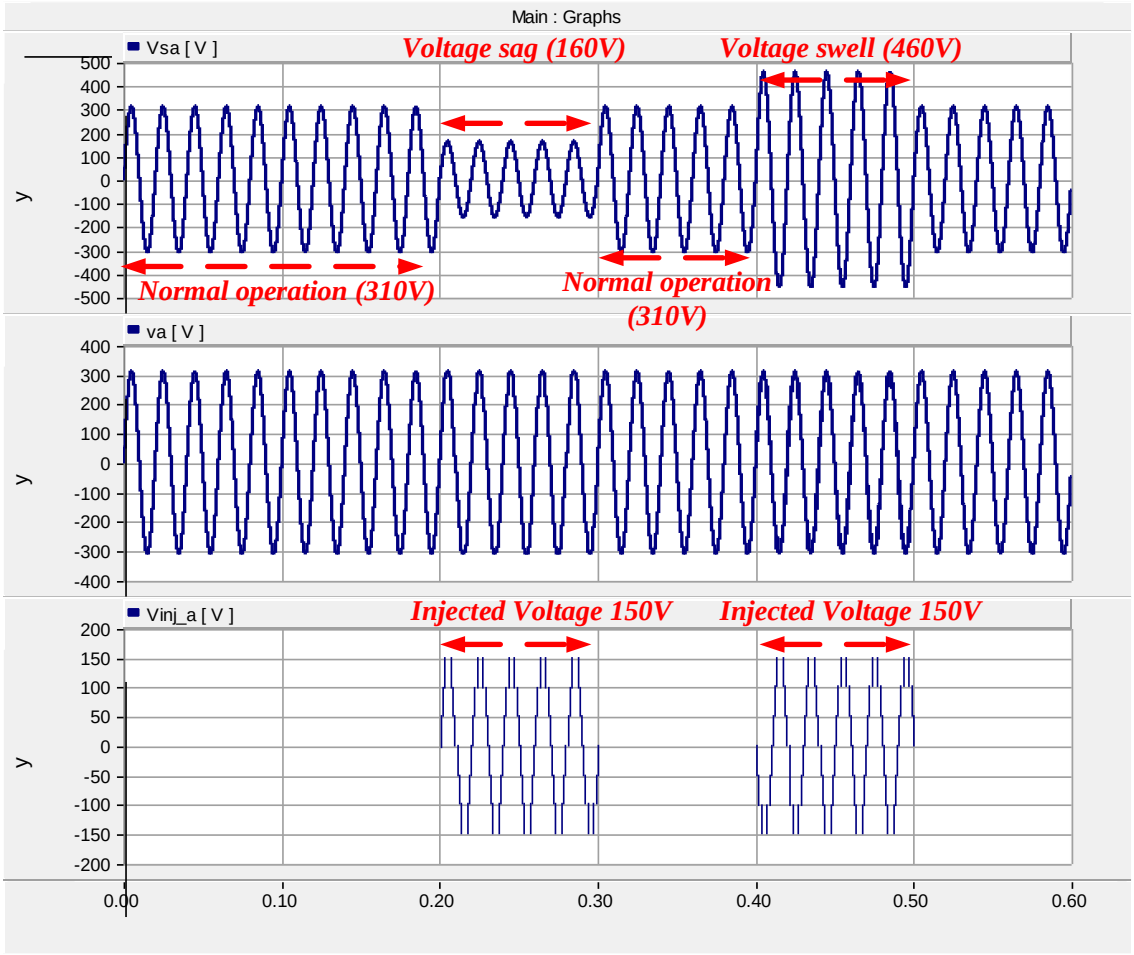


Figure 5.21: Varying sag and swell DVR output waveform

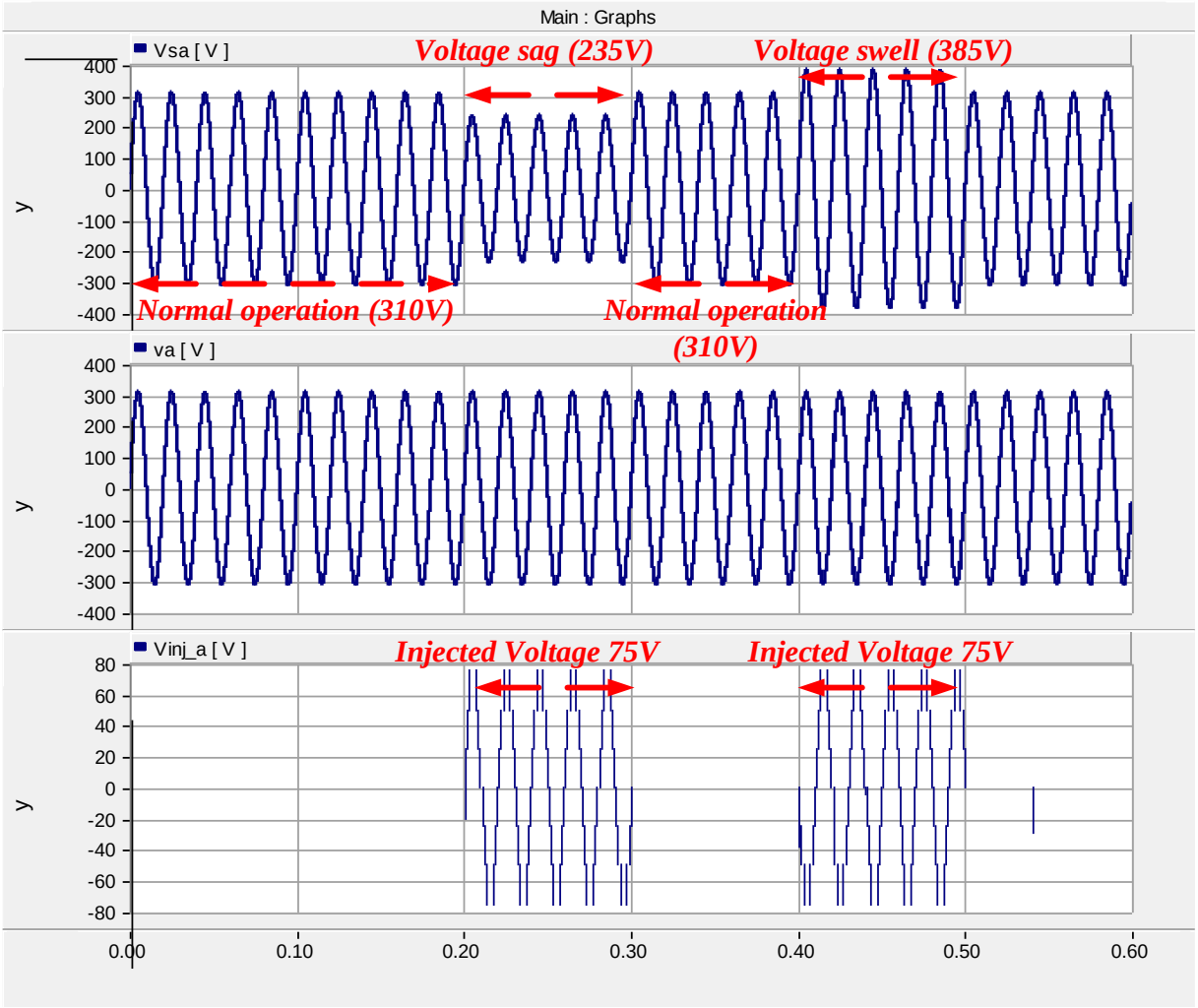


Figure 5.22: Varying sag and swell DVR output waveform

Fig. 5.22 shows a 310V load voltage system with 235V voltage sag condition and 385V voltage swell condition. 75V compensating voltage was injected by the DVR to resolve these disturbances. The input voltage of the MLI in the DVR topology during this condition is 15V and 30V for both isolated dc sources in each phase. Therefore, the maximum phase output voltage of the multilevel inverter is 75V.

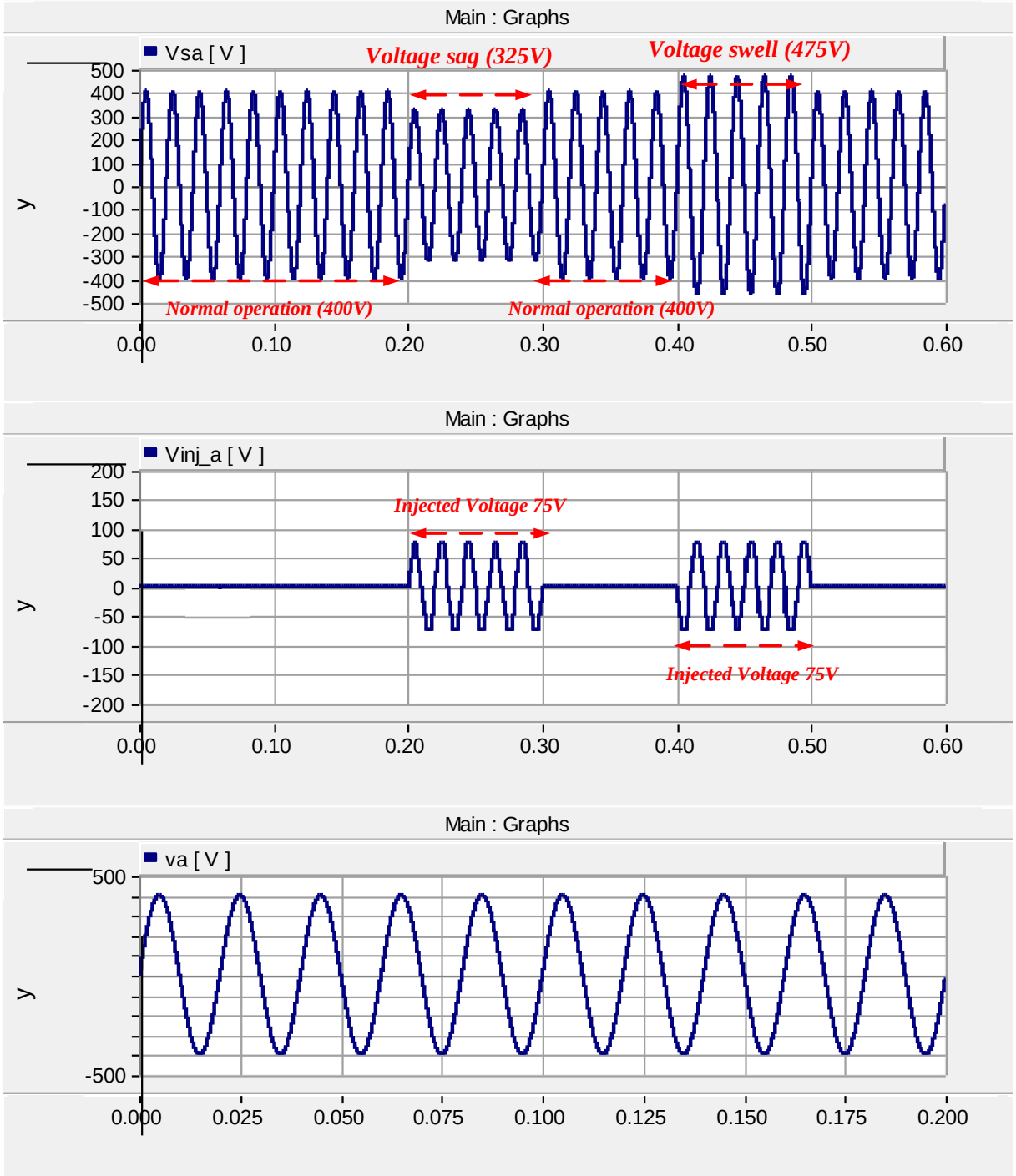


Figure 5.23: Varying sag and swell DVR output waveform

Fig. 5.23 shows a 400V load voltage system with 325V voltage sag condition and 475V voltage swell condition. 75V compensating voltage was injected by the DVR to resolve these

disturbances. The input voltage of the MLI in the DVR topology during this condition is 25V and 50V for both isolated dc sources in each phase. Therefore, the maximum phase output voltage of the multilevel inverter is 75V.

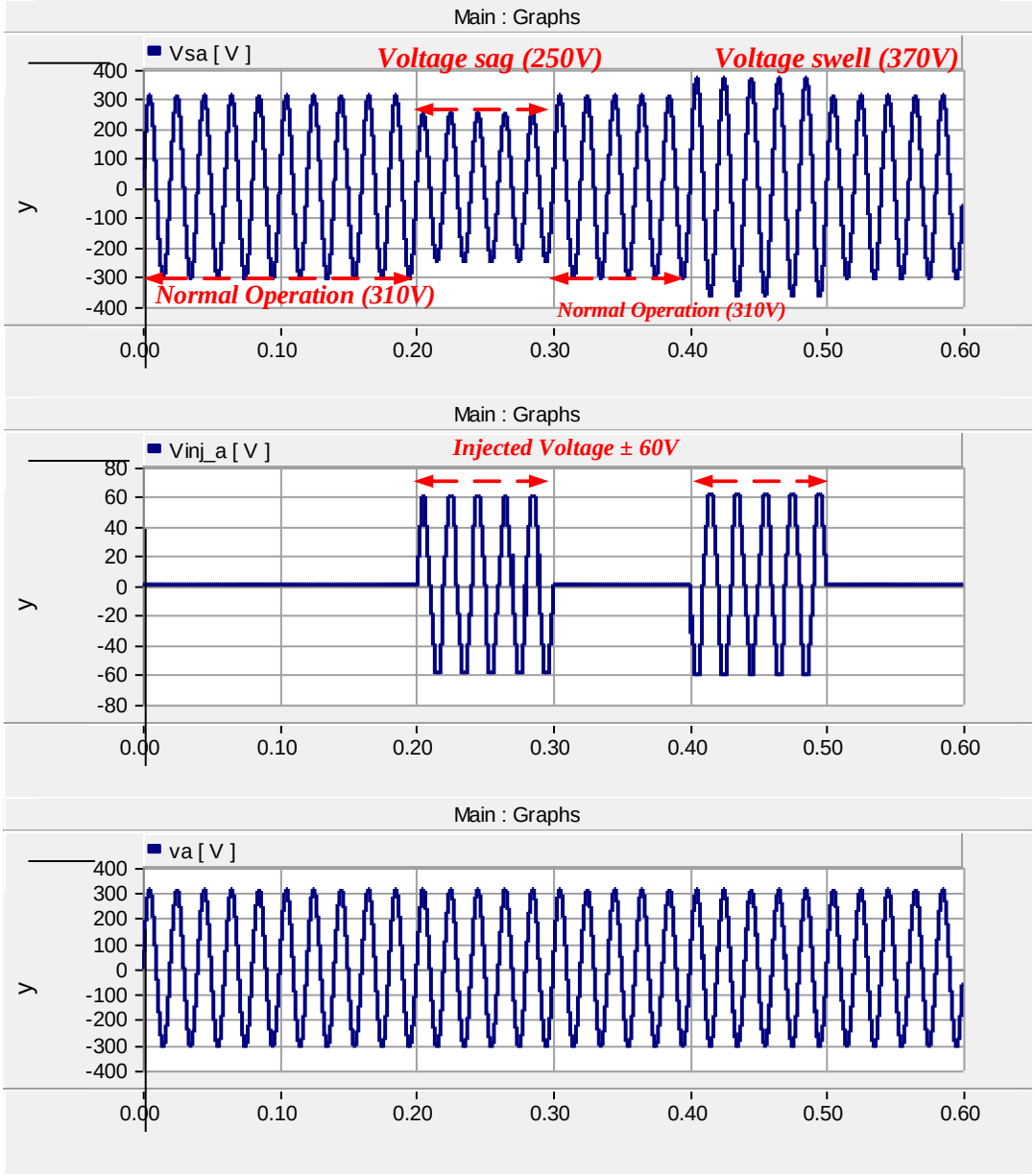


Figure 5.24: Phase A waveform for sag and swell condition

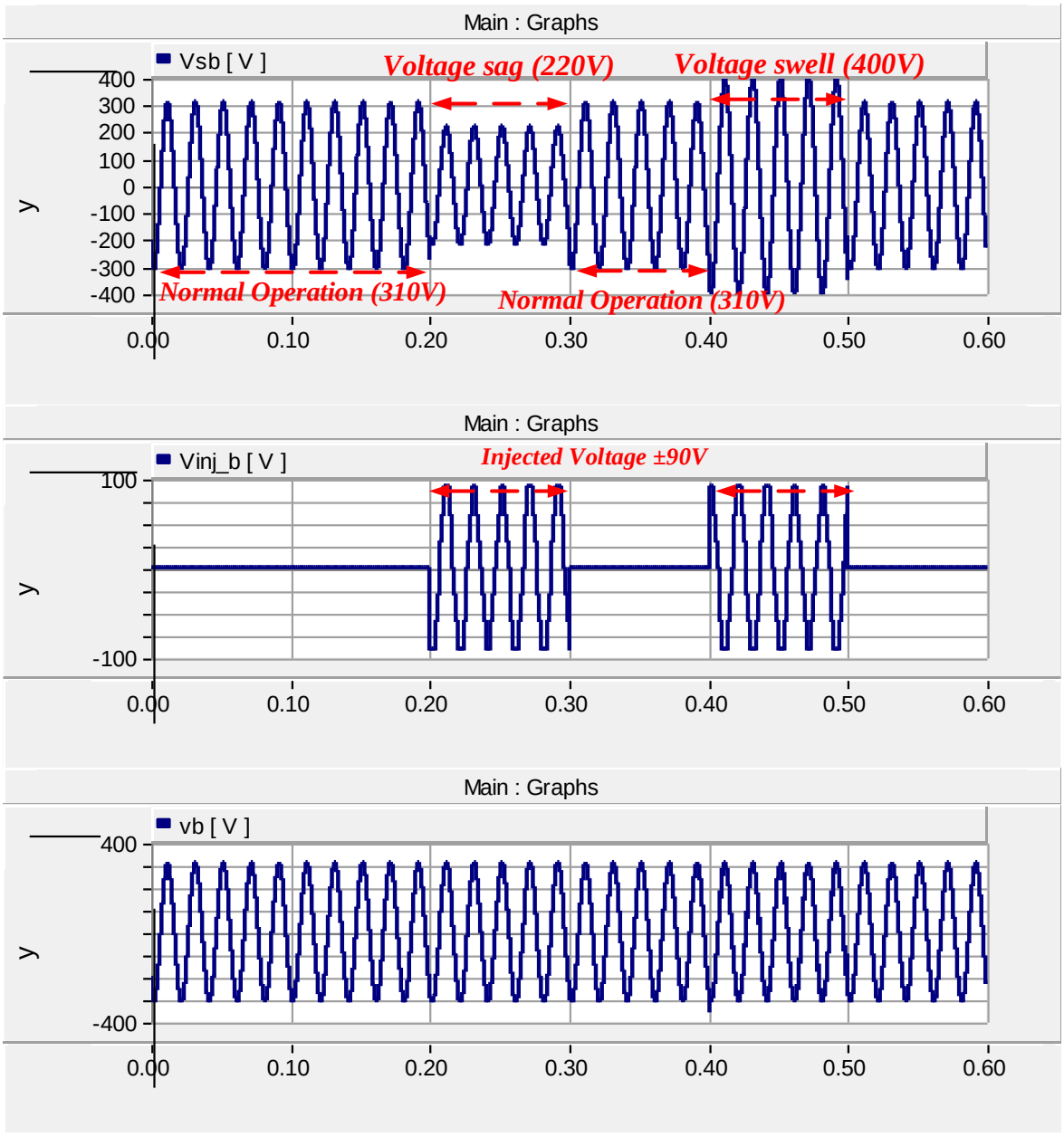


Figure 5.25: Phase B waveform for sag and swell condition

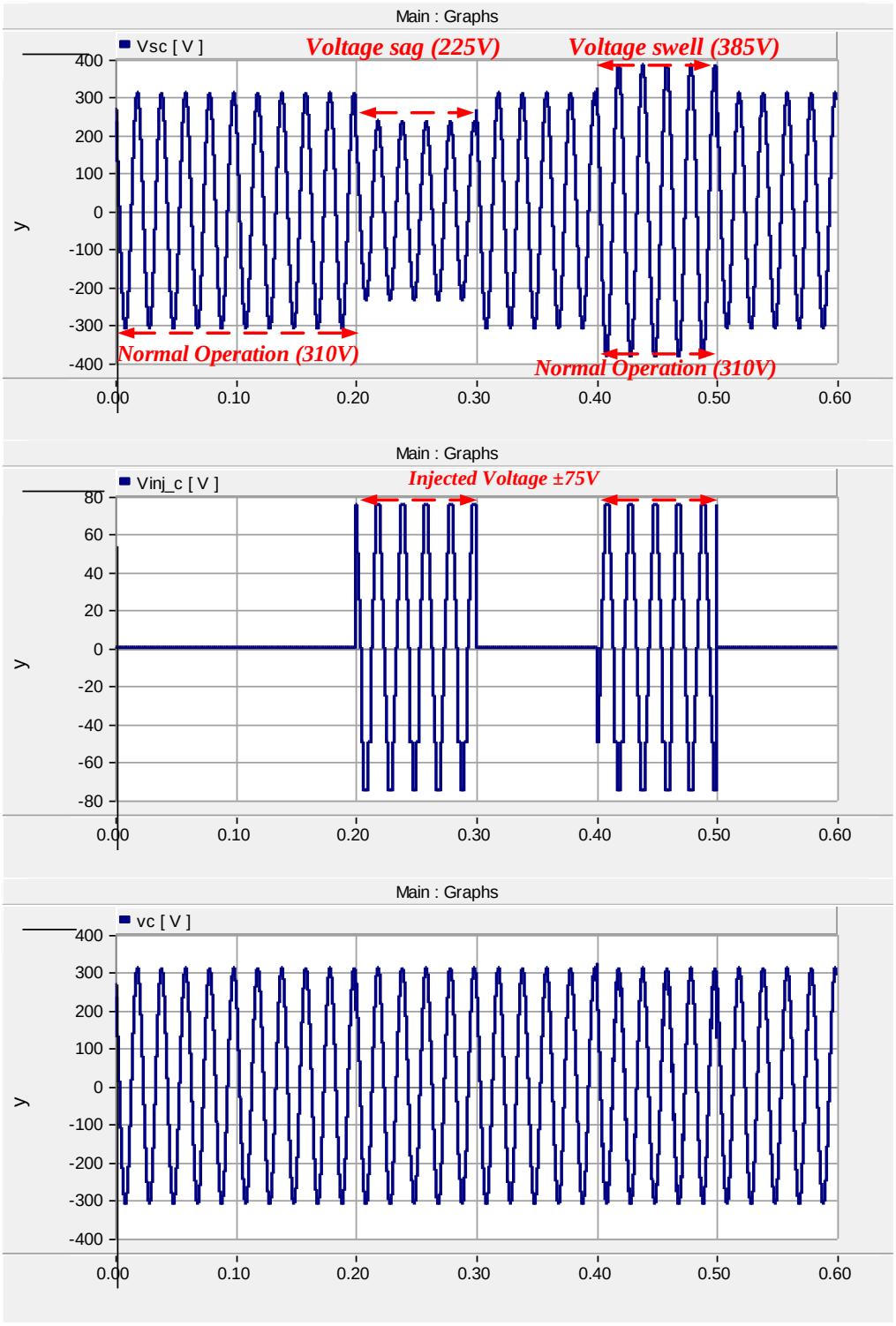


Figure 5.26: Phase C waveform for sag and swell condition

Analysis of the DVR has been done with different voltage sag and swell values for the three-phase system. Each phase encounters different magnitude of voltage sag and swell values from the others. The simulation results of this analysis is provided by Fig. 5.24 to Fig. 5.26. In phase A, shown by Fig. 5.24, the voltage sag and swell values are 250V and 370V accordingly, the injected voltage is +60V and -60V for the sag and swell condition respectively. In phase B, shown by Fig. 5.25, the voltage sag and swell values are 220V and 400V accordingly, the injected voltage is +90V and -90V for the sag and swell condition respectively. In phase C, shown by Fig. 5.24, the voltage sag and swell values are 225V and 385V accordingly, the injected voltage is +60V and -60V for the sag and swell condition respectively.

5.6 DVR Simulation under Varying Fault Conditions

In this simulation, operation of the dynamic voltage restores (DVR) under different fault conditions are investigated. In general, DVR is a power electronic device used to restore the grid's voltage to the normal condition when a fault occurs. From the topological aspect, DVR comprises an inverter that compensates the faulty conditions such as voltage sag-swell, unbalanced voltages and etc. Before beginning the analysis, some assumptions are required, such as the normal condition's definition. The assumptions are as follows:

1. The input three-phase voltages (v_{sa}, v_{sb}, and v_{sc}) in the normal condition are as follows:

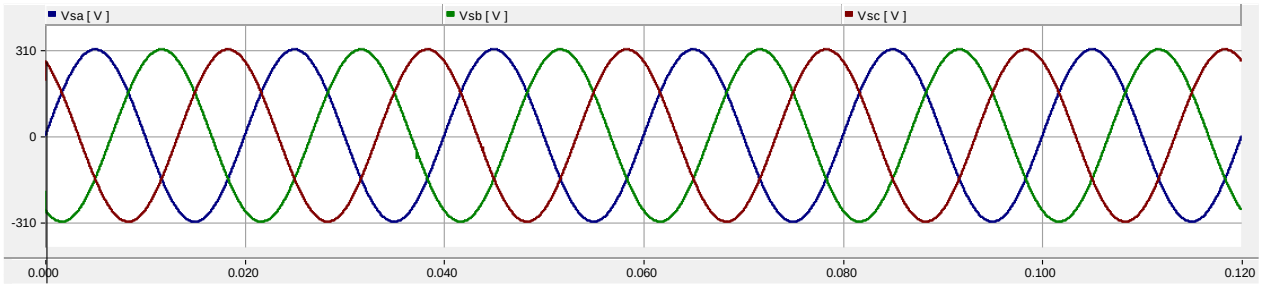
$$\begin{aligned} v_{Sa} &= 310\sin(100\pi t) \\ v_{Sb} &= 310\sin(100\pi t - 120°) \\ v_{Sc} &= 310\sin(100\pi t - 240°) \end{aligned} \tag{5.1}$$

2. The voltages on the three-phase output load are identified by v_a, v_b, and v_c for the phases A, B, and C, respectively.

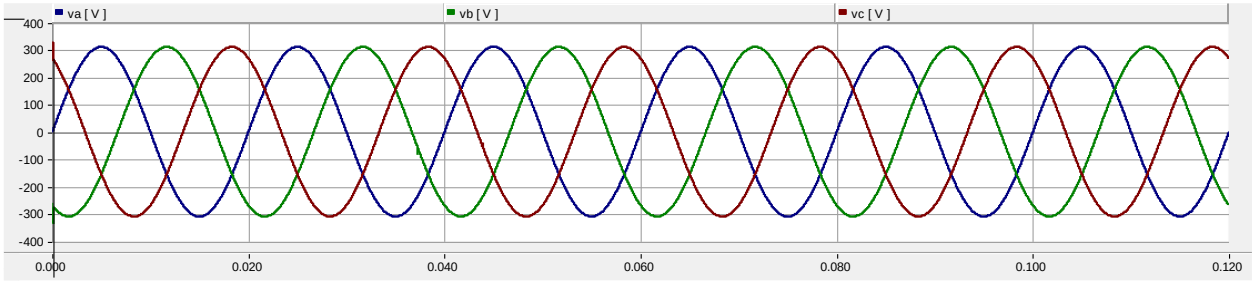
To study the working principle of this DVR, different case studies are considered, which are provided in the next sections:

Case Study #1 Normal Condition

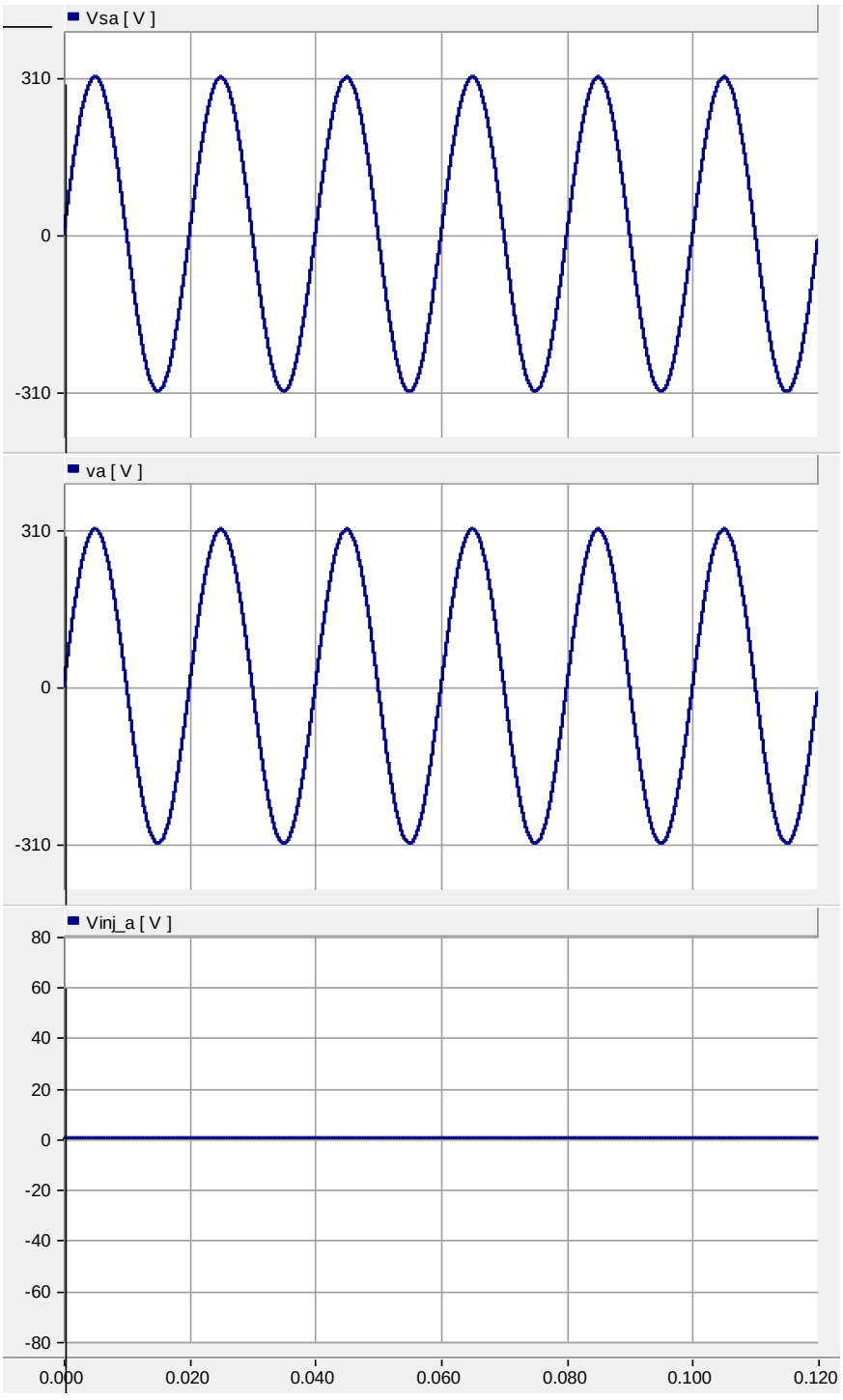
In this case study, it is assumed that no fault occurs. In other words, all input voltages are equivalent at all times. So, it is anticipated that DVR does not inject any voltages to the phases. To validate this claim, Fig. 1 shows the operation of DVR.



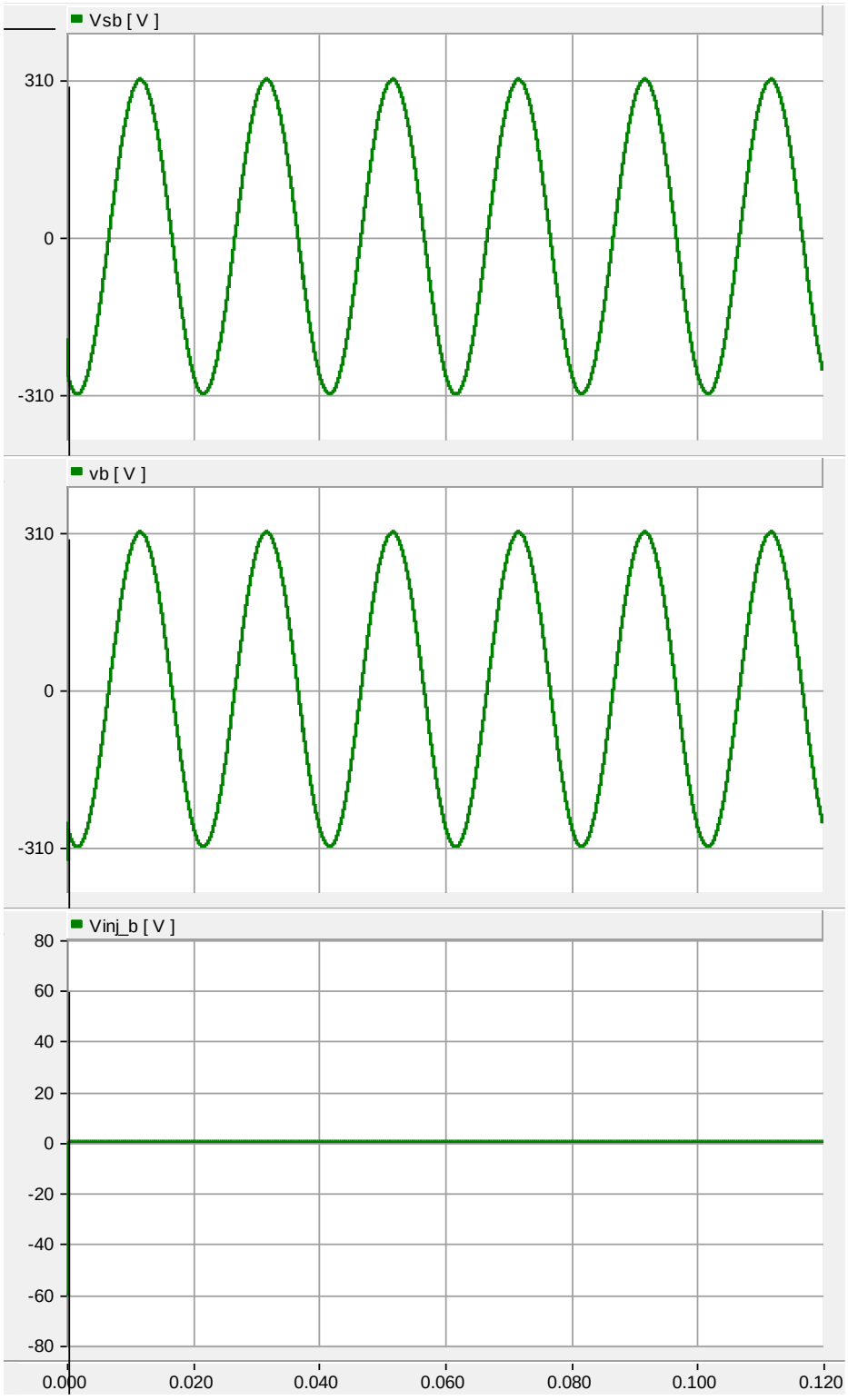
(a)



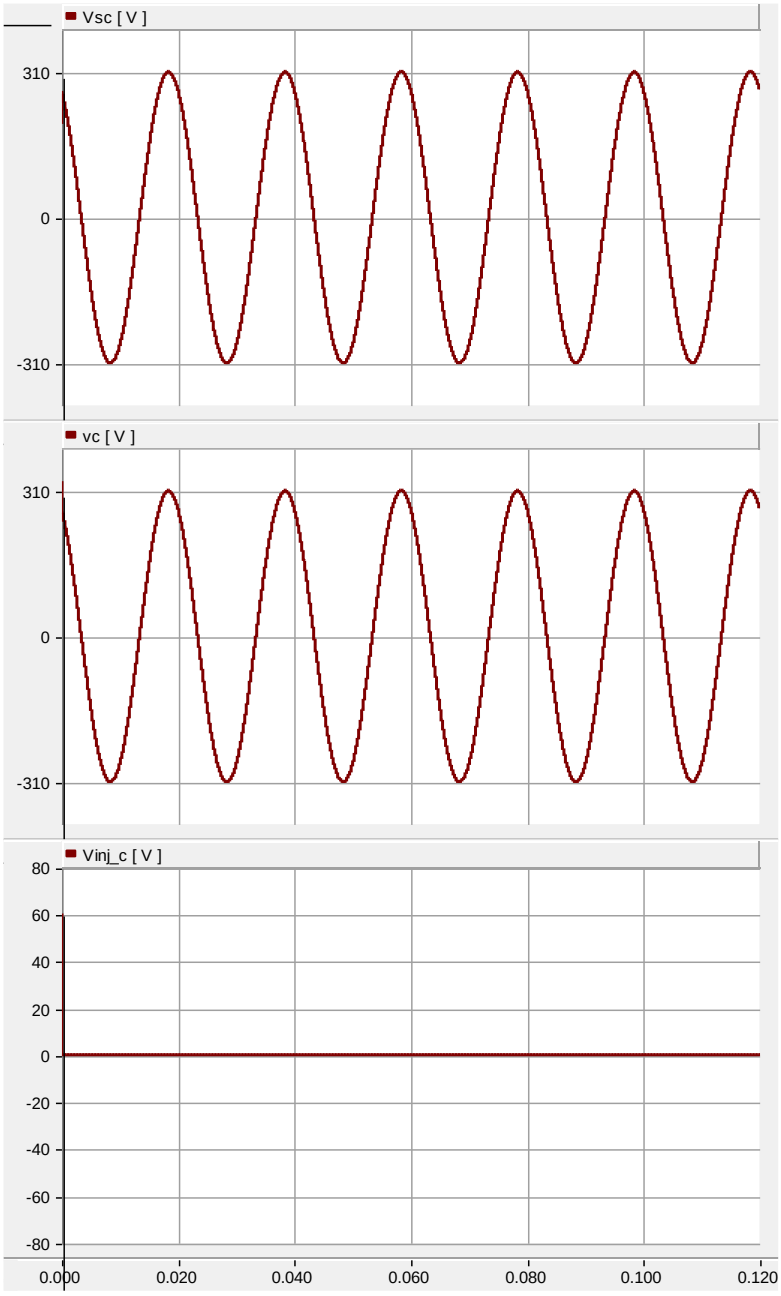
(b)


Vsa [V]
310
0
-310
va [V]
310
0
-310
Vinj_a [V]
80
60
40
20
0
-20
-40
-60
-80
0.000
0.020
0.040
0.060
0.080
0.100
0.120

(c)


Vsb [V]
310
0
-310
vb [V]
310
0
-310
Vinj_b [V]
80
60
40
20
0
-20
-40
-60
-80
0.000
0.020
0.040
0.060
0.080
0.100
0.120

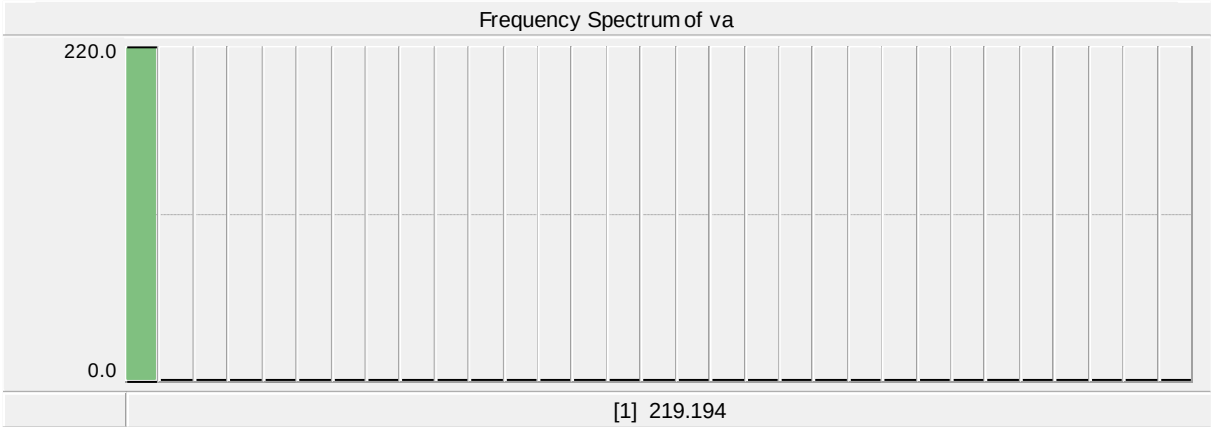
(d)



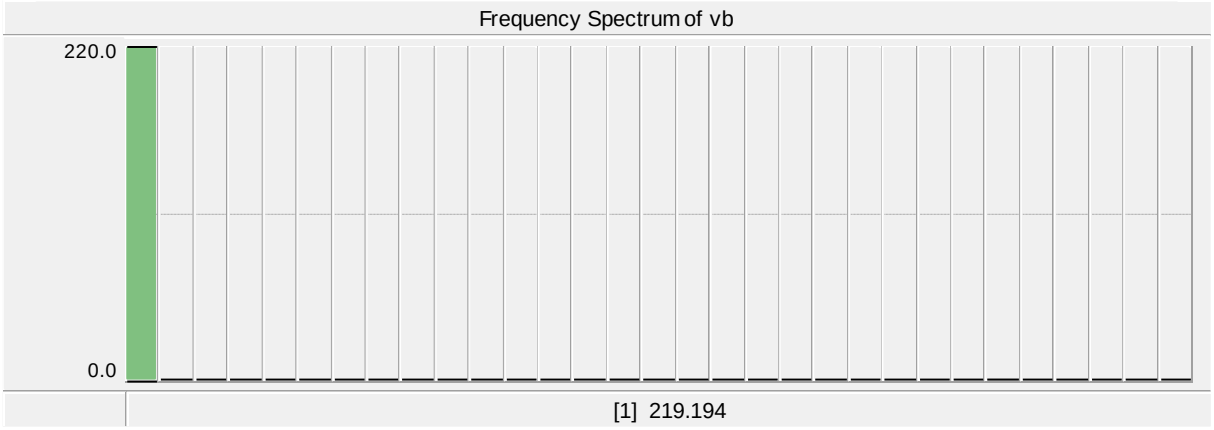
(e)

Figure 5.27: DVR's operation under normal condition: **(a)** input three-phase voltage, **(b)** output three-phase load's voltage, **(c)** waveforms of phase A, **(d)** waveforms of phase B, **(e)** waveforms of phase C

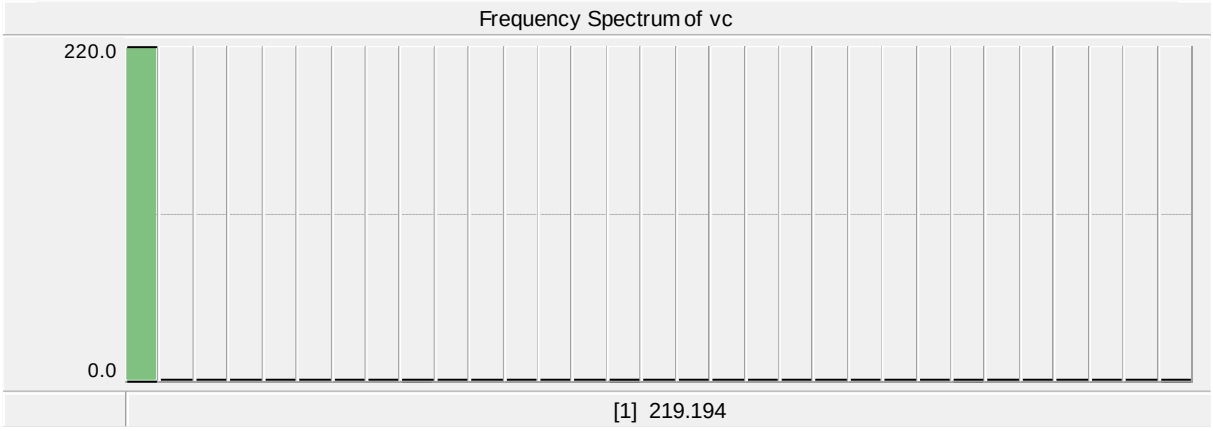
As illustrated by Fig. 5.27, the input and output voltages are the same and the multilevel inverter does not inject any voltages into the phases. To assure that the output voltage is sinusoidal, the harmonic spectrum of v_a is shown in Fig. 5.28.



(a)



(b)



(c)

Figure 5.28: Harmonic spectrum of output three-phase load in normal condition

Considering Fig. 5.28, it is considered that the output voltages have only the first harmonic, which means they are pure sinusoidal waveforms. Moreover, the total harmonic distortion (THD) of v_a, v_b, and v_c are approximately zero, verifies that these waveforms are pure sinusoidal.

Case Study #2: Voltage's Sag-Swell

In this case study, the working principle of DVR is studied under the voltage's sag-swell condition. It is anticipated that under the sag condition, the multilevel inverter injects the rest of the three-phase voltage to keep the output voltage load constant. Moreover, in the swell condition, the multilevel inverter should inject voltage levels with a phase difference of 180^0, to mitigate the load's voltage and fix it on the normal condition's magnitude. In this simulation, the magnitude of the grid's voltage is considered 310 V at the normal condition. During sag and swell conditions occur, these magnitudes change to 250 V and 370 V, respectively. So, the input three-phase voltages depending on the time can be expressed as follows:

$$
\begin{aligned}
v_{Sa} &= 310\sin(100\pi t) \\
v_{Sb} &= 310\sin(100\pi t - 120°) \qquad 0 < t < 0.02 \\
v_{Sc} &= 310\sin(100\pi t - 240°)
\end{aligned}
$$

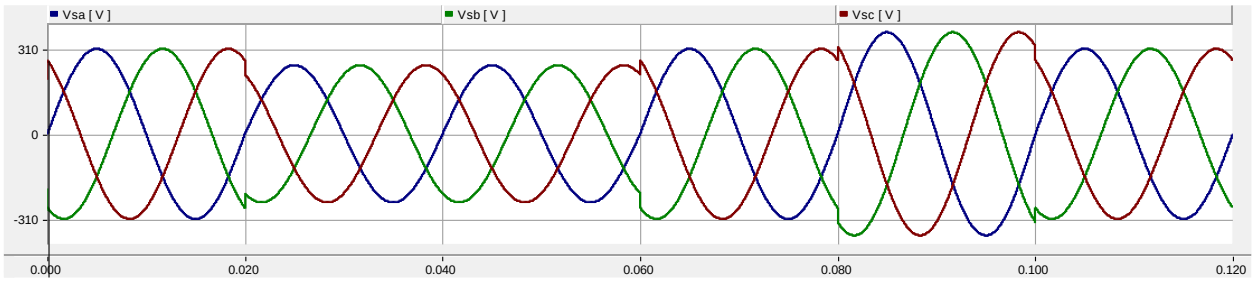
$$
\begin{aligned}
v_{Sa} &= 250\sin(100\pi t) \\
v_{Sb} &= 250\sin(100\pi t - 120°) \qquad 0.02 < t < 0.06 \\
v_{Sc} &= 250\sin(100\pi t - 240°)
\end{aligned}
$$

$$
\begin{aligned}
v_{Sa} &= 310\sin(100\pi t) \\
v_{Sb} &= 310\sin(100\pi t - 120°) \qquad 0.06 < t < 0.08 \\
v_{Sc} &= 310\sin(100\pi t - 240°)
\end{aligned}
\qquad (5.2)
$$

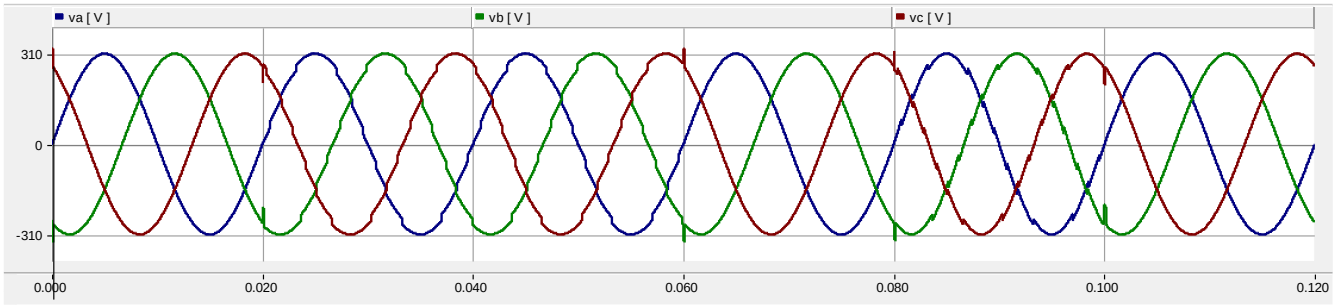
$$
\begin{aligned}
v_{Sa} &= 370\sin(100\pi t) \\
v_{Sb} &= 370\sin(100\pi t - 120°) \qquad 0.08 < t < 0.10 \\
v_{Sc} &= 370\sin(100\pi t - 240°)
\end{aligned}
$$

$$
\begin{aligned}
v_{Sa} &= 310\sin(100\pi t) \\
v_{Sb} &= 310\sin(100\pi t - 120°) \qquad t > 0.10 \\
v_{Sc} &= 310\sin(100\pi t - 240°)
\end{aligned}
$$

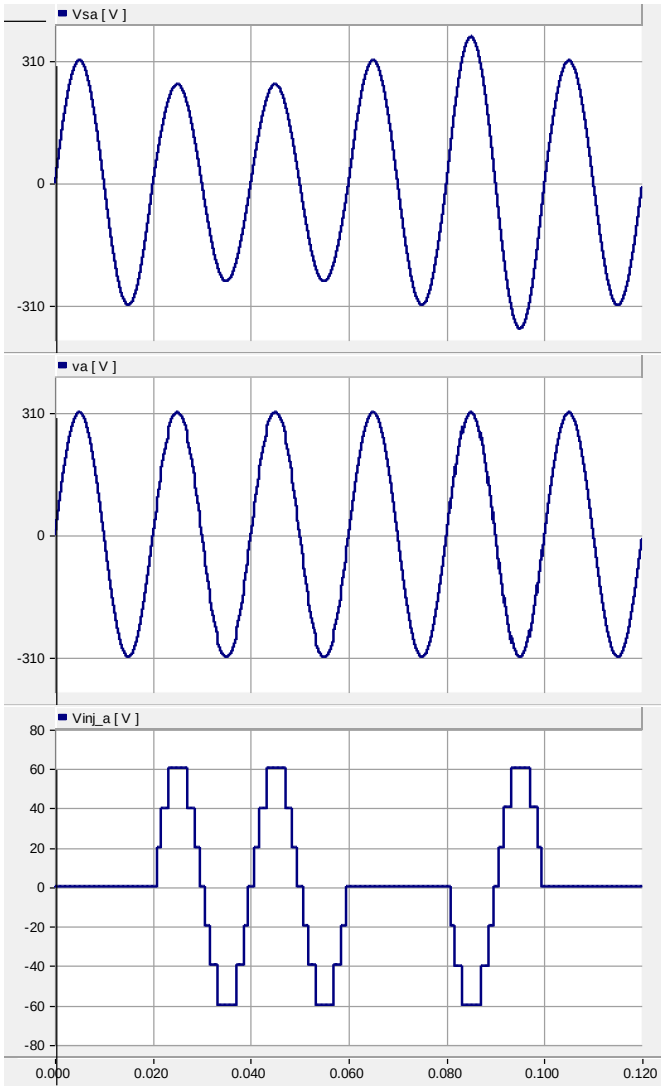
Considering (5.2), Fig. 5.29 shows the operation of DVR under the voltage sag-swell condition.



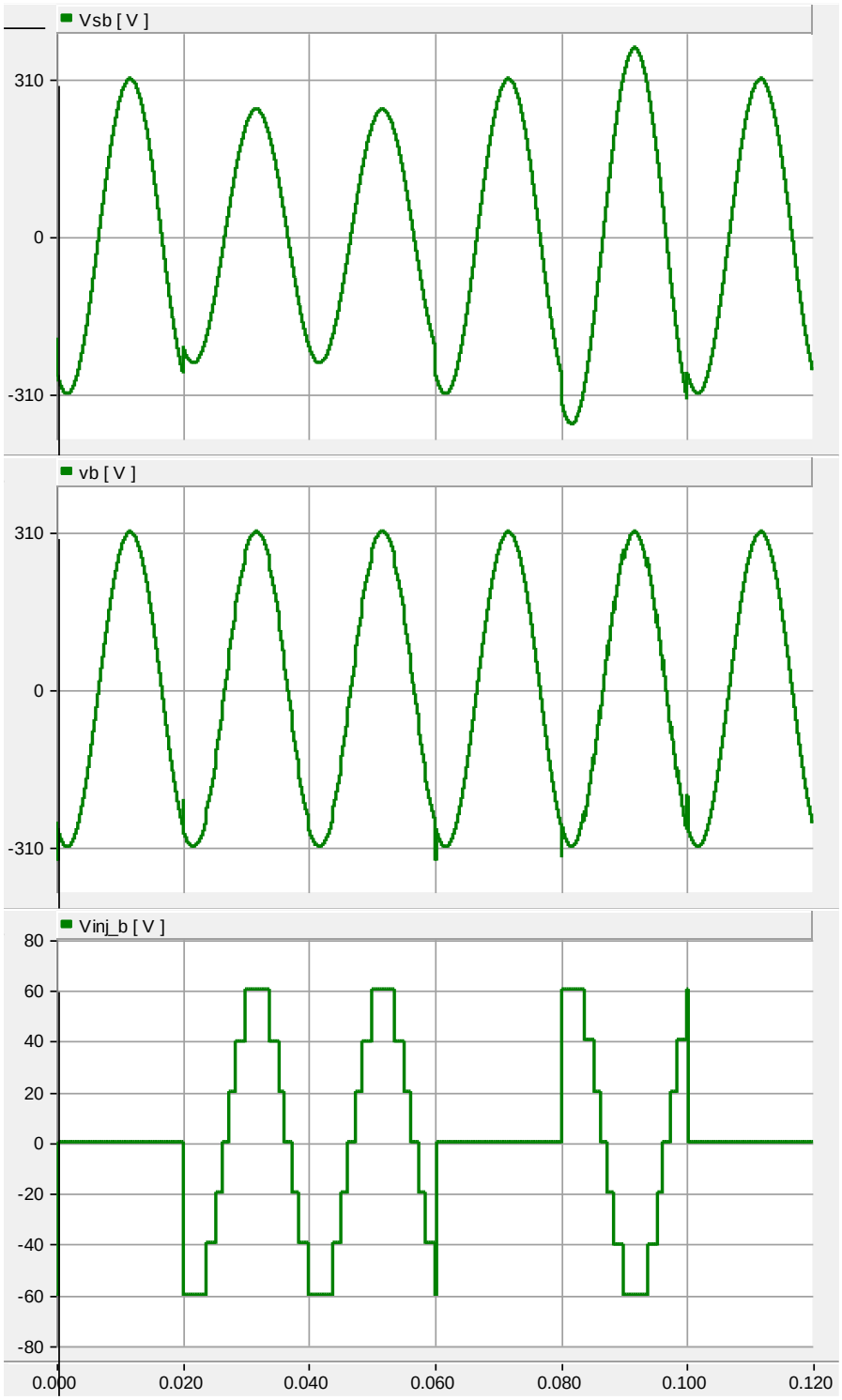
(a)


va [V]
vb [V]
vc [V]
310
0
-310
0.000
0.020
0.040
0.060
0.080
0.100
0.120

(b)


Vsa [V]
310
0
-310
va [V]
310
0
-310
Vinj_a [V]
80
60
40
20
0
-20
-40
-60
-80
0.000
0.020
0.040
0.060
0.080
0.100
0.120

(c)


Vsb [V]
310
0
-310
vb [V]
310
0
-310
Vinj_b [V]
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60
40
20
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-20
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-60
-80
0.000
0.020
0.040
0.060
0.080
0.100
0.120

(d)

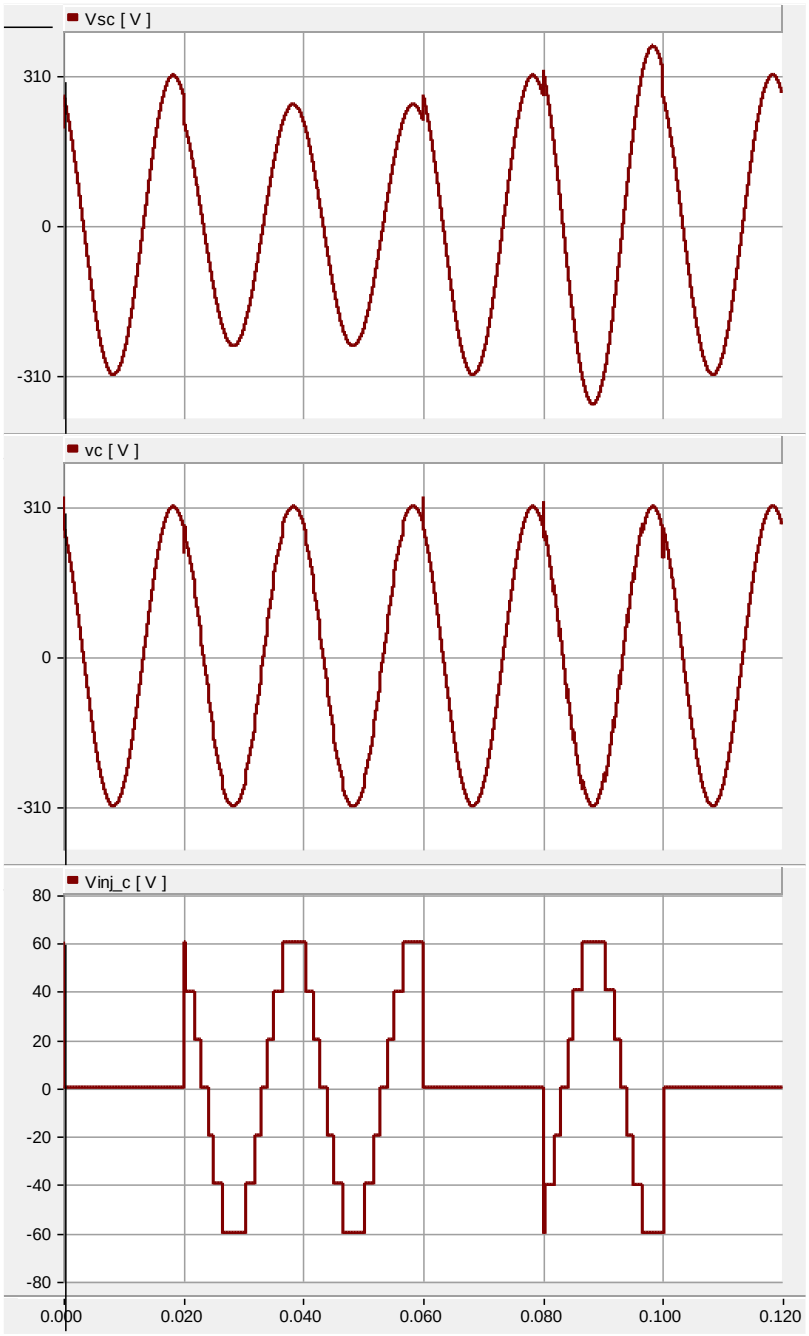
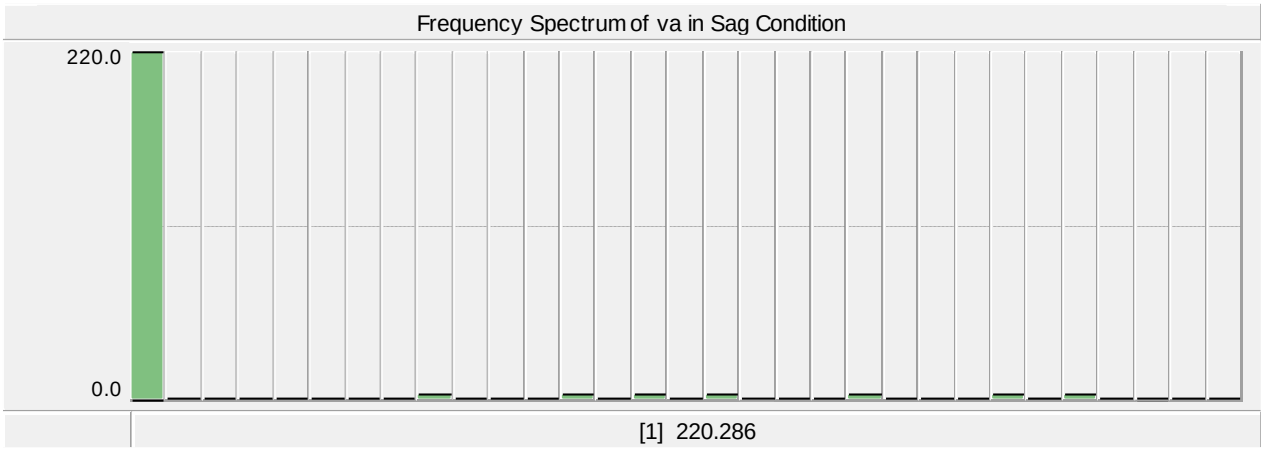


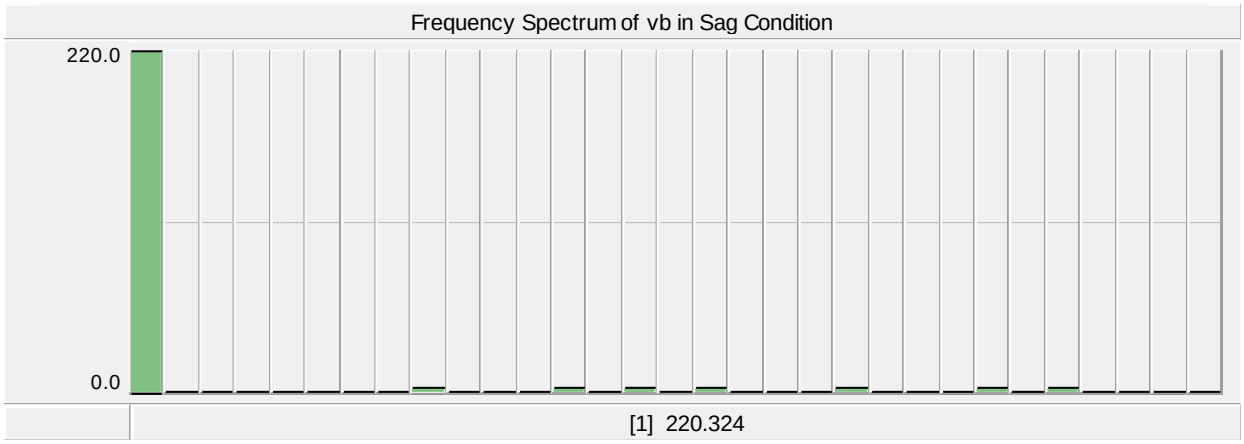
Figure 5.29: DVR's operation under voltage sag-swell condition: (a) input three-phase voltage, (b) output three-phase load's voltage, (c) waveforms of phase A, (d) waveforms of phase B, (e) waveforms of phase C.

As Fig. 5.29 shows, the sag condition occurs in $0.02 < t < 0.06$ where the three-phase input voltage magnitudes are decreased to 250V. In this condition, and the multilevel inverter injects the voltage levels to keep the magnitude of the output voltage in 310V. Moreover, the swell condition occurs in $0.12 < t < 0.18$ where the three-phase input voltages magnitudes are similarly increased to 370V, the multilevel inverter injects voltage levels to fix the output load's voltage's magnitude on 310 V.

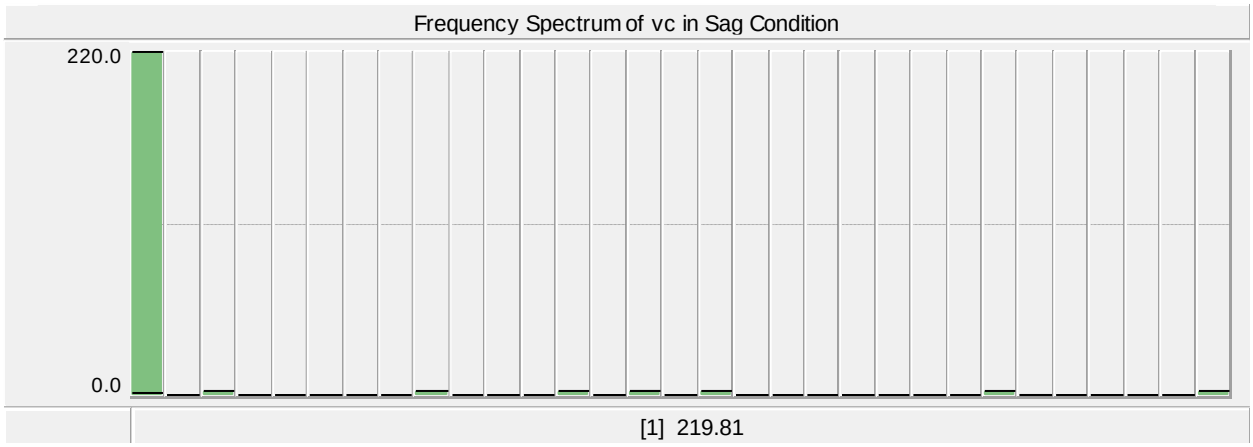
The harmonic spectrum of v_a in the sag and swell conditions are shown in Fig. 5.30. As shown in these figures, v_a is not a pure sinusoidal waveform because of having harmonics because of the limited number of multilevel inverter's voltage levels. Moreover, total harmonic distortion of three-phase load voltages are equal to 2.4% and 2.4% in the sag and swell conditions, respectively.



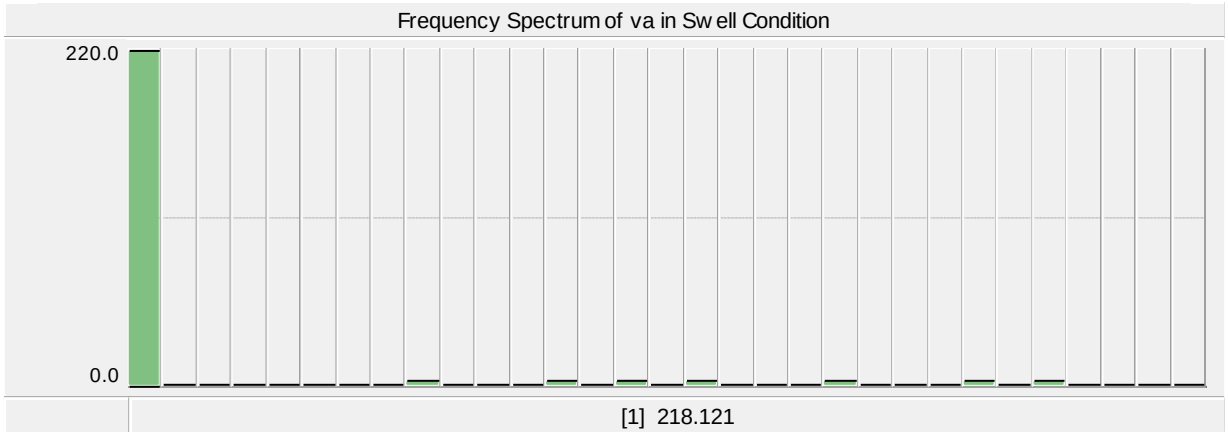
(a)


Frequency Spectrum of vb in Sag Condition
220.0
0.0
[1] 220.324

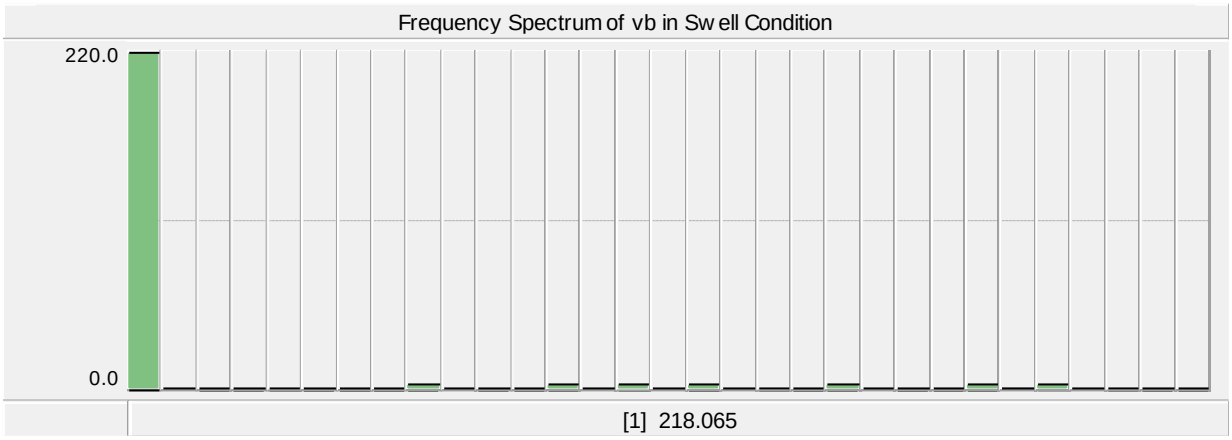
(b)


Frequency Spectrum of vc in Sag Condition
220.0
0.0
[1] 219.81

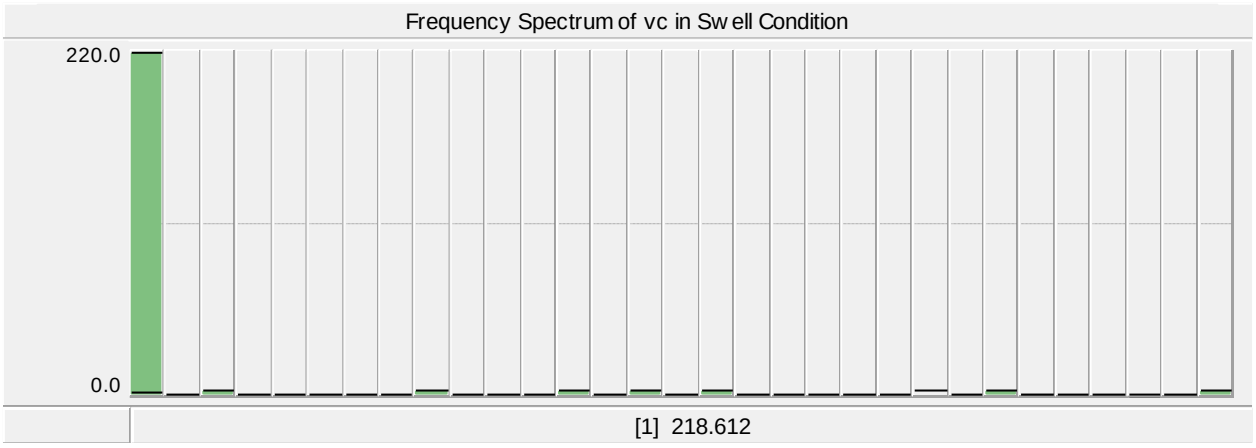
(c)


Frequency Spectrum of va in Swell Condition
220.0
0.0
[1] 218.121

(d)



(e)



(f)

Figure 5.30: Harmonic spectrum of output three-phase load in voltage sag-swell condition

Case Study #3: Voltage Distortion

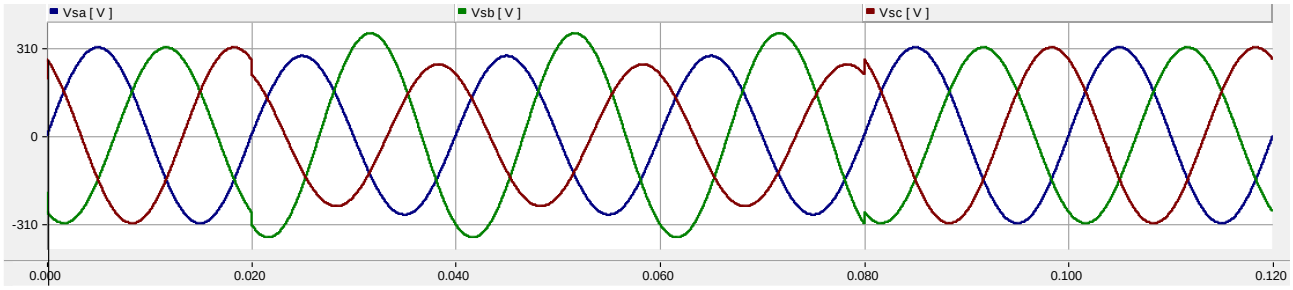
In this case study, the operation of DVR is analyzed under distorted three-phase input voltage. To simulate this condition, the input voltage load is selected from:

$$
\begin{aligned}
v_{Sa} &= 310\sin(100\pi t) \\
v_{Sb} &= 310\sin(100\pi t - 120°) \qquad 0 < t < 0.02 \\
v_{Sc} &= 310\sin(100\pi t - 240°)
\end{aligned}
$$

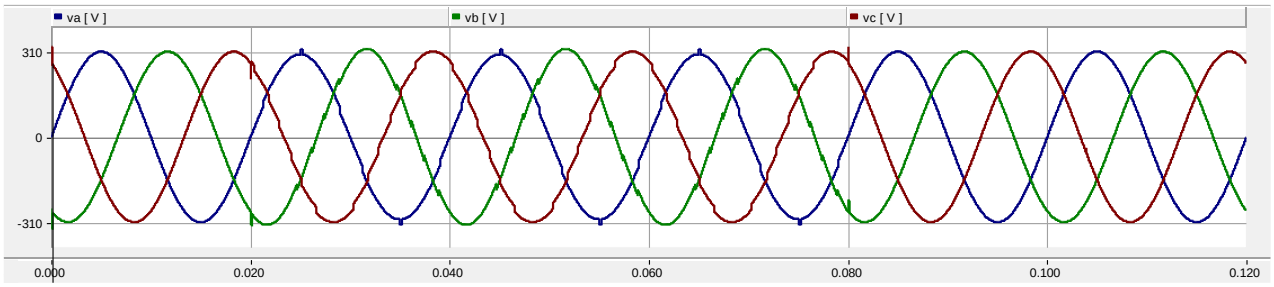
$$
\begin{aligned}
v_{Sa} &= 280\sin(100\pi t) \\
v_{Sb} &= 360\sin(100\pi t - 120°) \qquad 0.02 < t < 0.08 \\
v_{Sc} &= 250\sin(100\pi t - 240°)
\end{aligned}
\tag{5.3}
$$

$$
\begin{aligned}
v_{Sa} &= 310\sin(100\pi t) \\
v_{Sb} &= 310\sin(100\pi t - 120°) \qquad t > 0.08 \\
v_{Sc} &= 310\sin(100\pi t - 240°)
\end{aligned}
$$

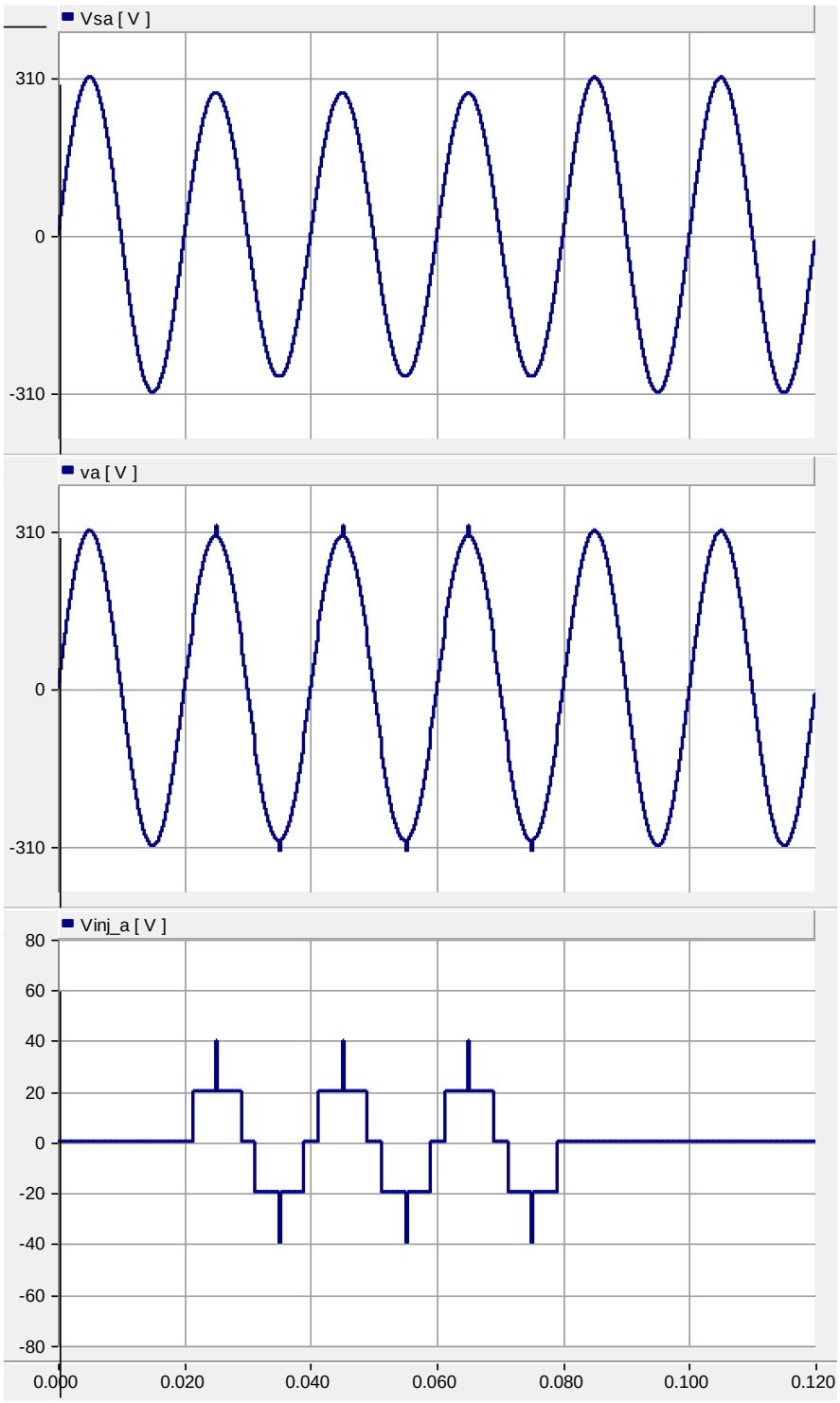
Fig. 5.31 shows the operation of DVR under the unbalanced input voltage condition.



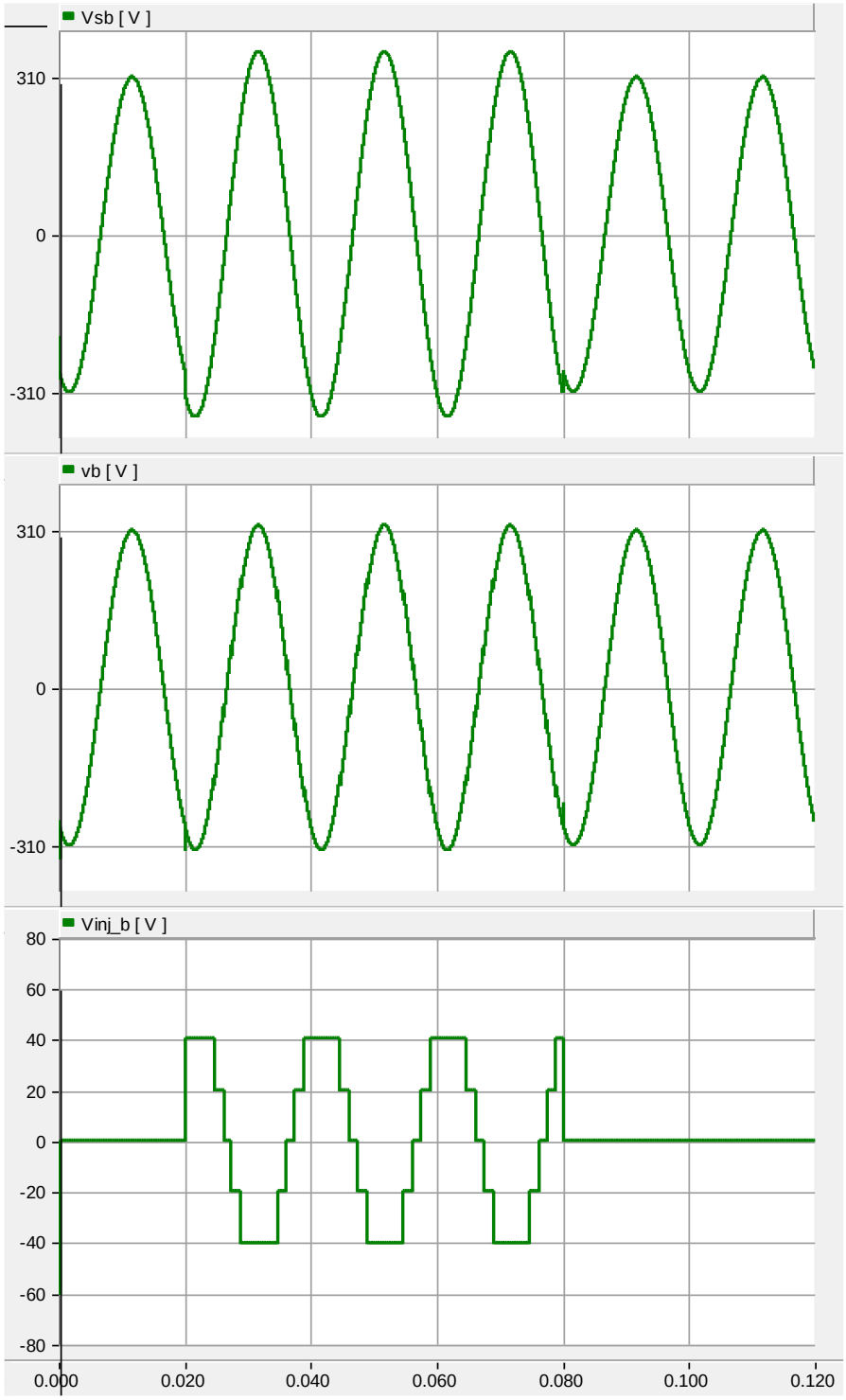
(a)



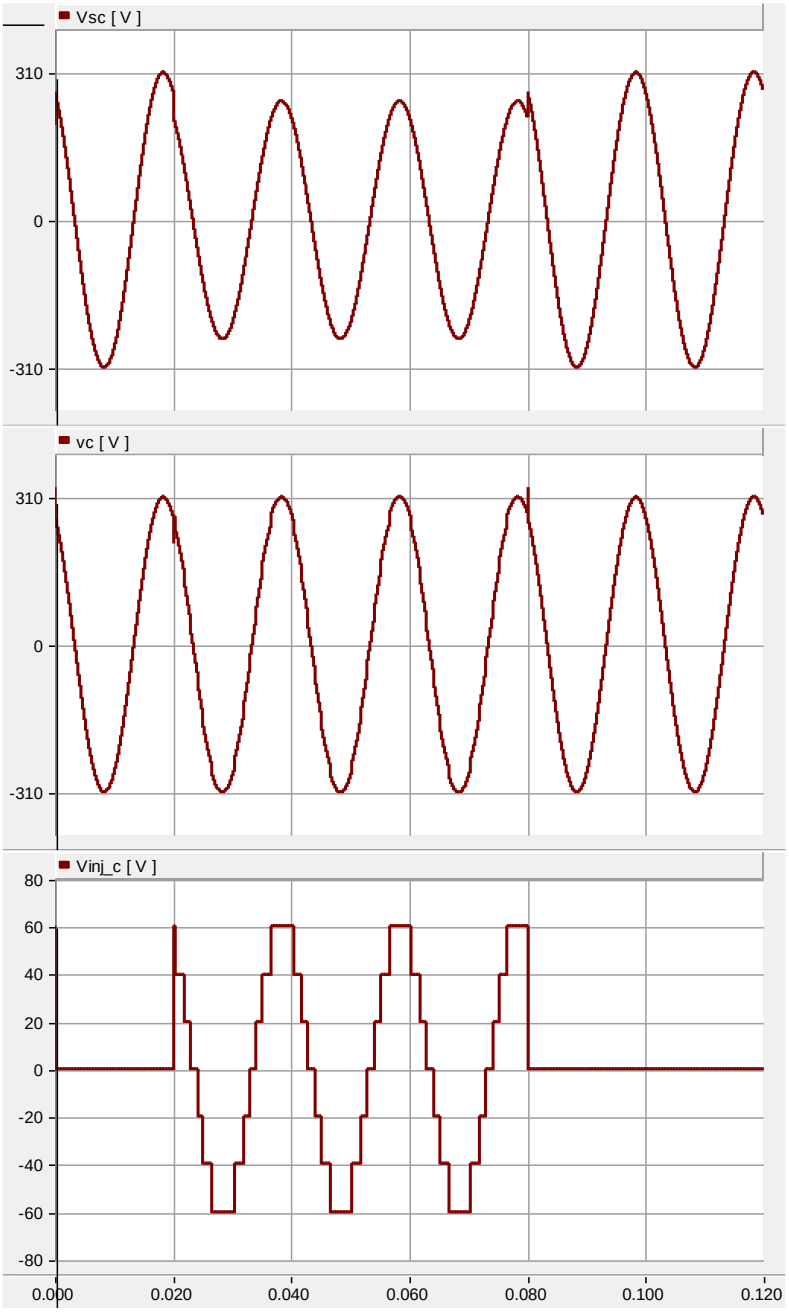
(b)


Vsa [V]
310
0
-310
va [V]
310
0
-310
Vinj_a [V]
80
60
40
20
0
-20
-40
-60
-80
0.000
0.020
0.040
0.060
0.080
0.100
0.120

(c)


Vsb [V]
310
0
-310
vb [V]
310
0
-310
Vinj_b [V]
80
60
40
20
0
-20
-40
-60
-80
0.000
0.020
0.040
0.060
0.080
0.100
0.120

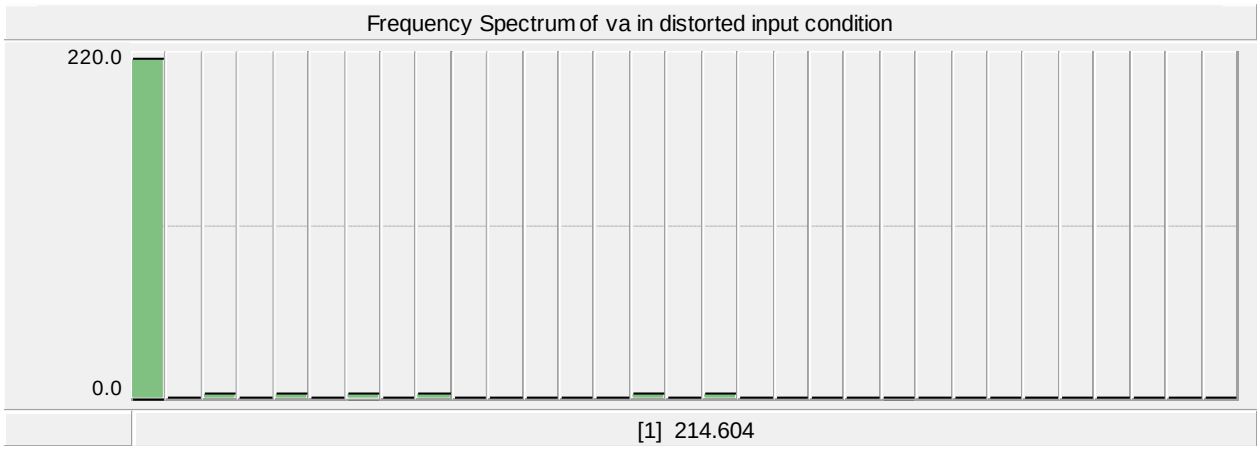
(d)



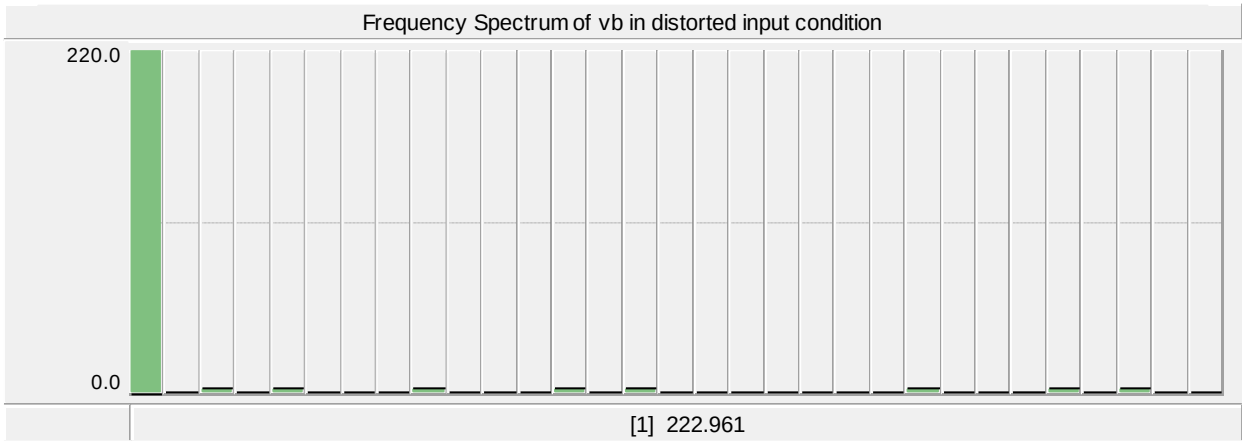
(e)

Figure 5.31: DVR's operation under distorted three-phase input voltage: (a) input three-phase voltage, (b) output three-phase load's voltage, (c) waveforms of phase A, (d) waveforms of phase B, (e) waveforms of phase C.

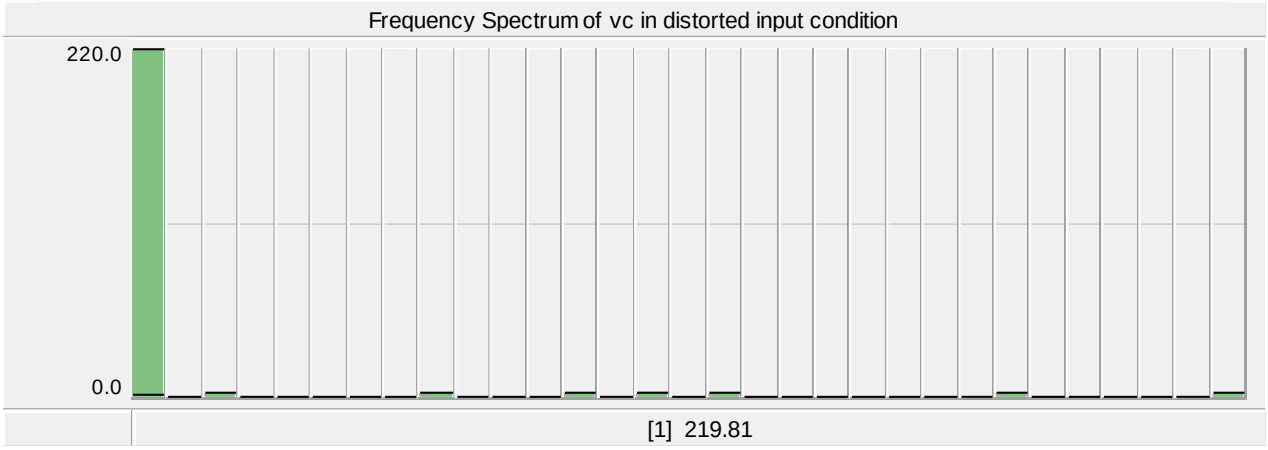
Fig. 5.31 shows that the multilevel inverter injects the appropriate voltage levels to keep the output voltages' magnitudes in 310V. In other words, each phase has its own injected voltage which is used to compensate for the input voltages' unbalancing. To study the performance of DVR under the unbalanced input voltages condition, the harmonic spectrums of the different phases' output voltages are shown in Fig. 5.32.



(a)



(b)



(c)

Figure 5.32: Harmonic spectrum of output three-phase load in unbalanced input voltage condition.

From Fig. 5.32 it is seen that the three-phase loads' voltages are not pure sinusoidal waveforms because they contain other harmonics. Considering the multilevel inverter, it can be inferred that this matter relates to the limited number of multilevel inverter's output voltage levels. Moreover, THD of v_a, v_b and v_c are equal to 2.37%, 2.33%, and 2.44%, which verifies that these waveforms contain harmonics.

Case Study #4: Third Harmonic Injection

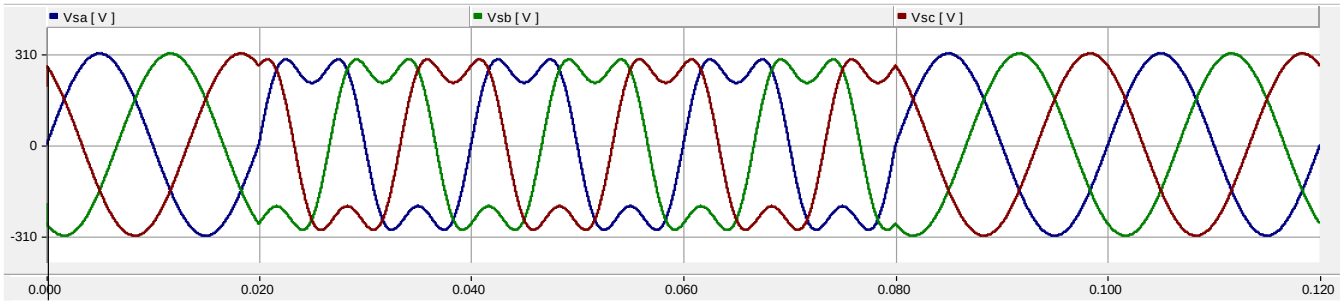
In this case study, the three-phase input voltages are adjusted as follows to simulate the third harmonic injection condition:

$$\begin{aligned} v_{Sa} &= 310\sin(100\pi t) \\ v_{Sb} &= 310\sin(100\pi t - 120°) \qquad 0 < t < 0.02 \\ v_{Sc} &= 310\sin(100\pi t - 240°) \end{aligned} \tag{5.4}$$

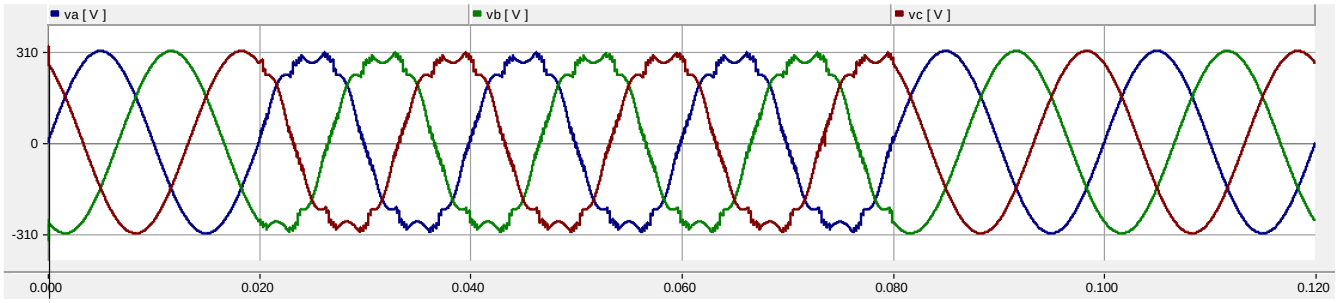
$$
\begin{aligned}
v_{Sa} &= 310\sin(100\pi t) + 100\sin(300\pi t) \\
v_{Sb} &= 310\sin(100\pi t - 120°) + 100\sin(300\pi t) \qquad 0.02 < t < 0.08 \\
v_{Sc} &= 310\sin(100\pi t - 240°) + 100\sin(300\pi t)
\end{aligned} \tag{5.5}
$$

$$
\begin{aligned}
v_{Sa} &= 310\sin(100\pi t) \\
v_{Sb} &= 310\sin(100\pi t - 120°) \qquad t > 0.08 \\
v_{Sc} &= 310\sin(100\pi t - 240°)
\end{aligned}
$$

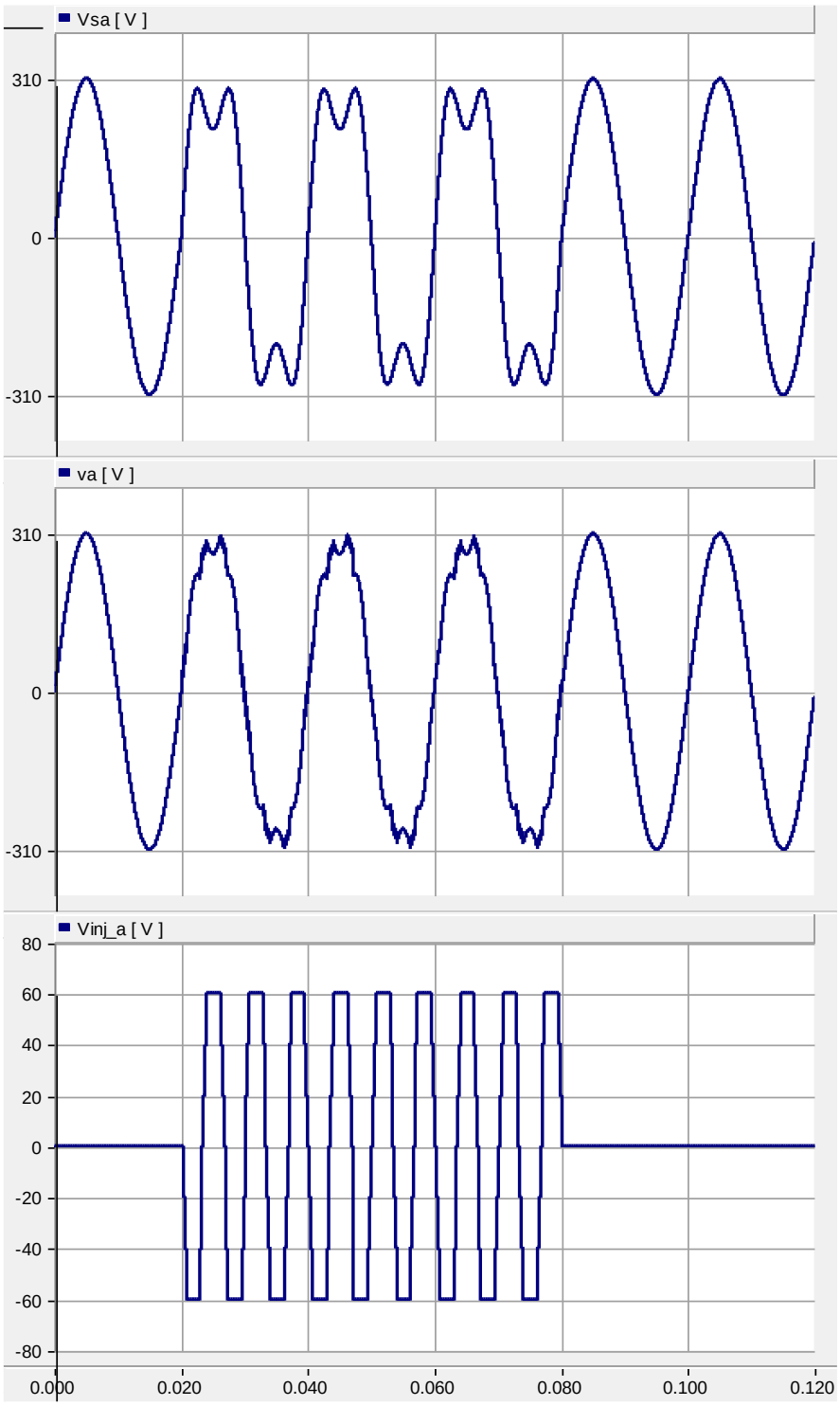
By having (5.4) and (5.5), the operation of DVR is demonstrated in Fig. 5.33.



(a)



(b)


Vsa [V]
310
0
-310
va [V]
310
0
-310
Vinj_a [V]
80
60
40
20
0
-20
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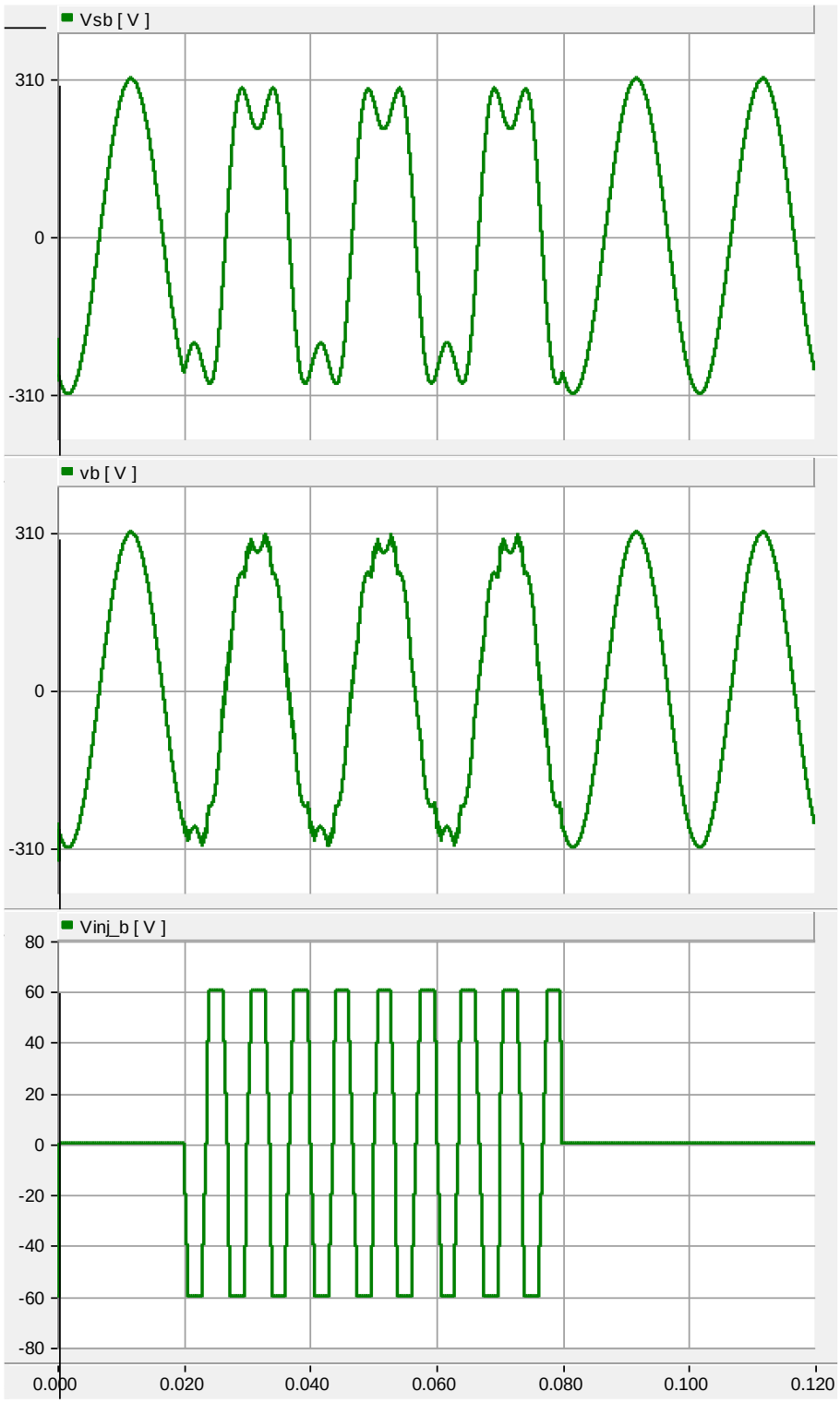
-60
-80
0.000
0.020
0.040
0.060
0.080
0.100
0.120

(c)


Vsb [V]
310
0
-310
vb [V]
310
0
-310
Vinj_b [V]
80
60
40
20
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-60
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0.000
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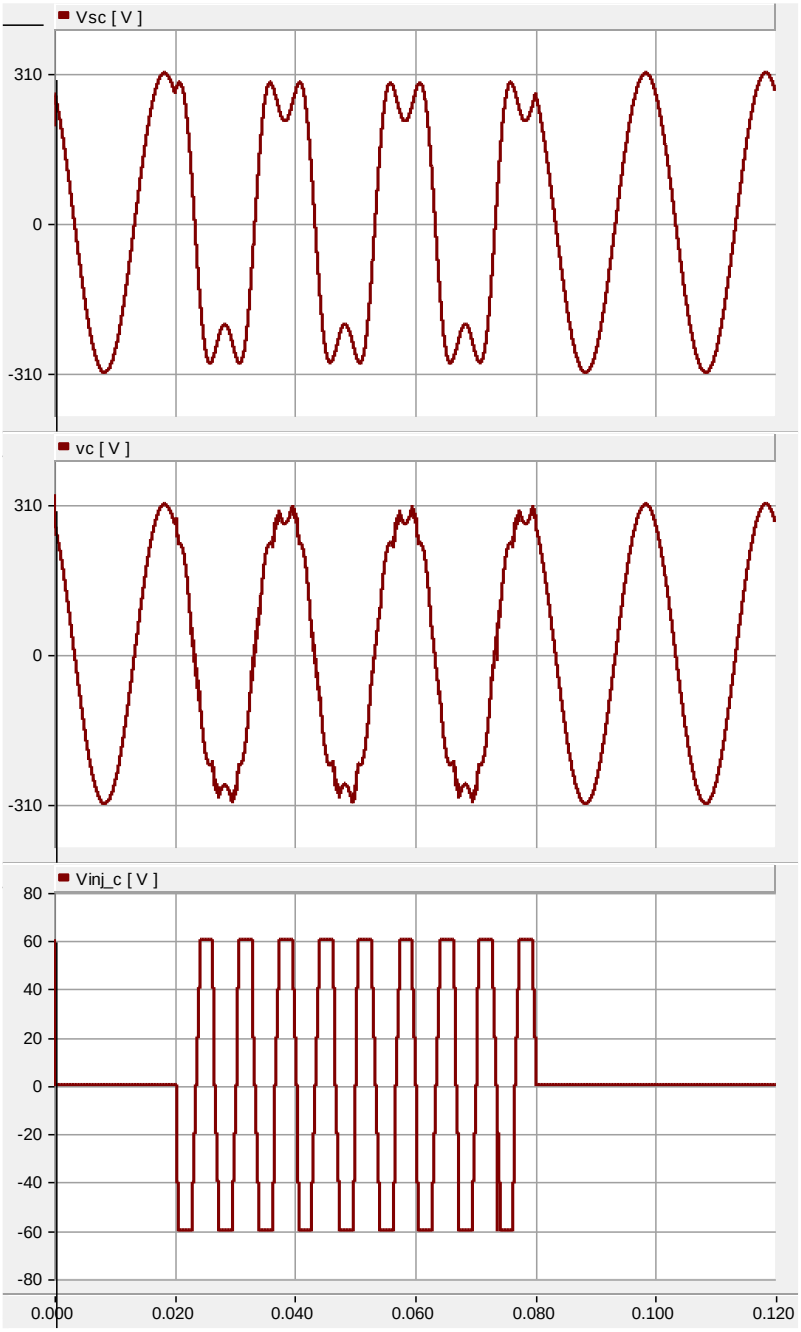
0.080
0.100
0.120

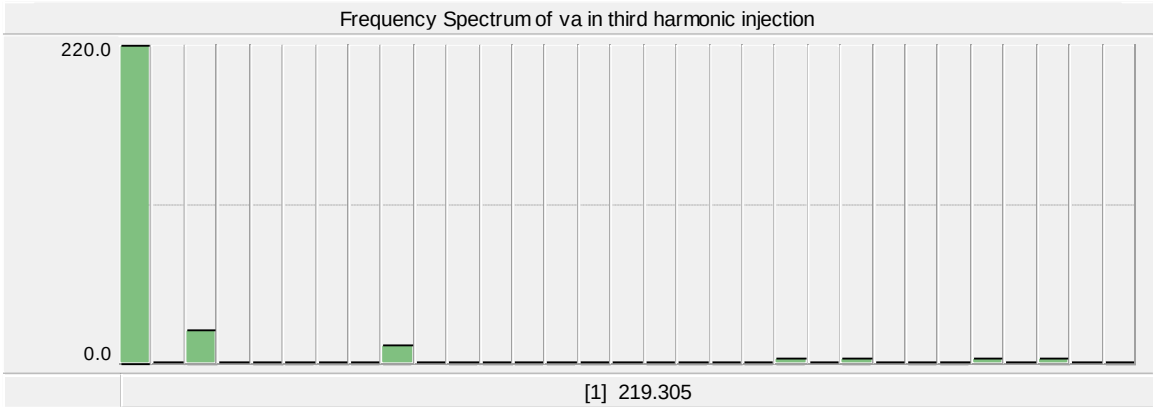
(d)



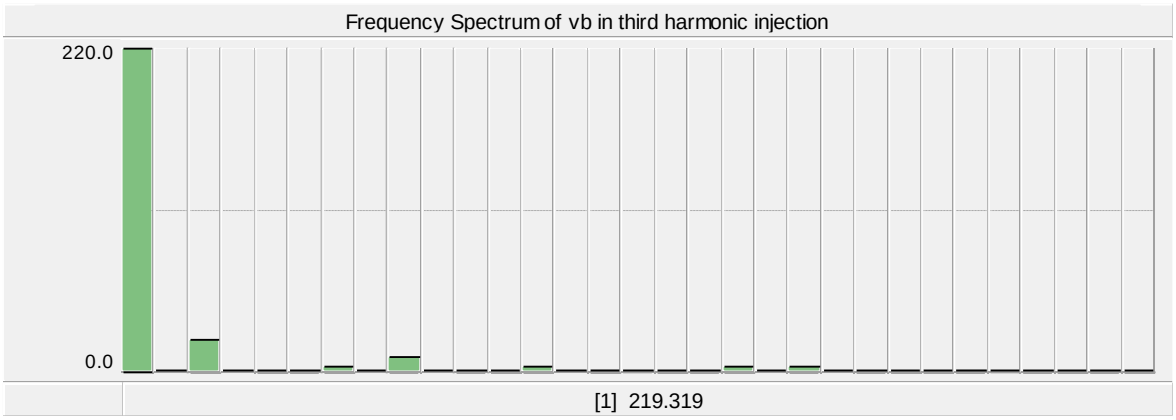
(e)

Figure 5.33: DVR's operation under third harmonic injection: (a) input three-phase voltage, (b) output three-phase load's voltage, (c) waveforms of phase a, (d) waveforms of phase b, (e) waveforms of phase c

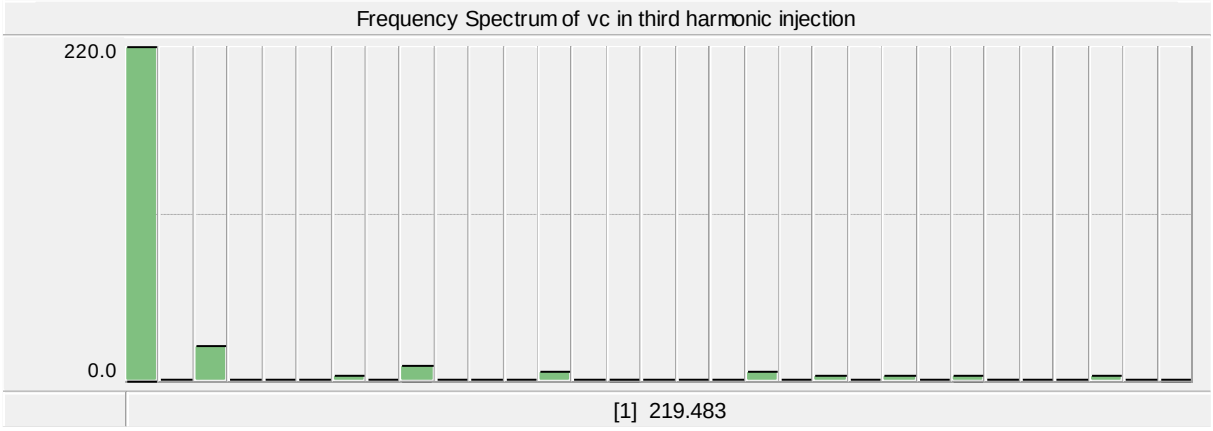
As Fig. 5.33 shows, DVR injects the additional voltage levels to compensate for the dispute between the input voltage in the normal and third harmonic injected conditions. These voltage levels make the magnitudes of v_a, v_b and v_c to be approximately 310V, equal to the normal condition's magnitude. However, considering the third-harmonic injected waveform, it is evident that the obtained voltage on the load does not have a near-sinusoidal shape. This issue is addressed in Fig. 5.34 using the harmonic spectrum of the output voltage waveforms. Considering Fig. 5.34, it is seen that the amplitudes of the other harmonics are relatively high compared to the previous studies. So, the output voltage waveforms are obtained from the sum of several sinusoidal waveforms. Moreover, output voltage waveforms' THD are equal to 11% which shows that these waveforms have several harmonics in their spectrum.



(a)



(b)



(c)

Figure 5.34: Harmonic spectrum of output three-phase load in third harmonic injection case

5.8 Conclusion

Simulation and experimental analysis of the proposed three-phase MLI based DVR topology have been provided in this section of the research. Output waveforms of phase voltages, currents and line-to-line voltages for experimental prototype and simulation models using same parameter values are equivalent in magnitude and shape. The quality of these waveforms are of high characteristic quality. Inverter efficiency was determined with varying input and output voltages; the efficiency graph of varying load values was also produced. Lastly, voltage compensations for sag and swell conditions using the proposed DVR topology was simulated and output waveforms generated. The DVR output waveforms are generated for multiple sag and swell conditions and also different load voltage magnitudes. Limitation of the proposed three-phase multilevel inverter based DVR was investigated.

CHAPTER 6

CONCLUSION

This work proposes an improved three-phase multilevel inverter developed from the conventional single-phase H-bridge. Two semiconductor power switches and one dc voltage source is added to the H-bridge architecture to obtain single-phase unit of the proposed MLI topology. Using extension technique, the proposed three-phase multilevel inverter is derived. This technique minimizes the dc voltage source count from six to four compared to three single-phase unit based three-phase MLI. Two topologies of the proposed three-phase MLI are presented, the first topology has three autonomous loads whiles the second topology is made up of Y connected three-phase loads. Three single-phase transformers in the second topology provides galvanic isolation between the inverter and load. The galvanic isolation feature of the second topology makes it suitable for application in dynamic voltage restorer (DVR). Therefore, the proposed three-phase multilevel inverter was applied in DVR for voltage compensation during voltage sag and voltage swell disturbances.

The proposed three-phase multilevel inverter is composed of less component count; four dc sources, eighteen driver circuit and eighteen semiconductor switches constitutes total component count in the first proposed topology. Three single-phase transformers are added to the first proposed topology to derive the total component count in the second proposed topology. The proposed three-phase multilevel inverter is simple to control using fundamental frequency control technique and less complex structurally. Also, the absence of capacitor voltage balancing in the proposed topology makes simple to control. Fundamental frequency control technique provides minimum switching losses compared some PWM (pulse-width) modulation technique. Each single-phase generates 7-levels output voltage and 13-levels line voltage is generated by the proposed three-phase multilevel inverter. Comparative investigation of proposed topology and recently published three-phase multilevel inverters shows superior features of the proposed topology in less component quantity such as dc voltage count, output voltage level count and driver circuit count. Also, lower voltage rated semiconductor switches are employed in the proposed three-phase multilevel inverter.

Simulation and experimental analysis of the proposed three-phase MLI and DVR topology were provided. Output waveforms of phase voltages, currents and line to line voltages between experimental prototype and simulation models using same parameter values are equivalent in magnitude and shape. The quality of these waveforms are of high quality. Inverter efficiency was determined with varying load resistance. Lastly, compensation of voltage sag and swell conditions using the proposed three-phase multilevel based DVR topology was simulated and output waveforms generated, various compensations were performed for varying sag and swell conditions. Better functionality was exhibited by the proposed DVR when it was tested under various fault conditions. Two main limitation of the proposed DVR was discovered during my research; output voltage magnitudes of the MLI and magnitude of the compensating voltage of the DVR.

FUTUR WORK

There are a few ideas, experimental investigations and limitations of my research that have been postponed to the future due to time constraints and unbearable challenges due to COVID 19. The aim of this thesis is a proposed three-phase MLI in conjunction with a DVR topology for the compensation of voltage during sag and swell conditions in distribution lines. Based on the derived results, observations and suggestion from jury members, investigating the following ideas will further academic knowledge in these areas:

1. Compensation range and capabilities of multilevel inverter based dynamic voltage restorers. Two factors are of outermost importance to me here i.e. the magnitude of the stepped inverter output voltage and the compensation duration of the dc source.
2. Design of a new MLI with output voltage levels greater than 31.
3. Experimental analysis of my DVR topology.

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APPENDICES

APPENDIX 1

IMPLEMENTATION OF PROPOSED MLI IN PSCAD SOFTWARE

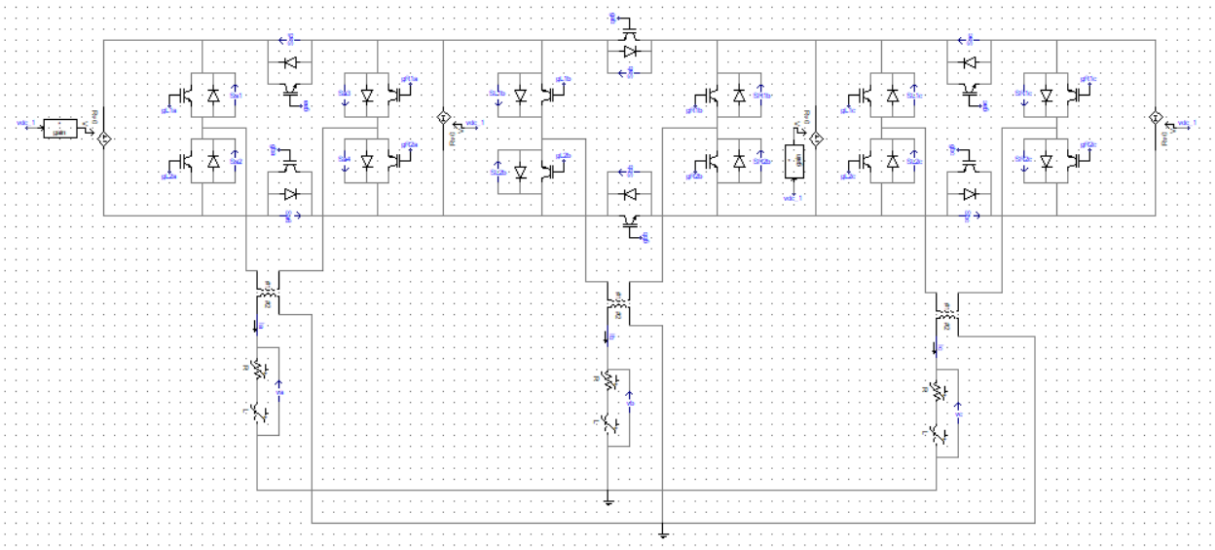

Fig. 1. Proposed three-phase multilevel inverter power circuit in PSCAD software

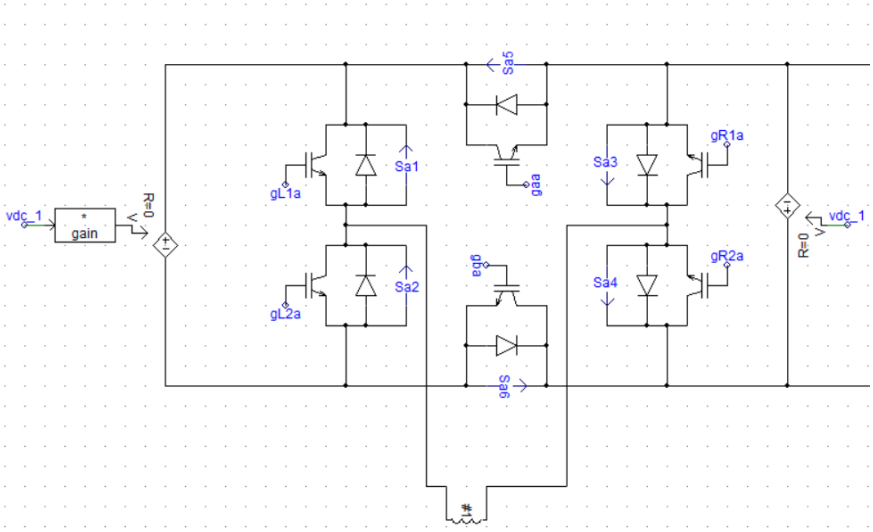

Fig. 12. Phase A of proposed three-phase multilevel inverter power circuit in PSCAD software

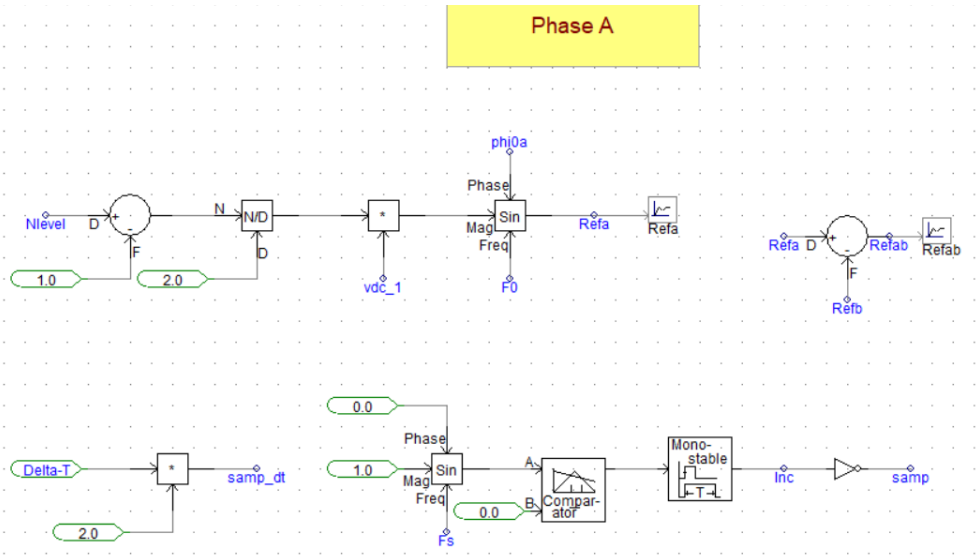

Fig. 13. Phase FFCM implementation in PSCAD

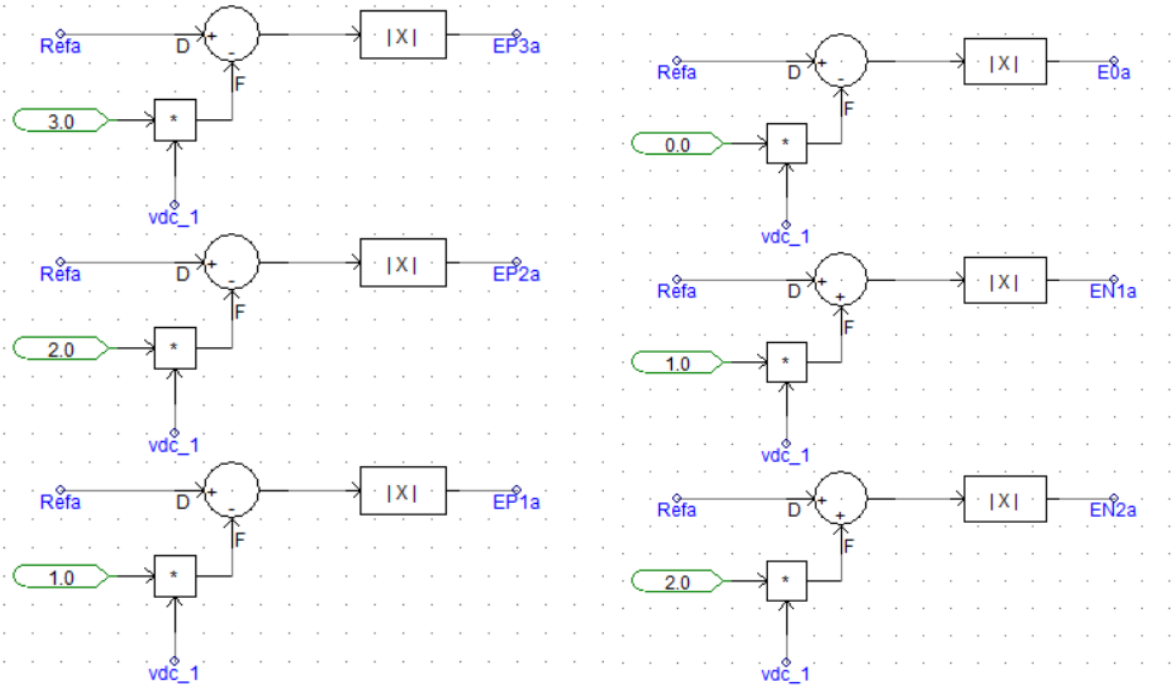

Fig. 14. Phase A FFCM implementation in PSCAD

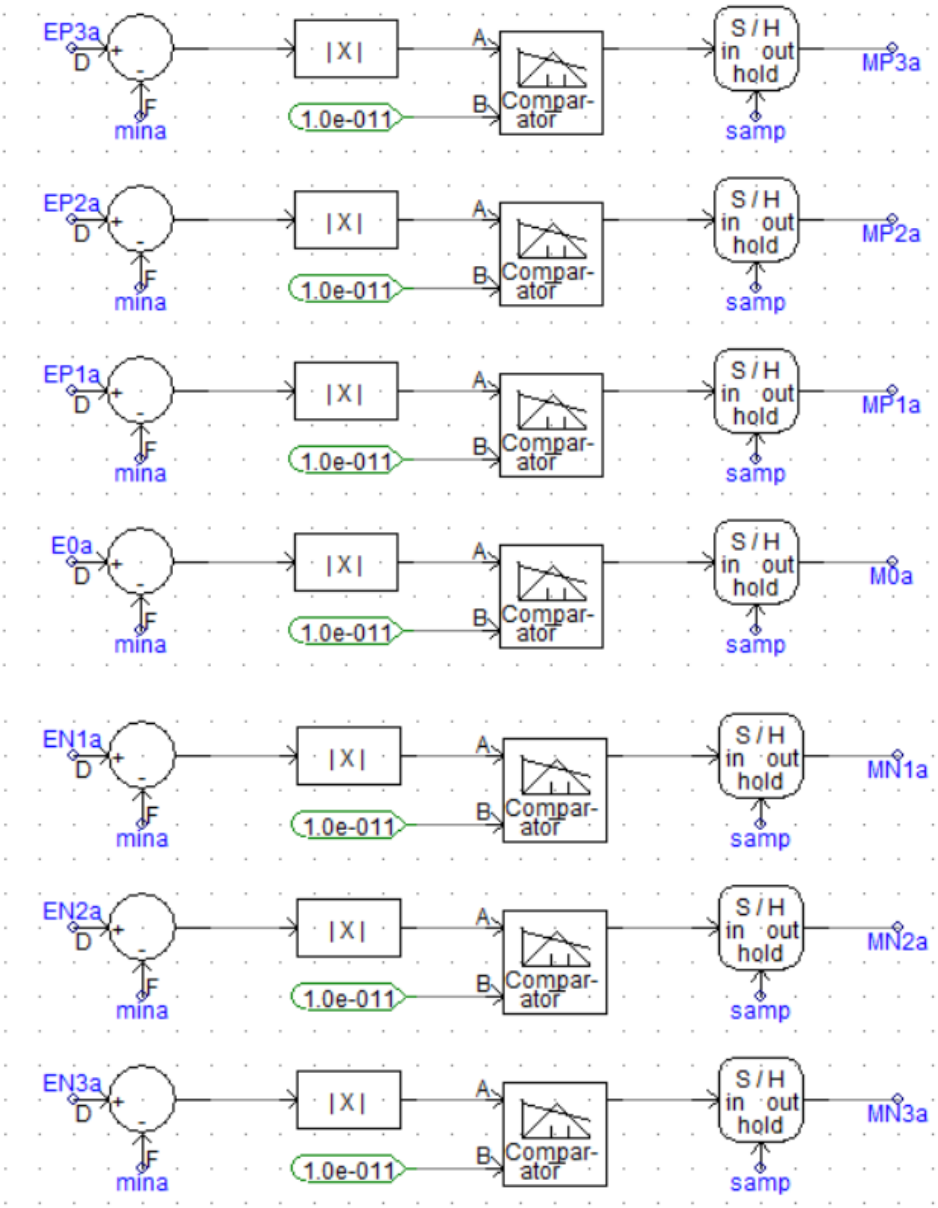

Fig. 15. Gate signal command generation

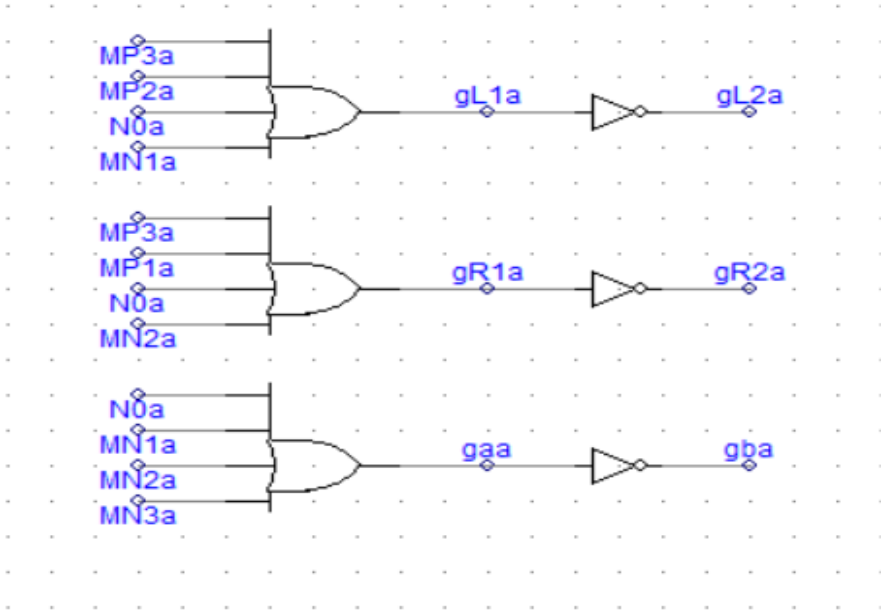

Fig. 16. Gate commands for switches

APPENDIX 2

IMPLEMENTATION OF PROPOSED MLI DVR IN PSCAD SOFTWARE

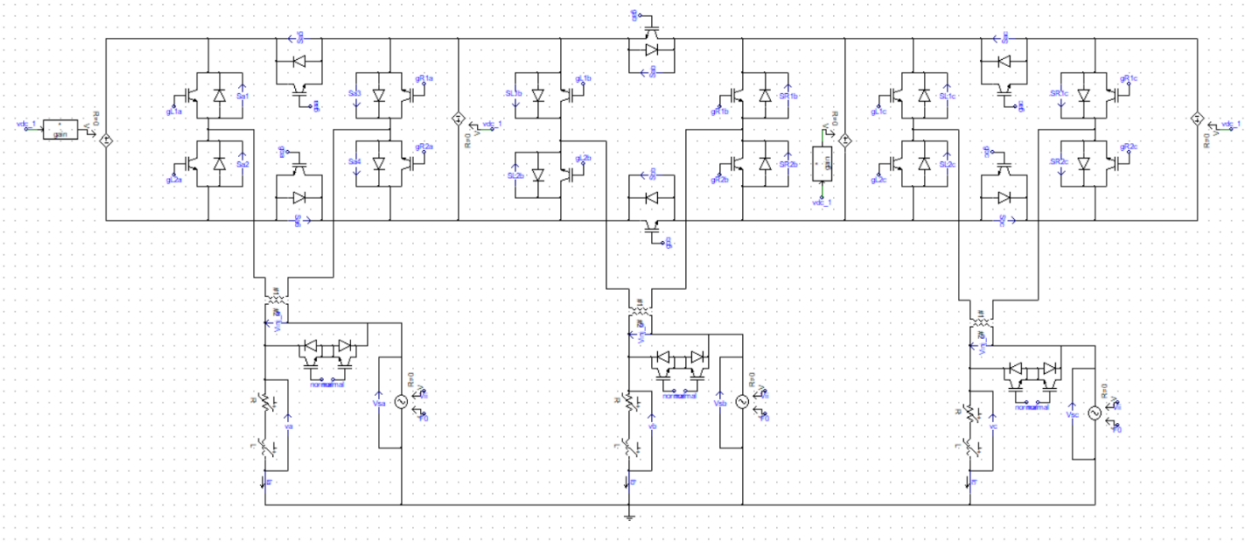

Fig. 21. PSCAD implementation of proposed MLI based DVR

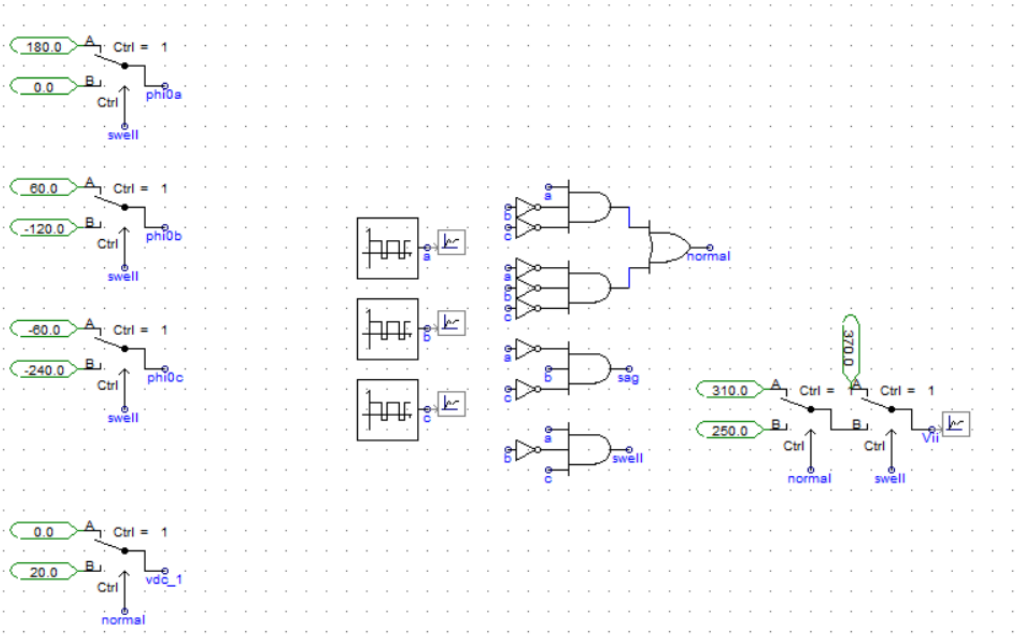

Fig. 20. DVR control strategy

APPENDIX 3
COMPARISON BASED REFERENCES

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APPENDIX 4

CURRICULUM VITEA

PERSONAL INFORMATION

Surname, Name: Tackie, Samuel Nii

Nationality: Ghana

Date and Place of Birth: 27th March 1988, Accra

EDUCATION

Degree	Institution	Year of Graduation
M.Sc. Electrical Engineering	Near East University, Electrical Engineering Department	2015
B.Sc. Electrical Engineering	Ho Technical University, Electrical Engineering Department	2007

WORK EXPERIENCE

Year	Place	Enrolment
Sept, 2015 – Present	NEU, Electrical Engineering Dept.	Lecturer
Sept, 2013 – Aug, 2015	NEU, Electrical Engineering Dept.	Research Assistant
Sept, 2010 – Feb, 2013	Tsito Senior High and Technical	Teacher
Sept, 2008 – Aug, 2010	ST. Proper's College	Teacher
Sept, 2007 – Aug, 2008	Keta Senior High	National Service

FOREIGN LANGUAGES

English, fluently spoken and written

MEMBERSHIP OF PROFESSIONAL ORGANISATION

Student member, Institute of Electrical and Electronics Engineers (IEEE)

PUBLICATIONS

Tackie, S.N.; Babaei, E. Modified Topology for Three-Phase Multilevel Inverters Based on a Developed H-Bridge Inverter. *Electronics* 2020, 9, 1848. doi.org/10.3390/electronics9111848

Tackie, S.N, Dimililer, K. Turjman, F. A. (2020). Wireless sensor devices in medical application: an overview. In F. A. Turjman (Ed.). Wireless medical sensor for IoT-based eHealth. *IET Digital Library*. doi:10.1049/PBHE026E, e-ISBN: 9781839530579.

Oyebade K. Oyedotun, Sam Nii Tackie, Ebenezer O. Olaniyi, Adnan Khashman, "Data Mining of Students' Performance: Turkish Students as a Case Study" *International Journal of Intelligent Systems and Applications(IJISA), IJISA* Vol. 7, No. 9, August 2015

Ozgur Cemal Ozerdem, Samuel Nii Tackie, Samet Biricik, "Performance evaluation of Serhatkoy PV (1.2MW) Power Plant", In *International Conference on Electrical and Electronics Engineering, ELECO* 2015" Bursa, Turkey. Published by IEEE

Samuel N. Tackie, ''Renewable Energy Sources in Ghana'' *International Conference on Energy, Environment and Economics (ICEEE2016),* Edinburgh Conference Centre, Heriot-Watt University, Riccarton, Edinburgh, EH14 4AS.

Tackie, S.N.; Babaei, E. "New Cascaded Asymmetrical Multilevel Inverter with Minimum Component Count"

Status: Pending Acceptance

Samuel Nii Tackie, Ozgur Cemal Ozerdem, “Photovoltaic Power plants; A case study for north Cyprus”

Status: Pending Acceptance

THESISES

Tackie S. N. (2015). Performance Evaluation of Serhatkoy PV Power Plant. Published Master Thesis, Near East University, Department of Electrical and Electronics Engineering, Faculty of Engineering, Nicosia, Cyprus.

COURSES GIVEN *(from 2015 to 2021)*

Undergraduate:

- High Voltage Techniques II
- Circuit Theory II
- Circuit Theory I
- Electromechanical Energy Conversion I
- Electronics I
- Computer Applications
- Electrical Materials
- Introduction to Electrical & Electronic Eng.

RESEARCH INTEREST

- Power Electronic Converters
- Custom Power Devices.
- Renewable Energy Sources

HOBBIES

- Reading, Basketball, Football, Gym.

APPENDIX 5

ETHICAL APPROVAL REPORT

NEAR EAST UNIVERSITY

ETHICAL APPROVAL DOCUMENT

Date: 08/02/2021

To the Graduate School of Applied Sciences

For the thesis topic entitled “Multilevel Inverter Based DVR”, the researchers declare that they did not collect any data from human/animal or any other subjects. Therefore, this thesis does not need to go through the ethics committee evaluation.

Title: Prof. Dr.

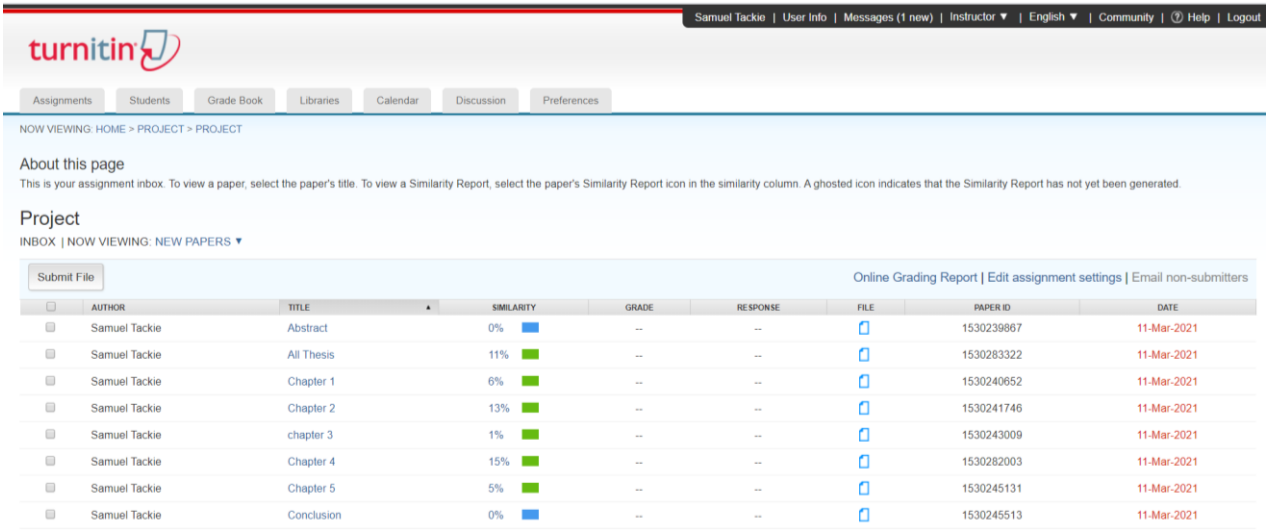
Name Surname: Ebrahim Babaei

Signature:

Role in the Thesis Research: Supervisor

APPENDIX 6

SIMILARITY REPORT



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