SHEHU MADAWAKI GUSAU

ANALYSIS AND SIMULATION OF STACKED MULTICELL INVERTER WITH REDUCED NUMBER OF VOLTAGE SOURCES

NEU

2021

ANALYSIS AND SIMULATION OF STACKED MULTICELL INVERTER WITH REDUCED NUMBER OF VOLTAGE SOURCES

A THESIS SUBMITTED TO THE INSTITUTE OF GRADUATE STUDIES

OF

NEAR EAST UNIVERSITY

BY

SHEHU MADAWAKI GUSAU

In partial Fulfilment of the Requirement for the Degree of Master of Science

In

Electrical and Electronics Engineering

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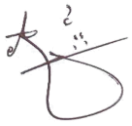
Approval of Director of Institute of Graduate Studies

Prof.Dr. Kemal Husnu Can Baser

We certify this thesis is satisfactory for the award of the degree of Masters of Science in Electrical and Electronics Engineering

Examination Committee in Charge:

Prof. Dr. Ebrahim Babaei — Supervisor, Faculty of Electrical and Computer Engineering, University of Tabriz.



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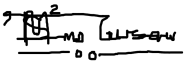
Signature: 

Date: 12/05/2021

ACKNOWLEDGEMENTS

It is my great pleasure to acknowledge the contributions of many individuals during the period of my studies at Near East University. Important personalities who have directly or indirectly helped toward the writing of this thesis.

I would like to extend my sincere and profound gratitude to my beloved mothers of my children, for their patience, support, understanding and numerous contributions to the overall achievement towards the completion of the program. Moreover, I would like to thank the management of the Federal Polytechnic Kaura Namoda who provides me with a full scholarship to study Master's degree in Electrical & Electronics Engineering at the Near East University. Also, I am greatly indebted to my supervisor Prof Dr. Ebrahim Babaei for his kind guidance throughout the period of my research. His comments and corrections have always helped me to improve my work in many ways. Moreover, I would like to thank my H.O.D; Prof..Dr..Bulent Bilgehen, and my Advisor Asst. Prof. Dr. Sertan Serte for their kind support and encouragement.

Furthermore, I would like to sincerely thank my parents for they are the key behind my success. A special mention of my Senior Brother Wadatau Madawaki for his moral and financial support offered to me which helps very much towards the completion of my studies. Ibrahim M. Madawaki is worthy to be mention for the greater role he played during my absence from home. Best regards to other family members.

To my parents…

ABSTRACT

Multilevel converters are instrumental in the integration of energy systems into electric power grids. A stacked multicell novel converter is presented in this research which is perfect in tying various energy/electric systems into the main power systems. Lower rated switches, one input dc voltage, reduced converter size, minimized converter losses, small installation area and reduced converter cost are the advantages of the presented stacked multicell converter when juxtaposed with traditional topologies. Simulation of the presented stacked multicell converter topology in five case scenarios with varying number of cells and stacks is investigated in PSCAD software environs and output waveforms generated and compared to theoretical waveforms.

***Keyword*:** multilevel converter, stacked multicell converter, power systems

OZET

Çok seviyeli dönüştürücüler, enerji sistemlerinin elektrik güç şebekelerineentegrasyonunda etkilidir. Çeşitli enerji / elektrik sistemlerini ana güç sistemlerine denemek için mükemmel olan bu araştırmada yığılmış çok hücreli yeni dönüştürücü sunulmaktadır. Düşük nominal anahtarlar, bir giriş dc voltajı, azaltılmış dönüştürücü boyutu, minimize edilmiş dönüştürücü kayıpları, küçük kurulum alanı ve azaltılmış dönüştürücü maliyeti, geleneksel topolojilerle bir araya getirildiğinde sunulan yığılmış çok hücreli dönüştürücünün avantajlarıdır. Beş durum senaryosunda yığılmış çok hücreli dönüştürücü topolojisinin simülasyonu PSCAD yazılım ortamında ve üretilen çıkış dalga formlarında değişen sayıda hücre ve yığın ile incelenmiş ve teorik dalga formlarıyla karşılaştırılır. `

***Anahtar Kelimeler*:** çok düzeyli dönüştürücü, yığın çok hücreli dönüştürücü,güç sistemleri

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LIST OF ABBREVIATIONS

E:	Input voltage
F_{sw} :	Switching frequency
F_o :	Output frequency
C :	Circuit capacitance
R_L :	Load Resistance
L_L(a) :	Load inductance
$C_L(b)$:	Load Capacitor
M:	Modulation index
F_{sw} :	Switching frequency
E :	Input voltage (2 upper stacks**)**
E :	Input voltage (1 lower stack)
$\frac{1}{2}$ E:	Input voltage (upper stack)
$\frac{1}{2}$ E:	Input voltage (lower stack**)**

CHAPTER 1

INTRODUCTION

1.1 Overview

Electric power is an integral component of any developed society. Stable, affordable and power quality are some major characteristics of electric power. An important device which is capable of providing the aforementioned characteristics is the power electronic converter. The term power electronic converter is a generalized expression which is used to describe the various types of devices in power supply systems which performs the following functions; rectification where the device is called rectifier, inversion where the device is called an inverter, chopping functions for both ac and dc systems, in the ac systems the device is called cycloconverter and for the dc systems the device is known as dc-dc choppers.

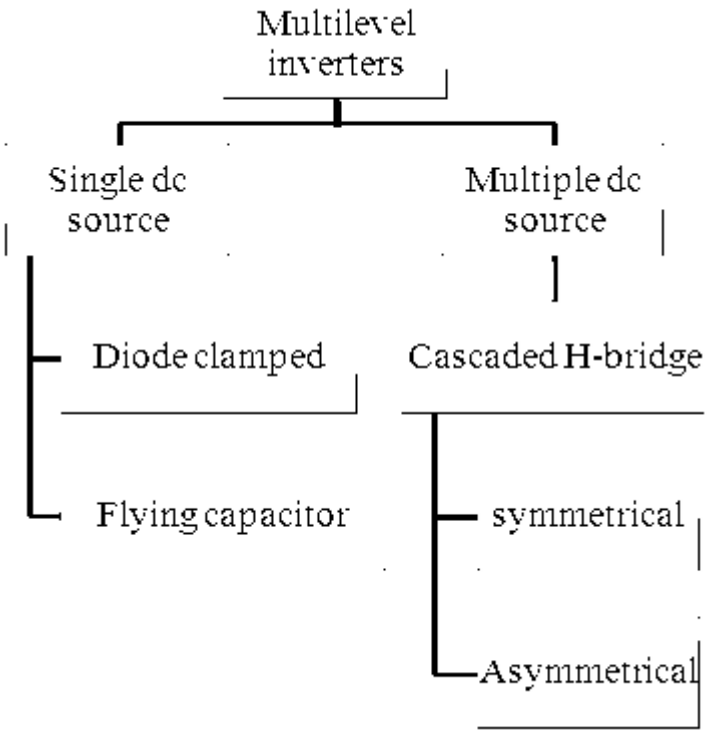

Figure 1.1: Multilevel inverter classification

Several topologies of inverters have been developed over the past decades; the conventional two level inverter is regarded as the pioneer inverter, however due to some

major limitations lack of stepped output voltages the multilevel inverter was developed to overcome these drawbacks. Multilevel inverter is a general terminology which is used to describe various inverter topologies which are competent in producing three levels of output voltage. The first "multilevel" inverter is the Diode clamped topology presented by (Fang Zheng Peng, 2003). Multilevel inverters in general offers multiple merits such as scalability, stepped output voltage, lower rated switches, quality output waveforms, reduced switching losses, reduced size and volume. Since the introduction of multilevel inverters about 30 years ago, it continues to receive maximum attention from researchers in academia and also multiple applications in various industrial setups. Researchers in academia have spearheaded the development of different categories of multilevel inverters. The three most common which are also regarded as the traditional topologies are the cascaded H-Bridge, Flying Capacitor and Diode Clamped multilevel inverters.

The use of fossil fuels as the main source of generating electric power has come under multiple reviews because of several concerns such as cost and price fluctuations of crude oil, negative effects on the environment and increased demand of electric power. The aforementioned drawbacks coupled with increased technological improvements have caused tremendous leap in the use of the various renewable energy sources for producing electric power. The global trend especially in developed countries is to have hundred percent generation capabilities based on renewable energy sources. Fig1.1 shows a comparative illustration of generation source between renewable and non-renewable sources.

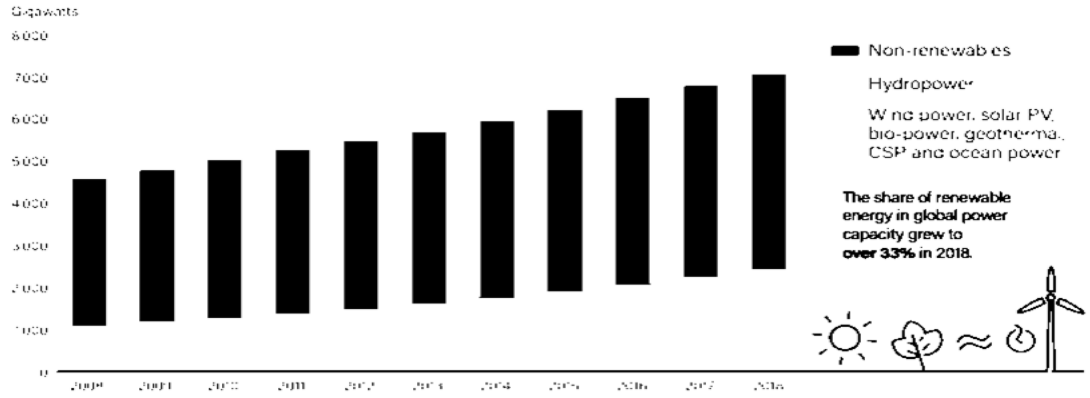

Figure 1.2: Electric power generating sources (2)

Power electronic converters are important components in power supply systems that allows for flexible and efficient integration of various modern generation systems such as renewable energy systems, distributed generation systems and other important grid based systems such as FACTS, HVDC and major power compensating technologies such as STATCOM, DVRs, UPs etc. Therefore, it can be said that power electronic converters are crucial devices in the power supply chain which performs various functions such as power magnitude control, power compensations, power direction control between the source (generation stations), the grid and the consumer.

The main controllable components in most converters are the power switches which can be any of the following MOSFETs, IGBTs Thyristor etc. By controlling the switching pattern i.e. the turn-on and *turn-off* states of the power switches produces the desired output voltage which in essence is to be a sinusoidal waveform. Power switches or semiconductor switches are critical components of the converter, they determine the size and volume, also they determine the efficiency and the cost of the converter. Basically the power ratings of the switches are very important hence it's appropriate to apply lower rated switches to maximise efficiency, reduce the size and volume and also minimise the cost of the converter. High power systems require high rated switches which are currently non-available commercially, however, these limitations can be overcome by selecting lower rated switches which can be utilized by connecting them in either series or parallel depending on the desired power characteristics. Among the traditional multilevel inverter topologies is the Flying capacitor in which two other topologies which are referred to as Flying Capacitor and Stacked Multicell topologies are derived. These two topologies of Flying capacitors have received tremendous attention over the past few years due to the many worthwhile advantages such as modularity, Transformer less functionality, clamping diodes are not required, isolated dc links not required, even allocation of switching stress, modularity, inbuilt self-balancing functionality and scalability (Holtz, Stadtfeld Lammert, 1985), (Siwakoti, 2018), (Li, Lee, & Boroyevich, 2010), & (Mailah et al., 2012).

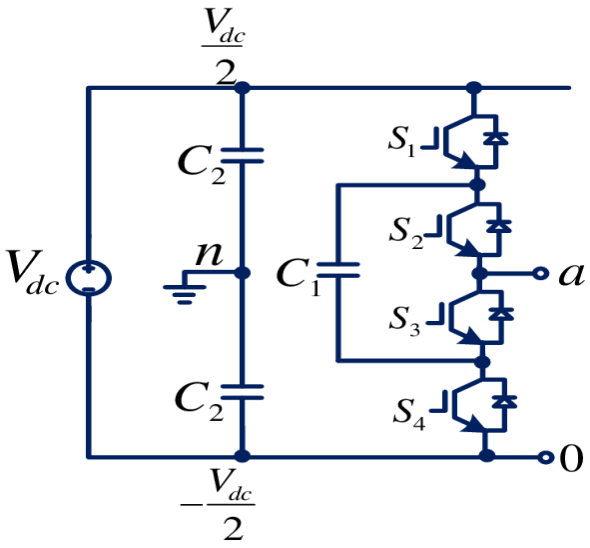

Figure 1.3: Single phase flying capacitor inverter

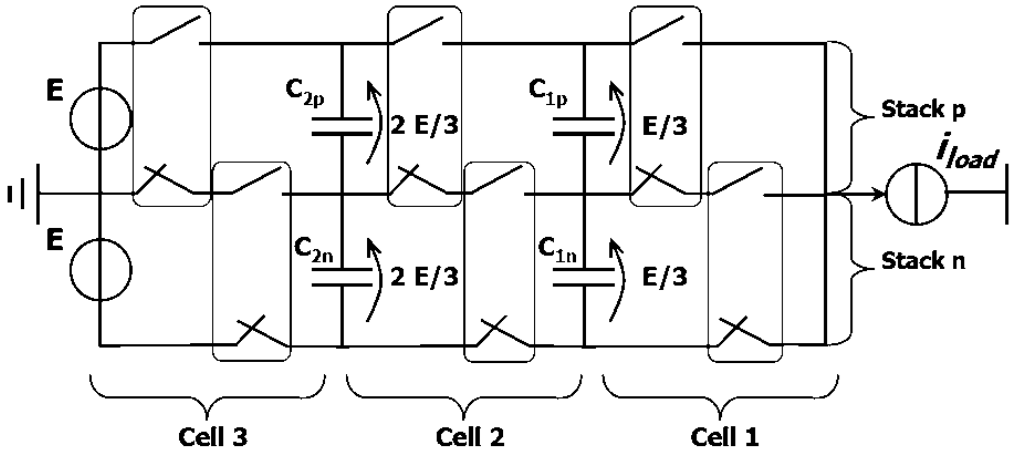

Figure 1.4: A *3 x 2* stacked multicell inverter

1.2 Thesis Problem

Multilevel converters have become integral components in the electric power generation and electric power supply systems. However, they are bedevilled with a few drawbacks which are being addressed by researchers in academia. A critical limitation amongst these drawbacks is the issue of efficiency. Several factors such as size, volume, cost and converter losses directly or indirectly affect the efficiency of converters. The total number of components or devices especially semiconductor switches and dc power sources employed in the converter design affects the cost of converter, increases the volume and

size of converter, increases the converters losses due to switching and conduction; these limitations directly or indirectly affects the converter efficiency and also the total performance of the converter. because of the importance of power electronics converters in power systems, they cannot be replaced with other devices however they can be remodelled or designed to limit these drawbacks thereby improving the performance and efficiency of the converter.

1.3 **The Aim of the Thesis**

The number of devices such as switches therefore minimum switching losses The above mentioned disadvantages of power electronics converters are critical factors which limits the performance and efficiency of the converter. Resolving or overcoming these limitations are important steps in solidifying power electronic converters as the appropriate device for power conditioning. The focus of this research is to present a multicell converter with a reduced number of dc power sources and also minimise the total number of semiconductor switches employed in the design of the converter; this definitely will result in a converter having a minimum size, reduced volume, minimum.

1.3.1 The Importance of the Thesis

As mentioned above, power electronic converters have become integral components in the electric power generation and electric power supply systems. However, a few limitations still bug these converters thereby limiting the efficiency and performance of the converter. The aim of this research is to present a multilevel converter topology which utilizes one dc power source and minimum number of devices. The presented topology will have the following merits:

- One dc source
- Minimum converter size
- Minimum converter volume
- Less installation area
- Less number of semiconductor switches
- Increased efficiency
- Improved performance

1.3.2 Limitation of Study

Simulation based research tends to have the least of limitations, however proper and efficient application of the software tool tends to introduce a few limitations when the applicant does not so much experience in its usage. Even in the absence of laboratory investigations, the chosen software of PSCAD provides minimum differences between laboratory results and simulation results.

1.4 Overview of the Thesis

This research or thesis is categorized into the following body of chapters:

Chapter 1: Introduction, Thesis Problem, Aim of the Thesis, The importance of the Thesis, Overview of the Thesis

Chapter 2: Literature Review of Multilevel Converters

Chapter 3: Presented Topology and Simulation Results

Chapter 4: Conclusion and Recommendation

1.5 Ethical Considerations

Considering the preparation of design requirements and ethical features of design procedures is implemented during the thesis work. Therefore, use of commonly recognised standards or customs, such as protection or confidentiality, are at pale; of trade-offs between different designs principles. The other Ethical consideration is giving appropriate credits while using the ideas or words of other researchers by proper citing.

CHAPTER 2

LITERATURE REVIEW OF MULTILEVEL INVERTERS

2.0 Introduction

Investigation of inverters specifically multilevel inverters will be reviewed in this section of my thesis. Inverters in general are devices which are used to change the waveform characteristics of voltage from a direct current nature into an alternating current nature. There are several topologies of inverters, these topologies are classified with respect to the following characteristic nature of the input voltage i.e. VSI (voltage source inverter) or CSI (current source inverter), the nature of the output voltage, the type of circuit topology etc. The various topologies of inverters possess individual advantages and disadvantages; however, the multilevel inverter topology offers multiple advantages when compared to other topologies especially the classical two level inverter.

2.1. Multilevel Inverters (MIL)

The multilevel inverter topology is regarded as one the revolution inverter topologies which has drastically changed the manner in which inverters are developed and applied. This is not to mention the countless advances which have been chalked in improving multilevel inverter topology. Also it continues to receive maximum attention in the various areas where study, development and application of multilevel inverters are required. Multilevel inverters are generally defined by the number of levels of voltage it's able to generate at the output. Hence any stepped output voltage with three or more levels is regarded as a multilevel inverter. In general, there are three conventional topologies of multilevel inverters, these topologies are the Diode Clamped topology, Flying Capacitor topology and the Cascade H-Bridge topology. Apart from these conventional topologies there are other topologies such as the impedance based MIL, Hybrid MIL which is developed by combining the conventional topologies or combining any of the conventional topologies with other topologies of inverters. Also there are the modular multilevel inverter topologies and finally there's the Multicell topology which is the major area of my research.

$$V_{C1} = \frac{1}{2}E_d = V_{C2} = \frac{1}{2}E_d \quad (2.1)$$

2.1.1 Neutral Point Clamped (NPC) MIL

Diode clamped MIL is also commonly referred to as neutral point clamped inverter is part of the conventional multilevel inverter topologies which applies several or multiple diodes as a clamping device for the source or input voltage, by this method the source voltage is shared equally across the number of capacitors connected between the input and the load. Because multiple diodes are required for clamping purposes, the total number of diodes required in this topology tends to be on the high side especially when higher steps of output voltage are desired. Direct relationship exists between the number of output steps and the number of capacitors connected to the clamping diodes. Another major limitation when higher levels of output voltage is desired is that, the structure of the inverter becomes complex and also its control technique is cumbersome. Unlike other multilevel inverter topologies, the Diode clamped topology requires just one dc input voltage. Several topologies of Diode clamped MIL have been presented after the first topology was presented by (Nabae, Takahashi, & Akagi, 1981). These other topologies seek to decrease the quantum of clamping diodes and also minimise the semiconductor switch count, on the number of output levels, higher levels are achieved by either changing the circuit structure of the initial topology or improve the various PWM techniques

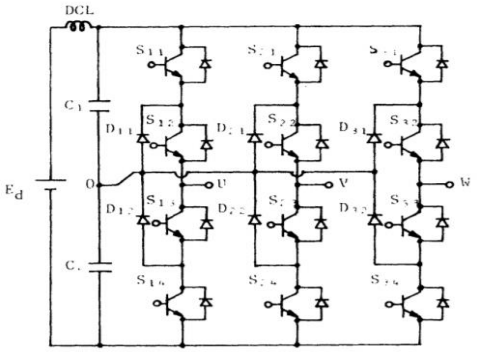

Figure 2.1: Three levels NPC (2)

The initial three-phase 3-level diode clamped topology is shown by Fig. 2.1. The structure of the presented topology requires six clamping diodes, one dc source, two capacitors, twelve power switches for the whole three-phase while each single phase requires only two clamping diodes and four power switches. The load voltages generated are between any of

the following magnitudes within a given time frame $0, \pm\frac{1}{2}E_d$. These magnitudes are the capacitor voltages which are expressed by (2.1). Fig. 2.2 shows the single-phase structure of the conventional or presented neutral point clamped. From this structure two new topologies referred to as active neutral point clamped (ANPC) and type T NPC have been developed. The main rational behind the development of these two topologies is to decrease the quantum of clamping diodes and give more freedom of control because diodes are uncontrollable devices. Fig. 2.3 shows the power circuit of the presented ANPC topology where unidirectional power switches are utilized in replacing the clamping diodes of the conventional structure. Fig. 2.4 shows the power circuit of the type T-NPC where bidirectional power switches are utilized in replacing the clamping diodes of the conventional structure.

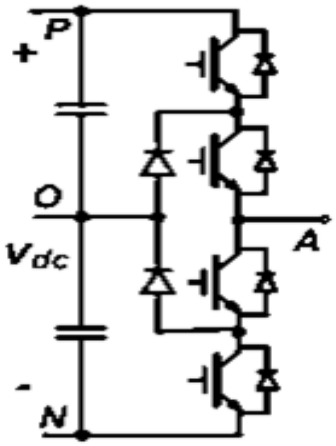

Figure 2.2: NPC (3)

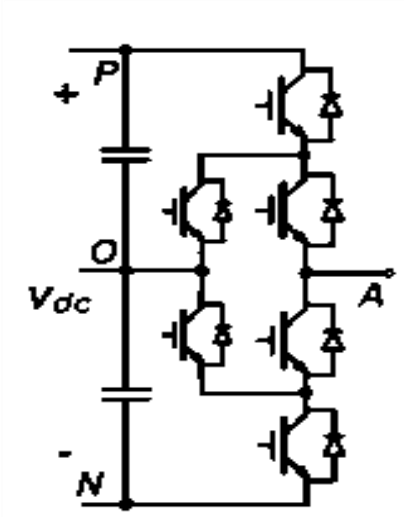

Figure 2.3: ANPC (3)

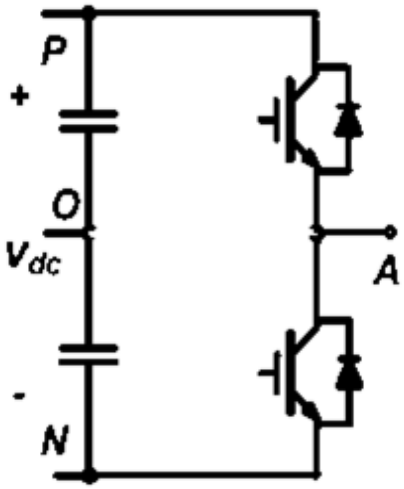

Figure 2.4: T-type NPC (3)

This section will review selected published NPC topologies as well as other improved or hybrid NPC topologies. Fig. 2.4 shows the presented five level ANPC by (Siwakoti, 2018). Which boast of less number of components especially power Switches. Analysing the power circuit reveals that it has one dc voltage input, two capacitors, six unidirectional switches for each single-phase, the component number will increase for the three-phase structure. Fig. 2.5 shows the single-phase topology while the Fig. 2.4 illustrates the three-phase structure.

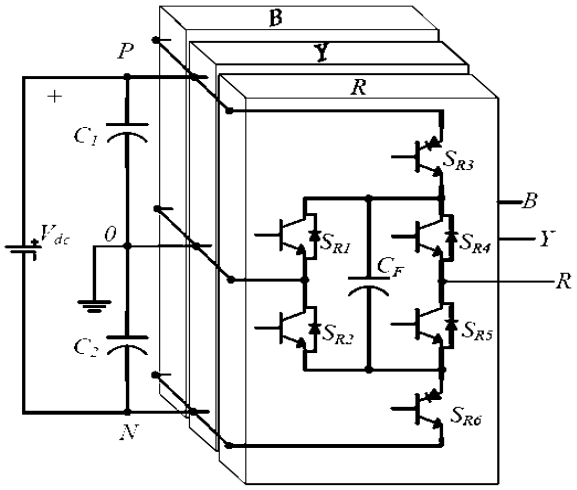

Figure 2.4: Three-phase 5-level ANPC (4).

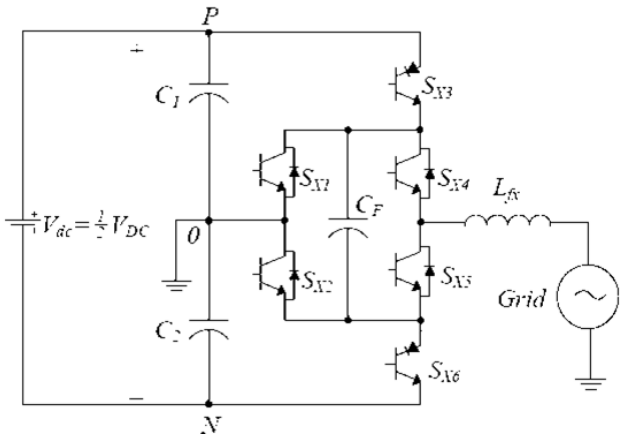

Figure 2.5: Single-phase 5-level ANPC (4).

An ANPC inverter with zero current transition capabilities is presented by (Li, Liu, Boroyevich, 2003). The presented topology is derived by adding a resonant tank and just one auxiliary switch to conventional ANPC structure. The zero current state during the turning off the power switch is achieved with less stress on the switch because the voltage stress is equivalent to the clamped voltages. The presented topology further boast minimum recovery power losses and power losses during the turn-off transition. Fig. 2.6 shows the single-phase structure of the presented topology whiles Fig. 2.7 shows its three-phase structure.

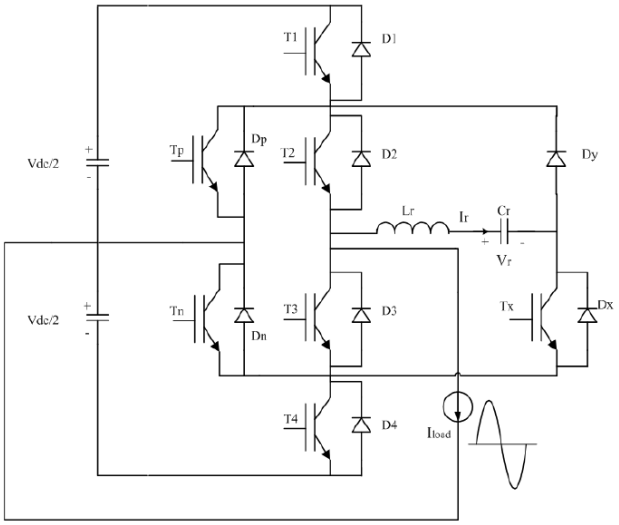

Figure 2.6: Single-phase ZCT-ANPC (5)

The magnitude of the output voltage in the presented topology is equivalent to the conventional topology, however this topology has two ways of connecting the neutral point and the node irrespective of the load currents direction.

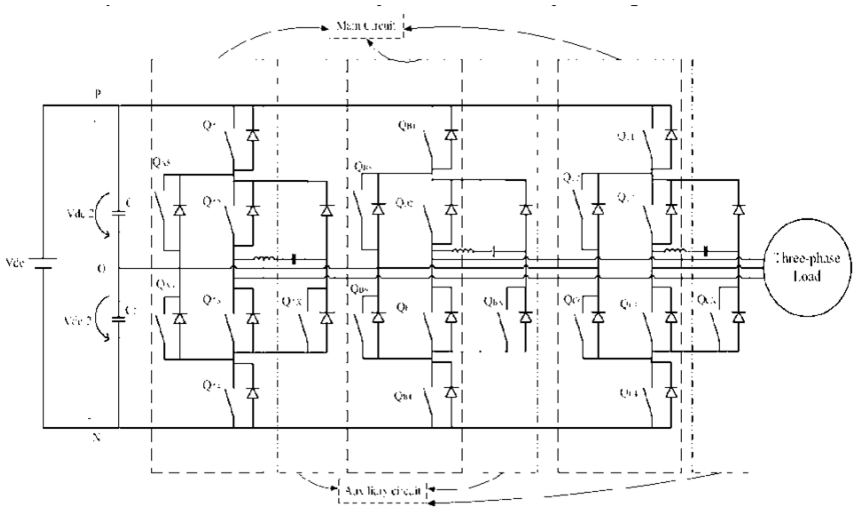

Figure 2.7: Three-phase ZCT-ANPC (6)

A 5-level neutral clamped MIL is proposed which is capable of reducing the total current in the distribution line was presented by (Mailah et al., 2012). Also the presented topology is capable of multiplying the input voltage to a significant value as desired. As in the case of all diode clamped topologies, the clamping diode in this presented topology is very high especially in the three-phase topology. one major merit of the neutral clamped topology is

that with higher output voltages, the harmonic content is minimised hence there's no need for an output filter which reduces the cost of the inverter topology. The power circuit of the presented three-phase topology is shown Fig. 2.8. the whole three-phase topology consist of one dc voltage source, four capacitors, 18 clamping diodes, 18 unidirectional power switches.

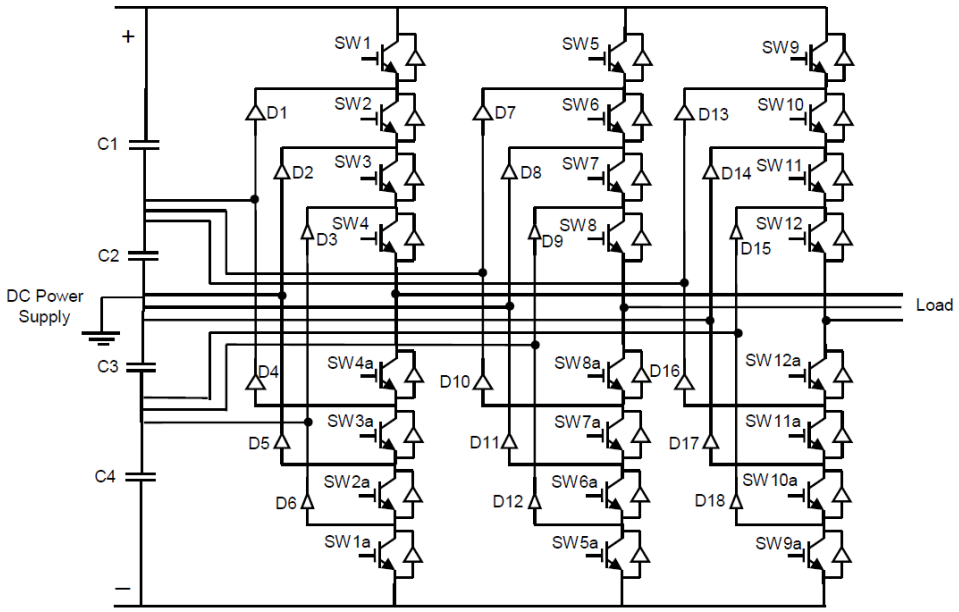

Figure 2.8: 5-level NPC

The presented topology has the following advantages:

a. Minimised clamping diode ratings
b. Reduced component count
c. Minimised system cost
d. Reduced switch ratings
e. Application of conventional PWM technique

A combined topology of impedance source (Z-Source) and neutral point clamped inverter was presented by (Xing, Cheng, Wang, 2014). This topology is able to amalgamate the advantages of these two topologies. The major advantages of the impedance based topology is buck-boost capability and ability to withstand the effects of electromagnetic radiations, this feature is provided or enabled due to the shoot-through state of the impedance based topology. fig. 29 shows the three-phase circuit of the presented Z-source

based neutral point inverter. The impedance structure is placed between the source and the three-phase switches.

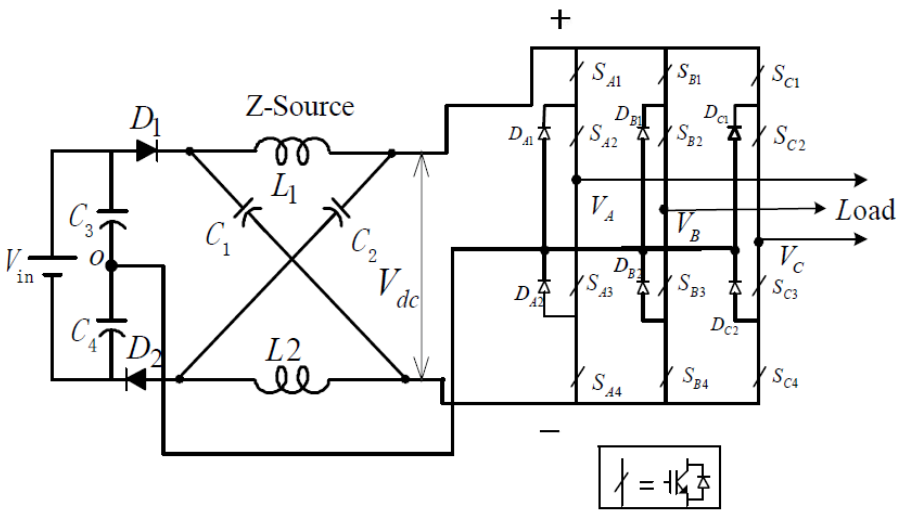

Figure 2.9: Three-phase ZS-NPC

Two modes of operations are possible in the presented topology. These modes of operations provide the buck-boost capabilities and also ability to withstand EMI effects. They are known as shoot-through (S-T) and non-shoot-through (N-S-T) states. The impedance structure is made up of two capacitors and two inductors, two diodes are placed in the upper and lower sections of the inverter for voltage blocking purposes. Because the presented topology is a three-phase the upper switches and lower switches are gated in shoot-through states for either the upper or lower control of the switches. In the upper shoot-though mode, the diode connected in the lower section is reverse biased whiles the diode connected in the upper section is reverse biased in the lower shoot-through mode.

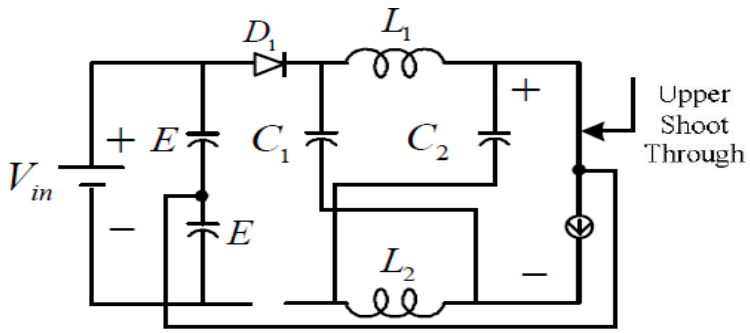

Figure 2.10: Upper shoot-through mode

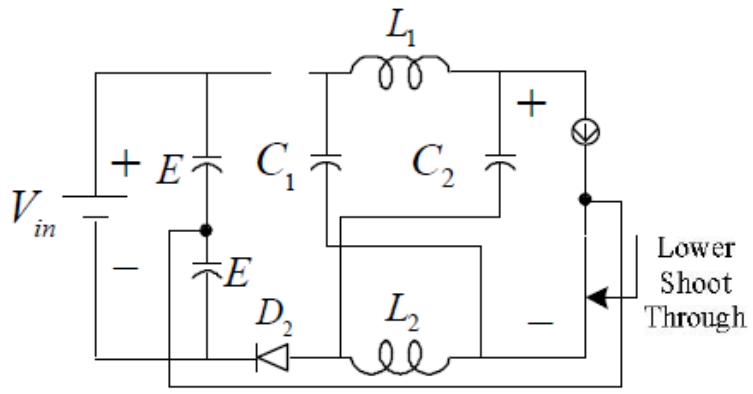

Figure 2.11: Lower shoot-through

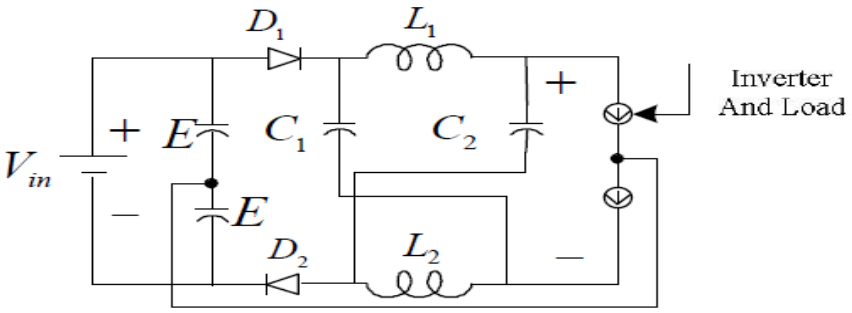

Figure 2.12: Non-shoot through state

During the non-shoot through state, the followings expressions are produced by analysing Fig. 2.12. In this state, diodes D_1 and D_2 conducts. The input voltage V_i is:

$$V = 2\,V_C - E \tag{2.2}$$

The inductor voltage $V_L$is given by:

$$V_L = 2E - V_C \tag{2.3}$$

The boost factor B and the ac load voltage V_{ac} are related by:

$$V_{ac} = B\frac{M}{\sqrt{3}}2E \tag{2.4}$$

A neutral point clamped inverter based quasi Z-Source topology is presented by (Ahmadzadeh, Babaei, 2018). The topology is a three-phase system. Here also the advantages of both topologies are embedded into a single structure. Also this topology

when compared conventional ZS topology and quasi ZS topology is able to provide a much greater boost factor with a lesser duty cycle. It also possesses continues current input capabilities. Applying a smaller duty cycle ensures a minimised THD content as well as reduced voltage stress.

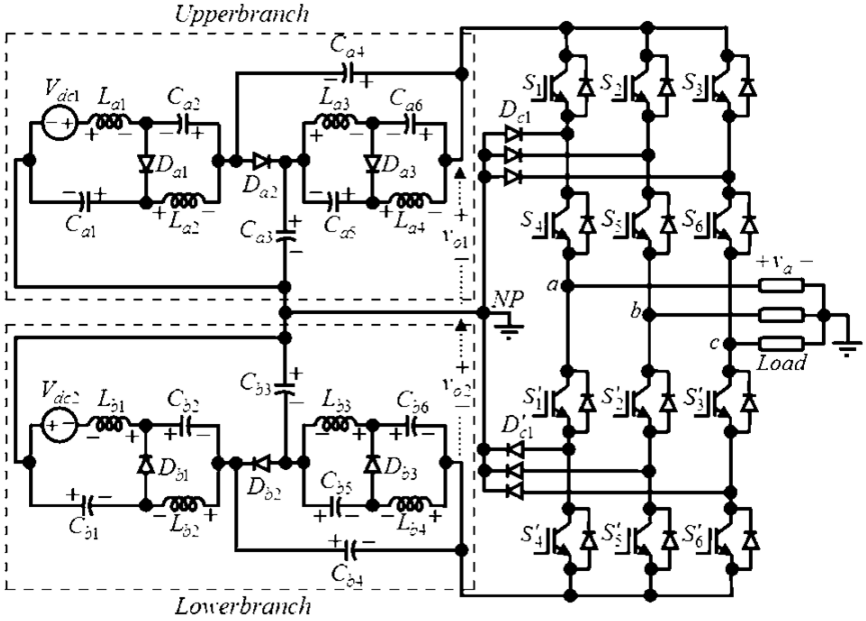

Figure 2.13: Three-phase QZS-NPC

There are four modes of operation of the presented topology; three shoot-through states, the shoot-through if for the upper branch only, the second is for the lower branch only whiles the state is a combination of the upper and lower branches. The fourth mode of operation is the non-shoot through mode. These modes of operation are illustrated by Fig. 2.14 where Fig. 2.14a to Fig. 2.14c represents the various three shoot through modes and Fig. 2.14d shows the non-shoot through state. The maximum upper voltage is given by

$$v_{upper,max} = \frac{V_{dc2}}{1-4D} \tag{2.5}$$

The maximum lower voltage is given by

$$v_{lower,max} = \frac{V_{dc2}}{1-4D} \tag{2.6}$$

The boost factor the presented topology is given by:

$$B = \frac{1}{1-4D} \tag{2.7}$$

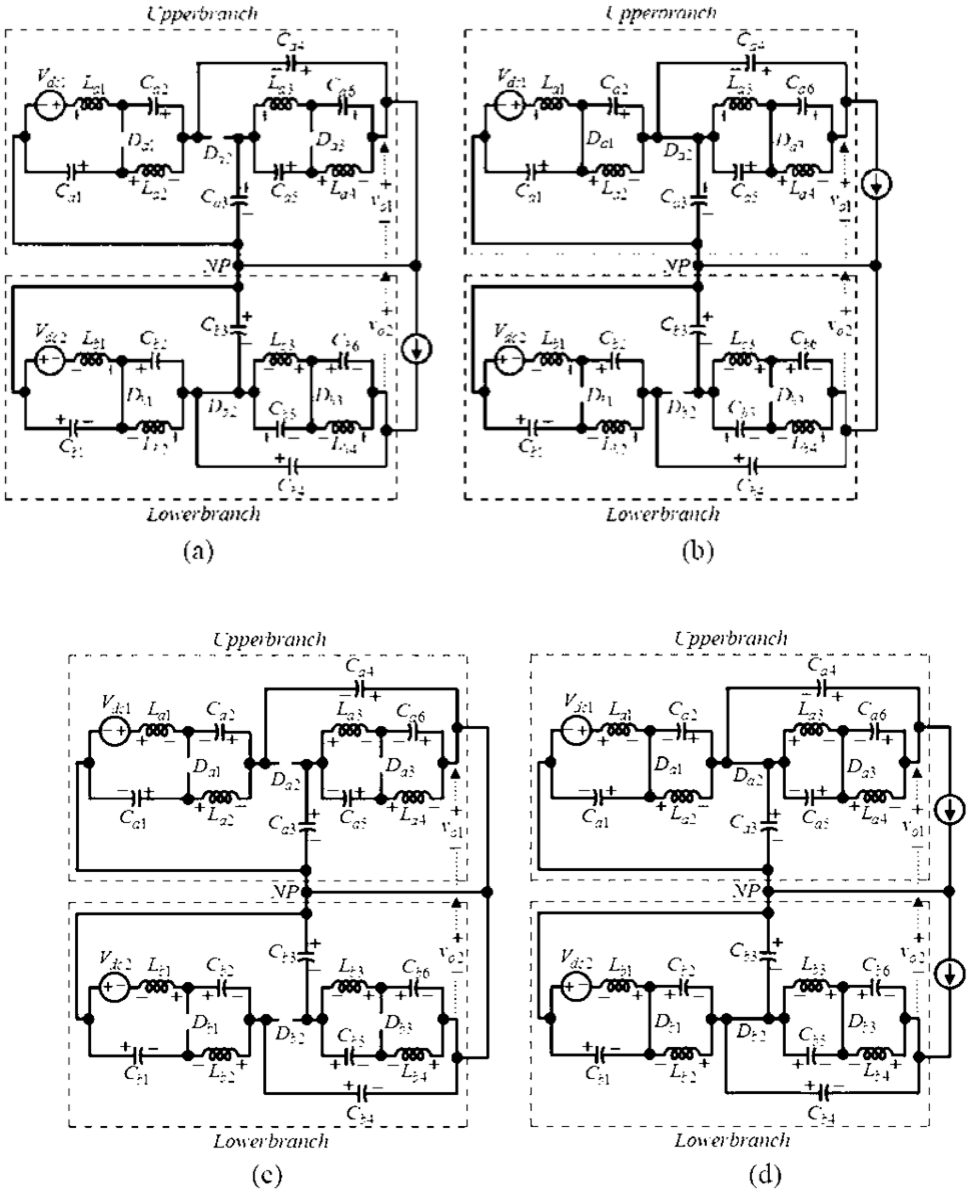

Figure 2.14: Three-phase QZS-NPC modes of operation

2.1.2 Flying Capacitor (FC) MIL

The Flying Capacitor (FC) topology utilizes multiple capacitors for the purpose of voltage clamping. The input voltage is only one dc source however; the magnitude of the stepped load voltage is determined by the clamping capacitors. Each stepped load voltage is made-up of the number of capacitors involved in the closed circuit for that state, therefore the sum of the clamping capacitor voltage in each state constitutes the load voltage. The FC topology and NPC topology have many similarities but differ in the component used for voltage clamping. They also share similar disadvantage of complex structure for high levels of load voltages and very difficult control techniques when higher steps of load voltages are desired. Some advantages as presented by (Sinha, Lipo, 1997). Those advantages of the Flying capacitor topology are listed below:

- Reduced harmonic content
- Elimination of output filter hence cost saving
- Used in high voltage application
- Applied in compensation of reactive powers
- Suitable for PV applications
- No clamping diodes are needed

The power circuit of a 5-level Flying Capacitor topology which is composed of the following components eight unidirectional switches, one dc source, ten clamping capacitors is shown by Fig. 2.15. to obtain the value of the input voltage as a stepped voltage, the four capacitor voltages are summed up to generate this value, looking at the power circuit of the FC structure, the series chain capacitors closest to the dc source have higher magnitudes. The presented topology is a single-phase inverter. The switching table of the presented topology is given by Table 2.1. during each state of operation, four unidirectional switches are gated on while the remaining switches are gated off. The FC topology is not suitable for higher levels of stepped load voltages and also the number of clamping capacitors are high and much higher when applied in higher levels of stepped voltages as presented by (Lai, Peng, 1996).

Table 2.1: Switching Table for 5-level FC inverter

	SWITCHES							
S TATE	**S_a1**	**S_a2**	**S_a3**	**S_a4**	**$S_a'4$**	**$S_a'3$**	**$S_a'2$**	**$S_a'1$**
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3 = V_{dc}/2$	1`	1	0	0	1	1	0	0
$V_2 = V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

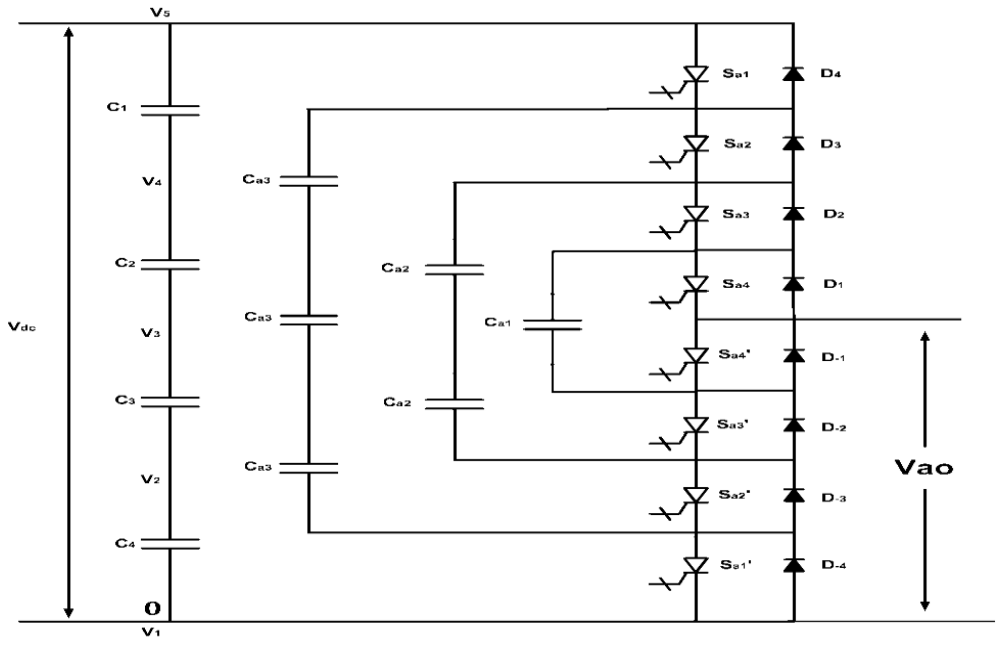

Figure 2.14: 5-level flying capacitor inverter (10)

Some advantages of the flying capacitor topology are:

- Used for compensation of reactive power
- Applicable in high voltage system
- Renewable energy applications
- Clamping diodes are not required
- Output filters are mostly not required
- Reduced system cost due to filter elimination

On the other hand, two principal drawbacks of the flying capacitor topology are the high number of clamping capacitors which are need and also increasing the number of stepped Below are some selected topologies of Flying capacitor for investigation on the structure of the topology, control techniques, applications and theoretical and experimental analysis. A comprehensive review of a single phase HB FC with unequal voltage magnitudes i.e. the values of voltages are not equal thus making them asymmetrical is presented by (Saccol, Giacomini, Batschauer, & Rech, 2019). Introducing the asymmetric feature will maximize the stepped output voltage without increasing the quantum of semiconductors thereby eliminating the complex structure associated high levels of output voltage. Voltage control of the presented topology is done using the charge regulation methodology. Fig. 2.15 shows the structure of the presented topology. There are eight unidirectional power switches, two capacitors and one input voltage.

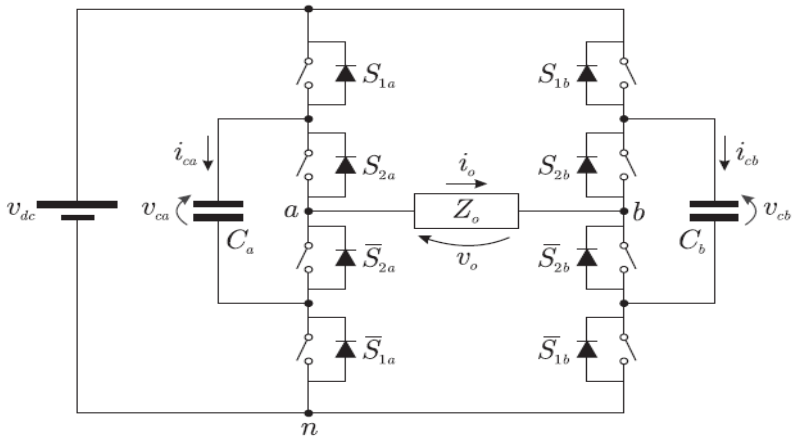

Figure 2.15: Single-phase asymmetric HB-FC

There are two legs in the presented topology's circuit, these legs are represented by v_{an} for the first leg and v_{bn} represents the second leg, each leg can individual generate up to four steps of load voltage, however this heavily dependent on the magnitude of capacitor voltage. The output voltage of this topology is given by:

$$v_o = v_{an} - v_{bn} \tag{2.8}$$

In other to regulate the voltage across each leg, the voltage ratio of the capacitors voltage has to be regulated or controlled. This is very important because the voltage of the capacitors needs to be controlled at values of nominal magnitude in other for the inverter to function effectively. However, this is not possible for asymmetric based flying capacitor inverters because depending on the values of load angle and modulation index, these capacitors values will separate. To overcome this limitation, an appropriate control method is required to bring back the voltage values to nominal magnitude or application of the reduction mode of the inverter. Two states of analysis is presented for the proposed topology, in the first mode, the capacitor voltages for the first leg is identical to the twice that of the second leg i.e. $2v_{cb} = v_{ca}$ whiles the second mode of analysis is given by $v_{ca} = v_{cb}$. The relationship between these voltages and the stepped or levels is given below by:

$$2v_{cb} = v_{ca} \tag{2.9}$$

$$v_{cb} = \frac{2}{m-1} \tag{2.10}$$

$$v_{ca} = v_{cb} \tag{2.11}$$

$$v_{cb} = \frac{2}{m-1} \tag{2.12}$$

An Fc topology of compact structure and high efficiency is presented by (Lei et al., 2017). This topology is a single-phase system which generates 7-Steps of load voltage. The presented topology is amongst the highly sought after inverters for the vehicle charging industry and renewable energy applications especially PV systems. The circuit of the presented uses low voltage switches and active buffer for decoupling power pulsating of the double-line frequency. This decreases the capacitance value when compared to classic systems.

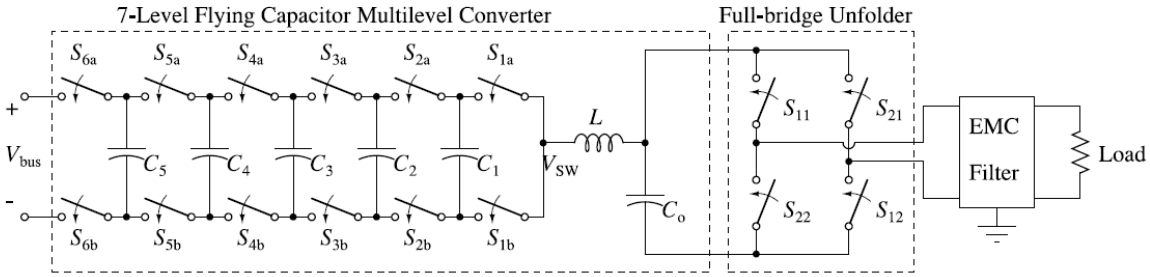

Figure 2.16: FC 7-level inverter

The structure of the presented topology is illustrated by Fig. 2.16. This structure is composed of two parts, the 7-level FC part coupled to a full HB part. Fig. 2.17 shows the same topology where parasitic inductance has been included as well as an output switch capacitance has also been added.

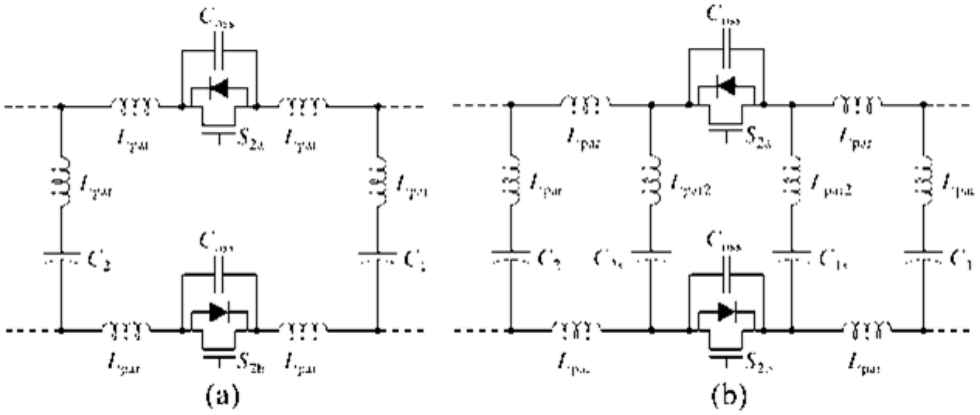

Figure 2.17: (FC 7-level a) decoupling capacitors not included (b) coupling capacitors added

The ripple inductor current $\Delta i_L$and capacitance value C are expressed below by, note N is the level count.

$$\Delta i_L = 0.25 \frac{V_{DC}}{f_{sw} L (N-1)^2} \tag{2.13}$$

A new inverter topology composed from the combination of the two level inverter and flying capacitor topology is presented by (Le & Lee, 2016). The presented topology has the capability to produce 6-levels of load voltage and its considered a hybrid topology because of its derivation method. Comparative analysis of this topology to other published topology with the same criteria shows the presented topology requires less quantity of components to produce the level of output voltage. Application of less quantum of circuit components is a plus because the size of the inverter is minimized, the volume and weight are also drastically reduced. The over efficiency of the inverter is high when compared to inverters that requires more components. The switching loss in this presented topology is not minimized because of the application of less components. The structure of the presented topology is given by Fig. 2.17. There are four capacitors and eight unidirectional power switches. The flying capacitor has 4 switches and three capacitors while the two level inverter has four switches and one capacitor. The switching or control mechanism of the presented topology is shown Table 2.2. from this switching table, the magnitudes of the various state voltages are indicated, the maximum load voltage is V_{dc}. Also the value of the load current during each state of switching is presented.

Table 2.2. Switching States for 6-level Hybrid FC

STATE	$\mathbf{S_{a1}}$	$\mathbf{S_{a2}}$	$\mathbf{S_{a3}}$	$\mathbf{S_{a4}}$	$\mathbf{V_{AN}}$	$\mathbf{i_{Ca}}$
V_0	0	0	0	0	0	0
V_1	1	1	0	0	$V_{dc}/5$	0
V_2	0	0	0	1	$2V_{dc}/5$	$-i_a$
V_3	0	0	1	0	$2V_{dc}/5$	i_a
V_4	1	1	0	1	$3V_{dc}/5$	$-i_a$
V_5	1	1	1	0	$3V_{dc}/5$	$-i_a$
V_6	0	0	1	1	$4V_{dc}/5$	0
V_7	1	1	1	1	$V_{dc}/5$	0

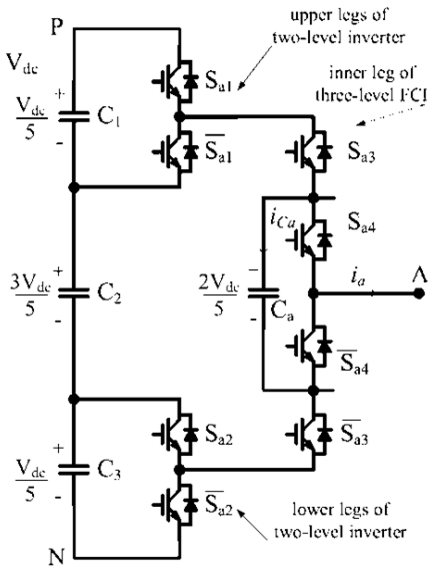

Figure 2.18: Hybrid FC inverter (19)

A novel fault detection and fault control technique was presented by (Amini & Moallem, 2017). Which was used to maximize the reliability and robustness of multilevel inverters especially the flying capacitor topology. Higher stepped voltages in FC topologies requires the application of more semiconductors switches and because of that they vulnerable to failures. The goal of the presented fault detection technique is to provide the same value of stepped voltage irrespective of any default or defective switches. This provides the ability of the converter to function appropriately during the fault condition of one switch. This achieved without undermining the converters operational quality.

The faulty semiconductor switches are detected by application of capacitor's charging state information and the switching arrangements data is also used. When the defective switches are identified, the control techniques to eliminate these switches in the switching sequence and transmits the information to other switches to generate the desired level of load voltage. The circuit of the FC used in this analysis is shown by Fig2.18 and the complete control technique for the control scheme is shown by Fig. 2.19.

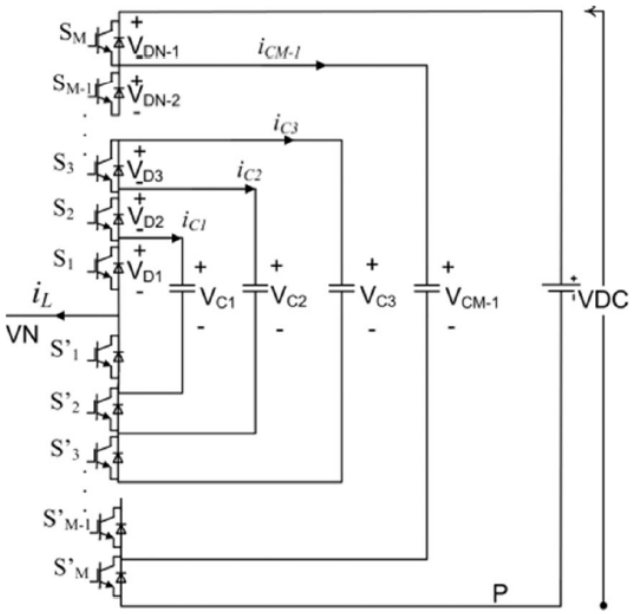

Figure 2.18: One leg of configured FC topology

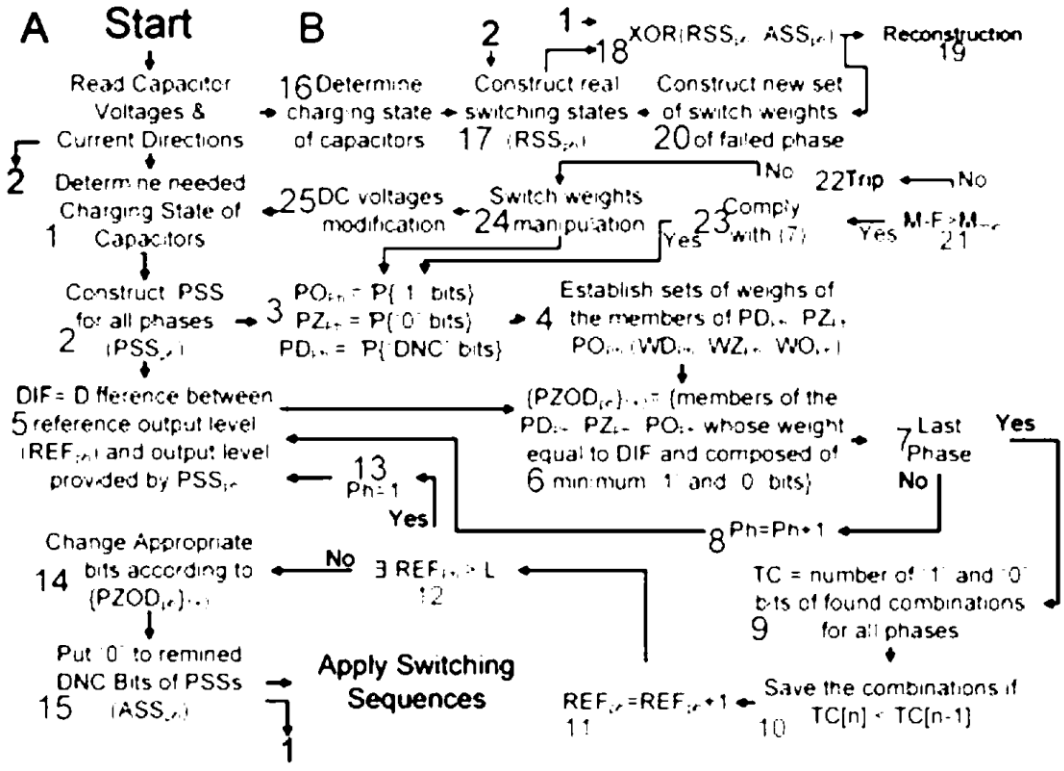

Figure 2.19: Presented control method

A different fault-bearing flying capacitor topology is presented by (Kou, Corzine, & Familiant, 2004). The feature in this topology works appropriately under only one switch default condition, the inverter is still able to provide the required stepped voltage by reprogramming the short-circuited defective switch. With this mechanism, the inverter has the capability to function correctly without any shortcomings hence the status of the reliability of the inverter is retained. The circuit used in analysing this method is shown by Fig. 2.21. There is one input voltage, two capacitors and six switches; three for the upper section and three for the lower section. Four stepped voltages can be produced by this inverter and the six control scheme during a faulty switch is shown by Fig. 2.20.

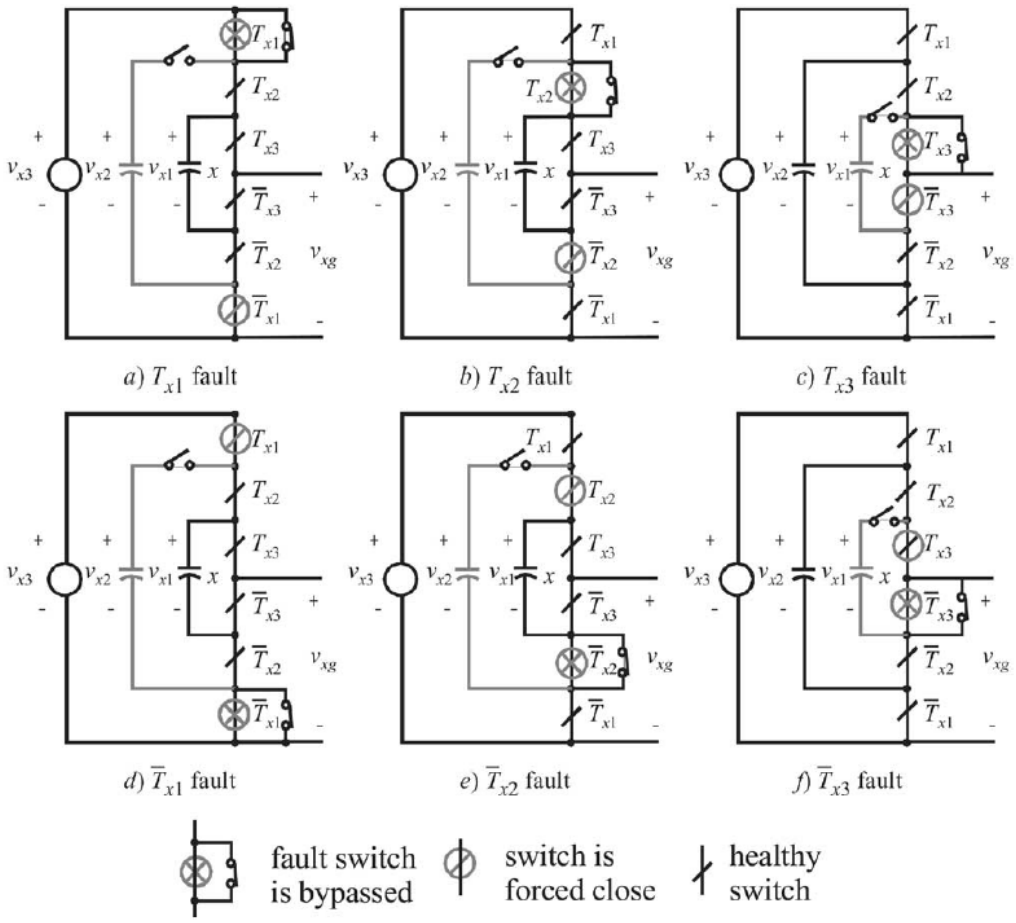

Figure 2.20: Six states of fault condition (15).

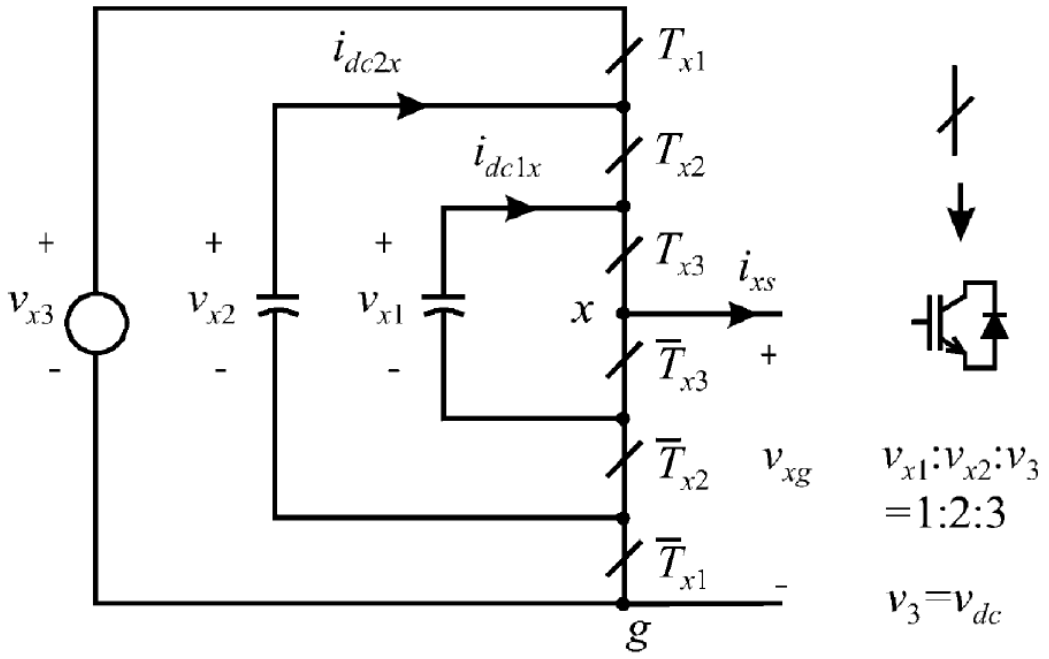

Figure 2.21: Fault-bearing FC (15).

A BSMC flying capacitor which is obtained by the Bridge-Modular-Switched-Capacitor structure is presented by (He & Cheng, 2016). Where a 5-level of stepped voltage is produced by this converter. Two topologies of switched capacitor and flying capacitor are combined to form this topology hence it combines the advantages of these two topologies which are high voltage boosting feature and multilevel functionality from the flying capacitor topology. The presented BSM topology possess the following advantages of deceased switching losses because of frequency modulation of the line voltage and reduced number fof devices in the circuit structure. These advantages provide an improvement of the power density and efficiency of the BSMC converter. The circuit structure of the presented converter is given by Fig. 2.22; there are twelve semiconductor swatches of unidirectional form and on dc source. The control mechanism of the presented converter is phase disposition method. Two states of control are applied in the converter operation. These states are illustrated by Fig. 2.23a and Fig. 2.23b. the capacitor voltages are given by:

$$Vu = U_{C1a} = U_{C1b} \tag{2.15}$$

$$2U_i = U_{C2a} = U_{C2b} \tag{2.16}$$

$$4U_i = U_d \tag{2.17}$$

$$4\,U_i = U_{\,C2a} + U_{C2b} \tag{2.18}$$

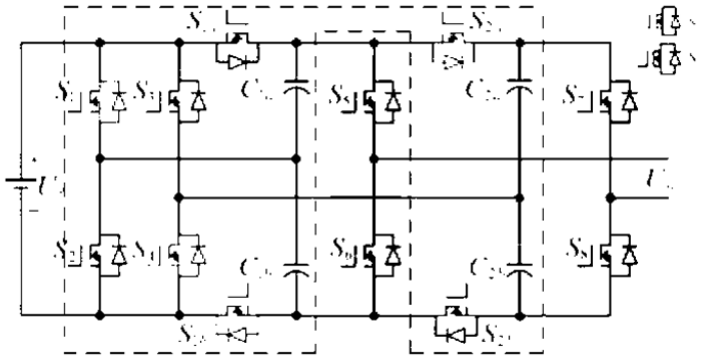

Figure 2.22: FC-BMSC inverter (16)

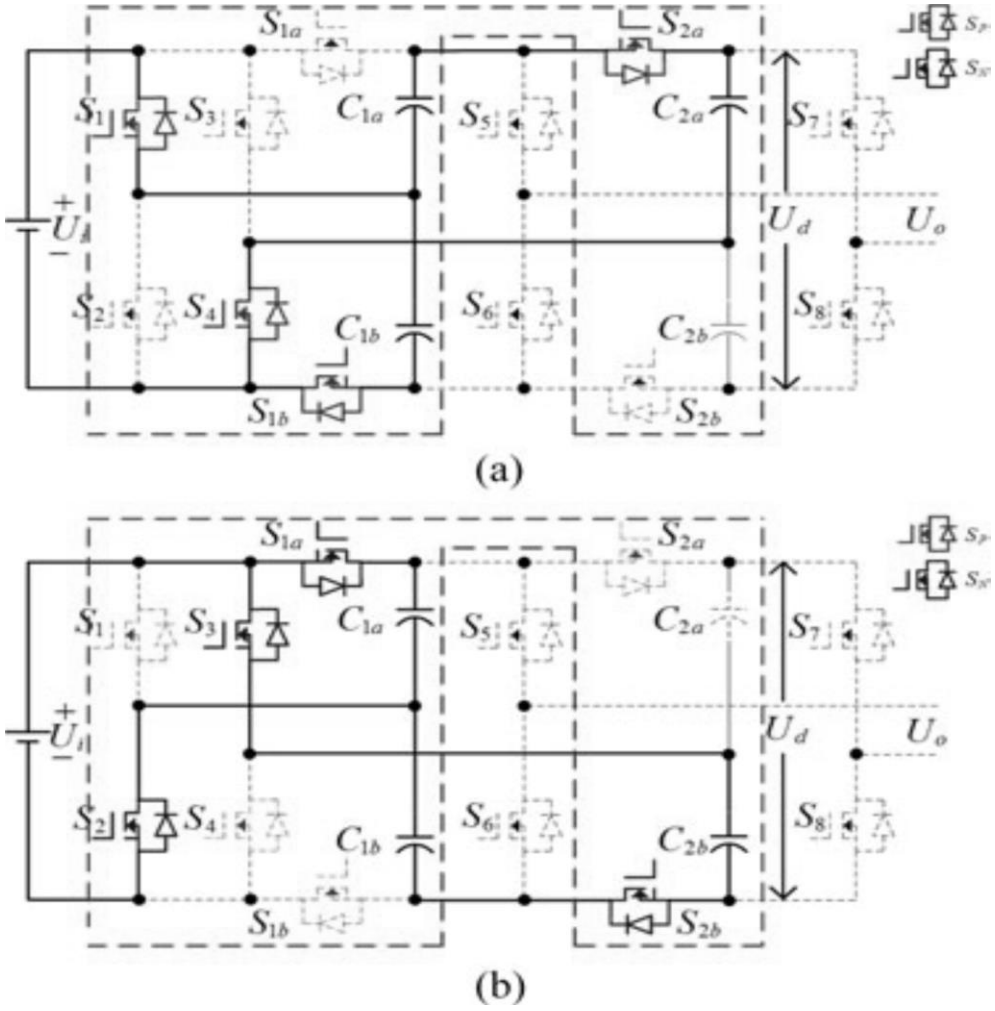

Figure 2.23: FC structure operation (16)

A split-source based inverter (SSI) developed from the flying capacitor is presented by (Abdelhakim, Mattavelli, & Spiazzi, 2017). These SSI topologies are single stage topologies which are able to provide a variety of functions such high boost capabilities. Incorporating the FC topology into SSI topology provides multilevel functionality of 3-levels.

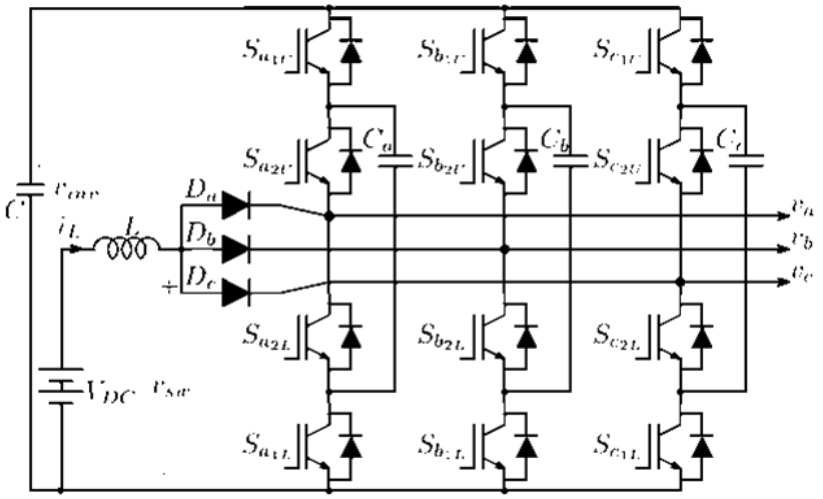

Figure 2.24: Presented 3-level SSI-FC

Fig. 2.24 shows the presented SSI-FC topology. the topology is a three-phase structure and made up of twelve power switches, one dc source, four capacitors and three diodes. Each leg of the presented topology contains two switches in the inner or lower part and two switches in the outer or upper section. The capacitance value is determined below by (2.19) where $I_{\emptyset}$ phase peak current and ΔV_C is the peak ripple voltage.

$$C = \frac{I_{\emptyset}}{f_s \Delta V_C 2\sqrt{2}} \tag{2.19}$$

Fig. 2.25 shows the charging and discharging mode of the inductor of Fig. 2.25. The inductor is charged by concurrently switching the lower switches of any phase. The circuit diagram during these periods of charging and discharging are shown by Fig. 2.25a and Fig. 2.25b respectively, the capacitor and inductor discharging periods are given by Fig. 2.25c. the inductor value is determined by:

$$L = \frac{V_{DC}(2M-1)}{2 f_s \Delta I_L} \tag{2.20}$$

The relation between in the output voltages are expressed by:

$$\frac{V_{in}}{V_{DC}} = \frac{1}{1-M} \tag{2.21}$$

$$\frac{V_{\emptyset}}{V_{DC}} = \frac{M}{1-M\sqrt{3}} \tag{2.22}$$

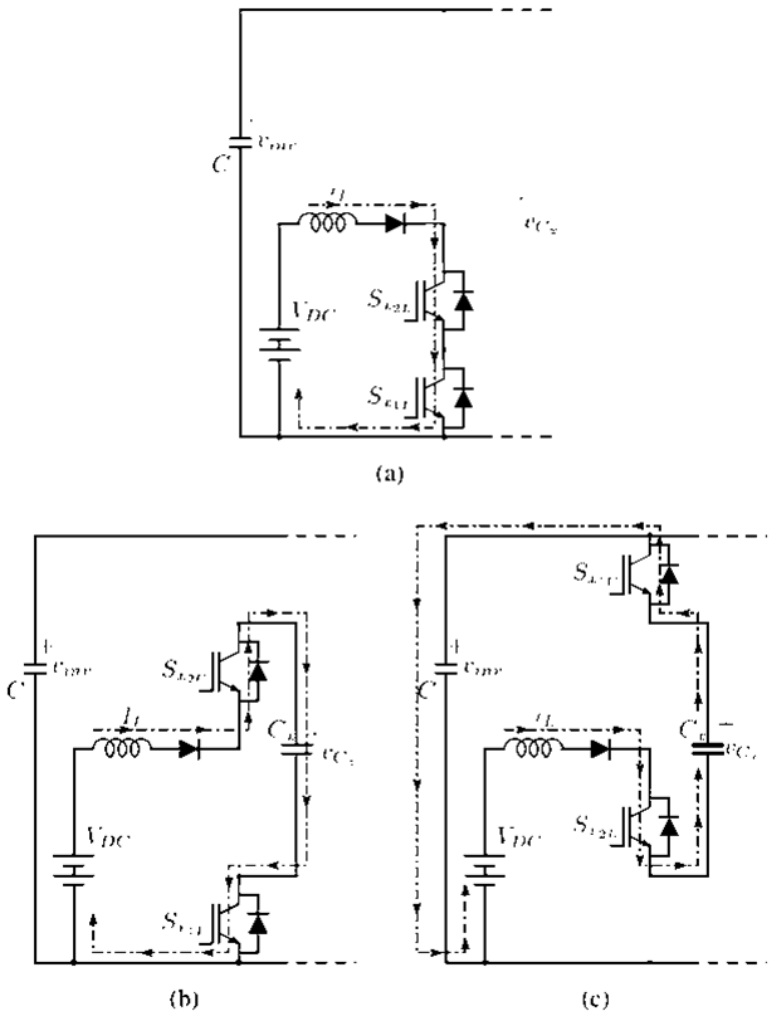

Figure2.25 Charging and discharging of inductor

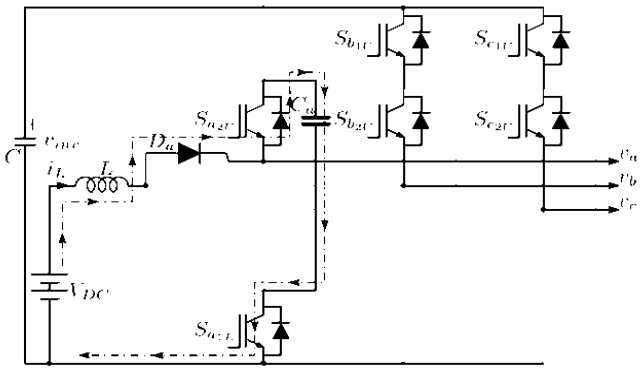

Figure 2.25: SSI FC inductor discharging-phase

2.1.3 Cascaded Multilevel Inverter

The cascaded multilevel inverter is the most applied inverter in both research and industry. This topology is derived by connecting more than two single-phase H-bridge structure in series or parallel but the series connection is the most frequently use or preferred choice. However, the word cascaded has being employed in both flying capacitor and neutral point topologies to describe the series connection of these basic units to provide a cascaded topology. Cascaded H-bridge topology is the conventional cascaded topology (Babaei & Hosseini, 2009). The Fig. 2.2 & 2.6 shows a cascaded H-bridge topology for a single phase system. This topology has two units H-bridge structures and its capable of producing 5-levels output voltage. In other to increase the number of stepped output voltage, the H-bridge units need to be increased. Tenconi et al., (1995). In their comparative investigation of the cascaded H-bridge and the conventional MIL topologies FC and NPC shows that, the cascaded topology is much simpler in both control mechanisms and topology structure. Unlike the FC and NPC, the cascaded topology does not require clamping elements of diodes for the NPC and capacitors for the FC structure. Eliminations of these components minimize the number of components and reduces the structure of the topology. The FC topology and NPC topology have many similarities but differ in the component used for voltage clamping. They also share similar disadvantage of complex structure for high levels of load voltages and very difficult control techniques when higher steps of load voltages are desired.

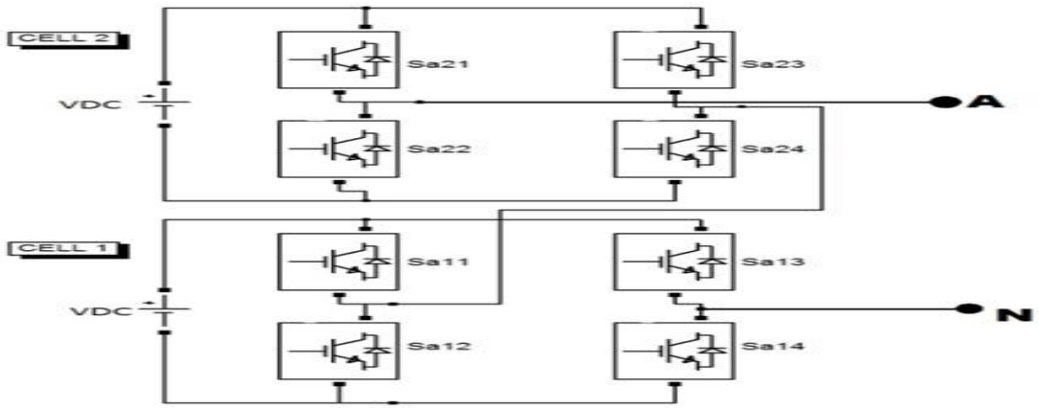

Figure 2.26: Cascaded HB inverter (19)

Table 2.3: 5-level cascaded converter (19)

S_a21	S_a23	S_a22	S_a24	S_a11	S_a13	S_a12	S_a14	V_A	V_N	V_o
1	0	0	1	1	0	0	1	+E	+E	+2E
1	0	0	1	1	1	0	0	+E	0	+E
1	0	0	1	0	0	1	0	+E	0	+E
1	0	0	1	0	1	1	0	+E	-E	0
1	1	0	0	1	0	0	1	0	+E	+E
1	1	0	0	1	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
1	1	0	0	0	1	1	0	0	-E	-E
0	0	1	1	1	0	0	1	0	+E	+E
0	0	1	1	1	1	0	0	0	0	0
0	0	1	1	0	0	1	0	0	0	0
0	0	1	1	0	1	1	0	0	-E	-E
0	1	1	0	1	0	0	1	-E	+E	0
0	1	1	0	1	1	0	0	-E	0	-E
0	1	1	0	0	0	1	0	-E	0	-E
0	1	1	0	0	1	1	0	-E	-E	-2E

The cascaded H-bridge topology has a relatively simple topology and its cascaded structure is of modularity form, these are the critical advantages with respect to the topology structure (Babaei, 2008). Other advantage of this topology is the possibility or capability of generating much higher stepped voltages. The control of the presented cascaded topology is shown by Table 2.3. All possible stepped output voltages are shown in this table. The

basic unit of the cascaded H-bridge contains four semiconductors and its control is performed by simultaneously gating diagonal switches for either positive or negative polarity voltage, zero voltage can be produced by simultaneously gating the lower or upper switches.

The H-bridges applied in the cascaded connection requires individual voltages thereby increasing the cost of the system. This limitation is of no longer concern because the rapid deployment of renewable energy sources such as photovoltaic systems. The output and the number of used H-bridges are related by:

$$n_L = 2n_{HB} + 1 \qquad (2.23)$$

Table 2.4: Symmetrical and Asymmetrical Inverters

	Symmetrical Inverter	**Asymmetrical inverter**	
		Binary	Trinary
Stepped output voltage	$2n + 1$	$2^{n+1}-1$	3^n
DC source quantity	N	N	N
Switches quantity	$4n$	$4n$	$4n$
Peak output voltage	N	$2n - 1$	$\frac{3^n - 1}{2}$

There are two types of cascaded H-bridge MIL, these types are symmetric and asymmetric cascaded H-bridge. These two topologies are equal with respect to the inverter structure, they have the same number components. The dc sources are equal; the semiconductor switches are also equal. However, they differ with respect to the magnitude of the voltage sources for each unit of the cascaded structure. Using Fig. 2.26 as case study, if the value of the input voltage of cell 1 is equivalent to that cell 2, then this topology is classified as symmetric but if there are difference in the magnitude of the input voltage of these cell units then they are classified as asymmetric topology. Asymmetric topologies are further classified according these groups; binary and trinary. Table 2.4 shows the mathematical

relationship existing between these categories of cascade H-bridge inverter (Babaei, 2008), (Babaei & Moeinian, 2010), & (Babaei & Hosseini, 2009).

A novel structure of cascaded MIL is presented by (Babaei et al., 2014). By improving the structure of the traditional H-bridge topology yields this presented topology. The basic circuit structure of this topology is given Fig. 2.28. There are two voltage sources of this topology and six power switches, all the switches in the H-bridge are unidirectional from the voltage perspective. Five stepped output voltage can be generated by this topology. The possible magnitude of output voltages are $0,\ \pm V_1,\ \pm\ (V_1 +\ V_2)$. The output waveform of this topology is shown by Fig. 2.27.

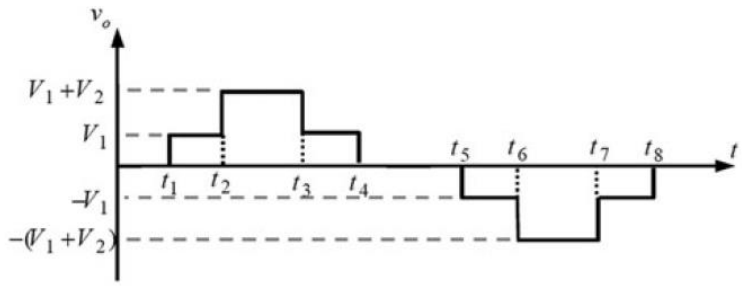

Figure **2.27:** Output voltage (23).

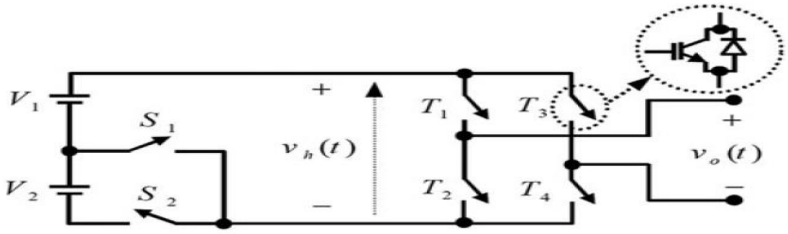

Figure **2.28:** Basic structure of cascaded MI (23).

Utilizing the basic structure of Fig. 2.28, the cascaded topology is produced by connecting the basic structure in series, the cascaded topology is illustrated by Fig. 2.29. Multiple control algorithms were presented to produce the desired stepped load. The relationship between the number of applied basic unit (x) and other parameters such switches, dc sources, levels are expressed by (2.24) to (2.28).

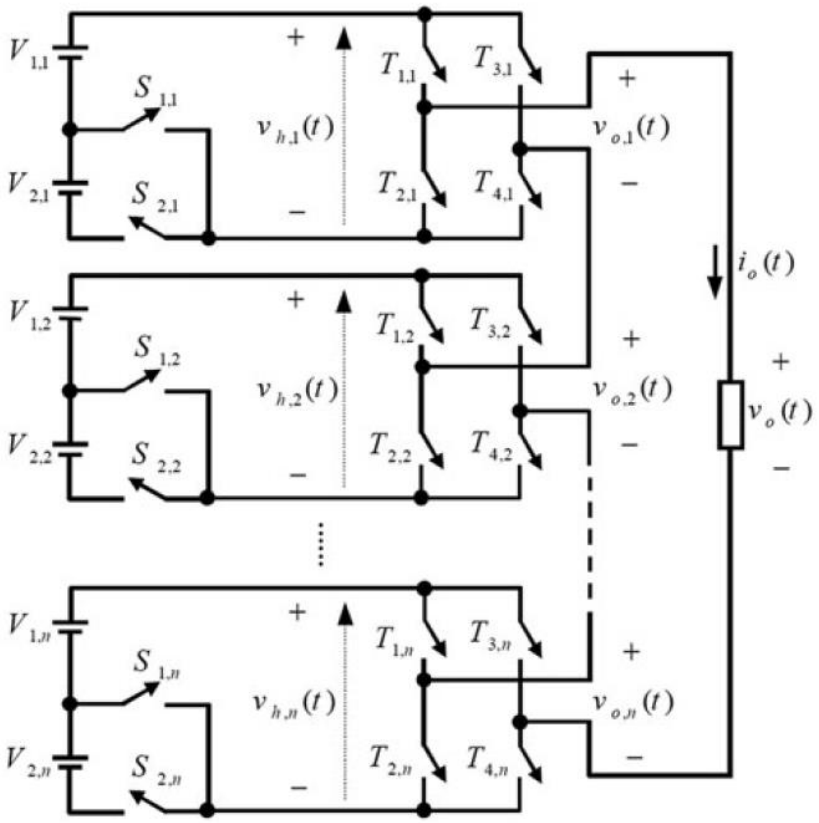

Figure 2.29: Cascaded MI (23).

$$\text{Switches number} = 6x \tag{2.24}$$

$$\text{DC source number } = 2x \tag{2.25}$$

$$\text{Level number } = 2^{x+1} - 3 \tag{2.26}$$

$$\text{Peak output voltage} = (2^{x+1} - 2)\text{V}_{\text{dc}} \tag{2.27}$$

$$\text{Blocking voltage} = 10(2^{x} - 1)\text{V}_{\text{dc}} \tag{2.28}$$

A new cascaded crisscross inverter is presented by (Arun & Noel, 2018). As illustrated in Fig. 2.30. This present to utilize fewer number of components, minimum voltage stress and good structure modularity. Analysis of the presented topology is investigated for both asymmetric and symmetric conditions. The crisscross topology is derived from half H-bridge structure and crisscrossed switches. The presented topology consists of four dc sources, ten switches and capable of producing nine levels of load voltage.

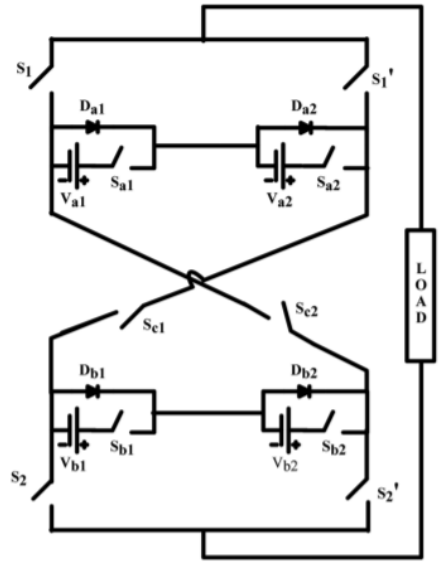

Figure 2.30: Crisscross cascaded MIL (24).

Fig. 2.31 shows the operating states of the presented topology. Fig. 2.31a generates positive and negative V_{a1} output voltage, Fig. 2.31 produces positive and negative values $(V_{a1} + V_{a2} + V_{b1})$. The inverter power losses are presented below as:

$$P_{COND,G} = \frac{1}{2\pi}\int_0^{2\pi} P_{CON,G}(t)d\omega t \quad (2.29)$$

Where $P_{CON,G}$ is given by:

$$P_{CON,D}\,(t) = \left[\, R_D I^{\beta}\,(t\,) + V_{ON,G}\,(t)\right] I\,(t) \quad (2.30)$$

Where $P_{CON,D}$ is given by:

$$P_{\,COND,D} = \frac{1}{2\pi}\int_0^{2\pi} P_{CON,D}\,(t)\,d\omega t \quad (2.31)$$

$$P_{\,SW} = \frac{1}{T}\left[\,\left(\,E_{\,ON} + E_{\,off} + E_{\,rec}\,\right)\right] \quad (2.31)$$

$$E_{\,ON} = \frac{1}{6} I V_{sw}\, t_{\,ON} \quad (2.32)$$

$$E_{\,off} = \frac{1}{6} I V_{sw} t_{\,off} \quad (2.33)$$

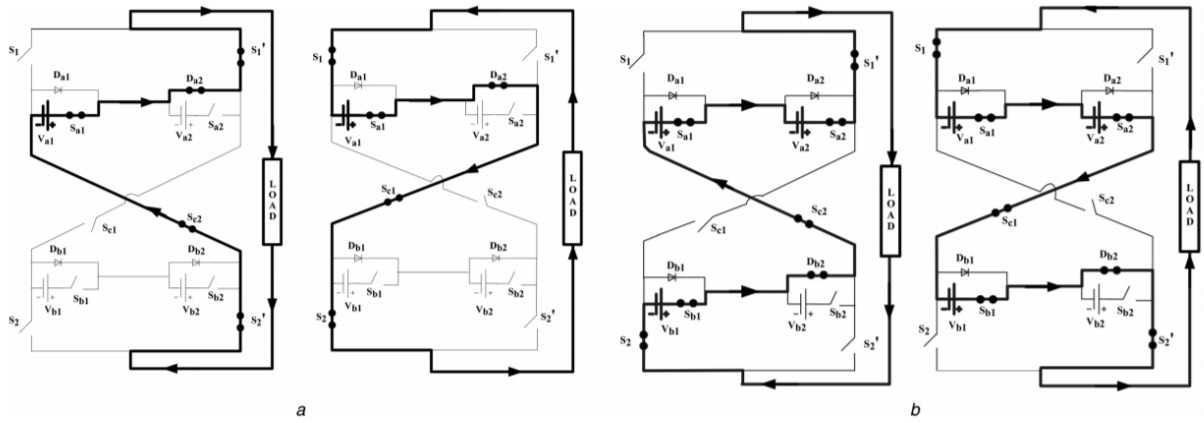

Figure 2.31: Operating states of the crisscross inverter (24)

A cross-switched cascaded MIL is presented by (Kangarlu, Babaei, Sabahi, 2013). Which was reviewed under both categories of cascaded MIL; symmetric and asymmetric. The present characteristics of the topology under symmetric conditions are reduced standing voltage, minimum component number and application of charge balance control method. Under asymmetric characteristics analysis, the presented topology produces the highest stepped voltage as compared to the symmetric conditions, the standing voltage is equivalent to the symmetric value.

A novel cascaded MI under symmetric and asymmetric investigation is presented by (Babaei, Laali, & Bahravar, 2015). Under symmetric condition, the presented topology is suitable for charge balance control method and most importantly reducing the component count. The standing voltage of the topology is not maximised under this condition. The fundamental structure is represented by Fig. 2.32 while the cascaded topology is shown by Fig.2.33. the fundamental structure is composed ten switches from which six switches are connected in the cross-switched form, there are four dc sources in this topology.

The mathematical relationship exiting the various structure parameters are expressed below. N_{dc} is dc voltage number, $N_{stepped}$ is the level number, $N_{switches}$ is the switch number and the standing voltage is expressed by $N_{standing}$.

$$N_{swicthes} = 2mn + 2m \tag{2.34}$$

$$N_{standing} = 4mnV_d \tag{2.35}$$

$$N_{dc} = mn \tag{2.36}$$

$$N_{stepped} = 2mn + 1 \quad (2.36)$$

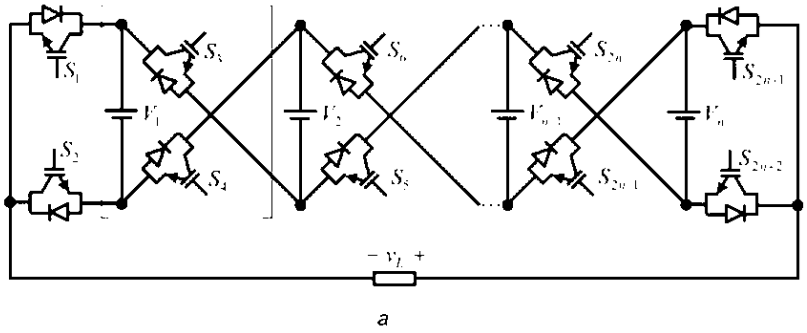

Figure 2.38: Common structure (25)

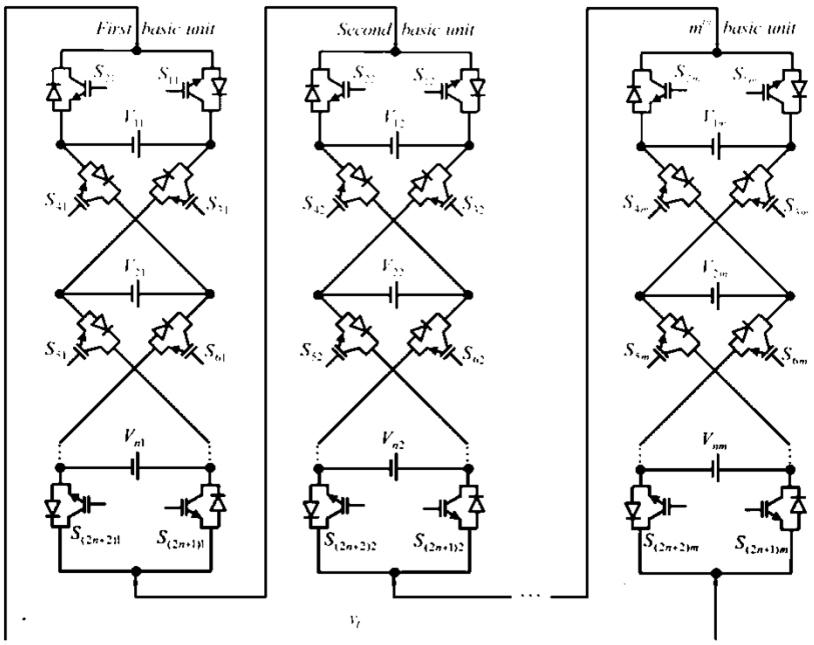

Figure 2.39: Cascaded topology (25).

A new cascaded MIL is presented by (Yahya, Usman Ali, & Ghani, 2019). The major characteristics of the presented topology is the excellent application of the dc source, reduced switching losses and application of fewer number of components such as switches. Juxtaposing this topology to the conventional H-bridge shows that the presented topology produces twice the number of stepped voltage, also it has modular structure and the used switches are all rated equally hence control and circuit structure are less complex. The

basic structure is shown by Fig. 2.40. There are four switches constituting the H-bridge structure while the remaining structure has one unidirectional switch and three bidirectional switch, also the input sources are four. The H-bridge is employed to produce either positive or negative polarity. Symmetric and asymmetric analysis of the presented topology is provided.

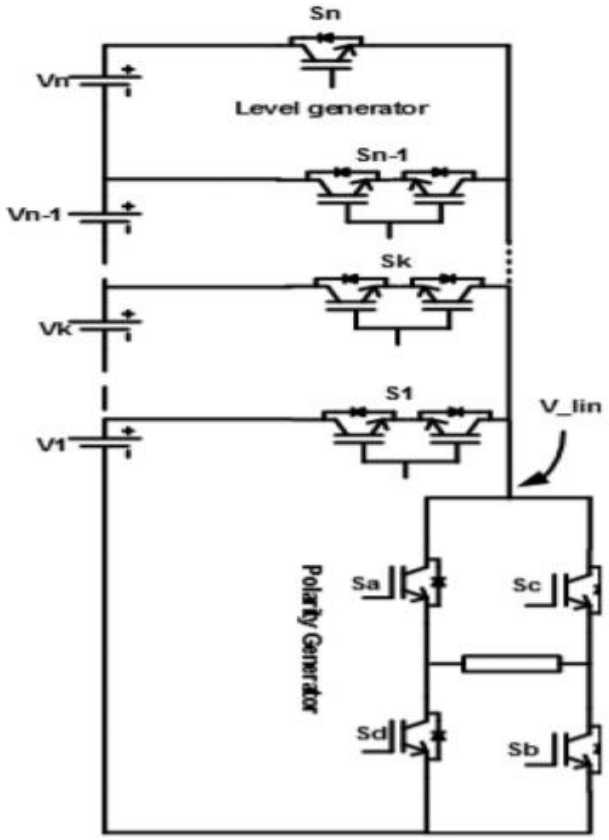

Figure 2.40: Basic structure

$$\begin{cases} V_{o,max} = (2n-1)V_{dc} \\ N_{step} = 4n-1 \\ N_{IGBT} = 2n+4 \\ N_{switch} = N_{driver} = n+6 \end{cases} \quad (2.37)$$

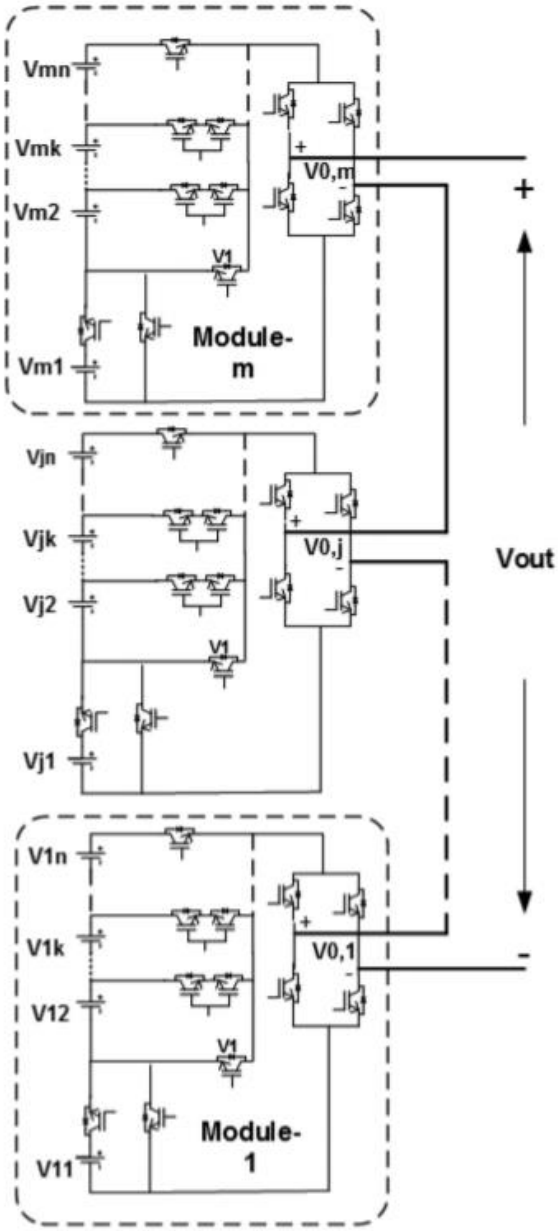

Figure 2.41: Cascaded topology

2.1.4 Stacked Multicell Multilevel Inverter

Stacked multicell converter (SMC) was presented by (Gateau, Meynard, & Foch, 2001). These are categories of multilevel inverters designed specifically for high power applications of 50MW and above and also application in DC medium power systems of 150kV peak value. SMC are described as hybrid topologies developed from the combination of commutations cells. SMC provides the capabilities of voltage constraint

sharing on multiple commutation cells and also application of lower rated switches because the input voltage is split into several fractions. Also the SMC boast of optimal dynamic performance because of increased stepped output voltages and proliferation of chopped frequency voltage. Finally, in the SMC, the flying capacitor volume numbers are drastically reduced, as presented by (Gateau et al., 2001). The structure of the SMC topology is shown by Fig. 2.42. This topology is of 3x2 nature. From this structure the number of columns is expressed by $p = 3$ and the number of stacks is expressed by $n = 2$. From the above data, the following expression are developed:

$$\text{Commutation cells } (\mathrm{p} \times \mathrm{n}) \tag{2.38}$$

$$\text{Flying capacitors } (\mathrm{p} - 1) \times \mathrm{n} = 4 \tag{2.39}$$

The capacitor voltage is given below where *i* is the cell number and *E* is the input voltage.

$$\text{Capacitor voltage} \mathrm{V_C} = \mathrm{i}\frac{\mathrm{E}}{\mathrm{p}} \tag{2.40}$$

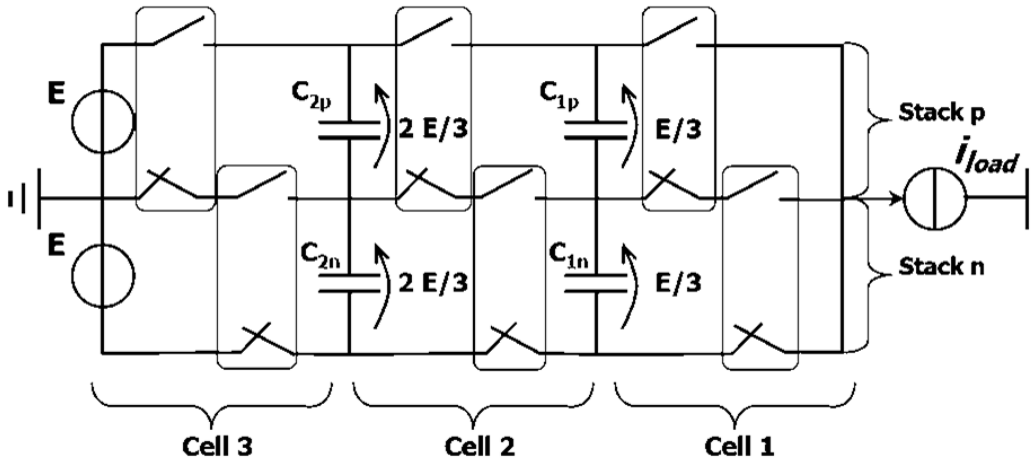

Figure 2.42 : Stacked Multicell converter

The semi conductors in the commutation are gated in a complementary fashion where the gate signals are noted with regard to the commutation cell. The control of the SMC converter is dependent on the required polarity of output voltage. If positive magnitude of output voltage is desired, the upper switches are gated on whiles the lower switches are gated on negative voltage is required, these state are illustrated by Fig. 2.43a and Fig. 2.43b respectively.

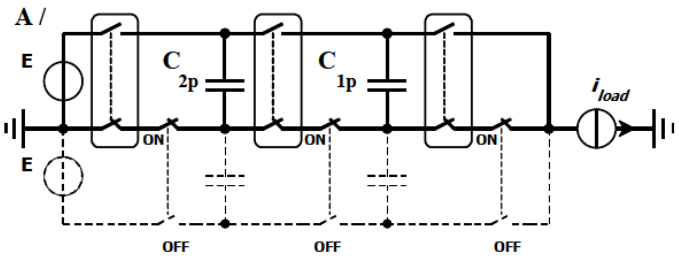

Figure 2.43a: SMC operational circuit

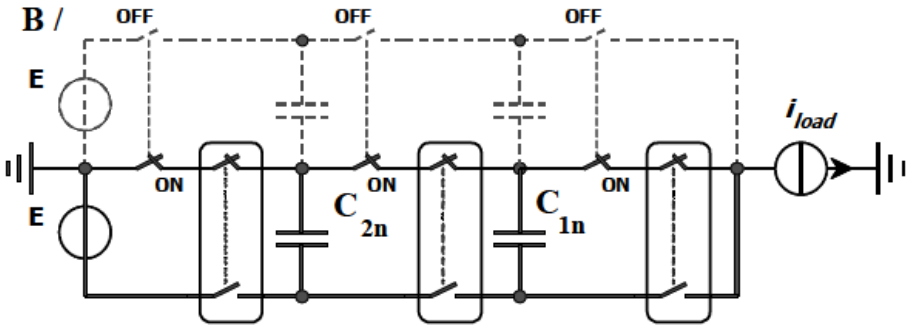

Figure 2.43b: SMC operational circuit

A reduced SMC topology applied a single dynamic voltage restorer (DVR) is presented by (Sadigh, Dargahi, Corzine, 2016). The main function of the reduced SMC in the DVR is to limit the fault current and also voltage compensator. Reduced SMC is the most advance topology amongst the family of SMC and has the following advantages reduced flying capacitor quantity which directly affects the converters cost and size. Fig. 2.44 shows the presented SCM (2x2) and Fig. 2.45 shows the DVR topology

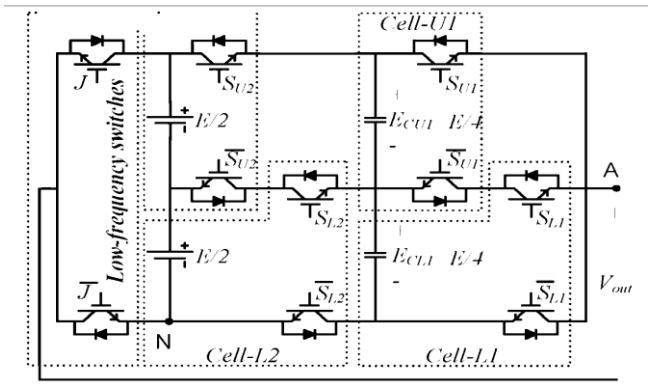

Figure 2.44: Stacked multicell converter

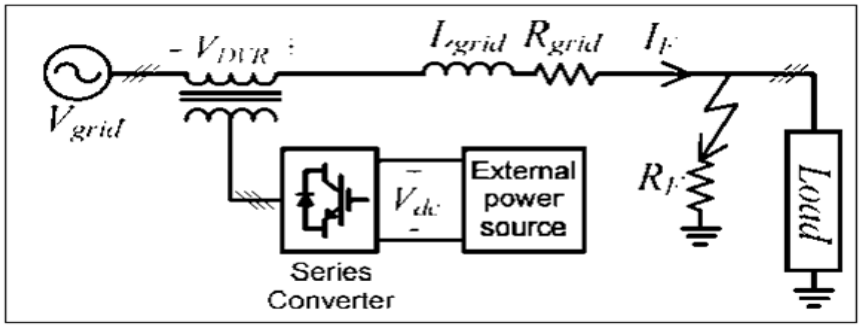

Figure 2.45: Single-phase DVR

A new voltage balancing technique for the SMC is presented by (Ghais, Pou, Agelidis, Ciobotaru., 2013). Where phase shift PWM method is applied. This new control method increases the stepped output voltage and it has a simple implementation technique. Proportional controller is employed in altering the duty cycle so that the voltages in the SMC can be balanced. Crossed effect which exists between the duty cycle and capacitor current is applied in efficient SMC voltage balancing. Fig.2.46 shows the three-phase SMC and each phase has 12 semiconductor switches and four capacitors. The corresponding phase shift PWM reference signal and output voltage waveforms are also indicated.

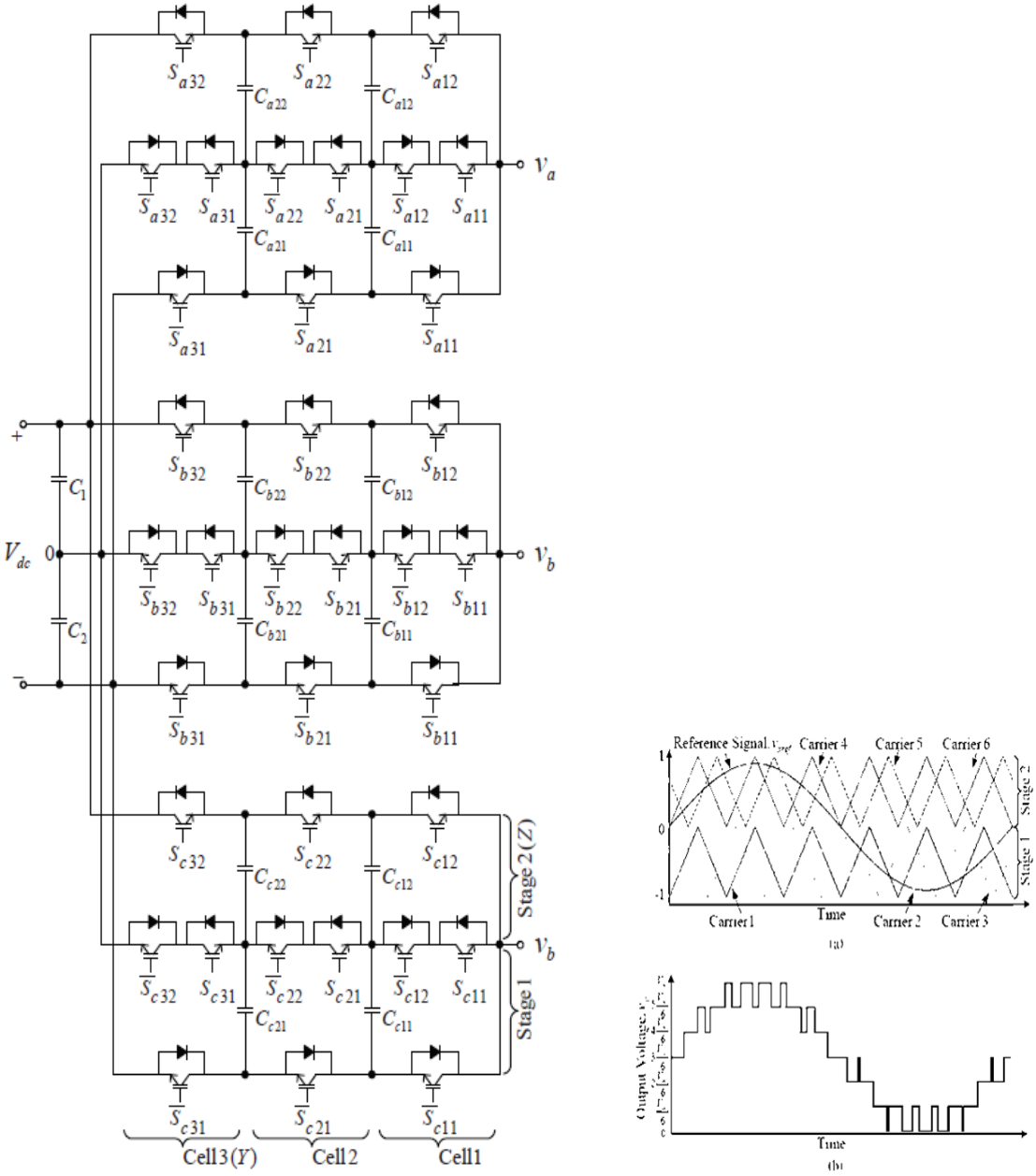

Figure 2.46: SMC with it reference signal and output voltage waveform

A hybrid SMC converter is presented by (Zhang, Xu, Hu, & Zhu, 2019). Which is one of the most sought after converters where high efficiency with low voltage applications are desired. Application of the appropriate modulation provides stepped output waveforms with high quality and also a converter with minimum power losses. Hence phase shift PWM technique is applied. Fig. 2.47 shows the presented hybrid SMC with 9-stepped output functionality. The hybrid topology is a combination an SMC and a half bridge inverter.

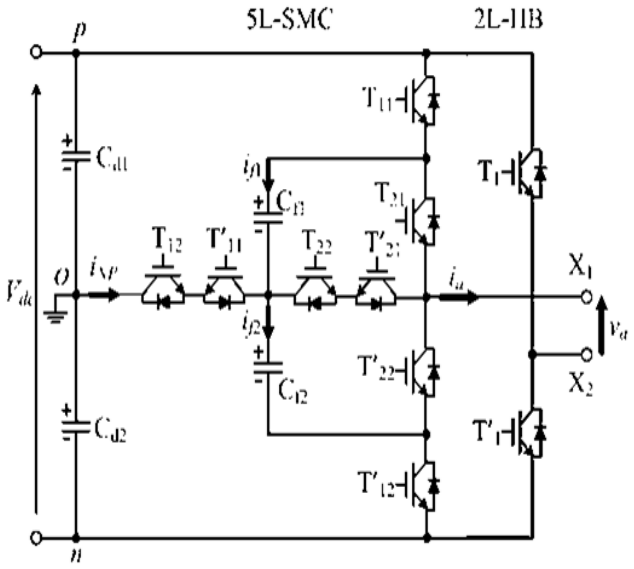

Figure 2.47: Hybrid SMC

TABLE CHAPTER

TABLE 1. Switching states, output voltage and effects on FCs.

States	LF cell	HF cell	Output voltage	NP current	FC current		FC voltage	
	T_2	$T_{11}T_{12}T_{21}T_{22}$	v_a	i_{NP}	i_{f1}, i_{f2}		v_{f1}, v_{f2}	
V_1	0	1 1 1 1	V_{dc}	0	0	0	n	n
V_2	0	1 1 0 1	$3V_{dc}/4$	0	i_a	0	↑	n
V_3	0	0 1 1 1	$3V_{dc}/4$	i_a	$-i_a$	0	↓	n
V_4	0	0 1 0 1	$V_{dc}/2$	i_a	0	0	n	n
V_5	0	0 0 1 1	$V_{dc}/2$	0	$-i_a$	$-i_a$	↓	↓
V_6	0	1 1 0 0	$V_{dc}/2$	0	i_a	i_a	↑	↑
V_7	0	0 1 0 0	$V_{dc}/4$	i_a	0	i_a	n	↑
V_8	0	0 0 0 1	$V_{dc}/4$	0	0	$-i_a$	n	↓
V_9	0	0 0 0 0	0	0	0	0	n	n
V_{10}	1	1 1 1 1	0	0	0	0	n	n
V_{11}	1	0 1 1 1	$-V_{dc}/4$	i_a	$-i_a$	0	↓	n
V_{12}	1	1 1 0 1	$-V_{dc}/4$	0	i_a	0	↑	n
V_{13}	1	0 1 0 1	$-V_{dc}/2$	i_a	0	0	n	n
V_{14}	1	1 1 0 0	$-V_{dc}/2$	0	i_a	i_a	↑	↑
V_{15}	1	0 0 1 1	$-V_{dc}/2$	0	$-i_a$	$-i_a$	↓	↓
V_{16}	1	0 0 0 1	$-3V_{dc}/4$	0	0	$-i_a$	n	↓
V_{17}	1	0 1 0 0	$-3V_{dc}/4$	i_a	0	i_a	n	↑
V_{18}	1	0 0 0 0	$-V_{dc}$	0	0	0	n	n

The current and voltage are given assuming i_a>0 with the notations:
"↓" represents capacitor discharging, "↑" represents capacitor charging,
"n" represents no influence on the flying capacitors.

The switching pattern of the presented converter is shown by Table 1 and the operational states the converter as well as the current paths is given by Fig. 2.48. The ac load voltage is expressed below by (2.41) where $a, b, c \; and \; d$ are switching functions of the SMC switches.

$$v_a ba.V_{dc} + \frac{1}{4}V_{dc}(a + b + c + d) \tag{2.41}$$

The flying capacitor's reference values are given by:

$$V_{fk1} = (n - k + 1)\frac{V_{dc}}{2n} \tag{2.42}$$

$$V_{fk2} = (n - k + 1)\frac{V_{dc}}{2n} \tag{2.43}$$

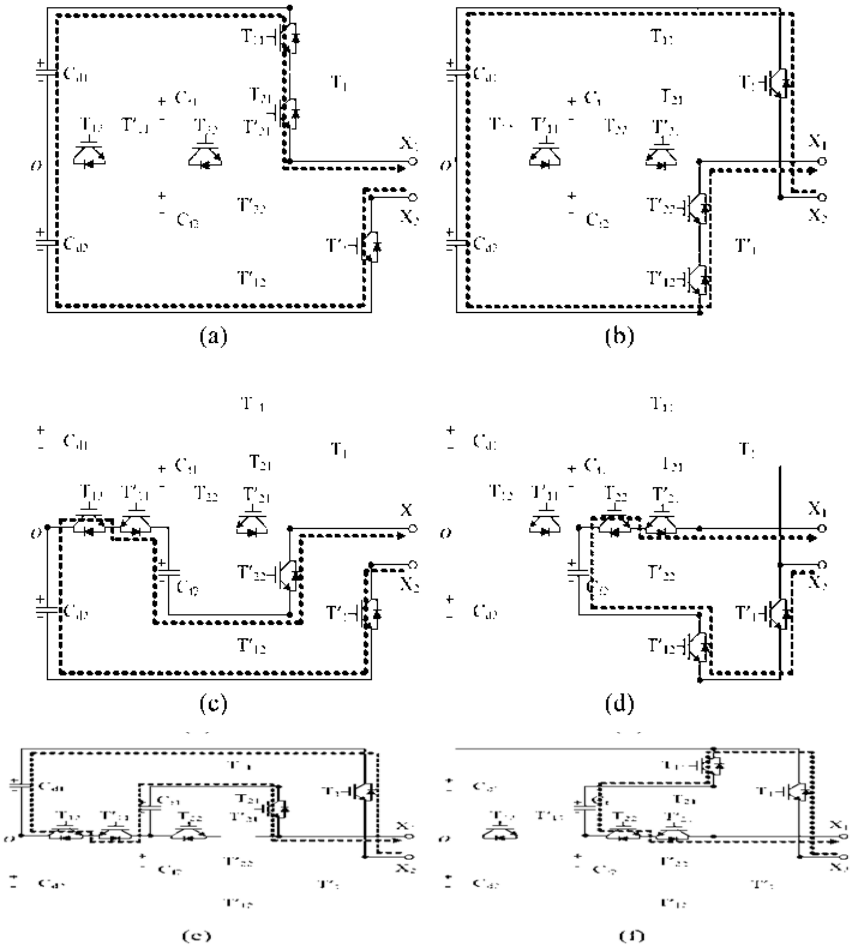

Figure 2.48: Operational states of hybrid SMC

A proposed SMC where elimination of one dc voltage is desired is presented by (Khoshkbar Sadigh, Dargahi, Shoulaie, & Pahlavani, 2012). By reducing the dc voltage quantity, the cost of the converter is minimized and also the size of the converter is also reduced. The voltage quantity is achieved by including semiconductor switches of low frequency characteristics. The one voltage SMC is presented by Fig. 2.49.

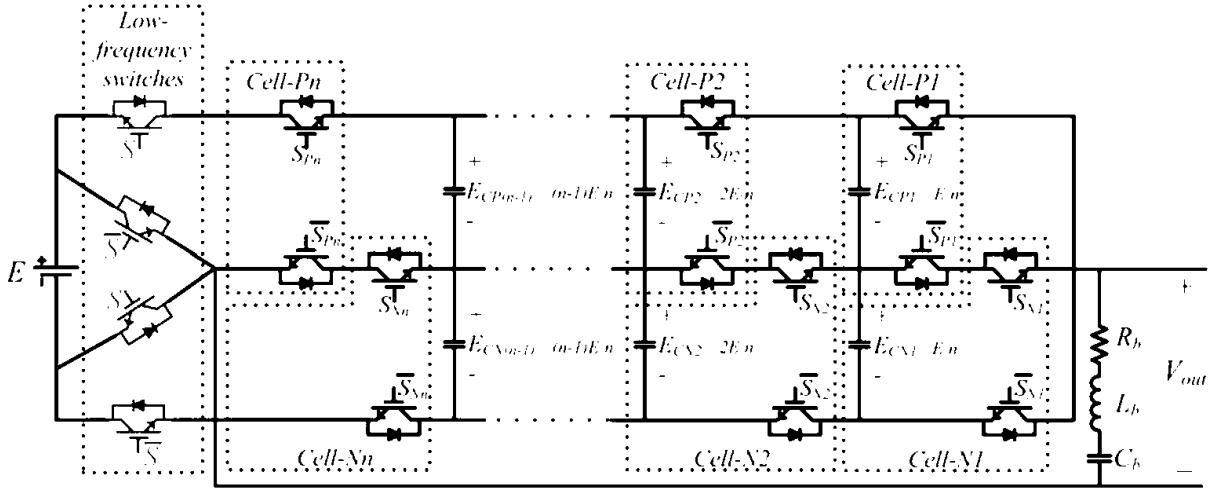

Figure 2.49: One voltage SMC

$$\frac{1}{2\pi f_{sw}} = \sqrt{L_b C_b} \qquad (2.44)$$

A new hybrid SMC is presented by (Banaei, Kazemi, & Oskuee, 2013). Which has the capability of producing maximum stepped voltages by employing less number of semiconductor switches. This hybrid topology is made up of three converters; the conventional SMC, full and half H-bridges. Fig. 2.50 shows the presented topology.

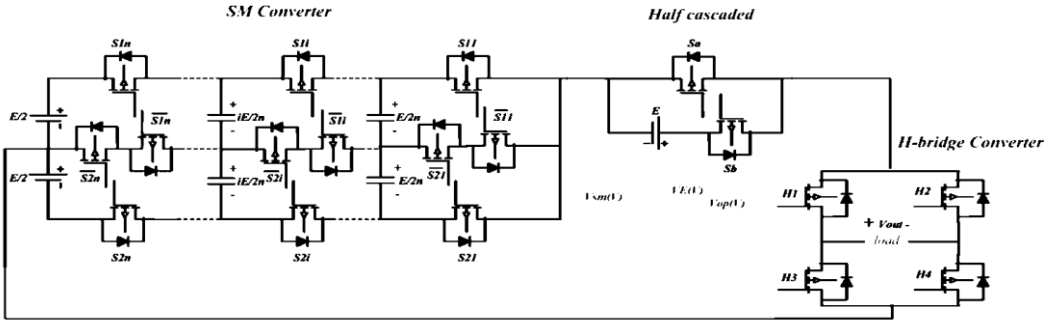

Figure 2.50: Hybrid SMC

$$9m = 8n + 1 \qquad (2.45)$$

F $$V_{o,rms} = \sqrt{\frac{1}{T}\int_0^T V_0^2(t)dt} \quad (2.46)$$

$$V_{op} = V_E + V_{SM} \quad (2.47)$$

A back to back SMC which is derived by two connecting conventional SMC together using low frequency switches is presented by (Hosseinzadeh, Babaei. Sabahi, 2012). This topology generates higher levels of voltage by using much fewer semiconductor switches and also minimizes the overall converter power losses. The power circuit of the proposed converter is given by Fig. 2.51. The following equations govern the presented converter:

$$N_{cell} = 2n + 2m \quad (2.48)$$

$$N_{level} = 2[(n+1)(2m+1)] - 1 \quad (2.49)$$

$$N_{level} = \frac{(N+2)^2-2}{2} \quad (2.50)$$

$$E_a = \frac{2n(2m+1)}{(2n+1)(2m+1)-1} \quad (2.51)$$

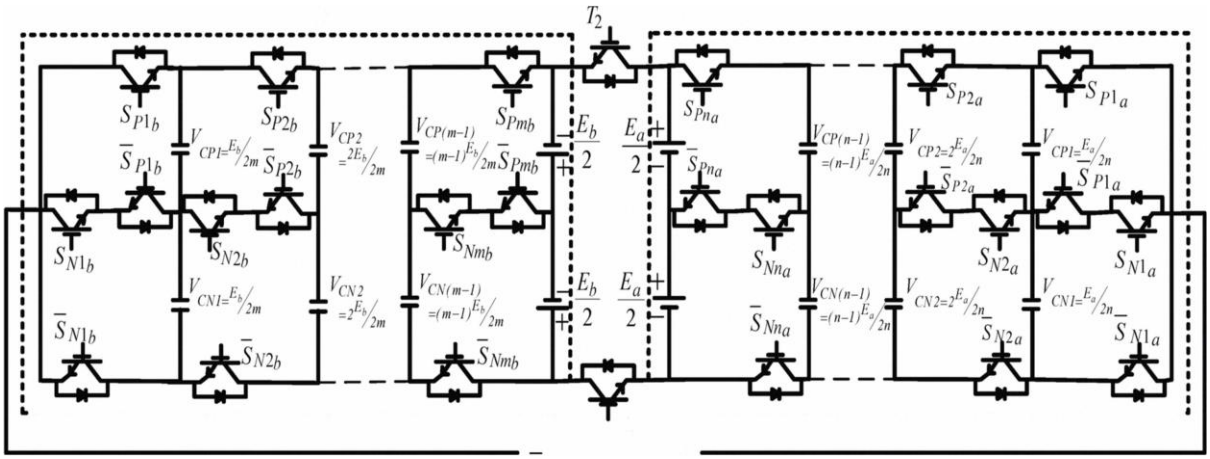

Figure 2.52 : Back to back SMC

$$Ev = E - E_a \tag{2.52}$$

$$V_c = \frac{iE}{n} \tag{2.53}$$

A new topology of SMC referred to as Mixed SMC is presented by (Sadeghi, Hosseini, Alizadeh, & Nikar, 2012). This converter is capable of doubling the stepped voltages and also well as doubling the rms voltage. The frequency spectrum is also improved drastically, lower rated switches are utilized and finally reduced converter losses. These advantages derived when the mixed SMC is compared to the conventional topologies in this family. All these merits are possible by adding semiconductor switches to the conventional SMC topology. Fig. 2.53 shows the presented mixed SMC power circuit.

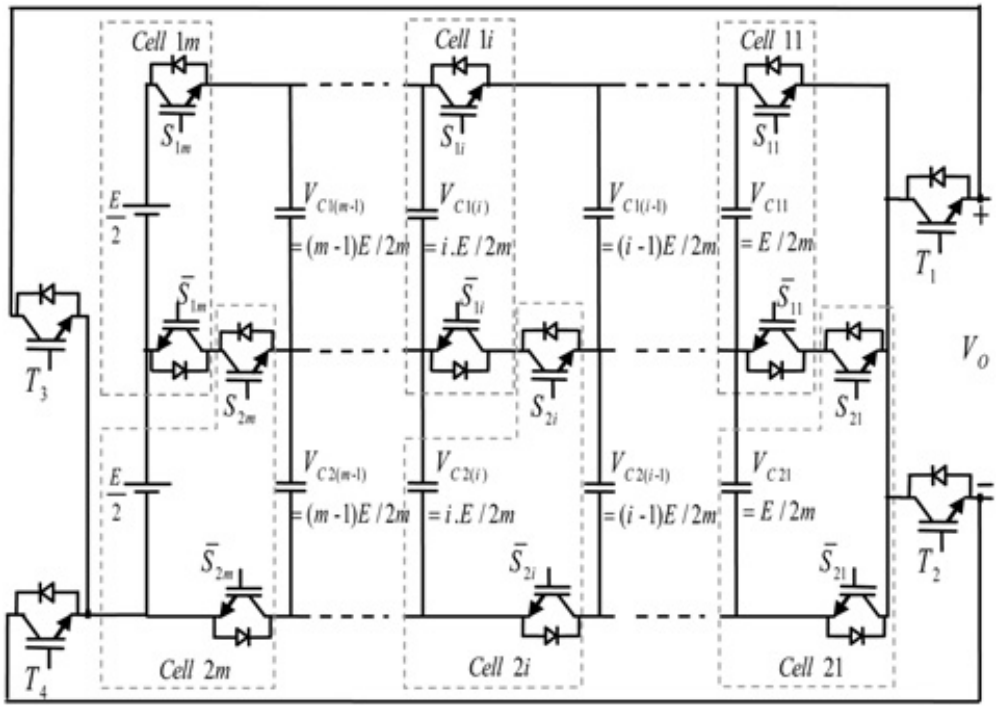

Figure 2.53: Mixed SMC

2.3 Conclusion

A review of selected multilevel inverter topologies was investigated in this section of the thesis. Multilevel inverters are capable generating levels of load voltage and are suitable for industrial applications due to the multiple advantages it can boast off. The conventional multilevel inverters are the cascaded H-bridge, the flying capacitor and neutral point clamped and various multicell topologies. These conventional topologies boast of individual advantages and disadvantages as such are suitable for specific application. However, multilevel inverters in general are suitable for application in renewable energy systems, electric vehicle charging, electric drives, various compensators, FACTS, HVDC, small medium and high power systems.

CHAPTER 3

PRESENTED TOPOLOGY AND SIMULATION RESULTS

3.1 Introduction

Multilevel inverters are revolutionary inverters which have changed the inverter industry both in the topology structure and control and also the application of inverter. Several improvements have been made in the topology structure and also control techniques. In the case of topological structure, application of the least possible devices especially semiconductor switches are the major point of concern for research because minimizing these components reduces the inverters power loss. The conventional topologies of Diode Clamped topology, Flying Capacitor topology and the Cascade H-Bridge topology are still being utilized in industry or they are the bedrocks from which new topologies are developed. Among the family of multilevel inverters is the stacked multicell converter (SMC).

Per the explanation in chapter two, the SMC are designed specifically for high power applications of 50MW and above and also application in DC medium power systems of 150kV peak value. SMC are described as hybrid topologies developed from the combination of commutations cells (Gateau et al., 2001). This type of SMC provides the capabilities of voltage constraint sharing on multiple commutation cells and also application of lower rated switches because the input voltage is split into several fractions. Also the SMC boast of optimal dynamic performance because of increased stepped output voltages and proliferation of chopped frequency voltage. Finally, in the SMC, the flying capacitor volume numbers are drastically reduced as described and presented by (Gateau et al., 2001). The structure of the SMC topology is shown by Fig. 2.42. This topology is of 3×2 nature. From this structure the number of columns is expressed by $p = 3$ and the number of stacks is expressed by $n = 2$. From the above data, the following expression are developed:

$$\text{Commutation cells } (\mathrm{p} \times \mathrm{n}) = 6 \tag{3.1}$$

$$\text{Flying capacitors } (\mathrm{p} - 1) \times \mathrm{n} = 4 \tag{3.2}$$

The capacitor voltage is given below where *i* is the cell number and *E* is the input voltage.

$$\text{Capacitor voltage } V_C = i\frac{E}{p} \tag{3.3}$$

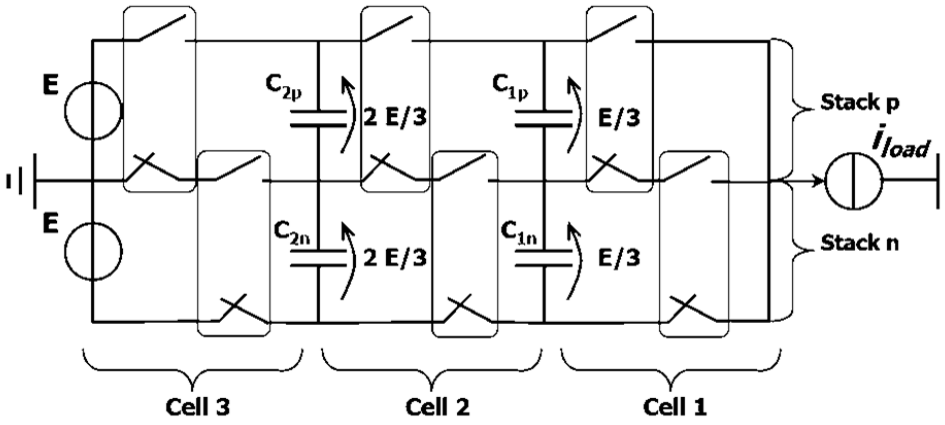

Figure 3.1: Stacked Multicell converter

3.1.1 Presented Topology

The presented stacked multicell converter is illustrated by Fig. 3.3 and is mostly suitable for application in FACTS, HVDC, integration of various renewable energy sources such as PV systems and also energy storage systems into major grid and also suitable for application in custom devices for power compensations. The presented topology of SMC when compared to traditional SMCs possess the following advantages, reduced voltage sources to one, reduced components such as semiconductor switches, utilization of lower rated switches, reduced converter cost, less installation area required and reduced converter losses. Conventional SMC is composed of two structures of flying capacitor multilevel which are stacked onto each other, operating the upper and lower stacks independently will lead to the generation of positive and negative output voltages respectively. The presented topology of Fig 3.3 is derived by eliminating one power switch from the conventional topology of Fig. 3.2. This is possible because each voltage source is required during each half cycle.

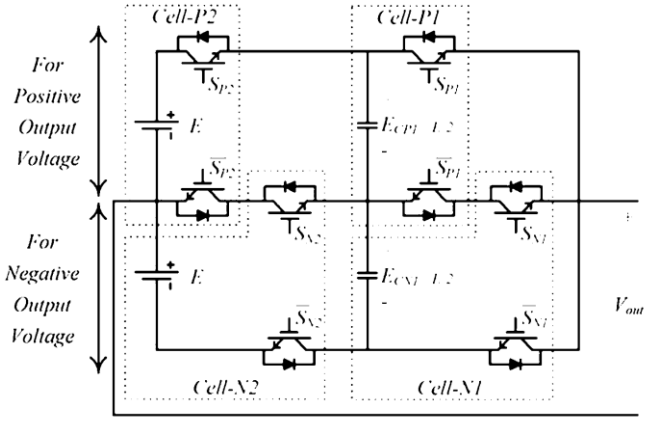

Figure 3.2: Two voltage source SMC

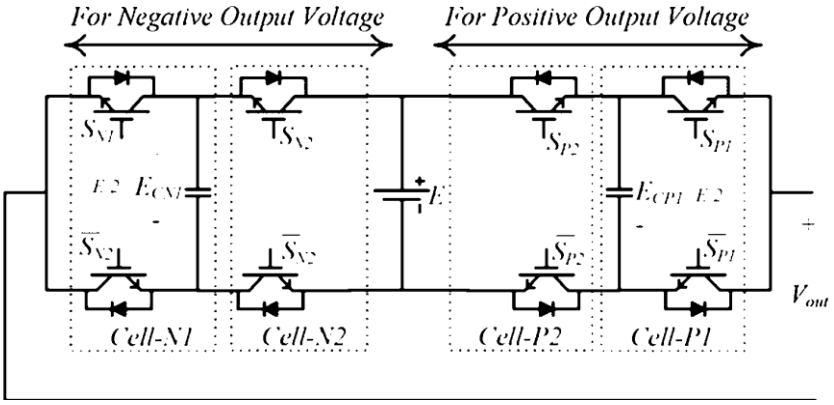

Figure **3.3:** Presented SMC topology

The presented five level 2×2 SMC is composed of one dc source, eight semiconductor switches and two capacitors. The dc source is positioned at the centre of the topology where its operation is based on switches before the dc source (left stack) and switches after the dc source (right stack). The switches before the dc source are gated to produce negative load voltage while the switches after the dc source are gated to produce positive load voltage. The capacitor energy (stored) for the presented topology is determined by:

$$U_{C_{N11}} = U_{C_{P11}} = \frac{1}{2} C \left(\frac{E}{2}\right)^2 \tag{3.4}$$

With four cells, the capacitor energy is determined by:

$$U_{T_{1\times4}} = C \left(\frac{E}{2}\right)^2 \tag{3.5}$$

The switching table of the presented topology is indicated by Table 3.1

Table 3.1: Switching Pattern

Switches		
Mode	$\{(\boldsymbol{S_{P2}}, \boldsymbol{S_{P1}}), (\boldsymbol{S_{N2}}, \boldsymbol{S_{N1}})\}$	**Output voltage**
1	$\{(1,1),(0,0)\}$	$+E$
2	$\{(1,0),(0,)\}$ $\{(0,1),(0,0)\}$	$+0.5E$
1	$\{(0,0),(0,0)\}$	0
2	$\{(0,0),(0,1)\}$ $\{(0,0),(1,0)\}$	$-0.5E$
1	$\{(0,0),(1,1)\}$	$-E$

The presented topology's structure can be extended to generate any desired level of load voltage by increasing the number of cell evenly, also the number of stacks can be increased or reduced. Fig. 3.4 shows $1 \times n$ cells of the SMC structure and its capacitor energy (stored) is determined by (3.6) where E and C are the dc source magnitude and capacitance value respectively.

$$U_i = \frac{1}{2} C \left(\frac{iE}{n}\right)^2 \quad i = 1, 2, \dots, n-1 \tag{3.6}$$

The total capacitor energy for SMC structure of Fig. 3.4 is expressed by:

$$U_{T_{1\times 2n}} = C\left(\frac{E}{2n}\right) \sum_{i=1,2,\dots}^{n-1} i^2 \tag{3.7}$$

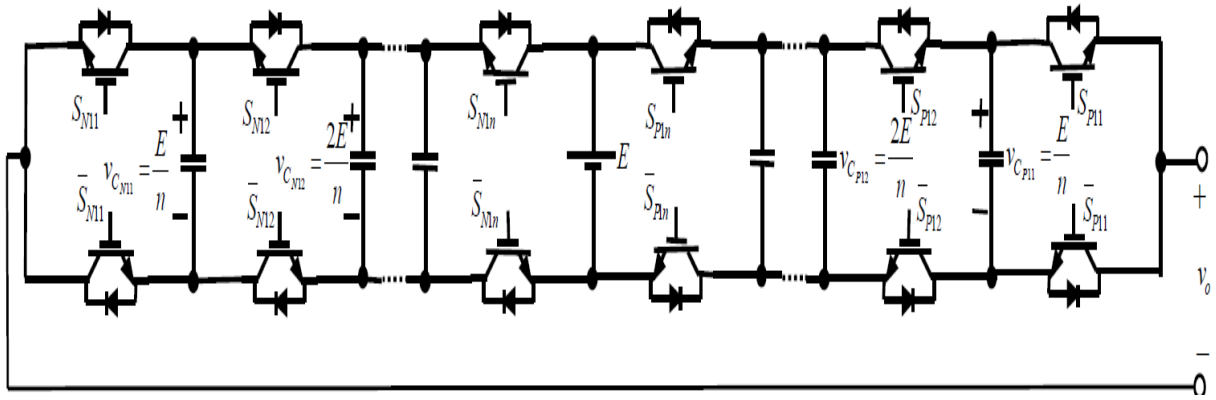

Figure 3.4: 1×4 SMC

Analysis of two stacks four cells SM converter is presented below. The structure of the 2×4 SMC converter is illustrated by Fig. 3.5 and its composed of eight commutation switches, one dc source, sixteen semiconductor switches and four capacitors. The source voltage is shared equally on the four capacitor by $\frac{E}{4}$. The stored capacitor energy for the 2×4 converter is determined by (3.8) when $i = 1, 2$.

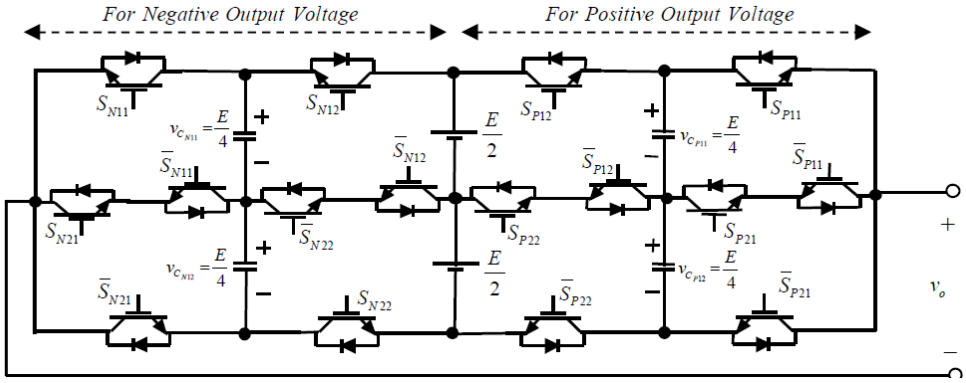

Figure 3.5: 2×4 SM converter

$$V_{T_{2\times4}} = 2C\left(\frac{E}{4}\right)^2 \tag{3.8}$$

The general equations governing stacked multilevel converter of $2 \times 2n$ structure is provided below utilizing Fig. 3.6. The number of cells of $2 \times 2n$ converter is expressed by;

$$N_{Cell,2\times2n} = 8n \tag{3.9}$$

The number of capacitor is determined by:

$$\text{N} = 4(1 - n) \tag{3.10}$$

The general voltage magnitude of the individual capacitors is determined by:

$$N_{Ckij,2\times 2n} = \frac{jE}{2n} \tag{3.11}$$

When $k = P, N \quad i = 1, 2 \quad j = 1, 2, \dots, n-1$

The stored capacitor energy is determined by:

$$U_{C_{kji},2\times 2n} = \frac{1}{2} C \left(\frac{jE}{2n}\right)^2 \tag{3.12}$$

When $k = P, N \quad i = 1, 2 \quad j = 1, 2, \dots, n-1$

The total stored capacitor energy is given by:

$$U_{T,2\times 2n} = C \left(\frac{E}{2n}\right)^2 \sum_{j=1,2,..}^{n-1} j^2 \tag{3.13}$$

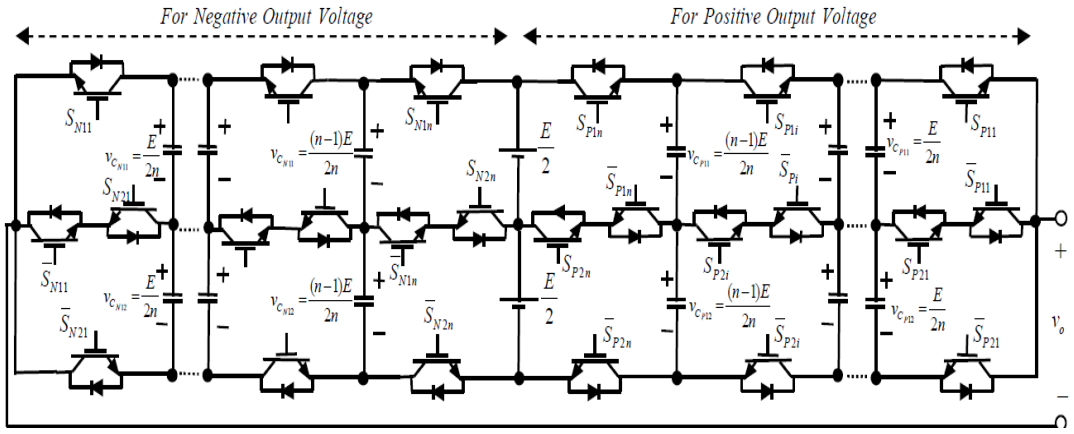

Figure 3.6: 2 × 8 SM converter

3.1.2 Simulation Results

Simulation results for the presented stacked multicell converter will be generated for five different topologies of the same converter. The difference in the various topologies is a variation in the number of stacks as well as the number of cells. The number of stacks will be increased from an initial number of one to a maximum number of four whiles the number of cells will be increased from an initial number of four to the highest number of eight. These results will be produced by constructing and simulating the various power

circuits in PSCAD software. The first SMC topology to be simulated is 1×4 and the simulation parameters are given by Table 3.2, the second topology is 2×4 and its simulation parameters are also given Table 3.3, the third topology is a 2×8 and its simulation parameters are given by Table 3.4, the fourth topology is a 3×4 and its simulation parameters are given by Table 3.5 and finally the fifth topology is a 4×8 and its simulation parameters indicated by Table 3.6. The output of the converter produces two phase load voltage and currents. Phase A has an RL (resistor and inductor) load whiles phase B has an RC (resistor and capacitor) load.

Table 3.2:. Simulation Parameters

1×4 SMC PARAMETERS	
COMPONENT	VALUE
Input voltage E	$300V$
Switching Frequency f_{sw}	$5KHz$
Output frequency f_0	$50Hz$
Circuit Capacitors C	$560\mu F$
Load resistance $R_{L(a)}$	25Ω
Load resistance $R_{L(b)}$	2Ω
Load Inductance $L_{L(a)}$	$30mH$
Load capacitance $C_{L(b)}$	$100\mu F$
Modulation index M	0.8

Table 3.3: Simulation Parameters

2×4 SMC PARAMETERS	
COMPONENT	VALUE
Input voltage (upper stack) $\frac{1}{2}E$	$150V$
Input voltage (lower stack) $\frac{1}{2}E$	$150V$

Switching Frequency f_{sw}	$5KHz$
Output frequency f_0	$50Hz$
Circuit Capacitors C	$560\mu F$
Load resistance $R_{L(a)}$	25Ω
Load resistance $R_{L(b)}$	2Ω
Load Inductance $L_{L(a)}$	$30mH$
Load capacitance $C_{L(b)}$	$100\mu F$
Modulation index M	0.8

Table 3.4: Simulation Parameters

2×8 SMC PARAMETERS	
COMPONENT	VALUE
Input voltage (upper stack) $\frac{1}{2}E$	$150V$
Input voltage (lower stack) $\frac{1}{2}E$	$150V$
Switching Frequency f_{sw}	$5KHz$
Output frequency f_0	$50Hz$
Circuit Capacitors C	$560\mu F$
Load resistance $R_{L(a)}$	25Ω
Load resistance $R_{L(b)}$	2Ω
Load Inductance $L_{L(a)}$	$30mH$
Load capacitance $C_{L(b)}$	$100\mu F$
Modulation index M	0.8

Table 3.5: Simulation Parameters

COMPONENT	VALUE
Input voltage (2 upper stacks) E	$100V$
Input voltage (1 lower stack) E	$100V$
Switching Frequency f_{sw}	$5KHz$
Output frequency f_0	$50Hz$
Circuit Capacitors C	$560\mu F$
Load resistance $R_{L(a)}$	25Ω
Load resistance $R_{L(b)}$	2Ω
Load Inductance $L_{L(a)}$	$30mH$
Load capacitance $C_{L(b)}$	$100\mu F$
Modulation index M	0.8

Table 3.6: Simulation Parameters

4 × 8 SMC PARAMETERS	
COMPONENT	VALUE
Input voltage (2 upper stacks) E	$75V$
Input voltage (2 lower stack) E	$75V$
Switching Frequency f_{sw}	$5KHz$
Output frequency f_0	$50Hz$
Circuit Capacitors C	$560\mu F$
Load resistance $R_{L(a)}$	25Ω
Load resistance $R_{L(b)}$	2Ω
Load Inductance $L_{L(a)}$	$30mH$
Load capacitance $C_{L(b)}$	$100\mu F$
Modulation index M	0.8

1 × 4 SMC Simulation Results

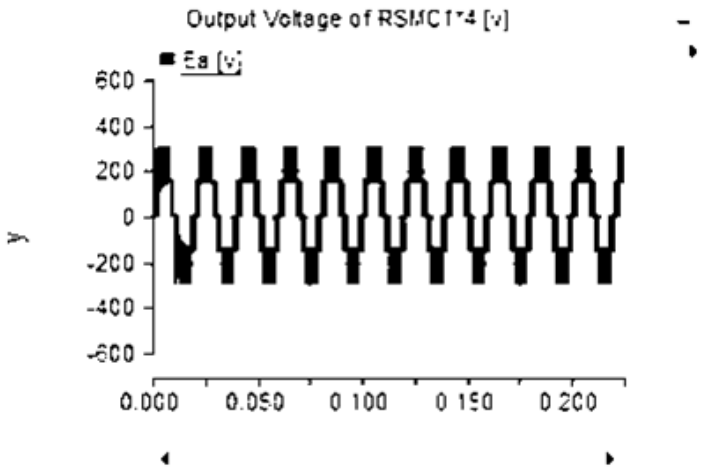

Figure 3.7: Output voltage waveform

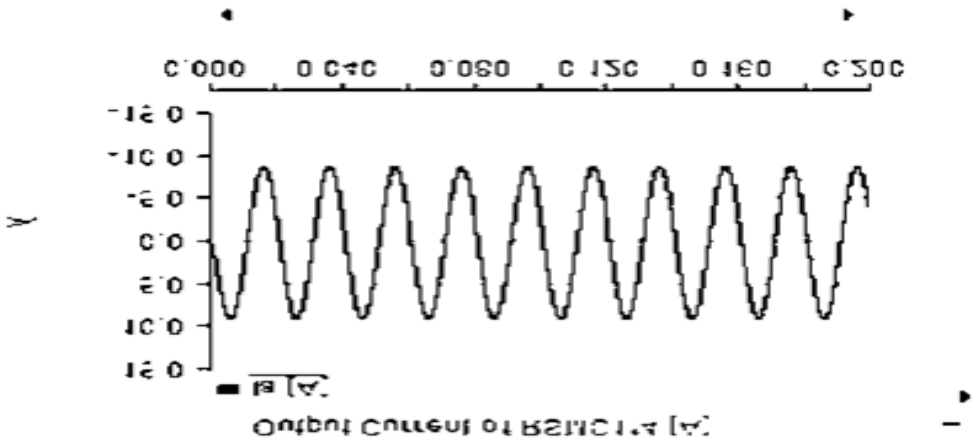

Figure 3.8: Output current waveform of phase A

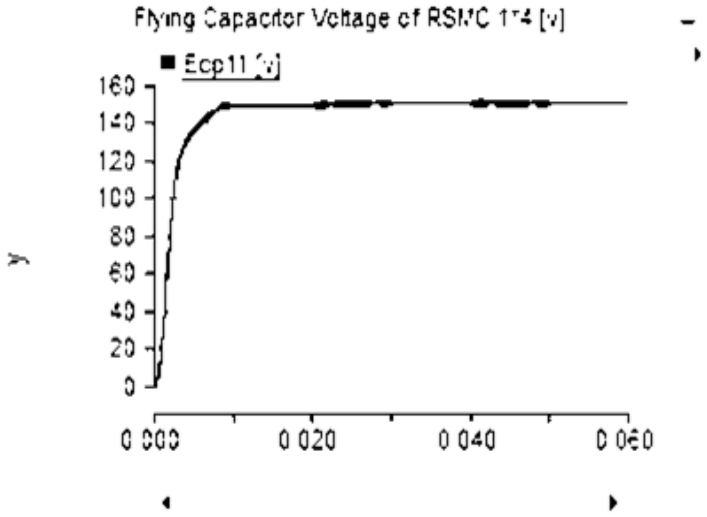

Figure 3.9a: Capacitor voltage waveform

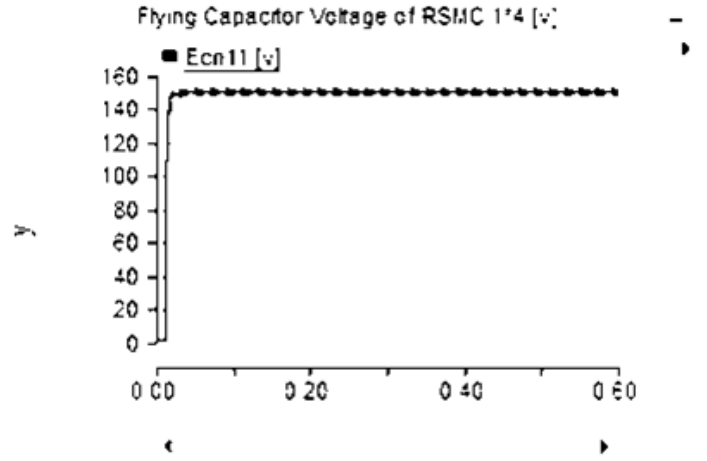

Figure 3.9b: Capacitor voltage waveform

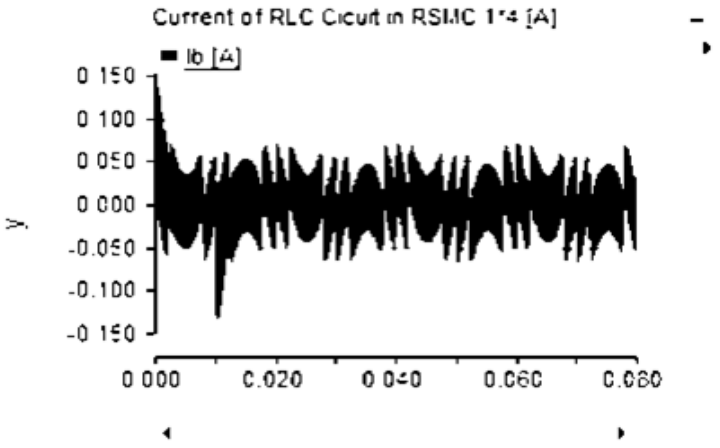

Figure 3.10: Output current waveform of phase B

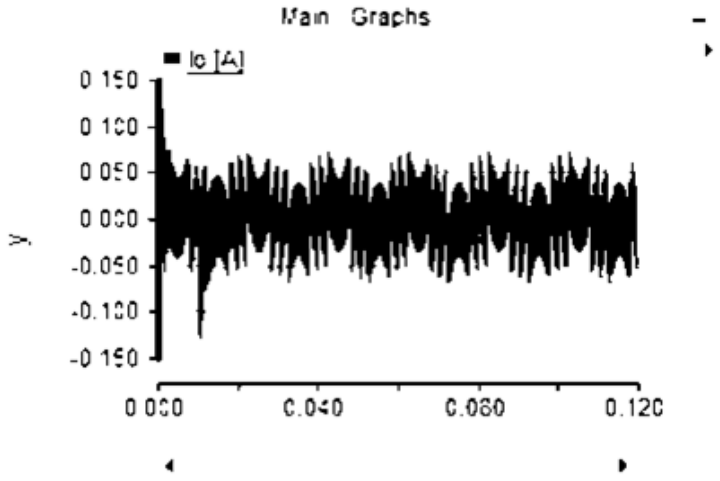

Figure 3.11: Main output current waveform

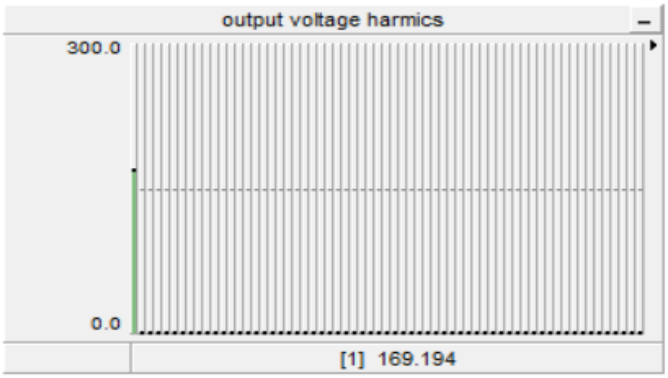

Figure 3.12: Waveform of output voltage harmonics

2X4 SMC Simulation Results

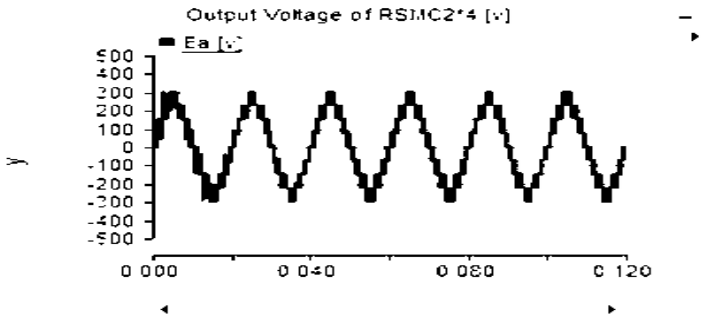

Figure **3.13:** Output voltage waveform

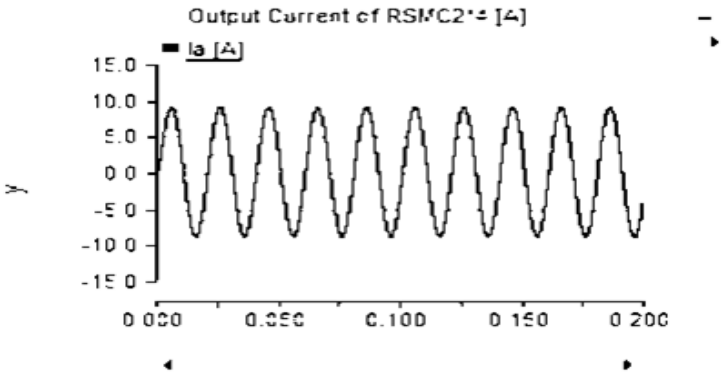

Figure 3.14: Output current waveform of phase A

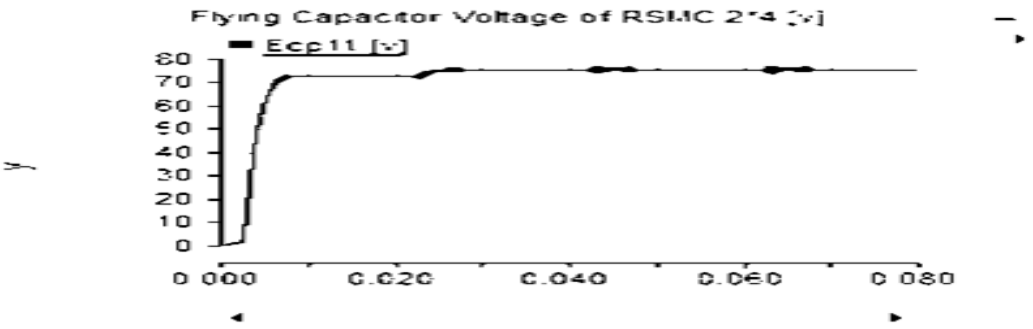

Figure 3.15: Capacitor voltage waveform

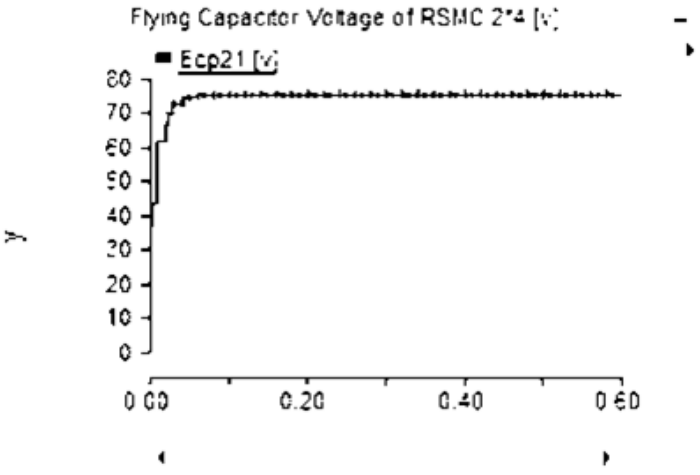

Figure 3.16: Capacitor voltage waveform

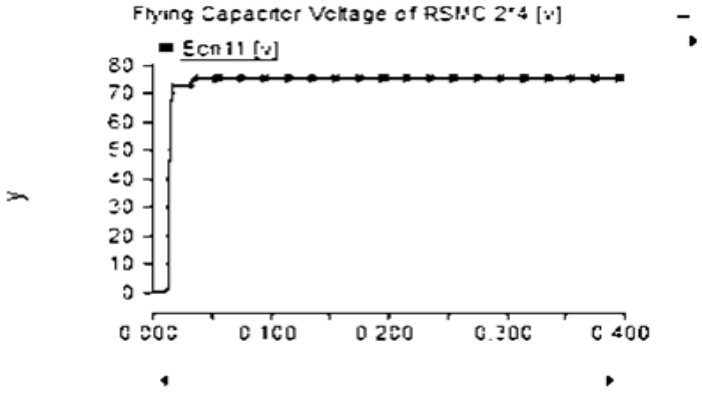

Figure **3.17:** Capacitor voltage waveform

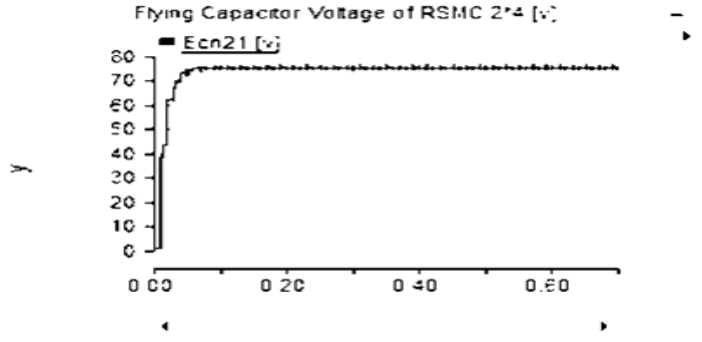

Figure 3.18: Capacitor voltage waveform

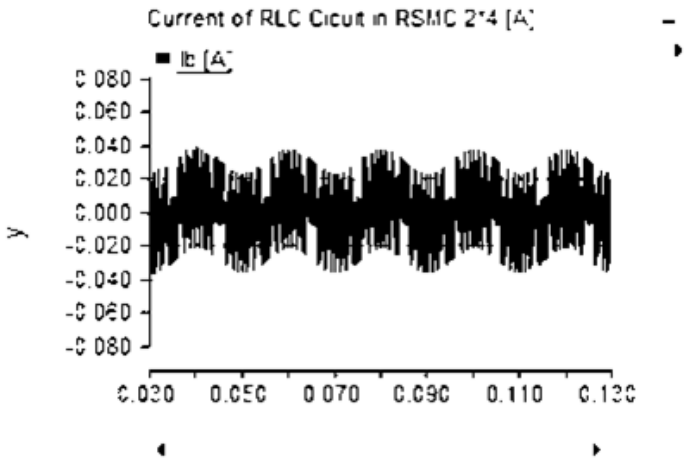

Figure 3.19: Output current waveform of phase B

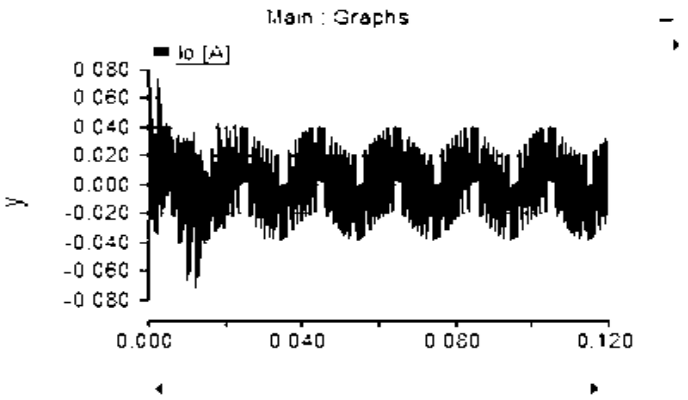

Figure 3.20: Main current output waveforms

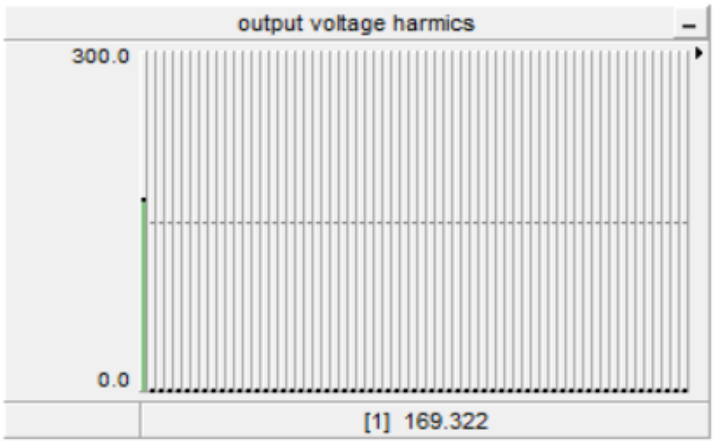

Figure3.21: Waveform of output voltage harmonics

2×8 SMC Simulation Results

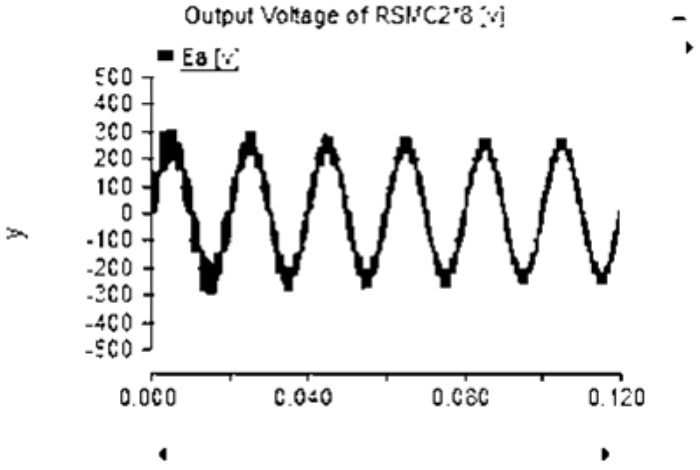

Figure 3.22: Output voltage waveform

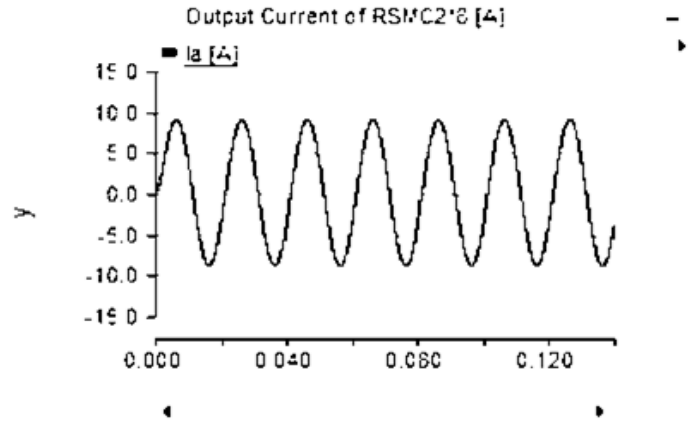

Figure 3.23: Output current waveform of phase A

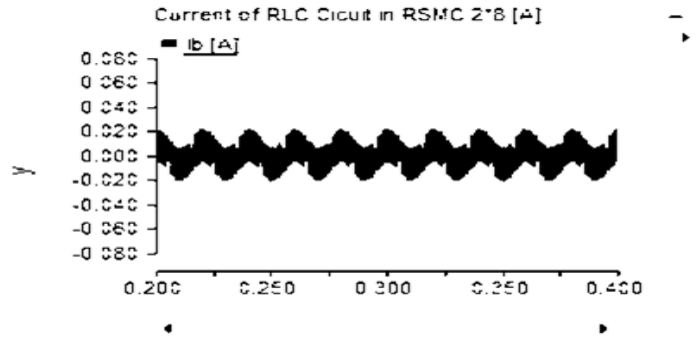

Figure 3.24: Output current waveform of phase B

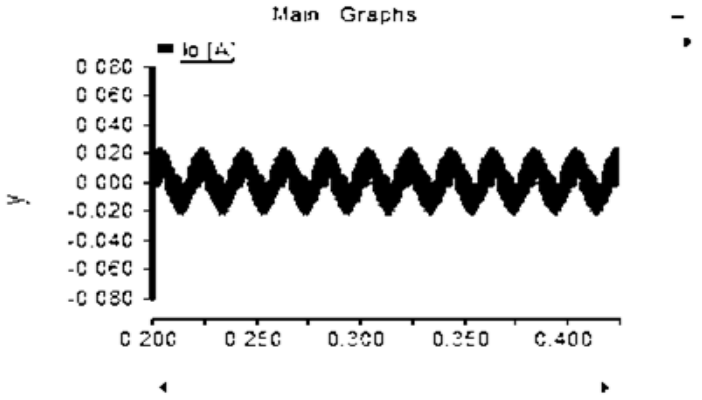

Figure **3.25:** Main output current waveform

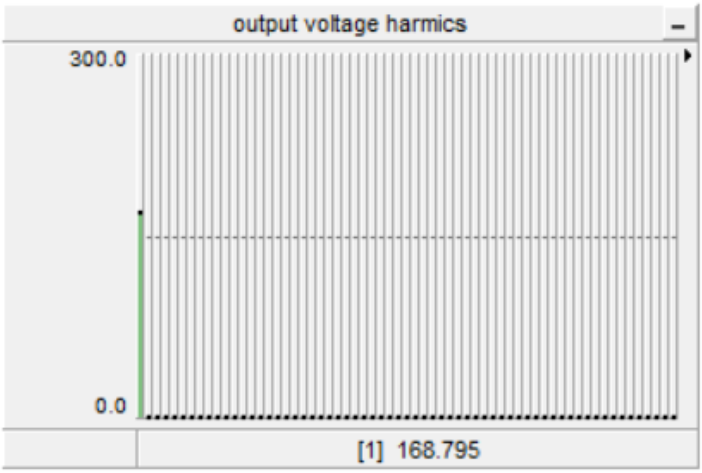

Figure **3.26:** Waveform of output voltage harmonics

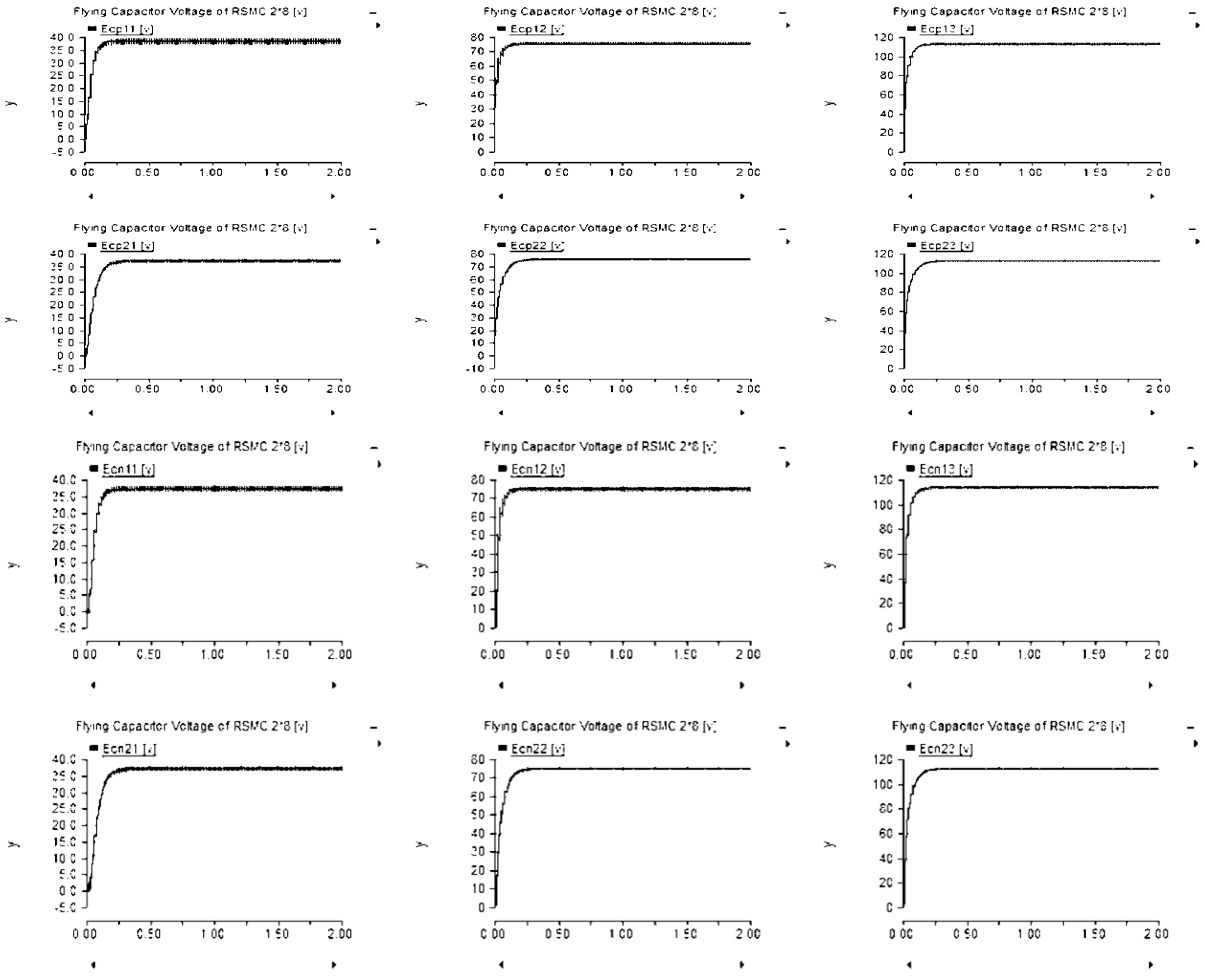

Figure 3.27: Capacitor voltage waveform

4×4 SMC Simulation Results

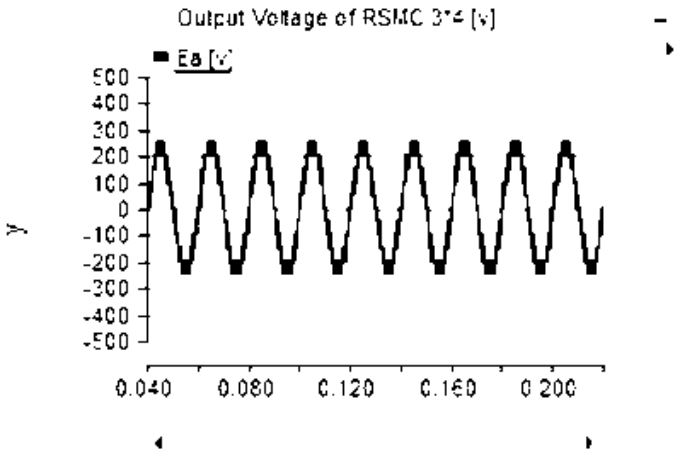

Figure 3.28: Output voltage waveform

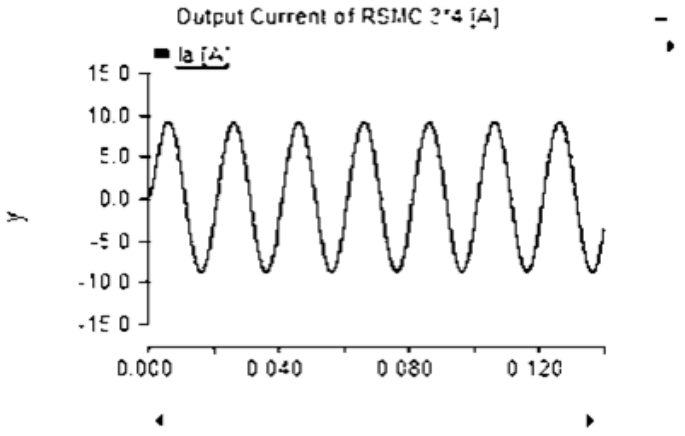

Figure 3.29: Output current waveform of phase A

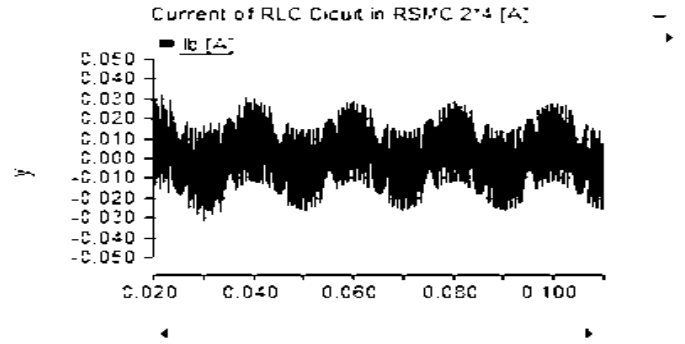

Figure 3.30: Output current waveform of phase B

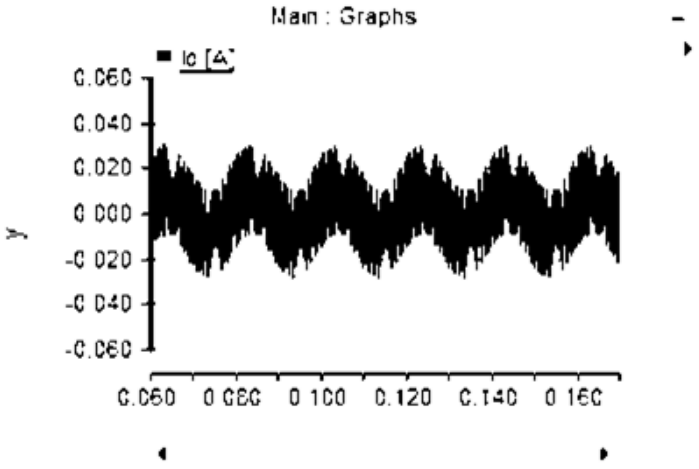

Figure 3.31: Main current output waveform

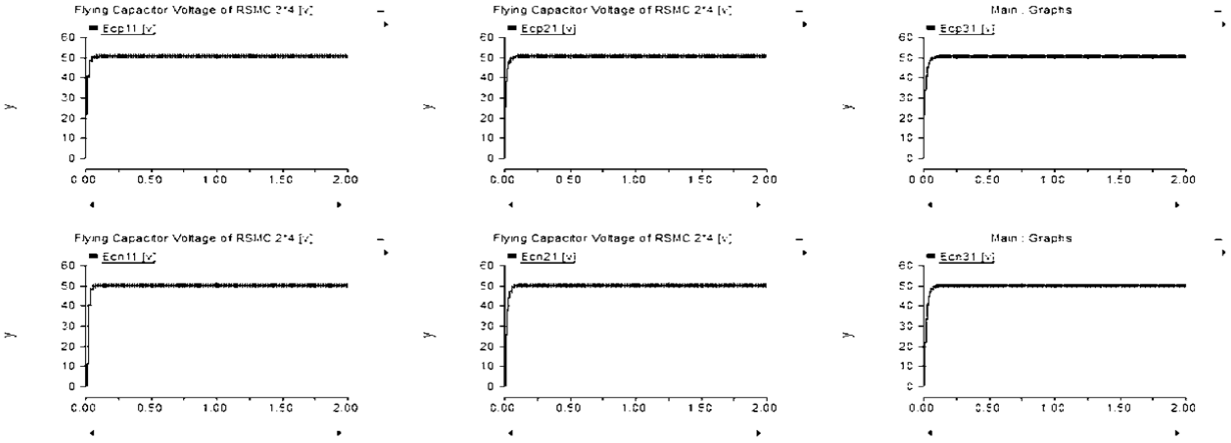

Figure 3.32: Capacitor voltage waveforms

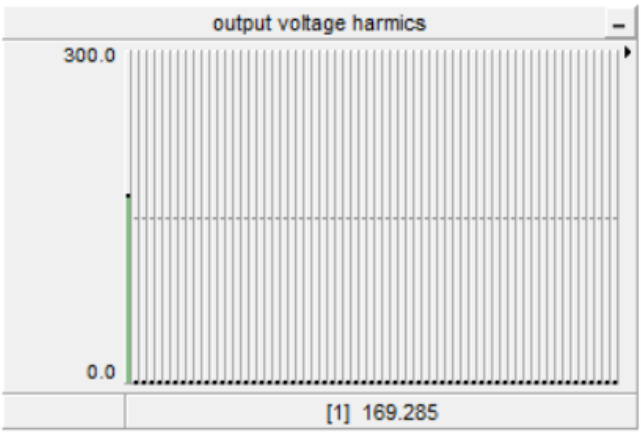

Figure 3.33: Waveform of output voltage harmonics

4 × 8 SMC Simulation Results

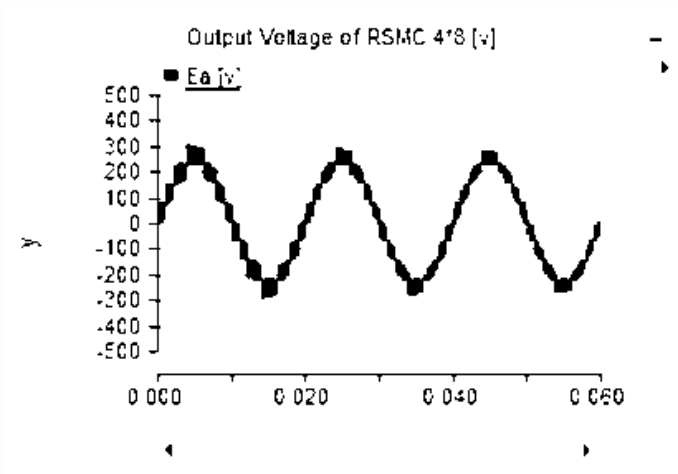

Figure 3.34: Output voltage waveform

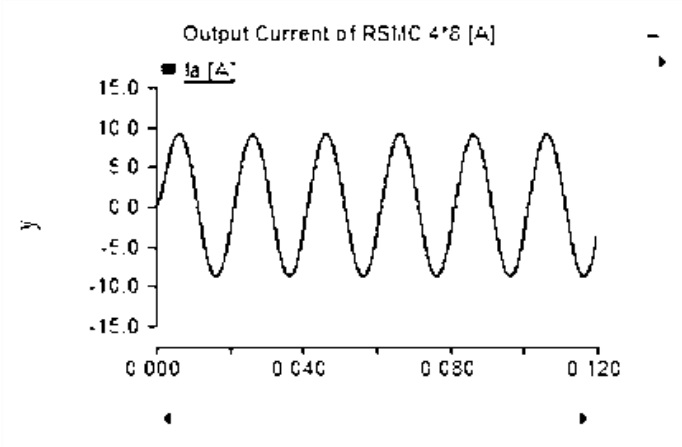

Figure **3.35:** Output current waveform of phase A

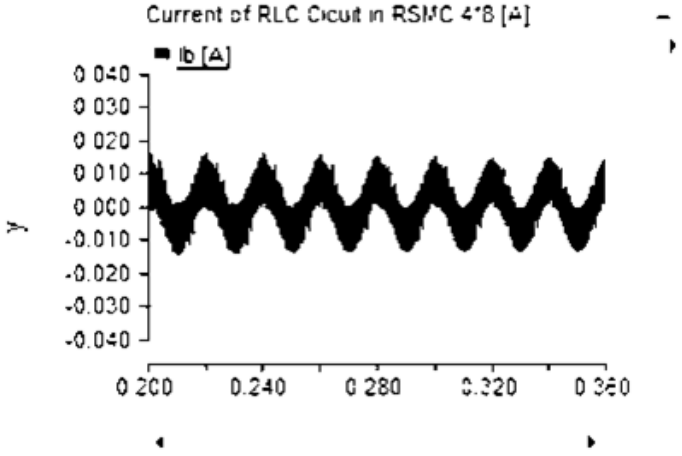

Figure **3.36:** Output current waveform of phase A

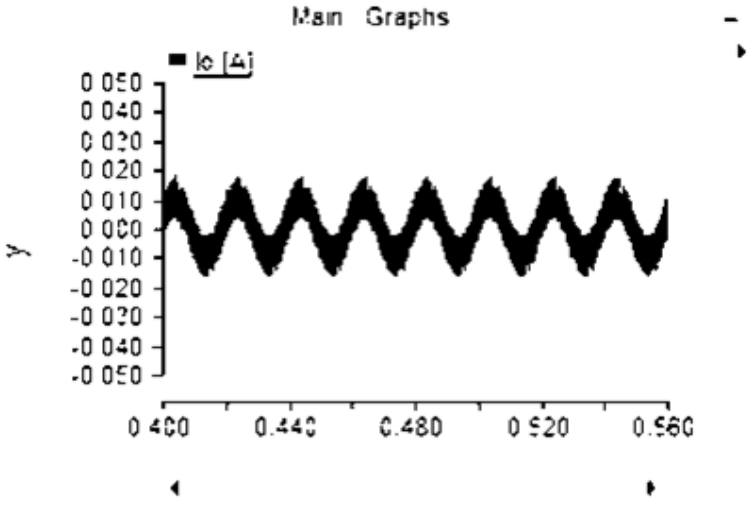

Figure **3.37:** Main current output waveforms

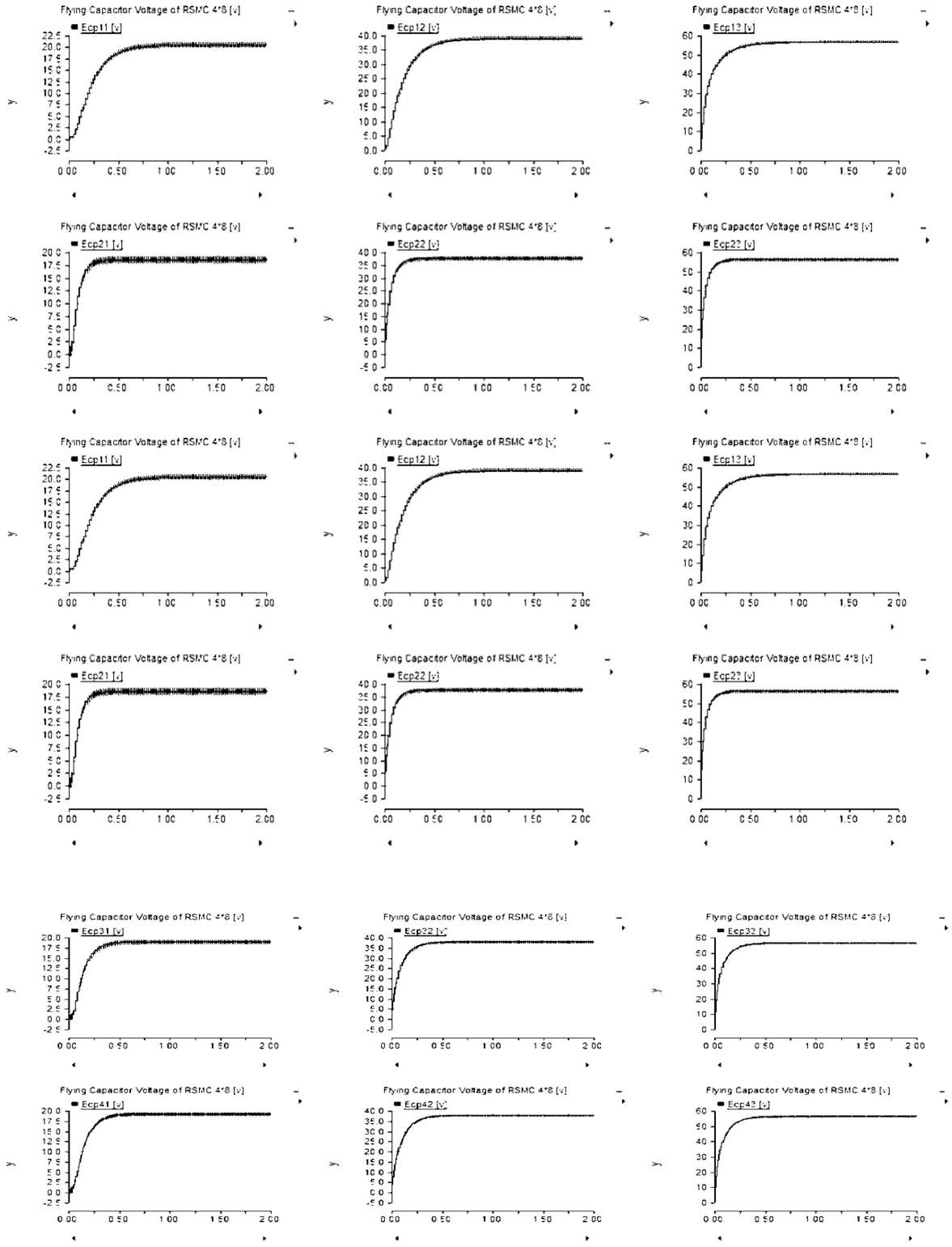

Figure 3.38: Capacitor voltage waveforms

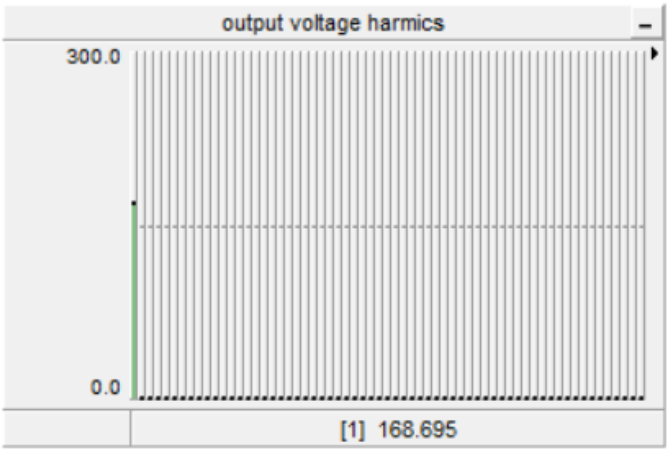

Figure 3.39: Waveform of output voltage harmonics

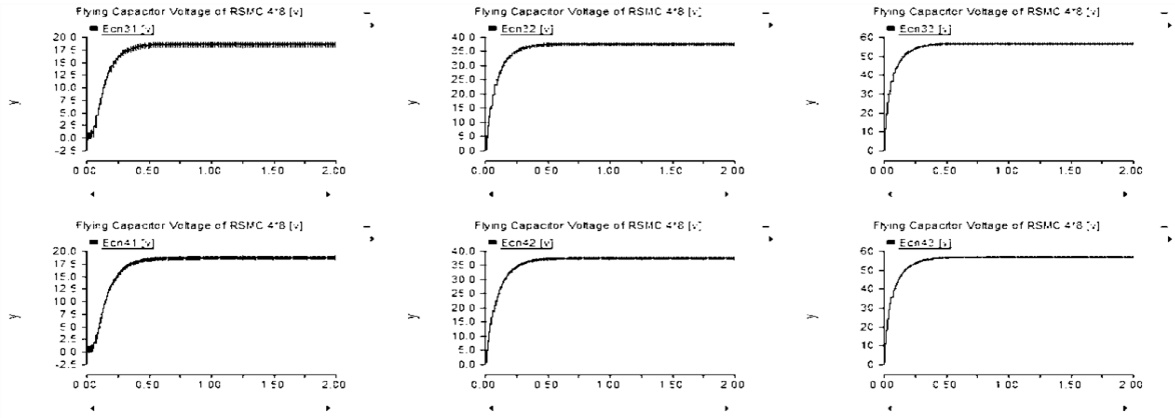

Figure 3.40: Capacitor voltage waveforms

Simulation results for the presented one voltage SM converter are presented for five different case scenarios. The topology's min concept is maintained i.e. application of one dc source, however, the number of stacks as well as the number of cells are varied for these five different cases. The first case is 1×4 topology which means the number of stacks is one whiles the number of cells is four, the results of the simulation for this topology is given by Fig. 3.7 to Fig. 3.12. the waveform of the output voltage and output currents are illustrated by Fig. 3.7 and Fig. 3.11 respectively, phase A and B output currents are given by Fig. 3.8 and Fig. 3.10 respectively, the capacitor voltage waveforms are indicated by Fig. 3.9a and Fig. 3.9b, the output harmonic spectrum is illustrated by Fig. 3.12. The second case is 2×4 topology which indicates that the number of stacks is two whiles the number of cells is four,

the results of the simulation for this topology is given by Fig. 3.13 to Fig. 3.21. the waveform of the output voltage and output currents are illustrated by Fig. 3.13 and Fig. 3.20 respectively, phase A and B output currents are given by Fig. 3.14 and Fig. 3.19 respectively, the capacitor voltage waveforms are indicated by Fig. 3.15 and Fig. 3.19, the output harmonic spectrum is illustrated by Fig. 3.21. The third case is 2×8 topology which indicates that the number of stacks is two whiles the number of cells is eight, the results of the simulation for this topology is given by Fig. 3.22 to Fig. 3.27. The waveform of the output voltage and output current are illustrated by Fig. 3.22 and Fig. 3.25 respectively, phase A and B output currents are given by Fig. 3.23 and Fig. 3.24 respectively, the capacitor voltage waveforms are indicated by Fig. 3.27 and the output harmonic spectrum is illustrated by Fig. 3.26. The fourth case is 3×4 topology which indicates that the number of stacks is three whiles the number of cells is four, the results of the simulation for this topology is given by Fig. 3.28 to Fig. 3.33. The waveform of the output voltage and output current are illustrated by Fig. 3.28 and Fig. 3.31 respectively, phase A and B output currents are given by Fig. 3.29 and Fig. 3.30 respectively, the capacitor voltage waveforms are indicated by Fig. 3.32 and the output harmonic spectrum is illustrated by Fig. 3.33. Finally, the fifth case is 4×8 topology which indicates that the number of stacks is four whiles the number of cells is eight, the results of the simulation for this topology is given by Fig. 3.34 to Fig. 3.40. The waveform of the output voltage and output current are illustrated by Fig. 3.34 and Fig. 3.37 respectively, phase A and B output currents are given by Fig. 3.35 and Fig. 3.36 respectively, the capacitor voltage waveforms are indicated by Fig. 3.38 and Fig.3.40 and the output harmonic spectrum is illustrated by Fig. 3.39.

3.1.3 Conclusion

A single dc voltage based stacked multicell converter is presented in this research. The presented topology is an enhancement of the conventional SM converter where the number of utilized source voltage is reduced to one thereby reducing the cost of the converter. Also lower rated semiconductor switches are applied where the switches are the least in number when compared to the traditional SMC. apart from the above numerated advantages, the presented topology also has the following advantages reduced converter cost, less installation area required and reduced converter losses. Simulation analysis of the

presented topology is carried out and results produced to verify the operational properties of the converter. Five case of simulations were investigated with various number of stacks and cells. All produced waveform affirms the correct operational state of the presented converter.

CHAPTER 4

CONCLUSION AND RECOMMENDATION

4.1 Conclusion

Applications of multilevel converters in the conditioning of the characteristics of electric power is an integral component in the supply of pollution free electric power with requisite or desired characteristics. This trend will continue and even improve in the foreseeable future due to integration of renewable energy and distributed generation source. There are various topologies of multilevel however this research seeks to implement the topology of stacked multicell converter.

Stacked multicell converter are mostly suitable for high power applications with power magnitudes of above 50MW and also medium DC power systems with voltage magnitude exceeding 50kV. SMC provides the capabilities of voltage constraint sharing on multiple commutation cells and also application of lower rated switches because the input voltage is split into several fractions. Also the SMC boast of optimal dynamic performance because of increased stepped output voltages and proliferation of chopped frequency voltage.

The structure of this research (thesis) is segmented into four chapters where in chapter one, the aim, problem and solution of the presented topology are discussed. In chapter two, literature review of the chosen topology is presented in broader perspective. In chapter three, analysis and simulation of the presented topology is given, then finally conclusion and recommendations are given in chapter four.

From chapter three, general topology of stacked multicell is presented. The principal advantage of the presented topology is reduction in the number of dc sources and the ease with which it can be scaled up any desired number of cells and stacks. Five different simulation results with various number of stacks and cells are produced. The number of stacks was increased from an initial number of one to a maximum number of four whiles the number of cells was also increased from an initial number of four to the highest number of eight. In all generated waveforms for the five case scenarios, the quality of the output waveforms is comparable to theoretical waveforms. These high standard of generated waveform via simulations confirms the operational working capabilities of the presented

topology. Finally, a single dc input based SMC is presented in this research with five different topologies. The presented topology is an improved version of the traditional SMC where there are multiple input dc sources. Reducing the quantity of input source reduces the cost of the converter and also makes it possible to utilize lower rated switches hence converter losses are minimized. In addition, the presented SMC has the following merits reduced converter cost, less installation area required and reduced converter losses. PSCAD software is utilized in simulating and generating the output waveforms of the SMC.

4.2. Recommendations

One major limitation of the presented SMC is the increased number of the lower rated switches when the number of stacks or cells are increased. As part of my future works, I wish to find innovative ways reducing the quantity switches while maintaining or improving the general topology of the presented SMC.

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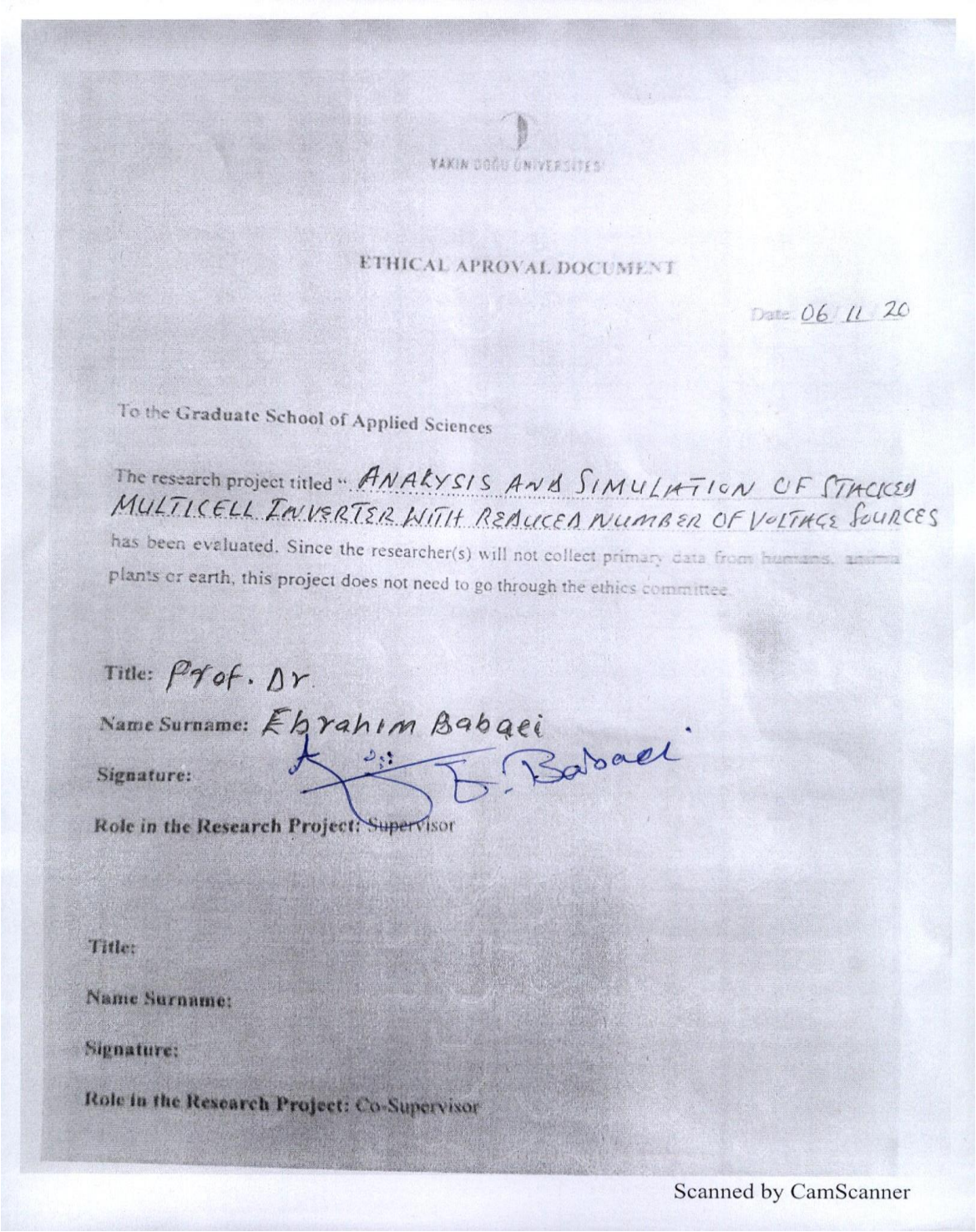
APPENDICES

APPENDIX 1

ETHICAL CONTRACT FORM



YAKIN DOĞU ÜNİVERSİTESİ

ETHICAL APROVAL DOCUMENT

Date: 06 / 11 / 20

To the Graduate School of Applied Sciences

The research project titled " ANALYSIS AND SIMULATION OF STACKED MULTICELL INVERTER WITH REDUCED NUMBER OF VOLTAGE SOURCES has been evaluated. Since the researcher(s) will not collect primary data from humans, animals plants or earth, this project does not need to go through the ethics committee.

Title: Prof. Dr.

Name Surname: Ebrahim Babaei

Signature: E. Babaei

Role in the Research Project: Supervisor

Title:

Name Surname:

Signature:

Role in the Research Project: Co-Supervisor

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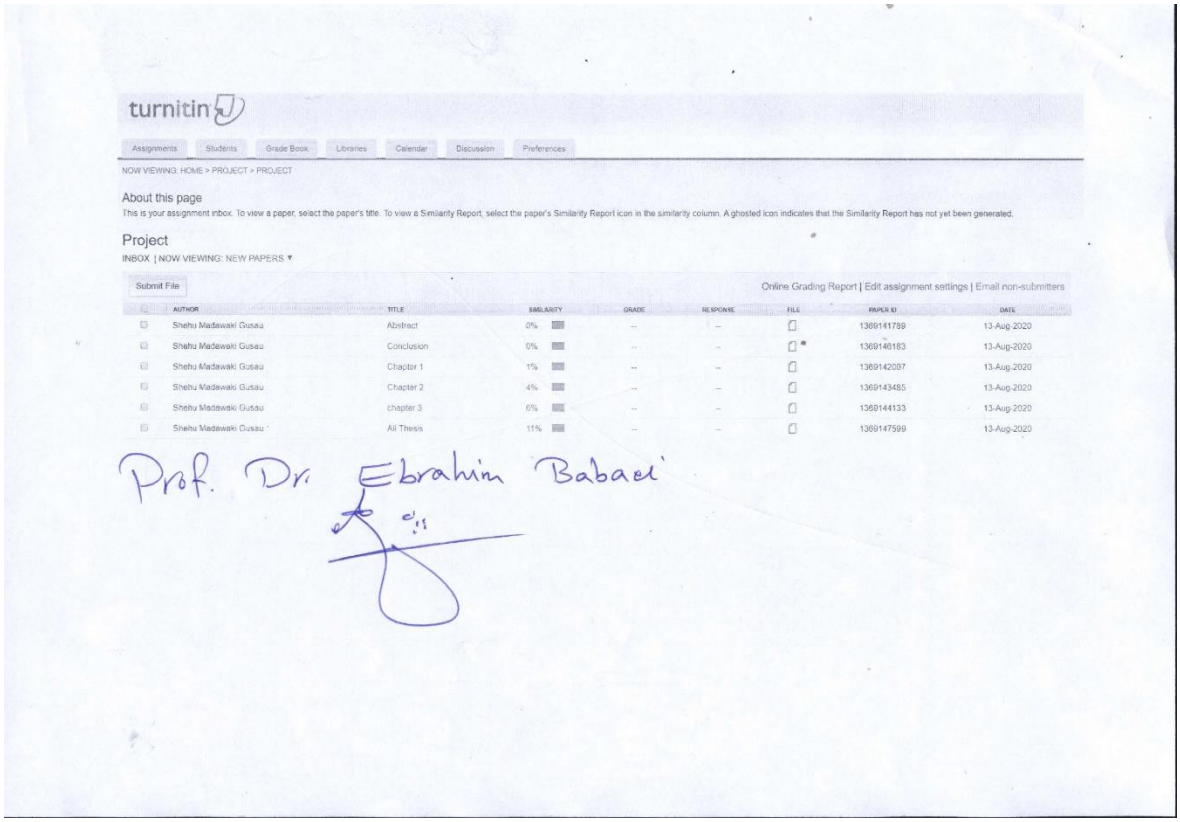
APPENDIX 2

SIMILARITY REPORT



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