NEAR EAST UNIVERSITY

INSTITUTE OF GRADUATE STUDIES

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SWITCHED INDUCTOR CAPACITOR BASED DC-DC CONVERTER FOR PV APPLICATIONS

M.Sc. THESIS

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Nicosia

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MASTER THESIS

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Assist. Prof. Dr. Samuel Nii Tackie

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Approval

We certify that we have read the thesis submitted by Brendon Kudakwashe Kurehwatira titled **"Switched Inductor Capacitor based DC-DC Converter for PV Applications**" and that in our combined opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Educational Sciences.

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Declaration

I hereby declare that all information, documents, analysis and results in this thesis have been collected and presented according to the academic rules and ethical guidelines of Institute of Graduate Studies, Near East University. I also declare that as required by these rules and conduct, I have fully cited and referenced information and data that are not original to this study.

Brendon Kudakwashe Kurehwatira

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Brendon Kudakwashe Kurehwatira

Abstract

Switched inductor capacitor based DC-DC converter for PV applications

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Assist. Prof. Dr. Samuel Nii Tackie

M.S.c, Department of Electrical and Electronics Engineering
January, 2022, 85 pages

A two stage DC-AC converter topology that features a Switched Inductor Capacitor (SLCN) DC-DC converter and a single phase H-bridge inverter is proposed in this thesis. The SLCN converter has 12 components including one power switch, and the H-bridge has 4 IGBTs with antiparallel diodes. The principal merits of the topology being proposed consist of high boost ratio, one power electronic switch and reduced voltage stress across the switch on the DC-DC side, low component count, and it's implemented using simple control techniques. The major trade-off for the proposed topology over single stage inverters is the high voltage gain and its suitability to DC loads.

A detailed analysis of the DC-DC topology is carried out in CCM, and a theoretical gain of 20 at 80% duty cycle is achieved in steady state. The proposed converter topology is suitable for solar PV application to boost low voltage to high voltage at grid consumer level or higher. The working principles of the proposed topology are validated by PSCAD simulations, using 20 kHz switching frequency and 80% duty cycle for the DC-DC side and modified sinusoidal PWM technique for the DC-AC side.

Key words: DC-DC converter, H-bridge inverter, high voltage gain, modified sinusoidal PWM, switched inductor capacitor network

Özet

Switched inductor capacitor based DC-DC converter for PV applications

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Bu tezde, Anahtarlamalı Endüktör Kondansatörlü (SLCN) DC-DC dönüştürücü ve tek fazlı H-köprü evirici içeren iki aşamalı bir DC-AC dönüştürücü topolojisi önerilmiştir. SLCN dönüştürücü, bir güç anahtarı dahil olmak üzere 12 bileşene sahiptir ve H-köprüsü, antiparalel diyotlara sahip 4 IGBT'ye sahiptir. Önerilen topolojinin başlıca avantajları, yüksek yükseltme oranı, bir güç elektroniği anahtarı ve DC-DC tarafında anahtar boyunca azaltılmış voltaj stresi, düşük bileşen sayısıdır ve basit kontrol teknikleri kullanılarak uygulanır. Tek kademeli eviriciler üzerinde önerilen topoloji için en büyük ödünleşim, yüksek voltaj kazancı ve DC yüklere uygunluğudur.

DC-DC topolojisinin ayrıntılı bir analizi CCM'de gerçekleştirilir ve kararlı durumda %80 görev döngüsünde 20'lik bir teorik kazanç elde edilir. Önerilen dönüştürücü topolojisi, güneş enerjisi PV uygulaması için düşük voltajı şebeke tüketici seviyesinde veya daha yüksek bir seviyede yüksek voltaja yükseltmek için uygundur. Önerilen topolojinin çalışma prensipleri, DC-DC tarafı için 20 kHz anahtarlama frekansı ve %80 görev döngüsü ve DC-AC tarafı için modifiye sinüzoidal PWM tekniği kullanılarak PSCAD simülasyonları ile doğrulanmıştır.

Anahtar kelimeler: DC-DC dönüştürücü, H-köprü inverter, yüksek voltaj kazancı, modifiye sinüsoidal PWM, anahtarlamalı indüktör kapasitör ağı

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List of Abbreviations

AC:	Alternating Current
CCM:	Continuous Conduction Mode
CSI:	Current Source Inverter
DC:	Direct Current
DCM:	Discontinuous Conduction Mode
EMI:	Electromagnetic Interference
HF:	Harmonic Factor
HVDC:	High Voltage Direct Current
IGBTs:	Insulated-Gate Bipolar Transistors
KVL:	Kirchhoff's Voltage Law
MATLAB:	MATrix LABoratory
MISO:	Multi Input Single Output
MPWM:	Multiple Pulse Width Modulation
MSPWM:	Modified Sinusoidal Pulse Width Modulation
PSCAD:	Power System Computer Aided Design
PV:	Photovoltaic
PWM:	Pulse Width Modulation
qZS:	quasi-Z-source
RMS:	Root Mean Square
SC:	Switched Capacitor
SEPIC:	Single Ended Primary Inductor Converter
SL:	Switched Inductor
SLCN:	Switched Inductor Capacitor Network
SL-qZS:	Switched Inductor quasi-Z-source
SLSC:	Switched Inductor Capacitor
SL-ZS:	Switched Inductor Z-source
SPWM:	Single Pulse Width Modulation
THD:	Total Harmonic Distortion
VSI:	Voltage Source Inverter
ZS:	Z-source

CHAPTER 1
Introduction

1.1 Overview

Over the last few years, electrical energy consumers have become more aware and involved in the energy market. They have become aware of issues like depletion of fossil fuels, and emissions resulting from use of these fuels. They are increasingly becoming involved in demand side generation of electricity for various reasons including but not limited to, cutting down their energy costs, participating in the movement for environmentally friendly and sustainable energy sources, and improved reliability for energy supply. As a result, there is growing attention towards renewable energy sources like solar, wind, biomass and etc. However, energy consumers are mostly interested in solar PV because the cost of installation which has significantly decreased over the years. Furthermore, solar PV systems can be mounted in urban spaces like rooftops, and this makes them an accessible and practical option for most consumers, in contrast to other renewable energy sources like wind.

In solar PV systems, there are four configurations namely stand-alone (off grid), grid-tie (grid connected), grid-tie with backup (grid-interactive), and grid fall back (Micheal, 2012). A lot of consumers who live away from the power network tend to use the off-grid systems, while those who live within the grid use grid-tied systems, with or without back-up. Those with grid interactive systems enjoy an uninterrupted power supply from their battery bank during a power cut. Whereas grid fall back is a system that allows use of the solar PV array to power a house or part of the house with solar energy from batteries until they go flat, then fall back to the grid while the batteries recharge. A lot of solar PV installations which are grid-tied utilize the second and third configurations, and they come with a high initial cost. The consumer is required to install a system that meets the grid requirements and other standards set by the utility company from the onset. Whereas, a grid fall-back system allows the consumer to start with one panel and one battery.

Grid fall-back system is suitable in countries where energy supply from the grid is unreliable, and there are neither government incentives towards consumer side renewable energy generation nor restrictions towards time of use for renewable energy systems. This is because it allows the consumer to switch to a renewable energy generator at will, and the consumers can avoid the cost of installing a large system from the onset.

In a 2019 article by GET.invest on Zimbabwe's energy sector, it is reported that the country continues to have power shortages which are shown by an estimated deficit of 60%. The Zimbabwe Electricity Supply Authority (ZESA) has an installed capacity of approximately 1940MW with a projected national demand of 2200MW (GET.invest, 2019). Therefore, apart from importing electricity from South Africa and Mozambique, the electricity authority meets the deficit by frequent load shedding.

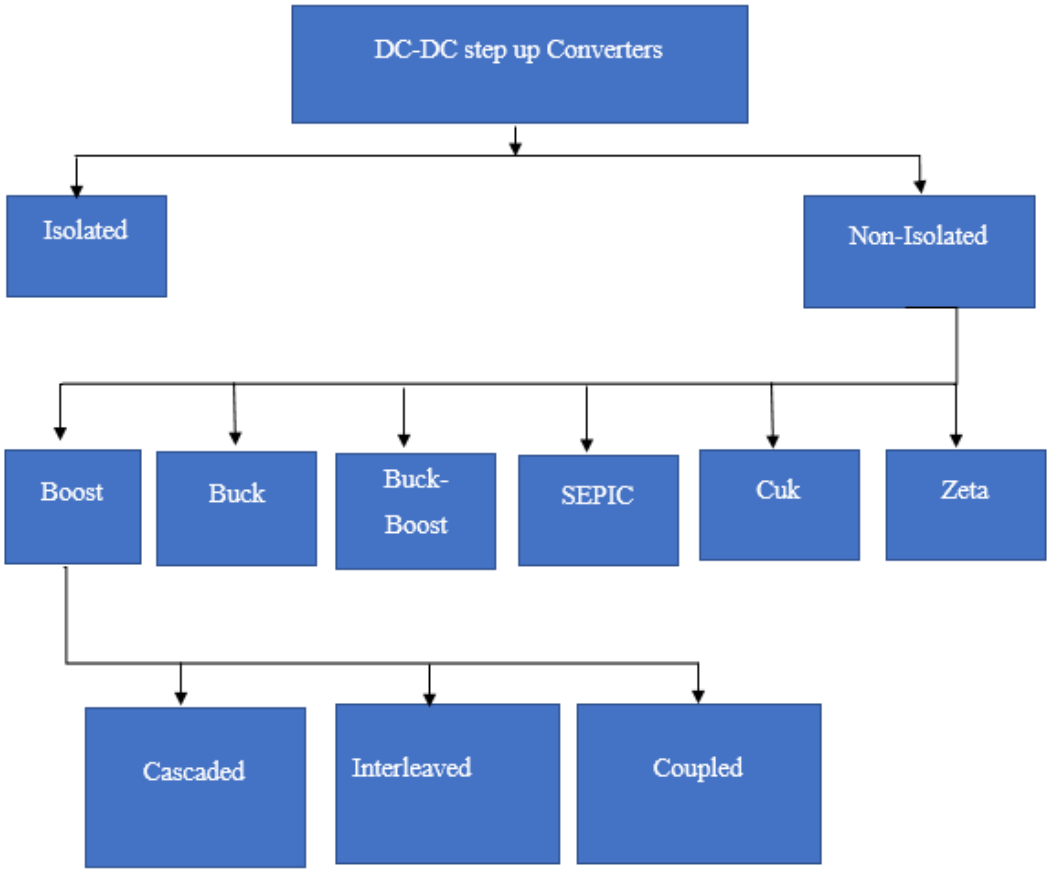
Load shedding is a method used to relieve the primary energy sources when the demand of electricity is greater than the supply to meet the demand of a selected consumers at a given time. Therefore, in countries like Zimbabwe where consumers in the electric grid experience extensive controlled power cuts periodically for up to 5 hours or more in a day, grid fall-back system is most suitable. For instance, electricity is cut from most residential areas to cater for the industrial and commercial loads during the day, and vice-versa for night times. A grid fall-back systems can be used to supply electric energy using the solar PV system during periods of load shedding, and the consumer switches back to the grid when it is online again.

Solar PV, like most renewable energy sources, suffers from issues of variability, low voltage, and incompatible output waveforms for grid connected loads. Therefore, a system is required to interface the solar energy source with the load. There are different energy conversion systems available to step up and regulate the voltage waveform from these sources so that it meets grid standards. Single stage and two stage DC-AC converter systems are used to interface the output of a renewable energy source with the load. Single stage systems lack the DC-DC step up conversion component solely meant for voltage boost, and it places it at a disadvantage with two stage DC-AC conversion systems. In order to boost the low DC voltage of the solar PV system, a high boost power electronic device is required. The output of the DC-DC boost converter in a two stage DC-AC system becomes the input of the DC-AC inverter. The inverter then transforms the waveform into a sinewave which is compatible with AC loads in the power system network.

DC-DC step up converters can be classified as isolated and non-isolated DC-DC converters, as shown in Figure 1. Isolated DC-DC converters use transformers which basically isolate the input and output side, and steps up or down the input voltage by controlling the turns ratio between the primary and secondary turns. However, isolated DC-DC converters are bulky and they are costly as they require high frequency transformers (Sadaf, et al., 2021).

Figure 1

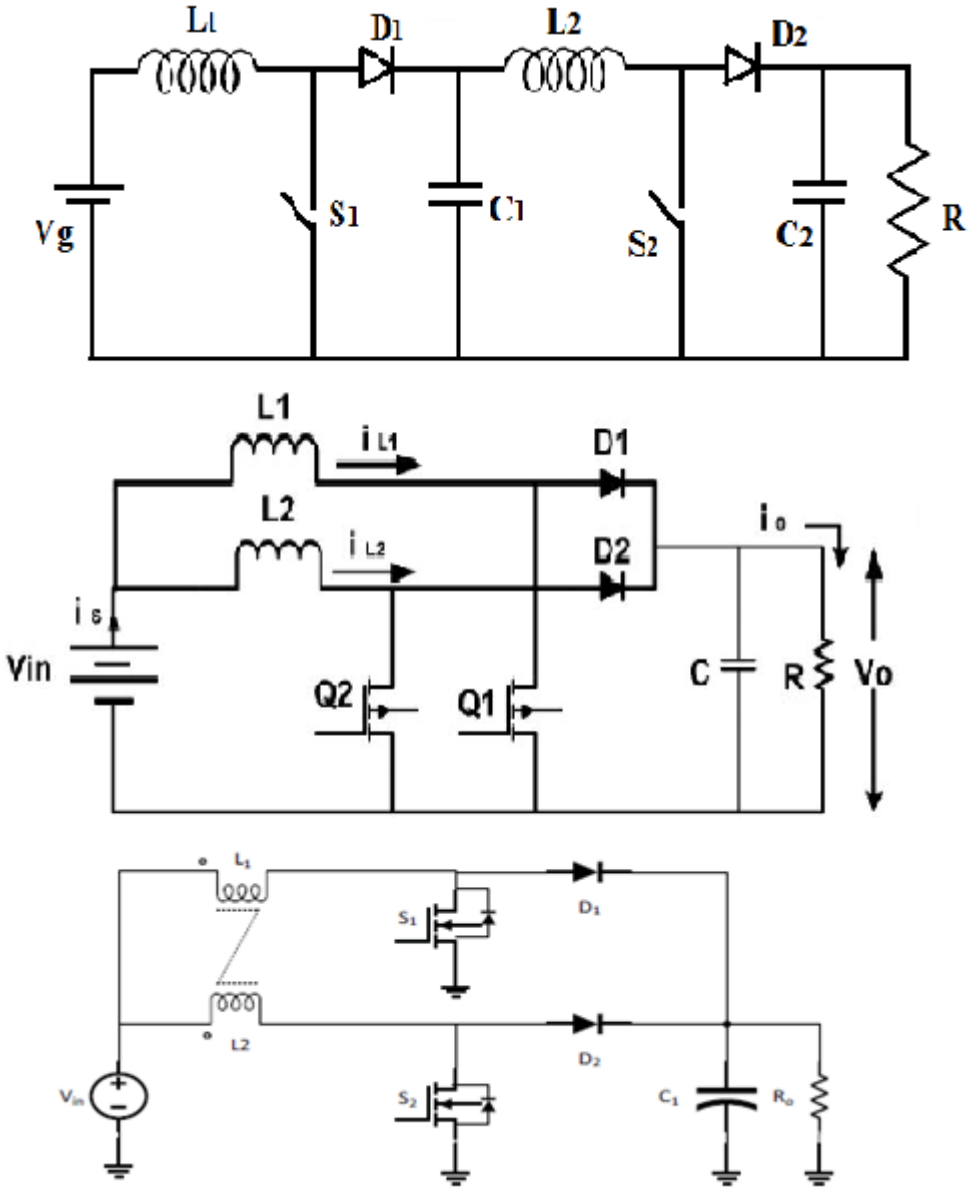
DC-DC Step Up Converter Classification



The non-isolated DC-DC converter category has boost, buck, buck-boost, Cuk, SEPIC, and Zeta converters. The traditional boost converter is capable of producing high voltage gains (up to five times the input voltage) but only when the duty cycle approaches unity. This causes heating issues, high conduction losses which result in reduced efficiency, and EMI in these converter devices (Rahman, et al., 2020). A buck converter steps down, and a buck-boost converter steps up or down the input voltage. Cuk, SEPIC, and Zeta converters have related structures with buck-boost converters, hence their voltage conversion capabilities are similar, although these topologies have more components and they are more complex (de Paula, et al., 2014).

Figure 2

Conventional Boost Converters in Different Topologies



Note. From top to bottom: Cascaded Boost Converter, Interleaved Boost Topology, and Coupled Inductor Boost Topology

Switched inductor and switched capacitor converter structures also provide high voltage conversion ratios in non-isolated topologies with soaring power density and efficiency (Nguyen, et al., 2013). However, switched inductor and switched capacitor structures are associated with large in input or source current ripples. And in the case of switched-capacitor boost converters, many active switches are used whose

voltage stress are not equal. At the back-end of the two stage DC-AC topology is an inverter which then transforms and regulates the DC output voltage of a DC-DC converter to a sine wave which meets the grid standards and requirements.

1.2 Statement of the Problem

As many electrical energy consumers are participating in demand side energy generation schemes, there is need for various options that allow consumers to use renewable energy sources in the grid starting with very few components. This will allow more consumers to be able to install solar PV systems, if the initial cost of setting up a solar system is considerably lower than the conventional grid connected systems.

A DC-DC topology with high boost ratio and less drawbacks on performance and efficiency is required to interface solar PV system with the DC load or inverter. Isolated DC-DC converters have issues related to having high frequency transformers. And other topologies derived from the boost converter become more complex and costly with increased component count, have increased voltage stress across circuit components, or some become complex topologies in terms of control and structure. Therefore, an overall DC-DC converter that can attain high voltage gain with a low component count and lesser drawbacks will be an ideal design. Additionally, an inverter is required to interface the DC-DC converter with AC loads.

1.3 Purpose of the Study

This thesis is set to design a topology that can be used in a grid fall-back system. The topology will be a two stage DC-AC converter capable of generating a boosted DC voltage and further transforming it to an AC voltage with respect to the load type. The target for the designed topology is a high boost ratio, minimum component count, reduced switch voltage, and relatively simple control techniques.

A DC-DC topology derived from a switched inductor capacitor network (SLCN) and is non-isolated, is proposed for the front-end side. At the back-end of the DC-AC converter topology, a single phase H-bridge sinusoidal PWM inverter is proposed. The overall DC-AC converter topology steps up a low voltage from a battery being charged by a solar PV system, and transforms it into a grid compatible sine wave, with a simple topology which has minimum component count.

1.4 Significance of the Study

The importance of the proposed DC-AC conversion system can be summarized as:

- Voltage gain is up to four times the gain of a traditional boost converter
- Reduced component count compared to other topologies
- One semiconductor switch is used on the DC-DC converter
- Reduced voltage stress across the switch
- The proposed DC-AC system can be used in grid fall back configuration.

1.5 Limitations

The major limitations of this research is that only simulation of the proposed DC-AC converter topology can be done, resulting from not having a well-equipped or standard laboratory facility to carry out an experiment which will validate the simulation outputs. PSCAD v4.2.1 will be used, and it provides the minimum differences between simulation outputs and experimental outputs.

1.6 Overview of the Thesis

The thesis is divided into four chapters, as follows:

Chapter 1: Overview, Statement of the Problem, Purpose of the Study, Significance of the Study, Limitations, Overview of the Thesis

Chapter 2: Literature Review for DC-DC Converters and H-bridge inverter

Chapter 3: Analysis of the Proposed Topology and Simulation Results

Chapter 4: Conclusion

CHAPTER 2
Literature Review for DC-DC Converters and H-Bridge Inverter

2.1 Introduction

The rise in use of renewable energy sources in the recent years has placed a high demand on DC-DC converters, both in terms of research and in their industrial development. They are mainly responsible for stepping up or down the voltage before it is converted to an AC waveform. And many topologies have been developed with varying properties, benefits, and drawbacks in an attempt to achieve high voltage gains, high efficiency, low component count, reduced voltage stress across switching devices, reduced losses, among other features. In this chapter, the DC-DC converter topologies listed below will be reviewed.

- Buck converters
- Boost converters
- Buck-boost converters
- Z-source converters
- Switched inductor-based converters
- Switched capacitor-based converters
- Switched inductor capacitor network based converters

The operating modes of DC-DC topologies can be analysed in CCM or DCM. During CCM the converter has two operating modes where the inductors are charging in the first mode and the inductors discharge in the second mode. With this mode of operation, the inductor current never reaches to a zero value. It increases from its lowest value which is not zero, to its peak value when energy is being stored in its magnetic field. And decreases from the peak value to its lowest value when the energy stored in the inductor's magnetic field collapses. There are three modes of operation in DCM, and the first two are similar to that of CCM. The third operating mode starts when the energy in the inductor has ran out because all the energy in the inductor has been delivered to the load at the end of second mode. This mode lasts until the switch is on again when the first mode starts. As a result, in DCM the inductor current increases from zero to its peak point, and decreases back to zero. In this review, the performance of DC-DC converters is analysed and discussed using their operation in CCM.

In DC-DC converters, there is hard switching and soft switching. Hard switching occurs when the switching device uses its own switching abilities to turn-on and off, and there is a voltage-current overlap during the switching (ON and OFF) transition, which causes losses. Ideally, current flows through the switch when it is closed and there is no voltage across the switch. And there is a voltage across the switch when it is open and no current flows through it, which makes the transition from ON state to OFF state or vice-versa instantaneous. As a result, in an ideal situation there are no power losses because at any point, voltage or current has a zero value. However, in practice during the ON and OFF switching transition, both voltage and current are applied to the switching device and they both have slightly high values (Naser, 2019). In such a scenario, the DC-DC converter experiences power losses and when this occurs, it is known as hard switching (Naser, 2019).

Soft switching is when an additional circuit is used to control the switching of the switching devices in order to force voltage or current to zero (Naser, 2019) or to shift the intersection of the voltage and current curves and minimize the losses, during the switching transition. In this switching technique, LC resonant circuits are used to control the turning on and off of the power electronic switch and implement soft switching to reduce the amount of unused power dissipated (Power Electronics News, 2020). Soft switching techniques require more complex control circuits, and while this reduces losses, switch stresses and EMI, it also increases the component count of the DC-DC converter (Power Electronics News, 2020). In this review, DC-DC converters are considered to be using hard switching.

According to the article by Power Electronics News (2020), PWM control techniques are implemented in power electronic converters to adjust the power delivered from input to output, and this can be done in analogue or digital domain. Under the digital domain, digital PWM techniques can be broadly classified as DC-DC converter PWM and Inverter PWM (Santra, et al., 2018). A set frequency and duty cycle is used in DC-DC converter PWM for open loop systems (Santra, et al., 2018), while inverters like Z-source require complicated PWM techniques to be implemented in open loop or closed loop systems. For instance, PWM in a DC-DC converter with one switch compares a reference DC signal to a carrier signal like saw tooth to generate the duty cycle of the converter. In this review, inverter PWM techniques will be discussed.

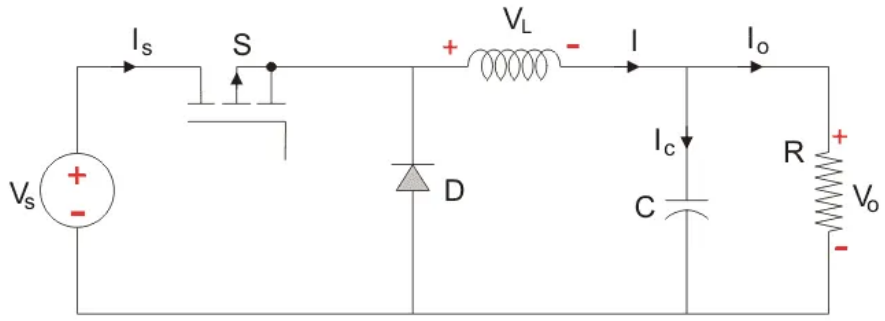
After stepping up the voltage in a DC-DC converter, and inverter is the next essential step to regulate the voltage from a DC waveform to an AC waveform. There are three types of inverter topologies that can be connected to a DC-DC topology to achieve a complete DC-AC conversion system. These are diode clamped inverters, capacitor clamped inverters, and H-bridge inverters. Among these inverter types, H-bridge inverters have the least number of components for any given voltage level. Therefore, a review of H-bridge inverters will be done in this chapter.

2.2 Buck DC-DC Converters

A buck converter is a voltage regulator that has average voltage output that is always lower than the input voltage. It is used in circuits or systems that implement voltage step down. The converter has one inductor, one capacitor, one diode and one semiconductor switch. Figure 3 shows a buck topology.

Figure 3

Buck Converter Topology



During mode 1 the switch S is closed as shown in Figure 4. During this mode the energy from the DC supply flows through the inductor, capacitor and load, and the diode is not conducting. The L and C elements are storing their energy in this operating mode. Inductor current increases linearly to a peak value from a low value. Equations (2.1) to (2.9) shows a mathematical analysis of mode 1.

During mode 1;

$$V_C = V_O \qquad (2.1)$$

The time period is defined as;

$$T = T_{on} + T_{off} \qquad (2.2)$$

The switching frequency is;

$$fs = \frac{1}{T} \quad (2.3)$$

Duty cycle is;

$$D = \frac{T_{on}}{T} \quad (2.4)$$

Using KVL to analyse the buck converter in Mode 1;

$$V_{in} = V_L + V_O \quad (2.5)$$

$$V_L = L\frac{di_L}{dt} = V_{in} - V_O \quad (2.6)$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{\Delta T} = \frac{V_{in} - V_O}{L} \quad (2.7)$$

And since the switch is closed for the time; $T_{on} = DT$

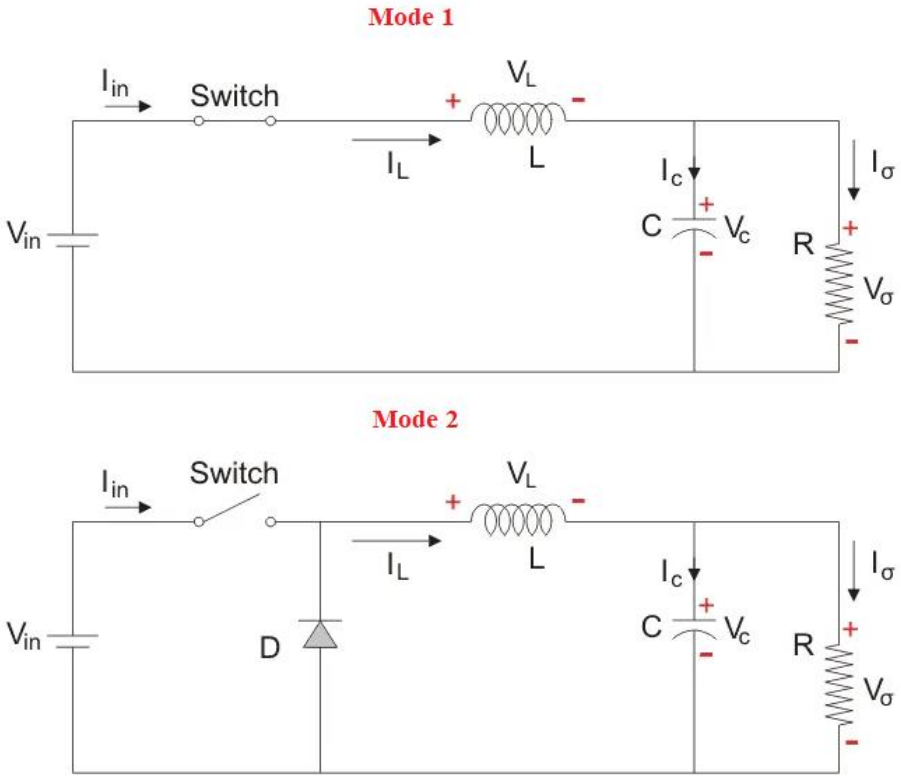
$$\Delta t = DT \quad (2.8)$$

The total change in inductor current when the switch is closed is;

$$(\Delta i_L)closed = \left(\frac{V_{in} - V_O}{L}\right) DT \quad (2.9)$$

Figure 4

Buck Converter in Operating Modes



When the switch S is opened as shown in Figure 4, mode 2 begins. During this operating mode, the diode is forward biased and it completes the loop for the energy

flow from the inductor to the load, since the inductor is discharging. The inductor current decreases from a peak value to low value, until the switch is closed again. Equations (2.10) to (2.17) show the mathematical analysis of mode 2. Additionally, the voltage gain of a buck topology is equal to D value as shown by equations (2.18) and (2.19).

Using KVL;

$$0 = V_L + V_O \tag{2.10}$$

$$V_L = L\frac{di_L}{dt} = -V_O \tag{2.11}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} \tag{2.12}$$

Since the time during which the switch is open is;

$$T_{off} = T - T_{on} = T - DT = (1-D)T = \Delta t \tag{2.13}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{(1-D)T} = -\frac{V_O}{L} \tag{2.14}$$

And the total change in inductor current when the switch is open is;

$$(\Delta i_L)open = \left(-\frac{Vo}{L}\right)(1-D)T \tag{2.15}$$

Since the net change in current of an inductor over one complete cycle is zero;

$$(\Delta i_L)closed + (\Delta i_L)open = 0 \tag{2.16}$$

$$\left(\frac{V_{in}-V_o}{L}\right)DT + \left(-\frac{V_o}{L}\right)(1-D)T = 0 \tag{2.17}$$

$$\frac{V_o}{V_{in}} = D \tag{2.18}$$

Therefore, the static gain (G) of a buck converter is given by;

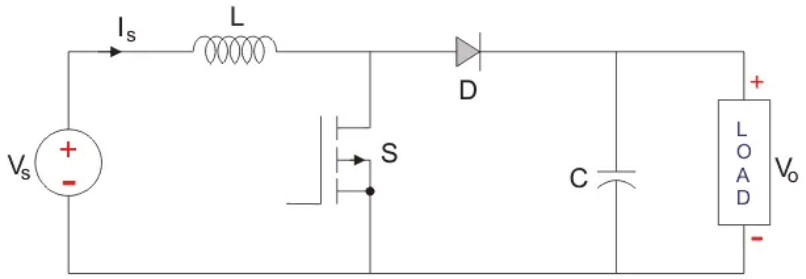
$$G = D \tag{2.19}$$

2.3 Boost DC-DC Converters

A voltage regulator that generates an average output that is equal or larger than the voltage across the input terminals is a Boost topology. This converter is implemented in circuits or systems where the input voltage has to be stepped up or increased to a higher voltage level. Figure 5 shows the conventional boost topology. The converter consists of the same components as buck converter - one inductor, one diode, one filter capacitor, and one semiconductor switch- but the arrangement is different. As a result, they regulate input voltage in different ways and produce different outputs in relation to their respective inputs.

Figure 5

Boost Converter Topology



The inductor in the boost circuit smoothens the current from the source and the capacitor limits the output voltage ripple (Bououd & Sbita, 2017). The circuit is divided into two operating modes as illustrated by Figure 6. The first mode of operation begins when S is closed, and the current which is increasing flows through the inductor (Rashid, 2013). All the current from the source is assumed to flow through the switch because it offers a path with less resistance compared to the path with a diode, capacitor and load. During the same time interval, the capacitor will be supplying energy to the load. When the switch S is opened the second mode of operation begins, and the diode provides path for current from the inductor, to the capacitor and load (Rashid, 2013). When the switch is turned off suddenly, it causes the inductor to create an opposing electromotive force (emf). This emf is in series with the source or input voltage, hence the voltage being supplied to the capacitor and load is higher than the input voltage. Equations (2.20) to (2.34) show the mathematical analysis of mode 1 and 2.

Using KVL to analyse the boost converter when the switch is closed in mode 1;

$$V_{in} = V_L \tag{2.20}$$

$$V_L = L\frac{di_L}{dt} = V_{in} \tag{2.21}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} \tag{2.22}$$

Since the switch is closed for a time;

$$T_{on} = DT = \Delta t \tag{2.23}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{DT} = \frac{V_{in}}{L} \tag{2.24}$$

$$(\Delta i_L)closed = \frac{V_{in}}{L} DT \tag{2.25}$$

Using KVL to analyse mode 2;

$$V_{in} = V_L + V_o \tag{2.26}$$

$$V_L = L\frac{di_L}{dt} = V_{in} - V_o \qquad (2.27)$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} \qquad (2.28)$$

When the switch is open for a time T_{off};

$$T_{off} = T - T_{on} = T - DT = (1-D)T = \Delta t \qquad (2.29)$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{(1-D)T} = \frac{V_{in}-V_o}{L} \qquad (2.30)$$

Inductor current when the switch is open (off) is;

$$(\Delta i_L)open = \left(\frac{V_{in}-V_o}{L}\right)(1-D)T \qquad (2.31)$$

Inductor current over one time period is zero;

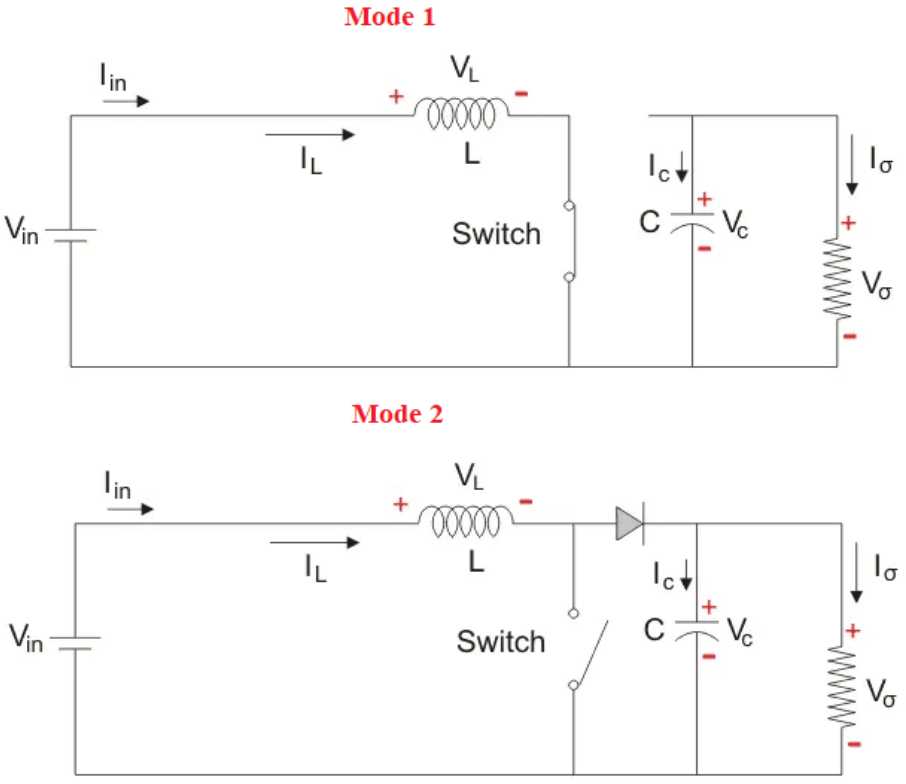
$$(\Delta i_L)closed + (\Delta i_L)open = 0 \qquad (2.32)$$

$$\left(\frac{V_{in}-V_o}{L}\right)(1-D)T + \left(-\frac{V_o}{L}\right)DT = 0 \qquad (2.33)$$

$$\frac{V_{in}}{V_o} = \frac{1}{1-D} \qquad (2.34)$$

Figure 6

Boost Converter in Operating Modes



Ideally, a boost converter can have a very high voltage gain because boost converter gain is obtained by the equation (2.34), where D is the duty cycle and is limited to values between 0 and 1. Since the gain is obtained from equation (2.34), it

means the gain will increase to infinity as the duty cycle approaches 1. However, having a very high voltage gain requires the semiconductor switches to be switched on for a longer time than they are switched off. The disadvantages of having that scenario (a high duty cycle) are, the switch is off for a short period of time and it will extend the ripple current which requires a huge inductor to suppress it, the huge maximum current switches will result in higher conduction losses, and a huge input and output current ripple is capable of seriously damaging the capacitors (He et al., 2014).

Different authors have discussed several other topologies related to or derived from boost DC-DC converters. Many of them attempt to improve one or more of the drawbacks of the conventional boost converter by implementing different control strategies or different topologies. In a paper by Kumar and Rao (2021), they reviewed various converter topologies for PV applications, like interleaved boost converters, zero switching boost converters and double boost converters. Their paper reports that an interleaved boost converter has the same gain as a traditional boost converter, it manages to distribute the input current among different elements in the topology, and it directly lessens current ripples at the input and output (Kumar & Rao, 2021). The zero-switching boost converter topology can cancel diode reverse recovery issues, and the double boost has reduced voltage stress, switching losses are decreased, and the voltage gain is doubled (Kumar & Rao, 2021).

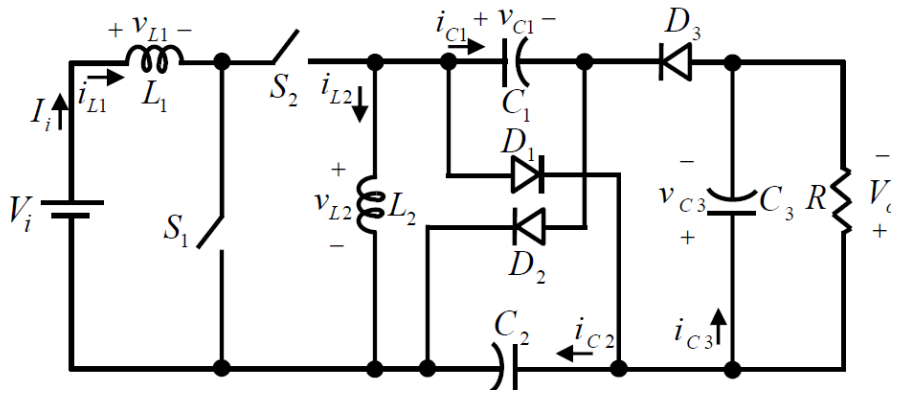
Another boost converter topology is proposed by Shahir and Azar (2018), and it is based on voltage lift technique. The topology consists of five passive elements, three diodes, and two semiconductor switches which are controlled by PWM technique. The voltage gain for this topology, and its circuit diagram are shown below in Equation (2.35) and Figure 7, respectively. With a 50% duty cycle and input voltage of 10V the average output voltage produced by their topology was 59V, and it is slightly above that of a traditional boost converter under the same conditions. However, the topology presented has a lower voltage gain compared to the other voltage lift based converters, and has higher component count too. Additionally, the maximum current and the switch voltage stress was constrained to the inductor in series connection with the source. As a result, the topology had no current ripples and had reduced voltage stress on the switch (Shahir & Azar, 2018).

The voltage gain for a converter by Shahir and Azar (2018) is given by;

$$G = \frac{(1+D)}{D(1-D)} \qquad (2.35)$$

Figure 7

Boost Converter Proposed by Shahir and Azar (2018)



Maheri et al. (2020) report that theoretically, boost converters have no current ripple at the input as an effect of the series connection between the inductor and the source, reduced voltage stress and unlimited boost ratio for unity duty cycle. However, they continued to report that in practice the drawbacks like diode recovery from reverse biased state, electromagnetic interferences, and high voltages across elements are what causes the reduction in duty cycle to 80% which also limits the gain at 5. This is the reason why most applications involving boost converters have a gain of 4 or 5. Switched capacitor technique and coupled inductor are mentioned as methods that have been employed to overcome this problem, and they do achieve high voltage gain compared to a traditional boost converter. However, they have drawbacks like current stress of switching, large input current ripple and large filters at the input (Shahir & Azar, 2018), respectively. The topology proposed in this paper has the same expression for voltage gain as the double boost converter topology mentioned in (Kumar & Rao, 2021), but it has four more components than the double boost topology.

2.4 Buck-boost DC-DC Converters

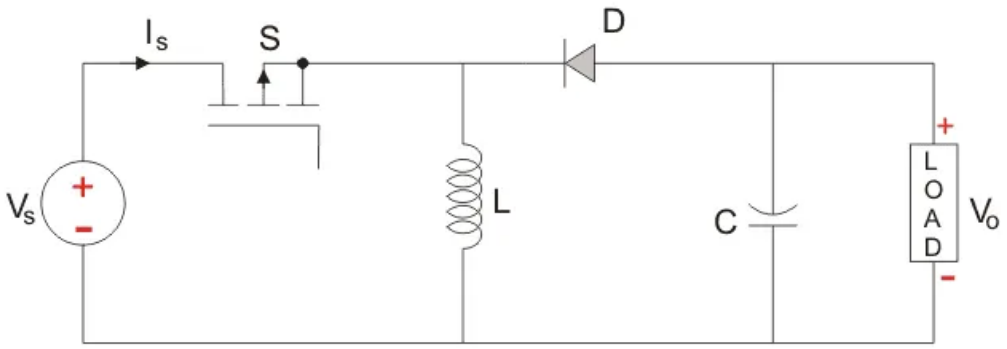
Buck-boost converters are voltage regulators capable of generating a smaller or larger output voltage compared to the input, and their polarities are different such that it's sometimes referred to as an inverting regulator (Rashid, 2013). Figure 8 shows the buck-boost topology. The buck-boost topology combines the characteristics of the

separate buck and boost topology into one circuit. The topology has an inductor, a filter capacitor, a diode and a semiconductor switch.

The buck-boost converter has two operating modes. Mode 1 is shown in Figure 9, it starts when S is closed. Current flows from the source through the switch to the inductor because the diode will be in reverse bias thereby blocking the flow of current in that direction. The current of the inductor rises from its lowest value to its peak value linearly in this operating mode, and the inductor energy being stored increases. Mode 2 is shown in Figure 9. Current flows through the load, to the diode and the inductor, resulting in the same direction of current flowing through the inductor. The current of the inductor decreases from a maximum level to a minimum value as the energy also decreases. The equations of the mathematical analysis of mode 1 and 2, and the resulting voltage gain are shown from equation (2.36) to (2.50).

Figure 8

Buck-boost Converter Topology



Using KVL to analyse;

$$V_{in} = V_L \quad (2.36)$$

$$V_L = L\frac{di_L}{dt} = V_{in} \quad (2.37)$$

$$\frac{d_{i_L}}{dt} = \frac{\Delta_{i_L}}{\Delta t} \quad (2.38)$$

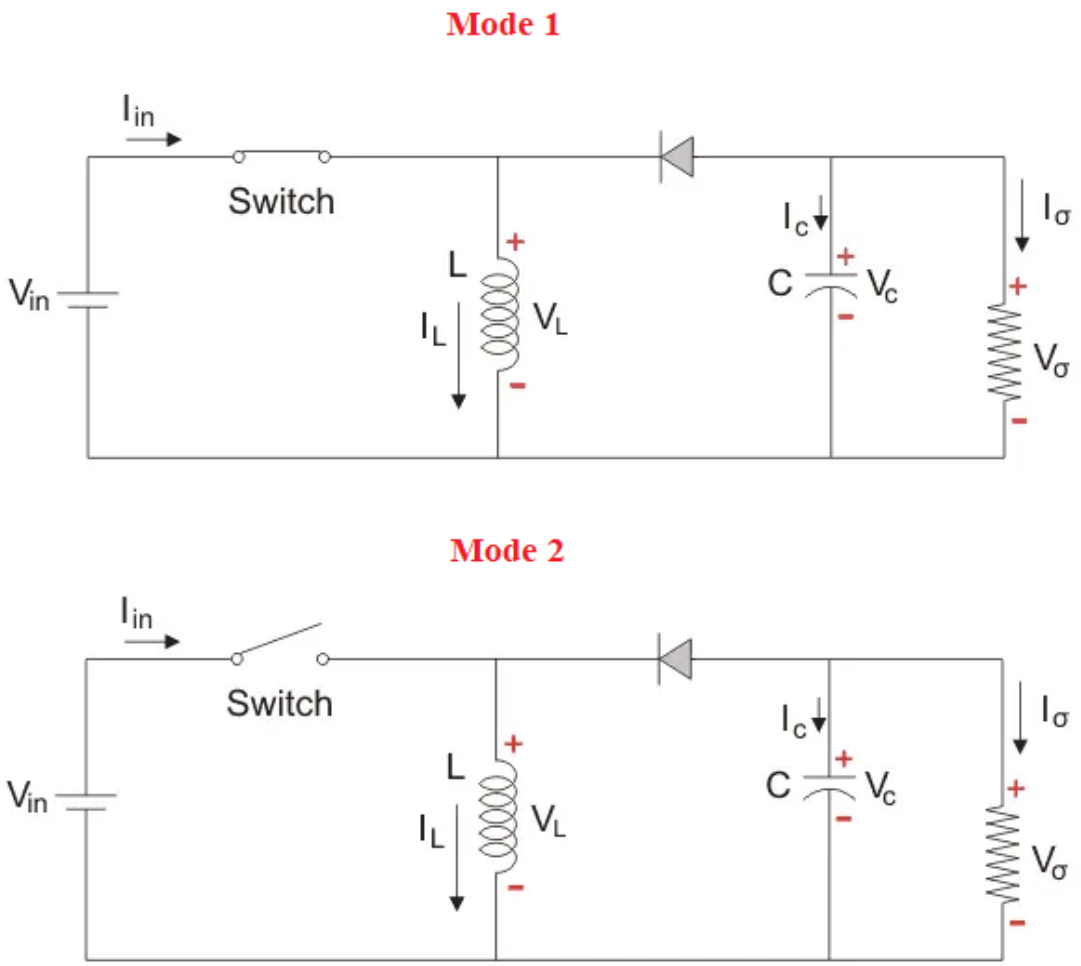
Since the switch is on (closed) for;

$$T_{on} = DT = \Delta T \quad (2.39)$$

$$\frac{d_{i_L}}{dt} = \frac{\Delta_{i_L}}{\Delta t} = \frac{V_{in}}{L} \quad (2.40)$$

Figure 9

Buck-Boost Converter in Operating Modes



And the total change in inductor current when the switch is closed is;

$$(\Delta i_L)closed = \left(\frac{V_{in}}{L}\right) DT \qquad (2.41)$$

Using KVL to analyse the buck-boost during mode 2 when the switch is open (off);

$$V_L = V_o \qquad (2.42)$$

$$V_L = L\frac{di_L}{dt} = V_o \qquad (2.43)$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} \qquad (2.44)$$

Since the switch is open during T_{off};

$$T_{off} = T - T_{on} = T - DT = (1-D)T = \Delta t \qquad (2.45)$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{(1-D)T} = \frac{V_o}{L} \qquad (2.46)$$

And the total change in inductor current when the switch is open is;

$$(\Delta i_L)open = \frac{V_o}{L}(1-D)T \qquad (2.47)$$

The net current change of an inductor is one time period is zero;

$$(\Delta i_L)closed + (\Delta i_L)open = 0 \quad (2.48)$$

$$\left(\frac{V_o}{L}\right)(1-D)T + \left(\frac{V_{in}}{L}\right)DT = 0 \quad (2.49)$$

As a result, the static gain of a buck-boost converter is given by;

$$G = \frac{V_o}{V_{in}} = \frac{-D}{1-D} \quad (2.50)$$

Where 0 < D < 0.5 results in step down, 0.5 < D < 1 results in step up, and D = 0.5 results in the same output as the input.

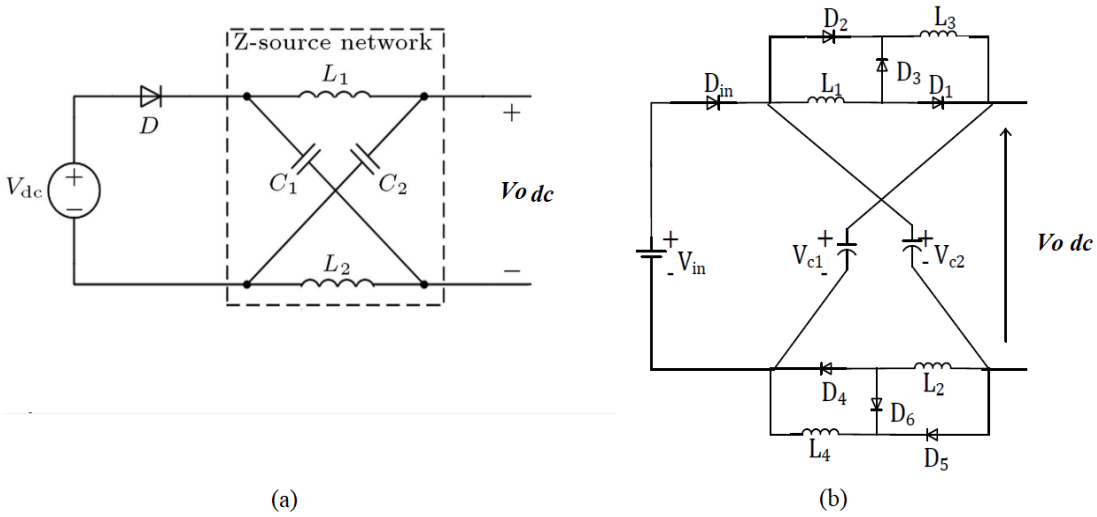
2.5 Z-source DC-DC Converters

A Z-source topology is a voltage regulator that has two capacitors and two inductors that are arranged in an X shaped structure as shown in Figure 10. Impedance-based converters came to existence as a way to overcome the shortcomings of VSI and CSI. Typically it is the inability of a VSI to step up input voltage and the risk of damaging the switches if they are misgated to cause a short circuit. Similarly, CSI are not able to step down their input voltage and also run the risk of switch damages if they are misgated to cause an open circuit. Impedance-based converters implemented as a DC-DC system have the ability to switch on the switches of the same leg (Gupta, et al., 2016). They can perform boost or buck voltage regulation to attain voltage greater or lesser than the input voltage, and the Z-source network behaves as a second order filter which can reduce the voltage ripples (Gupta, et al., 2016).

These topologies have issues like switch and capacitor voltage stress, but Gupta et al. (2016) states that switching control strategies like single boost and maximum boost methods have been developed, and modified impedance topologies like qZS and SL-ZS have been proposed to overcome such issues. ZS based converters have two operating modes namely, shoot through (ST) mode and non-shoot through (NST) mode (Gupta, et al., 2016). In shoot through mode the ZS circuit will be a short circuit, and in non-shoot through mode there will be a voltage across the output terminals. The voltage gain or boost factor of a ZS inverter is given by equation (2.51) where D is the duty cycle. The drawbacks of a ZS converter are that its inapplicable to very low input voltages, has inrush currents, has discontinuous input current, the output has a different ground with the input, and high voltage capacitors are needed which makes the converter costlier and bulkier (Gupta, et al., 2016).

Figure 10

ZS Topologies



Note. (a) ZS topology (b) SL-ZS topology

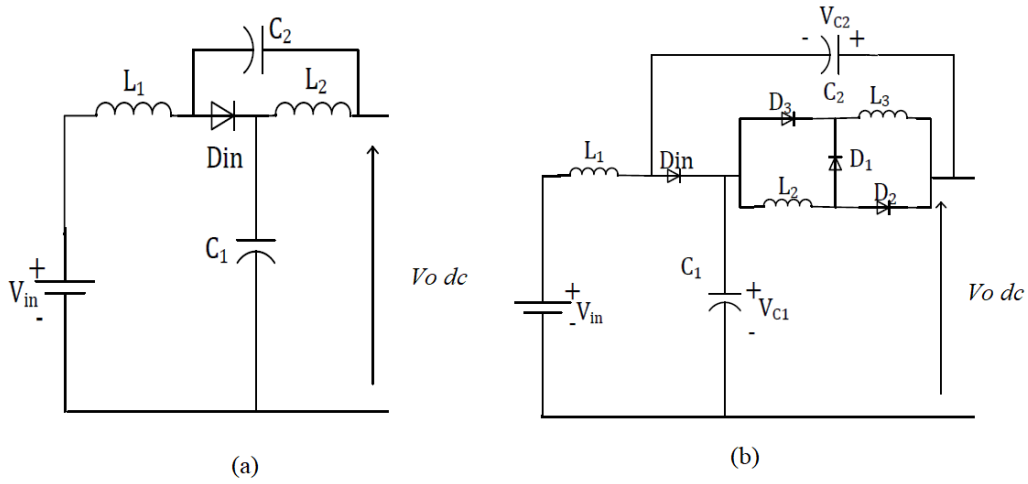
To overcome the shortcomings of a ZS DC-DC converter, other topologies like qZS, SL-ZS and SL-qZS DC-DC converter topologies were developed. A qZS topology is shown in Figure 11. The topology has reduced passive component ratings but still suffers from a duty ratio that is always less than 50% (Gupta, et al., 2016), among other merits and drawbacks respectively. A SL- ZS has switched inductor cell where an individual inductor was, in a conventional ZS topology as illustrated in Figure 10. Although there is improved output power quality in this topology, the components experience high voltage and current stresses (Gupta, et al., 2016). Finally, Figure 11 shows a SL-qZS which is a topology that combines the advantages of qZS and SL-ZS into a single topology. This allows it to have reduced capacitor voltage stress and lower inductor current stress compared to qZS, but its voltage gain is in fact lower than that of SL-ZS (Gupta, et al., 2016).

In the review made by Gupta et al. (2016), a qZS converter topology has an improved input profile and a common ground with its source input. The SL-ZS converter has increased static voltage gain with respect to the ZS. And the switched inductor qZS converter is able to suppress inrush current compared to the ZS. From a voltage gain perspective, the SL-qZS is the only converter with the most improved shoot through voltage gain ability, as illustrated by the equations (2.51) to (2.54) at 40% duty cycle. Additionally, the conventional ZS DC-DC converter topology

remains the only ZS based converter with the least component count at a given voltage gain value.

Figure 11

qZS Topologies



Note. (a) qZS topology (b) SL-qZS topology

The static voltage gain ratios for ZS, qZS, SL-ZS, and SL-qZS converters are given below at 40% duty cycle;

$$G_{ZS} = \frac{1}{1-2D} = 5 \qquad (2.51)$$

$$G_{qZS} = \frac{1}{1-2D} = 5 \qquad (2.52)$$

$$G_{SLZS} = \frac{1+D}{1-3D} = -7 \qquad (2.53)$$

$$G_{SLqZS} = \frac{1+D}{1-2D-D^2} = 35 \qquad (2.54)$$

2.6 Switched Inductor Based DC-DC Converters

Switched inductor (SL) converters are voltage regulators that make use of inductors, diodes and switches only, to adjust the input voltage to a desired output. In pure SL cells, there are no capacitors needed to achieve the task intended. SL cell come in different structures but a common structure has three diodes and two inductors as shown in Figure 12. SL based converter topologies are associated with high voltage conversion ratios compared to a boost converter, small average inductor currents which can significantly reduce the size of inductors used, and reduce the size of magnetic components if the inductors are integrated into one magnetic core on the

condition that they have the same inductance and operating conditions (He, et al., 2014).

The operation of a SL based DC-DC converter is reviewed using Sai Krishna et al. (2020)'s topology with two different sources, extracted from a traditional buck-boost topology. Figure 13 shows that the topology consists of two IGBTs without anti-parallel diodes so that no current flows between the sources, 4 diodes, 2 inductors, and a filter capacitor. The converter has three operating modes in CCM because of the two input sources.

During mode 1 shown in Figure 13, S_1 is on and S_2 is off, both inductors charge from the first input source through diodes D_1 and D_2, other diodes are reverse biased. During mode 2 shown in Figure 13, S_2 is on and S_1 is off, both inductors continue to charge from the second input source through diodes D_1 and D_2 while D_3 and D_4 are reverse biased. During mode 3 shown in Figure 13, both switches are off, energy from the inductors is delivered to the load side by means of the diodes D_3 and D_4 while the other diodes are in off state, and the voltage across the inductors is given by equation (2.63).

The drawback of this topology is that the sum of the individual duty cycles from each source should still be less than one, which also limits the voltage gain attained for a given duty cycle when compared to other single source topologies. The mathematical analysis of the three modes of operation are illustrated from equation (2.55) to (2.65), and the analytical waveforms in one period are shown in Figure 2.18.

Figure 12

Typical SL Cell

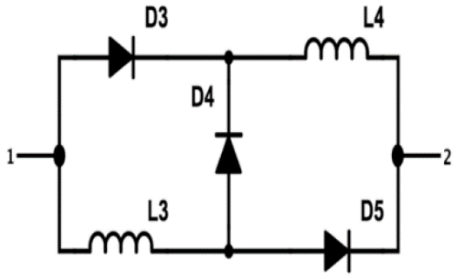
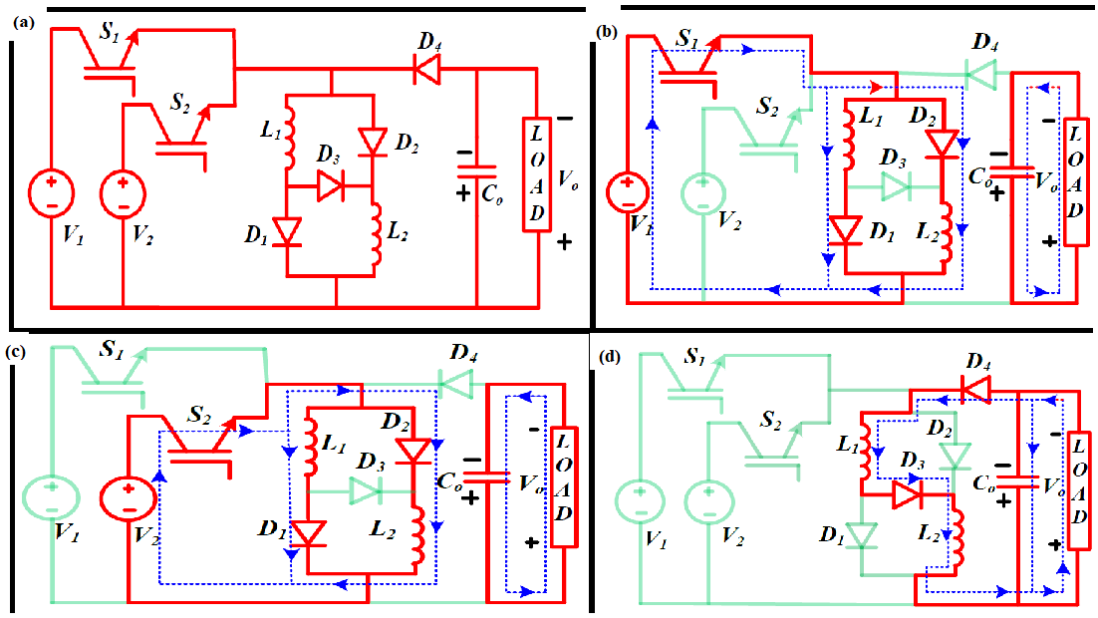


Figure 13

SL Converter



Note. (a) SL based converter topology, (b) in operating mode 1, (c) in operating mode 2, (d) in operating mode 3

The time period is defined as;

$$T = T_{on1} + T_{on2} + T_{off} \quad (2.55)$$

Duty cycle is;

$$D_1 = \frac{T_{on1}}{T} \quad (2.56)$$

$$D_2 = \frac{T_{on2}}{T} \quad (2.57)$$

Where $0 < (D_1 + D_2) < 1$

The time when the switch is on and off are defined by (2.58), (2.59) and (2.60), respectively;

$$T_{on1} = D_1 T \quad (2.58)$$

$$T_{on2} = D_2 T \quad (2.59)$$

$$T_{off} = T - T_{on1} - T_{on2} = T - D_1 T - D_2 T = (1 - D_1 - D_2)T \quad (2.60)$$

During mode 1;

$$V_{L1} = V_{L2} = V_1 \quad (2.61)$$

During mode 2;

$$V_{L1} = V_{L2} = V_2 \quad (2.62)$$

During mode 3;

$$V_{L1} = V_{L2} = \frac{V_o}{2} \qquad (2.63)$$

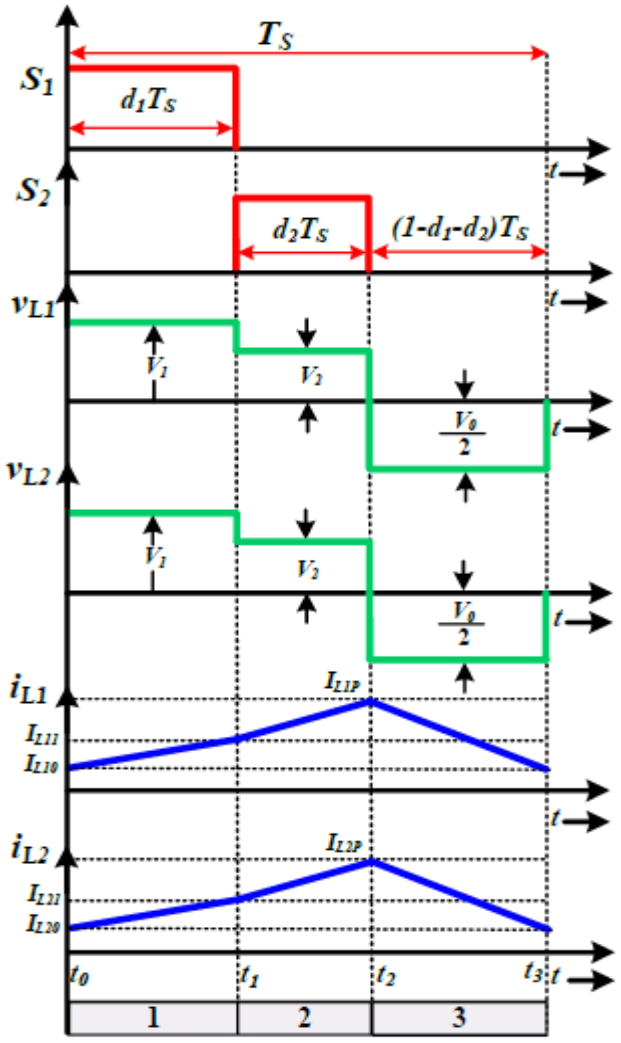
Using the voltage balance law for the average voltage across the inductor;

$$V_1 D_1 + V_2 D_2 = \frac{V_o}{2}\,(1 - D_1 - D_2) \qquad (2.64)$$

$$V_o = \frac{2(V_1 D_1 + V_2 D_2)}{(1 - D_1 - D_2)} \qquad (2.65)$$

Figure 14

SL Converter Analytical Waveforms



De Morais et al. (2017) proposed a SL structure which was derived from a Cuk DC-DC converter to achieve a high boost without increasing the duty cycle, by replacing the inductor in a conventional Cuk converter with a SL cell. The same operation of charging the inductors through the source voltage, followed by discharging the energy to the load occurs. At a 47% duty cycle, a 30V dc input voltage

fed into a De Morais et al. (2017) converter topology is regulated to 180V dc at the output. The transformer less DC-DC converter topology proposed by De Morais et al. (2017) has twice the static gain of a conventional Cuk DC-DC converter, as illustrated by the equations of their gain in (2.66) and (2.67). SL structures have an internal problem of high voltage stress on switches, because they are capable of unbalancing the current in a switching leg during a switching operation. This is attributed by the fact that during operation, inductors can be viewed as current sources connected in series.

Static voltage gain for the converter topology in (De Morais, et al., 2017) is given by;

$$G = \frac{2D}{1-D} \tag{2.66}$$

And that of a Cuk dc-dc converter is given by;

$$G = -\frac{D}{1-D} \tag{2.67}$$

2.7 Switched Capacitor based DC-DC Converters

Switched capacitor (SC) converters are voltage regulators which make use of capacitors, diodes and switches to transform the input voltage to the required level of output voltage. In pure SC cell, there are no inductors, and the cells are presented in varying structures. SC cells are used to replace an individual component in a circuit, such that their high voltage gain abilities become an added feature to the given topology. Adding a SC cell to a topology reduces the voltage across the switches, the voltage gain becomes at least double the gain of a boost converter, and all the capacitors can realise self-voltage balance (He, et al., 2014).

Chen et al. (2016) proposed to insert a SC cell in a modified PWM boost circuit, and the circuit diagram is shown in Figure 15. Two transistors S_1 and S_2 are used to drive the boost structure, whereby they switch on and off one after the other. Figure 16 shows the equivalent circuit when S_1 is on and S_2 is off, the inductor is charged by a line voltage from the source, C_3 is charged from C_1, C_4 is charged by a series voltage from C_1 and C_2, while C_1 and C_2 are discharging throughout this time interval. Figure 16 shows the circuit when S_1 is off and S_2 is on. During this time interval, C_3 charges C_2, D_4 is on while C_2 is being charged but switches off when C_2 and C_3 have the same voltage, C_1 is being charged as well, C_3 and C_4 are being discharged from the source and transferring the energy to the load (Chen et al., 2016). The analysis of the operating modes is shown in equations (2.68) to (2.82), and the

analytical waveforms of the inductor, capacitors, diodes and switches are shown in Figure 17.

Figure 15

SC Converter by Chen et al. (2016)

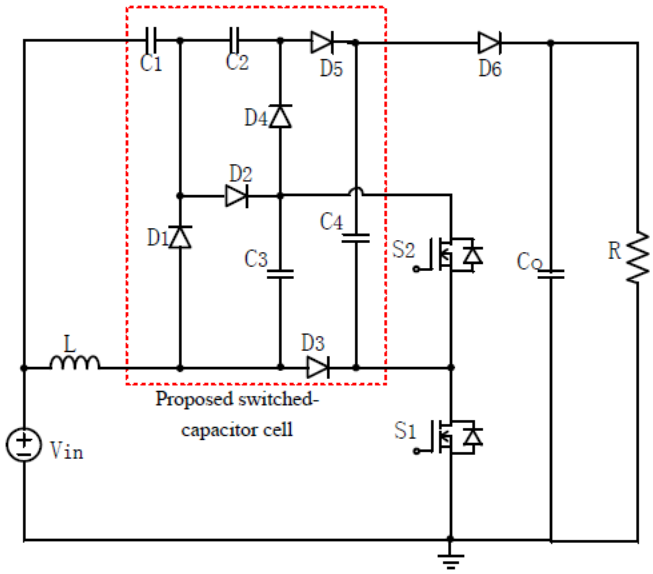
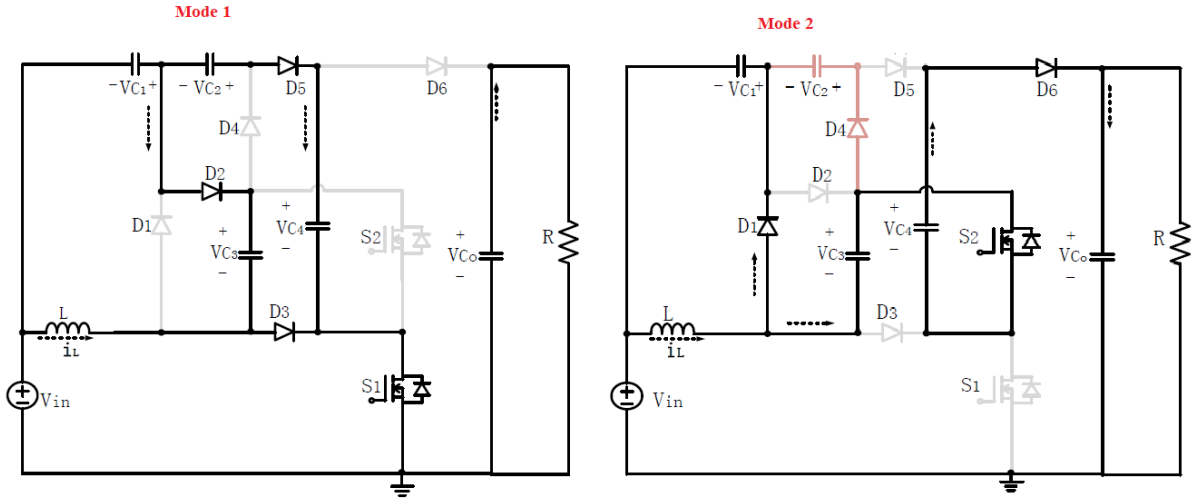


Figure 16

SC Converter in Operating Modes



During mode 1;

$$V_{in} - V_L = 0 \qquad (2.68)$$

$$V_{in} + V_{C1} - V_{C3} = 0 \qquad (2.69)$$

$$V_{in} + V_{C1} + V_{C2} - V_{C4} = 0 \qquad (2.70)$$

During mode 2;

$$V_L = V_{C1} \quad (2.71)$$

$$V_{CS} = V_{C2} \quad (2.72)$$

$$-V_{in} + V_L - V_{C3} - V_{C4} + V_o = 0 \quad (2.73)$$

$$V_{C1} = \frac{V_o}{4} - V_{in} \quad (2.74)$$

$$V_{C2} = V_{C3} = \frac{V_o}{3} \quad (2.75)$$

$$V_{C4} = \frac{V_o}{2} \quad (2.76)$$

By writing a steady-state volt-sec balance on the inductor;

$$DT * V_{in} + T(1-D)(V_{in} + V_{C3} + V_{C4} - V_o) = 0 \quad (2.77)$$

As results, the static gain of the converter is given below;

$$G = \frac{V_o}{V_{in}} = \frac{4}{1-D} \quad (2.78)$$

Voltage stress across the switches and diodes are given by;

$$V_{ds1} = V_o - V_{C4} = \frac{V_o}{2} \quad (2.79)$$

$$V_{ds2} = V_{C3} = \frac{V_o}{4} \quad (2.80)$$

$$V_{D1} = V_{C3} = \frac{V_o}{4} = V_{D2} = V_{D3} = V_{D4} \quad (2.81)$$

$$V_{D5} = V_{C4} = \frac{V_o}{2} = V_{D6} \quad (2.82)$$

Notice that the voltage across switch 1 and diode 6 are half of the output voltage, which equates to half of the voltage stress on similar components in a traditional boost converter.

The topology proposed by Chen et al. (2016) can regulate a 10V dc input voltage to 160V dc output voltage at 75% duty cycle, thereby placing its voltage conversion ratio at four times that of a conventional boost DC-DC converter. Theoretically, pure SC converters are an ideal solution for high voltage conversion ratios, except for the fact that to increase the boost capability more components or SC cells have to be included and they absorb a very pulsating current (Chen et al., 2016). Li et al. (2017) show that to achieve higher voltage gains, sometimes known as ultra-gains, more SC cells are needed. The topology proposed by Li et al. (2017) with one SC cell shown in Figure 18 has gain given by equation (2.83), a cascaded version in Figure 19 has a gain given by equation (2.84), and the experiment conducted implemented a passive version shown in Figure 19 with a voltage gain given by equation (2.85). With three SC cells, a nominal input voltage of 40V dc at 47% duty cycle, an output voltage of 300V dc.

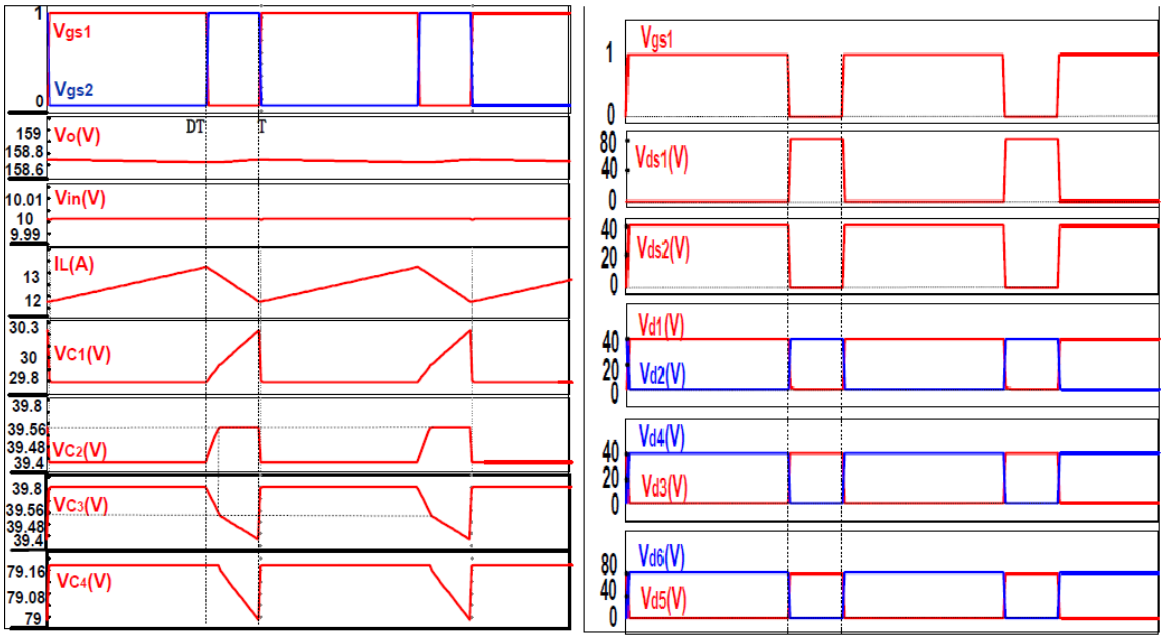
$$G_{cell} = \frac{2-D}{1-D} \quad (2.83)$$

$$G_{cas} = \left(\frac{2-D}{1-D}\right)^{n} \quad (2.84)$$

$$G_{pas} = \frac{n+1-D}{1-D} \quad (2.85)$$

Figure 17

SC Converter Analytical Waveforms



Note. Analytical waveforms for input and output voltage, diodes and switches, and inductor and capacitor elements

Figure 18

SC Converter Proposed by Li et al. (2017)

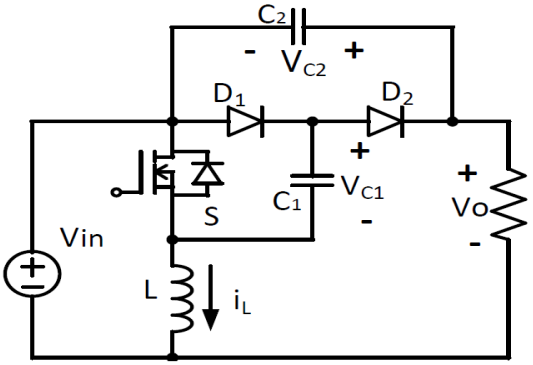
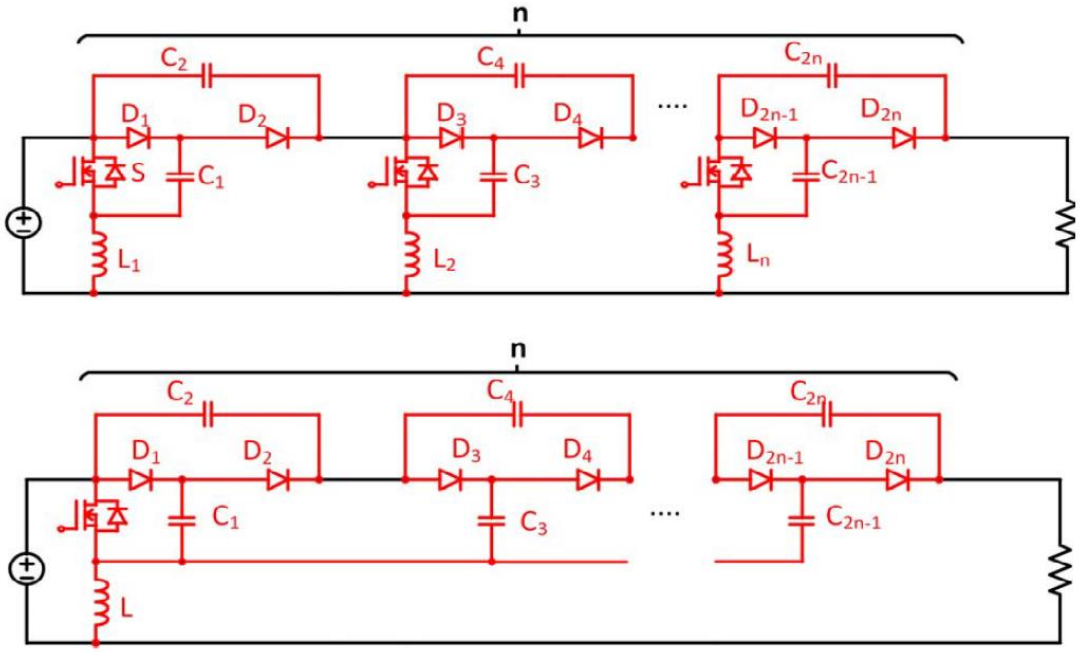


Figure 19

SC Based Converter Topologies Proposed by Li et al. (2017)



Note. Cascaded topology is above, and passive topology is below

2.8 SLCN based DC-DC converters

SLCN converters also known as hybrid switched inductor switched capacitor (SLSC) converters, are devices that combine the SL and SC structured into one converter topology. This is realised by inserting a capacitor in a conventional SL cell as shown in Figure 20, or arranging the SL and SC cells in a topology in such a way that their individual attributes are compounded into one topology as shown in Figure 21 and Figure 22. The main advantage of SLCN based converters is their ability to achieve very high voltage gain values, where some topologies can reach above 20 (Almalaq,et al., 2018). The principal operation of these networks varies, but it mainly relies on the charging of inductors in one mode and discharging them to the capacitors in the next mode of operation. During the discharge operation, inductors are connected in series which tends to increase their boost capabilities. As a result, some topologies cascaded the SL cells before they are fed into a SC cell.

The operation of a typical SLCN based converter topology is reviewed using the structure in Figure 22 proposed by Kumar and Kumar (2021). The diodes and inductors in this topology are arranged in a switched inductor structure, while the

remaining diodes form the SC structure, and the whole topology is driven by one switch.

Figure 20

SLCN Converter Proposed by Salehi et al. (2019)

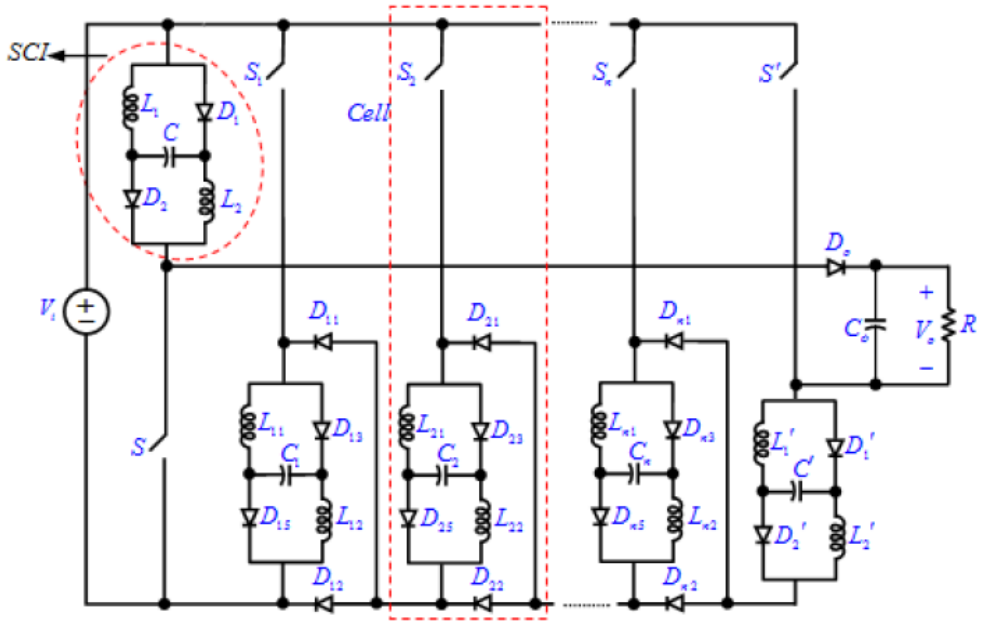


Figure 21

SLCN Converter Proposed by Almalaq et al. (2018)

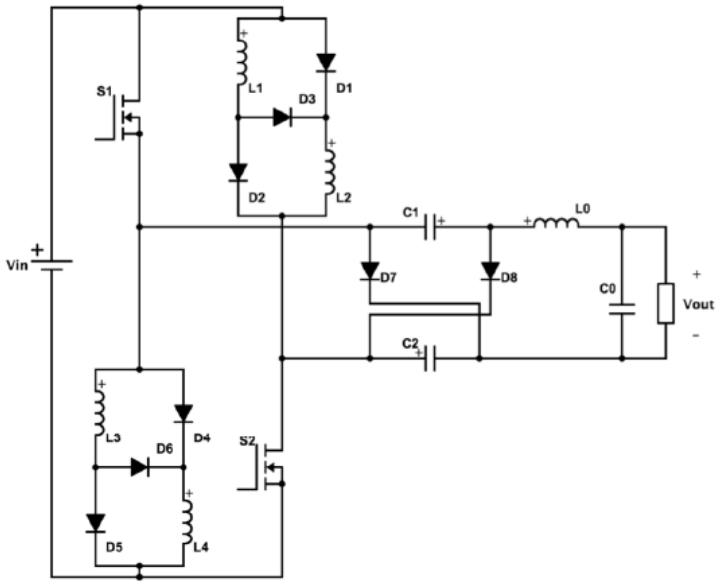
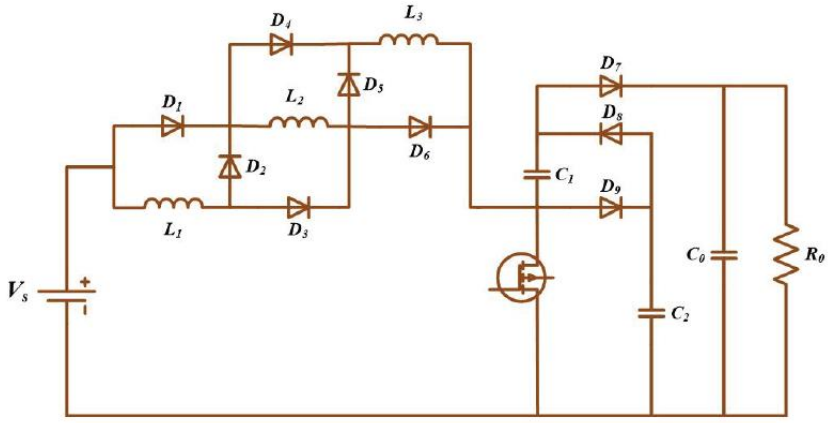


Figure 22

SLCN Converter Proposed by Kumar and Kumar (2021)



The first mode of operation of this topology is shown in Figure 23. During the first mode, the switch is on, diodes 1, 3, 4, 6, and 8 are conducting while the others are in off state, the inductors are each in a parallel connection to the source, they are storing energy whilst their current is rising from a minimum to a maximum value, the filter capacitor is discharging into the load, and capacitor C_2 is discharging into C_1. During the second mode shown in Figure 23, the switch is off, diodes 2, 5, 7, and 9 are conducting while the rest are in off state, the inductors that were in a parallel connection are now in a series connection, the inductors are discharging their stored energy to the load through diode 7 while the filter capacitor is being charged. The equations pertaining to the operating modes are from (2.86) to (2.102) below.

During mode 1;

$$V_{L1} = V_{L2} = V_{L3} = V_L = V_S \quad (2.86)$$

$$V_{C1} = V_{C2} \quad (2.87)$$

$$V_{co} = V_o \quad (2.88)$$

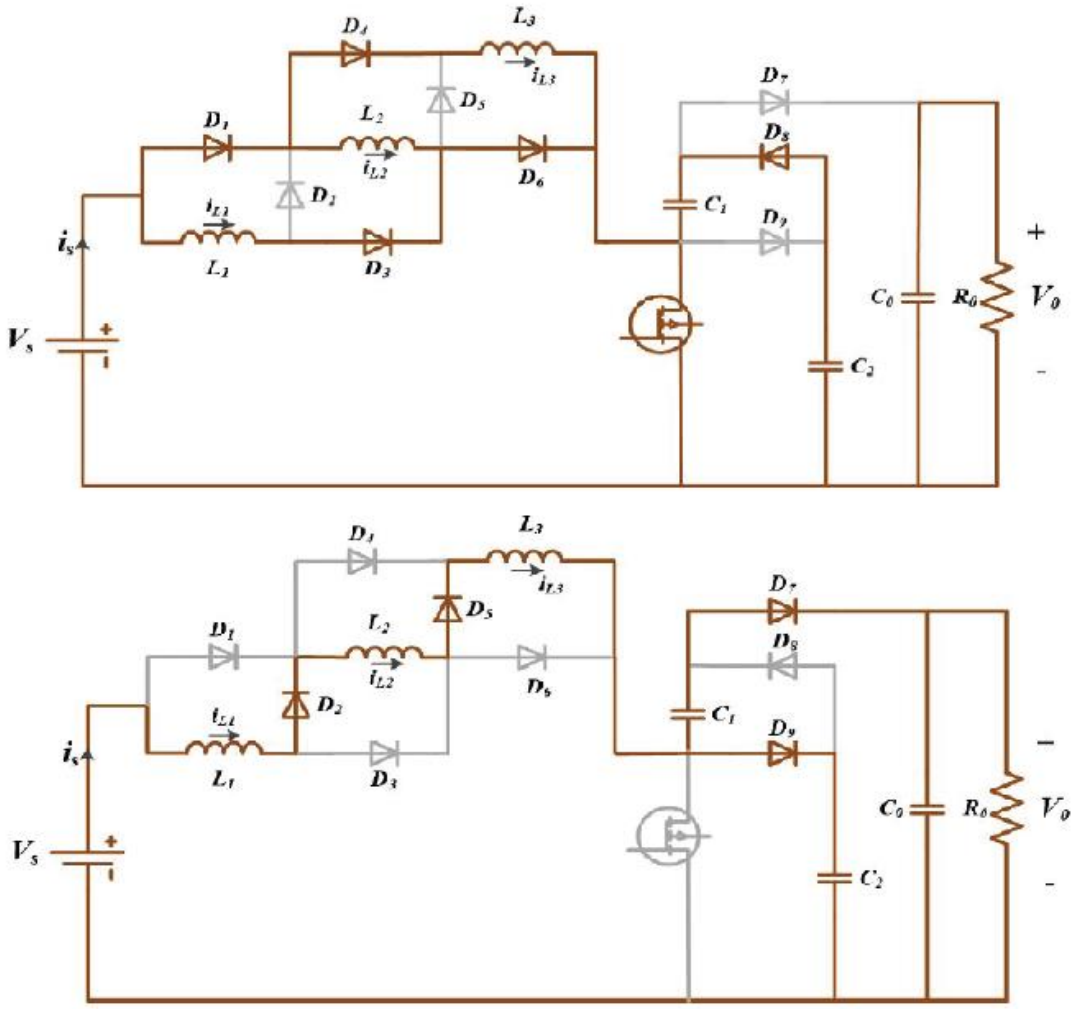
Current through each inductor is equal;

$$i_{L1} = i_{L2} = i_{L3} = i_L \quad (2.89)$$

$$i_{L1} + i_{L2} + i_{L3} = i_S \quad (2.90)$$

Figure 23

Kumar and Kumar (2021) Converter in Operating Modes



Note. (Above) operating mode 1, (below) operating mode 2.

During mode 2;

$$V_{L1} = V_{L2} = V_{L3} = V_L \qquad (2.91)$$

Using KVL;

$$V_S - V_{L1} - V_{L2} - V_{L3} - V_{C2} = V_L \qquad (2.92)$$

$$V_S - 3V_L - V_{C2} = 0 \qquad (2.93)$$

$$V_{C1} + V_{C2} = V_o \qquad (2.94)$$

According to the Voltage balance law, and using the assumptions that voltages across capacitors and across inductors are the same, respectively;

When the switch is on (DT);

$$V_{L1} = V_S \qquad (2.95)$$

And when the switch is off (T-DT);

$$V_S - V_{L1} - V_{L2} - V_{L3} - V_{C2} = 0 \quad (2.96)$$

$$V_L = \frac{V_S - V_{C2}}{3} \quad (2.97)$$

Average inductor voltage in one time period is;

$$DV_S + \frac{(1-D)(V_S - V_{C2})}{3} = 0 \quad (2.98)$$

$$2DV_S + V_S = (1-D)V_{C2} \quad (2.99)$$

Which gives the average voltage across the capacitor C_2 as;

$$V_{C2} = \frac{(1+2D)}{(1-D)} V_S \quad (2.100)$$

And under the assumption that the voltage capacitors 1 and 2 is the same;

$$V_{C2} = \frac{V_o}{2} \quad (2.101)$$

The static voltage gain of the SLCN based converter topology is;

$$G = \frac{V_o}{V_s} = \frac{2(1+2D)}{1-D} \quad (2.102)$$

Furthermore, if the topology proposed by Kumar and Kumar (2021) is extended by adding switched inductor cells as shown in Figure 24 from cell 1 to cell k, then the boost ratio for a "k" SL cell converter topology is given by;

$$G = \frac{V_o}{V_s} = \frac{2(1+kD)}{(1-D)} \quad (2.103)$$

Figure 24

Extended Version of Kumar and Kumar (2021) Converter

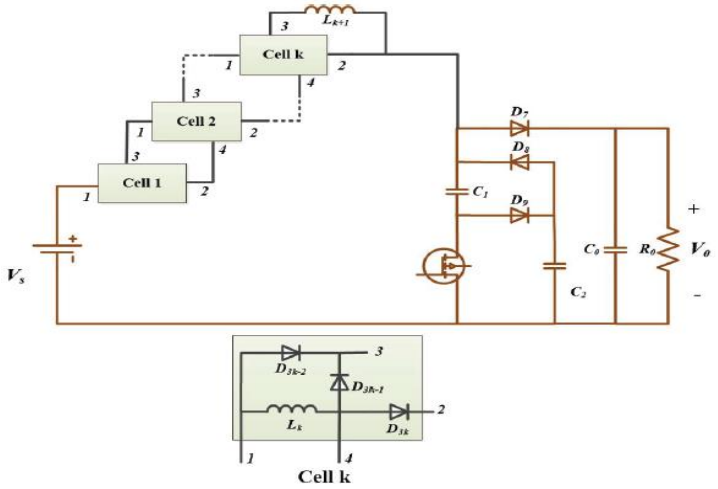
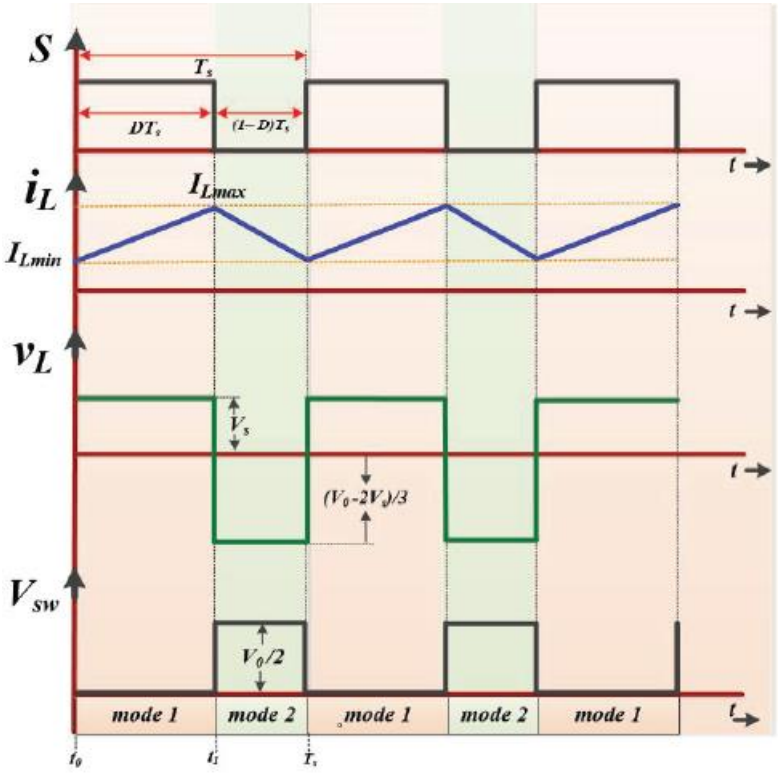


Figure 25

Analytical Waveforms for the SLCN Converter



Kumar and Kumar (2021) incorporates three SL cells into their topology and it attains a boost of 56 at a 90% duty cycle, and they recommend addition of more SL cells for higher output voltage applications. The topology proposed by Kumar and Kumar (2021) is a Cuk derived hybrid SL and SC DC-DC converter, which is capable of attaining an output which is 13 times the input voltage fed into its terminals, at a 75% duty cycle. This proves the ability of SLCN cells to enhance the boost ability of a converter, considering that a Cuk DC-DC converter would attain an absolute gain of 3 with the same 75% duty cycle.

Almalaq et al. (2018) presented another hybrid SLSC DC-DC converter shown in Figure 21, driven by two semiconductor switches, and it has two conventional SL cells arranged to feed into the SC cell structure. Theoretically, the converter Almalaq et al. (2018) proposed can boost the input voltage up to 23.5 times at 75% duty cycle. They verified the performance of the topology in MATLAB Simulink using a 12V dc input voltage, 50 kHz switching frequency and 75% duty cycle which resulted in a 280V dc output voltage. Salehi et al. (2019) proposed a similarly high gain DC-DC converter based on SLCN structures compared to the one by Almalaq et al. (2018), except that the capacitor is inserted within the SL cell. The topology proposed by

Salehi et al. (2019) is shown by Figure 20. Based on the simulation results implemented via PSCAD, an input voltage of 20V dc at 48% duty cells using two of the proposed SLCN cells, an output voltage of 250V dc is attained. Furthermore, using the expression for voltage gain associated with this topology by Salehi et al. (2019), a gain of 29 can be attained at 75% duty cycle using two SLCN cells. Table 2 below shows a comparison of selected topologies, with their voltage gain ratios, their gain values at 80% duty cycle, and the component count in each of the topologies.

Table 1

Comparison for the Discussed and Other Topologies

Converter Topology	**DC gain**	**Gain at D=0.8**	**Voltage stress across switch**	**Components**				
				L	**C**	**D**	**S**	**Total**
Buck	D	0.8	V_{in}	1	1	1	1	4
Boost	$\frac{1}{1-D}$	5	$\frac{V_{in}}{1-D}$	1	1	1	1	4
1.	$\frac{1+D}{D(1-D)}$	11.25	$Vs1 = -V_{L2}$ $Vs2 = Vin - V_{L2}$	2	3	3	3	11
Buck-boost	$\frac{-D}{1-D}$	-4	$V_{in} + V_{out}$	1	1	1	1	4
ZS	$\frac{1}{1-2D}$	-1.67	-	2	2	1	1	6
2.	$\frac{1}{1-2D}$	-1.67	-	2	2	1	1	6
SL-ZS	$\frac{1+D}{1-3D}$	-1.29	-	4	2	7	1	14
SL-qZS	$\frac{1+D}{1-2D-D^2}$	-1.45	-	3	2	4	1	10
SL	-	4	-	2	1	4	2	9
3.	$\frac{-2D}{1-D}$	-8	$\frac{2V_{in}-V_o}{2}$	3	2	1	2	7
SC	$\frac{4}{1-D}$	20	$Vs1 = \frac{Vo}{2}$ $Vs2 = \frac{Vo}{4}$	1	5	6	2	14
4.	$\frac{n+1-D}{1-D}$	11	$\frac{V_o}{n+1-D}$	1	4	4	1	10

Table 1 (Continued)

SLCN	$\frac{2(1+2D)}{1-D}$	26	$\frac{V_O}{2}$	3	3	9	1	16
5.	$\frac{4}{1-D}$	20	$\frac{V_O}{2}$	2	4	5	1	12
6.	$D+(1+D)\frac{1+3D}{1-D}$	31.4	-	5	3	9	1	18
7.	$\frac{(3+D)}{1-D}D$	15.2	$\frac{1+D}{1-D}V_{in}$	3	3	5	1	12

Note. L – inductor, C – capacitor, D – diode, S – switch. Topologies from other authors: 1. Boost converter (Shahir & Azar, 2018), 2. qZS (Gupta et al., 2016), 3. SL based converter (De Morais et al., 2017), 4. Generalised passive structure SC (Li et al. 2017), 5. SLCN (Sundaramoorthy, 2019) 6. SLCN (Almalaq et al. 2018), 7. SLCN (Arfin et al., 2019).

2.9 H-bridge Inverter

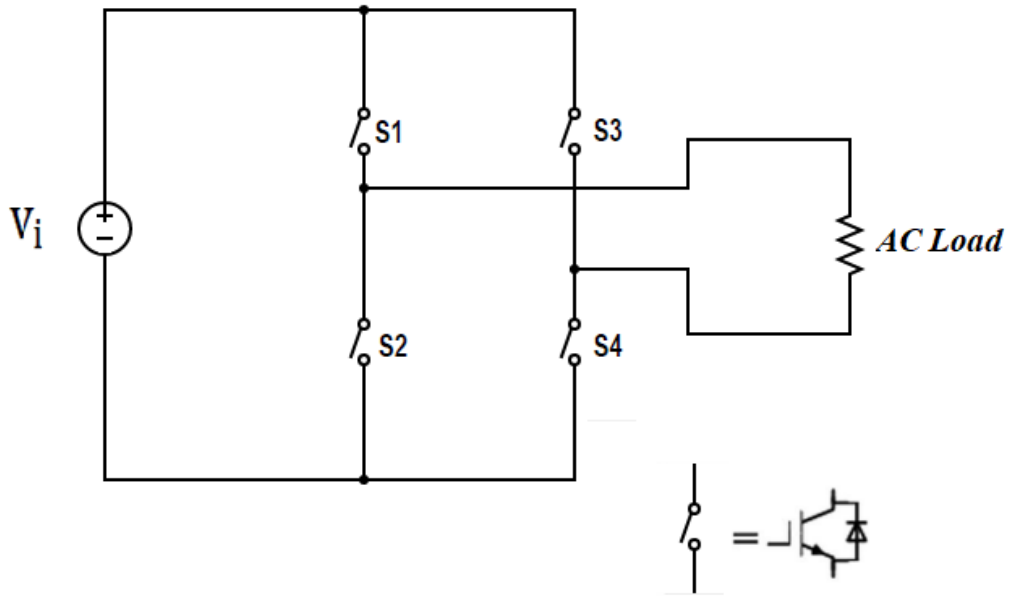
H-bridge inverters are power electronic devices which can convert DC voltage to AC voltage using four semiconductor switches. They are also known as full bridge inverters. A simple H-bridge equivalent circuit is shown in Figure 26. Switches in an H-bridge topology are turned on in a complimentary manner to avoid short circuiting the DC side of the circuit by turning on switches in the same leg. For instance, in the first half cycle S1 is switched on with S4 while S2 with S3 are off, and in the next half cycle they are reversed, respectively. Therefore, by implementing different switching modes, output voltage is positive, negative or zero at the output terminals.

Full bridge inverters have two types of output voltage waveforms namely, square waveform and sine waveform. Square wave inverters cause a humming sound and heating up of AC loads in some instances, and they are generally known to cause rapid reduction of life cycle in electrical appliances due to poor power quality (Das et al., 2020). H-bridge inverters can also be classified as three level inverters and multilevel inverters. Three level inverters have a single positive and negative voltage level, whereas multilevel inverters have more than one positive and negative voltage levels. However, three level H-bridge inverters suffer from power quality issues due to switching losses and high total harmonic distortion levels (Dehedkar & Thosar,

2018). In contrast, studies have shown that increasing the voltage levels of an H-bridge inverter reduces total harmonic distortion effectively (Yuditya, et al., 2020), and it is reported to decrease the requirement for filters (Dehedkar & Thosar, 2018). Other key features of multilevel inverters include their ability to achieve high output voltages from low switching frequency, low voltage stress in a given time period, less electromagnetic interference, and higher fundamental output (Alamri, et al., 2015).

Figure 26

H-Bridge Inverter Topology



Inverter PWM techniques are used in H-bridge inverters to transform a normally square waveform to a sinusoidal waveform at the output, that is, switches are opened in a pulsating manner to produce a pulsating pattern. If the average of every pulse is computed the result is a stepped sine wave, which can become more sine wave like with finer pulses. The magnitude of the sine wave is controlled by the width of the pulses, hence by trimming the ON and OFF switching times, the magnitude of the sine wave is controlled.

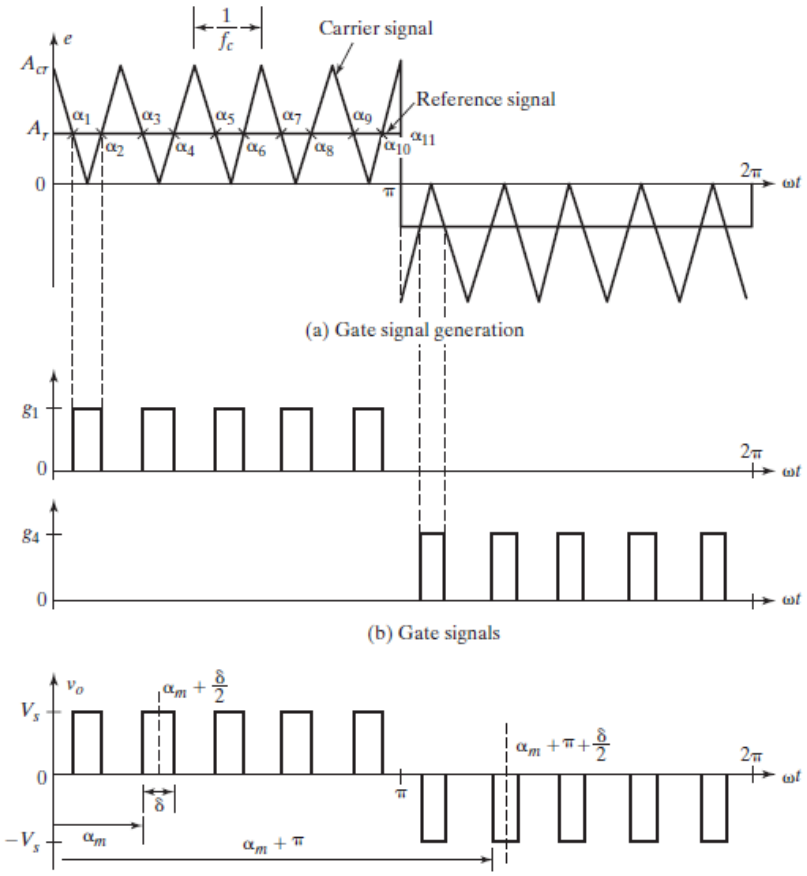
Full bridge inverters are controlled by low switching techniques where the active switch is commuted one or two times in one period, or high switching techniques like PWM where the switch is commuted numerous times in one period (Alamri, et al., 2015). Depending on the PWM technique applied, different waveforms can be achieved at the output of a full bridge inverter. The four types of PWM used to control H-bridge inverters are Single PWM, Multiple PWM, Sinusoidal PWM, and

Modified sinusoidal PWM. Sinusoidal PWM is commonly used because it is easy to understand, simple to implement, there are lower switching losses and it produces an output with less harmonics (Dehedkar & Thosar, 2018).

Single PWM compares a reference signal and a carrier signal to produce one pulse during its half cycle, and the resulting output waveform has one pulse in its half cycle. The RMS value of the output voltage in single PWM is given by equation (2.104), and is proportional to the pulse width. The pulse width is related to the amplitude modulation index. In multiple PWM, there a more pulses given by equation (2.105), and the RMS value of the output voltage is evaluated from equation (2.106). The order of harmonics in MPWM is the same as in single PWM, but the switching losses increase due to larger number of switching on and off (Rashid, 2013). Multiple PWM operation waveforms are shown in Figure 27.

Figure 27

Multiple PWM Waveforms



$$V_o = V_i \sqrt{\frac{\delta}{\pi}} \qquad where\ \delta\ is\ the\ width\ of\ a\ pulse \tag{2.104}$$

$$P = \frac{f_c}{2f_o} = \frac{M_f}{2} \tag{2.105}$$

$$V_o = V_s \sqrt{P\frac{\delta}{\pi}} \qquad where\ \delta\ is\ the\ width\ of\ a\ pulse \tag{2.106}$$

$$V_o = V_s \sqrt{(\sum_{m=1}^{P} \frac{\delta_m}{\pi})} \qquad ,where\ \delta_m\ is\ width\ of\ the\ mth\ pulse \tag{2.107}$$

Figure 28

Sinusoidal PWM Technique with Two Reference Signals

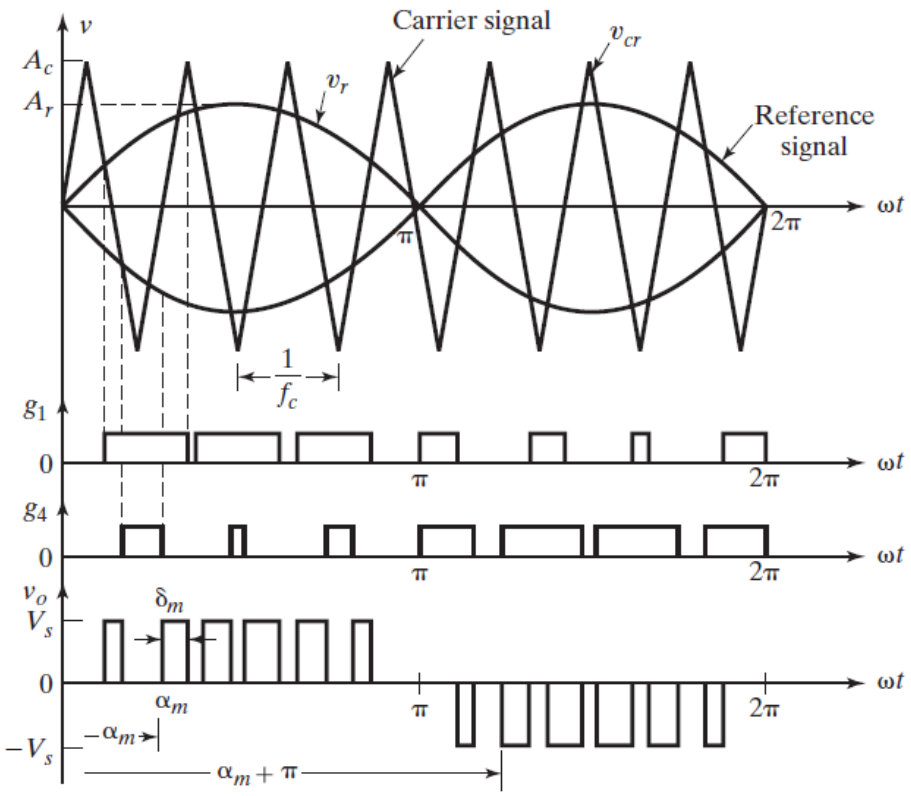
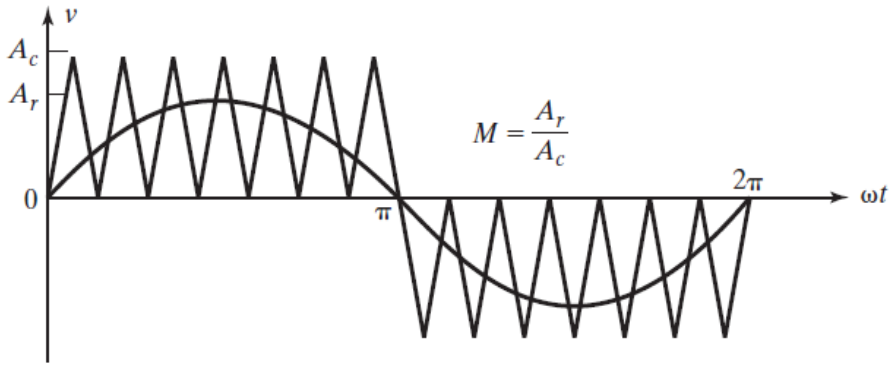


Figure 29

Sinusoidal PWM Technique with One Reference Signal



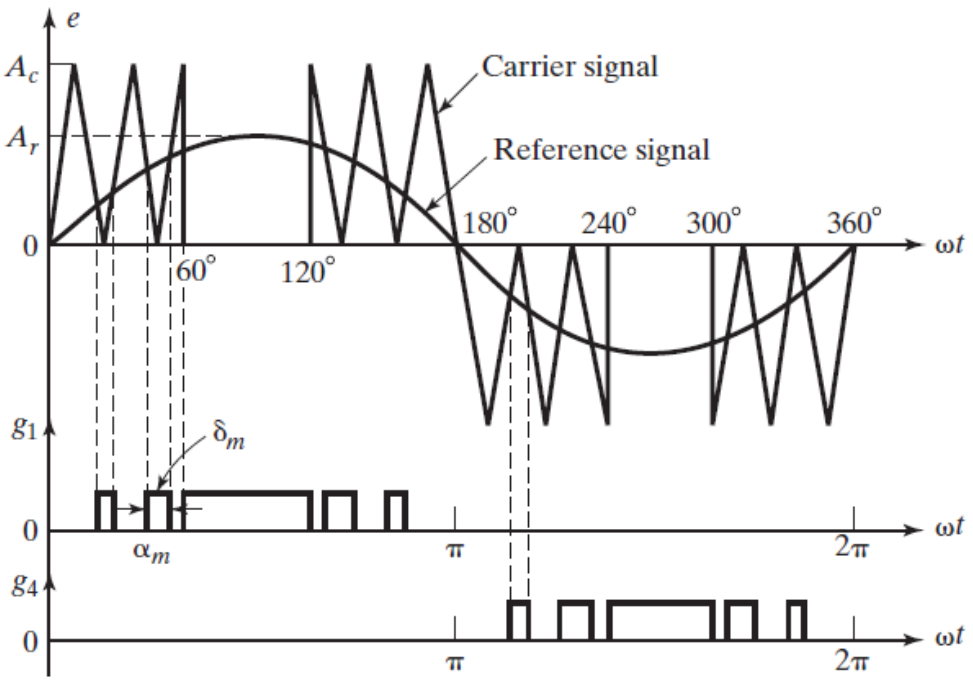
Sinusoidal PWM is used when the desired output is a sine wave, and instead of maintaining the same pulse width like in MPWM, the span of every pulse is changed in a similar way to the amplitude of a sine wave (Rashid, 2013). As illustrated in Figure 28 and Figure 29, sinusoidal PWM is achieved by comparing the intersections of a sinusoidal reference signal with a triangular carrier signal to generate the gate pulses. Since a sine wave is being used instead of a DC reference signal (in multiple PWM), the width of the pulses increases as the sine wave rises to its peak value. The RMS value produced by sinusoidal PWM and modified sinusoidal PWM technique is shown by equation (2.107). Sinusoidal PWM technique can be improved so as to apply the carrier signal in the first and last 60 degree intervals for every half cycle because the pulse widths near the sine wave peak change very little with respect to the variation of the modulation index (Rashid, 2013). And by making such changes, MSPWM is achieved as shown in Figure 30. MSPWM has an increased fundamental component, improved harmonic characteristics, reduced switching devices, and reduced switching losses, compared to sinusoidal PWM technique (Rashid, 2013).

Dehedkar and Thosar (2018) discuss the appropriateness of multilevel H-bridge inverters in single phase systems using three level, five level, and seven level H-bridge inverters. A MATLAB simulation of three H-bridge inverter topologies using sinusoidal PWM technique verifies that THD values of 30.92%, 16.95%, and 13.31% decrease with increasing inverter levels of three, five, and seven respectively. Das et al. (2020) presents the design of a 1 kW single phase inverter for standalone PV application using sinusoidal PWM. He used a 31 kHz triangular or carrier signal with two separate sine waves at zero- and 180-degree phase shift, to feed them into two comparators and they produced four sinusoidal PWM signals to control the H-bridge

inverter gates. The H-bridge inverter output is passed through a 50Hz low pass filter to produce a pure sine wave that is grid compatible, with THD value of 2.85%. Das et al. (2020)'s findings validate the generation of a pure sine wave in contrast to a square wave, and reduction of THD in a three-level inverter by use of low pass filters.

Figure 30

Modified SPWM Technique Waveforms



Alamri et al. (2015) investigate different types of losses in multilevel inverters implementing sinusoidal PWM, using a 7-level cascaded H-bridge inverter. The results of the investigation shows that switching contributes the larger portion which is 94% of all the inverter losses (Alamri, et al., 2015). The power lost when the switch opens and closes is the switching loss, and this is closely related to the switching frequency (Alamri, et al., 2015). This connects back to the sinusoidal PWM technique because the carrier frequency controls the switching frequency. Therefore, modified sinusoidal PWM is a better option as a control technique for the H-bridge inverter, in contrast to sinusoidal PWM because it generates a sine wave with less harmonics and has reduced switching losses.

2.10 Conclusion

In this chapter, it has been found that conventional boost converters can achieve high static voltage gains at extreme duty cycle. Buck-boost converters have a limited range of the duty cycle for the boost feature because they are buck converters as well. ZS converters and those derived from the impedance source topology have a mixture of drawbacks which include expensive high voltage capacitors and not being applicable to very low input voltage sources for ZS, a duty cycle that is always less than 50% for qZS, high voltage stress across components for SL-ZS, and a lower voltage gain than SL-ZS even with lower component count for SL-qZS. Semiconductor switches in SL converters experience high voltage stress due to inductor behaviour during discharge, while SC converters suffer from high component count for higher voltage gain features. As a result, SLCN converters such as one presented by Sundaramoorthy (2019) have moderate properties by combining the benefits of SL and SC cells in one topology to achieve high voltage gains. Finally, H-bridge inverters are discussed with respect to output waveform types, number of voltage levels at the output, and PWM techniques implemented. Their respective benefits and drawbacks within these classes are reviewed, and an inverter with a sinewave, three levels at the output, controlled by modified sinusoidal PWM has greater benefits based on component count and ease of control.

CHAPTER 3
Analysis of the Proposed Topology and Simulation Results

3.1 Introduction

In this chapter, the proposed topology is a two stage DC-AC converter which is a DC-DC combined with a DC-AC topology. A battery is used as input for the DC-DC topology and its output is the input of the DC-AC converter. The DC-DC topology is built from a switched inductor capacitor network (SLCN), and a single phase H-bridge inverter is used for the DC-AC converter. The DC-DC topology has 5 diodes, 4 capacitors, 2 inductors, and a power electronic switch to make a total of 12 components. It has a voltage gain of 20 at 80% duty cycle in theory. The operating modes and the corresponding mathematical analysis of the DC-DC topology are investigated in this chapter.

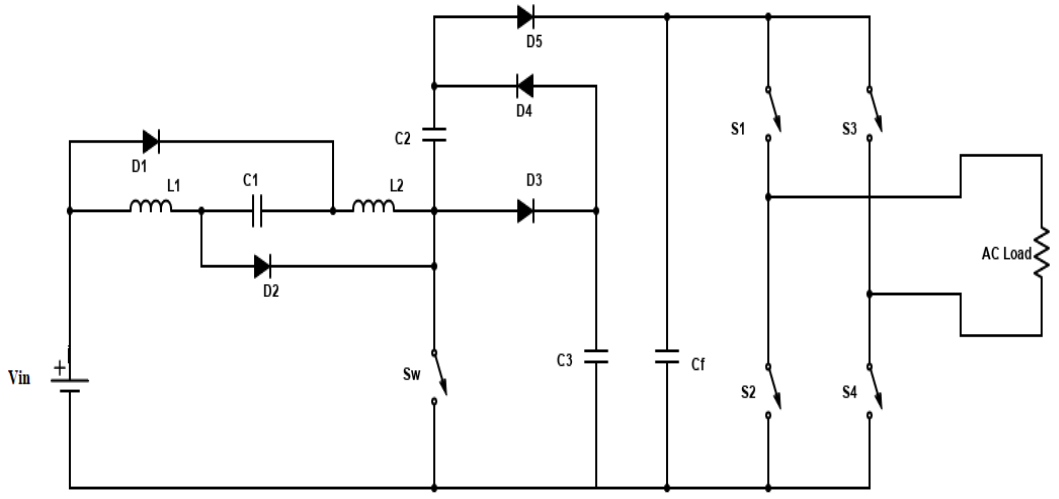
The H-bridge inverter has four power electronic switches which are controlled using modified sinusoidal PWM technique. The performance of the DC-DC and the DC-AC converters is validated by a simulation using PSCAD. And the simulation results are presented and discussed in this chapter.

3.2 Proposed Topology

Figure 31 depicts the proposed topology or the two stage DC-AC converter. The operating modes and mathematical analysis of the SLCN DC-DC converter and the H-bridge inverter are discussed in separate sections below.

Figure 31

Proposed Two Stage DC-AC Converter Topology



3.2.1 SLCN DC-DC Converter

The SLCN topology has two operating modes, and Figure 32 depicts the similar circuit of the topology in mode 1. Operating mode 1 is initiated by closing S (switching on). While the switch is closed, diodes D_3 and D_5 are in off state and diodes D_1, D_2, and D_4 are conducting. The inductors L_1 and L_2, and capacitor C_1 are connected in parallel and are being charged from the input source voltage, resulting in the same voltage across these individual elements and the source as shown in equation (3.1). The inductor currents rise from minimum values to maximum values during this operating mode. Capacitor C_3 has a double boosted voltage and it charges capacitor C_2 through diode D_4. As a result, capacitor C_2 also has a double boosted voltage as illustrated by equations (3.3) and (3.23). The current of the four passive elements being charged during this operation is flowing through the switch, and the first mode of operation ends when switch opens. The filter capacitor C_f delivers energy to the output side in this mode. The equations related to mode 1 are shown from equations (3.1) to (3.7), and the corresponding analytical waveforms for mode 1 are shown in Figure 34 from t_0 to t_1.

$$V_{L1} = \ V_{L2} = V_{C1} = V_S \tag{3.1}$$

Using KVL in the loop that contains input source and capacitor C_3;

$$\begin{cases} -V_S + V_{L1} - V_{C1} + V_{L2} - V_{C2} + V_{C3} = 0 \\ V_{L2} = Vs - V_{L1} + V_{C1} + V_{C2} - V_{C3} \end{cases} \tag{3.2}$$

Using KVL in the loop that contains C_f and C_3;

$$\begin{cases} -V_{C2} + V_{C3} = 0 \\ V_{C2} = V_{C3} \end{cases} \tag{3.3}$$

Using KVL in the loop with C_f and load;

$$\begin{cases} -V_{Cf} + Vo = 0 \\ V_O = V_{Cf} \end{cases} \tag{3.4}$$

Substituting equation (3.3) into equation (3.2);

$$V_{L2} = V_S - V_{L1} + V_{C1} \tag{3.5}$$

And the relationship between currents is expressed as;

$$i_S = i_{L1} + i_{L2} + i_{C1} \tag{3.6}$$

$$i_{C2} = i_{C3} \tag{3.7}$$

Figure 32

SLCN DC-DC Converter in Mode 1

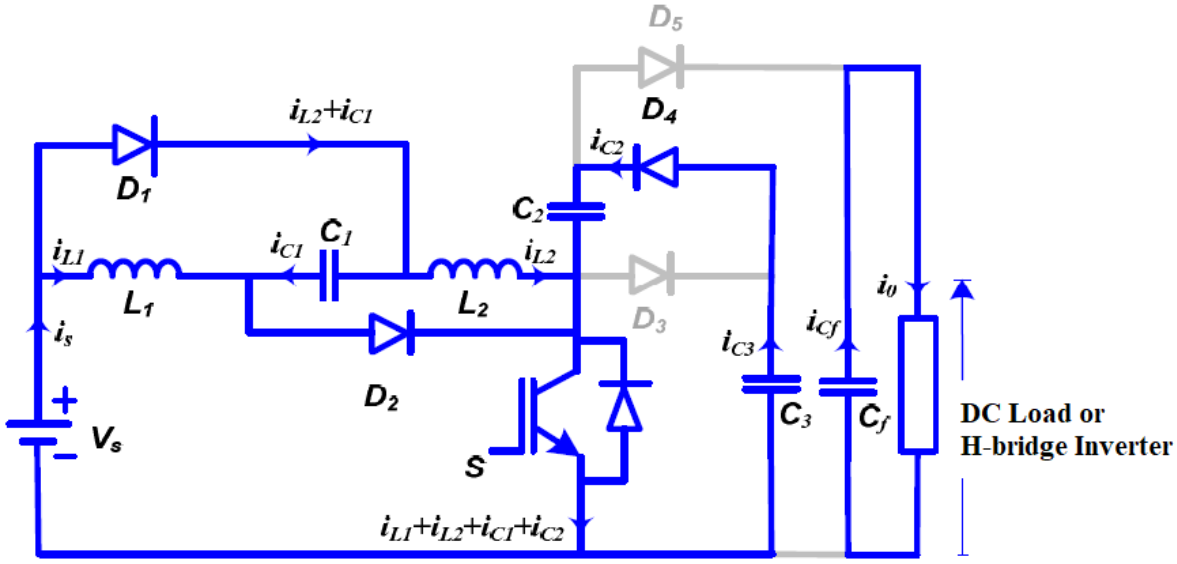
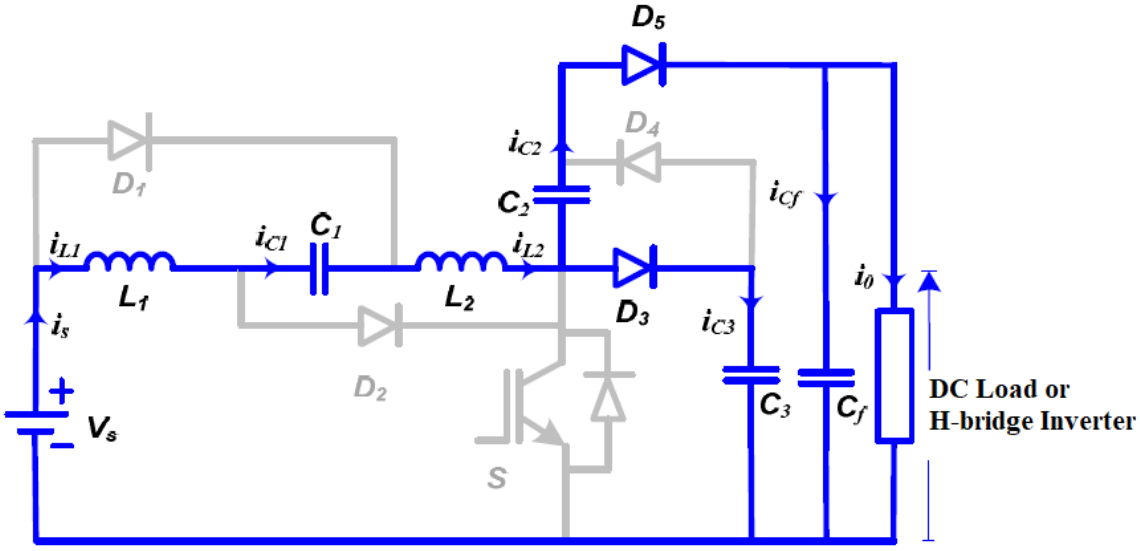


Figure 33

SLCN DC-DC Converter in Mode 2



The second operating mode is initiated by opening switch S (switching off), and the equivalent circuit of the converter during this operation is shown by Figure 33. The diodes D_1, D_2, and D_4 are in off state, while diodes D_3 and D_5 are conducting. During this operating mode, inductors L_1 and L_2, capacitors C_1 and C_2, and the input deliver energy to the load. Simultaneously, the input source, inductors L_1 and L_2, and the capacitor C_1 discharge power to the capacitor C_3. Capacitor C_3 acquires a double boosted voltage across its terminals, as shown by equation (3.23). Inductor currents

begin to decrease from maximum values to non-zero minimum values, and the energy stored in the inductors' magnetic fields falls. The current through capacitor C_1, and inductors L_1 and L_2 is equal to input current. Equations (3.8) to (3.11) show voltage and current relations for mode 2, and the analytical waveforms are shown in Figure 34 from t_1 to T_S. Note that the inductor voltage expression during this mode shown in Figure 34, is given by equation (3.11).

Using KVL in the loop containing input source and C_3;

$$\begin{cases} -V_S + V_{L1} - V_{C1} + V_{L2} + V_{C3} = 0 \\ V_{L1} = V_S + V_{C1} - V_{L2} - V_{C3} \end{cases} \quad (3.8)$$

Using KVL in the loop containing C_2, C_3, and C_f;

$$\begin{cases} -V_{C3} - V_{C2} + V_{Cf} = 0 \\ V_{Cf} = V_{C2} + V_{C3} \end{cases} \quad (3.9)$$

Using KVL in the loop containing C_f and load, V_{cf} relates with V_o as illustrated by equation (3.4);

Using KVL in the loop containing the input source and C_f;

$$\begin{cases} -V_S + V_{L1} - V_{C1} + V_{L2} - V_{C2} + V_{Cf} = 0 \\ V_{L2} = V_S + V_{C1} - V_{L1} + V_{C2} - V_{Cf} \end{cases} \quad (3.10)$$

$$V_{L1} = V_{L2} = \frac{Vo - 4Vs}{4} \quad (3.11)$$

Notice that the physical arrangement of L_1 and L_2, and C_1 elements in relation to C_3, resemble a traditional boost converter in its inductor discharge mode. Therefore, through this schematic arrangement it can be understood why capacitor C_3 acquires a double boosted voltage with respect to a traditional boost converter in this mode. Moreover, the analysis of how capacitor 3 has a double boosted voltage is illustrated by equations (3.18) to (3.23). Analysis of the output voltage equations and the derivation of the voltage gain ratio are illustrated from equations (3.17) to (3.25).

Definitions of switching period T_S;

$$T_S = \frac{1}{fs} \quad (3.12)$$

$$T_S = T_{ON} + T_{OFF} \quad (3.13)$$

And the duty cycle is defined as;

$$D = \frac{T_{ON}}{T_{OFF}} \quad (3.14)$$

Time when the switch is closed (switched on) is defined as;

$$T_{ON} = DT_S \quad (3.15)$$

And when the switch is open (switched off);

$$T_{OFF} = T_S - T_{ON} = T_S - DT_S = (1 - D)T_S \quad (3.16)$$

Using the voltage balance law of the inductor, the average voltage of inductor 1 and 2 in one switching period is zero. Additionally, since the inductor values are the same, the voltage across inductor 1 and 2 is also equal.

$$V_{L1} = V_{L2} = V_L \quad (3.17)$$

$$(V_L)on + (V_L)off = 0 \quad (3.18)$$

Using equation (3.2);

$$\begin{cases} V_{L2} = V_S - V_{L1} + V_{C1} + V_{C2} - V_{C3} \\ 2V_L = V_S + V_{C1} + V_{C2} - V_{C3} \\ V_L = \frac{1}{2}(V_S + V_{C1} + V_{C2} - V_{C3}) \\ (V_L)on = \frac{1}{2}(V_S + V_{C1} + V_{C2} - V_{C3})(DT_S) \end{cases} \quad (3.19)$$

Using equation (3.8);

$$\begin{cases} V_{L1} = V_S + V_{C1} - V_{L2} - V_{C3} \\ 2V_L = V_S + V_{C1} - V_{C3} \\ V_L = \frac{1}{2}(V_S + V_{C1} - V_{C3}) \\ (V_L)off = \frac{1}{2}(V_S + V_{C1} - V_{C3})(1 - D)T_S \end{cases} \quad (3.20)$$

Using equation (3.18);

$$\begin{cases} (V_L)on = -(V_L)off \\ \frac{1}{2}(V_S + V_{C1} + V_{C2} - V_{C3})(DT_S) = -\frac{1}{2}(V_S + V_{C1} - V_{C3})(1 - D)T_S \\ V_{C2}D = -V_S - V_{C1} + V_{C3} \end{cases} \quad (3.21)$$

Substituting equation (3.3);

$$\begin{cases} V_{C3}(D - 1) = -1(V_S + V_{C1}) \\ V_{C3} = \frac{Vs + Vc1}{(1-D)} \end{cases} \quad (3.22)$$

Substituting equation (3.1);

$$V_{C3} = \frac{2Vs}{1-D} = \frac{2}{1-D} V_S \quad (3.23)$$

Substituting equations (3.3) and (3.9) into equation (3.4);

$$\begin{cases} V_{Cf} = V_{C2} + V_{C3} \\ V_{Cf} = 2V_{C3} \\ V_O = V_{Cf} = 2V_{C3} \end{cases} \quad (3.24)$$

Substituting equation (3.23) into equation (3.24);

$$V_O = 2\left(\frac{2}{1-D}\right)V_S \quad (3.25)$$

Therefore, the output voltage and the static gain ratio are expressed by;

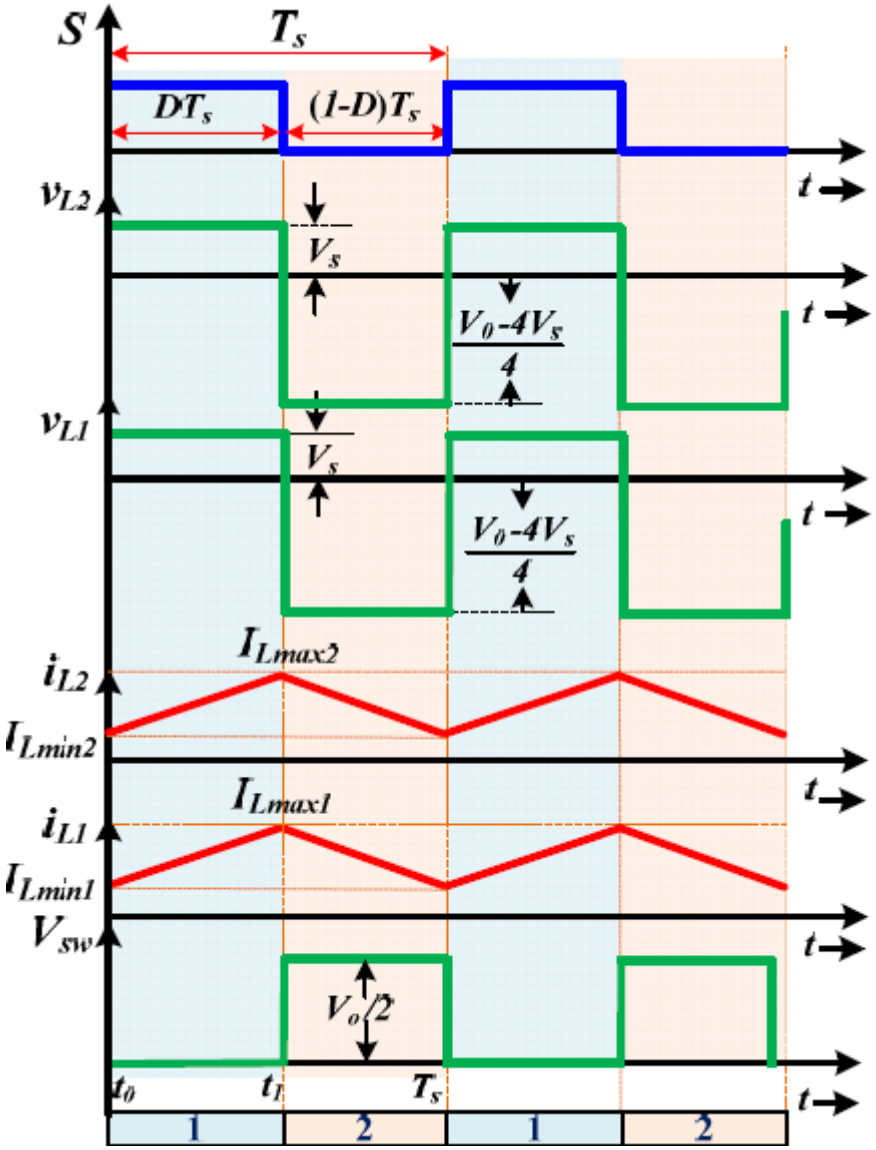
$$V_O = \frac{4}{1-D} V_S \quad (3.26)$$

$$G = \frac{Vo}{Vs} = \frac{4}{1-D} V_S \quad (3.27)$$

Notice that the static gain for the proposed topology is four times that of a conventional boost topology.

Figure 34

Analytical Waveforms for the SLCN Converter



3.2.2 H-bridge Inverter

The number of operating modes in an H-bridge inverter are 16, and they are shown in the Table 2 below. However, out of the 16 operating modes, only four are acceptable. For instance, when the power devices in the same leg are opened simultaneously there will be an open circuit (OC) at the output, and when the power devices in the same leg are closed simultaneously there will be a short circuit (SC). The equivalent circuit of a typical H-bridge open circuit is shown in Figure 35 and corresponds to the 5th operating mode. Other operating modes resulting in an open circuit are mode 1 to 4 and 9. The equivalent circuit illustrating a short circuit on the

input side of an H-bridge is shown by Figure 36 which corresponds to the 8th operating mode. Other modes of operation which result in a short circuit condition are mode 12 to 16.

Table 2
Different Operating Modes in an H-Bridge Inverter

Operation Modes	**Switch States**				**Results**
	S_1	**S_2**	**S_3**	**S_4**	
1	0	0	0	0	OC
2	0	0	0	1	OC
3	0	0	1	0	OC
4	0	0	1	1	OC and SC
5	0	1	0	0	OC
6	0	1	0	1	0V
7	0	1	1	0	-Vin
8	0	1	1	1	SC
9	1	0	0	0	OC
10	1	0	0	1	Vin
11	1	0	1	0	0V
12	1	0	1	1	SC
13	1	1	0	0	SC and OC
14	1	1	0	1	SC
15	1	1	1	0	SC
16	1	1	1	1	SC

In operating mode 6 and 11, the output voltage is zero as shown in equation (3.28). In operating mode 7 and 10, the output voltage is the negative and positive input source voltage respectively as illustrated in equation (3.28). The equivalent circuits of mode 6, 7 and 10 are shown by Figure 36 below. The H-bridge inverter is controlled using modified sinusoidal PWM. Equation (3.29) illustrate that output voltage is determined by how the carrier signal (Vc) compares to the reference signal (Vr). Additionally, gate signals of switches S_1, S_2, S_3 and S_4 are also designed to follow the inequalities shown in equations (3.30) to (3.33).

Using KVL in the equivalent circuits shown in Figure 36, the output voltage at the load terminals of an H-bridge is given by;

$$\begin{cases} V_O = 0V \\ V_O = V_{in} \\ V_O = -V_{in} \end{cases} \qquad (3.28)$$

Figure 35

H-Bridge Inverter in Open and Short Circuit Condition

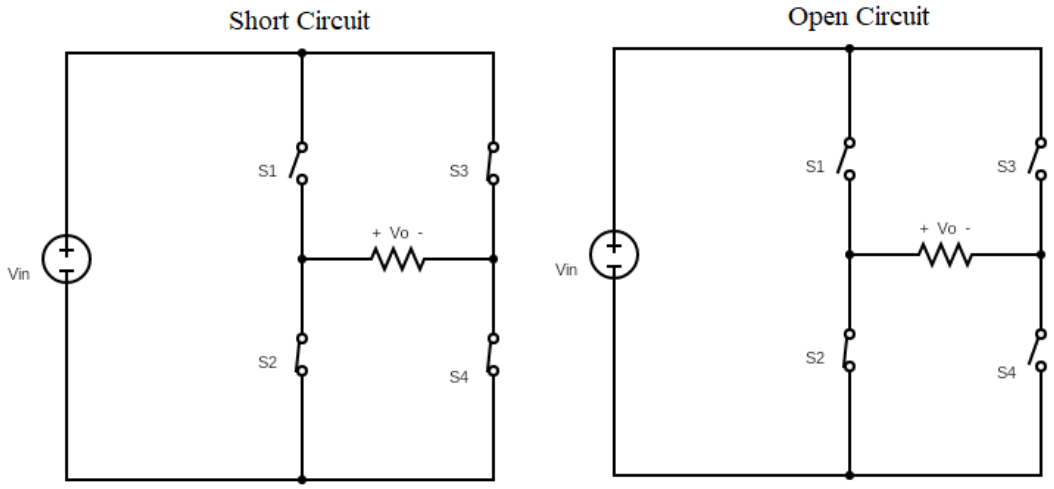
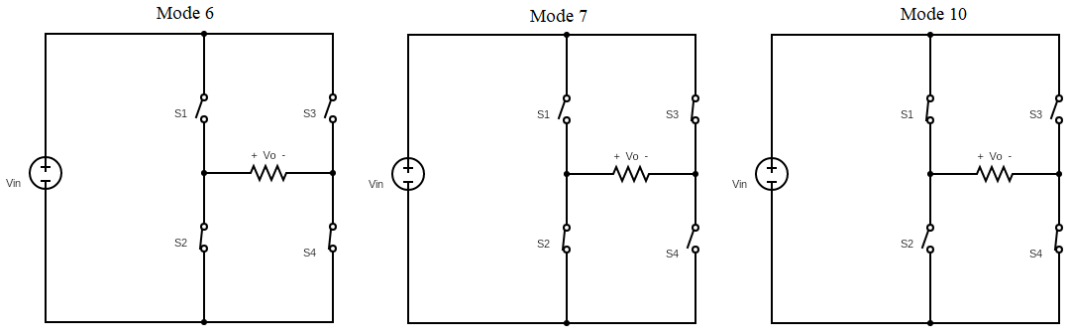


Figure 36

H-Bridge Inverter in Mode 6, 7 and 10



In PSCAD, comparators are used to implement the inequalities to generate the relevant gate signal for each switch. The value for carrier frequency is calculated as 700Hz by selecting the number of pulses (P) in the half-cycle of the output voltage to be 6, and using the equation (3.34). Analytical waveforms for MSPWM implemented on an H-bridge inverter are shown by Figure 37 below. The waveforms give an illustration of the gate signals and output waveform as they are generated from a comparison of the carrier signal (triangular) with the reference signal (sinusoidal).

And these output voltages shown in equation (3.28) are generated when the following output equations are satisfied respectively, in MSPWM technique;

$$\begin{cases} V_r < V_c \ and \ -V_r > -V_c \\ V_r > V_c \\ -V_r < -V_c \end{cases} \qquad (3.29)$$

The gate signals are also generated when the following inequalities are satisfied;

S_1 is ON when $V_c < V_r$ (3.30)

S_2 is ON when $V_r < V_c$ (3.31)

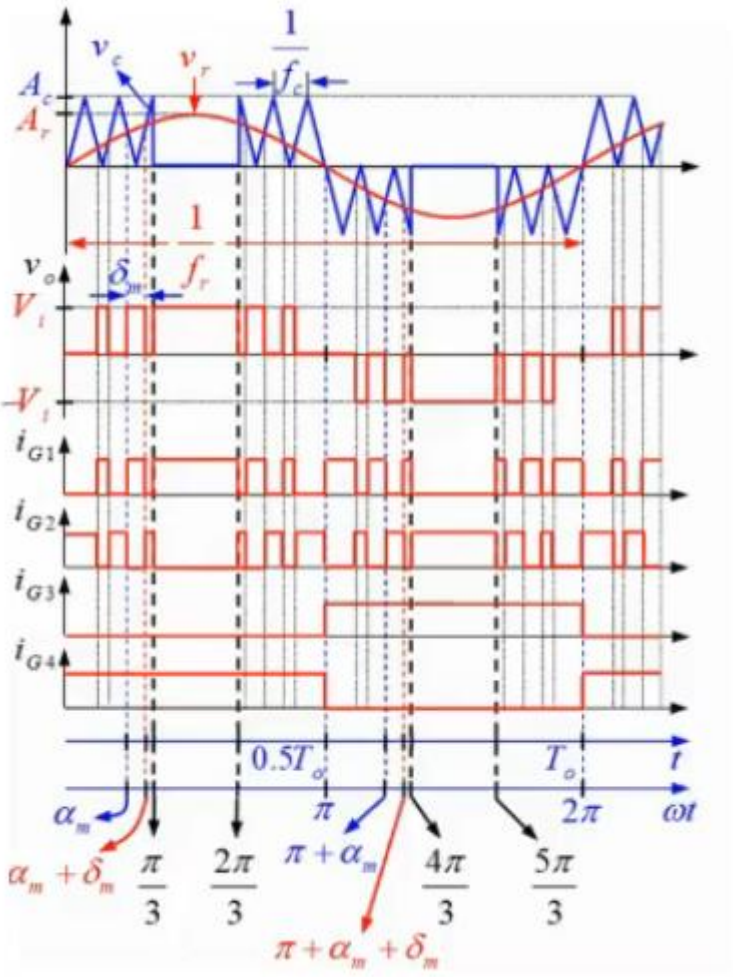
S_3 is ON when $V_r < 0$ (3.32)

S_4 is ON when $V_r > 0$ (3.33)

For a number of pulses, P in the half cycle, carrier frequency is given by;

Figure 37

Theoretical Waveforms for Modified Sinusoidal PWM Technique



3.3 Simulation Results

PSCAD simulation was carried out to validate the performance of the proposed converter topology that was discussed in the previous sections. Simulation variables for the DC-DC side and the DC-AC side of the converter are given in Table 3 below. The various input and output waveforms generated from the simulations are shown from Figure 38 to Figure 53 below. Table 4 is constructed to illustrate the overall performance of the proposed converter topology and to justify its application to interface a solar charged battery system.

Table 3

Simulation Parameters for the Proposed Converter Topology

DC-DC converter simulation parameters	
Input voltage, Vs	12V dc
Capacitors C_1, C_2, C_3, C_f	470μF
Inductors L_1, L_2	3.3 mH
Load, R	1000Ω
Duty Cycle, D	80%
Switching frequency, fs	20kHz
Target output voltage, Vo dc	240V dc
Switch type	IGBT with anti-parallel diode
DC-AC converter simulation parameters	
Input voltage, Vin	240V dc
Load inductor, L	10mH
Load resistor, R	10Ω
Amplitude modulation index, M_a	0.7
Carrier frequency, fc	800Hz
Filter Inductors, L_1 and L_2	10mH
Filter Capacitor	500μF
Target output peak voltage, Vo ac	240V ac
Switch type	IGBT with anti-parallel diode

Figure 38

DC-DC Converter Switch Characteristics for 12Vdc input

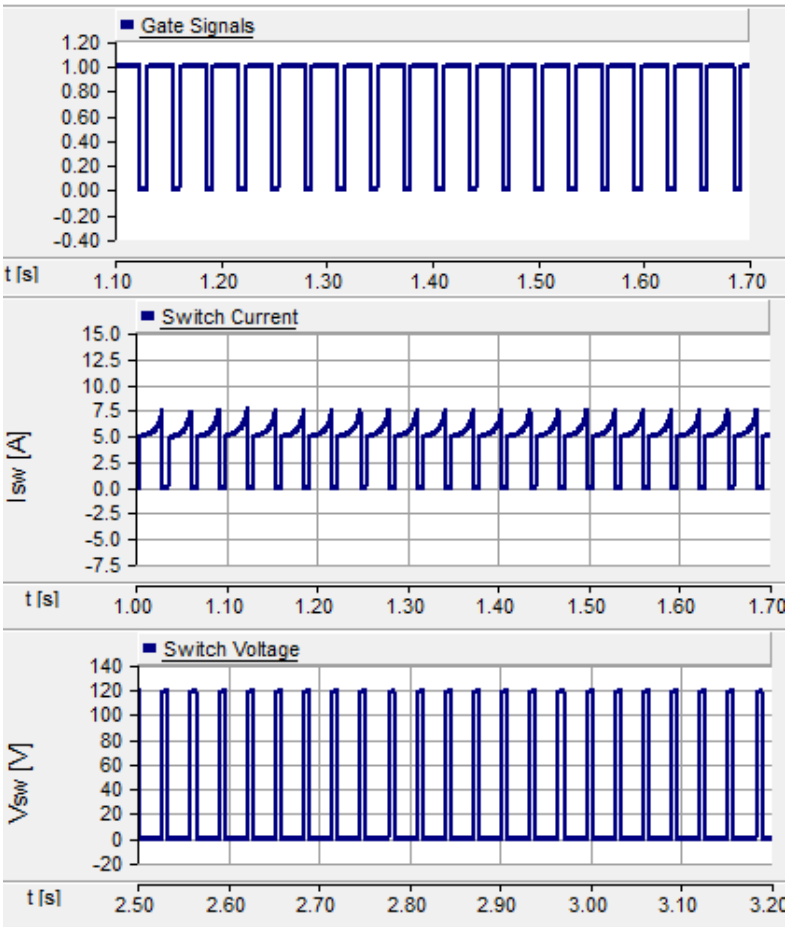


Figure 39

Inductor 1 and 2 Voltage and Current for 12Vdc input

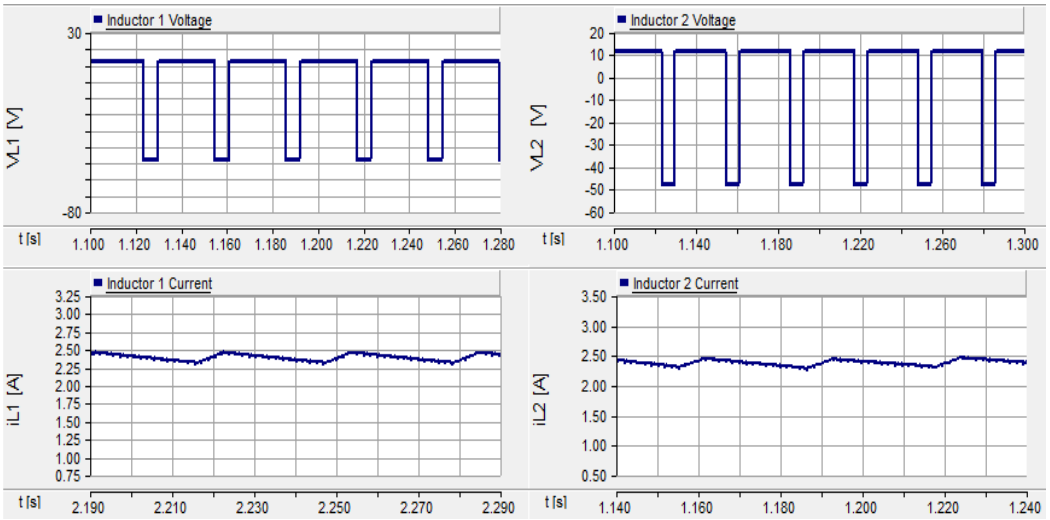


Figure 40

Capacitors Voltage and Current for 12Vdc input

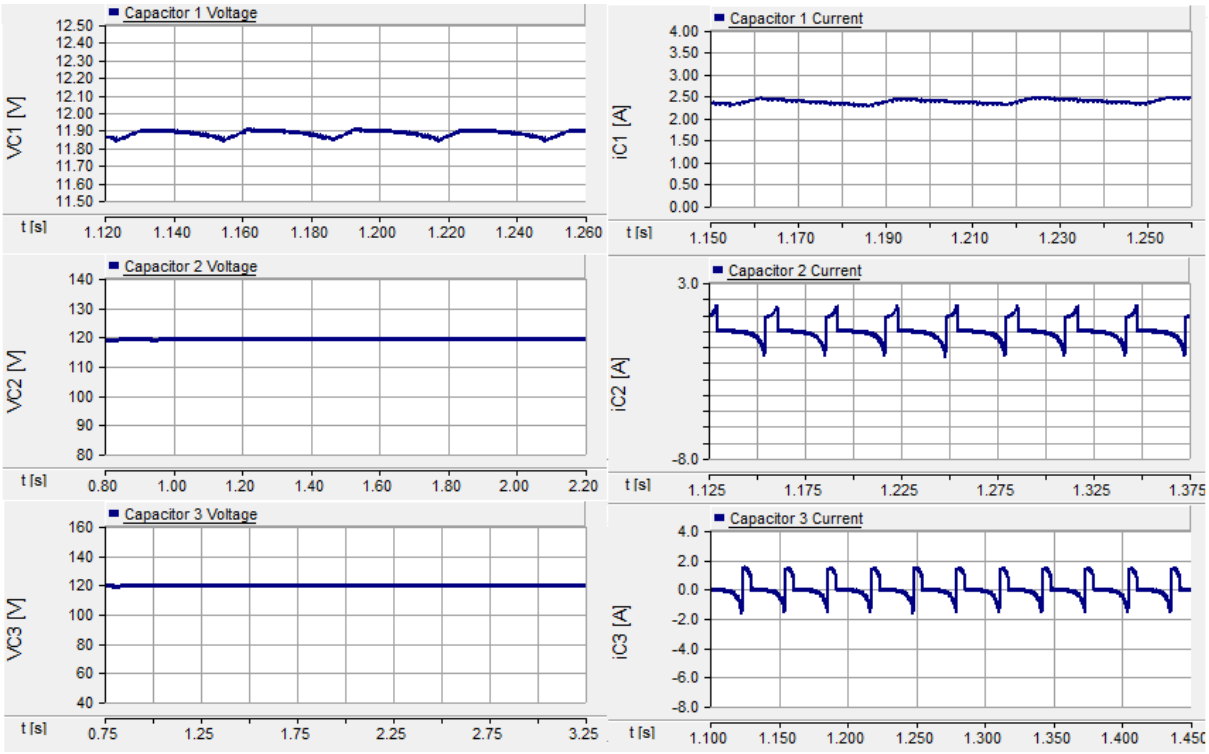


Figure 41

DC-DC Topology Output Voltage and Current for 12Vdc input

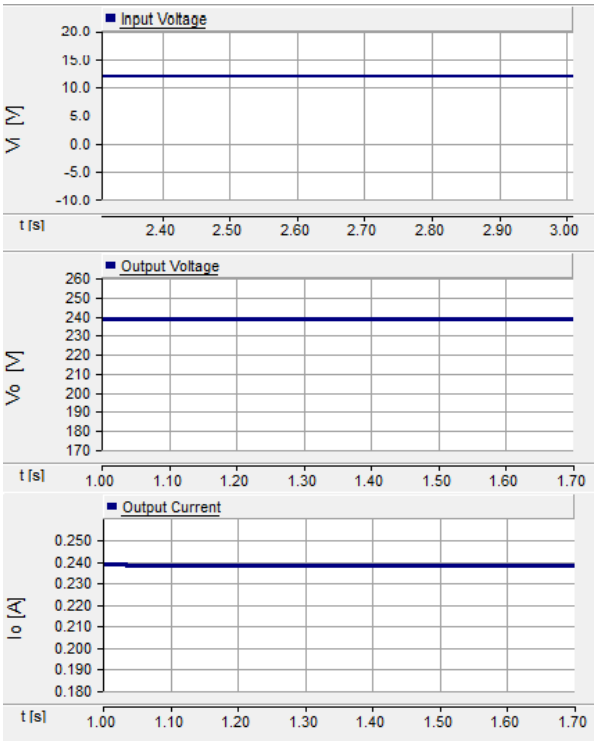


Figure 42

Switch Current and Voltage for 24Vdc input

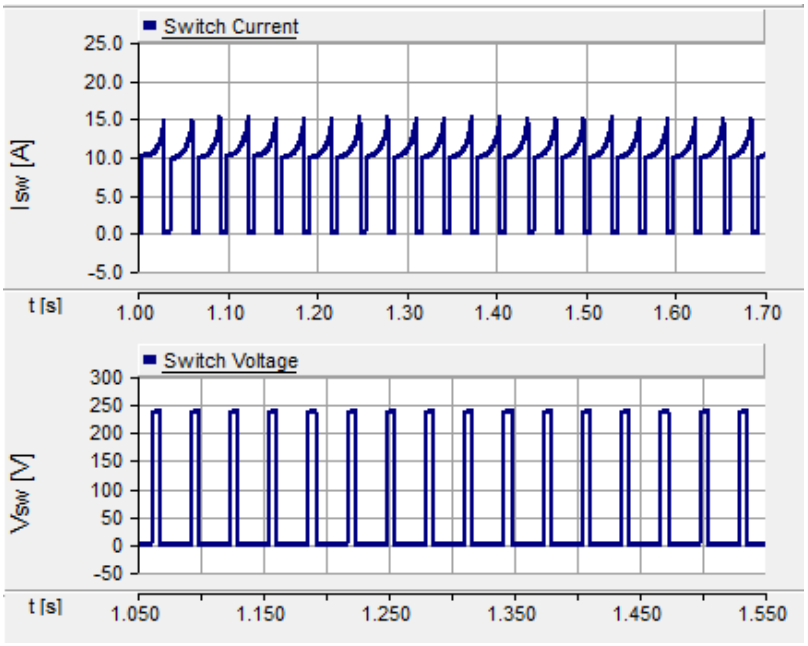


Figure 43

Inductor 1 and 2 Voltage and Current for 24Vdc input

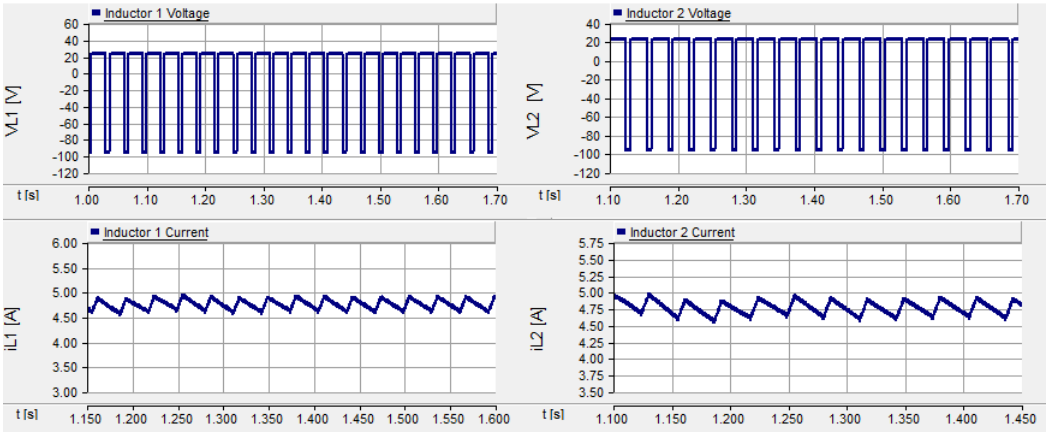


Figure 44

Capacitors Voltage and Current for 24Vdc input

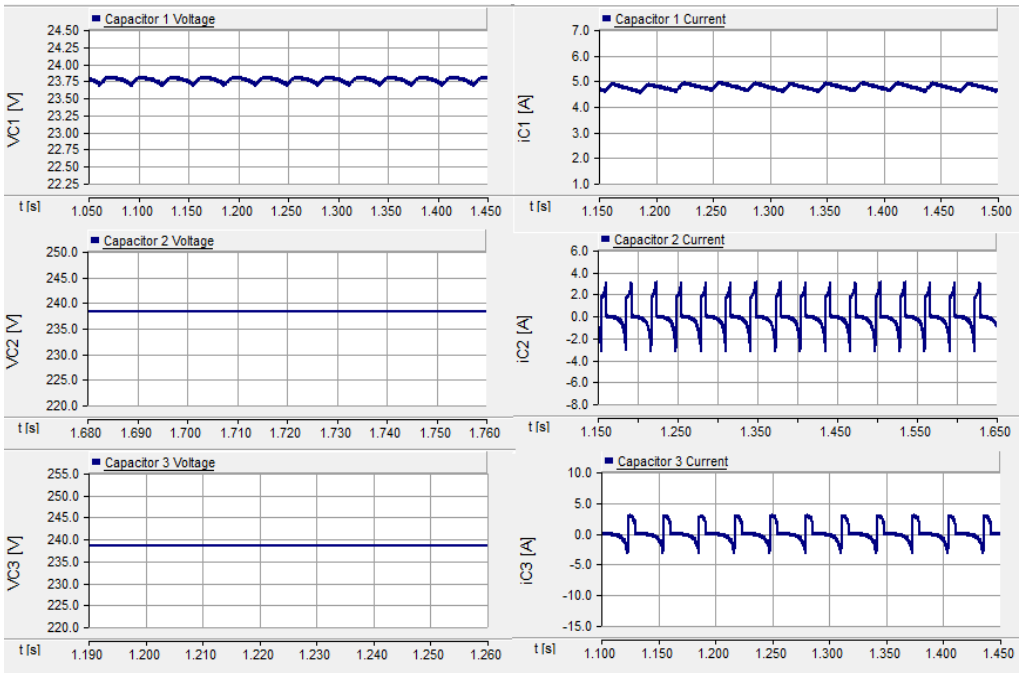


Figure 45

DC-DC Topology Output Voltage and Current for 24Vdc input

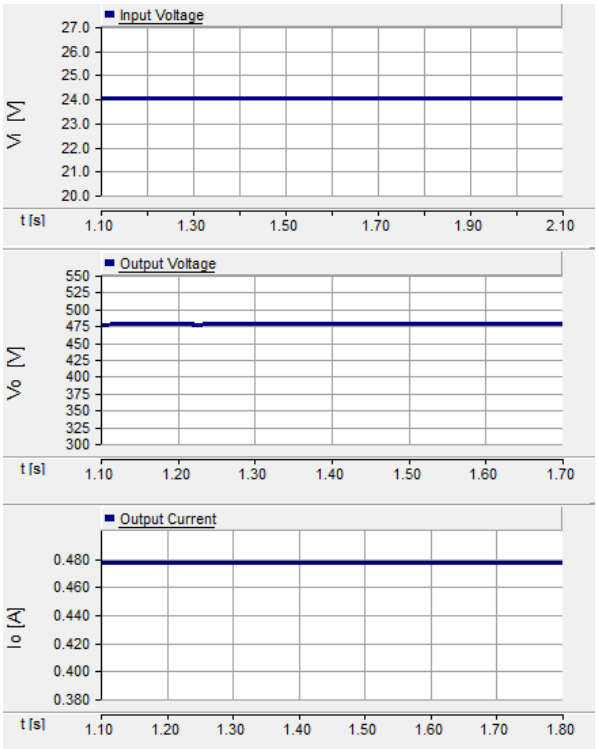


Figure 46

Switch Current and Voltage for 36Vdc input

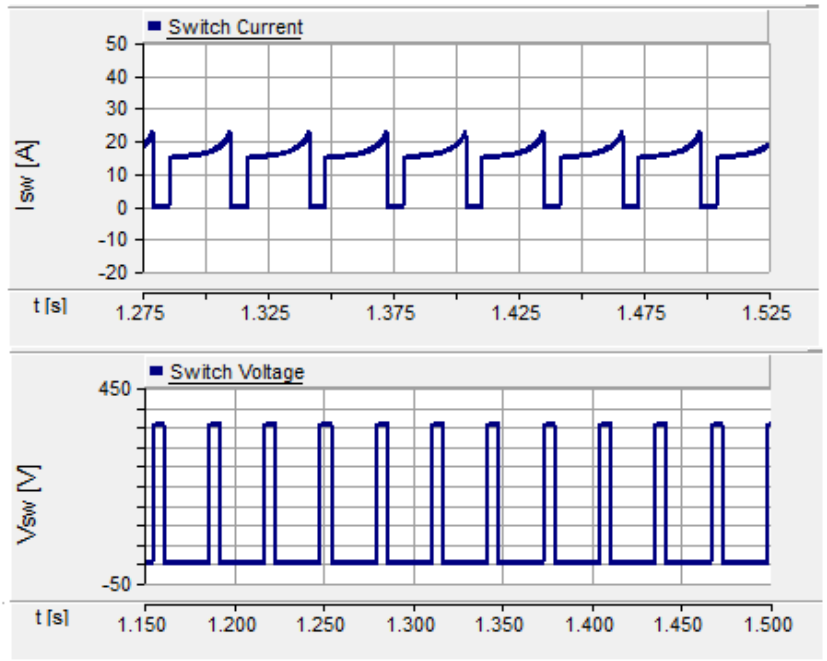


Figure 47

Inductor 1 and 2 Voltage and Current for 36Vdc input

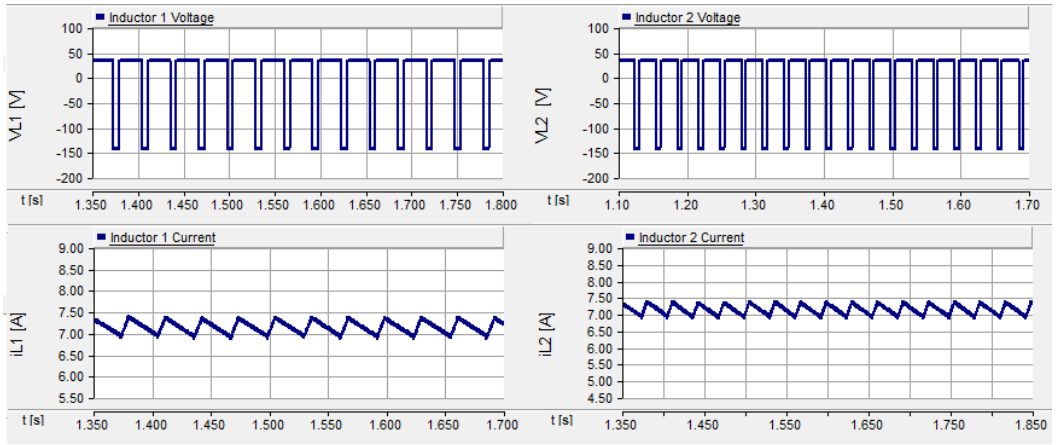


Figure 48

Capacitors Voltage and Current for 36Vdc input

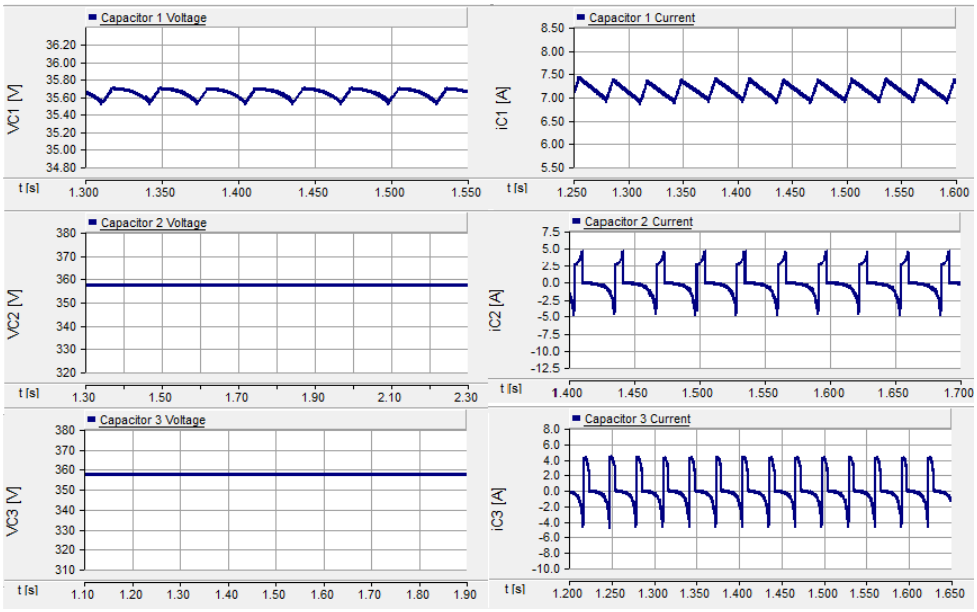


Figure 49

DC-DC Topology Output Voltage and Current for 36Vdc input

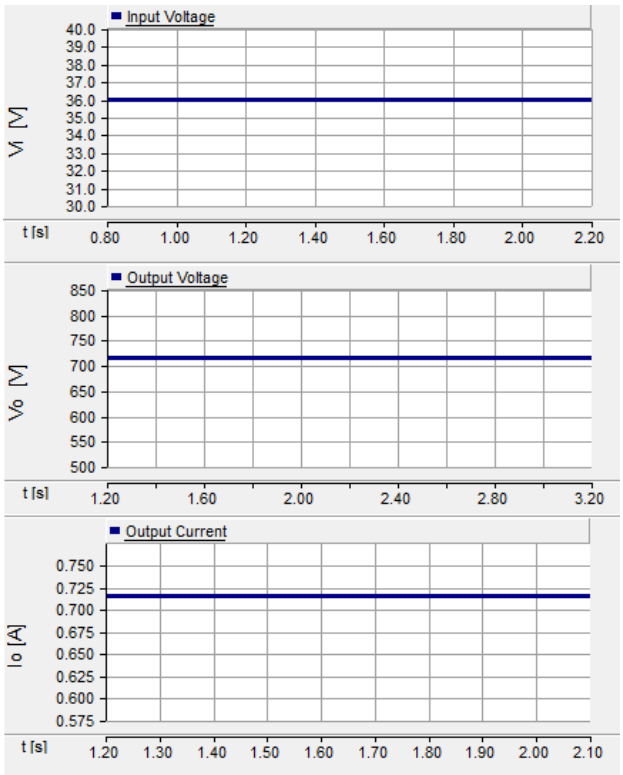


Figure 50

DC-AC Converter Gate Pulses

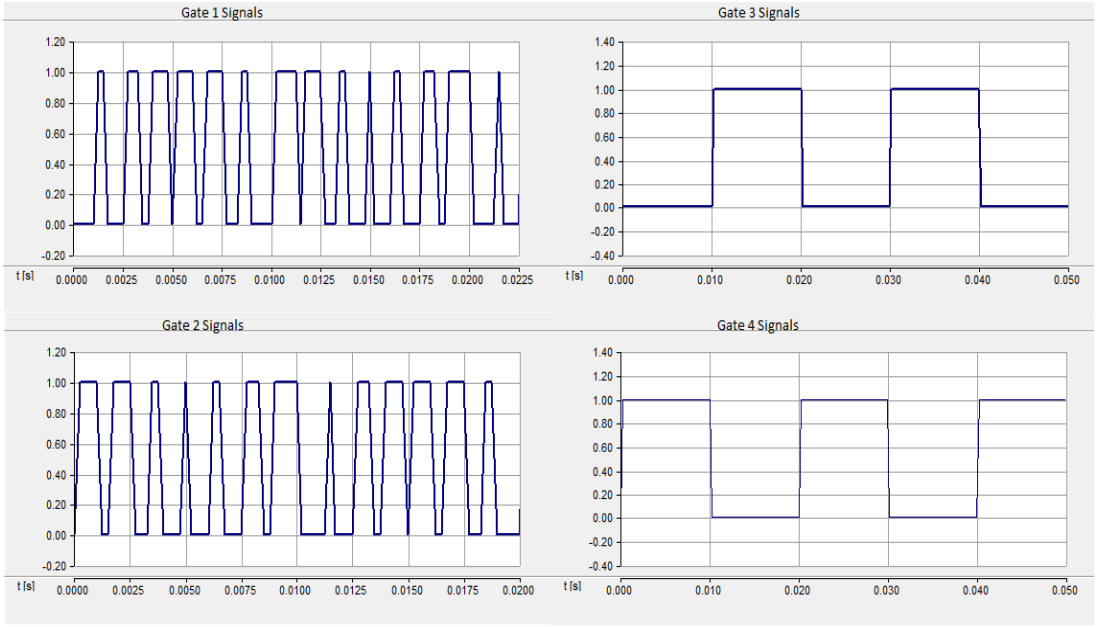


Figure 51

DC-AC Converter Carrier and Reference Signals

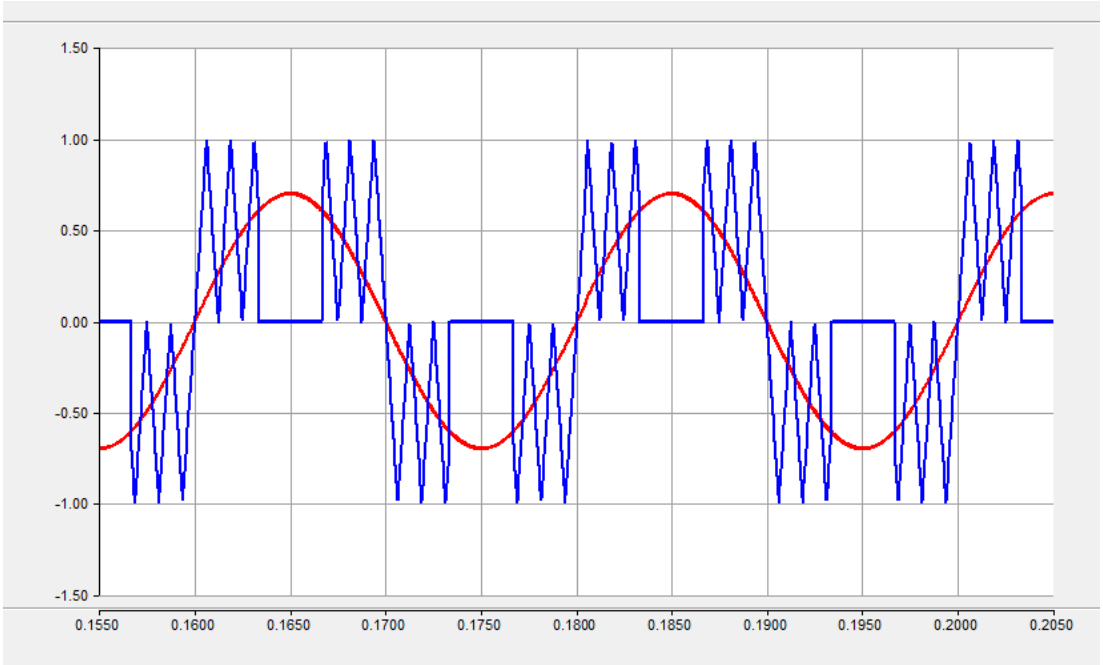


Figure 52

DC-AC Converter Output Current and Voltage Waveforms

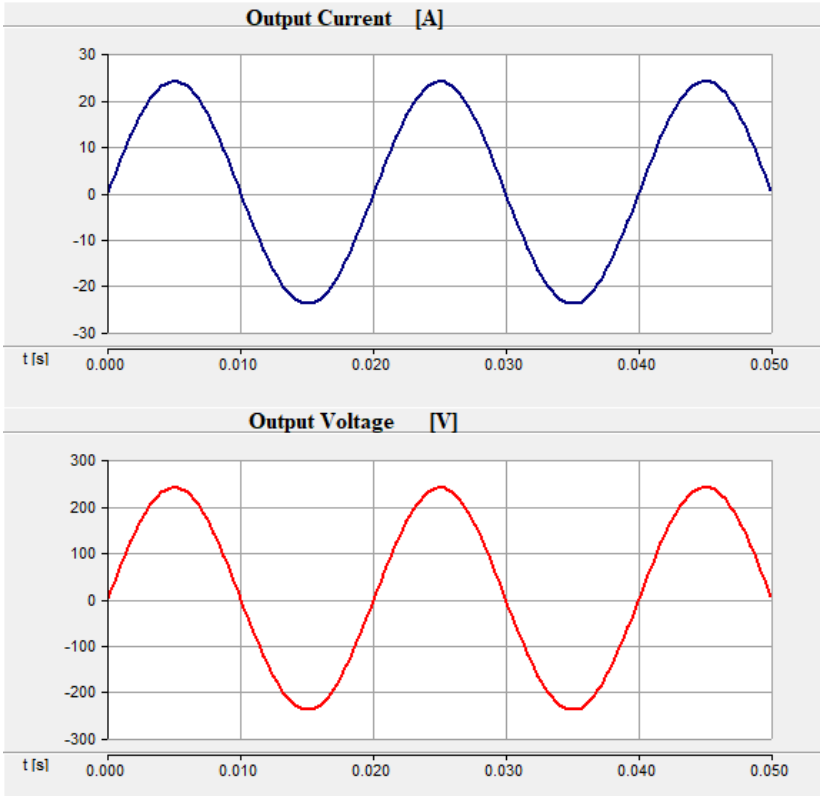
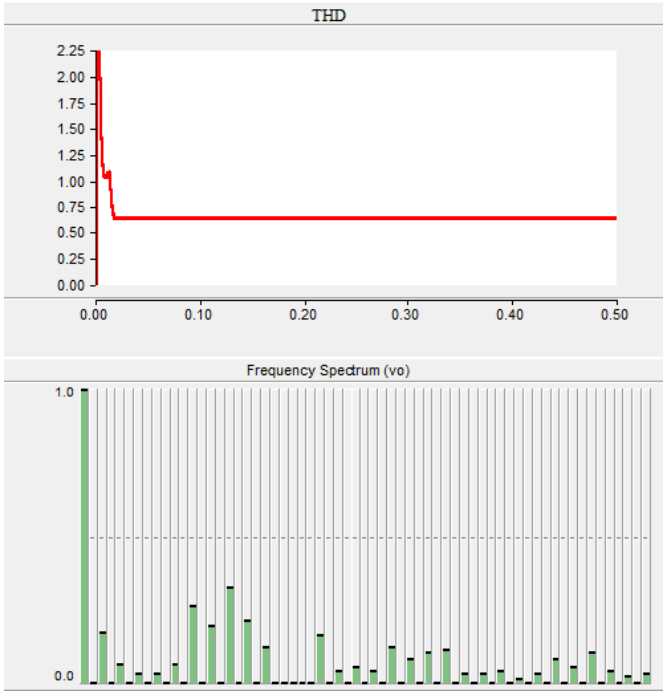


Figure 53

DC-AC Converter THD and Frequency Spectrums



The DC-DC converter side has excellent boost capabilities as shown in Table 4 below. Three simulations using different input voltages have validated the mathematical analysis which led to equation (3.26) because in all three cases the output voltage gain was approximately 20 at 80% duty cycle. In these results, the DC-DC converter also exhibits the ability to produce a variety of boosted output voltages from different input voltage values. Another point to note is that the output voltage gain generated is slightly lower because of the effect of unwanted electrical properties in the components e.g. the switch resistance. Both results shown in the Table 4 and Figure 39, Figure 43, Figure 47 validate the assumption made during mathematical analysis that the inductor voltages for inductor 1 and 2 are equal. Additionally, the analytical waveforms shown by Figure 39 confirm that the inductor voltages in charge and discharge mode are equal to equations (3.1) and (3.17) and the results in the Table 4.

Table 4

Simulations Results

DC-DC Converter						
Input Voltage, Vs	12V dc		24V dc		36V dc	
Output voltage, V_o	238.27V dc		476.54V dc		714.80V dc	
Output current, i_o	0.238A		0.476A		0.714A	
L_1 current, i_{L1}	2.31A	2.45A	4.58A	4.90A	6.88A	7.36A
L_2 current, i_{L2}	2.30A	2.46A	4.56A	4.88A	6.89A	7.36A
L_1 voltage, V_{L1}	-47.66V	11.92V	-95.35V	23.83V	-142.99V	35.77V
L_2 voltage, V_{L2}	-47.66V	11.92V	-95.31V	23.84V	-143.01V	35.75V
C_1 current, i_{c1}	2.33A	2.43A	4.67A	4.92A	6.90A	7.35A
C_2 current, i_{c2}	-1.55A	1.42A	-2.99	3.04A	-4.43A	4.54A
C_3 current, i_{c3}	-1.52A	1.50A	-2.96A	2.85A	-4.43A	4.28A
C_1 voltage, V_{c1}	11.81V	11.87V	23.68V	23.79V	35.54V	35.69V
C_2 voltage, V_{c2}	119.08V		238.17V		353.31V	
C_3 voltage, V_{c3}	119.16V		238.27V		357.42V	
Switch current, i_{sw}	0A	9.09A	0A	14.64A	0A	22.16A
Switch voltage, V_{sw}	119.04V	0.15V	238.32V	0.12V	357.56V	0.16V

Table 4 (Continued)

DC-AC Converter		
Carrier frequency, f_c	800Hz	
Peak harmonic factors (out of 63)	13^{th}	0.2563
	17^{th}	0.3188
Input voltage, V_{in}	240V dc	
Peak output voltage, V_o	239.27V ac	
Peak output current, i_o	23.17A ac	
Power	56.64W	
Power factor	0.95	
Frequency, f_o	50Hz	

Note. An arbitrary selection of simulation results for output voltage and current, passive elements voltages and currents, and switch currents and voltage for the DC-DC converter is presented, together with simulation results for the DC-AC converter side.

The results shown in Table 4 show that the capacitors C_2 and C_3 have the same current, and the current flowing in the switch leg is approximately equal to the sum of currents of the passive elements L_1, L_2, C_1, and C_2. The voltage across capacitors C_2 and C_3 is equal and it is double boosted because the values shown in Table 4 show that their respective capacitor voltages are half of the output voltage. Hence if they are half the output voltage which has quadruple gain of a conventional boost converter, that means the capacitors 2 and 3 have double boosted voltage.

The results shown in Table 4 about the voltage across the switch confirm the relationship shown by Figure 34 between the output and switch voltage. The switch voltage is approximately equal to half of the output voltage in all the three cases where input voltage is different. The results shown also prove the existence of unwanted electrical properties of the elements because there is a non-zero voltage value across the switch when it is closed, yet ideally the voltage should be zero. On the DC-AC

converter side, the inverter successfully converts the 240V dc to 240V ac peak voltage. And the output waveforms shown in Figure 52 are pure sinusoids through the use of a third order (LCL) low pass filter with a cut off frequency of 100Hz to eliminate the high frequency components shown in the frequency spectrum in Figure 53.

3.4 Application of the Proposed Topology

The simulation results presented in the previous section show that that power output of the proposed topology with respect to the given parameters is 56W. This power output is very low for real life application, hence this section demonstrates the suitability of the inverter using adjusted parameters. For instance, the load resistor at the DC-DC converter side is reduced from 1000Ω to 20Ω and the input voltage is increased to 24V while the other parameters are kept the same, in order to increase the power output.

In Chapter 1, it was mentioned that a grid fall-back system is suitable in a country like Zimbabwe. Therefore, considering that Zimbabwe uses 7.12 billion kWh of electric energy per year, giving an average of 479 kWh per capita per year (W.D., 2019), that means average energy consumption in day per given household is 1.312kWh. Table 5 below shows parameters for different components in a grid fall-back system.

Table 5

Data for the grid fall-back system for PV application

Battery	
Type	Deep cycle lead acid
Model	SAGM 12 205
Rated Voltage	12V
Rated Capacity	205Ah
Depth of Discharge	20-100%
Number of Batteries	2
Connection	Series

Table 5 (Continued)

DC-DC Converter	
Input Voltage	24V dc
Load Resistor	20 **Ω**
Output Voltage	351V dc
Output Current	17.5A
Power	6.142kW
DC-AC Converter	
Input Voltage	351V dc
Input Current	17.5A
Output Voltage (peak)	350V
Output Current (peak)	34A
Rated Power	5.868kW
Efficiency	95%
Power Factor	0.95
Frequency	50Hz
Load	
Energy Consumption per Capita	479kWh per year
	1.312kWh per day

Using two batteries connected in series, the battery energy capacity becomes 4.92kWh. Considering that the energy from the battery is fed through an inverter estimated to lose 5% of the power, the energy delivered to the load from the battery drops to 4.674kWh. For an average consumption of 1.312kWh per capita, the depth of discharge (DOD) for the battery bank in a day is approximately 28.1%, if evaluated using equation (3.34). At the given DOD the Solar SAGM batteries have more than 3000 cycles, which makes them last for more than 8 years in a Zimbabwean household where they are discharged once in a day during the period of load shedding.

$$\begin{cases} DOD = \dfrac{Energy\ Consumption\ per\ day\ [kWh]}{Battery\ Energy\ Capacity\ [kWh] \times Inverter\ Efficiency} \\ Battery\ Energy\ Capacitiy = \ Rated\ Voltage\ [V] \times \ Rated\ Capacity\ [Ah] \end{cases} \quad (3.34)$$

Figure 54 shows the simulation plots for the SLCN converter when an input of 24V from the batteries is fed to the SLCN converter, and 351V is generated at the output terminals. The output voltage is not 480V because non-isolated high gain DC-DC converters experience a decrease in voltage as the load power increases. In this case, the rated power of the inverter is 5.868kW.The inverter generates 350V, 34A as shown in Figure 55, and it has a low pass filtered 50Hz single phase modified sinusoidal waveform. The approximate voltage RMS value is 247V, and the power factor is 0.95 for the load considered in the PSCAD simulation, but in practice it will depend on the load connected at the terminals of the inverter.

Figure 54

Simulation Plots for the DC-DC Side

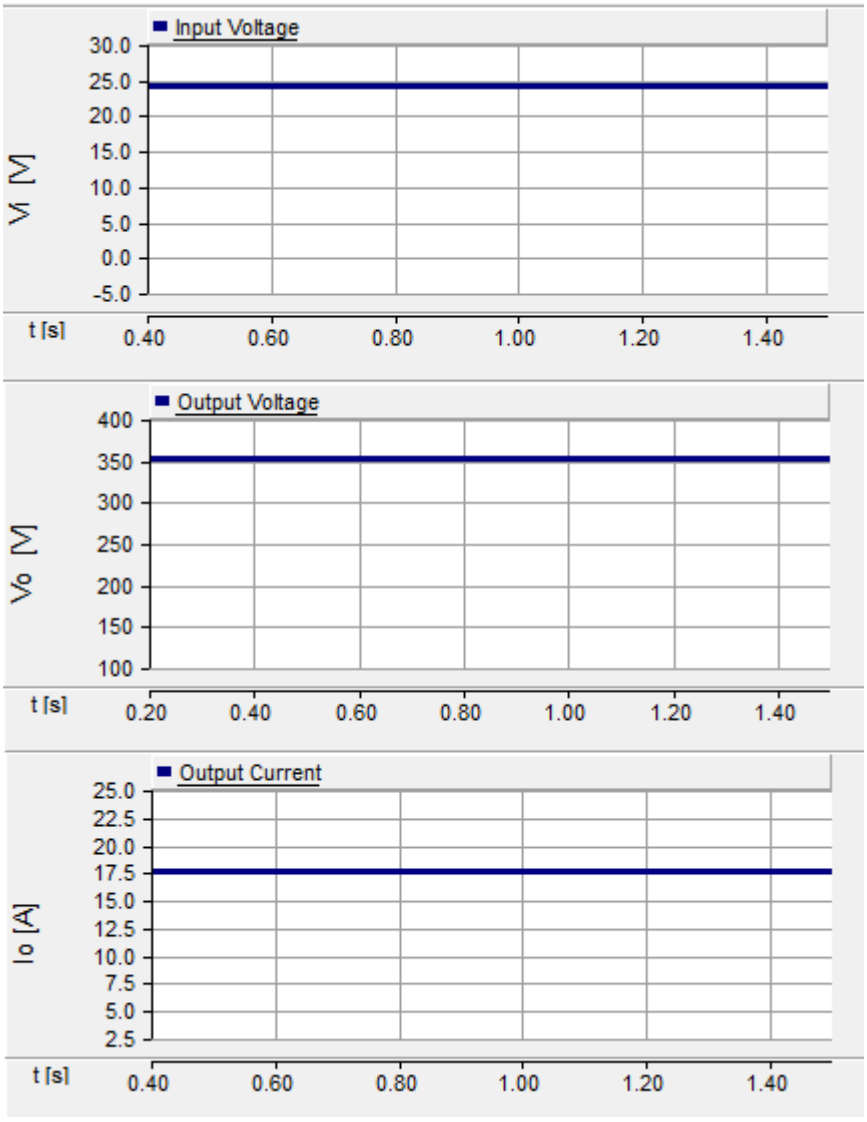
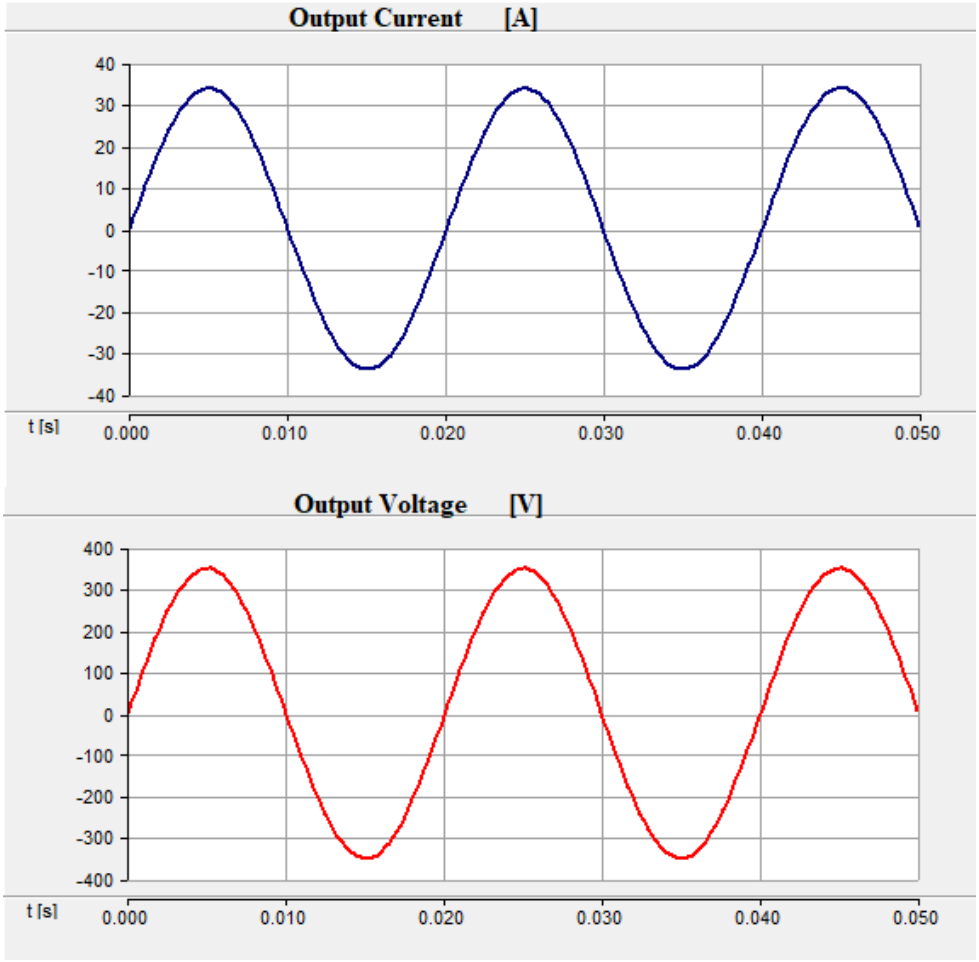


Figure 55

Simulation Plots for the DC-AC Side



3.5 Conclusion

This chapter describes the operation of the proposed topology. PSCAD simulations are done for the DC-DC and the DC-AC topology. Three different input voltages are considered on the DC-DC topology and the simulation results validated the boost ability of the SLCN converter topology. A 240V dc input voltage is fed into the DC-AC side and the simulation results validated the generation of an AC waveform at the output terminals of the inverter. Additionally, a case study for grid fall-back system is discussed using energy consumption data for a Zimbabwean household. Therefore, the PSCAD simulations carried out have validated the performance of the proposed topology and its suitability for PV application.

CHAPTER 4
Conclusion

4.1 Introduction

This chapter summarises the work done in this thesis by briefly reporting the results of the investigations made through literature review, mathematical analysis and simulations, and gives an example of application areas for the findings made. Finally, the chapter offers recommendations for future work that can be done to build on the findings made in this thesis.

4.2 Conclusion

This investigation was carried out to design a two stage DC-AC converter topology which is non-isolated, has high voltage gain, has reduced components, and a relatively easy control technique. A DC-DC topology and a DC-AC topology is combined to form one DC-AC converter topology. The DC-DC converter is based on SLCN, and the DC-AC converter is based on an H-bridge inverter. A literature review was done to investigate the DC-DC converters, their voltage gains, components count, operating modes in CCM, among other features. H-bridge inverters were also reviewed based on their classes, output waveforms, number of voltage levels, and PWM switching techniques.

The literature review shows that, a lot of DC-DC converters have been proposed and developed for high voltage step up applications, for implementation in solar PV systems. And it can be generally understood from the converters reviewed that high voltage gains are attainable in an increasing manner from the conventional boost converter, through Z-source based, SL based, SC based, and finally SLCN based. However, there are a set of drawbacks that are associated with these converters. Some of them are extreme duty cycle, high components count, high voltage stress, and complex control platforms as more high voltage gain cells are introduced in conventional converter types like boost, buck-boost, and Z-source DC-DC converters.

H-bridge inverters which generate a sine wave pose minimum danger on the lifespan of an appliance in contrast to those with square wave outputs. And H-bridge inverters with multi-level output voltage and controlled by MSPWM have reduced THD and higher efficiency, respectively. Therefore, a three level H-bridge controlled by modified sinusoidal PWM technique is used in this thesis for reduced component count and a simpler control technique.

The SLCN DC-DC converter has 12 components which consist of two inductors, four capacitors, five diodes, and one IGBT with an anti-parallel diode. A pulse generator with a duty cycle of 80% and switching frequency of 20 kHz is used to generate the gate signals of the semiconductor switch. The H-bridge inverter on the DC-AC side has four IGBTs with anti-parallel diodes, and modified sinusoidal PWM is used to control the four semiconductor switches.

Analysis of the DC-DC topology in CCM is carried out to derive the ratio between the output and input voltage in steady state. The mathematical analysis arrived to a voltage gain of 20 at 80% duty cycle, which is four times the gain of a traditional boost converter topology. Additionally, the voltage across the switch was half of the output voltage, and that counts as reduced voltage stress on the switch compared to converter topologies where switch voltage is equal to the output voltage.

Simulations in PSCAD v4.2 software were carried out to validate the findings made about the proposed topology. Three simulations were carried out and three input voltages were considered for the DC-DC converter, which are 12V dc, 24V dc, and 36V dc. Output voltages of 238V dc, 476V dc, and 714V dc were generated at the output terminals, with respect to the input voltages considered. These results show high boost capability of the converter and its ability to generate different output voltages for different input values. The simulation results confirmed that the DC-DC converter can generate high output voltages from low voltages like a battery voltage. Additionally, simulations were carried out on the inverter side with an input of 240V dc. The H-bridge inverter generated an output peak voltage of 239V AC at 50Hz which validated the use of the proposed topology in interfacing a low DC voltage source with an AC load.

More simulations were carried out after adjusting a few parameters to meet real life applications, and the results show that the proposed topology is suitable for use in a grid fall-back solar system. This is a system where a single battery or a system of batteries connected to generate the desired voltage is charged by a solar PV system. When the batteries are fully charged, they feed into an inverter topology. And the inverter output is connected to an AC load which can be a single appliance, a single circuit on the control panel, or a building, depending on the achieved voltage levels. The batteries will supply energy to a load until they have discharged a pre-set amount of energy. Then the AC load switches back to the grid and the batteries begin to charge

from the solar PV system again. This system is known as grid fall-back and the proposed topology can be used in such a system.

Since the DC-AC conversion is in two separate stages, the output terminal of the SLCN converter can be connected directly to a DC load. This is a feature which single stage inverters cannot offer because the DC-AC voltage conversion occurs in one circuit.

4.3 Recommendations

From what has been established theoretically and by simulation results, if a gain of 20 is achieved from 80% duty cycle, then there is smaller room for increased voltage gain without approaching extreme duty cycles. Therefore, to achieve higher voltage gains – also known as ultra-voltage gains - using the topology proposed in this thesis, the number of inductor cells can be increased to make it an N stage converter topology.

Other improvements that can be made to this thesis in future works are:

- Design of MISO DC-DC converter when two or more sources are available, and
- Design of a three phase two stage DC-AC converter, for solar PV applications connected to the grid transmission network.

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Appendices

Appendix A

Turnitin Similarity Report

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