ELIMINATION OF DOUBLE LINE FREQUENCY IN SINGLE-PHASE QUASI Z-SOURCE INVERTER BY CONTROLLING DC-LINK CURRENT

A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF APPLIED SCIENCES OF NEAR EAST UNIVERSITY

By
IGBINENIKARO OSAYI PHILIP

In Partial Fulfilment of the Requirements for the Degree of Master of Science in Electrical and Electronic Engineering

NICOSIA, 2020

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Approval of Director of Graduate School of Applied Sciences

Prof. Dr. Nadire CAVUS

We certify this thesis is satisfactory for the award of Masters of Science in Electrical and Electronic Engineering

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I am grateful to God almighty, for his grace that has kept me going throughout the period of study. Also, I am grateful to my supervisor Prof. Dr. Ebrahim Babaei and Prof. Dr. Fahreddin Sadikoglu, my thesis Co. supervisor for his numerous fruitful discussions and kind guidance throughout the period of my research. His comments and corrections have always helped me to improve my work in many ways. Moreover, I would like to thank my other colleagues and friends for their cooperation encouragement and assistance.

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To my parents…

ABSTRACT

Quasi-Z has increased a ton of consideration as of late because of its characteristic on second harmonic power stream in single phase network, it has different applications yet the one that is most captivating is it application on a grid-tie photovoltaic application. We use an enormous impedance source to reduce the direct current link flow as well as the 2^{nd} harmonic voltage part. The decrease when it comes to Quasi Z-source network has become a problem for research purpose. This thesis proposes a strategy for removing frequency in single-phase Qzsi that is double lined by controlling Dc-interface current by utilizing dc-side low-recurrence current wave damping control. During examination of intensity stream, a subsequent single-phase power model is inferred, and the wave control is broken down to reduce the qZS network. A present wave mode of regulation is proposed to guarantee concealment of second consonant power course through the inductors. PSCAD software was used for simulation of this thesis.

***Keywords*:** PSCAD; Qzs; Qzsi; single-phase system; double line-frequency ripple

ÖZET

Quasi-Z, tek fazlı şebekedeki ikinci harmonik güç akışı üzerindeki karakteristik özelliği nedeniyle geç bir ton düşünmeyi arttırmıştır, ancak farklı uygulamalara sahiptir, ancak en büyüleyici olanı, bir grid-kravat fotovoltaik uygulama üzerine uygulanmasıdır. Doğru akım bağlantı akışını ve 2. harmonik voltaj kısmını azaltmak için muazzam bir empedans kaynağı kullanıyoruz. Quasi Z-kaynak ağı söz konusu olduğunda azalma, araştırma amacıyla bir sorun haline gelmiştir. Bu tez, DC tarafı düşük tekrarlama akımı dalga sönümleme kontrolünü kullanarak Dc-arayüz akımını kontrol ederek çift hatlı tek fazlı Qzsi'de frekansı çıkarmak için bir strateji önermektedir. Yoğunluk akımının incelenmesi sırasında, müteakip bir tek fazlı güç modeli çıkarılır ve qZS ağını azaltmak için dalga kontrolü bozulur. İndüktörler aracılığıyla ikinci ünsüz güç yolunun gizlenmesini garanti etmek için mevcut bir dalga düzenleme modu önerilmektedir. Bu tezin simülasyonu için PSCAD yazılımı kullanılmıştır.

Anahtar Kelimeler: PSCAD; Qzs; Qzsi; tek fazlı sistem; çift hat frekans dalgalanması

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LIST OF ABBREVIATIONS

AC:	Alternating Current
BJT:	Bipolar Junction Transistor
C:	Capacitor value
CCM:	Continuous Conduction Mode
D:	Duty cycle
DC:	Direct Current
DCM:	Discontinuous Conduction Mode
E:	Energy stored in the inductor
IGBT:	Insulated Gate Bpolar Transistor
L:	Inductor value
LCD:	Liquid Crystal Display
MOSFET:	Metal–Oxide–Semiconductor Field-Effect Transistor
P:	Power Switching loss
PV:	Photo-Voltaic
S:	Switch
SMPS:	Switching-Mode Power Supply
T:	Total time period
t:	Time period
Co:	Output Capacitor
C1:	The First Capacitor value
C2:	The Second Capacitor value
Do:	Output Diode
D1:	Diode number One
ΔIL:	The variation Inductor current
ΔILoff:	The variation Inductor current during off-state
ΔILon:	The variation Inductor current during on-state
fs:	Switching Frequency
ICo:	Output Capacitor Current
ID:	Diode Current
IL:	Inductor Current

IL1p:	Parallel Currant during Inductor number One
IL2p:	Parallel Currant during Inductor number Two
ILmax:	Maximum inductor current
IS:	Switch Current
L1:	Inductor number One
L2:	Inductor number Two
R:	The value of Output Resistant
S1:	Switch number One
S2:	Switch number two
∂**:**	Constant
t0:	Time at the start point
t1:	Time at the point One
t2:	Time at the point One
LB:	The Inductor Time constant for Boundary Condition
T1:	Switch constant time
Vi:	Input Voltage
VO:	Output Voltage

CHAPTER 1
INTRODUCTION

Impedance source inverter topology has come to be famous to be used in SP grid-tie PV topologies, also in cascaded inverters and un-interrupted power applications. Due to the improvement of voltage and also the function of inverting an alternative current can be added into a power conversion state, the proposed can be made more precise while evaluating the chopper state and the inverter state wished in a traditional converter. Dealing with the SP- qZSI-based Cascaded multilevel inverter has a good direct current-hyperlink voltage even though the Photo voltaic ray changes over a huge distance, and it additionally minimizes the wide varieties of photo-voltaic modules to (Shuo et al., 2010). When dealing with SP converters, the line frequency (2ω) which is doubled, its strength flows via the direct current part. The angular frequency energy inside the direct current facet leads to 2ω voltage and modern-day distortion for both the traditional S-P H-bridge converter and the impedance source inverter modules. The angular frequency voltage ripple of the direct current-hyperlink bus has to be confined at a distance that's tolerant in engineering, in any other case the converter output voltage will have ripples. For the traditional H-bridge converter with most effective one capacitor at the dc part, a normal approach to lower 2ω voltage ripple is to buffer the 2ω power within the large dc-link capacitor. For the S-P qZSI, the dc facet consists of a network of inductors and capacitors in place of a single capacitor as within the traditional single-phase H-bridge inverter. Researchers found at that 2ω voltage and modern-day distortion network can represent the correlation among the distorted wave and parameters of the impedance. Solutions blanketed the complex terms gotten in and, in which no exploratory check was sent, and a computerized arrangement was the best way to plan the quasi z-source organized form for smothering its wave. Furthermore it can be desired to build up a more straightforward expository approach that mirrors the correlation of the 2ω swell and the structuring or limiting the impedance arrangement. introduced a logical approach that state that we can legitimately reveal the connection between the wave and impedance parameters, yet the circuit don't give adequate data to limit the qZS network parameters in light of the fact that there is no power circuit approach. Checking the investigative approaches in brought about

enormous determined qZS impedance values despite the fact that and utilized shut circuit regulator to decrease the direct current-interface 2ω voltage wave. (Peng, F.Z.2003).

1.1 Thesis Problem

Dealing with the thesis problem, the proposed work can be made progressively smaller in correlation with both phases which are chopper boost and inverters that are required in a traditional converter. Dealing with SP inverter framework, the frequency (2ω) which is double lined controlled moves across the direct current side, where ω is the key precise recurrence.

We would definitely see that the converter yield voltage will be rippled when the wave $V_{ac}$of direct current-interface voltage isn't adequately little. By and by, when the quasi z-source impedance is intended to restrain the voltage swell V_{ac} inside a building acceptable range, generally our dc-ac yield voltage will be deformed.

1.2 Aim of the Thesis

This thesis research is aimed at the method of eliminating double line frequency in single phase Quasi Z-source inverter by controlling Dc-link current by utilizing dc-side low-frequency current wave damping control. This would be done using investigation of intensity stream, a subsequent symphonious network is determined, moreover our wave control is dissected for reduction of the network. We use a present wave damping control that is proposed to guarantee concealment of 2^{nd} harmonic power flow through the inductors. We make use of PSCAD to check the simulation results, experimental result is also verified and hypothetical examination.

1.3 The Importance of the Thesis

The importance of this thesis research lies on the fact that qZSI SP topology, the direct current part comprises of a system of *L* and *C* as opposed to a solitary capacitor as in the customary SP H-B converter. The network is utilized to expand the efficiency of the voltage related to arranged shoot-through states during activity of the qZSI.

1.4 Limitations of the Study

Dealing with the limitations of this work. We are assigning same value for two inductors and also same value for two separate capacitors.

- Both capacitors will have diverse current effect in inductors L_1andL_2. Specifically, we would have a higher 2ω inductor current wave in any event for inductor L2 when $C_1$and$C_2$are not in equilibrium. Enormous 2ω inductor current wave will bring about huge genuine power misfortune and huge current deformation on $L_1$and L_2.
- Our recent structure expects to acquire steady inductor current without 2ω swell. Since C_1andC_2 are in arrangement for the equivalent 2ω current wave and the direct current-link capacitance has a most extreme incentive at C1=C2 which diminishes the 2ω wave of the dc-interface voltage. On the off chance that the capacitor C2 has littler capacitance, its 2ω voltage wave should be larger.
- We compare the circumstance occurrence if $L_1$and L_2 have various inductances. The demonstrating and regulating configuration should likewise be confounded if $C_1 \neq C_2$and $L_1 \neq L_2$.

1.5 Thesis Outline

This thesis has four chapters as follows.

Chapter I of this thesis introduces general background, outlines the challenges and drawbacks inherited by conventional H-bridge inverters, poor performances and proposed ways to minimize them.

Chapter II discusses the fundamental background, investigates the relevant theories, characteristics and comprehensive literatures review and recent achievements on various Quasi Z-source of different levels against the traditional inverters and their vast importance.

Chapter 3 introduces different components arrangement, theoretical analysis, on Quasi Z-source Inverters

Chapter 4 simulation of results using PSCAD software to prove the higher voltage gain performances of the inverter.

Chapter 5 focuses on conclusions and summary of the thesis. General recommendations and identifies the areas to advance the work in the future will also be presented.

1.6 Ethical Consideration

Considering the standard ethical feature and preparation of research procedures, the standard research procedures are implemented throughout the thesis. Moreover, the appropriate considerations and credit were given during the use of other people`s words or ideas by proper citing.

CHAPTER 2
RELATED RESEARCH

This chapter will review the circuit analysis and mode of operations; switching mechanisms and practical capabilities of the converter to produce output voltage with less voltage stress higher voltage gain and high efficiency throughout the operation by focusing on z-source converters.

In addition, the evaluation of the designed converters will discuss the basic forms and several modifications made on the converters; and possible solution to the disadvantages which these converters may face both now and in the future. This study will concentrate on z-source converter by putting maximum consideration on some of the previous topologies. Converter is an electronic circuit that can convert electrical quantities which can be phase, magnitude or frequency of current and voltage from low voltage level to higher level and from high level to low level with the help of switching circuit arrangement.

2.1.1 Conventional impedance source converter

This converter was first proposed by F.Z Peng in 2004. This thesis presents an impedance converter that gives solution to the conventional V-S converter and C-S inverter. The conventional Z-SC simply what it does is converting dc-ac without the use of a chopper and it also acts like a boost -buck due to its special kind of circuit topology.

For us to overcome the issues pertaining to voltage and current source inverter we come across this conventional impedance inverter and its regulating procedure to help us achieve any power conversion we want, be it from direct current to alternating current; from alternating current to direct current and so on. The figure below shows us a conventional ZSC. Our impedance network has a special impedance circuit that couples the converter original circuit to a load, direct current source or to an entirely different converter.

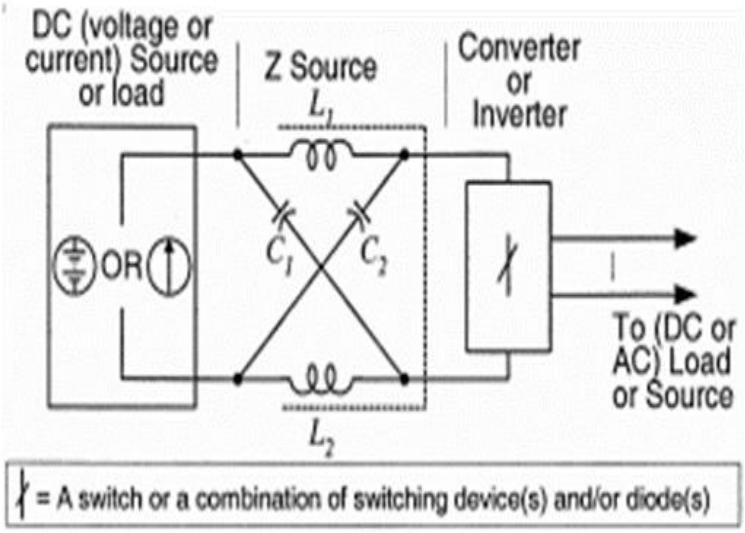

Figure 2.1: General structure of an Impedance-source converter

The diagram above shows us an inductor $l_1$andl_2 and c_1 and c_2 that are positioned in an X like manner that helps the Z-source converter to be coupled or a load or a direct current source. The z-source which is a direct current can either be a VS or a CS. Our source is either a battery, a diode, as the case may be or can be a hybrid or combination of both. We can also make use of anti- parallel switches for z-source converter. A split or separate inductor $l_1$and l_2 gives us the inductance of the circuit. Furthermore, power conversion of all kinds can be done using the conventional z-source converter (rectifiers, choppers, cyclo-converters and inverters).

2.1.2 Advantages of z-source converter over v and i source converter

- The capacitance and inductance used in z-source converters dc-link make it act as a constant large ZVS while the Voltage source converter which uses an inductor in the dc-link makes the source impedance high and makes it act as a stable CS, while the current source converter which uses a capacitor in its direct current-link makes it act as a small ZVS.
- The z source converter can have a load or source that is either a V or C. That means we can use a battery, a rectifier, an *L*, C or the combining the listed component and many more.

- The impedance source is used in step-down or step-up converters while current or voltage source converters are used in either boost or buck converter operation.
- Power loss is relatively low when using impedance source converters but in voltage source converters power loss is low due to filters while in current source converters power loss is also low.
- The impedance source converter can be used in different applications especially in PV cells because the input voltage can change highly. In regards to that the alternating current voltage at the load from zero to uncountable despite the value of the VS
- Impedance source converters have high efficiency due to reduced power loss unlike voltage and current converters.

2.1.3 Limitation of conventional z-source converter

In conventional impedance source converters, it has a lower average switching device when dealing with low boost ratio, that is why most times when we have low voltage, we use a boost ratio that's much higher. In impedance source converters sometimes there can be misfiring of switches.

2.1.4 Improvement in conventional z-source converter

Improving the conventional impedance source converter. We make use of a switch instead of a diode. This section would discuss about the bi-directional z-source inverter which replaces the conventional impedance source by eliminating the diode from its circuit and making use of switches. The operation of the diode is similar to the switch during inverter mode but in a rejuvenated way and also have a gate signal. Bi-directional impedance source inverter stores the exchanged alternating current and direct current power in either forward and reverse part. These bi-directional z-source inverters can avoid the undesirable operation mode when the impedance source inverter operates with low power factor and Inductance.

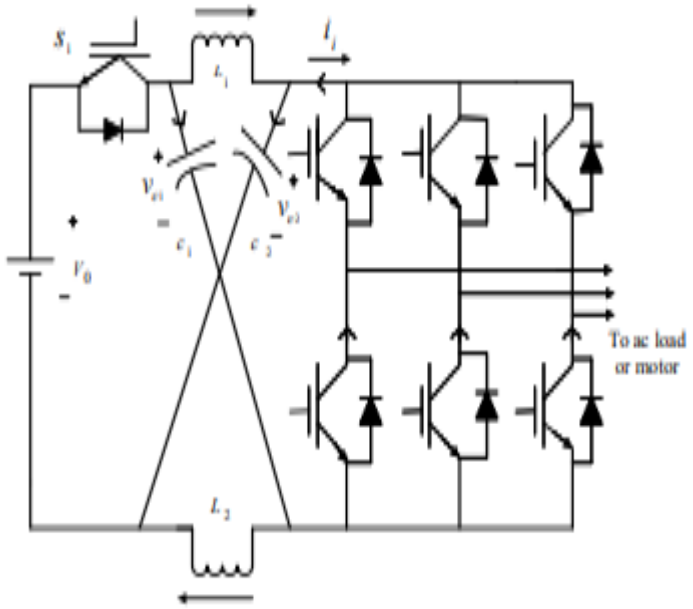

Figure 2.2: Bi-directional z-source inverter (Peng, F.Z.2003)

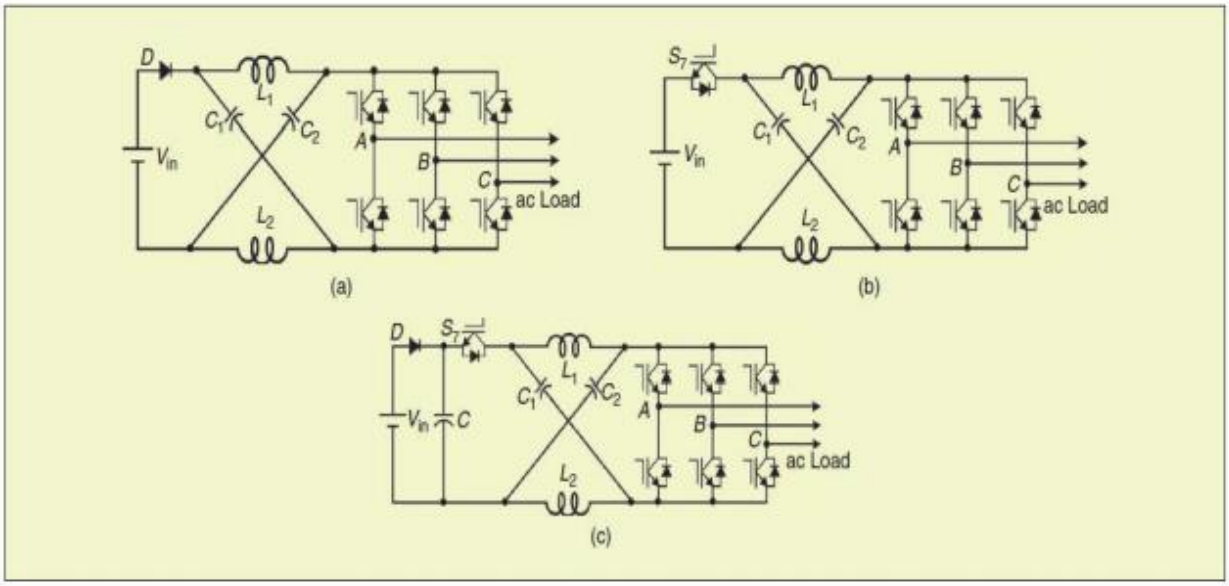

Figure 2.3: Impedance source inverter topologies a) ZSI b) Bidirectional ZSI (c) High performance ZSI (Peng, F. Z.; Ding. X.,2007)

2.2 Impedance-Source IMC (ISIMC)

The recent converter topologies that combined Z-source with indirect matrix converters are proposed in (Liu, Ge, Jiang, Abu-Rub, & Peng, 2014; Shuo et al., 2010). Figure 2.10 shows how the converter circuit are used for ac/ac conversion system. They are composed

of the following parts: A alternating current source, a Z-source or quasi Source network, rectifier circuit, an inverter and alternating current load. The incorporation of the impedance network makes it possible for the converters to work in boost as well as buck modes (buck-boost).

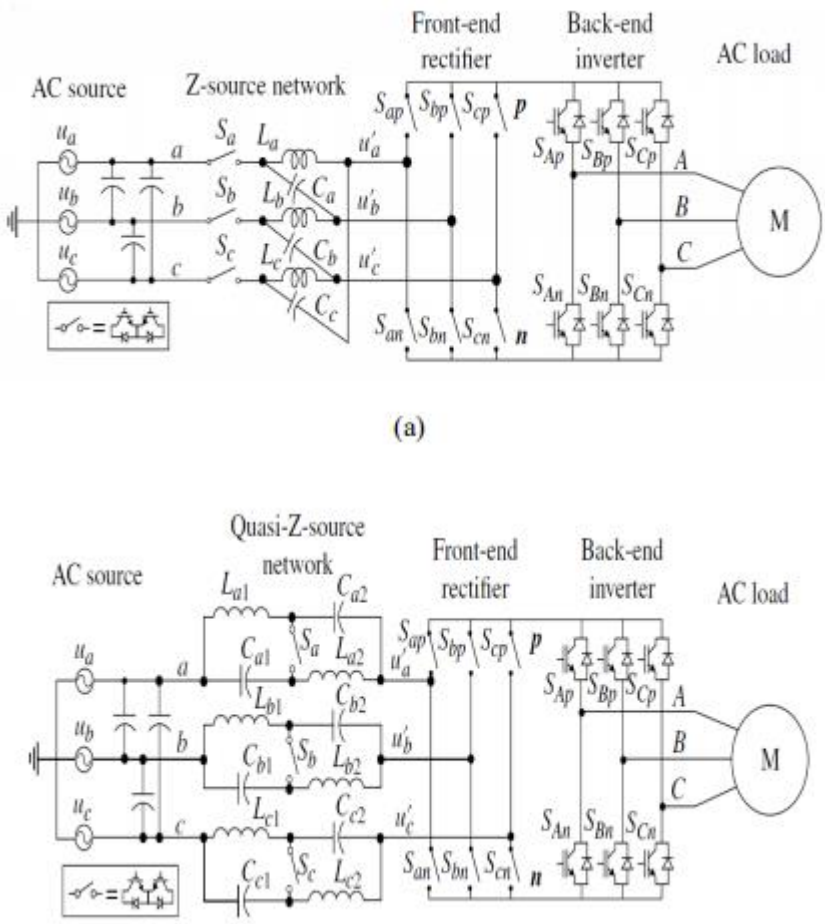

Figure 2.4: ZSIMC Topology(a) ZSIMC (Shuo et al., 2010) (b) qZSIMC (Liu et al.,2014)

2.3 Circuit Description of a CPT System

The CPT system that is proposed. Which includes an inverter with 4 diodes connected together, a coupling capacitance with two plate coupling materials, three order LC tank, Z-impedance network, a full bridge rectifier and also with a direct current output.

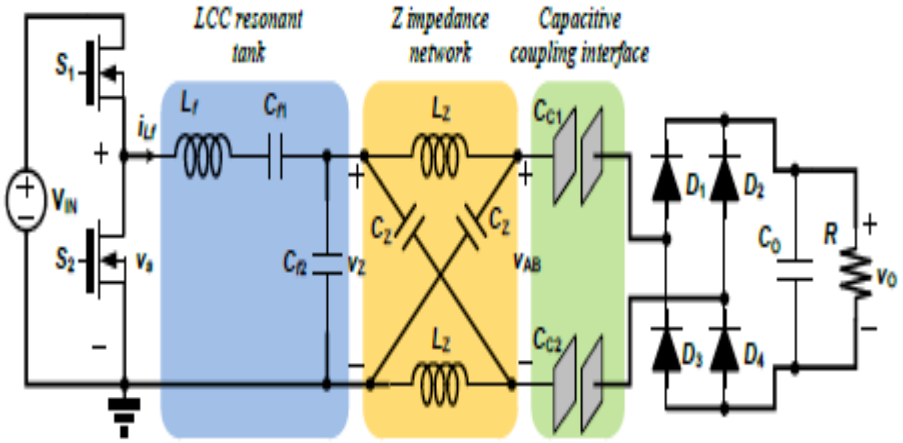

Figure 2.5: A proposed CPT system

2.3.1 LCC resonant network

The LCC resonant is composed of some component such as L_f, $C_{f1}, and\ C_{f2}$ followed by the Z-impedance network, which is connected in series to the half-bridge inverter. Note that both resonance filter tank may also be used. A series filter tank has no high step-up voltage capacity, but the inductor capacitor inductor filter, which has an extra *L* attached to it may have a high voltage boost but would raise the CPT network in size and in cost. Whereas the C_f capacitance which is connected in parallel with the Z-impedance will help in the voltage boost at the v_{in} and also help with the power transfer ability of the CPT system. The LCC tank component should be able to follow the following equation conductions

$$C_{f1} = C_{f2} \tag{2.10}$$

$$C_f = \frac{C_{f1}C_{f2}}{C_{f1}+C_{f2}} = \frac{C_{f2}}{2} \tag{2.11}$$

net

$$L_f = \frac{1}{\omega_s{}^2 C_f} = \frac{2}{\omega_s{}^2 C_{f2}} \tag{2.12}$$

2.3.2 Compensating the impedance network

We should note that these two inductors which are identical and the capacitors which are also two, make up the Z-impedance, it is called a Z-impedance because it forms a symmetrical Z shape structure. In the aforementioned the Z-impedance increase the voltage boost at the input voltage v_z and making up for the capacitive coupling interface. It does not have any effect when an open circuit fault or short circuit fault occur. It does not generate spike when the load and the secondary coupling is removed.

2.3.3. Designing of an impedance network

Z-impedance compensation is modeled with the wave approximated way, imagine this inverter is on a steady CCM, and the *LC* tank has a large fundamental frequency of the Ac starting voltage. The figure below shows an image of V that flows at C_{f2} capacitor with a sinusoidal AC source voltage V_z. The effective coupling capacitance, which is represented as $(C_c = C_{c1}C_{c2}/C_{c1} + C_{c2})$, the effective AC resistance, which is given by the rectifier and the output would be equivalent to $9/\pi 2$, as the filtering capacitor is used after the rectifier.

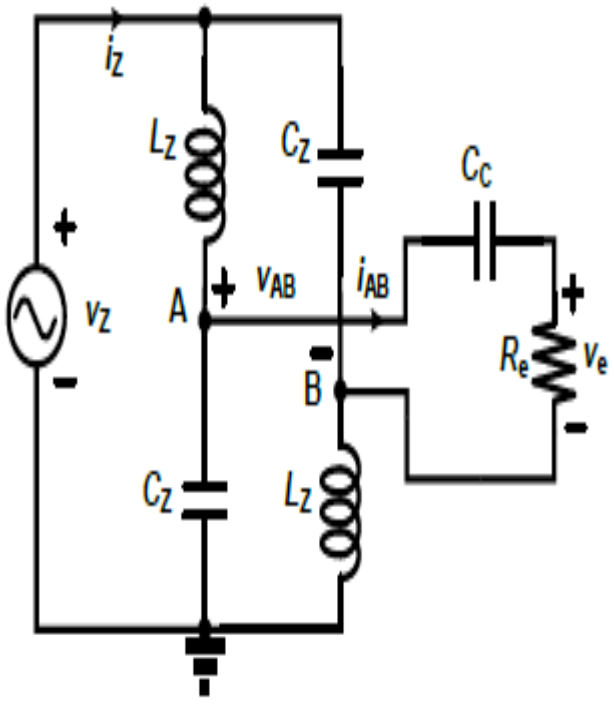

Figure. 2.6: A simple CPT circuit diagram showing Z impedance network

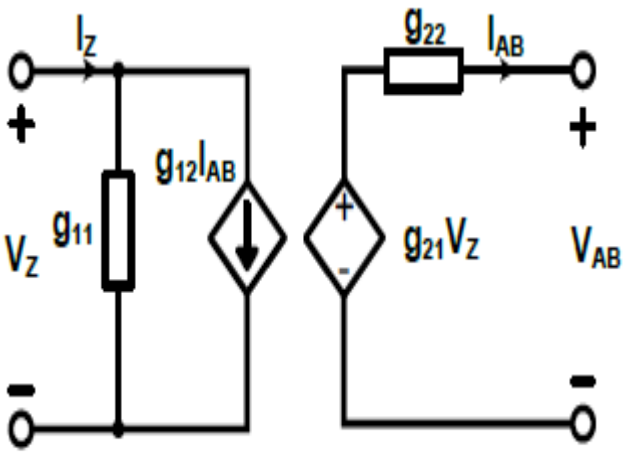

Figure. **2.7:** The Z impedance network showing g-parameters

2.4 Impedance Source Application in Grid connected PV System

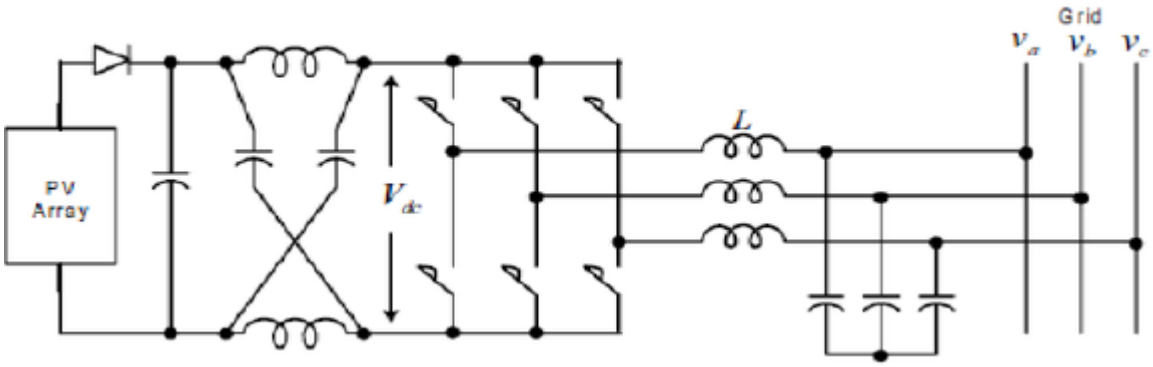

Figure 2.8: Three phase grid connected system

$$L\,{di_a}/{dt} = -v_a + V_{an} \quad (2.1)$$

$$L\,{di_b}/{dt} = -v_b + V_{bn} \quad (2.2)$$

$$L\,{di_c}/{dt} = -v_c + V_{bn} \quad (2.3)$$

Where v_a,v_b,v_c are 3 phase voltages of the grid

$$v_a = V \cos wt \quad (2.4)$$

$$v_b = V \cos (wt - \frac{2}{3}\pi) \quad (2.5)$$

$$v_c = V \cos (wt - \frac{4}{3}\pi) \quad (2.6)$$

While V_{an} ,V_{bn},$V_{cn}$are the inverter phase voltages, which is gotten from the inverter switching state. The source inverter has a total of 8 states, in which 6 of them are active while two are inactive. For each of the 8 states the equivalent 3 phases are S_{an}, S_{bn}, S_{cn} can be found.

$$V_{an} = \frac{1}{3}(2S_{an} - S_{bn} - S_{cn}).V_{dc} \quad (2.7)$$

$$V_{bn} = \frac{1}{3}(2S_{bn} - S_{an} - S_{cn}).V_{dc} \quad (2.8)$$

$$V_{cn} = \frac{1}{3}(2S_{cn} - S_{an} - S_{bn}).V_{dc} \quad (2.9)$$

The impedance source converter has three main control operations which are step up, higher step up and higher constant step up. In the figure below the procedure we would use to regulate the impedance input system would be the higher boost.

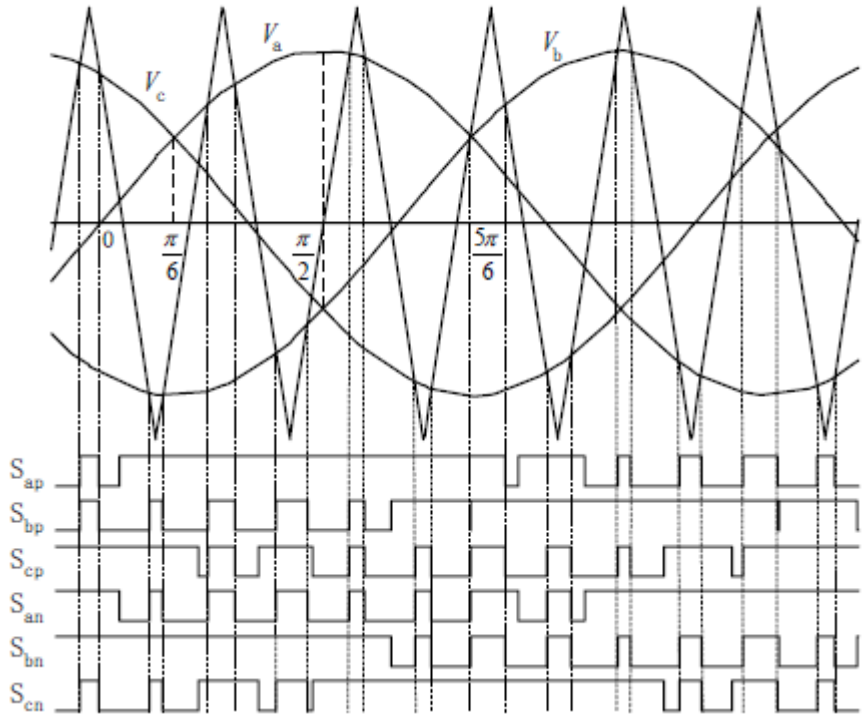

Figure 2.9: Maximum boost control

If the input voltage of ZSI is enormous, no step-up is needed so it behaves like a conventional converter.

2.5 ZS Resonance Inverter with Wireless Power Transfer Application

The WPT which is also known as wireless power transfer, it is a technology which is recently use in in Electric vehicle (EV) battery bank, it is highly preferred now because of it reliability, and also because it uses no cable which make it environmental friendly. It make use of on-line inductive power transfer which is also known as (OLPT), the charging facilities are kept underground and the coil that receives the signal that is kept under the electric vehicle receive the power to charge its battery without any wire connection, even while the car is in motion.

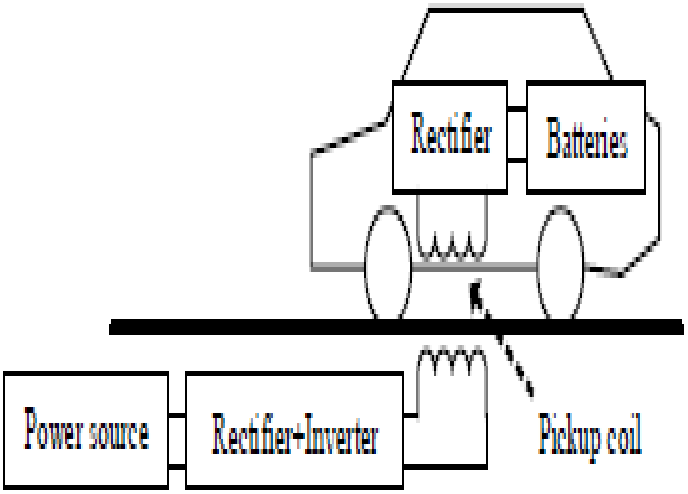

Figure. 2.10: WPT system for online power transfer

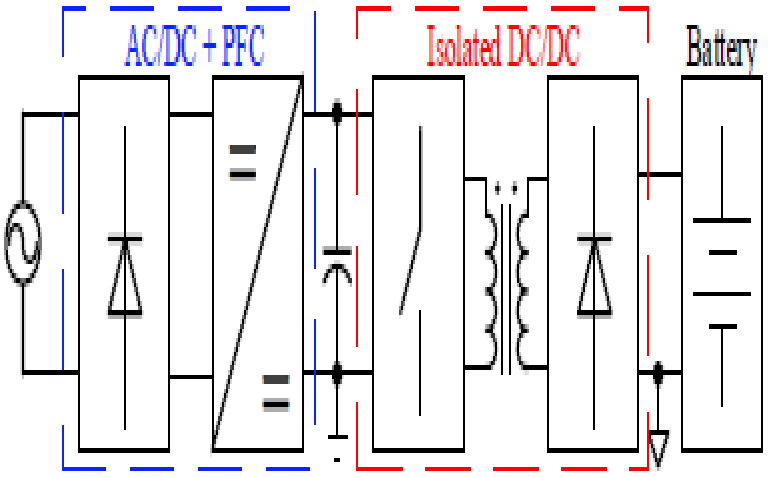

Figure. 2.11: An OBC Block Diagram

The single stage OBC inverter have be research for an online power transfer (OLPT) applications. Our pf was adjusted when checking the load of the system at the same time. Most of the single-phase single stage configurations, most of them have 1 *MOSFET or IGBT*, therefore having minimized amount. This system is derived from a fly back, so it has large problem on the semi-conductor *MOSFET or IGBT*, which lead to high voltage consumption and also high conduction loss.

There are many topologies of a single-phase single stage inverter with PFC which has be investigated but the PFC inverter is use here.

2.5.1 A typical on-board battery charger

This battery has 2 parts as shown on the diagram below, the front-end stage which is commonly use in PFC inverter, in a modern EV battery charger, it is a boost inverter. These typical step-up inverter- on board charger is shown in the figure below, where the second stage which is also DC/DC stage, consist of an SRC, which is also known as series resonance converter or inverter, which is highly used in wireless power transfer application.

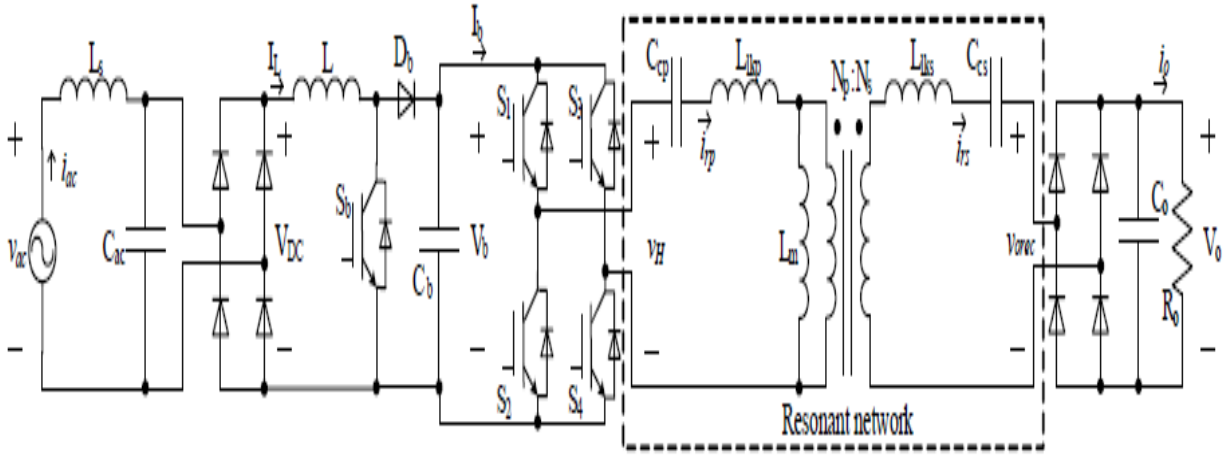

Figure 2.12: Step-up on-board battery charger

According to the typical step-up inverter gives high power factor, high power density and minimum rate. Also, the ripple current is also very high. As the energy maximizes the efficiency and the ability to handle heat dissipation also increase, the conventional boost converter is good for small and average power range of about 3.5KW. and also its witches operate under high switching conditions thereby increase the switching loss and thereby also increase conduction losses, these reduces switching frequencies.

2.5.2 An on-board battery charger

In this research, the proposed-on board battery converter uses the Z-sources network (ZSN) inverter for PFC applications. Since this topology was introduced in, its uses have increased, especially in regulating voltages. In OBC application, the ZSN can be seen in the PFC section, accompanied by the DC/DC inverter, it is assume in this as series resonant converter. The OBC can be called Z-source resonant converter (ZSRC). the ZSn which is located in ZSRC, add an excellent characteristic of PFC even without any addiction of switches as a normal PFC converter do. It gives high resistance to the on-board converter. This variable is also necessary because it provide a boost feature to the system, which is highly use for voltage regulation. The output voltage can be regulate by using the active duty cycle, which is used in the SCRs. Both the control variable are in the SCR H-bridge inverter, the ZSRC don't need any extra circuit to perform the power factor conversion. Note, because of ZSN, the ZSRC can perform both the PFC and the DC-DC conversion in one stage.

2.5.3 Applications of zsi in renewable energy systems

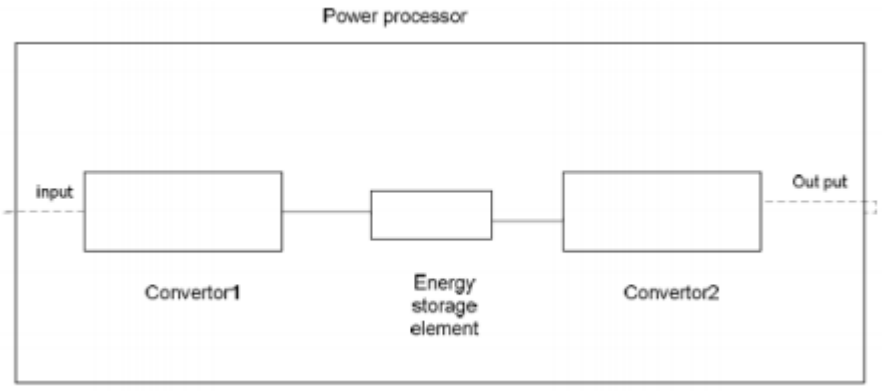

Figure 2.13: Block diagram of a power processor

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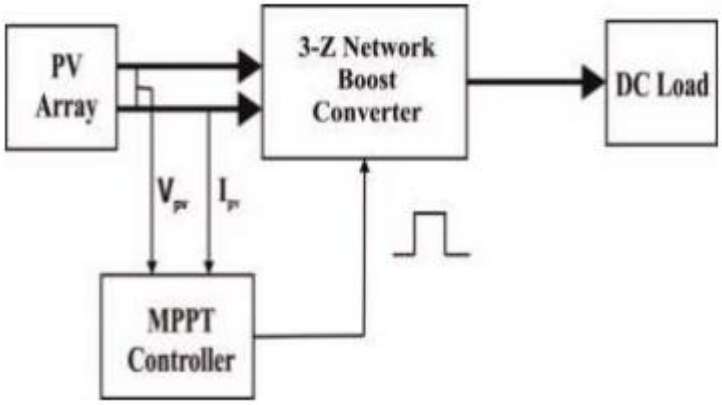

Figure 2.14: A proposed 3-Z Network boost system (kayatri et ai.,2016)

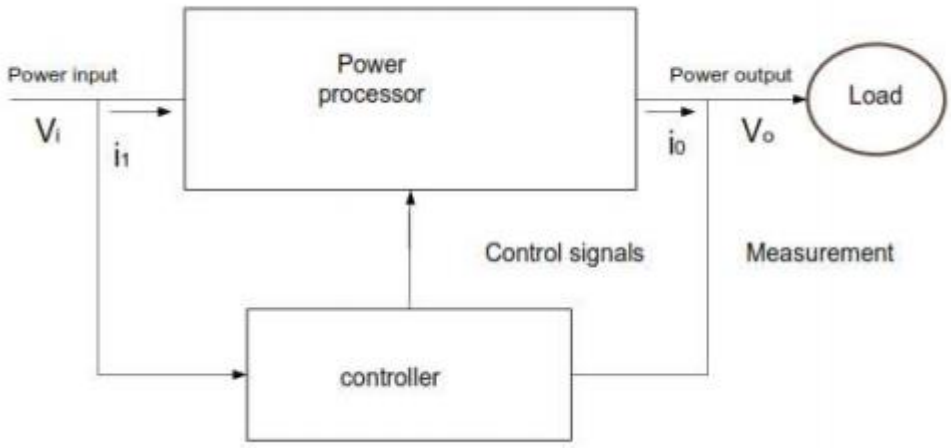

Figure 2.15: A power electronic system (Ja'far 2012)

2.6 Wireless Power Transfer Based on Electric Field to Compensate Z-impedance

There are two interface that are involve in the coupling effect, which is made of two plate which conduct electricity, these plates are either of aluminum or copper in the form of a pad, the material are therefore coated with a non-conducting or a dielectric material, which help for insulation. Note, the applications are determined by the shape and size of this plate in form of a pad.

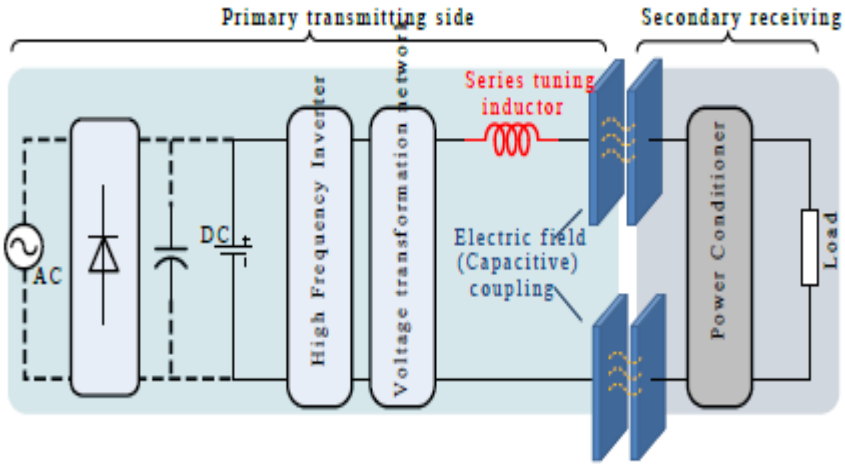

Figure 2.16: A simple CPT system

2.7 MPPT for G-T PV Applications Using ZSI

Now a day, PV system is mostly used in generation of power and in power electronics and high voltage system due to its low environmental impact and also because of its high availability of the solar radiation., The photo voltaic generation depends on the l condition and the temperature, like sun radiation level and the temperature. To be able to remove the high strength that is needed in the ambient temperature, MPPT in Photo Voltaic is important. The efficiency of the PV system can be reduction if the Photo voltaic module is not operating in the maximum power point (MPP) at every time, irrespective of its states.

In a typical PV grid system, it has two power conversion stages. The other is the downstream stage which is DC-AC conversion stage, which is from the energy buffer to the grid. A typical 2 state grid tie PV system is described below. The idea for two stages is necessary because of its inherent limitation of the DC-AC inverters for the boosting and stepping down the voltages easily. Ordinarily, the inverter that is known as VSI only step-down voltage while the inverter classified as CSI, only boost current.

It is worth knowing that the MPP voltage of a PV module can either be higher or lower than that of the grid voltage because of its environmental conditions, which make its important to have a power conversion system that can step up and step down the voltage easily to track the MPP properly.

Lately, a recent type of inverter, which is impedance –source converter was researched. That answers the limitations of VSIs and CSIs [11-13]. DC/AC inverters that the design is based on the idea of ZSC, which is denoted as Z-source inverter (ZSI), which can boost

and buck the voltage easily, which is very good for the design of a single stage PV harvesting systems.

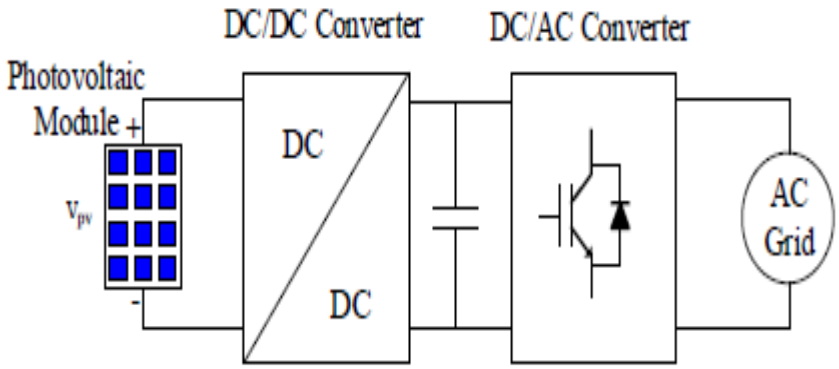

Figure: 2.17: 2 state GT- PV system arrangement

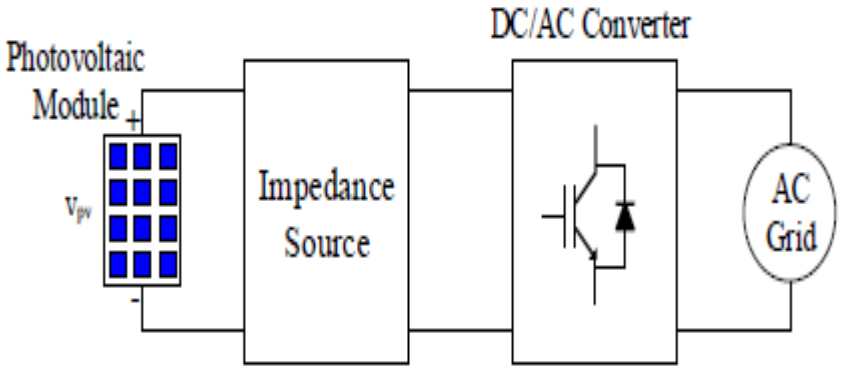

Figure 2.18: SPZ source GT-PV arrangement

2.7.1 Impedance-source converters

The impedance source converter has been used in power converter applications to create a convenient way of converting all loads. A ZSI, which is use in the PV harvesting module. The advantage of impedance source inverter is its ability to move through all kinds of states for increasing the load. When in the shoot through stage, both the switches in its one leg of the inverter are turn ON together. Controlling the ZSI it requires high level technique which is still under investigation. But in this research, the simple boost is used

for analyzing the switching signals. This strategy operate like that of the traditional based pulse width modulation, where its gained voltage is :

$$G = MB = \frac{V_{ac}}{V_o/_2} = \frac{M}{2M-1} \quad (2.13)$$

M denote the modular rating, while B represent the step-up consideration factor, it is also the amplitude of the inverter output voltage, V_{ac} and V_o. Represent the direct current-LV. The boosting factor is represented as

$$B = \frac{1}{1-2D} \quad (2.14)$$

D denote the duty ratio of the shoot-through

2.7.2 Mppt techniques

MPPT is very valuable in PV module because of it little wave at maximum power point, good and getting the maximum power point, fast convergence are the relevance of a maximum power point tracker process, several method or algorithm of MPPT technique are developed in different literatures, but the one that is used in this research.

2.7.3 Pec for mpc

As we know MPC has recently emerge as a leading strategy for power converter electronic system due to its fast-dynamic response and also high stability margin, which make it well suitable for Maximum point power tracker of Photo voltaic systems functioning in some states. it uses a particular system to evaluate the anticipated value of the system state, it also uses this technique to reduce the cost function.

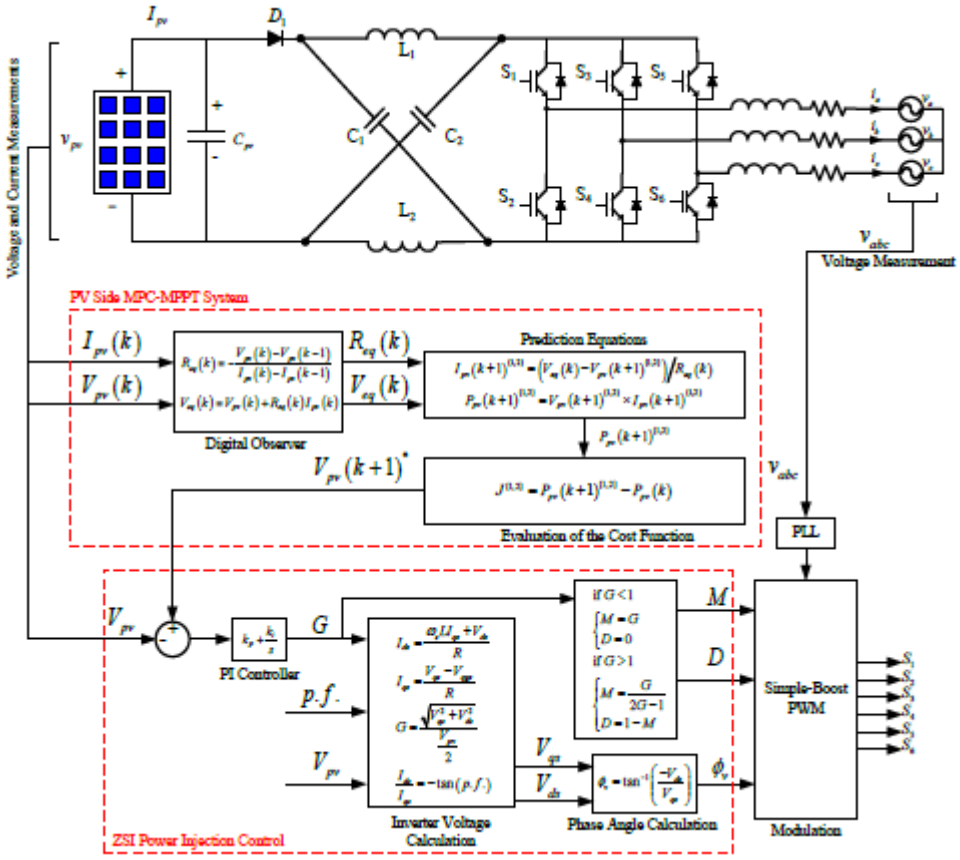

Figure: 2.19: The GTZSI and its regulated system

2.8 Z-source Matrix Converters

Combining the traditional matrix converters with a Z-network produces a Z-source based matrix converters. Since we have two structures of matrix converters; direct (CMC) and indirect (IMC), two Z-source based matrix converter topologies are produced. Z-source based IMC (ZIMC) and Z-source based CMC (ZCMC). Hence, the problem of voltage gain limitation in classical MC can be solved using this arrangement.

CHAPTER 3
THEORETICAL FRAMEWORK

This thesis builds up a concise frequency model which is double lined. The thesis is arranged in this format:

The 2ω model is inferred in the second part;

The control stream analysis of 2ω and the limited qZS C_a and L for SP-ZSI are focused upon in third part;

Fourth section has to do with the control of the ripple/wave damping;

Section five (5) has to do with the assessment of the impedance design;

In chapter 4 is where we go into details about our simulation which was done with the help of PSCAD and experimental studies.

3.1 Modeling a SP QZSI

3.1.1 2ω power amplification and ss model of sp-qzsi

Figure 3.1: shows a conventional SP QZSI.

Direct current link envelop

$$v_{PN} = V_{PN} + v_{ac}(t) \tag{3.1}$$

$$v_a = M[V_{PN} + v_{ac}(t)] \sin \omega t = MV_{PN} \sin \omega t + Mv_{ac}(t) \sin \omega t \tag{3.2}$$

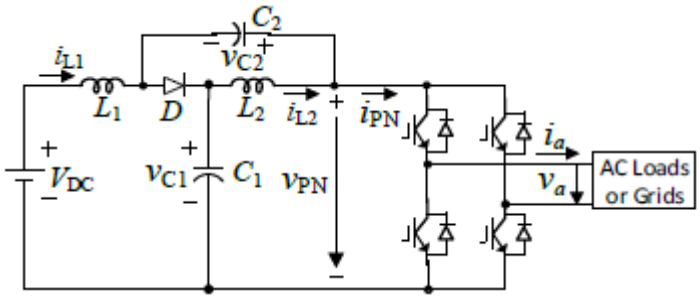

Figure 3.1: Schematic diagram of the proposed topology of S-P QZSI showing the direction of V and I

According to the diagram above, the inverter output will be disturb with symphonic v_{ac} of the direct current link voltage isn't adequately little .Practically speaking, The QZSI is intended to confine the voltage or swell v_{ac} around a design range, the output of the inverter can be shown as

$$v_a = MV_{PN} \sin \omega t \tag{3.3}$$

Using $MV_{PN} = \sqrt{2}V_0$, the output voltage becomes

$$v_a = \sqrt{2}V_0 \sin \omega t \tag{3.4}$$

From this we equate the ac output current for linear load to be

$$i_a = \sqrt{2}I_0 \sin(\omega t - \emptyset) \tag{3.5}$$

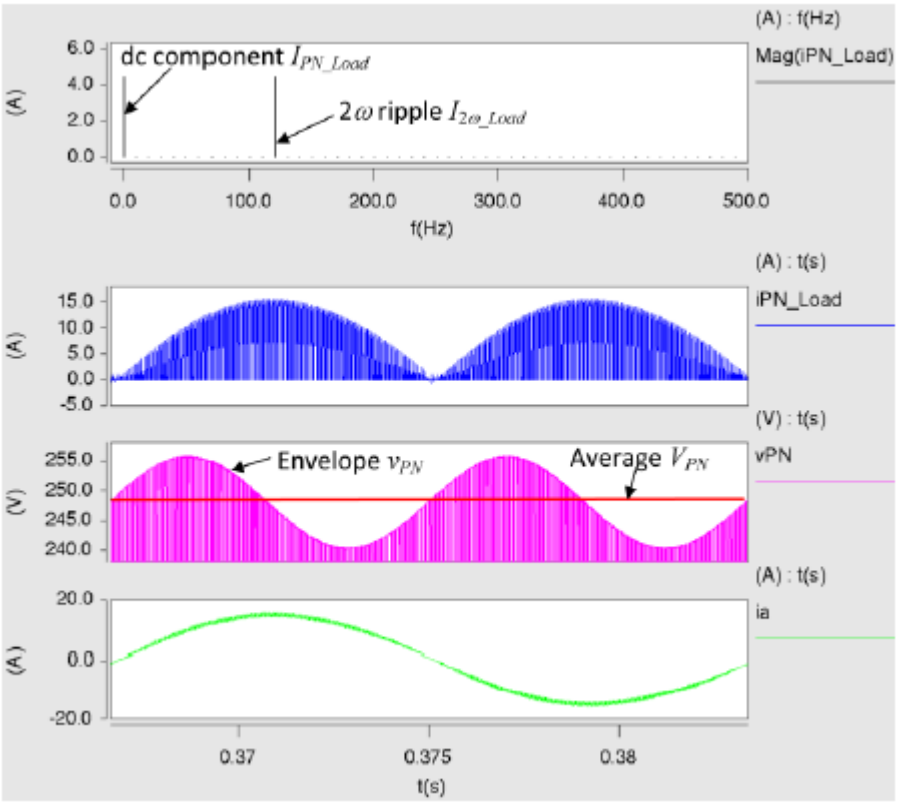

Figure. 3.2: Illustrating the double line frequency of the direct current link

Φ, which is the phase angle between V and I is given as, and the rms current of the load is given by I_0 .
We deduce the output power to yield

$$P_0 = V_0 I_0 \cos \emptyset - V_0 I_0 \cos(2\omega t - \emptyset) \quad (3.6)$$

$$v_{ac} = 0.5 \varepsilon V_{PN} \cos(2\omega t - \delta) \quad (3.7)$$

$$I_{PN} = \frac{1}{1-D} I_{PN\_Load}, \quad I_{2\omega} = \frac{1}{1-D} I_{2\omega\_Load} \quad (3.8)$$

D is noted as the S-T duty cycle defined as $D = T_{sh}/T_s$. T_{sh} is denoted as the S-T time interval; T_s is denoted as switching cycle.
concisely, the average current would be

$$i_{PN} = I_{PN} + i_{ac}(t) \quad (3.9)$$

Where $i_{ac}(t)$ is the second harmonic current ripple- that control other frequencies is illustrated as

$$i_{ac}(t) = I_{2\omega} \cos(2\omega t - \alpha) \quad (3.10)$$

During the shoot- through state, we analyze figure 3.3a to give us

$$L_1 \frac{di_{L1}}{dt} = V_{DC} + v_{c2} - (r_{L1} + r_{c2}) i_{L1} \qquad C_1 \frac{dv_{c1}}{dt} = -i_{L2}$$
$$L_2 \frac{di_{L2}}{dt} = v_{c1} - (r_{L2} + r_{c1}) i_{L2} \qquad C_2 \frac{dv_{c2}}{dt} = -i_{L1} \quad (3.11)$$

The direct current link V, produce zero, and there is no power transfer to the load.

$$P_{dc,1} = 0 \quad (3.12)$$

In non-shoot-through state, figure 3.3b shows that the power generated from the DC side to the AC side is given as

$$P_{dc,2} = v_{PN} i_{PN} \tag{3.13}$$

Therefore, the following equations are attained:

$$L_2 \frac{di_{L1}}{dt} = V_{DC} - v_{C1} - (r_{L1} + r_{C1}) i_{L1} + r_{C1} i_{PN} \qquad C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{PN}$$

$$L_2 \frac{di_{L2}}{dt} = -v_{C2} - (r_{L2} - r_{C2}) i_{L2} + r_{C2} i_{PN} \qquad C_2 \frac{dv_{c2}}{dt} = i_{L2} - i_{PN} \tag{3.14}$$

After getting $L1$ and $L2$ it yields

$$L_1 \frac{di_{L1}}{dt} = (1 - D)(V_{DC} - v_{C1}) + D(V_{DC} + v_{C2}) - [D(r_{L1} + r_{C2}) + (1 - D)(r_{L1} + r_{C1})] i_{L1} + (1 - D) r_{C1} i_{PN} \tag{3.15}$$

$$L_2 \frac{di_{L2}}{dt} = -v_{C2}(1 - D) + D v_{C1} - [D(r_{L2} + r_{C1}) + (1 - D)(r_{L2} + r_{C2})] i_{L2} + (1 - D) r_{C2} i_{PN}$$

$$C_1 \frac{dv_{C1}}{dt} = (i_{L1} - i_{PN})(1 - D) - D i_{L2}$$

$$C_1 \frac{dv_{C2}}{dt} = (i_{L2} - i_{PN})(1 - D) - D i_{L1}$$

Average power given to the load over each switching period is

$$P_{in} = (1 - D).P_{dc,2} + D.P_{dc,1}$$

$$= (1 - D) v_{PN} i_{PN} + D \times 0$$

$$= (1 - D)[V_{PN} I_{PN} + V_{PN} i_{ac}(t) + I_{PN} v_{ac}(t) + v_{ac}(t) i_{ac}(t)] \tag{3.16}$$

Finding this, $|v_{ac}(t)\, i_{ac}(t)|$, makes it lower than the other terms. Ignoring the product $v_{ac}(t)\, i_{ac}(t)$ in (3.16) deduces the input power to

$$P_{in} = (1 - D)[V_{PN}I_{PN} + V_{PN}i_{ac}(t) + I_{PN}v_{ac}(t)] \quad (3.17)$$

Because $P_0 = P_{in,}$ equating (6) and (17) gives

$$V_{PN}I_{PN}(1 - D) = V_0 I_0 \cos\emptyset \quad (3.18)$$

$$(1 - D)[V_{PN}i_{ac}(t) + I_{PN}v_{ac}(t)] = -V_0\, I_0 \cos(2\omega t - \emptyset)$$

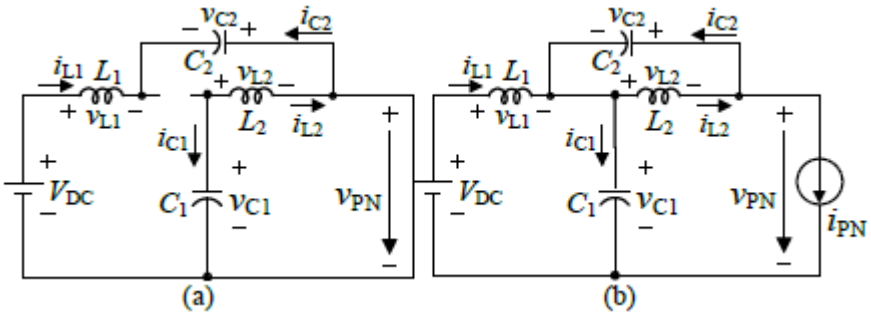

Figure.3.3: The S-P QZSI equivalent circuits. (a) shoot-through state; (b) non-shoot-through state

In this thesis, both the C_a of the S-P QZSI are of the same capacitance why both the L has same inductance, i.e., C=C_1=C_2 and L=L_1=L_2. Which are illustrated as follows:

1. When we have two capacitor that differs in capacitance, we would have different current behavior in inductor *L1* and L2. The aim of the design is to have a constant inductor current without having distorted waves.

2. We would notice an obvious occurrence that will be present if both inductors have unsimilar inductances. When we want to regulate and do the design it would be hectic because $C_1 \neq C_2$ and $L_1 \neq L_2$, If $C = C_1 = C_2$ and $L = L_1 = L_2$ the 4th -order system in

(10) can be minimized to the 2nd -order system shown in (3.19). $C_1 = C_2 = C$, $L_1 = L_2$ =L, $r_{L1} = r_{L2} = r_L$, and$r_{C1} = r_{C1} = r_C$ (3:15) gives

$$L\frac{d(i_{L1} - i_{L2})}{dt} = V_{DC} - (v_{C1} - v_{C2}) - (r_L + r_C)(i_{L1} - i_{L2})$$

$$C\frac{d(v_{C1} - v_{C2})}{dt} = i_{L1} - i_{L2} \tag{3.20}$$

From which follows

$$\begin{cases} LC\frac{d^2(v_{C1} - v_{C2})}{dt^2} + C(r_L + r_C)\frac{d(v_{C1} - v_{C2})}{dt} \\ \quad + (v_{C1} - v_{C2}) - V_{DC} = 0 \\ LC\frac{d^2(i_{L1} - i_{L2})}{dt^2} + C(r_L - r_C)\frac{d(i_{L1} - i_{L2})}{dt} \\ \quad + (i_{L1} - i_{L2}) = 0 \end{cases} \tag{3.21}$$

Referring to previous equations, during the steady state (3.21) becomes

$$i_{L1} - i_{L2} = 0, \qquad (v_{C1} - v_{C2}) - V_{DC} = 0 \tag{3.22}$$

Then the 4th-order system in (3:15) becomes the 2nd order dynamic system which is written as:

$$L\frac{di_{L1}}{dt} = (1 - D)V_{DC} + (2D - 1)v_{C1} - (r_L - r_C)i_{L1} + (1 - D)r_C i_{PN}$$

$$C\frac{dv_{C1}}{dt} = (1 - 2D)i_{L1} - (1 - D)i_{PN} \tag{3.23}$$

3.1.2 Mathematical analogy of current ripple and 2ω voltage

When we re-arrange equation 3.23, we come across a two-order differential equation:

$$\frac{d^2v_{C1}}{dt^2} + \frac{r_L + r_C}{L}.\frac{dv_{C1}}{dt} + \frac{(1-2D)^2}{LC}v_{C1} + \frac{1-D}{C}\frac{di_{PN}}{dt}$$

$$+\frac{1-D}{LC}[r_L + 2Dr_C]i_{PN} - \frac{(1-D)(1-2D)}{LC}V_{DC} = 0 \quad (3.24)$$

$$\frac{d^2i_{L1}}{dt^2} + \frac{r_L + r_C}{L}.\frac{di_{L1}}{dt} + \frac{(1-2D)^2}{LC}i_{L1} - \frac{(1-D)r_C}{L}\frac{di_{PN}}{dt}$$

$$-\frac{(1-D)(1-2D)}{LC}I_{PN} = 0 \quad (3.25)$$

Referring to [3.24], the general solution of (3.24) is $v_{c1} = y_c + y_p$. The harmonizing function y_c is the extensive result of the homogeneous differential equation in (3.24)

$$\frac{d^2y_c}{dt^2} + \frac{r_L+r_C}{L}.\frac{dy_c}{dt} + \frac{(1-2D)^2}{LC}y_c = 0 \quad (3.26)$$

$$m_{1,2} = \frac{-\frac{r_L+r_C}{L} \pm \sqrt{\left(\frac{r_L+r_C}{L}\right)^2 - 4\frac{(1-2D)^2}{LC}}}{2} \quad (3.27)$$

Which makes the roots real part to become negative making $y_c = 0$ when dealing with conditions at steady state. from (3.10) and (3.24), assuming the actual solution to be;

$$y_p = a_1\cos(2\omega t - \alpha) + b_1\sin(2\omega t - \alpha) + K \quad (3.28)$$

Differentiating y_p and substituting the answer in equation 3.24 and re-arranging them gives us

$$[-4\omega^2 a_1 + 2\omega b_1\frac{r_L + r_C}{L} + a_1\frac{(1-2D)^2}{LC}$$

$$+I_{2\omega}(r_L + 2Dr_C)\frac{1-D}{LC}]\cos(2\omega t - \alpha) + [-4\omega^2 b_1$$

$$-2\omega a_1 \frac{r_L+r_C}{L} + b_1 \frac{(1-2D)^2}{LC} - 2\omega I_{2\omega} \frac{1-D}{C}] \sin(2\omega t - \alpha) \quad (3.29)$$

$$+\frac{(1-2D)^2}{LC} k - \frac{(1-D)(1-2D)}{LC} V_{DC} + I_{PN} \frac{(1-D)(r_L+2Dr_C)}{LC} = 0$$

Equation (3.29) is meant to be an identity, the coefficients $a_1, b_1, and\ k$ gives us

$$a_1 = -\frac{[(1-2D)^2 - 4\omega^2 LC][I_{2\omega}(1-D)(r_L+2Dr_C)]}{[(1-2D)^2 - 4\omega^2 LC]^2 + [2\omega C(r_L+r_C)]^2}$$

$$-\frac{[2\omega I_{2\omega}(1-D)L][2\omega C(r_L+r_C)]}{[(1-2D)^2 - 4\omega^2 LC]^2 + [2\omega C(r_L+r_C)]^2}$$

$$b_1 = \frac{[(1-2D)^2 - 4\omega^2 LC][2\omega I_{2\omega}(1-D)L]}{[(1-2D)^2 - 4\omega^2 LC]^2 + [2\omega C(r_L+r_C)]^2}$$

$$-\frac{[I_{2\omega}(1-D)(r_L+2Dr_C)][2\omega C(r_L+r_C)]}{[(1-2D)^2 - 4\omega^2 LC]^2 + [2\omega C(r_L+r_C)]^2}$$

$$k = \frac{1-D}{1-2D} V_{DC} - \frac{I_{PN}(1-D)(r_L+2Dr_C)}{(1-2D)^2}$$

This means the capacitor C_1 at steady state has the voltage

$$v_{C1} = a_1 \cos(2\omega t - \alpha) + b_1 \sin(2\omega t - \alpha)$$

$$+\frac{1-D}{1-2D} V_{DC} - \frac{I_{PN}(1-D)(r_L+2Dr_C)}{(1-2D)^2} \quad (3.30)$$

Using same method in equation (3.25) for both inductors we can determine their steady state:

$$i_{L1} = i_{L2} = a_2 \cos(2\omega t - \alpha) + b_1 \sin(2\omega t - \alpha) + \frac{1-D}{1-2D} I_{PN} \quad (3.31)$$

With

$$a_2 = \frac{[(1-2D)^2 - 4\omega^2 LC] I_{2\omega}(1-D)(1-2D)}{[(1-2D)^2 - 4\omega^2 LC]^2 + [2\omega C(r_L+r_C)]^2}$$

$$+\frac{4\omega^2C^2I_{2\omega}r_C(1-D)(r_L+r_C)}{[(1-2D)^2-4\omega^2LC]^2+[2\omega C(r_L+r_C)]^2}$$

$$b_1=\frac{-[(1-2D)^2-4\omega^2LC][2\omega CI_{2\omega}(1-D)r_C]}{[(1-2D)^2-4\omega^2LC]^2+[2\omega C(r_L+r_C)]^2}$$

$$+\frac{2\omega CI_{2\omega}(1-D)(1-2D)(r_L+r_C)}{[(1-2D)^2-4\omega^2LC]^2+[2\omega C(r_L+r_C)]^2}$$

The 2ω voltage ripple and current ripple amplitude can be gotten mathematically from equation (3.30) and (3.31), sequentially. To make it easier we ignore the internal resistance of both inductors and capacitors, making the capacitor voltage C_1 to be

$$v_{C1}=\frac{2\omega I_{2\omega}(1-D)L}{(1-2D)^2-4\omega^2LC}\sin(2\omega t-\alpha)+\frac{1-D}{1-2D}V_{DC} \tag{3.32}$$

The inductor currents would be

$$i_{L1}=i_{L2}=\frac{I_{2\omega}(1-D)(1-2D)}{(1-2D)^2-4\omega^2LC}\cos(2\omega t-\alpha)+\frac{1-D}{1-2D}I_{PN} \tag{3.33}$$

Peak voltage for the dc-link envelope would be

$$v_{PN}=\frac{4\omega I_{2\omega}(1-D)L}{(1-2D)^2-4\omega^2LC}\sin(2\omega t-\alpha)+\frac{1}{1-2D}V_{DC} \tag{3.34}$$

Looking at (3.1), (3.10), (3.19), and (3.34), we deduce the equation to

$$i_L=\frac{1-2D}{\sqrt{[4\omega^2LC-(1-2D)^2]^2+\left[\frac{4\omega LI_{PN}(D-1)}{V_{PN}}\right]^2}}.\frac{V_0I_0}{V_{PN}} \tag{3.35}$$

$$v_C=\frac{2\omega L}{\sqrt{[4\omega^2LC-(1-2D)^2]^2+\left[\frac{4\omega LI_{PN}(D-1)}{V_{PN}}\right]^2}}.\frac{V_0I_0}{V_{PN}} \tag{3.36}$$

The phase angle would be;

$$\alpha = \emptyset - arctan\frac{4\omega LI_{PN}(1-D)}{[(1-2D)^2-4\omega^2 LC]V_{PN}} \quad (3.37)$$

We can determine the capacitance and inductance by using both equation 3.35 and 3.36. i^*L and v^*c, would be;

$$L = \frac{v^*_C(1-2D)}{2\omega i^*_L} \quad (3.38)$$

$$C = \frac{(1-2D)^2+\sqrt{(1-2D)^2\left(\frac{V_0 I_0}{V_{PN} i^*_L}\right)^2-\left[\frac{4\omega LI_{PN}(D-1)}{V_{PN}}\right]^2}}{4\omega^2 L} \quad (3.39)$$

3.1.3 Little-wave topology of s-p qzsi

When dealing with steady state, the terminology that changes on the left side in equation (3.23) gives us zero. Dealing with steady state, $i_{L1}, v_{C1} and\ i_{PN}$ in (3.23) becomes $I_{L1}, V_{C1}, and\ I_{PN}$ under constant D_e. Small variations d, $i_{s,L1}, v_{s,C1}\ and\ i_{s,PN}$ that may occur over $D_e, I_{L1,} V_{C1}\ and\ I_{PN}$, respectively, are expressed as

$$i_{L1} = I_{L1} + i_{s,L1}, \quad v_{C1} = V_{C1} + v_{s,C1}, \quad i_{PN} = I_{PN} + i_{s,PN}, \ D = D_e + d \quad (3.40)$$

Using equation (3.23) and (3.40), we determine the little signal model to be:

$$L\frac{di_{s,L1}}{dt} = (2D_e - 1)v_{s,C1} - (r_L + r_C)i_{s,L1} + (1 - D_e)r_C i_{s,PN}$$

$$+d(2V_{C1} - V_{DC} - r_C I_{PN}) + 2d.v_{s,C1} - d.r_C i_{s,PN} \quad (3.41)$$

$$C\frac{dv_{s,C1}}{dt} = (1 - 2D_e)i_{s,L1} - (1 - D_e)i_{s,PN}$$

$$+d\left(I_{PN} + i_{s,PN} - 2I_{L1} - 2i_{s,L1}\right)$$

Multiplication of two little signals should be discarded, i.e., $d.v_{s,C1}, d.i_{s,PN}, and\ d.i_{s,L1}$, the little signal model is re-arranged to give us

$$L\frac{di_{s,L1}}{dt} = (2D_e - 1)v_{s,C1} - (r_L - r_C)i_{s,L1} + (1 - D_e)r_C i_{s,PN}$$

$$+ d(2V_{C1} - V_{DC} - r_c I_{PN}) \qquad (3.42)$$

$$C\frac{dv_{s,C1}}{dt} = (1 - 2D_e)i_{s,L1} - (1 - D_e)i_{s,PN} + d(I_{PN} - 2I_{L1})$$

For d=0, we get

$$L\frac{di_{s,L1}}{dt} = (2D_e - 1)v_{s,C1} - (r_L + r_C)i_{s,L1} + (1 - D_e)r_C i_{s,PN}$$

$$C\frac{dv_{s,C1}}{dt} = (1 - 2D_e)i_{s,L1} - (1 - D_e)i_{s,PN} \qquad (3.43)$$

Equation,(3.43), show us , $D = D_e$

3.2 2ω Evaluating Control Stream and Enhancing QZS Circuit

We mentioned earlier that the quasi impedance network can be considered in a way to control second harmonic V and I, by using (3.38) and (3.39), we note that we don't minimize the impedance network. The second harmonic ripple amplitudes i^*L and v^*c, the added L and C are huge. Here, an optimization solution is to reduce the QZS network using second harmonic power flow calculation.

3.2.1 Evaluation of 2ω power components

We can derive the second harmonic power equation from (3.43) at the constant shoot-through duty cycle D_e. also the second harmonics for both L, can be calculated as:

$$p_{L-2\omega} = 2I_{L1}.L\frac{di_{s,L1}}{dt} \qquad (3.44)$$

And the two capacitors for 2ω power is

$$p_{C-2\omega} = C\frac{dv_{s,C1}}{dt}(V_{C1} + V_{C2}) = V_{PN}C\frac{dv_{s,C1}}{dt} \quad (3.45)$$

From the summation of (3.44) and (3.45) with (3.43) can be written as;

$$p_{L-2\omega} + p_{c-2\omega} = V_{DC}i_{s,L1} - (1 - D_e)\left(2v_{s,C1}I_{PN} + V_{PN}i_{s,PN}\right) \quad (3.46)$$

Adding both (3.19), (3.46) we get

$$p_{L-2\omega} + p_{C-2\omega} = V_{DC}i_{s,L1} + V_0 I_0 \cos(2\omega t - \emptyset) \quad (3.47)$$

2ω power direct current source would yield

$$p_{source-2\omega} = V_{DC}i_{s,L1} \quad (3.48)$$

From equation (3.6), we get

$$p_{0-2\omega} = V_0 I_0 \cos(2\omega t - \emptyset) \quad (3.49)$$

The equation (47) can be written as

$$p_{L-2\omega} + p_{C-2\omega} = p_{source-2\omega} + p_{0-2\omega} \quad (3.50)$$

And from (44), (45), and (48), there are

$$p_{L-2\omega} = -4\omega L I_{L1} i_L \sin(2\omega t - \emptyset) \quad (3.51)$$

$$p_{C-2\omega} = 2\omega C v_C V_{PN} \cos(2\omega t - \alpha) \quad (3.52)$$

$$p_{source-2\omega} = V_{DC} i_L \cos(2\omega t - \alpha) \quad (3.53)$$

Defining $P_{L-2\omega}, P_{C-2\omega}, P_{source-2\omega}$ *and* $P_{0-2\omega}$ as the phasors of $p_{L-2\omega}, p_{c-2\omega}, p_{source-2\omega}$, and $p_{0-2\omega}$ in (3.49), (3.51)-(3.53), we have

$$P_{L-2\omega} = 4\omega L I_{L1} i_L e^{j\left(\frac{\pi}{2}-\alpha\right)} \tag{3.54}$$

$$P_{C-2\omega} = 2\omega C v_C V_{PN} e^{-j\alpha} \tag{3.55}$$

$$P_{source-2\omega} = V_{DC} i_L e^{-j\alpha} \tag{3.56}$$

$$P_{0-2\omega} = V_0 I_0 e^{-j\emptyset} \tag{3.57}$$

We get, our power flow phasor equation in (50) to be

$$P_{L-2\omega} + P_{C-2\omega} = P_{source-2\omega} + P_{0-2\omega} \tag{3.58}$$

In (3.18), (3.33) -(3.37), and (3.54) -(3.57) the correlation gives us

$$P_{L-2\omega} = \frac{4\omega L {V_0}^2 {I_0}^2 \cos\emptyset}{\sqrt{{V_{PN}}^4[(1-2D_e)^2-4\omega^2 LC]^2+[4\omega L V_0 I_0 \cos\emptyset]^2}} e^{j\left(\frac{\pi}{2}-\alpha\right)} \tag{3.59}$$

$$P_{C-2\omega} = \frac{4\omega^2 LC V_0 I_0 {V_{PN}}^2}{\sqrt{{V_{PN}}^4[(1-2D_e)^2-4\omega^2 LC]^2+[4\omega L V_0 I_0 \cos\emptyset]^2}} e^{-j\alpha} \tag{3.60}$$

$$P_{source-2\omega} = \frac{V_0 I_0 {V_{PN}}^2 (1-2D_e)^2}{\sqrt{{V^2}_{PN}[(1-2D_e)^2-4\omega^2 LC]^2+[4\omega L V_0 I_0 \cos\emptyset]^2}} e^{-j\alpha} \tag{3.61}$$

$$\alpha = \emptyset + arctan\frac{4\omega L V_0 I_0 \cos\emptyset}{[4\omega^2 LC-(1-2D)^2]{V_{PN}}^2} \tag{3.62}$$

In (3.57) and (3.59) -(3.62) describe the effect of ϕ, which the phase angle between voltage and current, on the second harmonic powers $\mathbf{P}_{0\_2\omega}$, $\mathbf{P}_{L\_2\omega}$, $\mathbf{P}_{C\_2\ \omega}$, and $\mathbf{P}_{source\_2\omega}$. It is worth

knowing that the power factor Cos ϕ, needed no to be reduced so not to cause DCM of QZSI.

CHAPTER 4

PROPOSED TOPOLOGY AND SIMULATION RESULTS

4.1 Presented Topology

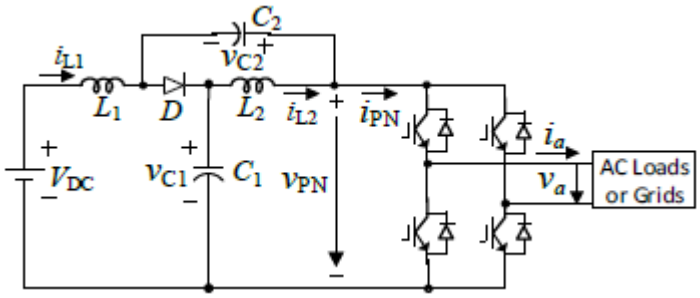

Figure 4.1: Proposed Circuit Diagram for simple phase QZSI

This part of the thesis ascertains the use of software simulation (PSCAD) to get our results. From our chapter 3, we mentioned that the optimized method yields a greatly reduced quasi z-source L and C in contrast to the previous way. We summarize our design terms in table I for simulation purpose.

Table 4.1: Simulation Parameters

Components	Quantity	Values
Input voltage	1	
Inductor	2	0.000517H
Capacitor	2	1900µF
switches (IGBT)	4	
Diode	1	
Total	**10**	

4.2 Simulation Results

The simulated results are as follows.

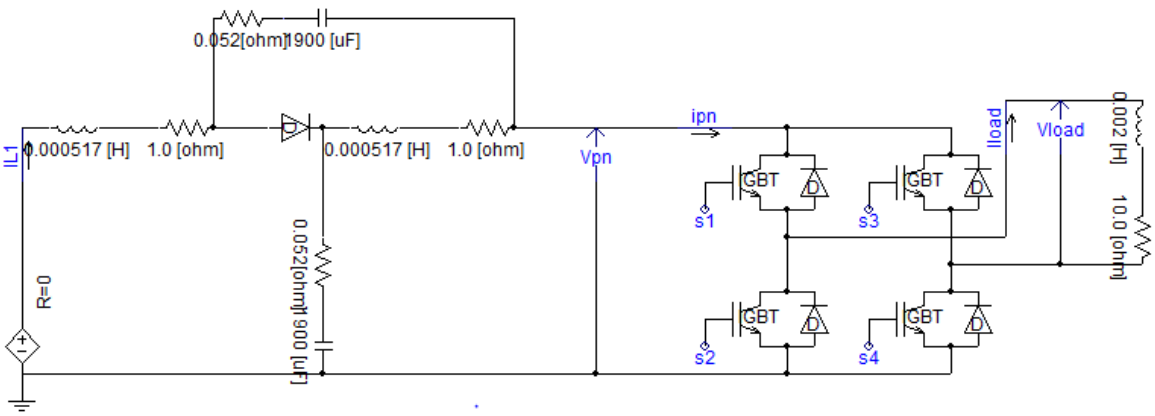

Figure 4.2: PSCAD Designed Circuit Diagram for Single phase QZSI

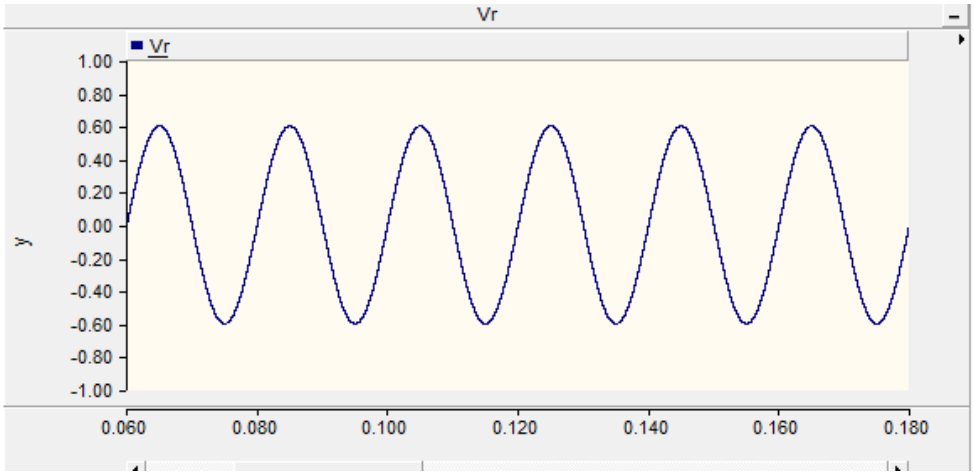

Figure 4.3: The Voltage of the load inductive resistance

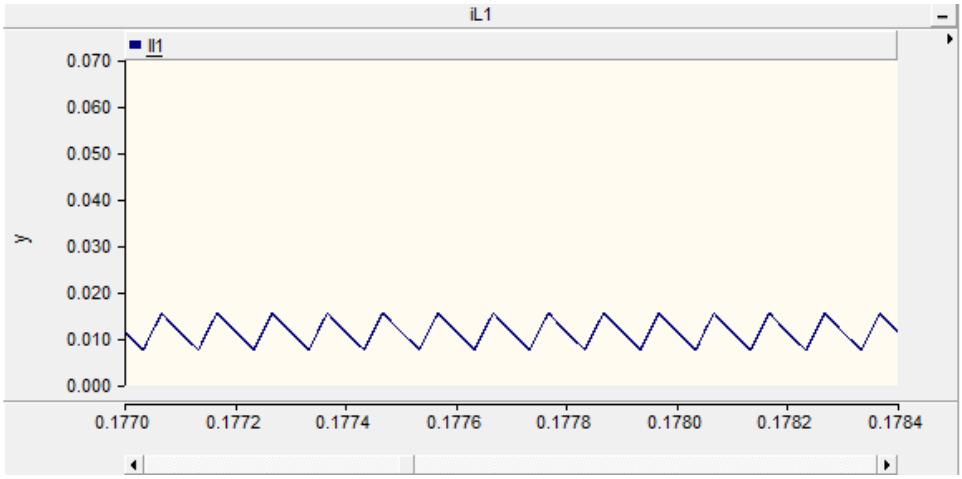

Figure 4.4: The Input Current

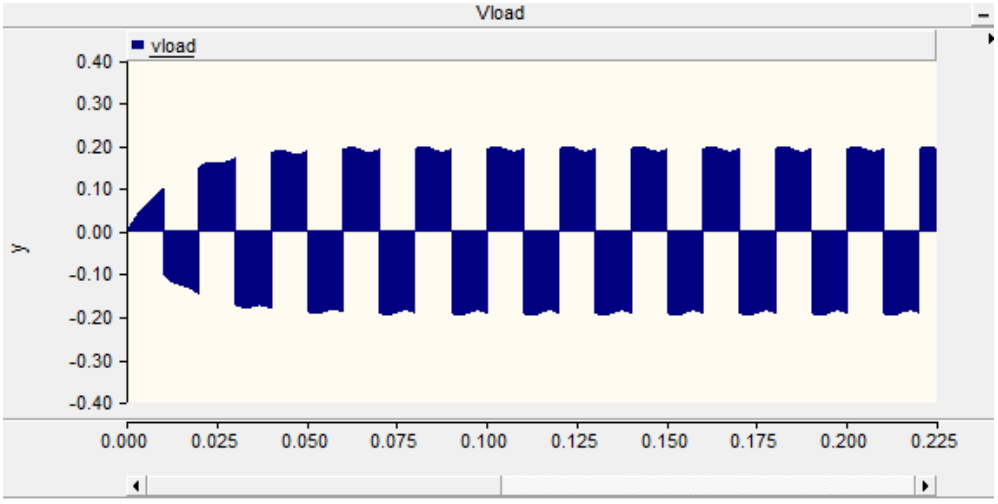

Figure 4.5: The Voltage at the load

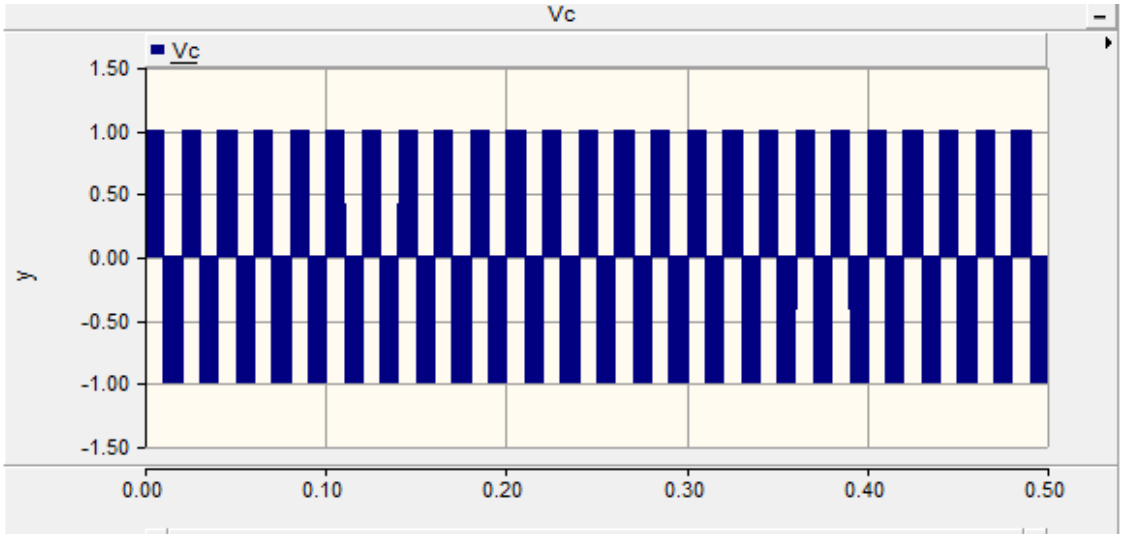

Figure 4.6: Capacitive Voltage

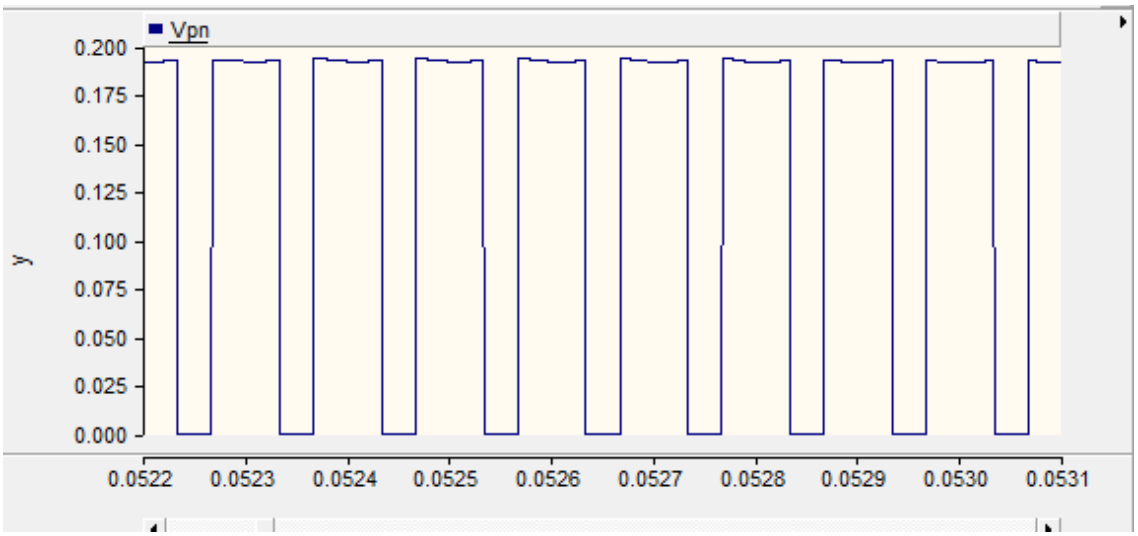

Figure 4.7: Average Direct current link peak Voltage envelope

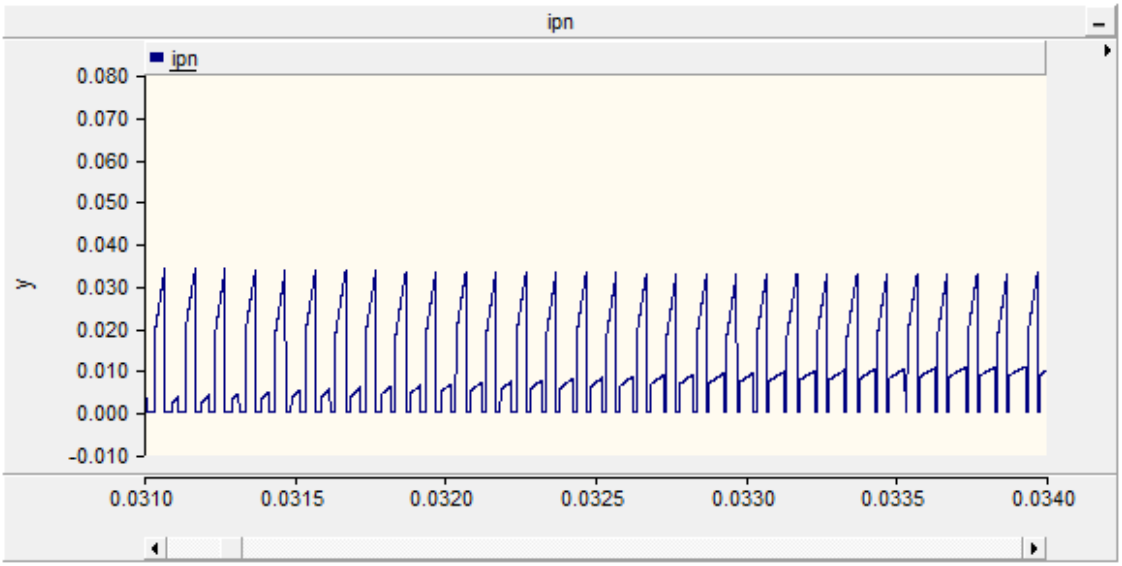

Figure 4.8: The Direct Current link peak current

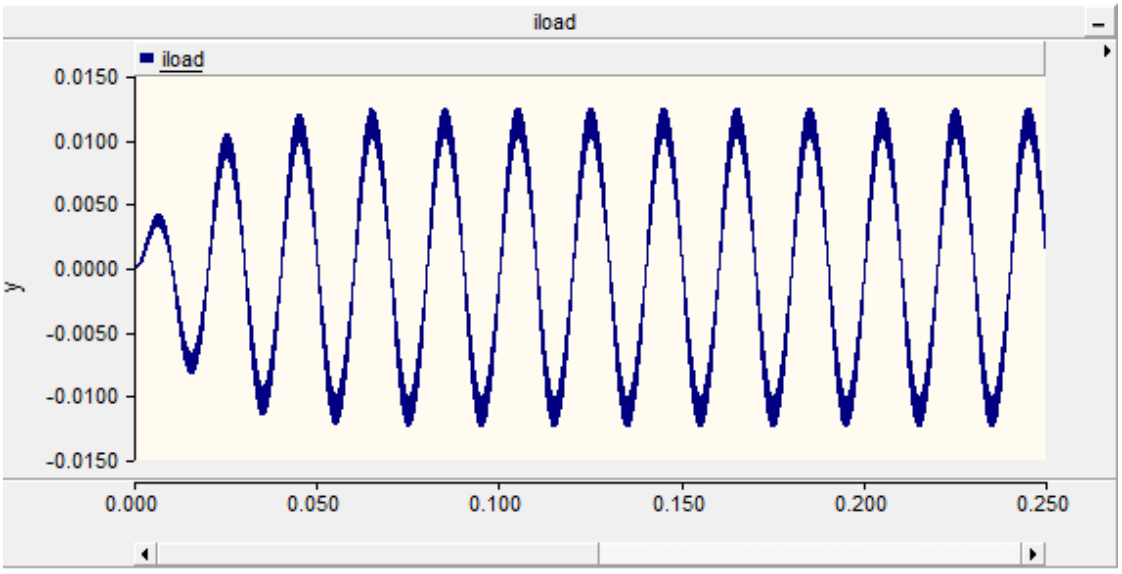

Figure 4.9: Current at the Load

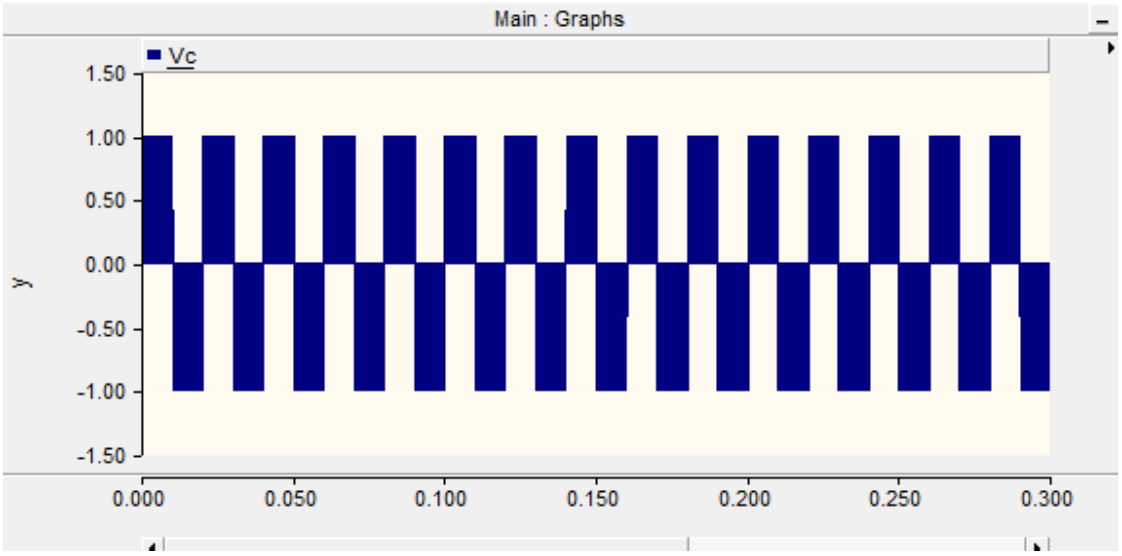

Figure 4.10: Voltage across capacitor

CHAPTER 5
CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

An improvement plan technique was proposed to limit the impedance system of the converter and to simultaneously diminish the distorted wave in the quasi z-source capacitors. We had to compare the proposed and attained quasi-z-source capacitance to the previous capacitance, this quasi z source '*L'* is exceptionally little so as confining its exchanging recurrence current wave. We proposed a model and power stream for the 2ω ripple and also the current of an inductor wave was proposed and intended to guarantee the removal of ripples in the circuit which was important to be able to accomplish the ideal structure. Hypothetical examination, impedance assessment, was done and also, we used PSCAD software to simulate and evaluate our results.

5.1 Recommendations

The mode of operations in this thesis research is covered only by single phase QZSI and it is designed with two capacitors of same values $C=C_1=C_2$ and two inductors of same inductance, $L=L_1=L_2$. A future research objective from this work is to design a single phase QZSI that will have different capacitance and also different inductance. The different capacitance will cause distinctively current anomaly in L1 and L2, the inductor L2 would have a higher distorted wave especially if capacitance of the circuit is not in equilibrium. Furthermore, when we have large inductor ripple current it brings about high amount of real power loss. Likewise, when the capacitance is not equal it will cause the dc-link voltage to be higher in light of the fact that it is the after effect of the total of the 2ω voltage wave of the two capacitors.

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