NENUBARI MARVIN KOMI

31-LEVELS CASCADED MULTILEVEL INVERTER WITH LESS COMPONENTS

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NEAR EAST UNIVERSITY

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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

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M.Sc. THESIS

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Nicosia

November, 2022

Approval

We certify that we have read the thesis submitted by Komi Nenubari Marvin titled **"31-Levels cascaded multilevel inverter with less components"** and that in our combined opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Masters in Electrical and Electronics Engineering.

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Declaration

I hereby declare that all informant, documents, analysis and results in this thesis have been collected and presented according to the academic rules and ethical guidelines of the institute of Graduate Studies, Near East University. I also declare that as required by these rules and conduct, I have fully cited and referenced information and data that are not original to this study.

Komi Nenubari Marvin

Day/Month/Year

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Abstract

31-Levels cascaded multilevel inverter with less components

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M.S.c, Department of Electrical and Electronics Engineering

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This thesis proposes two new basic units of a single-phase multilevel inverter. The basic units are developed into submultilevels by series connection. Based on the new submultilevel units, several cascaded topologies of single-phase multilevel inverters are proposed. Amongst the proposed topologies is a cascaded structure composed of two submultilevels. This proposed cascaded inverter generates only 15-levels of positive output voltage, when coupled to an H-bridge, 31-levels of positive and negative output voltages are generated. The proposed 31-levels single-phase inverter is realized with minimum component count i.e. 4 dc sources, 12 unidirectional semiconductor switches and driver circuits respectively. High quality output voltage waveform, generation of high levels of output voltage with fewer components, less complex cascaded structure, lower mass and dimension of inverter , diminished cost of inverter, minimal level of inverter setbacks, and use of lesser voltage rating switches are the primary benefits of the envisaged configuration. To confirm the benefits and effectiveness of the suggested inverter, a comparison is made between the recently proposed inverter and current designs. Also calculated is the converter's standing voltage. Simulation findings are then used to verify the feasibility and effectiveness of the developed multilayer inverter.

Keywords: Cascaded Multilevel Inverter; Fundamental Frequency; Symmetric and Asymmetrical and Standing voltage.

Özet

31-Levels Cascaded Multilevel Inverter with less components

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Bu tezde, tek fazlı çok seviyeli bir eviricinin iki yeni temel birimi önerilmektedir. Temel birimler, seri bağlantıyla alt düzeylere dönüştürülür. Yeni çok düzeyli alt birimlere dayalı olarak, tek fazlı çok seviyeli eviricilerin birkaç kademeli topolojisi önerilmiştir. Önerilen topolojiler arasında iki alt-çoklu seviyeden oluşan kademeli bir yapı bulunmaktadır. Bu önerilen kademeli evirici, bir H köprüsüne bağlandığında sadece 15 seviyeli pozitif çıkış gerilimi üretir, 31 seviyeli pozitif ve negatif çıkış gerilimi üretilir. Önerilen 31 seviyeli tek fazlı evirici, minimum bileşen sayısı, yani sırasıyla 4 dc kaynak, 12 tek yönlü yarı iletken anahtar ve sürücü devresi ile gerçekleştirilmiştir. Önerilen topolojinin ana avantajları, yüksek kaliteli çıkış gerilim dalga biçimi, daha az bileşen sayısı ile yüksek seviyelerde çıkış gerilim üretimi, daha az karmaşık kademeli yapı, azaltılmış inverter hacmi ve boyutu, azaltılmış inverter maliyeti, minimum evirici kayıpları ve daha düşük değerli anahtarların uygulanmasıdır. Önerilen eviricinin bu avantajlarını ve üstünlüğünü doğrulamak için, önerilen evirici ve mevcut topolojilerin karşılaştırmalı analizi incelenmiştir. Dönüştürücünün daimi gerilimi de hesaplanır. Son olarak, önerilen çok seviyeli eviricinin uygulanabilirliği simülasyon sonuçları ile doğrulanmıştır.

Anahtar Kelimeler: kademeli çok seviyeli evirici, temel frekans, simetrik ve asimetrik ve sabit gerilim.

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List of Abbreviations

AC:	Alternative Current
CHB:	Cascaded H-Bridge
DC:	Direct Current
FACTS:	Flexible Alternative Current Transmission Systems
FC:	Flying Capacitors
FFC:	Fundamental Frequency Control
HVDC:	High Voltage Direct Current
IGBT:	Insulated-Gate Bipolar Transistor
KVL:	Kirchhoffs Voltage Law
MI:	Modulation Index
MLI:	Multi-Level-Inverter
MOSFET:	Metal-Oxide-Semiconductor Field-Effect Transistor
NLC:	Nearest Level Control
NPC:	Neutral Point Clamped
PWM:	Pulse-Width Modulation
THD:	Total Harmonic Distortion

CHAPTER 1

Introduction

1.1 Scope of the Research

The primary application of cutting edge or avant-garde semiconductor based devices namely; diodes, IG bipolar transistor (IGBT), MO-semiconductor field-effect transistor (MOSFET) and appropriate control mechanism to properly condition voltage for various applications such as integration of renewable energy into grid system, industrial drive systems, electric vehicle charging, electric locomotives, Flexible Alternative CTS and High Voltage DC transmission is known as power electronics (PE). It provides the means by which the characteristic of voltage can be changed or varied from AC to DC or DC to AC, buck or boost functionality within the same or different form of voltage (AC or DC) and also frequency and phase variations.

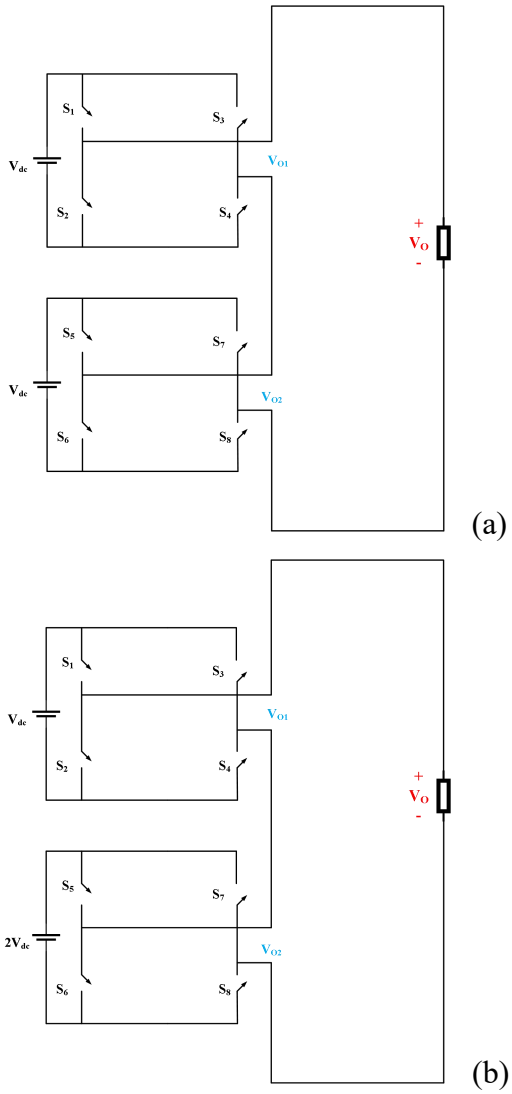
The physical means which voltage conditioning is achieved is by the application of a device commonly known as power electronic converter or converter for short. The term converter broadly covers all devices which are able to change the form or nature of voltage and also provide amplitude variations. One of these commonly used converters is the multilevel inverter (MLI) which has been in existing for past three decades. The quantum of attention being received by multilevel inverter from researchers and also as a first-choice device for industrial applications is overwhelming and such will (MLI) continue to be in existence for a long while. Several topologies of multilevel level inverters have been developed since the introduction of the three conventional topologies. These conventional topologies are CHB, FC and DC inverters. Classification of multilevel inverters are done from various points of view, some of the factors used in classifying multilevel inverters are:

- Number of DC source utilized
- Type of input/source
- Type of phase
- With or without transformer
- Control technique utilized

Cascaded H-Bridge (CHB) MLI is the most popular topology amongst the conventional multilevel inverter topologies. This fact can be attributed to the many advantages it offers when compared to the other two topologies of FC and DC MLIs. The most important advantage is the simplicity with which higher levels of output voltages can be derived. Unlike the other two topologies, higher levels of output voltage is a major limitation because of complex inverter structure and cumbersome control technique. CHB multilevel inverters also have major limitation; each CHB unit requires separate dc source but recent published topologies attempt to utilize one dc source and a number of capacitors. Therefore, there is a trade between the dc source quantity and the capacitors.

Cascaded H-bridge multilevel inverters are derived when two or units of H-bridge inverters are series connected. From KVL point of view, connecting the H-bridge units in series will provide the needed level or stepped output voltage. The total output voltage of the cascaded structure is the sum of the output voltage of the individual H-bridge inverters in the cascaded connection. From the voltage magnitude perspective, CHB are classified into two distinct categories; these are symmetric and asymmetric CHB MLI. These two types of cascaded H-bridge inverters differ only voltage magnitudes. Symmetric topologies have equal magnitudes of voltages for each of the H-bridge units, however, asymmetric topologies have unequal magnitude of H-bridge voltages. Examples of symmetric and asymmetric topologies are shown by Figure 1a and Figure 1b accordingly. The examples shown below have two units of H-bridge inverters only, however, theoretically, there are no limits to the quantity of H-bridge units for the cascaded structure.

Figure 1
(a) Symmetric CHB MLI (b) Asymmetric CHB MLI

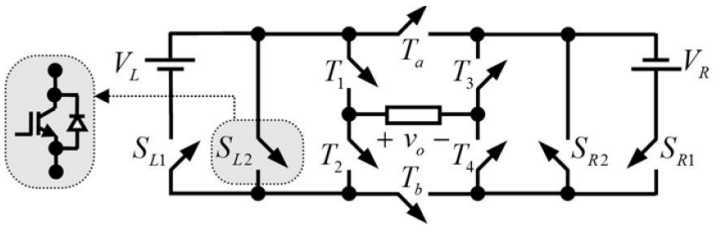


Asymmetric topologies are categorized into binary and trinary topologies. Two new terms or topologies introduced by (E. Babaei, 2022) are semi-symmetric and semi-asymmetric. These topologies have voltage variations which are semi in magnitude from one H-bridge to the other H-bridge units in the cascaded structure. Detailed analysis of these topologies are presented in chapter 3 of this thesis. Multilevel inverters have come to stay and are not being obsolete any time soon. Rather, researchers investigating ways of improving existing topologies by design new topologies. Therefore, newly designed MLI topologies have two common similarities; reducing the quantity of devices mainly semiconductor switches and dc

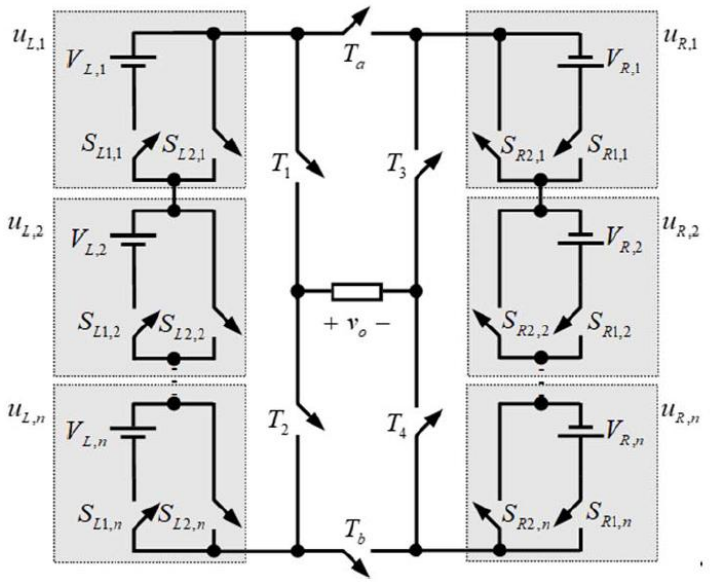
sources and at the same time generating highest or maximum levels of output voltages. Several of such new topologies with reduced component quantity have been published in academia and other are being utilized in industries. Below are some examples of MLI topologies designed with less component count. Single-phase topologies alone will be mentioned here because this thesis focus on cascaded single-phase topologies. Figure 2a shows a single-phase MLI with high output voltage levels, the cascaded structure is shown by Figure 2b

Figure 2

(a) Single phase MLI (b) Cascaded single phase MLI (Aalami et al., 2018)



(a)



(b)

1.2 Statement of Problem

Although multilevel inverters have gained much popularity in academia and industry because of the enormous advantages they possess, they still have a few limitations. These limitations tend to reduce efficiency of these inverters. Conventional cascaded H-bridge multilevel inverters require more dc sources and semiconductor power switches to generate higher levels of output voltage. For

example, the cascaded structure of Figure 1a utilizes two dc sources and eight semiconductor power switches to generate 5-levels of load voltage. With the same component count, the cascaded structure of Figure 1b can generate 7-levels of load voltage. As shown by the two topologies, the latter topology (asymmetric) is able to generate more levels of load voltage by varying the magnitude of one of the H-bridges. Trinary topologies are able to even generate higher levels of load voltage by further varying the magnitude of the dc source, with the same component configuration of Figure 1b, 9-levels of load voltage is generated by trinary topologies. Therefore, it's evident that output voltage levels of multilevel inverters can be highly maximized by controlling the magnitude of the input voltages.

1.3 Research Purpose and Objective

The research purpose and objective is to comprehensively investigate symmetric as well as asymmetric cascaded MLI topologies with respect to potential output voltage levels when magnitudes of the input or source voltages are varied. This comprehensive investigation will encompass single-phase H-bridge multilayer trickled inverters. This thesis offers a novel cascaded multilayer inverter based off a new fundamental and sub multilevel unit built on the findings of a thorough and extensive research. The proposed multilevel inverter is analyzed under symmetric and asymmetric dc voltage characteristics. Theoretical computation of inverter losses and standing voltage is provided. Comparative analysis of the proposed topology and existing topologies are reviewed. Finally, the power circuit of the proposed topology is built and simulated in PSCAD software.

1.4 The Significance of the Thesis

Multilevel inverters have gained much popularity in academia and industry because of the enormous advantages they possess. They have therefore become integral part of voltage conditioning. The importance of this research is to lay bare the advantages and disadvantages of symmetric and asymmetric multilevel inverters by comprehensive investigations. The results of this investigations shows that asymmetric multilevel inverters require less component count to generate higher levels of load voltage when compared to symmetric multilevel inverter. Utilizing fewer components to achieve much greater output voltage has some essential benefits:

- Low dimension and capacity
- Cost - effective and secure inverter
- Decreased wastage
- Improved efficacy and waveform quality

It is also essential to note that certain cascaded multilevel inverters do not need a transformer.

1.5 Limitation of Study

Simulation based research tends to have the least of limitations, however proper and efficient application of the software tool tends to introduce a few limitations when the applicant does not so much experience in its usage. Even in the absence of laboratory investigations, the chosen software of PSCAD provides minimum differences between laboratory results and simulation results. Cascaded multilevel inverters become complex structurally and difficult to control if very high levels of output voltages are desired.

1.6 Outline of the Study

The overall content of the dissertation was depicted in four sections, each of which adheres to the criteria of the near east university. Below are the various outlines of the sections.

Chapter 1: The content of this section includes Introduction and other subsections namely; research scope and background; Problem Statement; Research aim/objectives; Research significance and Thesis Outline.

Chapter 2: comprises Theoretical and Empirical Review of Multilevel Converters.

Chapter 3: comprises Topology Proposed and Results of Simulation

Chapter 4: contains Future Works and Conclusion

CHAPTER 2

Literature Review of Multilevel Inverters

2.1 Introduction

Within the last few years, power electronic converters or devices have become essential tool in electrical power conditioning for all categories of power. These converters can be found in low power gadgets such as power supplies with small switching capabilities for use in mobile devices, laptops, and desktop computers, motor drive system for electric cars and bikes and large power devices utilized in distribution and transmission grids. Various topologies and control techniques have been developed during these times; these topologies are suitable for single or multi-phase systems applications in industrial, grid or drives systems.

Comprehensive literature review of multilevel inverters (MLI) is presented in this section of my research. This review focuses on three main points; power circuit or topology, modulation techniques and new trends (topologies) with emphasis on the reduction of topology components (mainly switches and dc sources). Continuous industrial and academic interest in multilevel inverters has resulted in the presentation of novel topologies and improved control techniques.

2.2 Multilevel Inverters (MLI)

Multilevel inverters were introduced as an alternative to the two-level inverter which has some drawbacks such as the use of large filters to eliminate high harmonics and its unsuitability for high power applications due to high power ratings of semiconductors devices (Trabelsi et al., 2021). Interest in multilevel inverter development keeps soaring in industry and academia since the first MLI topology was introduced in the 1980s. This continuous interest has led to the development of new topologies and modulation techniques. Multilevel inverters make use of small multiple dc sources to generate three or more levels of output voltages; higher levels of output voltage produce quality ac output waveform. With respect to categorization, multilevel inverters are grouped into three groups namely; cascaded H-bridged, flying capacitor and diode clamped multilevel inverters. The above topologies are regarded as the traditional or conventional topologies. Other topologies of multilevel inverters such as hybrid MLI, impedance based MLI topologies and modular MLI

have been presented over the years. Additionally, reducing component quantity as well as enhanced techniques of modulation are the primary focus of newer topologies of MLI.

2.2.1 Cascaded H-Bridge MLI (CH-MLI)

The simplest topology amongst conventional MLI in terms of architecture and modulation is the Cascaded H-bridge MLI (CH-MLI). Also, it's the most utilized and researched topology in academia and industry. As the name implies, cascaded H-bridge MLI is derived by series connection of two or more H-bridge structures. The term "cascaded" is also applied to flying capacitor and diode clamped topologies, which also means the series connection of multiple units of the respective topologies. However, the latter topology, cascaded H-bridge MLI is able to easily support higher levels of output voltage when compared to flying capacitor and diode clamped topologies. Figure 3, shows the conventional H-bridge inverter; 3-levels of output voltage is generated by the H-bridge inverter when appropriate switching and modulation techniques are employed. Table 1 illustrates the acceptable switching states of the inverter. The ***on*** or ***off*** states of the various switches are represented by one (1) or zero (0) respectively. The cascaded H-bridge inverter is shown by Figure 4, this structure is suitable for single-phase applications, increasing the number of "legs" to three makes it ideal for three-phase power systems. Three H-bridges are series connected to form the cascaded topology.

Figure 3

H-bridge inverter

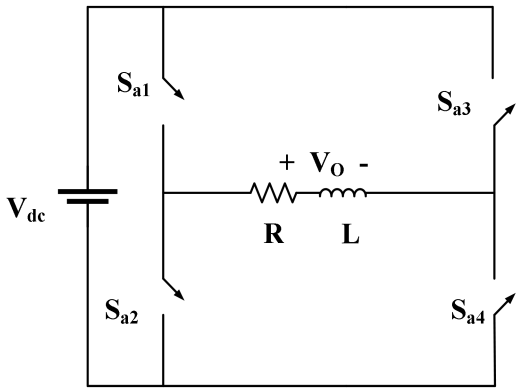


Table 1
H-bridge inverter switching table

	SWITCHES				
STATE	**S_1**	**S_2**	**S_3**	**S_4**	**V_O**
I	1	0	0	1	V_{dc}
II	0	1	1	0	$-V_{dc}$
III	1	0	1	0	0
	0	1	0	1	

The cascaded topology generates 7-levels of output voltage. 2-levels of output voltage is added for each H-bridge added to the cascaded connection. Sum output voltages for the three units of H-bridges provide the total output voltage of the cascaded structure. Since the source voltages of each H-bridge are equal in magnitude, individual H-bridges are able to generate the same magnitude of output voltages. Therefore, some states of operation produce repetitive magnitudes of output voltages. To eliminate these repetitive total output voltages, switching operations which produce these magnitude of total output voltage is reduced to one state. Table 2 shows the switching states for the cascaded topology of Figure 4.

Figure 4
H-bridge Inverter

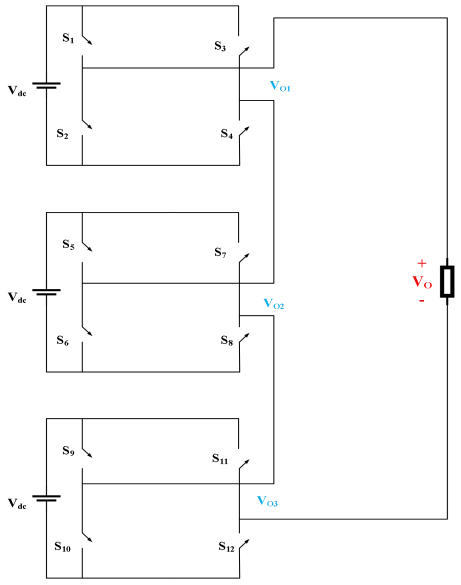


Table 2

Switching pattern for 7-levels inverter

STATE	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	V_O
I	1	0	0	1	1	0	1	0	0	1	0	1	V_{dc}
II	1	0	0	1	1	0	0	1	0	1	0	1	$2V_{dc}$
III	1	0	0	1	1	0	0	1	1	0	0	1	$3V_{dc}$
IV	1	0	1	0	1	0	1	0	0	1	0	1	0
V	0	1	1	0	0	1	0	1	1	0	1	0	$-V_{dc}$
VI	0	1	1	0	0	1	1	0	1	0	1	0	$-2V_{dc}$
VII	0	1	1	0		1	1	0	0	1	1	0	$-3V_{dc}$

Although Table 2 shows the switching states of the 7-level inverter, other permutation of switching can generate the same desired output shown in Table 2 For example, to generate positive V_{DC}, either the first, second or third H-bridge is controlled to generate positive V_{DC} whiles the other H-bridges are controlled to generate zero voltage. This methodology can be applied to other states of switching; hence the provided switching states of Table 2 is not a fixed switching.

Table 3

Cascaded MLI topologies

	Symmetrical Inverter	**Asymmetrical inverter**	
		Binary	**Trinary**
Output voltage level	2n + 1	2n + 1 -1	3n
Quantity of DC sources	N	n	n
Quantity of switches	4n	4n	4n
Quantity of driver circuit			
Maximum output voltage	N	2n - 1	$\frac{3^n - 1}{2}$

Cascaded H-bridge multilevel inverters are generally categorized into two groups; symmetric and asymmetric cascaded H-bridge multilevel inverters. These two topologies of cascaded H-bridge multilevel inverters are equivalent in architecture but differs by virtue of the dc voltage magnitude of the H-bridges applied. In cases where the dc voltages are equal in magnitude for all H-bridges in the cascaded architecture, then the symmetric cascaded H-bridge multilevel inverter is formed. However, if there's any difference in the dc voltage magnitude of the H-bridges, then asymmetric cascaded multilevel inverter is formed. Asymmetric cascaded MLI is also categorized into two groups, binary and trinary topologies. The mathematical relationship between the different topologies of cascaded MLI is depicted in Table 3. The number of H-bridges employed in the cascaded architecture is denoted as *n* in the table.

Figure 4: Contains three H-bridges, if the input voltages of all three H-bridges are equivalent in magnitude then symmetric cascaded MLI is formed as shown by Figure 5 and Figure 6. However, varying the input voltage of any of the H-bridges will result in the formation of asymmetric cascaded MLI as depicted by Figure 7a and Figure 7b.

Figure 5
Symmetric cascaded MLI

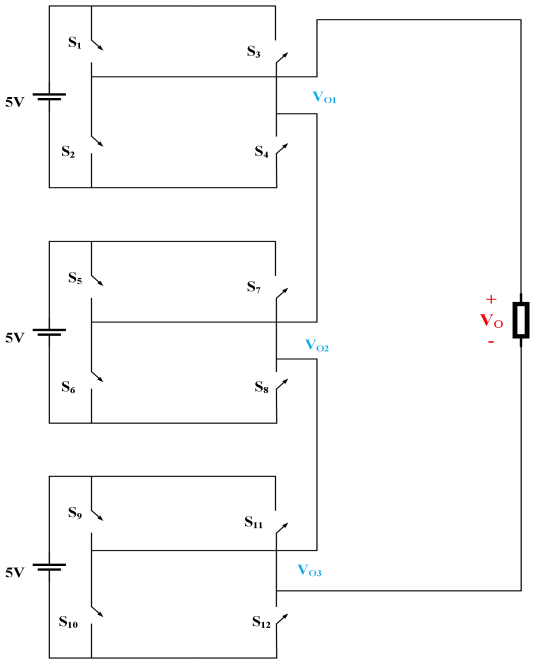
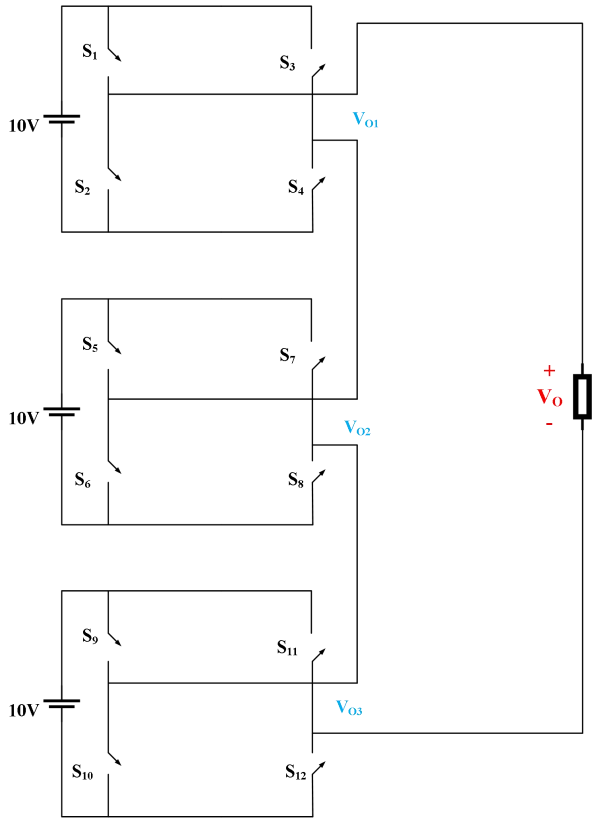
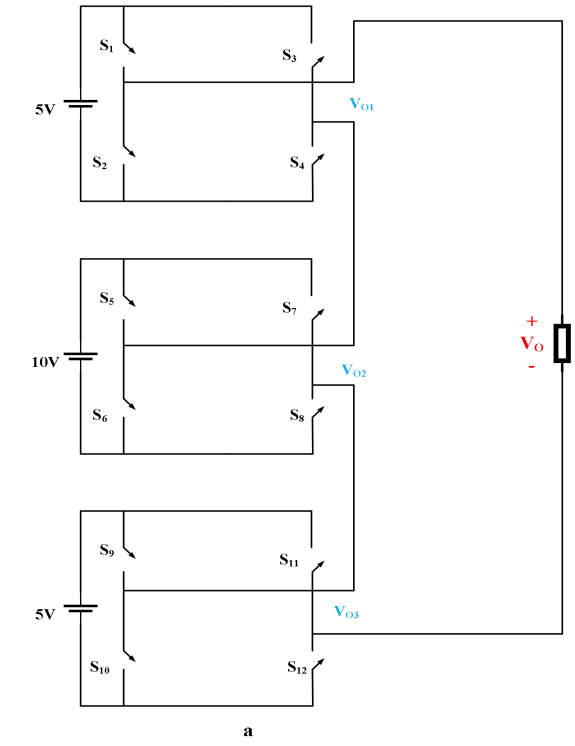


Figure 6
Symmetric Cascaded MLI

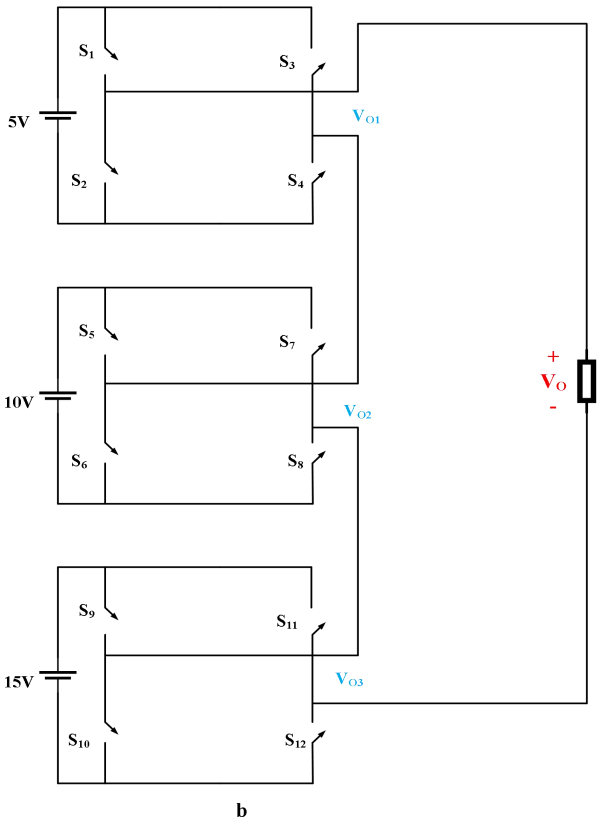


Symmetric and asymmetric cascaded MLI topologies are similar in structure but differ in the number of output voltages levels they can generate individually. With the same number of H-bridges in a cascaded structure, asymmetric topologies produce more levels of output voltages than the symmetric topology. Also, trinary topologies produce more output voltage levels than binary topologies. To produce equally number of output voltage levels between binary and trinary topologies, the latter topology utilizes less number of H-bridges for the cascaded structure. Similarly, asymmetric topologies utilize less number of H-bridges to produce equal output voltage levels as the symmetric topologies. Reduced H-bridge count translates into less quantity of power switches and therefore reduced switching and conduction losses.

Figure 7
Symmetric Cascaded MLI topologies



a



b

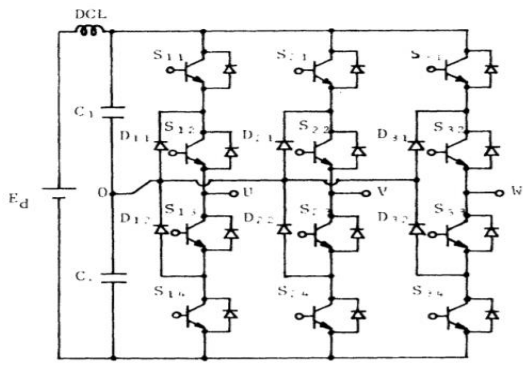
2.2.2 Diode Clamped MLI

Diode clamped MIL also known as NPC (neutral point clamped) is the other type of the conventional MLI. NPC topologies are different in structure from cascaded MLI but a bit similar to flying capacitor (FC) topology. NPC topologies utilizes one dc voltage source and cascaded capacitors which provides the various magnitude of output voltage levels. Therefore, there is a direct correlation between the number and voltage magnitude of capacitors and number and magnitude of output voltage levels. The voltage source and cascaded capacitors are connected in parallel. Also, NPC topologies employs high number of diodes for voltage clamping purposes. These diodes increase the overall component quantity and is the major drawback of NPC topologies. Increasing the number of output voltage levels increases the quantity of capacitors and diodes required, this disadvantage makes NPC topologies not suitable for generating higher levels of output voltage. Modularity of NPC topologies is complex and also control mechanism becomes complicated when compared to cascaded topologies. The first NPC topology illustrated by Figure 8 was introduced by Nabei in 1981. As predicted by Figure 8, the presented NPC topology is a three-phase MLI composed of one dc source, two capacitors, six clamping diodes and 12 semiconductor switches. The maximum levels of output voltage of the first NPC topology is 3-levels i.e. generated load voltages are 0V, $+\frac{1}{2}E_d$, $-\frac{1}{2}E_d$. The source voltage is shared equally across the two capacitors; therefore, the capacitor voltages are expressed below by equation (2.1).

$$\mathrm{V_{C1}} = \frac{1}{2}\mathrm{E_d} = \mathrm{V_{C2}} = \frac{1}{2}\mathrm{E_d} \tag{2.1}$$

Figure 8

Three-phase 3 levels NPC MLI (Nabei, 1981)



Other types of NPC topologies derived from the conventional topology of Figure 8 have been presented. Below are some examples of improved NPC topologies. Figure 9 shows single-phase conventional topology where the clamping diodes are illustrated in red colour. The clamping diodes are replaced with semiconductor switches to produce active NPC shown by Figure 10. Also, T-type NPC is derived when bidirectional switch is put in place of the clamping diodes, Figure 11 shows the T-type NPC.

Figure 9
NPC (Nabei, 1981)

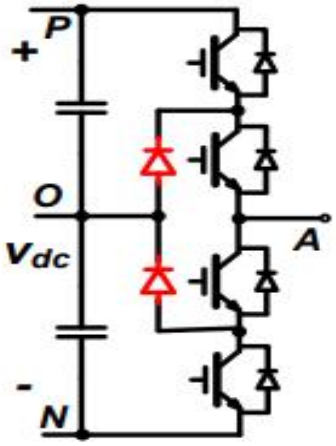


Figure 10
Active NPC (Nabei, 1981)

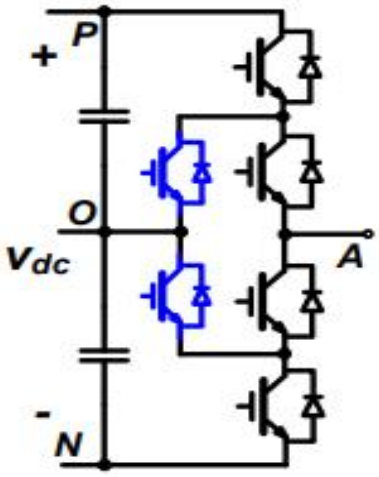
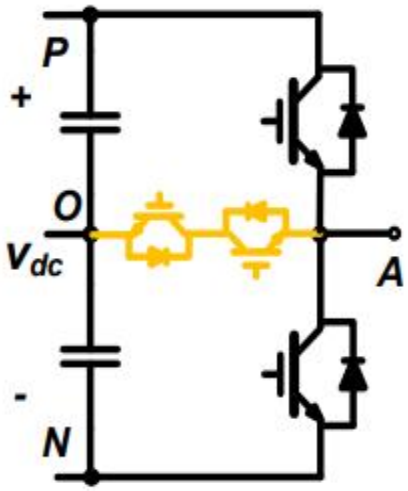


Figure 11

T-type NPC (Nabei, 1981)



2.2.3 Flying Capacitor MLI

Flying capacitor (FC) multilevel inverters are similar in structure and operation when compared to NPC topology. FC topology was introduced in 1992 by Meynard and Foch (Meynard and Foch, 1992). FC multilevel inverters are composed of one dc source connected in parallel to multiple cascaded capacitor networks and cascaded semiconductor switch structure. Each cascaded capacitor network provides each output voltage level. The source voltage is divided across the cascaded capacitor networks hence the load voltage determined by these capacitor voltages. One major advantage of FC topology is the application one dc voltage source, on the other hand, application of multiple clamping capacitors increases the size and cost of FC topologies. Also, application of FC topologies for higher levels of load voltage is a major drawback because of the increased capacitor quantity, complex structure and complicated control techniques. FC topologies provide the following advantages (Sinha and Lipo, 1997);

- Acceptable for photovoltaic application
- Minimizes harmonic content
- Clamping diodes are not required
- Multiple dc sources not required unless in cascaded topologies
- Suitable for high voltage system

- Output filter are not required when FC topologies are used
- Useful for reactive power compensation

The dc voltage magnitude of each cascaded capacitor network varies in magnitude to the other capacitor network i.e. each cascaded capacitor network provide different magnitude or level of load voltage.

Table 4
5-levels FC MLI switching pattern (Lai and Peng, 1996).

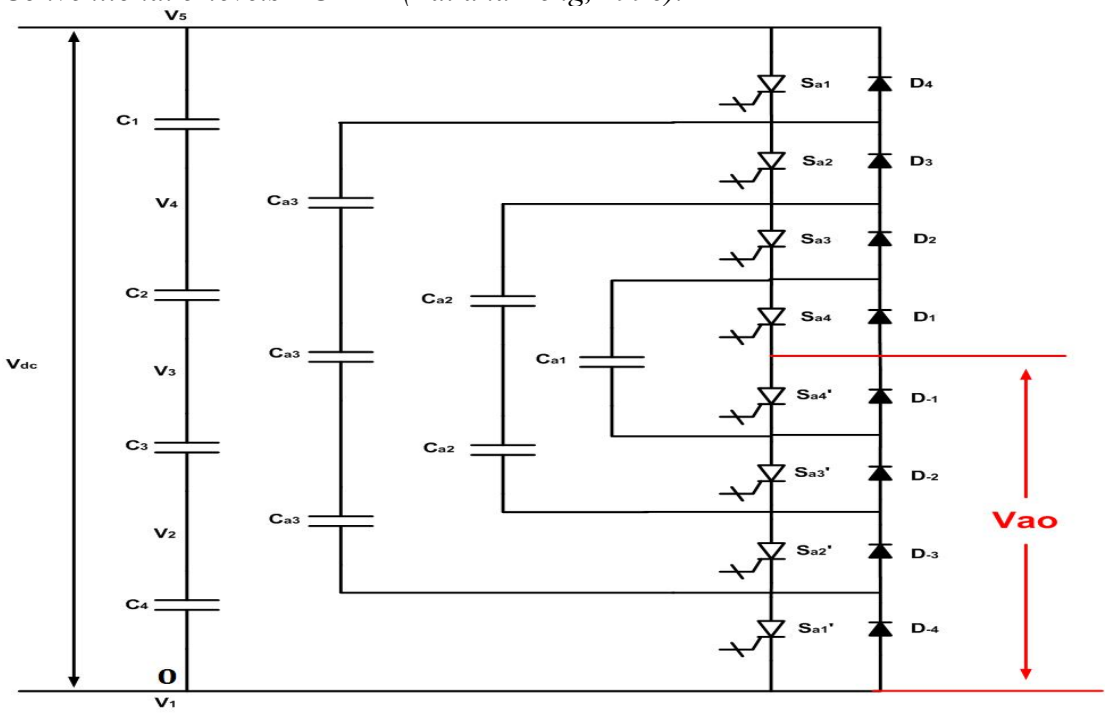
	SWITCHES								VO
STATE	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$	
I	1	1	1	1	0	0	0	0	$V_5 = V_{dc}$
II	1	1	1	0	1	0	0	0	$V_4 = 3V_{dc}/4$
III	1	1	0	0	1	1	0	0	$V_3 = V_{dc}/2$
IV	1	0	0	0	1	1	1	0	$V_2 = V_{dc}/4$
V	0	0	0	0	1	1	1	1	$V_1 = 0$

Figure 12 shows a conventional 5-levels FC multilevel inverter. As illustrated in Figure 12, there are three cascaded capacitor network and one independent capacitor. In total, ten clamping capacitors, one dc source and eight semiconductor switches are used to build the topology.

The desired output voltage is generated by following the correct switching state shown by Table 4. Capacitor C_{a1} provide the output voltage magnitude for state IV, capacitors C_{a2} provide the output voltage magnitude for state III, capacitors C_{a3} provide the output voltage magnitude for state II and finally capacitors C_1, C_2, C_3 and C_4 provides the output voltage magnitude for state I. The corresponding voltage magnitudes are given in Table 4 for state of operation (Lai and Peng, 1996).

FC topologies provide inner voltage level redundancy. When compared to NPC topology, FC topology provides redundancy for phases whiles redundancy for line to line is provided for by NPC topology only (Lai and Peng, 1996; Tolbert et al., 1999). Redundancy provides the necessary control to balance capacitor voltages and also regulate charging and discharging of the capacitor voltages.

Figure 12
Conventional 5-levels FC MLI (Lai and Peng, 1996).



2.3 Selected Multilevel Inverter Topologies

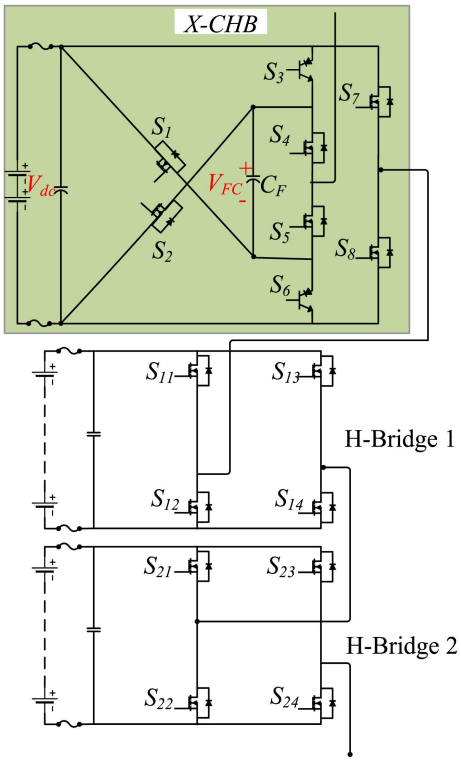
This section reviews selected published papers on the three conventional MLI topologies of described above. Also, other types of multilevel inverter topologies such as Hybrid MLI and Stacked MLI will be reviewed. However, much credence will be placed on cascaded H-bridge topologies since that's is the focal point of this thesis.

2.3.1 Cascaded H-Bridge MLI Review

A fault tolerant hybrid based cascaded H-bridge multilevel inverter was presented in (Mhiesan et al 2020). Due to increased semiconductor switch count in the cascaded topology, the probability of having faulty switches is high. This reduces the reliability and operation of cascaded H-bridge topologies. Therefore, a new characteristic is introduced which ensures cascaded H-bridge topologies are robust and reliable during operation. This new feature is achieved by introducing crossed or X shaped switches into the conventional H-bridge structure. Figure 13 shows the structure of the proposed hybrid cascaded topology, two units of H-bridges are cascaded together with a third H-bridge which contains the X shaped feature. The presented topology has 14 power switches and 2 transistors, each unit of H-bridge contains 2 dc sources and 1 capacitor. Apart from the fault tolerant capabilities of the

presented topology, it also has voltage boosting feature by a factor of 2. The presented hybrid topology can generate 7-levels of voltage.

Figure 13
Single-phase hybrid cascaded H-bridge MLI (Mhiesan et al 2020)



In (Hasan et al 2018), a new topology of cascaded three-phase H-bridge inverter having high frequency magnetic link and reduced component count was presented. The major limitation of cascaded H-bridge which requires each unit to have separate dc source is eliminated in this topology. Also galvanic isolation feature is provided in this topology where input and output sections of the inverter can be separated when required. This characteristic makes the presented topology suitable for grid applications. The presented topology generates higher levels of output voltage because of the application of asymmetric feature. Figure 14a show the presented topology which composed of one traditional 2-levels three-phase inverter and cascaded structure of H-bridges, Figure 14b shows the conventional H-bridge. The magnetic link of high frequency is provided by a toroid core which enables high power density and compact size of the inverter. The toroid core is shown by Figure 15.

Figure 14
Cascaded three-phase multilevel inverter (Hasan et al 2018)

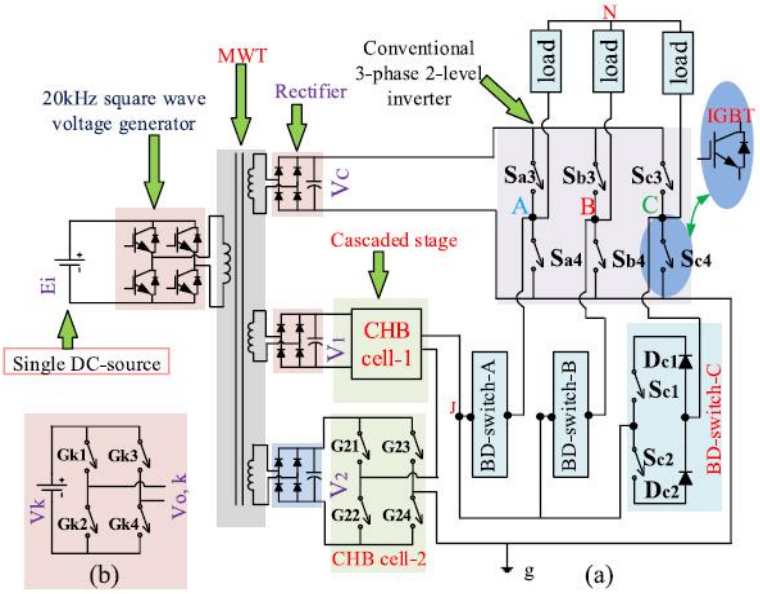
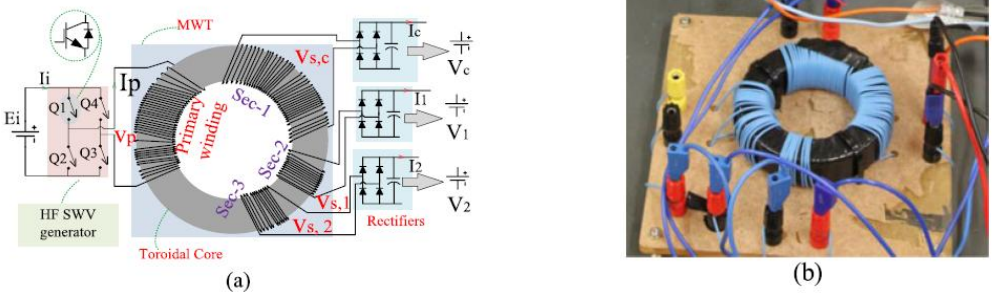


Figure 15
Toroid magnetic link: (a) single dc source feeding multiple rectifiers (b) multi-winding transformer. (Hasan et al 2018)



A new single topology of cascaded MLI was presented by the authors in (Babaei et al 2015). The cascaded topology is derived by series connection of the presented basic unit illustrated by Figure 16. The presented topology generates positive output voltages only hence H-bridge is required to generate negative output voltages. 5 semiconductor switches and three dc source make up the basic unit. The major advantages of the presented topology are reduction in component quantity i.e. dc sources, driver circuit and semiconductors switches whiles being able to generate higher levels of output voltage. These advantages are true when compared to conventional cascaded H-bridge inverters. Different voltage algorithms are presented for the input dc source to obtain the highest possible levels of output voltage. Figure

17a shows the cascaded structure without an H-bridge while Figure 17b shows the cascaded structure incorporated with an H-bridge.

Figure 16
Basic unit structure (Babaei et al 2015)

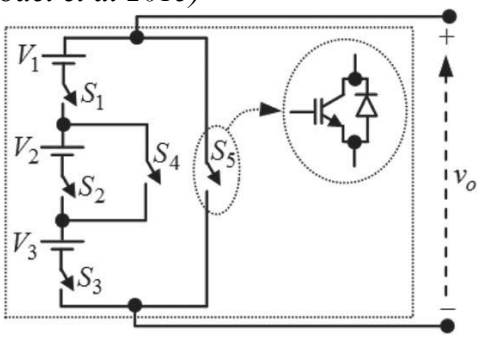
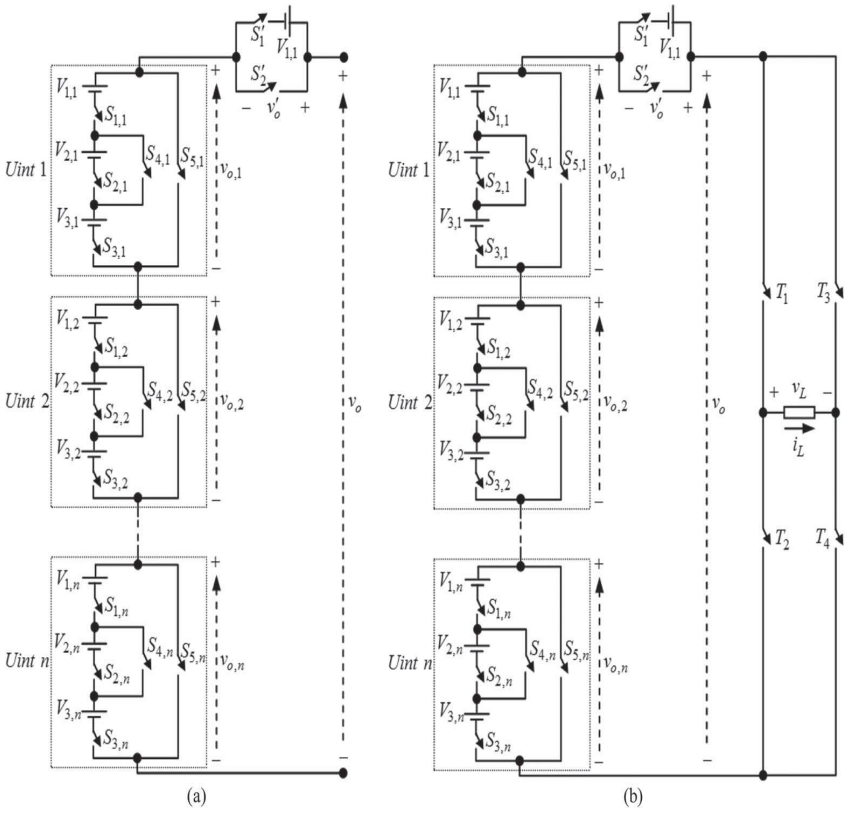


Figure 17
Cascaded single-phase MLI: (a) without H-bridge (b) with H-bridge. (Babaei et al 2015)



An improved cascaded H-bridge inverter is presented in (Siddique et al 2019). The basic unit is derived by adding 2 unidirectional switches, 1 bidirectional switch and 2 dc sources to the H-bridge topology; the derived structure is illustrated by Figure 18. Generalized structure of the same topology is illustrated by Figure 19. The driver

circuit and switches are governed by the following equations below. k denotes the number of dc sources:

$$N_{driver,F} = (N_{driver,F} - 1)\frac{k+4}{4k-2} \quad (2.2)$$

$$N_{driver,S} = In(\frac{N_{driver,S}+1}{2})\frac{k+4}{In(2k)} \quad (2.3)$$

$$N_{driver,T} = In(N_{driver,T})(\frac{k+4}{In(4k-1}) \quad (2.4)$$

$$N_{switch,F} = (N_{switch,F} - 1)\frac{2k+2}{4k-2} \quad (2.5)$$

$$N_{switch,S} = In(\frac{N_{switch,S}+1}{2})\frac{2k+2}{In(2k)} \quad (2.6)$$

$$N_{switch,T} = In(N_{switch,T})(\frac{2k+2}{In(4k-1}) \quad (2.7)$$

Figure 18
Basic unit (Siddique et al 2019)

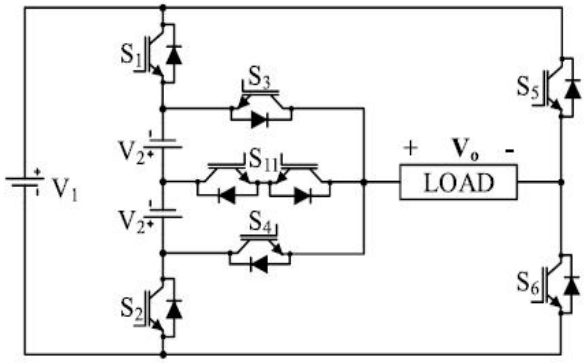
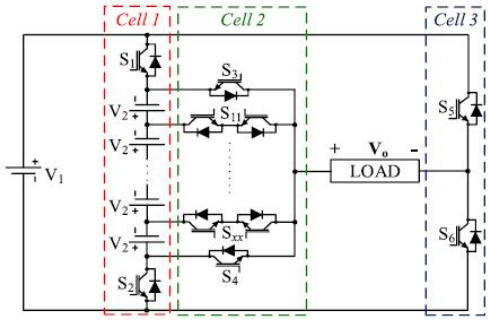


Figure 19
Generalized structure (Siddique et al 2019)



The possible switching pattern of the basic unit is illustrated below by Figure 20. Each output voltage is indicated separate block diagram, e.g. to generate zero (0) output voltage, switches S_1, S_3 and S_5 conducts whiles the others remain off.

This is represented by the first block on the left hand side of Figure 20. The second block shows the conducting switches when V_{dc} is generated.

Figure 20
Basic unit switching states for positive half cycle (Siddique et al 2019)

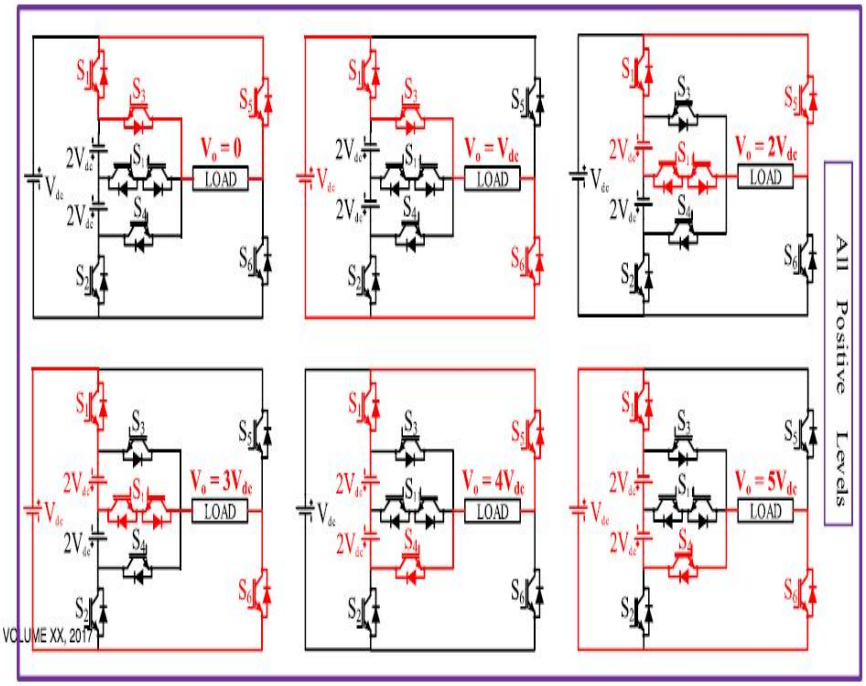
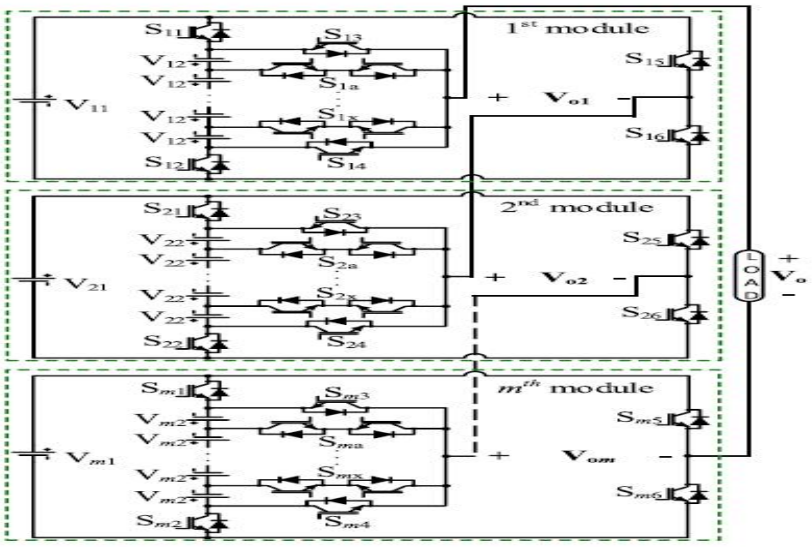


Figure 21
Cascaded structure of improved H-bridge inverter (Siddique et al 2019)



2.3.2 Diode Clamped MLI Review

A new active NPC multilevel inverter was presented by (Lee et al 2020). Active NPC are derived by replacing clamping diodes of the conventional NPC with semiconductor power switches. The voltage gain capabilities in Active NPC are naturally low therefore more dc sources are required to generate high levels of output voltage. The presented topology resolves limitations of the conventional Active NPC topologies, its cable of generating 7-levels of output voltage and 1.5 times boosting feature. This topology is derived from the 5-levels topology presented in (Siwakoti, 2018) by adding only one semiconductor switch. The 7-levels can be increased to 9-levels or 11-levels by adding a floating capacitor and three semiconductor switches. 5-levels and 7-levels structures are represented by Figure 22 and Figure 23 respectively. Figure 24 shows the 9-levels with unity voltage gain or 11-levels with 2.5 voltage feature.

Figure 22
Active 5-levels NPC inverter. (Siwakoti, 2018)

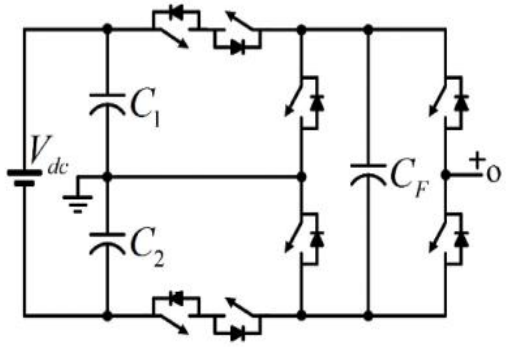


Figure 23
Active 7-levels NPC inverter. (Siwakoti 2018)

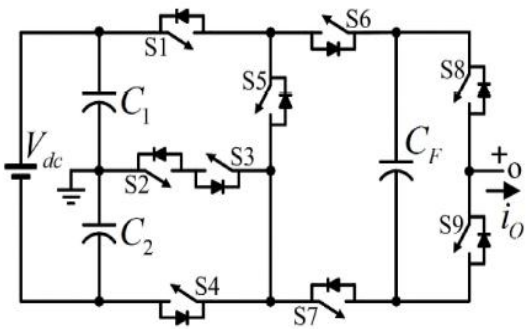
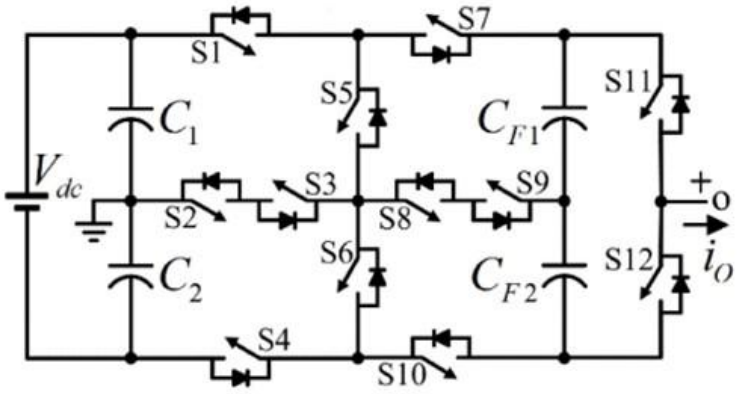


Figure 24
Active 11-levels NPC inverter. (Siwakoti, 2018)



The peak to peak ripple voltage at fundamental frequency is given below by the equation (2.8) where:

$$\Delta V_C = \frac{\hat{I}_{load}}{2\pi f_o C} \tag{2.8}$$

- ΔV_C is the dc-link capacitor ripple voltage.
- $\hat{I}_{load}$ is the maximum load current of the fundamental.
- f_o is the fundamental frequency of 50Hz.
- C is the capacitance of C_1 and C_2.

Similarly, floating capacitors' voltage ripples are determined by equation (2.9) below where:

$$\Delta V_{CF} = \frac{\hat{I}_{load} \cos\left(90^0 - 0.5\theta\right) cos\varphi}{\pi f_o C_F} \tag{2.9}$$

- ΔV_{CF} is the floating capacitor ripple voltage.
- $\hat{I}_{load}$ is the maximum load current of the fundamental.
- f_o is the fundamental frequency of 50Hz.
- C_F is the floating capacitor.

Impedance based topologies have proven to have higher boosting features. In (Xing et al 2014), Z-source network is combined with NPC inverter to yield ZS-NPC inverter for three-phase applications. Impedance based inverters have two modes of operation, shoot-through and non-shoot-through states, the latter state provides electromagnetic radiation protection for the switches, also the boosting feature is achieved during this state. The presented topology is shown by Figure 25.

For three-phase operation of the presented topology, upper and lower shoot through are enabled as shown by Figure 26 and Figure 27 respectively, one state of non-shoot through is enabled which is shown by Figure 28. The following equations are developed for the non-shoot through operation. The input voltage V_i is determined when the ZS diodes D1 and D2 are conducting by equation (2.10), during this state, the V_L inductor voltage is given by equation (2.11), the boost factor B, load voltage V_{ac} and modulation index M are related and expressed by equation (2.12).

$$V_i = 2(V_C - E) \tag{2.10}$$

$$V_L = 2E - V_C \tag{2.11}$$

$$V_{ac} = B\frac{M}{\sqrt{3}}2E \tag{2.12}$$

Figure 25
Z-Source three-phase NPC inverter. (Xing et al 2014)

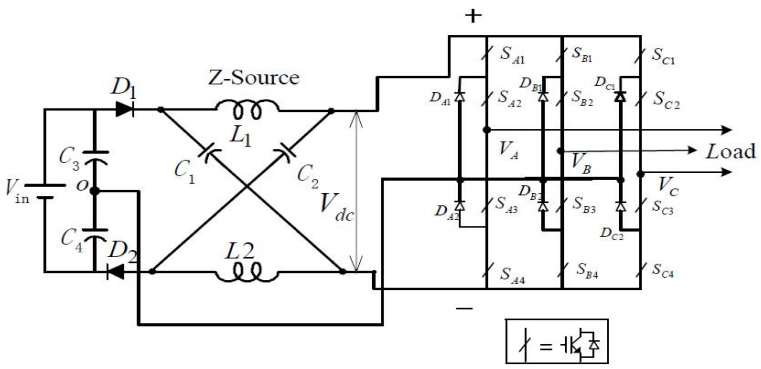


Figure 26
Shoot-through state for upper level (Xing et al 2014)

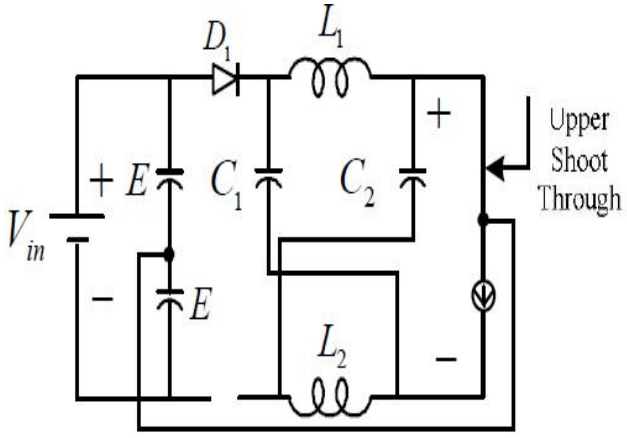


Figure 27
Shoot-through state for lower level (Xing et al 2014)

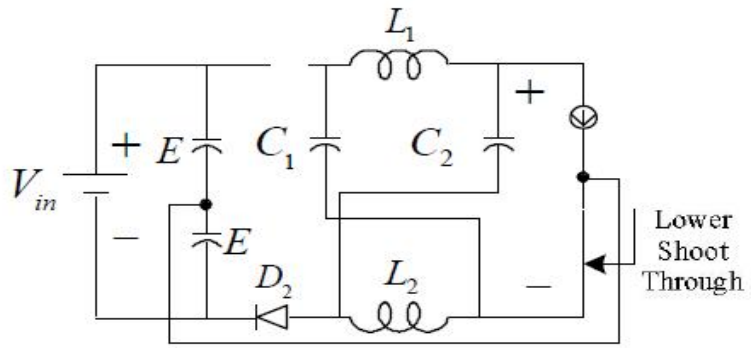
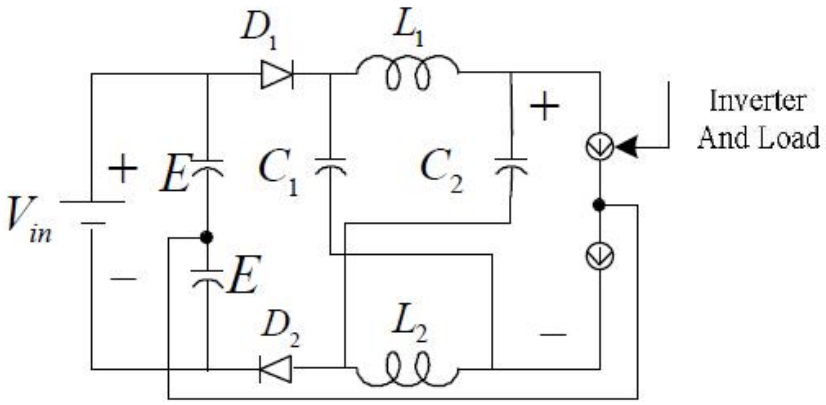


Figure 28
Non-shoot through state (Xing et al 2014)



Quasi ZS networks (QZS) are improved version of the conventional ZS networks. Quasi ZS networks provides higher boosting capabilities when compared to the traditional ZS networks, this feature is achieved with minimum duty cycle. Total harmonic distortion (THD) is reduced because of the applied duty cycle. Also inrush current characteristic is present in QZS inverters and voltage stress on switches is less. A three-phase quasi Z-source NPC is presented by (Ahmadzadeh and Babaei 2018) is illustrated by Figure 30. This QZS-NPC (Ahmadzadeh and Babaei, 2018) has two states of operations; shoot-through and non-shoot-through. Shoot through state has three mode of operation: the upper and lower sections are operated individually for the first and second modes of operation and are combined for the third mode of operation. These modes of operation are depicted by Figure 29. During the upper level shoot through operation, the following equations are developed for the upper and lower peak voltages and boost factor.

$$v_{upper,peak} = \frac{V_{dc2}}{1-4D} \tag{2.13}$$

$$v_{lower,peak} = \frac{V_{dc2}}{1-4D} \tag{2.14}$$

$$B = \frac{1}{1-4D} \tag{2.15}$$

Figure 29

Upper and lower operations of ZS-NPC (Ahmadzadeh and Babaei, 2018)

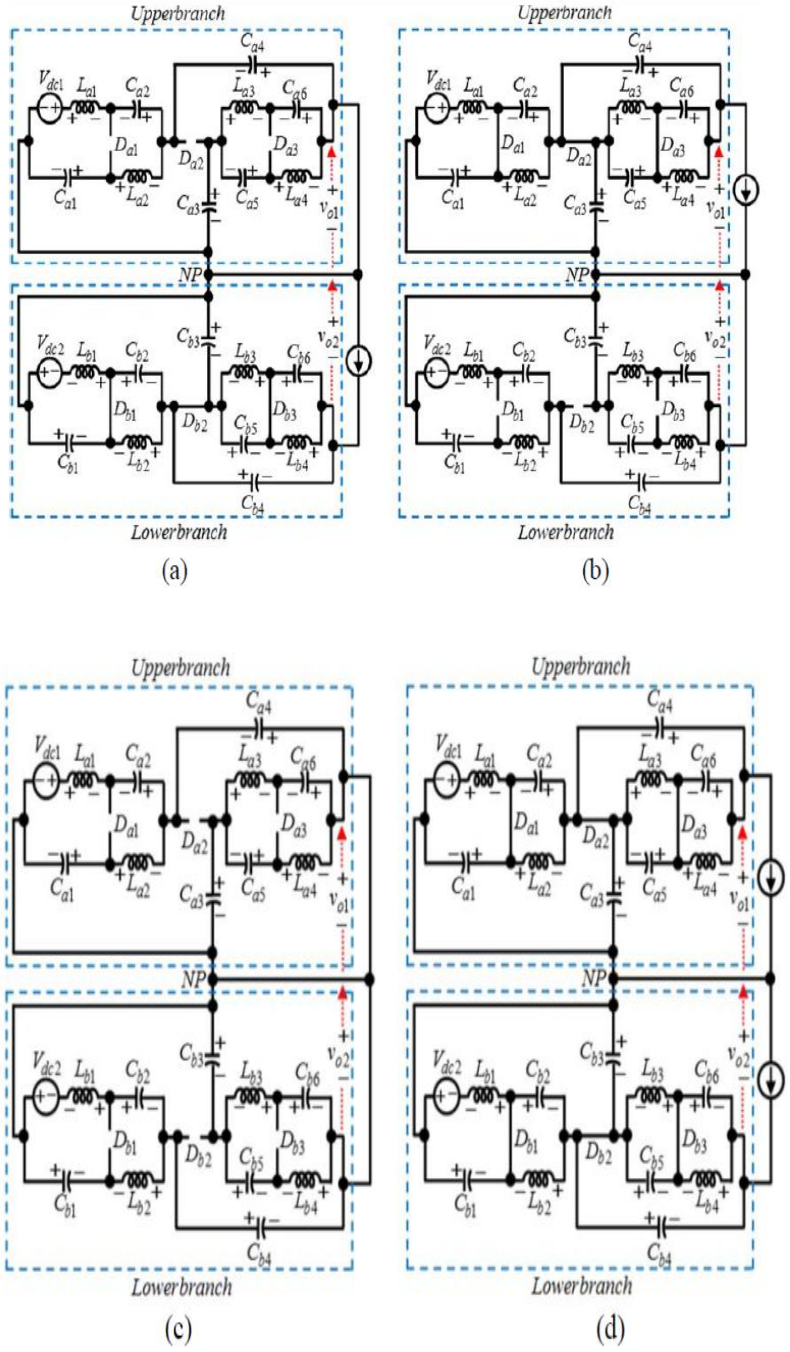
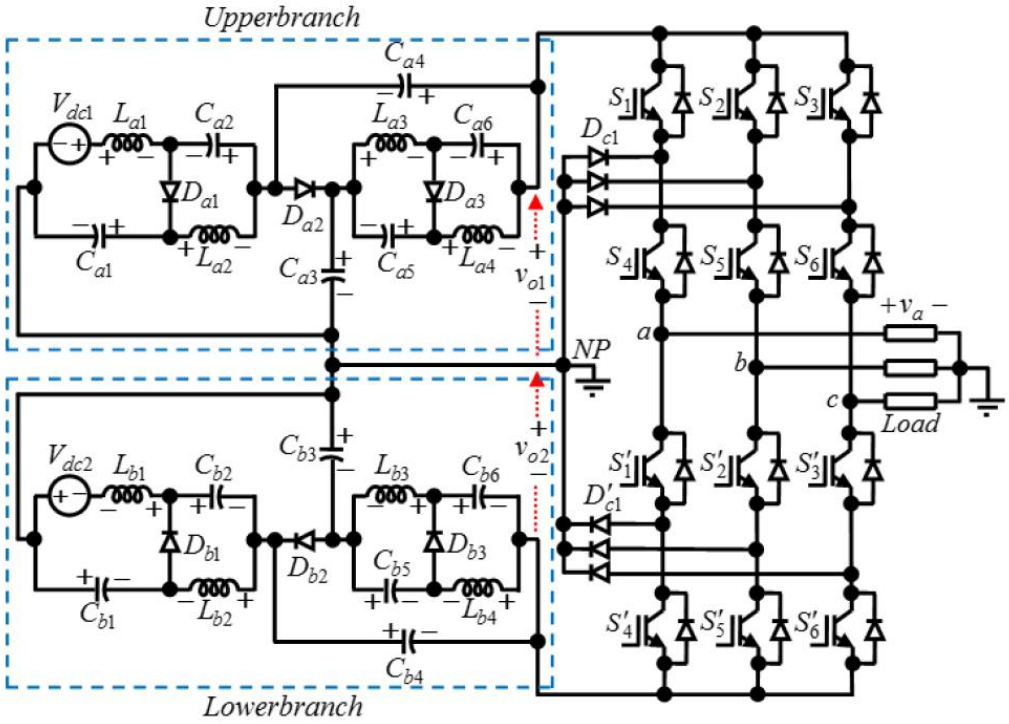


Figure 30
Quasi Z-source three-phase NPC inverter (Ahmadzadeh and Babaei, 2018)



In (Siwakoti 2018), the author present an active 5 levels NPC with minimum component quantity. The three-phase topology contains less number of semiconductor switches. All the phases share one dc voltage source and two capacitors, however each phase contains 1 capacitor, 4 power switches and 2 transistors. Figure 31 shows the three-phase structure whiles Figure 32 shows phase A of the same topology. The presented boost NPC topology is suitable for application in renewable energy systems, traction devices, fans and rolling mills.

Figure 31
6-levels three-phase active NPC (Siwakoti 2018)

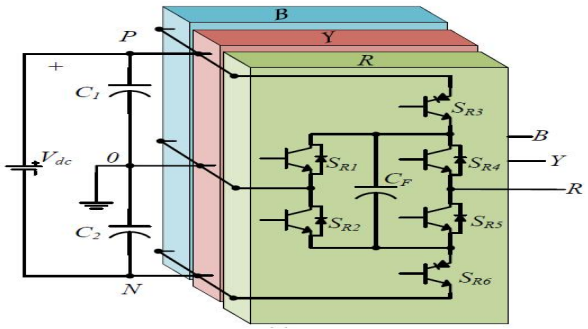
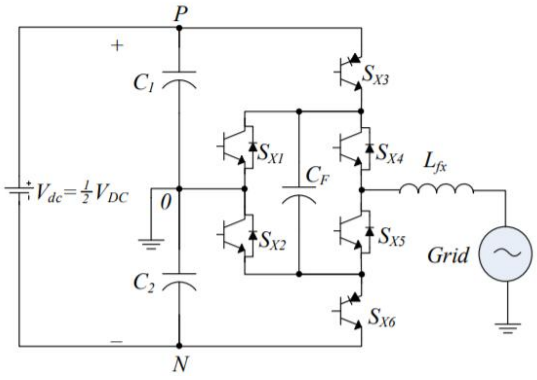


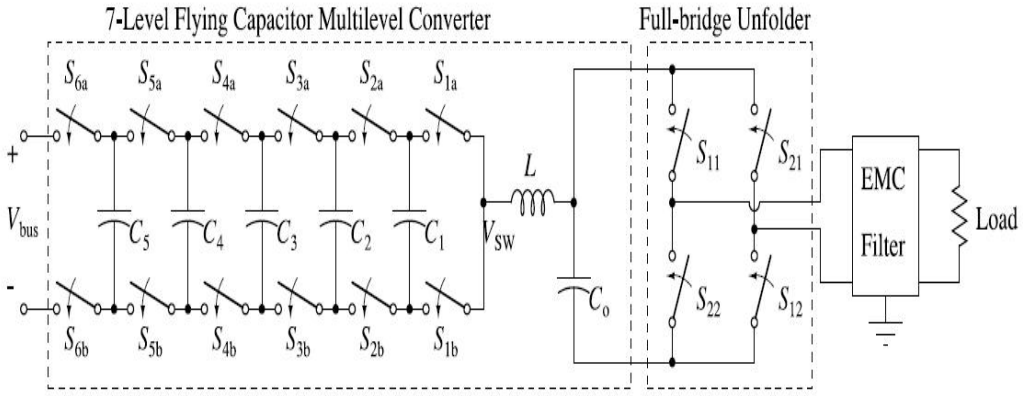
Figure 32
Single-phase active NPC inverter (Siwakoti 2018)



2.3.3 Flying Capacitor MLI Review

A high efficient and compact structure of flying capacitor MLI was presented by the authors in (Lei et al 2017). The presented topology is a single-phase which can generate 7-levels of load voltage. Due its positive characteristics, the presented FC MLI is suitable for renewable energy applications such as photovoltaic systems and electric vehicle charging systems. Figure 33 shows the power circuit of the presented FC topology. Double-line frequency power pulsating decoupling is achieved by the use of active buffer, as such the capacitance value is minimized as compared to other topologies. Lower voltage rated power switches are used in the presented topology and as such losses due to switching and conduction are minimized.

Figure 33
7-levels FC MLI (Lei et al 2017)



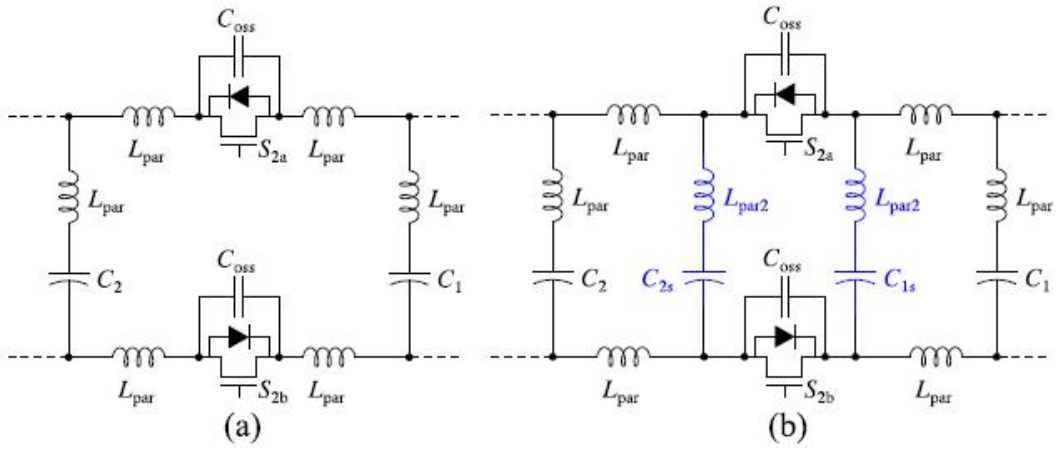
As depicted by Figure 33, the presented topology is composed of the FC structure coupled to an H-bridge inverter, the Fc structure contains sub units with

each unit having two switches and one capacitor. Parasitic inductance and coupling capacitor are introduced into the presented topology and illustrated by Figure 34. the capacitance C and inductor ripple current value Δi_L values are determined by equations (2.16) and (2.17) respectively.

$$C = \frac{I_{out,max}}{\Delta V_C f_{sw}(N-1)} \tag{2.16}$$

$$\Delta i_L = 0.25 \frac{V_{DC}}{f_{sw} L (N-1)^2} \tag{2.17}$$

Figure 34
7-levels FC inverter: a) without decoupling capacitors b) With coupling capacitors (Lei et al 2017)



A novel cascaded FC inverter with boosting functionality was presented by (Chen et al 2020). The presented FC cascaded topology is achieved by series connection of two flying capacitor units. The total capacitor count in the presented topology is reduced when compared to conventional FC topology, also the presented topology has boosting capabilities, a feature absent in traditional FC topology. Another interesting feature of the presented topology is self-voltage balancing capabilities of the capacitors i.e. no special control technique is required. Figure 35 and Figure 36 shows the three-phase and single-phase structures of the presented topology respectively. From the two structures, one dc source is shared by all phases, each phase has the following component count; 2 capacitors and 9 semiconductor switches.

Figure 35
Three-phase FC inverter (Chen et al 2020)

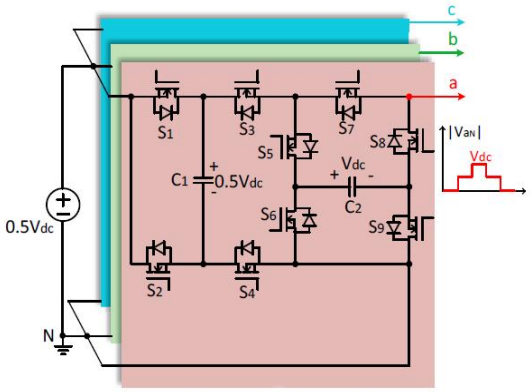
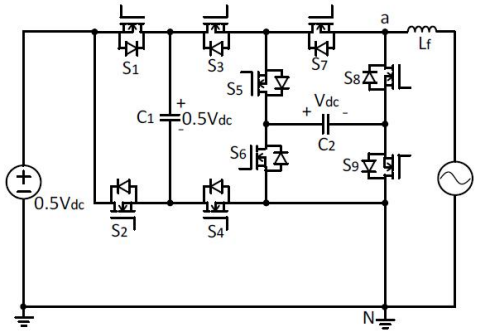


Figure 36
Single-phase FC inverter (Chen et al 2020)



The presented topology's voltage gain G is expressed below as:

$$G = \frac{V_{aN\_max}}{V_{in}} = \frac{V_{dc}}{1.5V_{dc}} = 2 \tag{2.18}$$

Where:

- V_{aN_max} is the peak ac voltage.
- V_{in} is the dc input voltage.

C2 capacitance is expressed below as:

$$C_2 \geq \frac{100M_{ac}[\cos(\omega t_2) - \cos(\omega t_1)]}{R\omega} \tag{2.19}$$

Where

- M_{ac} is the modulation.

- R is the load resistance.

Multilevel inverters undoubtedly play important roles in power sectors such as integration of renewable energy sources into grid and also application in industrial drive systems. MLI with less component quantity are more desirable because of the following advantages:

- Compact size
- Less component quantity
- Reduced cost
- Reduced size
- Minimum losses (switching and conduction)
- Higher efficiency

Based on the above merits, a new 7-levels three-phase multilevel inverter was presented in (Abhilash et al 2019). The presented topology is a combination of existing topologies to harness the advantages of these topologies. These topologies which put together forms the new FC topology are:

- VSI 2-levels inverter
- H-bridge inverter
- FC inverter

Figure 37 and Figure 38 shows the three-phase and single-phase structures of the presented FC multilevel inverter respectively. From the two structures, one dc source is shared by all phases, each phase has the following component count;2 capacitors and 9 semiconductor switches.

Figure 37
Three-phase FC multilevel inverter (Abhilash et al 2019)

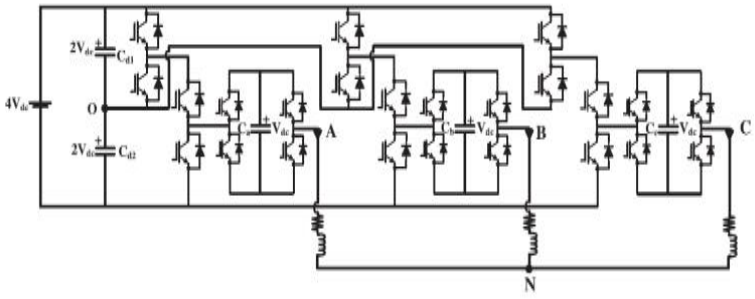
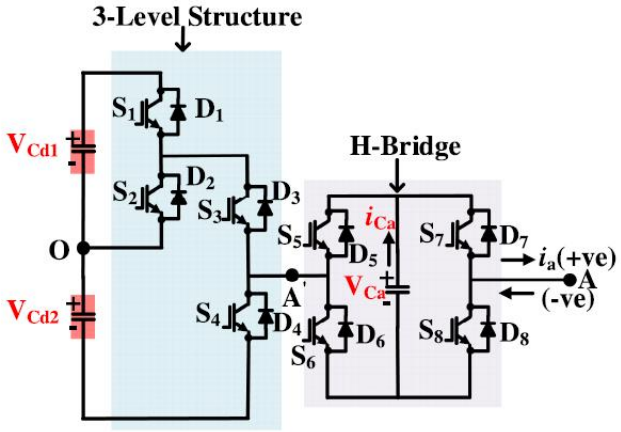


Figure 38
Single-phase FC inverter (Abhilash et al 2019)



2.4 Control Techniques of Multilevel Inverter

Using an appropriate control technique will significantly contribute to achieving the desired goal of having an efficient working converter. Several control schemes have been proposed by researchers and majority of these control techniques fall within the ambit of the popular method known as pulse width modulation (PWM) techniques. According to (Babaei et al 2007) and (Josh et al 2011), MI modulation techniques can be categorized into the following sub groups:

a. PWM techniques
b. Non-PWM techniques

Further categorization of these groups will be represented by Figure 39 and Figure 40. Figure 39 represents the MI modulation techniques proposed by (Babaei et al 2007) while Figure 40 shows the detailed classification of MI modulation techniques proposed by (Josh et al 2011). Both classifications similar but the proposed method of (Josh et al 2011) has more details and also it's made of two diagrams; Figure 40a and Figure 40b. Figure 40a shows MI modulation methods whiles Figure 40b shows Sinusoidal modulation methods (a subsidiary of Figure 40a).

Figure 39
MI Modulation classifications (Babaei et al 2007)

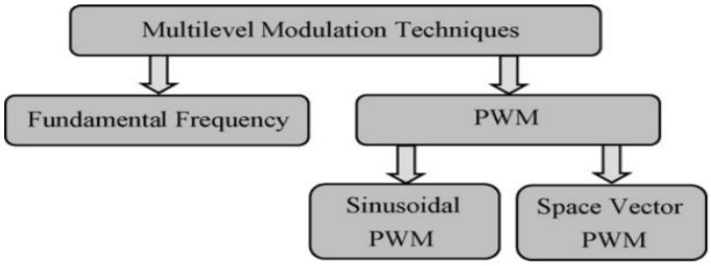
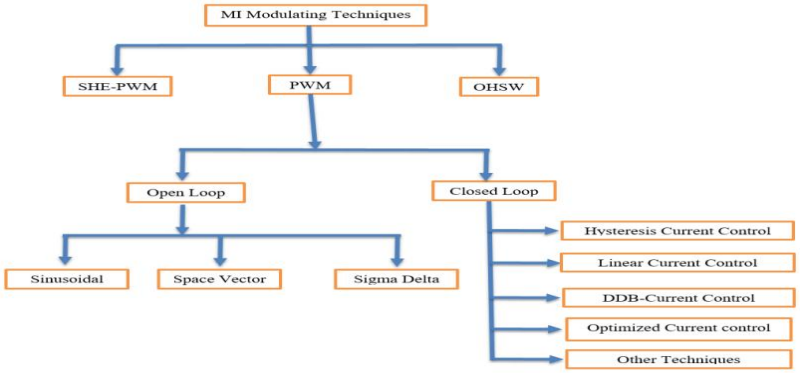
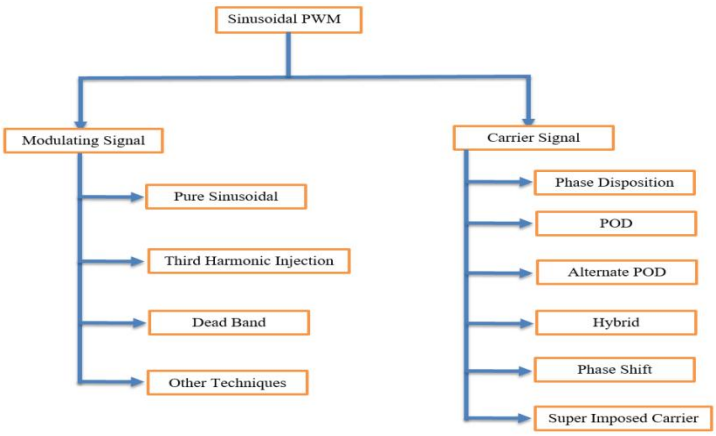


Figure 40
Classification of MI modulation techniques (Josh et al 2011)



(a) MI modulation techniques



(b) Sinusoidal PWM control techniques

The choice of PWM based control technique is heavily dependent on the desired output characteristics of the converter and also the performance and concept differences of the chosen PWM method, the cost of the chosen control method is also

an in important criteria in the selection of PWM methods. The following factors also affect the proper PWM control method selection:

a. Type of converter.
b. Power level.
c. Used semiconductor switches.

In (Holtz et al 1985), performance criteria of the various control methods which are offshoot PWM has been proposed, these criteria are used to determine the efficiency of the chosen PWM method, also these criteria will aid in the selection of the appropriate PWM control method.

a. Current Harmonics
b. Harmonic Spectrum
c. Torque harmonics
d. Switching frequency
e. Rule of polarity consistency
f. Dynamic performance

In categorization of PWM control methods are done according to feed-forward and feed-back schemes. In the feed-forward schemes, carrier-based and non-carrier based PWM techniques are explained. Examples of the feed-back schemes are Non-optimal techniques, current control in sub-oscillation mode etc. Analysis of the effects of the desired control method on the switches during turn-on and turn-off time is also investigated; switches possess different characteristics hence respond different during turn-on and turn-off periods. Factors which cause the differences in characteristics can be attributed to:

a. Semiconductor material type
b. Switch ratings
c. Electrode waveforms
d. Switching current
e. Device temperature

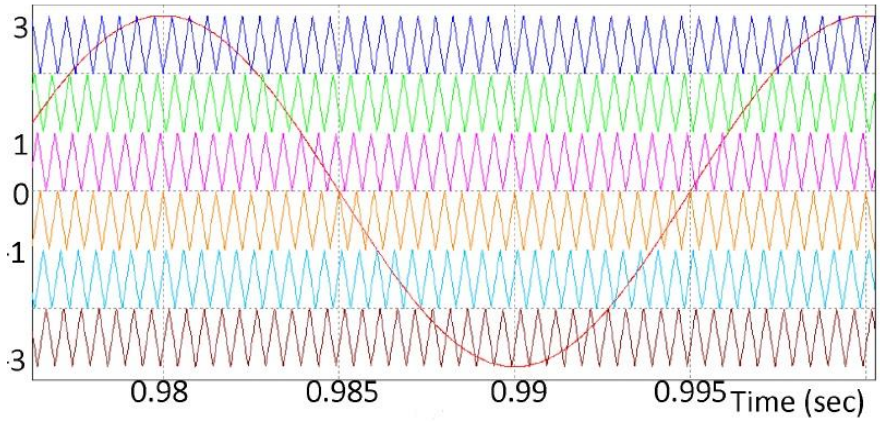
Multicarrier PWM technique which is an offshoot of Carrier based PWM method is mostly suitable for multilevel inverter applications (Calais et al 2001), hence has received more literature attention (Lai and Peng, 1996; Sinha and Lipo,

1997; Tolbertet al., 1999; Babaei et al., 2015; Hasan et al., 2018; Siwakoti, 2018; Siddique et al., 2019; Lee et al., 2020; Mhiesan et al., 2020). Two groups of multicarrier PWM exist;

a. Carrier Disposition method (CD)
b. Phase shifted method (PS)

However a third method known as hybrid method is derived from combination of the above two methods. The hybrid topology uses m-1 carries for m-step MI, also the various carriers have the same magnitude of frequency but shifted waveforms (Atkar et al., 2016). In terms of application, CD method is suitable for NPC converter whiles PS method is suitable for FC and cascaded MI topologies (Calais et al., 2001). The CD technique is also referred to as level shifted in Kanimozhi and Geetha, (2014) and McGrath (2002), and it's much preferred to the PS technique because the PS technique has a much higher THD. Carriers of the PS technique have same frequency and amplitude (peak-peak) (Atkar et al., 2016).

Figure 41
Hybrid Multicarrier PWM (Atkar et al., 2016).



To understand the various PWM control methods, the following basic parameters should be explained mathematically:

$$m_f = \frac{f_c}{f_o} \tag{2.20}$$

$$m_a = \frac{A_0}{A_{CPP}} \tag{2.21}$$

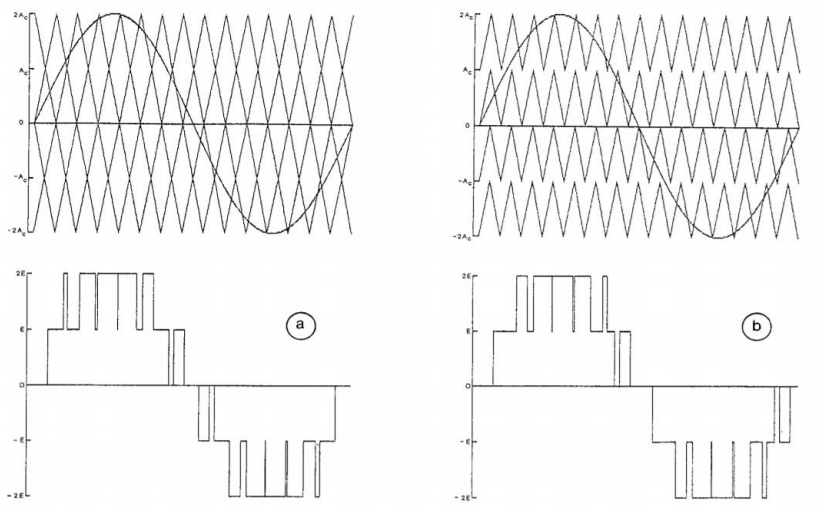
$$m_a = \frac{A_0}{4A_{CPP}} \tag{2.22}$$

From equation (2.20), m_f is the modulating frequency whiles f_c and f_o are the carrier signal frequency and reference signal frequency respectively. From equation (2.21) and (2.22), m_a is the amplitude modulation index, A_{cpp} is the maximum or peak value of the carrier signal and A_o is the reference signal's amplitude. Equation (2.21) is the m_a formula for PS method and equation (2.22) is the m_a formula for CD method (Calais et al., 2001). The carrier disposition method has the following sub-groups:

a. POD Technique
b. PD Technique
c. APOD Technique

Figure 42

Carrier Disposition modulation: a) APO b) PO (Calais et al., 2001)



In the PD method, there's phase alignment of all carrier signals whiles in the APOD method, there's a 180^0 phase shifting between individual carriers and adjoining carriers, however there's an out of phase of 180^0 between carries which are above and below the sinusoidal zero point (Chen et al., 2020). According to Siwakoti (2018), two methods of PWM techniques exist, namely; fundamental switching frequency and high switching frequency, the latter has the following sub categories of PWM:

a. SVP
b. SHE

c. SPWM

For multilevel inverter applications, the space vector technique is widely preferred because of its many advantages such ease to implement and its simplicity. Analysis of the various sub groups of the sinusoidal methodology are investigated. A new type of control scheme based on the PS method and known as dual reference PS-PWM and it's applied in a photovoltaic system based inverter having n-levels of output steps. For MI based higher power application purposes, the SHE technique is proposed in (Dahidah et al 2015) due its various minimum modulation methods, also SOPWM (synchronous optimal PWM) technique is applied in a cascaded topology having 9-steps of output voltage by (Rathore and Edpuganti 2015). One major disadvantage of the various control or modulation methods applied in MI can be attributed to a reduction in the modulation index or reference voltage which cause erosion of the voltage levels; a problem mostly experienced in variable speed control machines (Mahato et al., 2017). Two types of PWM techniques known as Depenbrock's Discontinuous method 1 and 3 are reviewed in (Rushiraj et al 2016). A novel control scheme based on Phase shifted SPWM technique in proposed in (Feng et al 2003); it's applied in resolving voltage balancing problems in FC converter.

Voltage control methods based on PWM techniques of single and three phase inverters is analyzed in (Muhammed and Rashid 2004). Examples of PWM based techniques suitable for voltage control of single phase converter (but not limited) are;

a. Single PWM
b. Multiple PWM
c. Sinusoidal PWM
d. Modified-Sinusoidal PWM
e. Phase-Displacement Control

The above-mentioned control techniques are mostly suitable for single phase converters; the most widely used technique amongst the above techniques for the control or regulation of voltage is the sinusoidal PWM however it has a number of disadvantages such as minimum primary (fundamental) voltage output. The following modulation techniques offers improved performance due to their advanced status: delta (Ziogas, 1981), trapezoidal (Ohnishi and Okitsu, 1983), harmonic

injection (Boost and Ziogas, 1988; Taniguchi and Irie, 1988), stair (Thorborg and Nystorm, 1988) and stepped (Ohsato et al., 1991; Salmon et al., 1991).

A three phase converter is an inverter with three output voltage waveforms phase shifted by 120^0. Most three phase converters are achieved by utilizing multiple single phase converters. Voltage regulation of a three phase converter can be achieved by control methods which are applied in the single phase converter however the following control techniques frequently used. The following PWM based control techniques are commonly applied in three phase inverter:

a. SVPWM
b. 600 PWM
c. Sinusoidal PWM
d. Third harmonic PWM

CHAPTER 3

Proposed Topology and Simulation Results

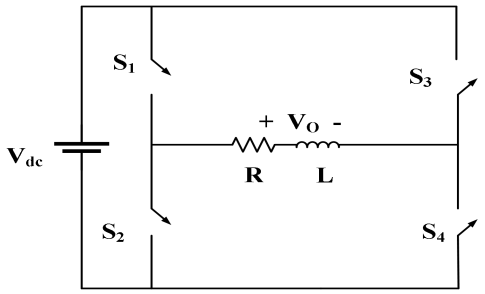
3.1 Introduction

This section presents a fully explained analysis of single-phase cascaded H-bridge multilevel inverters. As explained in previous chapters, it is classified into symmetric and asymmetric topologies. Comprehensive analysis based on mathematical computation and power circuit simulations are provided to confirm advantages and disadvantages of symmetric and asymmetric topologies. Firstly, simulation of conventional H-bridge inverter is provided since cascaded H-bridge MLI are founded on H-bridge inverter. Subsequently different simulation results of cascaded-bridge MLI are provided for symmetric and asymmetric topologies. Finally, attempts are made to simulate new terminologies of cascaded H-bridge MLI introduced by Prof Ebrahim Babaei during MSc lecture known as modelling and design of power electronic converters. These new terms are semi-symmetric and semi-asymmetric.

3.2 H-Bridge MLI

Figure 43 shows the power diagram of conventional H-bridge inverter. The circuit composes of four unidirectional power switches, one voltage source and an RL load. The switching system shown in Table 5 is used to create the required output voltage levels through a sinusoidal pulse width modulation approach.. H-bridge inverters generally are able to generate only 3-levels of output voltage i.e. one positive level, zero level and one negative level.

Figure 43
H-bridge inverter



The concept of sinusoidal PWM technique just as all conventional PWM techniques requires reference and carrier signals. In case of sinusoidal PWM, the reference and carrier's signals are sine signal and triangular signals respectively. The two signals are plotted on the same plane with equal frequency but varying amplitudes. The carrier signal has higher amplitude compared to the reference signal. Figure 44 shows concept of sinusoidal PWM technique. The crossing point of the sine wave creates various intervals which are used in generating the gate signals. For each interval, reference and carrier signals are compared, if reference signal is observed to be bigger than carrier signal, maximum output voltage is generated for this interval. However, if the reference signal is lower to carrier signal, zero output voltage is generated for such interval. Maximum positive voltage is generated for positive half-cycle whiles maximum negative voltage is generated for negative half-cycle.

Figure 44
Sinusoidal PWM

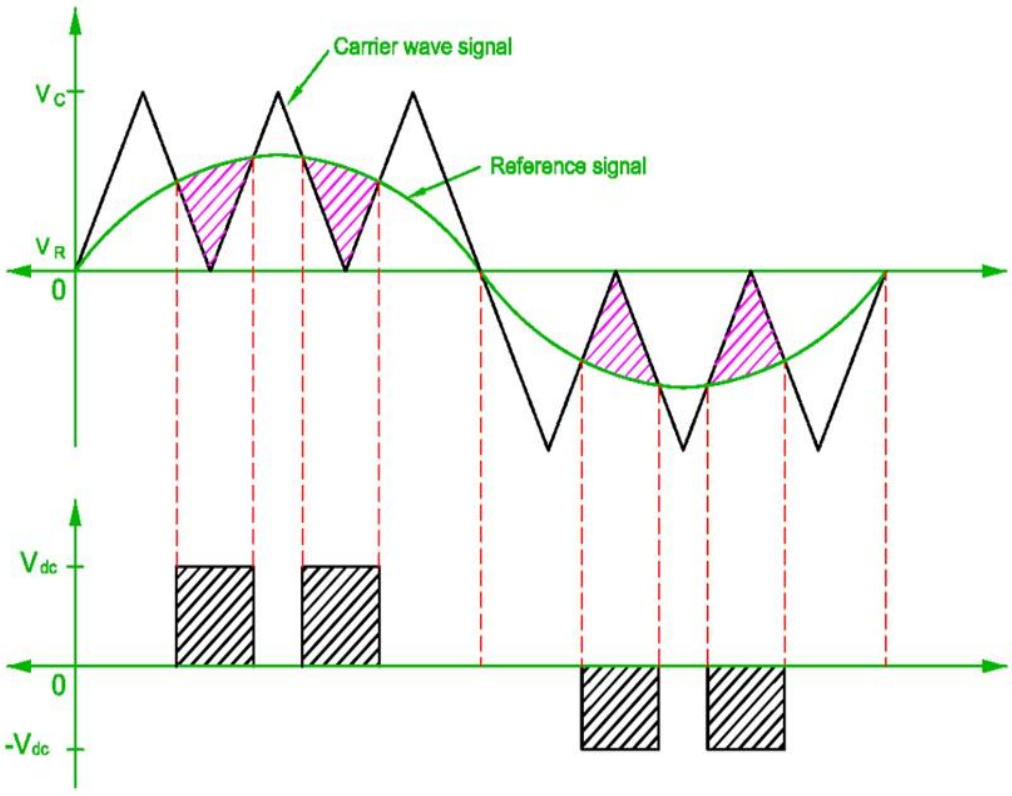


Table 5 shows the switching scheme of H-bridge inverters. Three states of operation are required to generate the 3-levels of output voltage. With an input of V_{dc} as shown by Figure 43, the possible output voltages that can be generated are $+V_{dc}$, $0V_{dc}$ and –

V_{dc}. Transverse switching will produce positive or negative output voltages ie turning on switches S_1S_4 generates positive output voltage, likewise turning-on switches S_2S_3 generates negative output voltage. Zero output voltage is generated from two different switching mechanism, turning-on switches S_1S_3 or S_2S_4 will generate zero output voltage, all these switching schemes are illustrated by Table 5.

Table 5
H-bridge inverter switching

STATE	SWITCHES				OUTPUT VOLTAGE (V_O)
	S_1	S_2	S_3	S_4	
I	1	0	0	1	V_{dc}
II	0	1	1	0	$-V_{dc}$
	1	0	1	0	
III	0	1	0	1	0

Table 6 lists the system parameters utilised in the simulation of Figure 43's H-bridge inverter. PSCAD was used to model the internal power circuit of the above H-bridge inverter using the characteristics listed in Table 6. Figure 45 to Figure 48 show the generated output waveforms. Figure 45 depicts the waveforms of the reference and carrier signals. Figure 46 shows that with a 400V input voltage, the resultant load voltage is exactly 400V, proving that the switching sequence in Table 5 is correct. Figure 47 shows that the load current is around 80A. Figure 48 depicts the FFT of the mentioned inverter output voltage; the lowest harmonics of the inverter voltage are approximately zero. The voltage THD is smaller than 3%

Table 6
Simulation Parameters

Parameter	Symbol	Magnitude
Carrier frequency	f_c	700Hz
Reference amplitude	A_r	0.7
Inductance	L	0.01mH

Resistance	R	2 Ω
DC-link voltage source	V_{dc}	0.4kV

Figure 45
Carrier and reference output voltage waveform

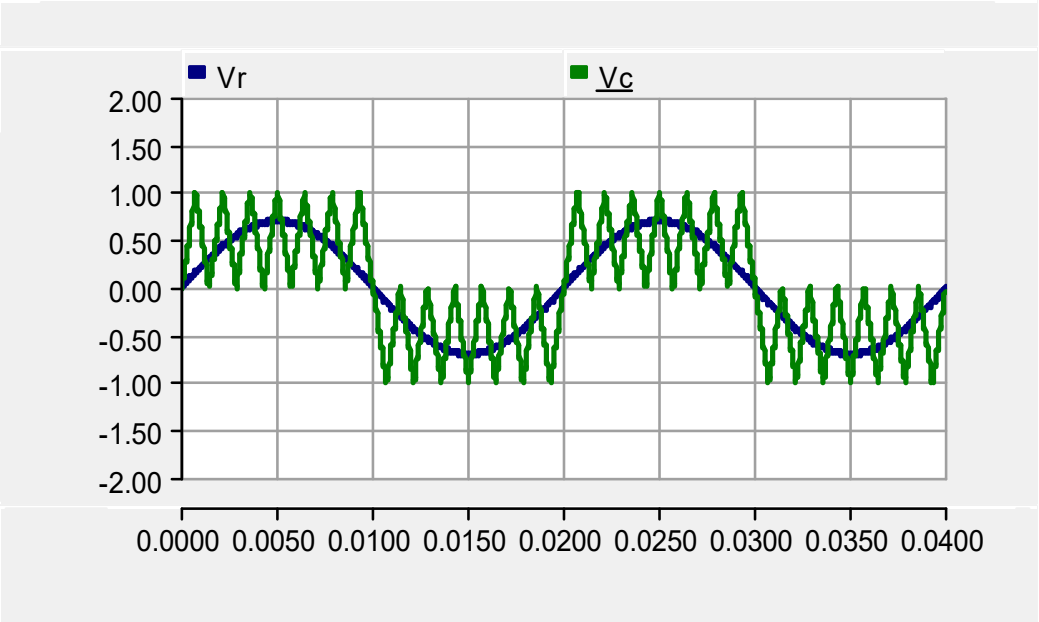


Figure 46
Load voltage waveform

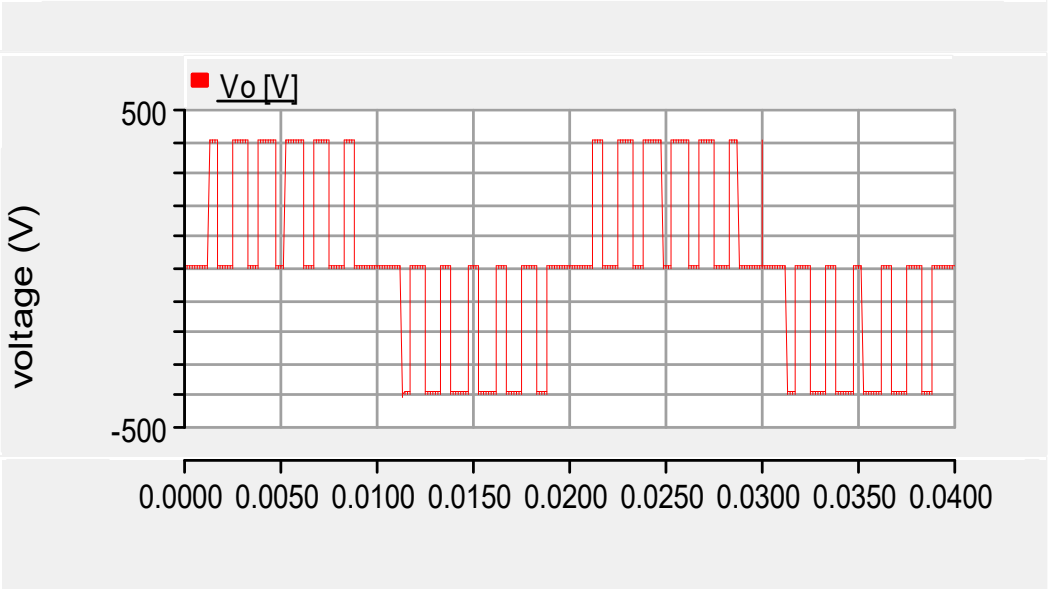


Figure 47
Load current waveform

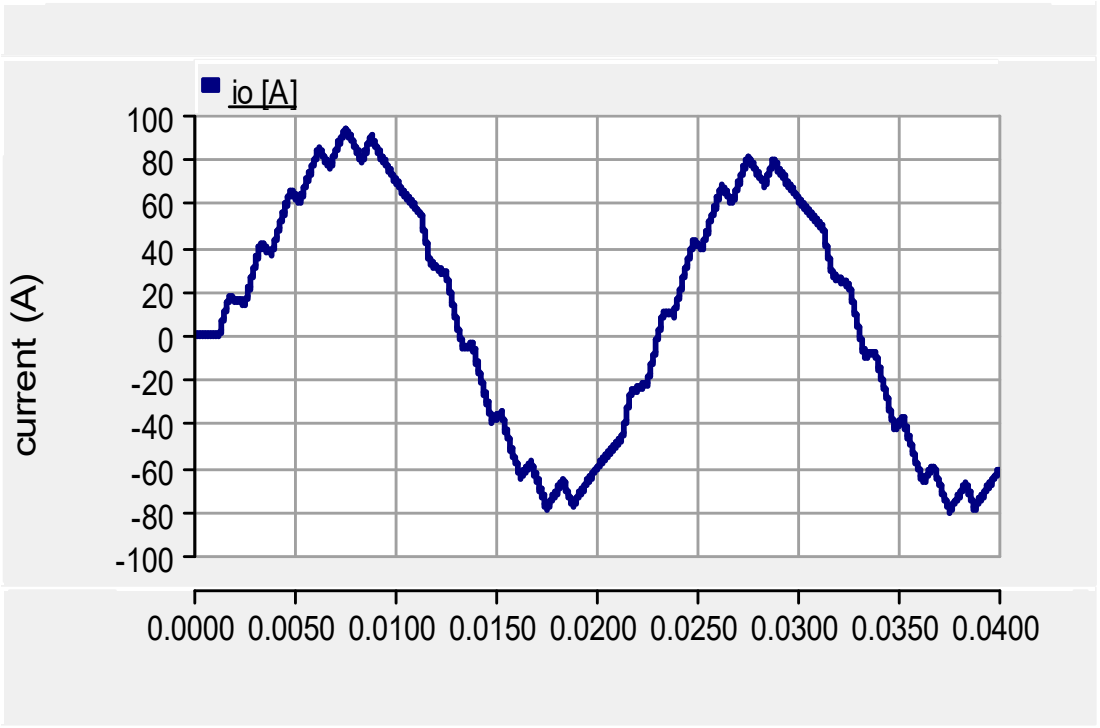
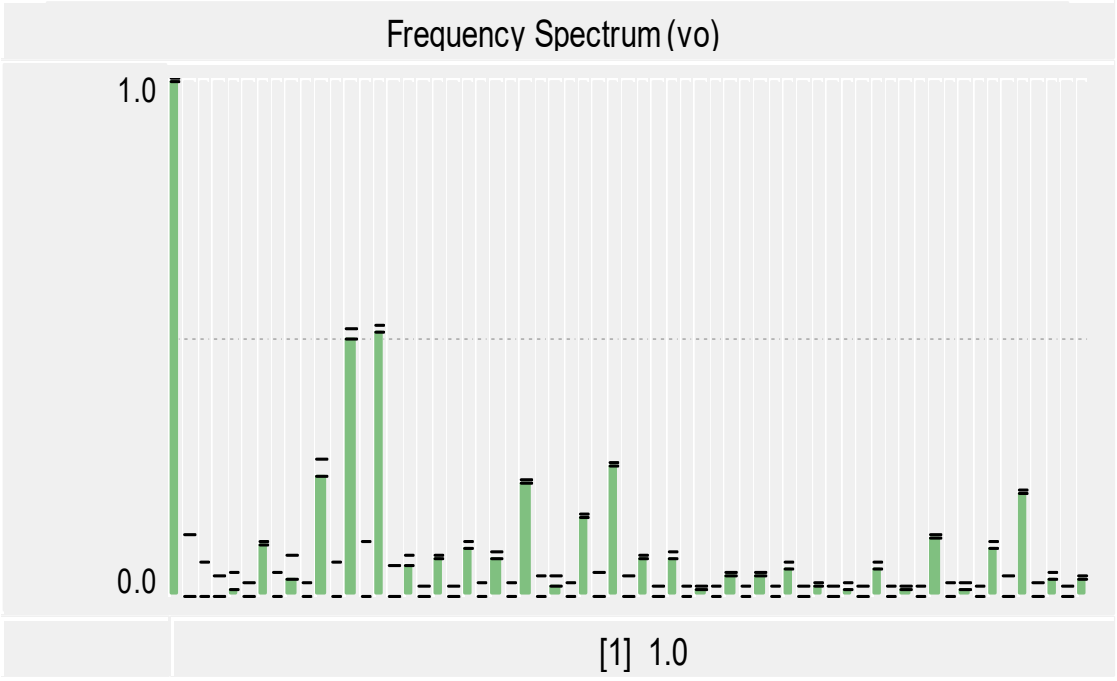


Figure 48
FFT waveform



3.3 Cascaded H-Bridge Multilevel Inverter.

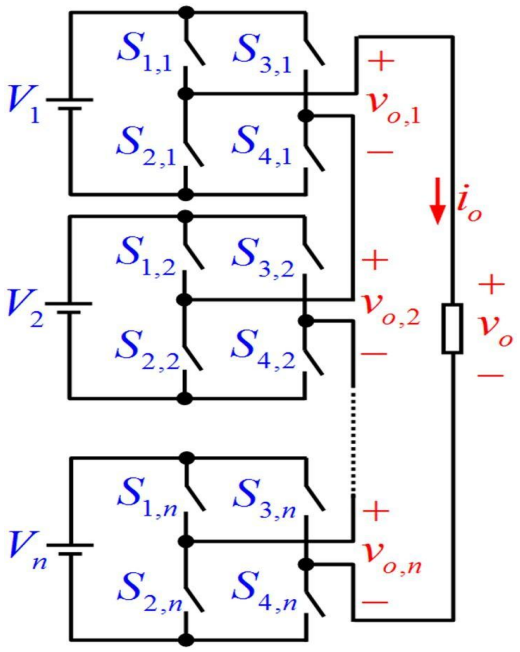
This section simulates varieties of cascaded H-bridge multilevel inverter topologies.it is important to note that simulated topologies here are single-phased and use various H-bridge inverter modules. Cascaded H-bridge MLIs are classified into symmetric and asymmetric topologies, as detailed in earlier chapters. For these two types of the inverters, simulation waveforms are shown.

A generalised structure for a single-phase cascaded H-bridge inverter is presented in Figure 49. Because it is a generalised structure, the number of H-bridge units in the structure is represented by n. The generalised structure will have symmetric and asymmetric topologies if the input voltage sources are equal and unequal.

To exhibit theoretical relationship between symmetric and asymmetric MLI topologies for the generalized structure of Figure 49, equation (3.1) to equation (3.12) are provided to produce the general computations of relevant parameters such as load voltage levels, component quantity (dc source, driver circuit, IGBT etc.) for symmetric and asymmetric topologies when two units of H-bridge inverters are used in the cascaded structure. Therefore, the equivalent inverter structure is the same as that of Figure 50.

Figure 49

Cascaded MLI with n H-bridge units



For symmetric topologies with two units of H-bridges, the input voltages are expressed as:

$$V_1 = V_2 = V_3 = V_n = V_{dc} \tag{3.1}$$

The output voltage level is determined by:

$$N_{step} = 2n + 1 \tag{3.2}$$

The switch, driver circuit and IGBT quantity are determined by:

$$N_{S,D,I} = 4n \tag{3.3}$$

The peak output voltage is determined by:

$$V_{o,peak} = nV_{dc} \tag{3.4}$$

Using the same figure of Figure 49, the following expressions are provided for binary topology of asymmetric MLI with two units of H-bridges. The input voltages are related by:

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \end{cases} \tag{3.5}$$

The levels of output voltage are determined by:

$$N_{step} = 2^{n+1} - 1 \tag{3.6}$$

The switch, driver circuit and IGBT quantity are determined by:

$$N_{S,D,I} = 4n \tag{3.7}$$

The peak output voltage is determined by:

$$V_{o,peak} = (2^n - 1)V_{dc} \tag{3.8}$$

Using the same figure of Figure 49, the following expressions are provided for trinary topology of asymmetric MLI with two units of H-bridges. The input voltages are related by:

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 3V_{dc} \\ V_3 = 9V_{dc} \end{cases} \tag{3.9}$$

The output voltage outputs are determined by:

$$N_{step} = 3^n \tag{3.10}$$

The switch, driver circuit and IGBT quantity are determined by:

$$N_{S,D,I} = 4n \tag{3.11}$$

The peak output voltage is determined by:

$$V_{o,peak} = \left(\frac{3^n - 1}{2}\right) V_{dc} \tag{3.12}$$

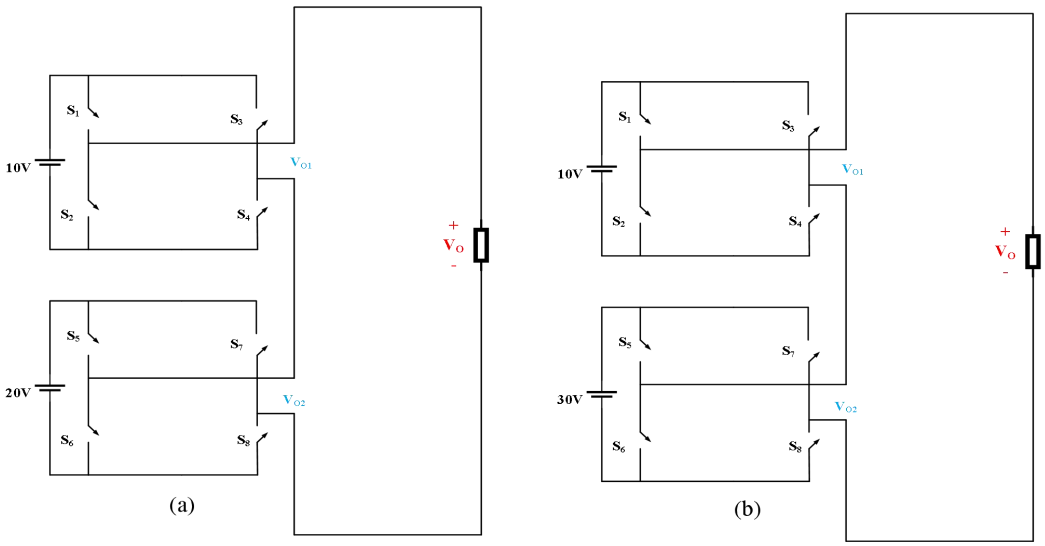
Figure 50 shows the power circuit of two units of H-bridge inverter constituting an asymmetric multilevel inverter. Asymmetric multilevel inverters are grouped into binary and trinary topologies. The major difference in these topologies is the nature of the magnitude of input voltage. The mathematical expressions below differentiate the binary topology from trinary topology.

The input voltage of the binary and trinary topologies for Figure 50 is expressed by equations (3.13) and (3.14) respectively.

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_{dc} \end{cases} \tag{3.13}$$

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 3V_{dc} \end{cases} \tag{3.14}$$

Figure 50
Single-phase cascaded MLI



From equations (3.13) and (3.14) above, if $V_{dc} = 10V$, then the input voltages for Figure 50 for binary and trinary topologies of cascaded H-bridge multilevel is given by equations (3.15) and (3.16) respectively.

$$\begin{cases} V_1 = 10V \\ V_2 = 20V \end{cases} \tag{3.15}$$

$$\begin{cases} V_1 = 10V \\ V_2 = 30V \end{cases} \tag{3.16}$$

Table 7 shows the switching pattern for binary and trinary topologies. As shown by the Table 7, trinary topologies are able to generate more levels of load voltage even-though the power circuit of the inverter does not change i.e. binary and trinary have similar topology but differ in input voltage magnitudes.

Table 7
Switching pattern of symmetric and asymmetric MLI

STATE	SWITCHES S	S	S	S	S	S	OUTPUT VOLTAGE
BINARY ASYMMETRIC CASCADED H-BRIDGE MLI							
I	0	0	1	1	0	1	10V
II	0	1	0	1	0	0	20V
III	0	0	1	1	0	0	30V
IV	1	0	1	0	1	0	0
V	1	1	0	1	0	1	-10V
VI	0	1	0	0	1	1	-20V
VII	1	1	0	0	1	1	-30V
TRINARY ASYMMETRIC CASCADED H-BRIDGE MLI							
I	0	0	1	1	0	1	10V
II	1	1	0	1	0	0	20V
III	1	0	1	1	0	0	30V
IV	0	0	1	1	0	0	40V
V	1	0	1	0	1	0	0
VI	1	1	0	0	1	0	-10V
VII	0	0	1	0	1	1	-20V
VIII	0	1	0	0	1	1	-30V
IX	1	1	0	0	1	1	-40V

The load output waveforms of binary and trinary topology of Figure 50 are illustrated by Figure 51 and Figure 52. As shown by the waveforms, the binary topology generates 7-levels of load voltage using input voltage magnitudes expressed by equation (3.15) while trinary topology generates 9-levels of load voltage using input voltage magnitude expressed by equation (3.16).

Figure 51
Binary topology output waveform

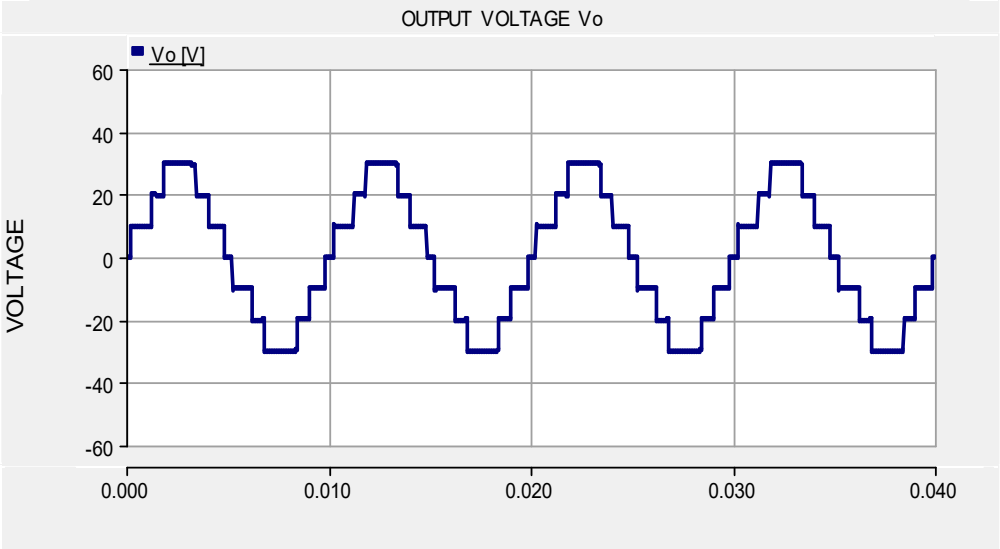


Figure 52
Trinary topology output waveform

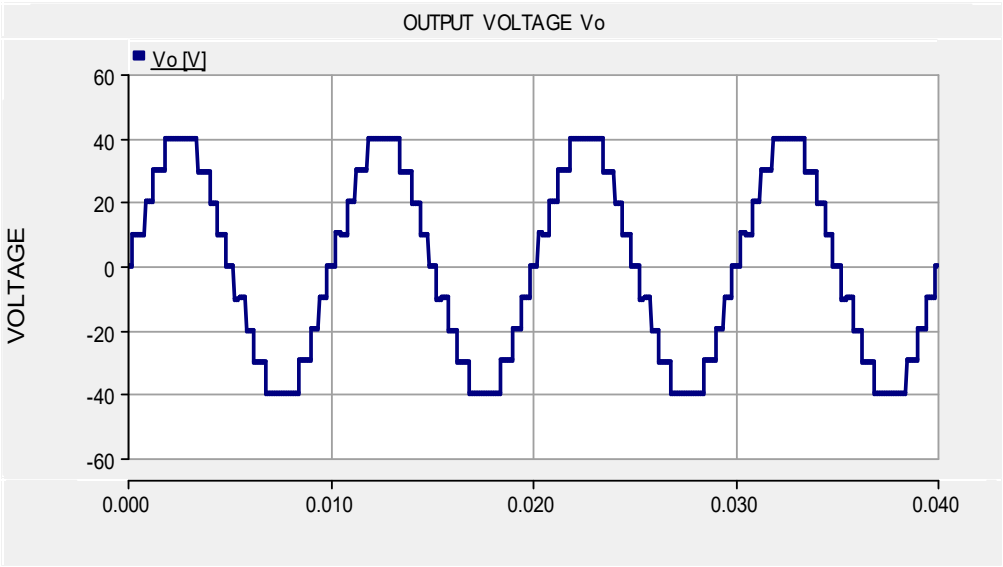


Figure 53 shows symmetric multilevel inverter structure with 10V input voltage magnitude and Figure 54 depicts symmetric load voltage waveform generated after simulation accordingly. With two units of H-bridge inverter, symmetric MLI can generate 5-levels of load voltage; this is validated by Figure 54 which is the simulation output waveform. Increasing the units of H-bridge inverter will increase the levels of load voltage.

Figure 53
Symmetric multilevel inverter

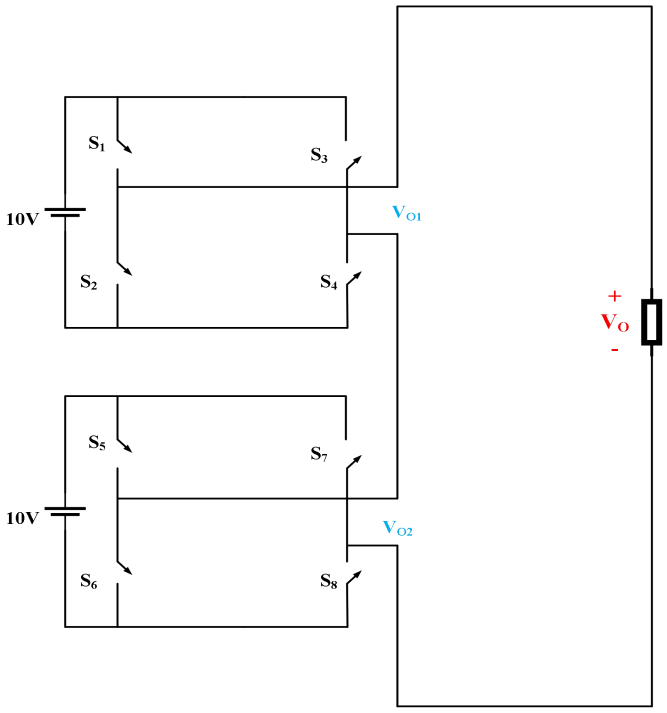
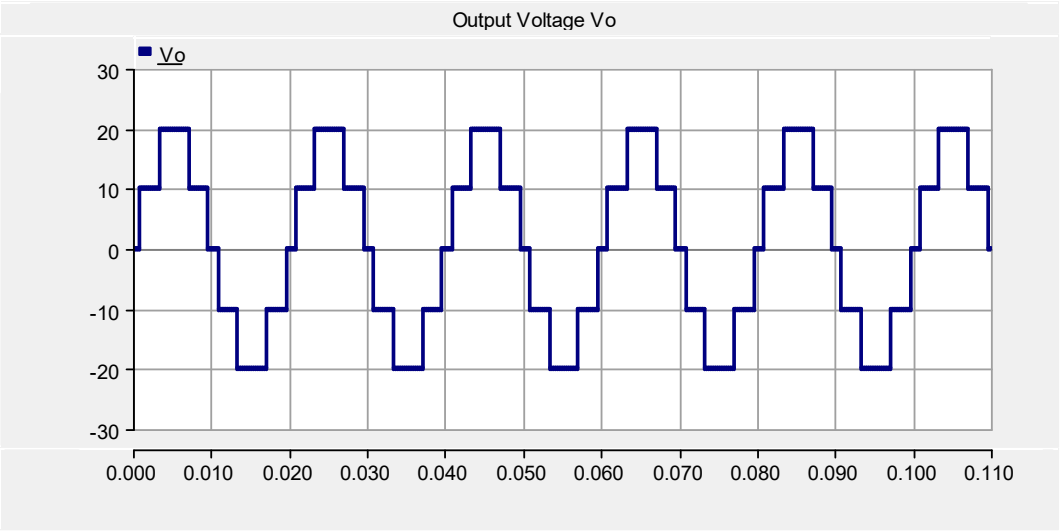


Figure 54
Symmetric topology output waveform



For the symmetric topology to generate levels equivalent to the binary topology of Figure 51, its cascaded structure will require three units of H-bridge inverter. This means that, binary topology will utilize two units of H-bridge while symmetric topology will utilize three units of H-bridge to generate equivalent load voltage levels. Figure 55 shows the symmetric structure with three H-bridge units and its output waveform is depicted by Figure 56. As shown by the waveforms of Figure 50 and Figure 55, binary topology of two units of H-bridge generates equivalent waveform as symmetric topology of three units of H-bridge.

Figure 55
Symmetric multilevel inverter

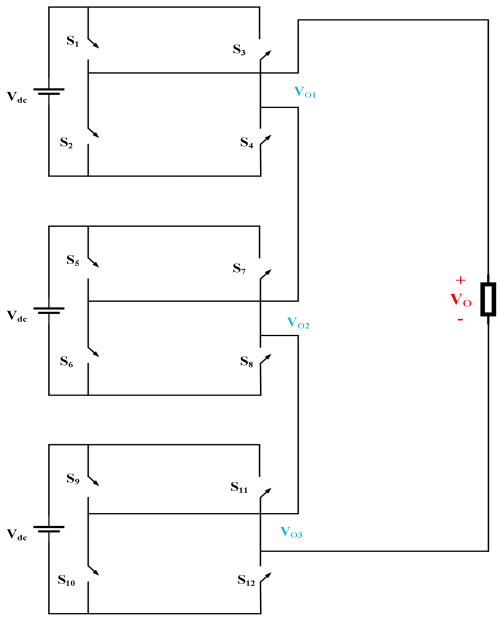
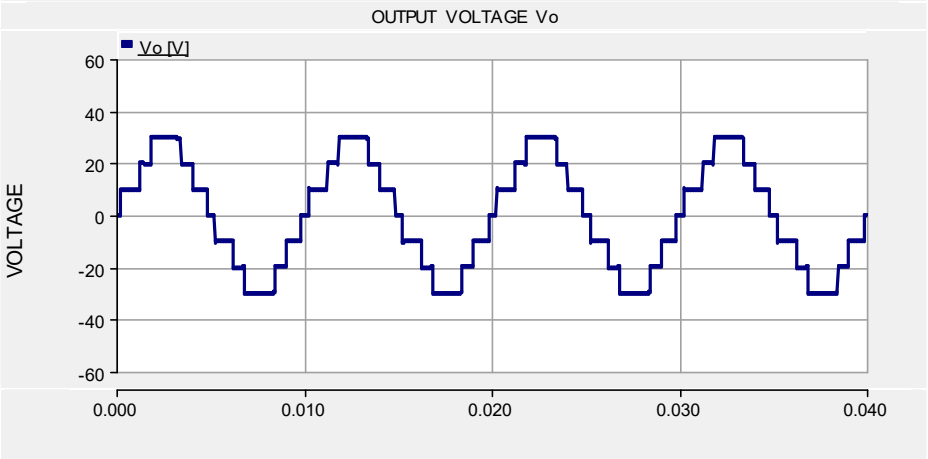


Figure 56
Symmetric topology output waveform



It's evident from the above results that, cascaded H-bridge multilevel inverters utilize two or multiple units of H-bridge inverters to generate higher levels of output voltages. Symmetric and asymmetric topologies were investigated theoretically and by simulations. Results of both investigation shows that asymmetric cascaded H-bridge inverters utilize less number of H-bridges but generates the highest levels of output voltage when compared symmetric topology.

3.4 Proposed Cascaded Multilevel Inverter

Figure 57 depicts the components of my proposed cascaded single-phase multilevel inverter. The Figure 57a comprises of one DC input source and two uni-directional power switches. By adding, one DC source and one switch to the circuit of Figure 57a will enable the new circuit of Figure 57b to generate positive and negative output voltages. Both dc sources should be equal in magnitude. Figure 58 shows the sub multilevel structures. It is derived by series connection of two basic units. The components of Figure 5a are two direct current supplies and four uni-directional controls, while components of Figure 58b include four direct current supplies and six uni-directional controls. If n represent each basic unit of Figure 57, then the structures of Figure 58 are composed of $2n$ accordingly. Figure 57a generates 1-level of positive output voltage while Figure 57b generates 3-levels of $(+V_1, 0, -V_2)$ output voltages. Figure 58a generates 3-levels of positive output voltages and whereas 5-level of both positive and negative output voltages are generated in Figure 58b.

The topologies of Figure 57a and Figure 58a require an H-bridge structure to generate negative output voltages. With respect to n, the dc source count and switch count for Figure 57a and Figure 58a are expressed by equations (3.17) and (3.18) respectively, where Q_{VDC} and Q_{SW} represent the quantity of dc sources and switches accordingly. Figure 59 shows various cascaded topologies using the sub multilevel of Figure 57a. Each cascaded topology of Figure 59 generates only positive stepped output voltages. Figure 59a and Figure 59c generates 15-levels and 63-levels of positive stepped output voltages if asymmetric input voltages are utilized. Theoretical output waveform of my proposed positive 15-level MLI inverter is represented by Figure 60.

For $n = 2$

$$\begin{cases} Q_{Vdc} = n \\ Q_{SW} = 2n \end{cases} \quad (3.17)$$

For n =1

$$\begin{cases} Q_{Vdc} = n \\ Q_{SW} = n \end{cases} \quad (3.18)$$

Figure 57
Basic units of the proposed MLI

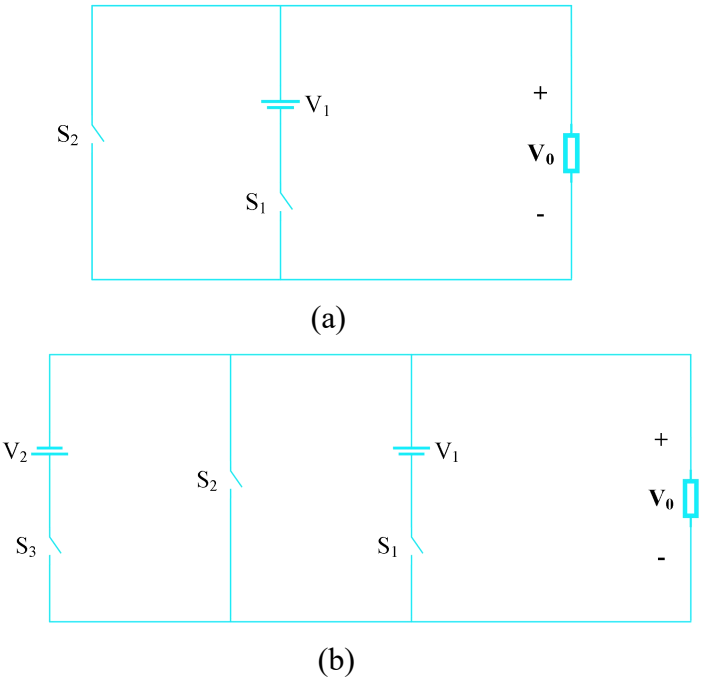


Figure 58
Sub-multilevel inverter topologies

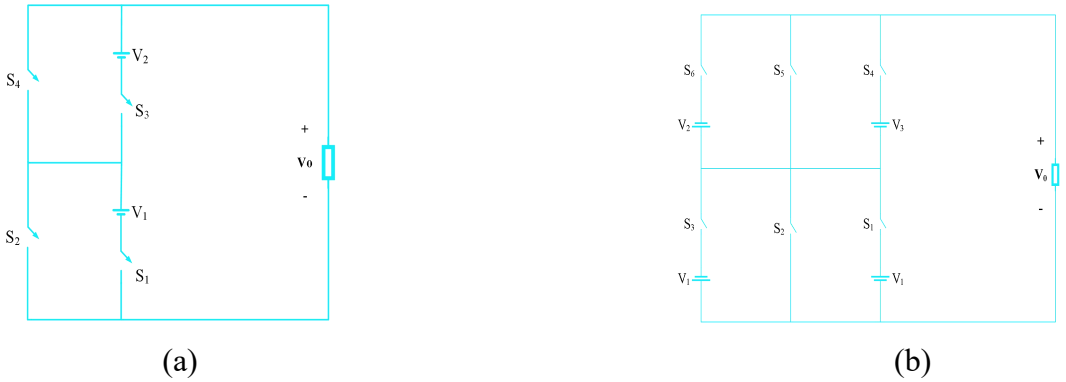


Figure 59
Various cascaded structures of the proposed inverter

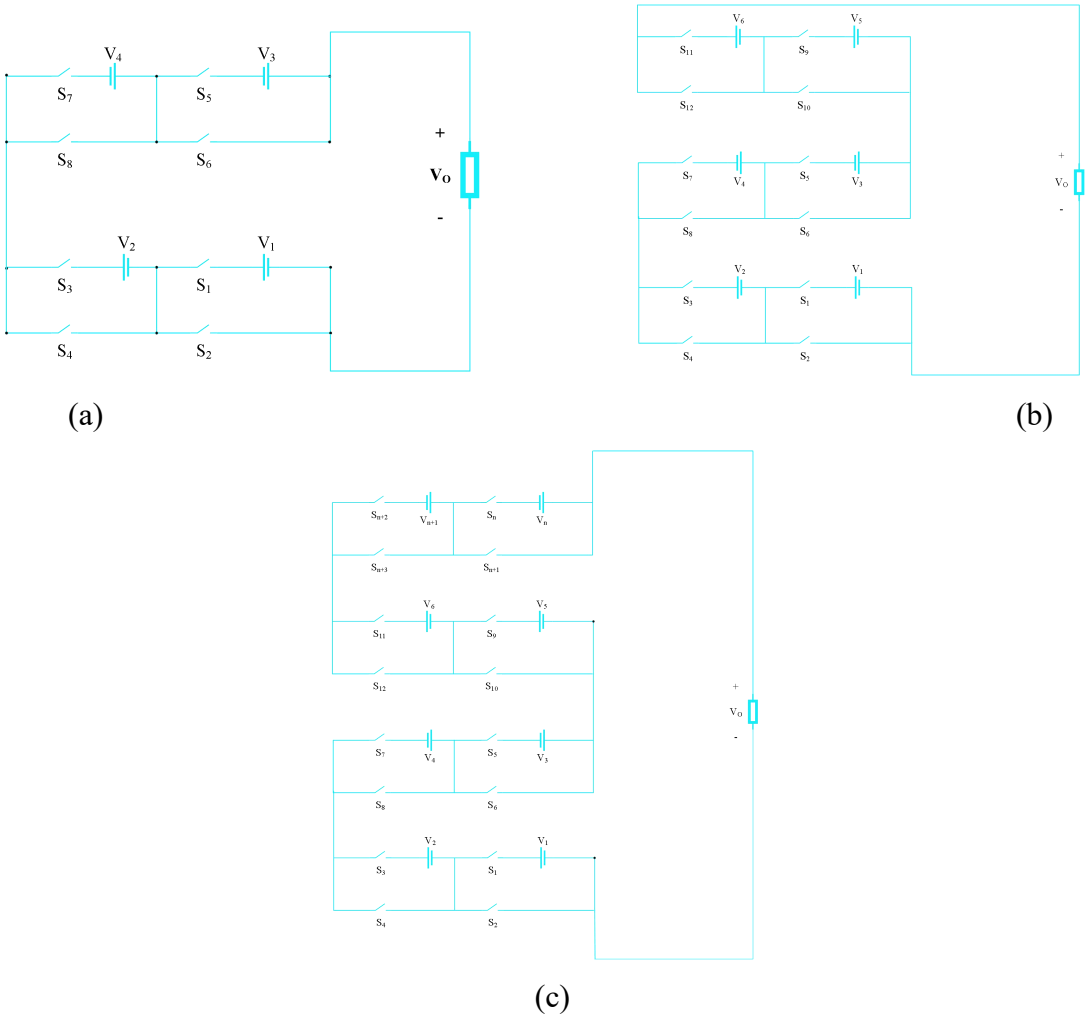
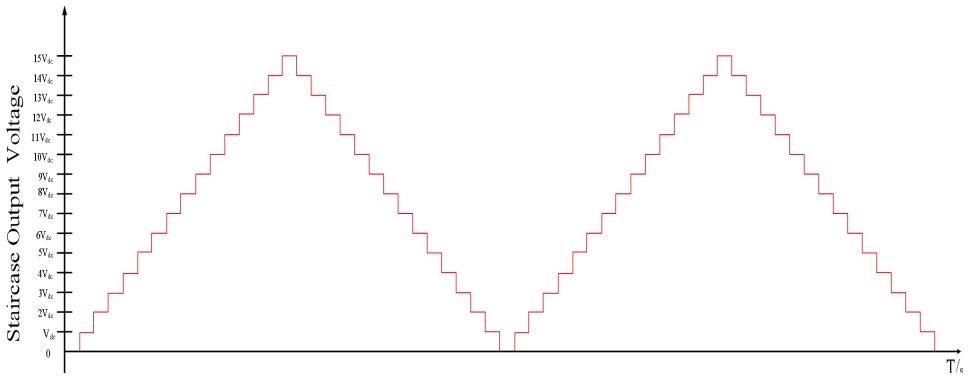


Figure 60
Positive 15-level waveform of proposed inverter



3.4.1 Magnitude of DC Sources

Cascaded multilevel inverters are classified either as symmetric or asymmetric based on the magnitude of the dc sources. All direct current supplies have the same magnitude in symmetric topologies, however direct current supplies magnitude varies in asymmetric topologies. With equal number of basic units in their cascaded structures, asymmetric topologies produce higher levels of output voltage compared to symmetric topologies. Based on the above characteristics, symmetric and asymmetric computation of the dc sources is provided below. It should be emphasised that symmetric and asymmetric analyses are only possible when there are several dc sources.

3.4.1.1 Symmetric DC Sources

Considering Figure 58, 3-levels and 5-levels of output voltage can be formed by Figure 58a and Figure 58b when magnitudes of input voltages are equal (symmetric characteristic). Let *n* represent the number of basic units in a given structure such as Figure 58a, therefore $V_{o,n,max}$ (maximum output voltage/ output maximum voltage) is expressed as:

For *n* = 2, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_{dc} \\ V_{o,2,max} = V_1 + V_2 = 2V_{dc} \end{cases} \quad (3.19)$$

For *n* = 3, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_{dc} \\ V_{o,3,max} = V_1 + V_2 + V_3 = 3V_{dc} \end{cases} \quad (3.20)$$

For *n* = 4, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_{dc} \\ V_{o,4,max} = V_1 + V_2 + V_3 + V_4 = 4V_{dc} \end{cases} \quad (3.21)$$

For *n* = 5, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_5 = V_{dc} \\ V_{o,5,max} = V_1 + V_2 + V_3 + V_4 + V_5 = 5V_{dc} \end{cases} \quad (3.22)$$

For *n* = 6, the maximum output voltage is computed by:

$$\begin{cases} \mathrm{V_1 = V_2 = V_3 = V_4 = V_5 = V_6 = V_{dc}} \\ \mathrm{V_{o,6,max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 6V_{dc}} \end{cases} \quad (3.23)$$

As a result, the suggested MLI symmetric maximum output supply voltage is represented as

$$V_{o,max} = nV_{dc} \quad (3.24)$$

Similarly, The suggested MLI output voltage values for symmetric dc input sources are computed as:

For *n* = 2, the maximum output voltage level is computed by:

$$\begin{cases} \mathrm{V_1 = V_2 = V_{dc}} \\ \mathrm{V_{o,2,max} = V_1 + V_2 = 2V_{dc}} \\ \mathrm{N_{LEVEL} = n + 1 (if\ n = 2, N_{LEVEL} = 2 + 1 = 3\ i.e.\ 0V, V_{dc}, 2V_{dc}} \end{cases} \quad (3.25)$$

For *n* = 3, the maximum output voltage level is computed by:

$$\begin{cases} \mathrm{V_1 = V_2 = V_3 = V_{dc}} \\ \mathrm{V_{o,3,max} = V_1 + V_2 + V_3 = 3V_{dc}} \\ \mathrm{N_{LEVEL} = n + 1 = 4 - Levels} \end{cases} \quad (3.26)$$

For *n* = 4, the maximum output voltage level is computed by:

$$\begin{cases} \mathrm{V_1 = V_2 = V_3 = V_4 = V_{dc}} \\ \mathrm{V_{o,4,max} = V_1 + V_2 + V_3 + V_4 = 4V_{dc}} \\ \mathrm{N_{LEVEL} = n + 1 = 5 - Levels} \end{cases} \quad (3.27)$$

For *n* = 5, the maximum output voltage level is computed by:

$$\begin{cases} \mathrm{V_1 = V_2 = V_3 = V_4 = V_5 = V_{dc}} \\ \mathrm{V_{o,5,max} = V_1 + V_2 + V_3 + V_4 + V_5 = 5V_{dc}} \\ \mathrm{N_{LEVEL} = n + 1 = 6 - Levels} \end{cases} \quad (3.28)$$

For *n* = 6, the maximum output voltage level is computed by:

$$\begin{cases} \mathrm{V_1 = V_2 = V_3 = V_4 = V_5 = V_6 = V_{dc}} \\ \mathrm{V_{o,6,max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 6V_{dc}} \\ \mathrm{N_{LEVEL} = n + 1 = 7 - Levels} \end{cases} \quad (3.29)$$

3.4.1.2 Asymmetric DC Sources

Variation in direct current supplies magnitude indicates an asymmetric feature of the direct current supplies. Both binary or trinary computation is possible in asymmetric dc magnitude computation, the latter produces more output levels compared to binary topologies. Considering Figure 58, if the magnitudes of input voltages are unequal (asymmetric characteristic) then 4-levels and 7-levels of output voltages will be generated by Figure 58a and Figure 58b respectively. Let *n* represent the number of basic units in a given structure such as Figure 58a, therefore expressed below is $V_{o,n,max}$ (the highest output supply voltage or output maximum voltage) as:

For *n* = 2, highest output voltage or maximum outgoing voltage is computed as:

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_{dc} \\ V_{o,2,max} = V_1 + V_2 = 3V_{dc} \end{cases} \tag{3.30}$$

For *n* = 3, the maximum output voltage is computed as:

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_{o,3,max} = V_1 + V_2 + V_3 = 6V_{dc} \end{cases} \tag{3.31}$$

Again, for *n* = 3, the maximum output voltage is computed as:

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_{o,3,max} = V_1 + V_2 + V_3 = 7V_{dc} \end{cases} \tag{3.32}$$

For *n* = 4, the maximum output voltage is computed as:

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_{o,4,max} = V_1 + V_2 + V_3 + V_4 = 8V_{dc} \end{cases} \tag{3.33}$$

Again, for *n* = 4, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ \mathrm{V_{o,4,max} = V_1 + V_2 + V_3 + V_4 = 15V_{dc}} \end{cases} \tag{3.34}$$

For n = 5, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ \mathrm{V_{o,5,max} = V_1 + V_2 + V_3 + V_4 + V_5 = 15V_{dc}} \end{cases} \tag{3.35}$$

Again, for n = 5, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ \mathrm{V_{o,5,max} = V_1 + V_2 + V_3 + V_4 + V_5 = 31V_{dc}} \end{cases} \tag{3.36}$$

For n = 6, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ V_6 = 6V_{dc} \\ \mathrm{V_{o,6,max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 21V_{dc}} \end{cases} \tag{3.37}$$

Again, for n = 6, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ V_6 = 32V_{dc} \\ \mathrm{V_{o,6,max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 63V_{dc}} \end{cases} \tag{3.38}$$

Similarly, the output voltage levels for asymmetric dc sources of the proposed MLI are expressed by:

For n = 2, the maximum output voltage level is computed thus:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ \mathrm{V_{o,2,max} = V_1 + V_2 = 3V_{dc}} \\ \mathrm{N_{LEVEL} = 2n\ (if\ n = 2, N_{LEVEL} = 2(2) = 4\ i.e.\ 0V, V_{dc}, 2V_{dc}, 3V_{dc}} \end{cases} \quad (3.39)$$

For n = 3, the maximum output voltage level is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 3V_{dc} \\ \mathrm{V_{o,3,max} = V_1 + V_2 + V_3 = 6V_{dc}} \\ \mathrm{N_{LEVEL} = 2n} \end{cases} \quad (3.40)$$

Again, for n = 3, the maximum output voltage level is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 4V_{dc} \\ \mathrm{V_{o,3,max} = V_1 + V_2 + V_3 = 7V_{dc}} \\ \mathrm{N_{LEVEL} = 2n + 1} \end{cases} \quad (3.41)$$

For n = 4, the maximum output voltage level is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ \mathrm{V_{o,4,max} = V_1 + V_2 + V_3 + V_4 = 8V_{dc}} \\ \mathrm{N_{LEVEL} = 2n + 0} \end{cases} \quad (3.42)$$

Again, for n = 4, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ \mathrm{V_{o,4,max} = V_1 + V_2 + V_3 + V_4 = 15V_{dc}} \\ \mathrm{N_{LEVEL} = 3n + 3} \end{cases} \quad (3.43)$$

For n = 5, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ \mathrm{V_{o,5,max} = V_1 + V_2 + V_3 + V_4 + V_5 = 15V_{dc}} \\ \mathrm{N_{LEVEL} = 3n + 0} \end{cases} \tag{3.44}$$

Again, for n = 5, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ \mathrm{V_{o,5,max} = V_1 + V_2 + V_3 + V_4 + V_5 = 31V_{dc}} \\ \mathrm{N_{LEVEL} = 6n + 1} \end{cases} \tag{3.45}$$

For n = 6, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ V_6 = 6V_{dc} \\ \mathrm{V_{o,6,max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 21V_{dc}} \\ \mathrm{N_{LEVEL} = 3n + 3} \end{cases} \tag{3.46}$$

Again, for n = 6, the maximum output voltage for binary asymmetric structure is computed as:

$$\begin{cases} \mathrm{V_1 = V_{dc}} \\ \mathrm{V_2 = 2V_{dc}} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ V_6 = 32V_{dc} \\ \mathrm{V_{o,6,max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 63V_{dc}} \\ \mathrm{N_{LEVEL} = 10n + 3} \end{cases} \tag{3.47}$$

Based on the symmetric and asymmetric analysis of the strength of the dc sources shown above, it is clear that the newly proposed single-phase topology, which consists of fewer power switches and dc sources, has reduced inverter size and volume. Figure 59a depicts the suggested inverter architecture, which includes eight unidirectional controllers and four (4) direct current supplies. To generate 15 levels of positive stepped output voltages, the fundamental frequency modulation approach is used. Table 8 shows the switching sequences in Figure 59a. During the 15th state, switches S1, S3, S5, S7 conduct while the remaining switches stay in blocking mode, generating a positive voltage of 15Vdc. The noted output voltage of the 14th state is positive In this condition, 14Vdc is present, and S1, S2, S3, and S4 are active.

The conducting switches in the 13th state are S1, S2, S3, and S4, whereas the remaining switches are non-conducting, resulting in positive 13Vdc. The conducting switches S1, S2, S3, and S4 create positive 12Vdc in the 12th state, while the remaining switches are in blocking mode. The active switches in the 11th state are S1, S2, S3, and S4, which provide a positive voltage of 11Vdc. The conducting switches that create 10Vdc in the tenth state are S1, S2, S3, and S4. S1, S2, S3, and S4 are active switches in the 9th state that provide 9Vdc positive voltage. S1, S2, S3, and S4 are the conducting switches in the eighth state, and positive 8Vdc is created. During the 7^{th} state positive $7V_{dc}$ voltage is generated by the following active switches.

Table 8

Switching Pattern

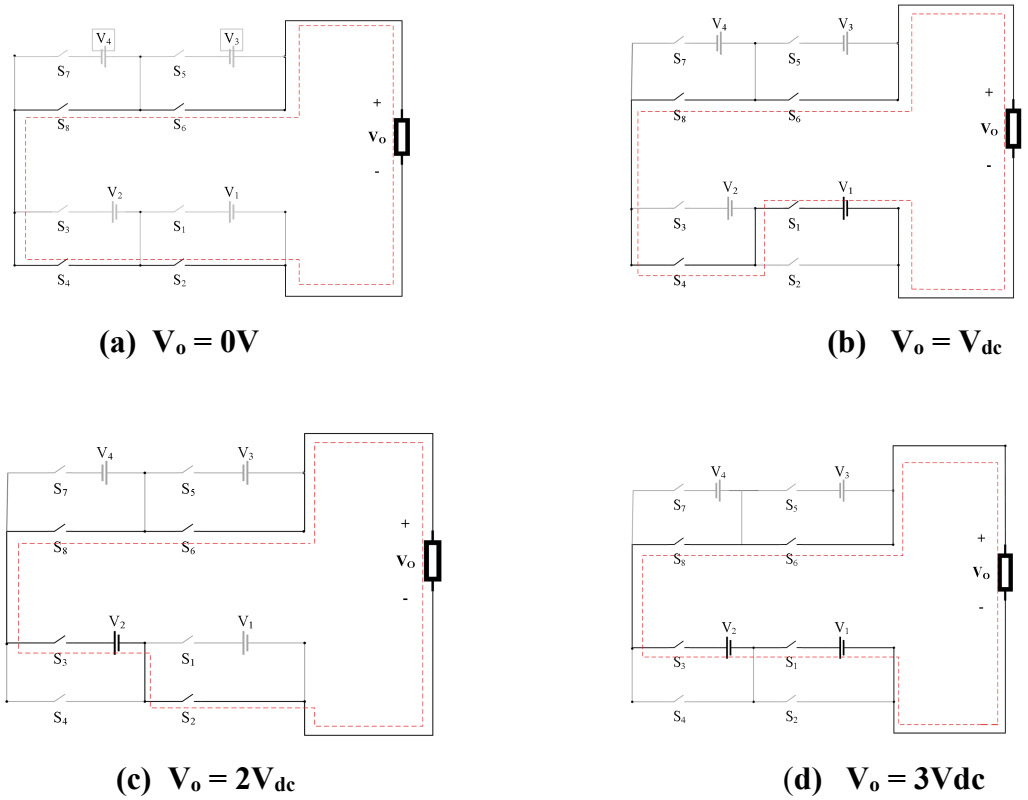
State	Switches	DC Sources	Output Voltage V_O
1	S_1, S_4, S_6 and S_8	V_1	V_{dc}
2	S_3, S_2, S_6 and S_8	V_2	$2V_{dc}$
3	S_1, S_3, S_6 and S_8	$V_1 + V_2$	$3V_{dc}$
4	S_2, S_4, S_5 and S_8	V_3	$4V_{dc}$
5	S_4, S_1, S_5 and S_8	$V_1 + V_3$	$5V_{dc}$
6	S_2, S_3, S_5 and S_8	$V_2 + V_3$	$6V_{dc}$
7	S_1, S_3, S_5 and S_8	$V_1 + V_2 + V_3$	$7V_{dc}$
8	S_2, S_4, S_6 and S_7	V_4	$8V_{dc}$
9	S_1, S_4, S_6 and S_7	$V_1 + V_4$	$9V_{dc}$
10	S_2, S_3, S_6 and S_7	$V_2 + V_4$	$10V_{dc}$

11	S_1, S_3, S_6 and S_7	$V_1 + V_2 + V_4$	$11V_{dc}$
12	S_2, S_2, S_5 and S_7	$V_3 + V_4$	$12V_{dc}$
13	S_1, S_4, S_5 and S_7	$V_1 + V_3 + V_4$	$13V_{dc}$
14	S_2, S_3, S_5 and S_7	$V_2 + V_3 + V_4$	$14V_{dc}$
15	S_1, S_3, S_5 and S_7	$V_1 + V_2 + V_3 + V_4$	$15V_{dc}$
16	S_2, S_4, S_6 and S_8	-	

In state 6 (6th state), $6V_{dc}$ is generated by the active S_1, S_2, S_3 and S_4 controls whiles the remaining switches are in blocking state. During the 5th state, the active controls are S_1, S_2, S_3 as well as S_4 and the produced voltage is $5V_{dc}$. In state 4 (4th state), conducting switches are S_1, S_2, S_3 including S_4 and generated voltage output is $4V_{dc}$. In state 3 (3rd state), conducting switches S_1 to S_4 generated voltage $3V_{dc}$. At 2nd state, conducting switches S_1 to S_4 produced voltage $2V_{dc}$ and finally 1st state produces 0 voltages when the following switches S_1, S_2, S_3 with S_4 are active. These various states of switching are illustrated by Figure 61a to Figure 61p and Table 8 shows the switching pattern of the inverter for positive stepped output voltages.

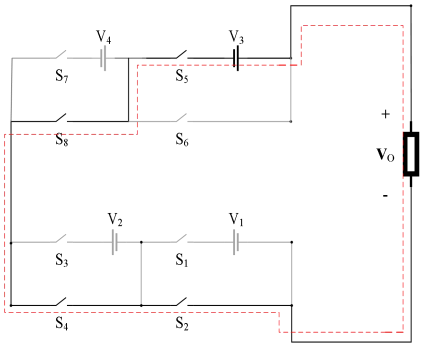
Figure 61

Switching states of proposed positive 16-level inverter

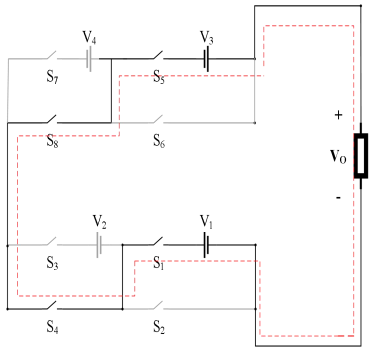


(a) $V_o = 0V$ **(b) $V_o = V_{dc}$**

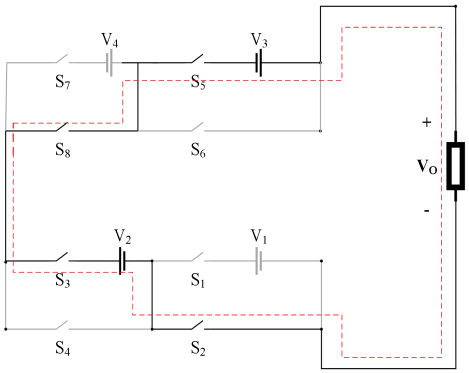
(c) $V_o = 2V_{dc}$ **(d) $V_o = 3Vdc$**



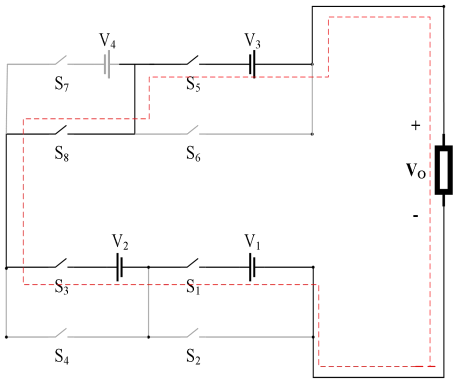
(e) $V_o = 4V_{dc}$



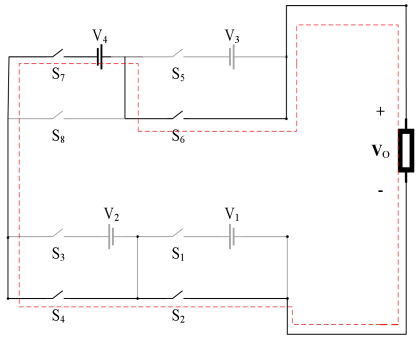
(f) $V_o = 5V_{dc}$



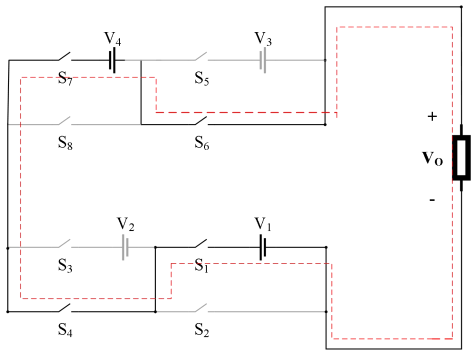
(g) $V_o = 6V_{dc}$



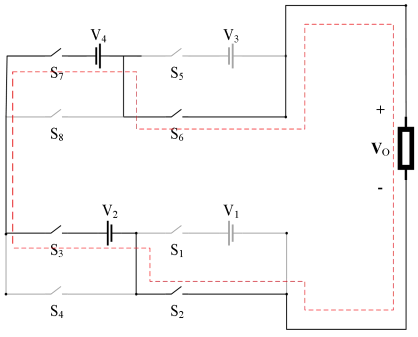
(h) $V_0 = 7V_{dc}$



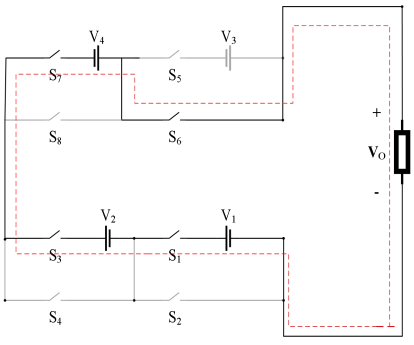
(i) $V_0 = 8V_{dc}$



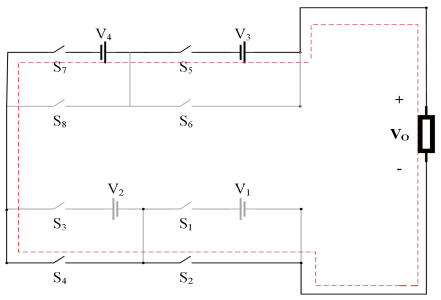
(j) $V_0 = 9V_{dc}$



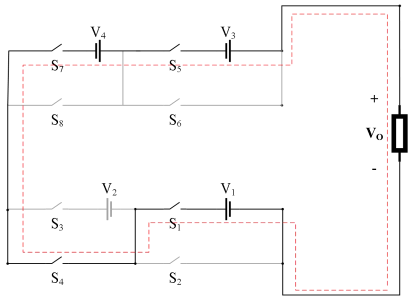
(k) $V_o = 10V_{dc}$



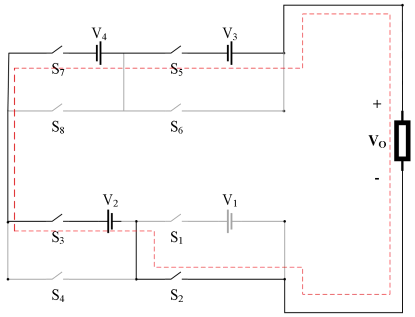
(l) $V_o = 11V_{dc}$



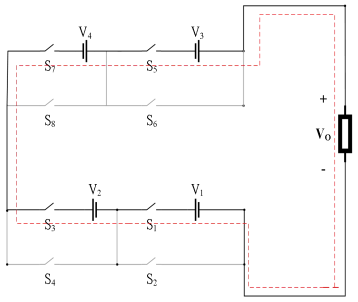
(m) $V_o = 12V_{dc}$



(n) $V_o = 13V_{dc}$



(o) $V_o = 14V_{dc}$



(p) $V_o = 15V_{dc}$

3.5 Proposed cascaded 31-level MLI

Figure 62

Proposed cascaded 31-level MLI

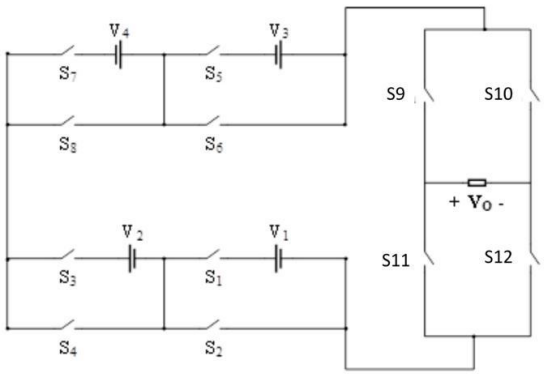


Figure 62 show the power circuit of the proposed cascaded 31-level single phase asymmetrical MLI. The proposed asymmetrical MLI is derived by cascading two submultilevel units of Figure 58a. Incorporating an H-bridge structure will enable the generation of positive and negative stepped output voltages. The component count for the proposed 31-level inverter are four dc sources, twelve

unidirectional switches and twelve driver circuits. The output voltage level count and component quantities are computed by equations (17) to equations (20). Again, let n represent the number of basic units in the cascaded structure.

3.5.1. Inverter Losses

Three factors define the total energy losses experienced by the postulated configuration: switching power losses, power losses in a transformer, power losses in blocking voltage, and due to conduction. During operating modes of the inverter, switching losses occur, while conduction losses occur during the conducting phase of the switches.

3.5.2. Switching losses

All semiconductor power switches experienced switching losses in both the on and off states. Energy lost during the on and off states of the postulated multilayer inverter serves as the terms used to represent the switching losses. In this study we denote these two states by the symbols E_{on} and E_{off}. P_{SW} provides the overall switching energy losses. Before and after a switch is activated I and I' currents are measured. In its off position, a switch has a voltage of V_{sw}. Both the on and off times are indicated by the symbols t_{on} and t_{off}.

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} \left[\left(\frac{I'}{t_{on}} t \right) \left(-\frac{V_{sw,k}}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{sw,k} I' t_{on} \tag{3.48}$$

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} \left[\left(\frac{V_{sw,k}}{t_{off}} \right) \left(-\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt = \frac{1}{6} V_{sw,k} I t_{off} \tag{3.49}$$

$$P_{SW} = f_s \sum_{k=1}^{N_{switch}} \left(\sum_{i-1}^{N_{on,k}} Eon,k + \sum_{i=1}^{N_{off,k}} E_{off,k} \right) \tag{3.50}$$

3.5.3. Conduction Losses

During the on-state of a semiconductor switch, conduction losses occur. Components such as transistor and antiparallel connected diode constitute the control switch of the proposed inverter. Summation of the total losses of power of the transistors and the diodes ($P_{C,T}$) and ($P_{C,D}$) respectively defines the conduction power losses (P_C). β value is dependent on the type of semiconductor switch employed and it's a constant value provided by the manufacturer. Transistor and diodes resistance

are presented as R_T and R_D respectively and their related voltages as V_T and V_D respectively.

$$P_{C,T}(t)=(V_T+R_T i^{\beta}(t))i(t)$$
$$P_{C,T}=\frac{1}{2\pi}\int_0^{2\pi} n_T(t)[V_T+R_T i^{\beta}(t))i(t)]d(\omega t) \quad (3.51)$$

$$P_{C,D}(t)=(V_D+R_D i(t))i(t)$$
$$P_{C,D}=\frac{1}{2\pi}\int_0^{2\pi} n_D(t)[(V_T+R_D i(t))i(t)]d(\omega t) \quad (3.52)$$

$$P_C=P_{C,T}+P_{C,D} \quad (3.53)$$

Total inverter power loss P_{LOSS} is given by:

$$P_{Loss}=P_{sw}+P_C \quad (3.54)$$

Therefore the efficiency η of the inverter is evaluated by:

$$\eta=\frac{P_{out}}{P_{in}}=\frac{P_{in}-P_{Loss}}{P_{in}} \quad (3.55)$$

3.5.4. Blocking Voltage

Blocking or standing voltage of a power electronic converter is determined by computing the off-state maximum voltage of individual power switches then summing them to give the total standing voltage of the converter. Standing voltage of converters have a direct relationship with the cost of converter. The proposed multilevel inverter of Figure 62 has 12 There are eight unidirectional power switches in the main circuit and four in the H-bridge session. As a result, the suggested multilayer inverter's standing voltage (VStanding) is determined.
by:

$$V_{standing}=\sum_{k=1}^{s}\sum_{j=1}^{12} V_{s,k,j} \quad (3.56)$$

Where $V_{s,k,j}$ is the blocking voltage of unidirectional switches$S_{k,1}$, $S_{k,2}\dots S_{k,12}$ for the kth switch. The blocking voltages of the 8 main circuit switches are expressed by:

$$V_{s,k,1}=V_{s,k,2}=V_{dc} \quad (3.57)$$
$$V_{s,k,3}=V_{s,k,4}=2V_{dc} \quad (3.58)$$
$$V_{s,k,5}=V_{s,k,6}=4V_{dc} \quad (3.59)$$

$$V_{s,k,7} = V_{s,k,8} = 8V_{dc} \quad (3.60)$$

The blocking voltage of the 4 H-bridge switches are expressed by:

$$V_{s,k,1} = V_{s,k,2} = V_{s,k,3} = V_{s,k,3} = 15V_{dc} \quad (3.61)$$

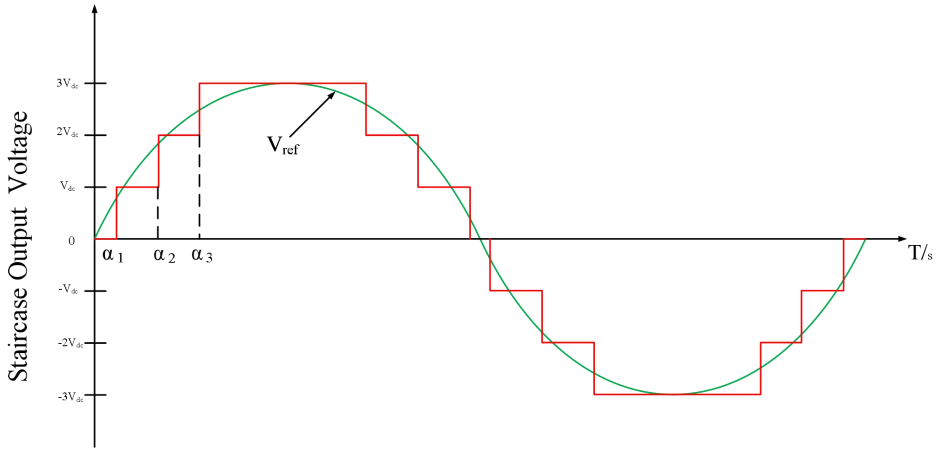
So total standing voltage of the converter therefore is:

$$V_{Standing} = 2(15V_{dc}) + 4(15V_{dc}) = 90V_{dc} \quad (3.62)$$

3.5.5. Fundamental Frequency Control

Nearest level control (NLC) also known as fundamental frequency control (FFC) is employed in switching the proposed single-phase multilevel inverter. Figure 63 shows creation of 7-levels of load voltage through the concept of NLC operations. Each voltage level is produced by comparing the reference voltage with the stepped voltage; the point at which these two voltages meet is the voltage level that is used. If this point is closer to upper voltage level, then that magnitude of output voltage is generated. However, if the point is closer to the lower voltage level, then that magnitude of voltage is generated. Basically, NLC enables selection of closest (nearest) voltage level to be generated by the proposed MLI. For three-phase inverter control, each phase is controlled independently with phase difference of 120^0. NLC technique is much simplified with respect to algorithm when compared to NVC (nearest vector control) because selecting the closest value is simple. In three-phase inverter control, NLC provides independent phase controls unlike SVC which controls three-phase inverters directly [a].

Figure 63
NLC technique



3.5.6. Comparative Analysis

The proposed 31-level single-phase MLI is juxtaposed with other multilevel inverter topologies with respect to the switch and control circuit count, direct current (dc) count, output voltage level count as well as the total component count. This comparative analysis illustrated in Table 3.5 enables us to demonstrate the merit and demerit of the proposed inverter. All referenced topologies in Table 9 generate 31-level of output voltage.

Table 9
Comparative Analysis

Topology	Output voltage Level N_L	Number of Switches N_{IGBT}	Number of Driver Circuits N_{DR}	Number of DC Source N_{DC}	Number of Capacitors N_C	Number of Diodes N_D	Total Components
[1]	31	16	12	4	-	-	32
[2]	31	14	12	3	-	-	29
[3]	31	14	14	4	-	-	32
[4]	31	18	18	2	4	92	44
[5]	31	16	16	2	4	2	40
[6]	31	12	12	3	4	-	31
[7]	31	14	10	6	-	-	30
CHB	31	60	60	15	-	-	135
FC	31	60	60	1	-	35	156
NPC	31	60	60	1	28	-	149
Proposed	31	12	12	4	-	-	28

Considering number of switches (IGBT), the postulated topology and [6] need the fewest switches; nevertheless, the design in [6] employs three dc sources and four capacitors. Compared to existing topologies, the given architecture uses just four dc sources and a fraction of the capacitors. The proposed topology does not require diodes and capacitors to generate 31-level of output voltage. The required number of control circuit with respect to the postulated configuration and other configurations are less, however, the topology in [7] requires the least computation

of driver circuits. Considering the sum of components required, the proposed topology requires the smallest amount of components. The CHB topology requires the highest number of direct current (DC) sources in the table 16 dc sources; the FC topology uses 35 Diodes, while the NPC topology uses 28 capacitors and 1 dc source.

3.6 Simulation Results

This section provides simulation studies as relates the proposed single-phase 31-level multilevel inverter of Figure 62. The cascaded structure is made-up of two submultilevel units having 4 dc sources, 12 power switches and RL load. Simulation of the proposed inverter was done by building its power circuit in PSCAD/ EMTDC software.

Table 10
Simulation Parameters

Parameters	Magnitude
Switching Frequency f_s	50kHz
Load frequency f_o	50Hz
DC Sources V_{dc}	$V_1 = 15V, V_2 = 30V,$ $V_3 = 60V, V_4 = 120V$
Modulation Index	1
Load Resistance R	50Ω
Load Inductance L	0.055H

Table 10 shows the simulation parameters. Figure 64 to Figure 66 shows the output waveforms of proposed 31-level multilevel inverter. The total load voltage and reference voltage waveforms are presented by the illustration in figure 64. As depicted by the waveforms, the stepped load voltages perfectly align with the reference sinusoidal waveform. The maximum voltage is 225V with a frequency of 50Hz. Varying the magnitude of input voltages will vary the magnitude of the output voltage. Figure 65 shows the load current waveform with a peak value 4.23A. Load voltage and current waveforms contain less distortion i.e. they are perfect sinusoidal waveforms.

Figure 66 shows the standing voltage waveforms for all switches in the proposed 31-level inverter. The standing voltage within switch S_1 and S_2 is 15V. The

standing voltage within switch S_3 and S_4 is 30V. The standing voltage within switch S_5 and S_6 is 60V. Standing voltages across switch S_7 and S_8 is 120V. all the switches in the H-bridge have equal standing voltages i.e. S_9, S_{10}, S_{31} and S_{12} have 225V switching voltages across them.

Figure 64
Load voltage and reference voltage waveforms

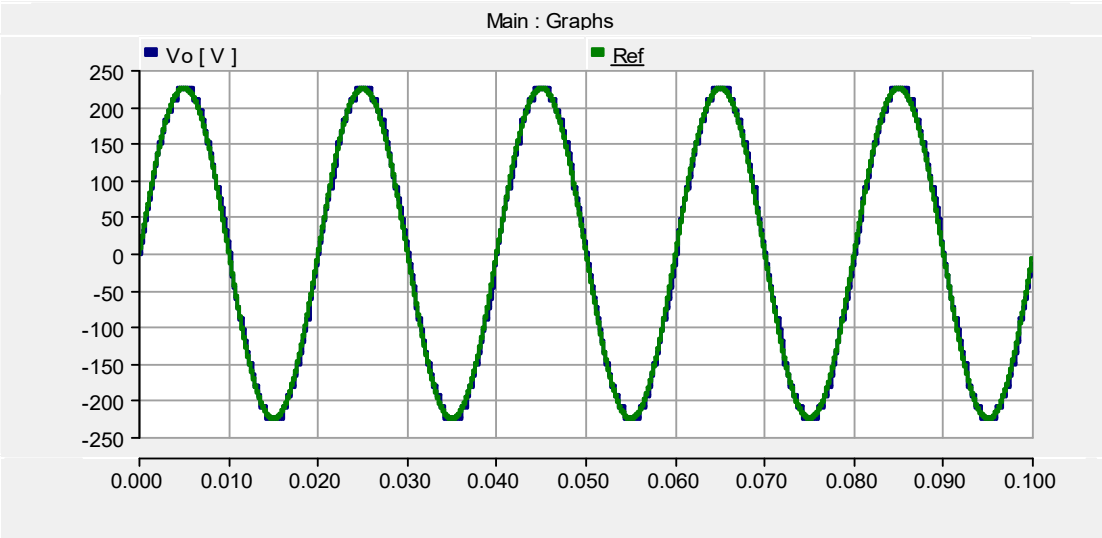


Figure 65
Load current waveform

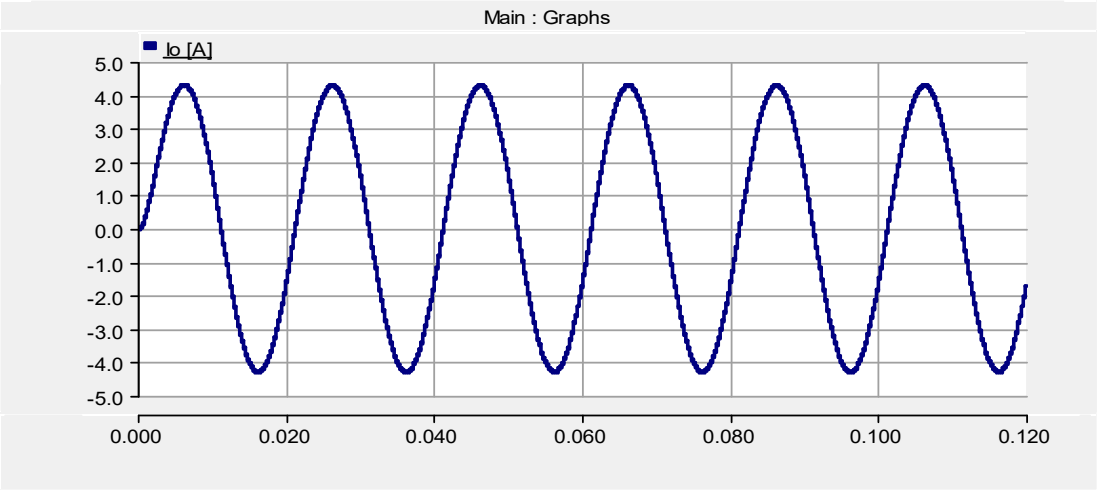
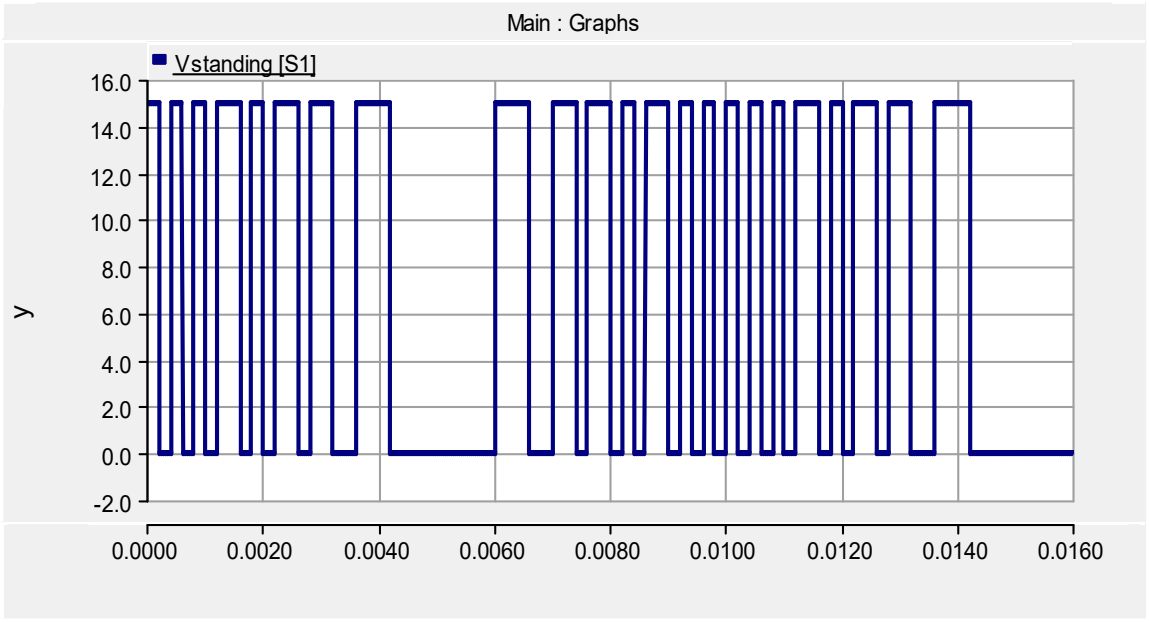
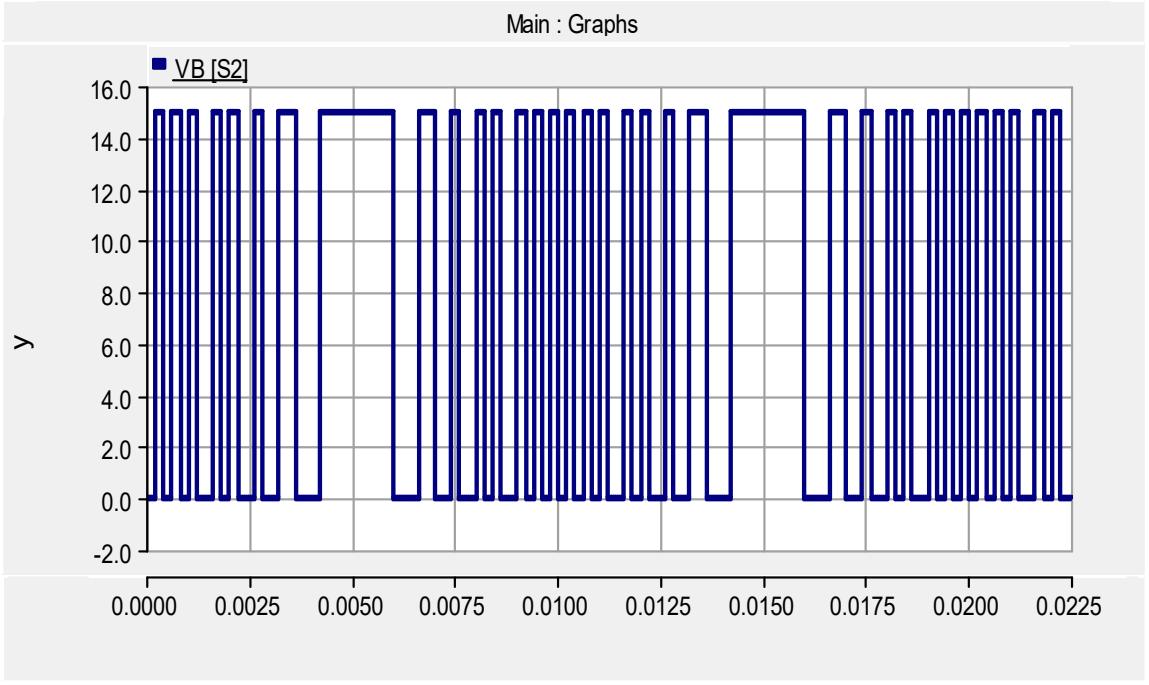


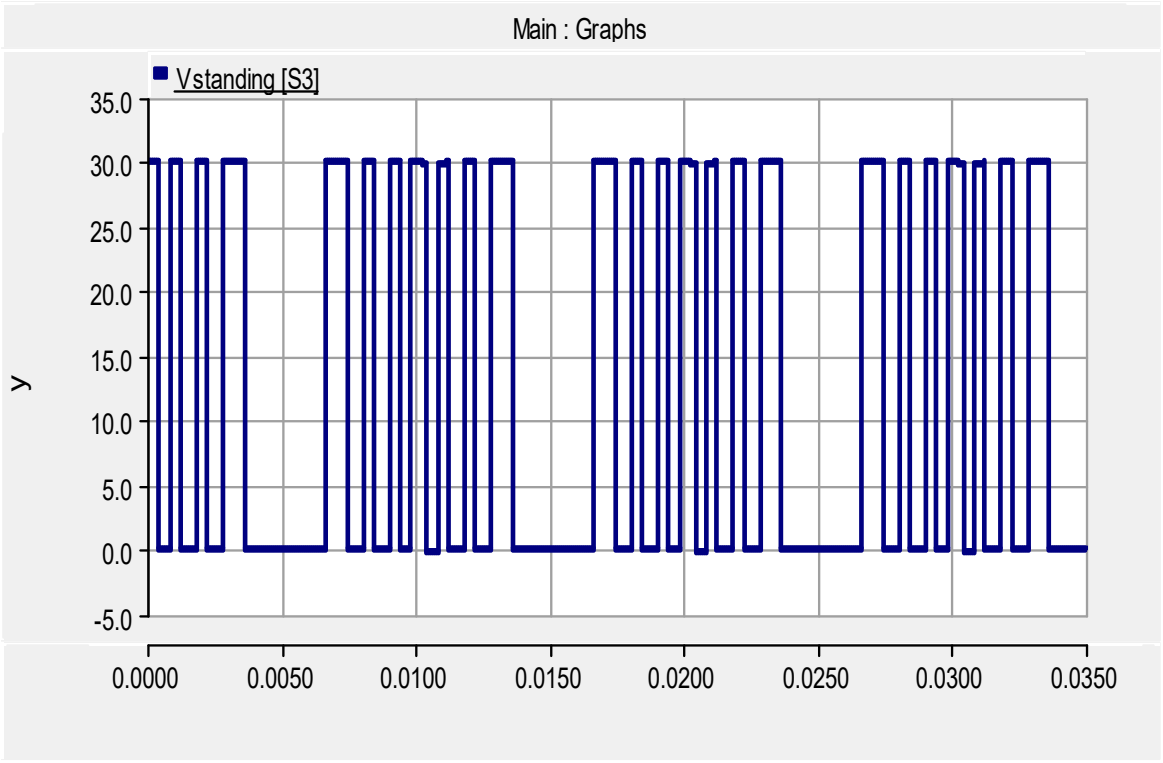
Figure 66
Switch standing voltages



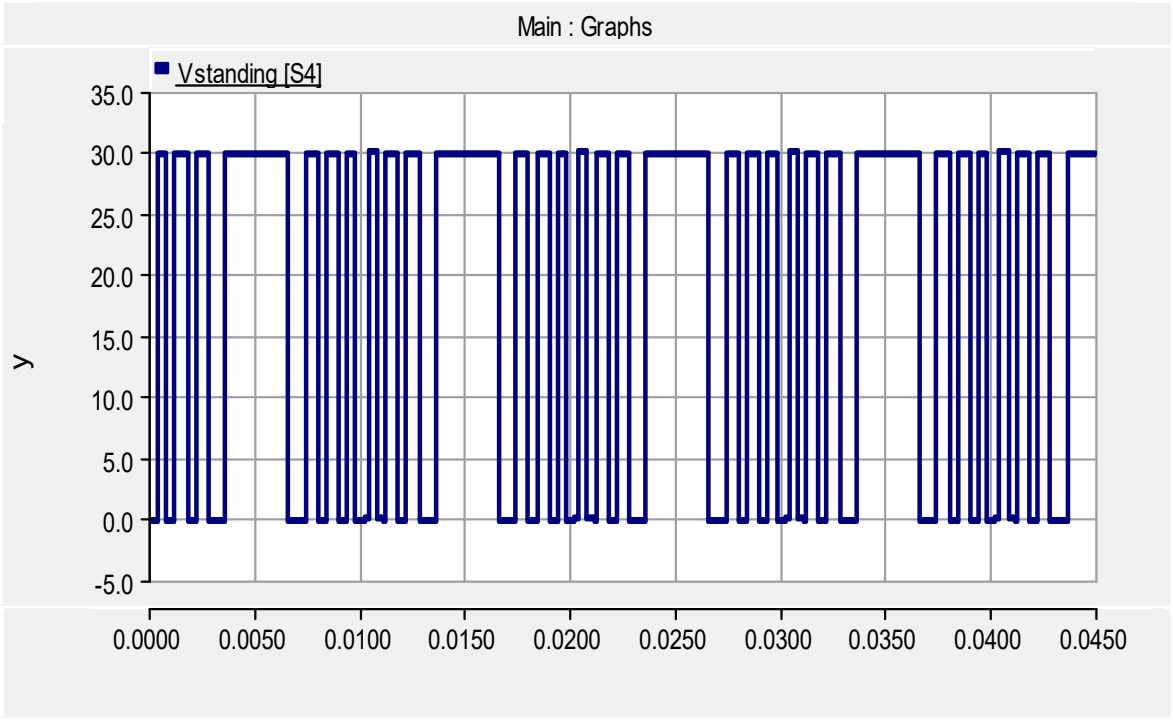
(a)



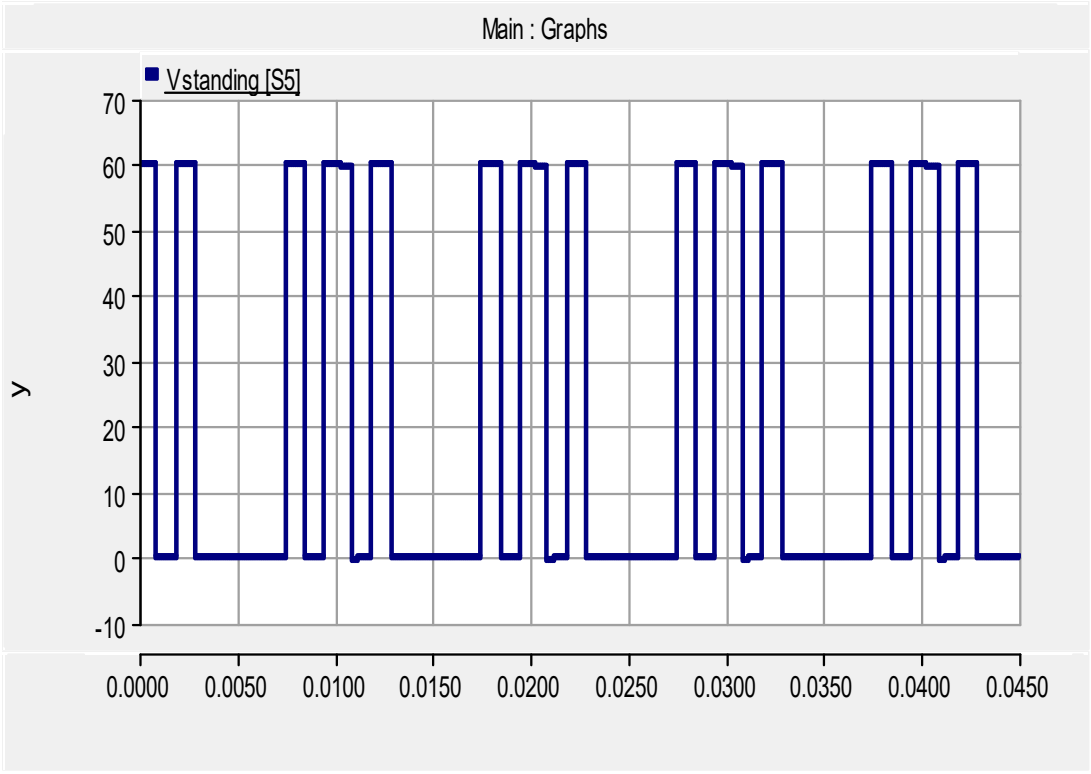
(b)


Main : Graphs
Vstanding [S3]
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
y
0.0000
0.0050
0.0100
0.0150
0.0200
0.0250
0.0300
0.0350

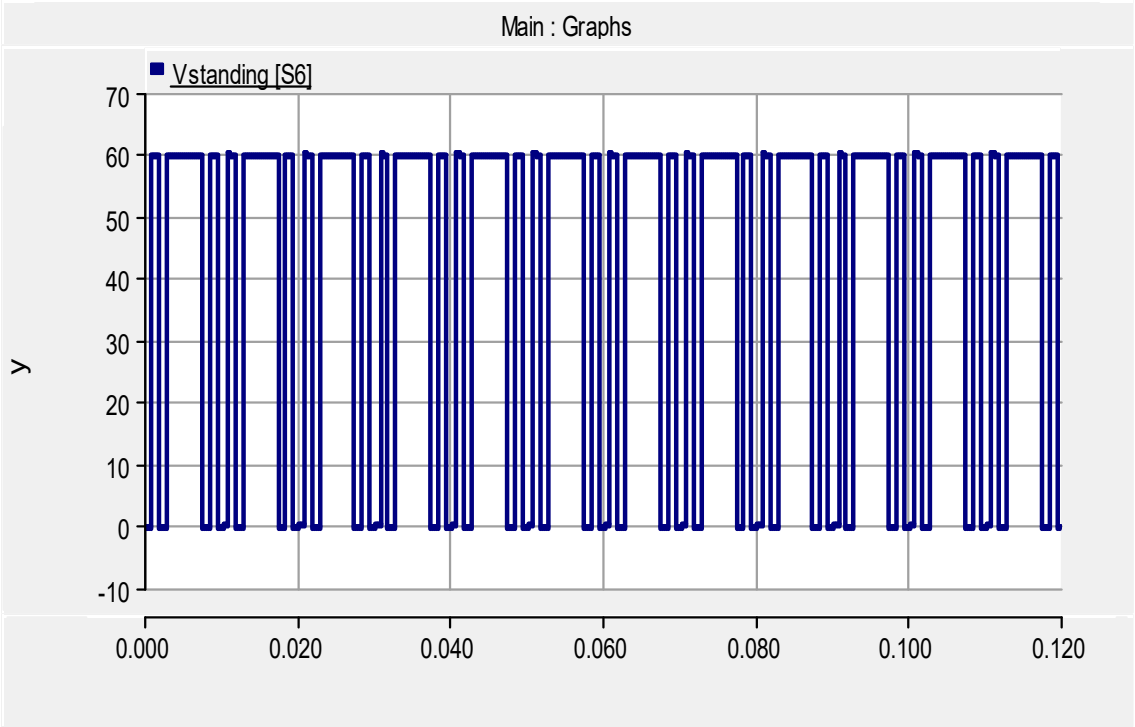
(c)


Main : Graphs
Vstanding [S4]
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
y
0.0000
0.0050
0.0100
0.0150
0.0200
0.0250
0.0300
0.0350
0.0400
0.0450

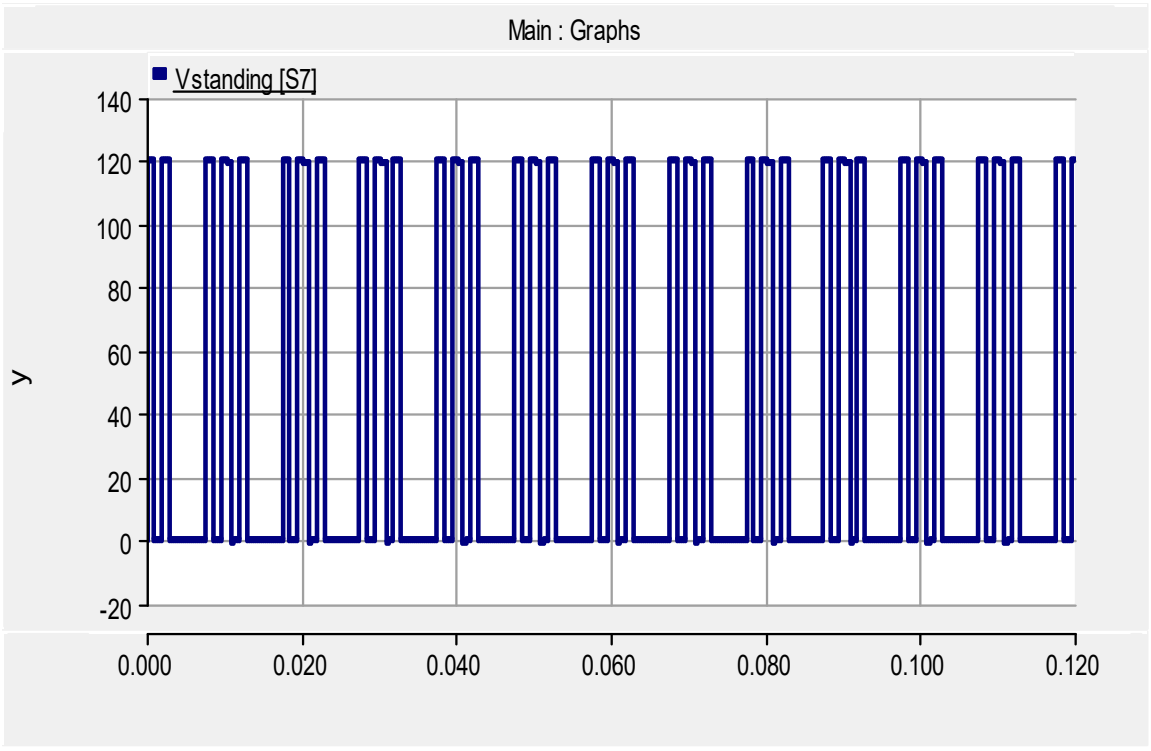
(d)


Main : Graphs
Vstanding [S5]
70
60
50
40
30
20
10
0
-10
y
0.0000
0.0050
0.0100
0.0150
0.0200
0.0250
0.0300
0.0350
0.0400
0.0450

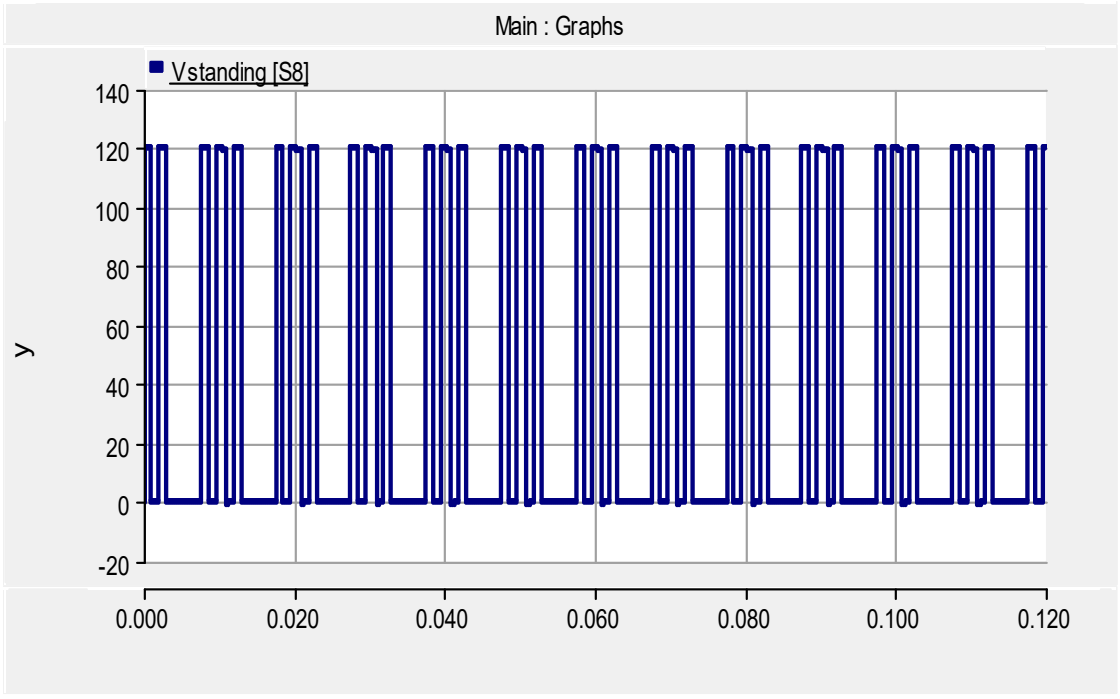
(e)


Main : Graphs
Vstanding [S6]
70
60
50
40
30
20
10
0
-10
y
0.000
0.020
0.040
0.060
0.080
0.100
0.120

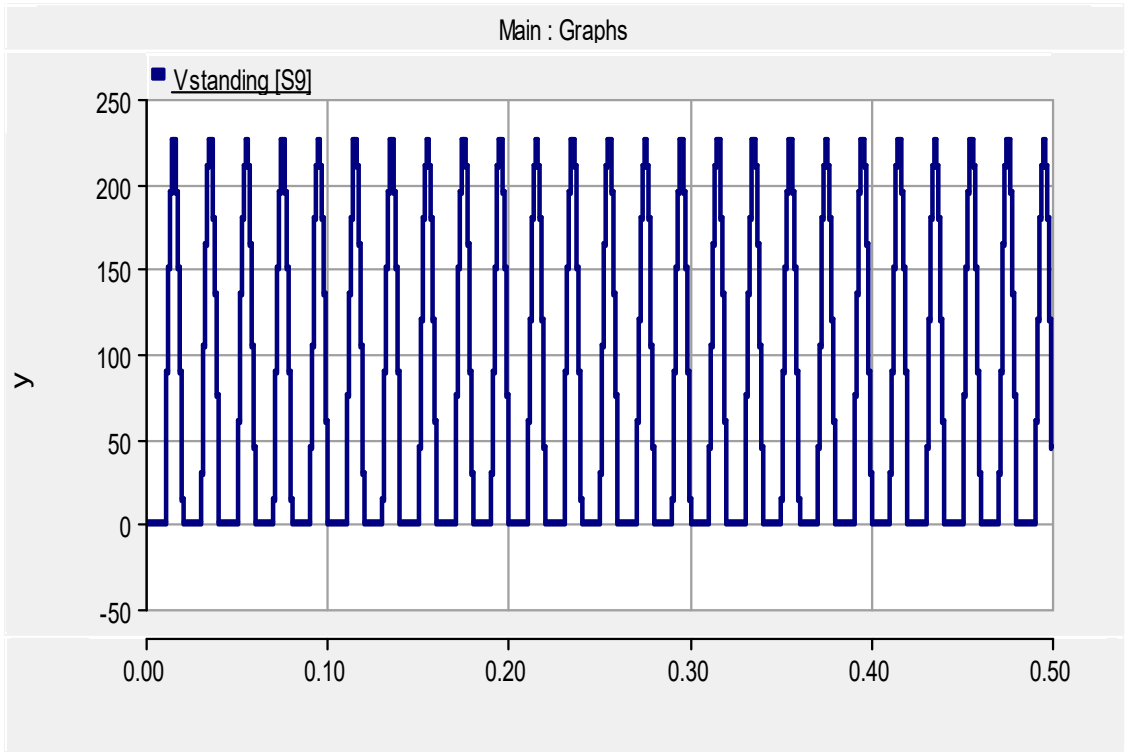
(g)


Main : Graphs
Vstanding [S7]
140
120
100
80
60
40
20
0
-20
y
0.000
0.020
0.040
0.060
0.080
0.100
0.120

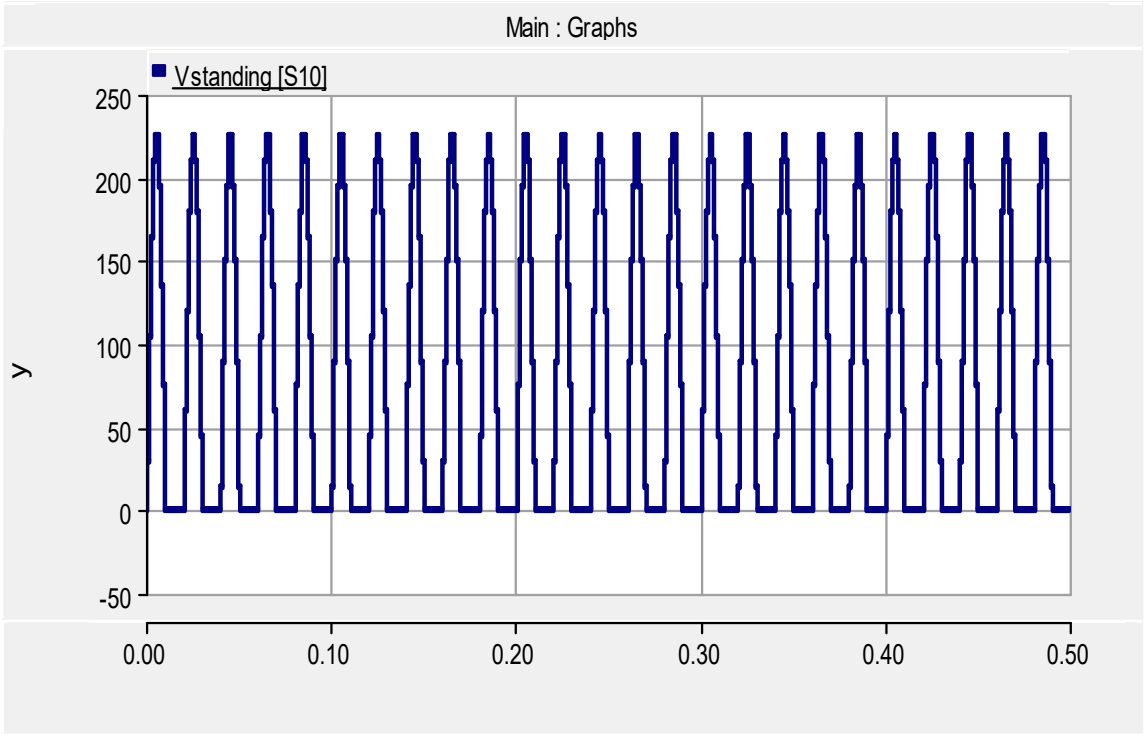
(h)


Main : Graphs
Vstanding [S8]
140
120
100
80
60
40
20
0
-20
y
0.000
0.020
0.040
0.060
0.080
0.100
0.120

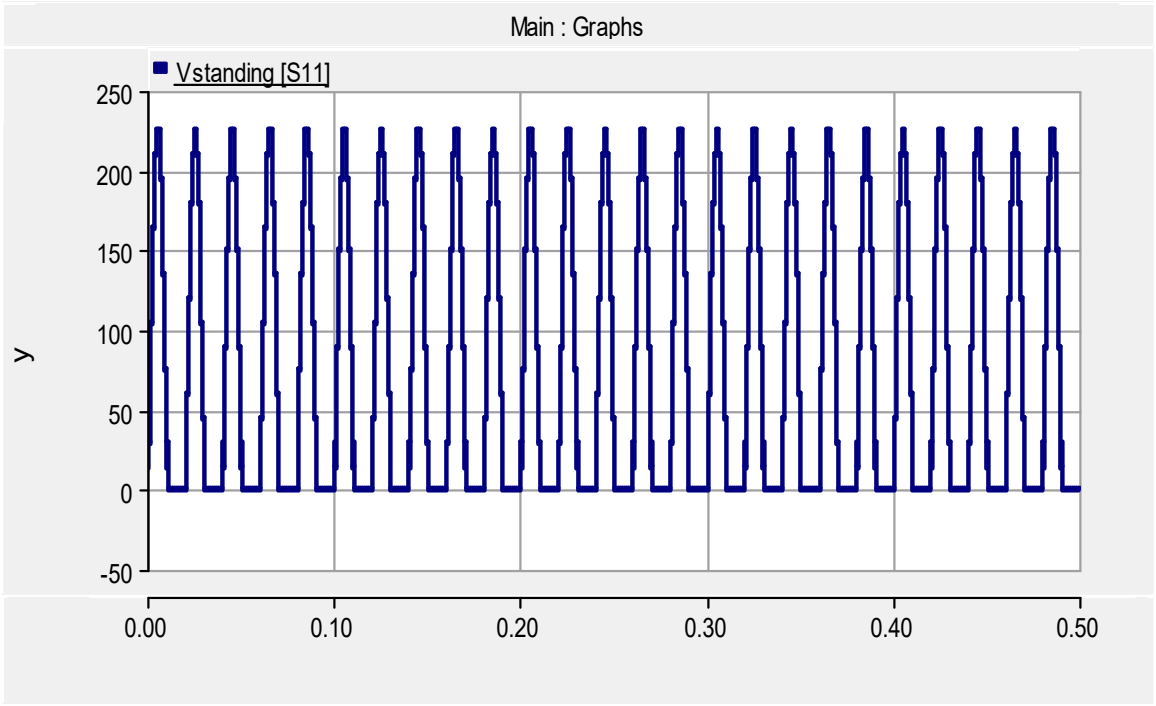
(i)


Main : Graphs
Vstanding [S9]
250
200
150
100
50
0
-50
y
0.00
0.10
0.20
0.30
0.40
0.50

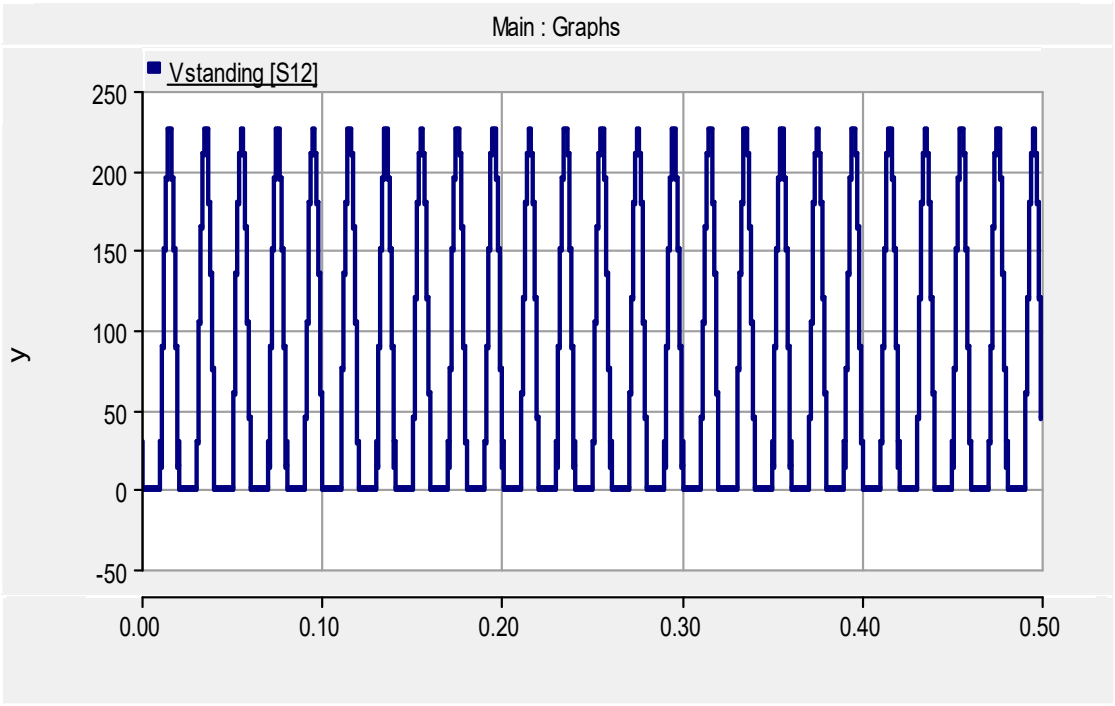
(j)


Main : Graphs
Vstanding [S10]
250
200
150
100
50
0
-50
y
0.00
0.10
0.20
0.30
0.40
0.50

(k)


Main : Graphs
Vstanding [S11]
250
200
150
100
50
0
-50
y
0.00
0.10
0.20
0.30
0.40
0.50

(l)


Main : Graphs
Vstanding [S12]
250
200
150
100
50
0
-50
y
0.00
0.10
0.20
0.30
0.40
0.50

(m)

CHAPTER 4

Conclusion and Recommendation

4.1 Conclusion

Power electronic converters have become an integral component in the supply and distribution of electric power in any modern power system. Most of the advances in areas such as microgrid, distributed generation and transportation (ship, trains, electric vehicles and buses and airplanes) which have been chalked so far will not be possible without the application of power electronic converters. Power electronic converters provide the means by which the characteristic of voltage can be changed or varied i.e. from ac to dc or dc to ac, buck or boost functionality within the same or different form of voltage (ac or dc) and also frequency and phase variations. This thesis focused on one of the most used and researched converter, the multilevel inverter. The quantum of attention received by multilevel inverter from researchers and also as a first choice device for industrial applications is overwhelming and such will (MLI) continues to be in existence for a long while. This research provided a comprehensive analysis of symmetric and asymmetric multilevel inverters and also proposed a new 31-level multilevel which has less component count when compared to other topologies.

Even though multilevel inverters have gained much popularity in academia and industry they still have a few limitations which tend to reduce the efficiency of these inverters. One of these limitations is the high number of components required and the less number of output voltages that are generated. Therefore, this thesis provided a comprehensive investigation of symmetric and asymmetric characteristics of multilevel inverters. The results of the investigations proved that asymmetric multilevel inverters provide higher levels of output voltage juxtaposed with symmetric multilevel inverters even though the component or circuit structure for inverters remain the same. Also, it established that trinary asymmetric topologies provided far high levels of output voltage juxtaposed with binary and asymmetric inverters.

Based on the above revelations, this thesis proposed a new single-phase multilevel inverter which is able generate higher levels of output voltage and uses less

components compared to other existing multilevel inverter topologies. In this comparative investigation, it was established that overall component count the proposed topology was far less than 11 exiting topologies. The proposed topology derived by cascading two submultilevels coupled to an H-bridge was investigated under symmetric and asymmetric conditions and the latter provided 31-levels of output voltage using the same number of components as the symmetric conditions. For equal number of basic units (e.g. n = 6), the symmetric topology generates 7-level of positive output voltage with maximum output voltage of $6V_{dc}$ while the asymmetric topology generates 22-level or 64-level of positive output voltage with maximum output voltage of $22V_{dc}$ and $63V_{dc}$ respectively.

The power circuit of the proposed topology comprises 4 dc sources, 12 power switches, an *RL* load and 12 driver circuit. The proposed multilevel inverter was controlled by fundamental frequency control technique. Fundamental frequency control technique provides reduced switching losses when juxtaposed with some PWM techniques. The theoretical computation of inverter power losses which is the sum of switching and conduction power losses was provided. Also, standing voltage or blocking voltage computations were done mathematically and by simulation. Results of both investigations are equivalent.

Simulation investigation of the proposed single-phase 31-level multilevel inverter was done by building its power circuit in PSCAD/ EMTDC software. The load voltage waveform perfectly aligns with and the reference voltage. This proves that the proposed multilevel inverter controlled by fundamental frequency control is suitable for generating any sinusoidal output waveforms. The load current waveform is also a pure sinusoidal waveform which means the current harmonics are less. The standing voltage waveform of each switch was provided and the peak magnitudes are equivalent to the theoretical computations.

Finally, this thesis proposed a cascaded 31-level inverter. Theoretical analysis of the proposed inverter with respect to power circuit, symmetric and asymmetric voltage characteristics and standing voltage was provided. Also, simulation investigation was conducted. Theoretical and simulation results are in agreement with each other. The

proposed topology has the following advantages; high quality output voltage waveform, generation of high levels of output voltage with less component count, less complex cascaded structure, reduced inverter losses and the application of lower rated switches.

4.2 Future Work

Recommendations for future work are to be able to provide experimental results for the proposed multilevel inverter and also provide a three-phase topology for photovoltaic applications.

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Appendix

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