NDEY JALLOW

HIGH VOLTAGE GAIN DC-DC CONVERTER BASED ON MODIFIED QUASI Z-SOURCE AND SWITCHED CAPACITOR NETWORK

MASTER THESIS

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NEAR EAST UNIVERSITY

INSTITUTE OF GRADUATE STUDIES

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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Approval

We certify that we have read the thesis submitted by Ndey Jallow titled **"High Voltage Gain DC-DC Converter Based on Modified Quasi Z-Source and Switched Capacitor Network"** and that in our combined opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Educational Sciences.

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Declaration

I hereby declare that all information, documents, analysis and results in this thesis have been collected and presented according to the academic rules and ethical guidelines of Institute of Graduate Studies, Near East University. I also declare that as required by these rules and conduct, I have fully cited and referenced information and data that are not original to this study.

Ndey Jallow

14/11/2022

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Ndey Jallow

Abstract

High Voltage Gain DC-DC Converter Based on Modified Quasi Z-Source and Switched Capacitor Network

Jallow, Ndey
Assist. Prof. Dr. Samuel Nii Tackie
MSc, Department of Electrical and Electronics Engineering
October, 2022, 84 pages

This thesis presents a new high gain dc-dc converter. This converter is based on a modified quasi z-source topology and a switched capacitor network. The aim of this presented converter is to be attain high boost of the input voltage with very low duty cycles. In addition when compared to other high gain converters this presented converter has few elements and low stress on its semiconductors. Furthermore, steady state analysis and mathematical analysis of the converter is carried out. A comparison with other high gain converters is also done. Finally, the duty cycle was varied to observe how the output voltage would behave.

Keywords: high voltage gain, modified quasi, z-source network, voltage stress

Özet

High Voltage Gain DC-DC Converter Based on Modified Quasi Z-Source and Switched Capacitor Network

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Bu tez, yeni bir yüksek kazançlı dc-dc dönüştürücü sunmaktadır. Bu dönüştürücü, değiştirilmiş bir yarı z-kaynak topolojisine ve anahtarlamalı bir kapasitör ağına dayanmaktadır. Sunulan bu dönüştürücünün amacı, çok düşük görev döngüleri ile giriş geriliminde yüksek artış elde etmektir. Ek olarak, diğer yüksek kazançlı dönüştürücülerle karşılaştırıldığında, bu sunulan dönüştürücünün yarı iletkenlerinde az eleman ve düşük stres vardır. Ayrıca, kararlı durum analizi ve dönüştürücünün matematiksel analizi yapılır. Diğer yüksek kazançlı dönüştürücüler ile bir karşılaştırma da yapılır. Son olarak, çıkış voltajının nasıl davranacağını gözlemlemek için görev döngüsü değiştirildi.

Anahtar Kelimeler: yüksek gerilim kazancı, değiştirilmiş yarı, z-kaynak ağı, gerilim stresi

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List of Abbreviations

AC:	Alternating current
CCM:	Continuous Conduction Mode
DC:	Direct Current
DCM:	Discontinuous Conduction Mode
EMI:	Electromagnetic Induction
IGBT:	Insulated Gate Bipolar Transistor
LED:	Light Emitting Diode
MOSFET:	Metal-oxide Semiconductor Field-effect Transistor
PV:	Photovoltaic
PWM:	Pulse Width Modulation
QZSI:	Quasi Z-source Inverter
SC:	Switched Capacitor
SEPIC:	Single Ended Primary Inductor Converter
SL:	Switched Inductor
THD:	Total Harmonic Distortion
VSI:	Voltage Source Inverter
ZSI:	Z-source Inverter

CHAPTER 1

1.0 Overview

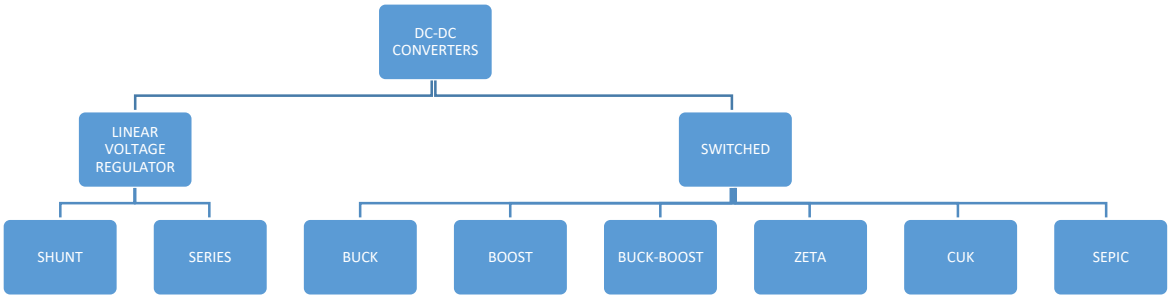
As world population and modernization increases by day, demand for energy has increased tremendously. Transportation, aircraft, trains, automobiles, ships, building, health care, education, communication, etc. all require energy to function properly. However the number one problem the energy sector is facing is the short supply of fossil fuel sources like diesel due to price volatility. These fossil sources also pose high threats like global warming and climate change to our environment. In order to address these issues an alternative like renewable energy was introduced as a means to not only address the scarcity of fuel but to also help combat climate change.

However, most of the time the power generated from renewable energy needs processes like boosting and inverting to suit the intended applications. DC-DC converters have been one of the devices that are being used in renewable energy systems.

DC-DC converters operate on dc voltage, they convert low voltage dc to high voltage or high voltage dc to low voltage dc by the use of a switching element which converts DC to AC square wave signal which is then passed through a filter to convert it to DC voltage. The output of this voltage can either be lower or higher depending on the need. From the name it is clear that these converters only work on DC voltage. As illustrated below in figure 1 DC-DC converters can be classified into two namely linear and switch. Each of these have different topologies that perform specific functions.

Figure 1

DC-DC Converters



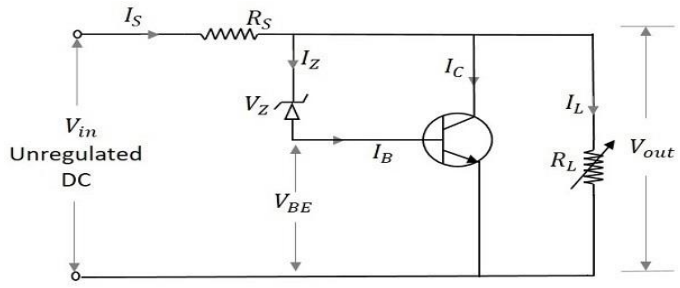
A linear regulator is a device that maintains a constant voltage. The resistance of this regulator varies in response to the voltage input and the load on the system, resulting in a constant output voltage. This device is designed to function as a variable resistor, constantly altering a voltage divider to maintain a constant result voltage and emitting the variations as heat to the environment. This works by utilizing a resistive voltage drop to make and direct a given voltage output while the switch mode works by putting away the energy input intermittently and afterward delivering that energy to the output at an alternate voltage. Linear voltage controller has two types, the shunt and series voltage controller.

Shunt Regulator

Shunt regulator works by allowing a changeable resistance path between the source voltage and ground. It has been discovered that total dosage exposure degrades loop gain and affects regulation, however using a shunt regulator topology can greatly increase dependability at larger total doses. (Chen, et al., 2008). Shunt capacitors can provide the system with reactive power. Because a capacitor's reactive power output is related to the square of the system voltage, its efficacy at high and low voltages may be compromised. As a result, capacitors are commonly constructed using a combination of fixed and switched capacitors to increase their performance under various loading situations. As a result, they are unable to create changeable reactive power on a continuous basis. (Hosseini et al., 2018)

Figure 2

Shunt Regulation (Hosseini et al, .2018).



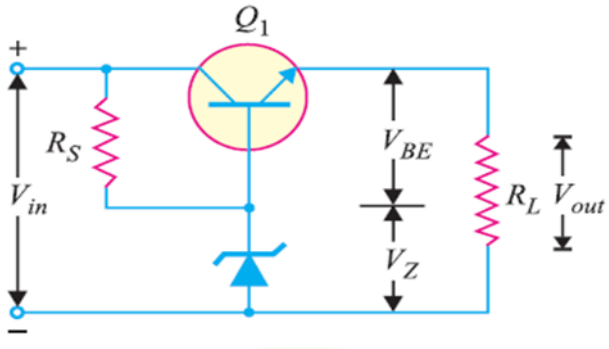
Series Regulator

A series voltage regulator is the most common type of linear voltage regulator, and it is more effective than shunt regulators. In distribution systems, series voltage regulators are often employed to regulate voltage. However these devices are incapable

of generating reactive power, and their operation only forces the source to do so. Furthermore, they have a delayed response time and operate in a step-by-step manner. (Hosseini et al, .2018). For better efficiency of the device, designers focus on minimizing the voltage and reducing the transistors, even though some circuits cannot effectively regulate the input voltage as it approaches a desired output voltage. Those that are able to regulate the input voltage are known as Low Dropout regulators. Unlike shunt regulators, a series regulator can only supply current.

Figure 3

Series Regulator (Hosseini et al, .2018).



Switched-mode converter

When it comes to DC-DC converters, switching converters are more efficient than linear regulators, which usually consists of a simpler circuits that lowers voltages by wasting energy as heat without stepping up current in the output.

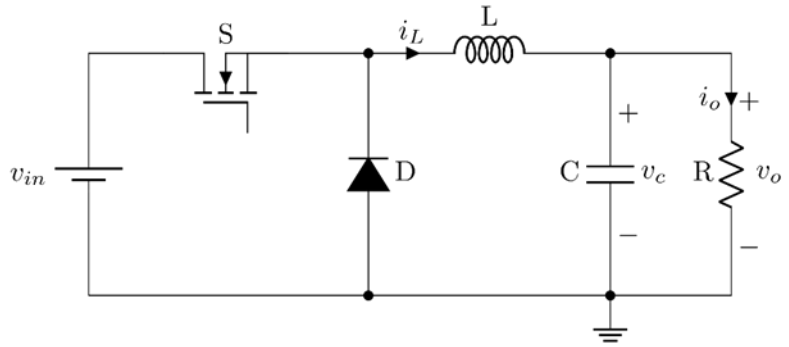
Buck Converter

Buck converter or step down converter is a kind of switched-mode converter which makes use of at least one diode and a switch, one capacitor and an inductor.

Buck converter and its derivatives are well-known for its ability to create step-downs hence this converter steps down input DC voltage from a high level to a lower level. Buck conversion is a popular and commonly used technique in electrical circuits for portable devices such as VLSI and integrated circuits etc. Current in buck converters is derived from its power source in the form of pulses and the battery source's dependability is influenced by the ripples. Buck converters can operate in either CCM or DCM by nature of switching actions which is determined by continuity of current flow through the inductor.

Figure 4

Buck Converter



Boost Converter

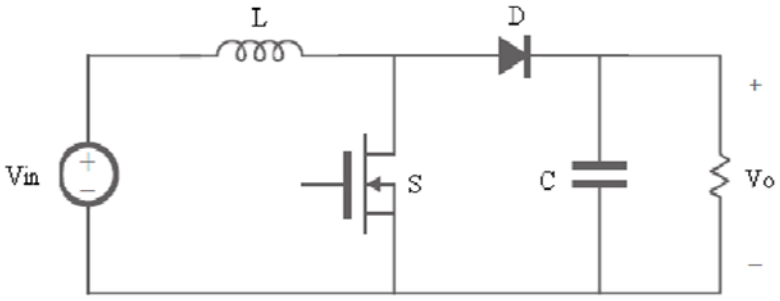
Boost converter as specified in the name is a converter that increases or boosts dc voltage while stepping down current i.e. boost converter steps up voltage from lower level to higher level. It's a type of switched-mode converter consisting of a switch, a capacitor, an inductor, a diode with a voltage source. Boost converters can be prone to voltage ripples, this however can be eliminated by making use of filters consisting of capacitors, the capacitors can be connected at the input and output of the converter. Furthermore, boost converters are also extremely nonlinear systems, for this reason a range of linear and nonlinear control approaches have been investigated for attaining effective voltage regulation with substantial load changes. This converter gets its power source from DC sources like solar panels, DC generators etc. A boost converter's primary idea consists of two separate states.

In the on-state the switch is closed, causing the inductor current to increase while in the off-state the switch is open, the current will decrease because it can only flow through the inductor to the diode and the load, and for this reason the inductor will generate a voltage to compensate for the loss current. This voltage will in turn charge the capacitor to a voltage much greater than the input voltage.

This converter is used in hybrid electric circuits, LED driver, LED backlight, flash light, and solar power systems.

Figure 5

Boost Converter Topology

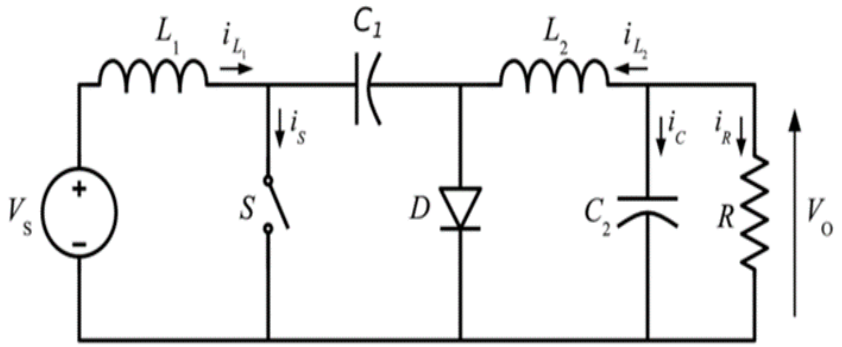


Buck–boost Converter

Buck-boost converter makes used of features from the buck converter and boost converter, its basic circuit contains capacitors, inductors, a switch, diode and a voltage source. The lack of a ground line in the switch makes the drive circuitry more difficult to operate, which might be a disadvantage of this converter. Occasionally, a DC-DC buck converter is used to create a little amount of output voltage from a large amount of input power, allowing for smaller devices and longer battery life. Buck-boost converters, on the other hand, may produce output voltages that are greater or lower than the input voltage and can provide both steps up and steps down output voltage. Buck-boost converters can work in one of two conduction modes: continuous or discontinuous. Buck-boost converter can operate either as a buck converter or a boost converter at a given time, it cannot operate as both simultaneously. (Soheli et al., 2018). Application s of this converter include battery power systems, self-regulating power supplies, etc.

Figure 6

Buck-boost Converter (Soheli et al., 2018).

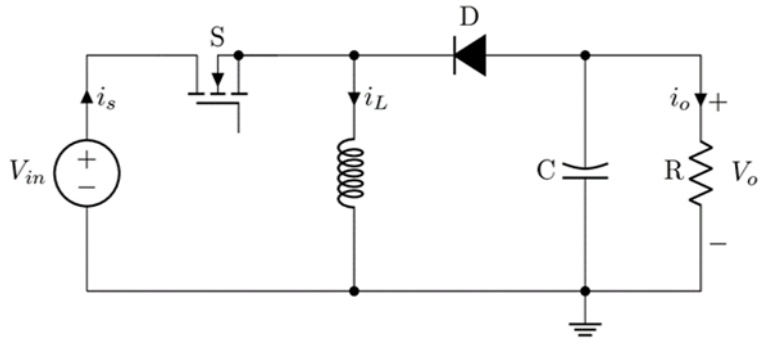


Cuk Converter

The operation of cuk converter is identical to a buck-boost converter, except for the fact that the output voltage of the cuk converter is reversed when compared to the input voltage, ie the polarity of the input voltage and the output voltage are opposite (Ahmethodžić, et al.,2017). One of the advantages of the cuk converter is that it uses a capacitor for energy transmission rather than an inductor as in other basic DC-DC converter topologies. The interleaved configuration was extensively implemented a short time ago because of its unique benefits. Reduced settling time and decreased ripple content on the output side are two major advantages. The main advantage of using a non-isolated Cuk converter over a buck-boost converter or other DC-DC topology is that it may provide completely regulated DC output voltage. It improves the settling time period while reducing the ripple content in both the input and output sides. (Tuvar & Ayalani, 2019).

Figure 7

Cuk Converter (Tuvar & Ayalani, 2019).



SEPIC Converter

SEPIC is basically a combination of boost and inverted buck-boost, it has identical features to buck boost converter. However, it has a non-inverted output which produces an output which has the same polarity as the input voltage. This converter makes use of a capacitor to couple voltage from the input to the output which as a result makes it easy to respond to a short-circuit output and be able to shutdown fully.

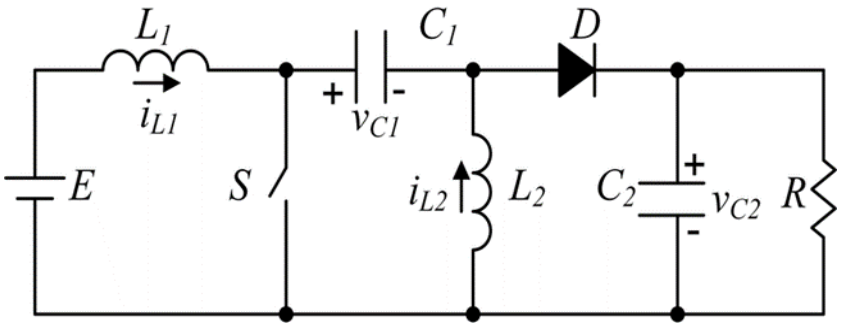
SEPIC, like any other switched mode converter, converts voltage by energy transfer between capacitors and inductors. Switches like MOSFET because of their

ability to have a greater input impedance and low voltage drop are used to control the quantity of energy exchanged or transferred.

SEPIC is used in single lithium batteries because of its ability to either lower to boost the voltage at the output of the regulator.

Figure 8

Sepic Converter Topology

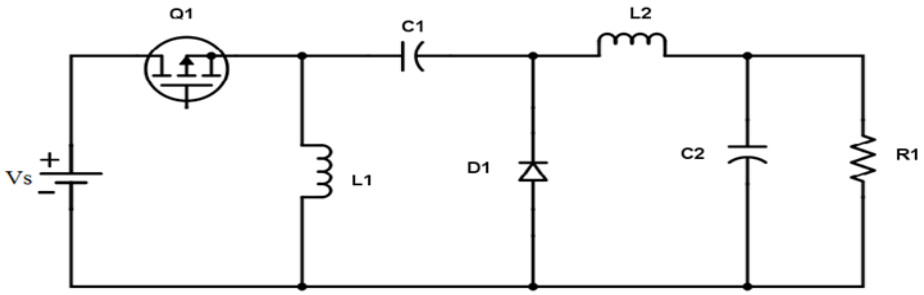


ZETA

A ZETA converter is a converter that generates positive output voltage from an input voltage that is either greater or lower than the output voltage. Zeta has the same operational function as the SEPIC but their difference is that SEPIC is developed from the boost converter topology while the zeta was developed from the buck topology. Zeta has very low output voltage ripple, similar to the buck and cuk converters. Inductor in series with v_{out} in each of these converters prevents abrupt fluctuations in output current from increasing ripple voltage**.** ZETA converter topology consists of two inductors and two capacitors that can operate to either lower or boost voltage. This converter is alternative for controlling power sources low-cost wall wart that have unregulated supply.

Figure 9

Zeta Converter Topology



1.1Thesis problem

In an effort to combat global warming and climate change renewable energy was introduced. However, to be able to use the power generated from renewable energy devices like dc-dc converters and inverters are needed. However, these devices are affected by numerous drawbacks. Switching converters for instance, tend to be expensive and highly susceptible to noise interference, the choppers can be quite unstable with supply of current and voltage which makes them inadequate. Fly-back converter types are affected by ripples, losses and electromagnetic interference.

In addition some impedance sources have issues like high duty cycles, numerous elements, low gain and in situations where the boot range ratio of the impedance source find it hard to increase the average power of the switching device. Quasi z-source topology derived from z-source to address low gain but it is not effective in high modulation index.

1.2 Aim of Thesis

Like all other converter devices this converter is set to address a number of issues that were noticed from converters before. This thesis aims to tackle issues that are highlighted below:

- This device for conversion should have the ability to perform with high efficiency and reduced losses.
- Less cost.
- This converter should be able to achieve a high voltage gain compared to conventional z-source dc-dc converter and quasi z-source.
- Less voltage stress on the elements.
- Less number of elements.

The above will be verified by running simulations on PSCAD/EMTDC.

1.3 Importance of this thesis

The presented converter has less number of elements which as a result reduces the complexity and cost of the circuit. Furthermore, because DC-DC converters have the ability to lower or increase voltage it therefore lessens damage to the device and also

saves space on the batteries. The z-source inverter compared to traditional i-source and v-source inverters has a buck-boost feature that allows it to give any desirable output despite the input. In addition z-source converters have a higher voltage gain and low duty cycles compared to conventional i-source and v-source converters. The z-source topology is simple which therefore reduces cost and improves efficiency. The quasi z-source converter operates on low shoot through current. Secondly it has low voltage stresses on its capacitors and low current stress on the inductors.

1.3 Limitation

Although the paper has been written and conducted with utmost thought and analysis it is however impossible to say that it has no limitations. Firstly, all stimulations are conducted using PCAD which means we can only go as far as the scope of the software which will render minimal control over the results. Even though results from simulations on computer software are a standard academic practice it is without a doubt to say that experiments conducted in a laboratory would give a much better analysis and results but the lack of said materials has been a major limitation.

1.4 Overview of thesis

This thesis is divided into the following:

Chapter 1: Introduction, thesis problem, aim of this thesis, importance of this thesis, limitations, overview of the thesis.

Chapter 2: Literature review on impedance based DC-DC Converters.

Chapter 3: Analysis of the presented topology and simulation results.

Chapter 4: Conclusion and recommendation for future works.

CHAPTER 2

Literature Review on Impedance Based DC-DC Converters

2.0 Overview

Energy has been an essential issue throughout human history, nearly encompassing existence. Although traditional energy resources such as coal, oil, and gas have long been used to supply energy. The disadvantages of these fuels lead to the introduction of renewable energy sources, but in order to utilize renewable energy we will need devices like converters and inverters. For this reason researchers in the area of power conversion and control developed a high interest in impedance source converters. This chapter will be a review on impedance source networks.

2.1 Z-source DC-DC converter

The impedance source network was first proposed by Feng in 2002 in order to address the shortcomings of the I-source and v-source inverter. In the impedance source topology the components are connected in an x shape as shown in figure 10, this is to optimize the voltage gain. Impedance source topology can be used ac-ac, ac-dc, dc-dc, etc.

Focusing on the dc-dc topology of the impedance network, the converter proposed by Kumar & Veerachary (2017) shows how the topology is ideal for great step-up applications. However this is only possible because of the fact that the energy source is secluded from the load, with that the boost ratio of the converter is higher and we can also get positive values for the output voltage and clamp switch voltage.
As shown in figure 11 this converter makes use of the boost converter circuit with modifications i.e. the inductor in a boost converter circuit is replaced with an impedance network. For this reason the converter able to perform better compared to I-source and v-source converters.

When the power is acquired from a dc voltage source it works in two states namely current-fed and voltage-fed. Only two switches s_1 or s_2 are used in each of the two modes. All switches can be constructed consisting of a free-wheeling diode and power transistor, or a power electronic switch like MOSFET, to enable the flow of

current in both directions. The signal is filtered with the use of small capacitors and inductors. (Fang, 2008).

Figure 10

Z-source Inverter (Peng, 2002).

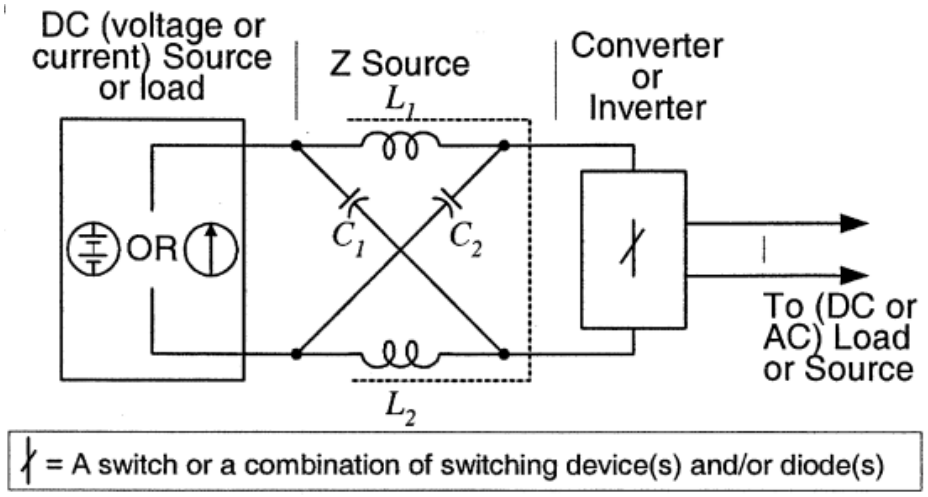
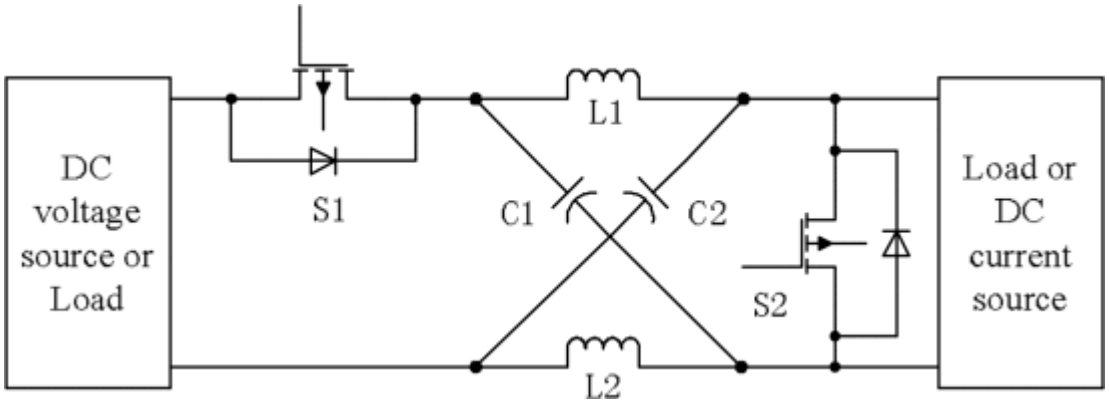


Figure 11

Z-source DC-DC Converter (Fang, 2008).



There are two modes of operation in this topology. In the first mode the source is a dc voltage source, this mode is also referred to as the voltage fed mode. In mode two the source is a dc current. Furthermore, mosfet is used as a switch in order to allow the current to flow in both directions. Pwm is used to control the switching. In voltage-fed operational mode or mode 1, the active component of the S_1 and switch S_2 are operated in an alternative manner, leaving the different two devices in a switched state. When the power movement is inverted, while the other two devices are switched as shown in

figure 12 the active portion of S2, the diode and switch S1 are operated in the opposite order. The boost ratio of the converter for both operational modes as shown in table 1 at steady state can be derived using the duty cycle. (Fang, 2018).

Figure 12

Operation Modes of Z-source DC-DC Converter (Fang, 2008).

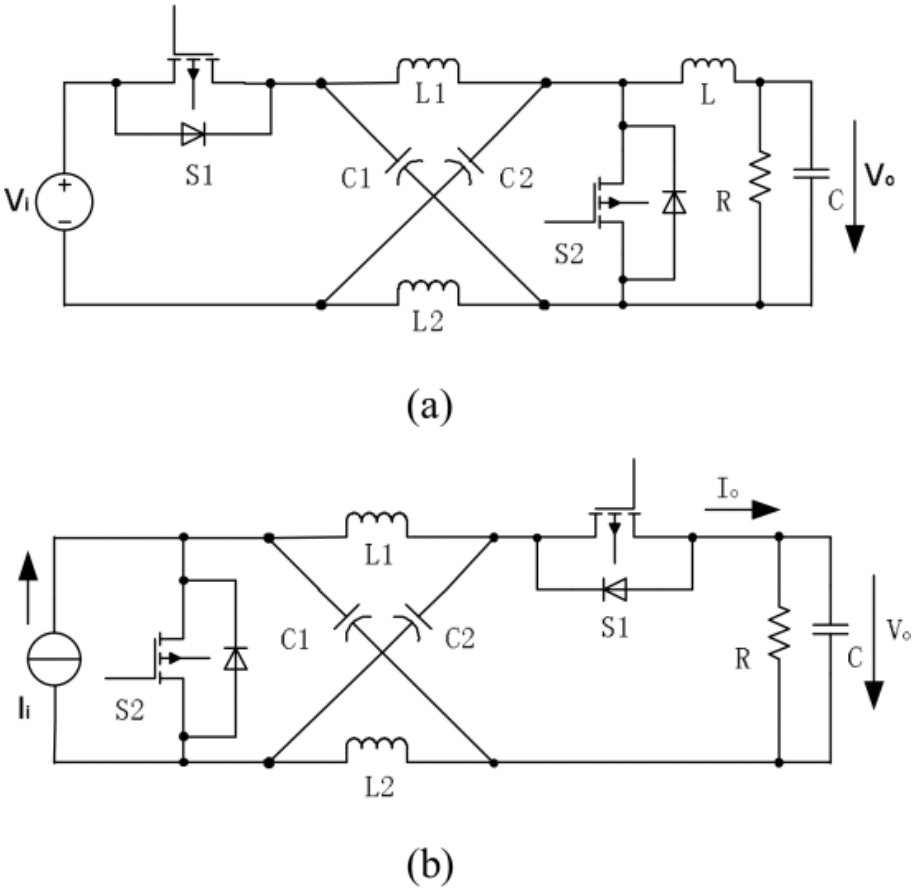


Table 1

Voltage Transmission Quotient of Z-source Converter (Fang, 2018)

Z-source dc-dc converter	Voltage gain in each mode of operation
Voltage fed	$\frac{1-D}{1-2D}$
Current fed	$\frac{2D-1}{D}$

A current-fed Z-source topology could also be tested. To make the analysis easier, we just look at power movements from source to load and disregard the opposite scenario. As a result, the active portion of the diode, switch 1 and switch 2 may be omitted, as presented in Figure 13. This circuit has two states, which are illustrated in Figures 13 a. and b, respectively. (Fang, 2018).

The Z-network is proportioned, similar to that of other impedance source topologies, in that L_1 and L_2, as well as C_1 and C_2, have the equal capacitance and inductance, correspondingly. As a result we have symmetry and equivalent circuits. (Fang, 2018).

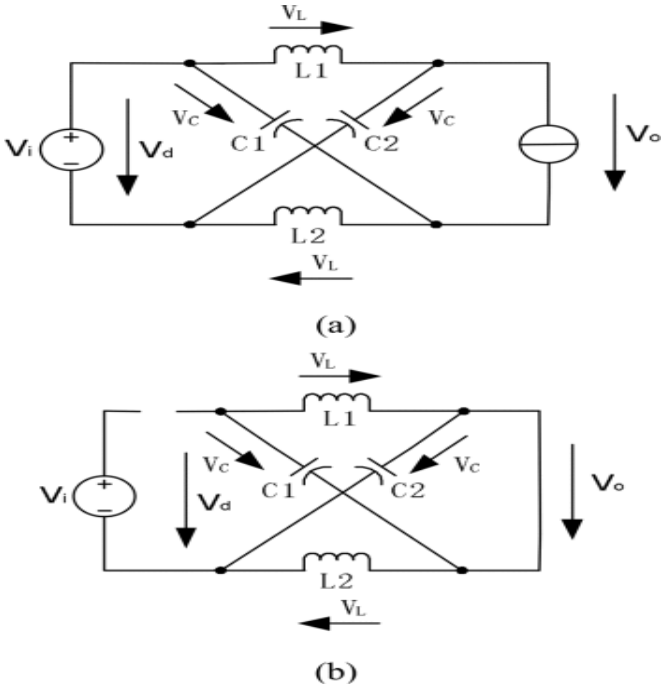
$$V_{C1} = V_{C2} = V_C \quad and \quad V_{L1} = V_{L2} = V_L \tag{2.0}$$

S_1 is turned active, while S_2 is inactive in mode 1. The inductors release and transport energy to the load while the capacitors in the z-network are charged by the dc source. As shown in Figure 13(a), the converter's instance in this condition is (1-D) T, where T stands for the cycle of switching and D is the duty cycle of switch S_2 (Fang, 2018).

$$V_C = V_i - \nu_L, \qquad V_O = V_i - 2\nu_L \tag{2.1}$$

Figure 13

(a) When S1 is active and S2 is inactive. (b) When S1 is inactive and S2 is active (Fang, 2018).



S_2 is on while S_1 is off in mode 2. While capacitors in the z-network release, the inductors charge up and store energy before releasing or transmitting the load. As presented in Figure. 13(b), the converter's levels are DT (Fang, 2018)

$$V_C = \nu_L, \qquad V_O = 0 \tag{2.2}$$

The value of V_i and the dc voltage source are equal.

In steady state the inductor's average voltage should be zero, according to (2.0) and (2.1) (Fang, 2018).

$$\frac{V_C}{V_i} = \frac{1-D}{1-2D} \tag{2.3}$$

The peak voltage at the output of the converter may be stated as follows during a switching cycle:

$$\upsilon_0 = 2V_C - V_i = \frac{V_i}{1-2D} \tag{2.4}$$

The converter's average output voltage may be represented as follows:

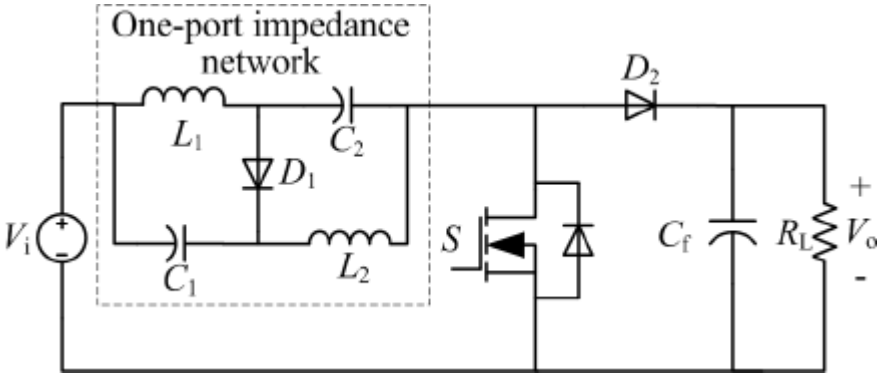
$$\nu_0 = V_C = \frac{1-D}{1-2D} V_i \tag{2.5}$$

The duty ratio D may obviously be reduced or raised to improve the voltage at the output of the suggested converter. Whether the output voltage is in phase with input or not is dependent sole on the duty cycle, this feature can only be seen in the Z-source converter. The inductance and capacitance needs of the impedance network based devices are usually minimal since the frequency of switching is so high, resulting in a tiny and light system (Fang, 2018).

Modified Z-source dc-dc converter was proposed by Yang et al. (2014) to address some of the shortcomings of the z-source converter, these include the voltage stress on the semiconductors and the capacitor and the narrow load range. In the modified converter as shown in figure 14 the x shaped impedance form is modified to a one port impedance network. Pulse width modulation is used to control the switches.

Figure 14

Modified Z-source Network (Yang et al., 2014).



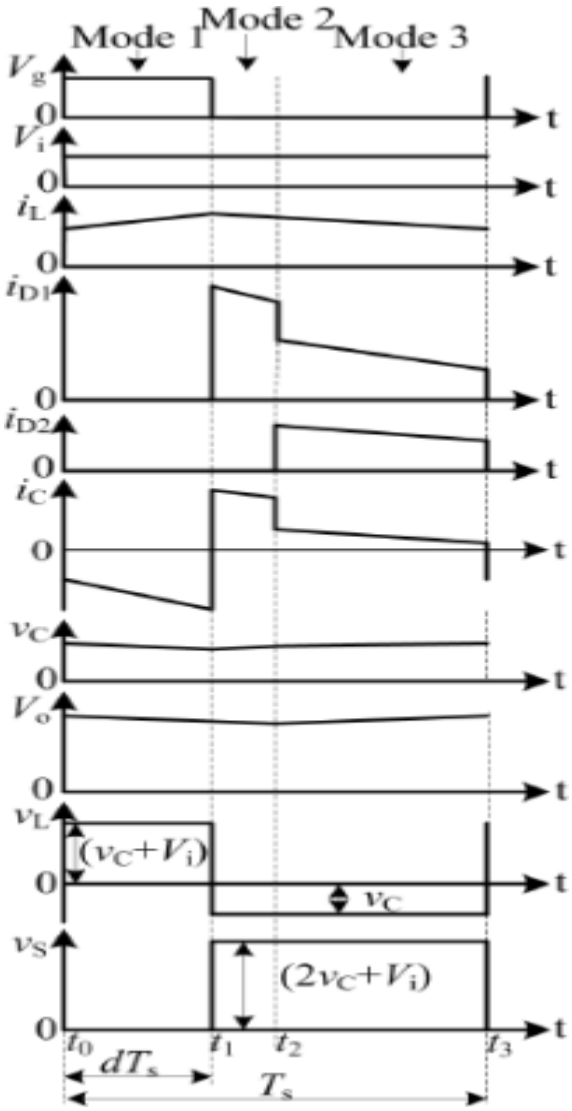
In a matter of switching period the converter operates in three modes. The resulting equations can be deduced from the symmetric nature of the one port impedance network.

$$\begin{cases} i_{L1} = i_{L2} = i_L \\ i_{C1} = i_{C2} = i_C \end{cases} \tag{2.6}$$

$$\begin{cases} V_{L1} = V_{L2} = V_L \\ V_{C1} = V_{C2} = V_C \end{cases} \tag{2.7}$$

Figure 15

Waveform Analysis of Modified Z-source Converter (Yang et al., 2014).



Mode 1: $t_0 - t_1$

In this mode the switch is active while D_1 and D_2 are not operational as shown in figure 16.a. the equations below can be derived from this mode of operation.

$$\begin{cases} i_L = -i_C \\ i_i = 2i_L \end{cases} \quad (2.8)$$

$$V_L = V_i + V_c \quad (2.9)$$

$$V_s = V_i + 2V_C \quad (2.10)$$

Mode 2: $t_1 - t_2$

In this mode of operation the switch is inactive and D_1 is forward biased as shown in figure 16.b. the equations below can be deduced from this mode of operation.

$$\begin{cases} i_L = -i_C \\ i_{D1} = 2i_L \end{cases} \quad (2.11)$$

$$V_L = -V_C \quad (2.12)$$

$$V_s = V_i + 2V_C \quad (2.13)$$

Mode 3: t_2-t_3

In this mode the switch is off while D_1 and D_2 are on as shown in figure 16.c. the equations below are derived from this mode of operation.

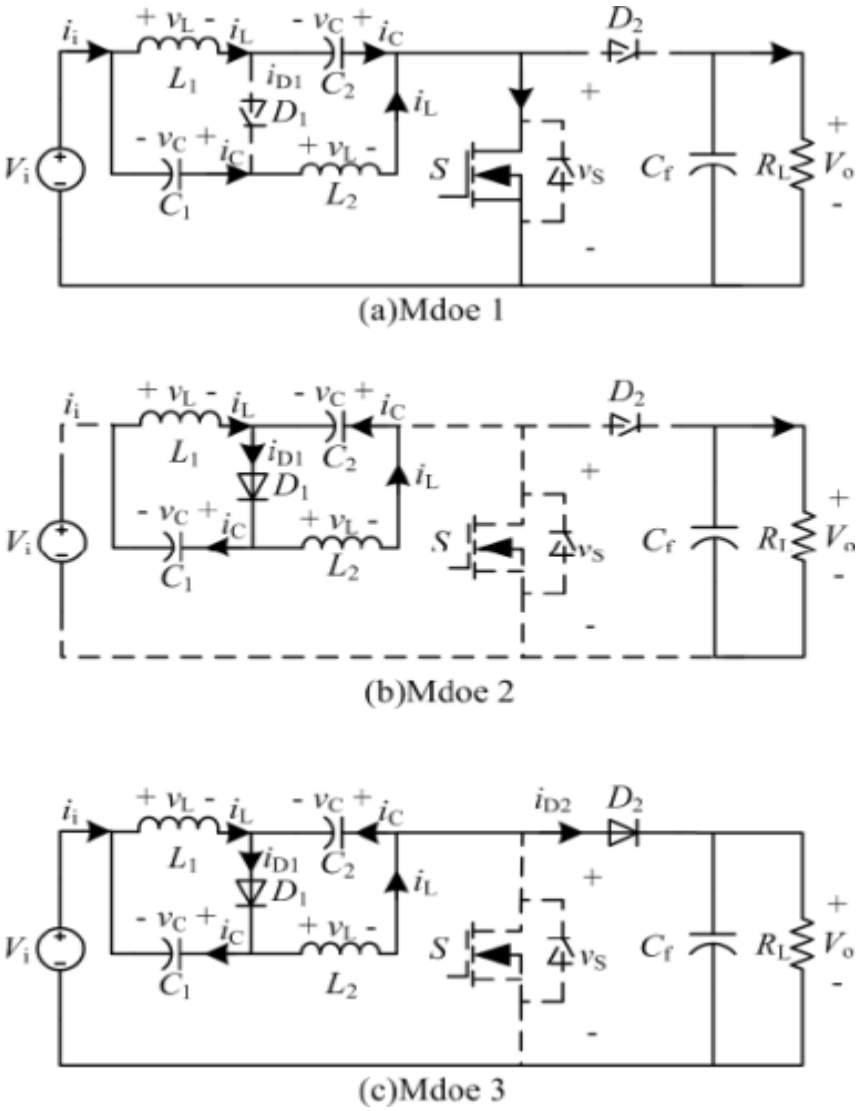
$$\begin{cases} i_i = i_L - i_C \\ i_{D1} = 2i_L - i_i \end{cases} \quad (2.14)$$

$$V_O = V_s = V_i + 2V_C \quad (2.15)$$

The period of operation of modes 1 and 2 is (1-D) T. the duration for mode 1 is DT.

Figure 16

Modes of Operation Modified Z-source Converter (Yang et al., 2014).



In addition using volt-second balance law on the inductors, we get the following:

$$(V_i + V_C)DT + (-V_C)(1 - D)T = 0 \quad (2.16)$$

Solving for V_c we get:

$$V_C = \frac{D}{1-2D} V_i \quad (2.17)$$

From (2.15) and (2.17) the equation of gain ratio of this converter can be written as:

$$G = \frac{V_O}{V_i} \qquad V_O = \frac{1}{1-2D} \quad (2.18)$$

Therefore:

$$G = \frac{1}{1-2D} \tag{2.19}$$

Table 2

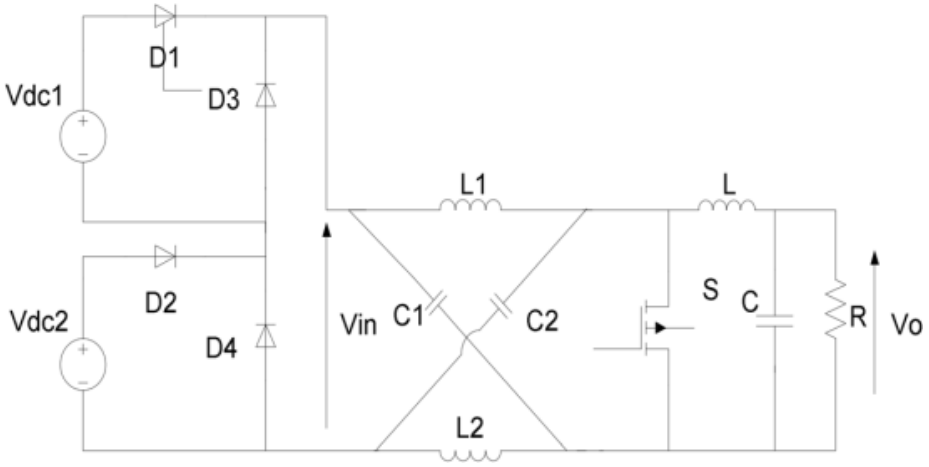
Comparison between Modified Z-source Converter and Traditional Z-source Converter (Yang et al., 2014).

Voltage	Modified z-source dc-dc converter	Traditional z-source dc-dc converter
V_o	$\frac{1}{1-2D}V_i$	$\frac{1-D}{1-2D}V_i$
V_C	$\frac{D}{1-2D}V_i = DV_O$	$\frac{1-D}{1-2D}V_i = V_o$
V_s	$\frac{1}{1-2D}V_i = V_O$	$\frac{1}{1-2D}V_i = \frac{1}{1-D}V_O$

Furthermore, for where there is more than one renewable energy source the dual input dc-dc z-source converter proposed by Sedaghati & Babaei (2016) is suitable. In this topology two sources can be connected to form a single system. Moreover, this proposed topology has four states of operation depending on whether the dc sources are active or not.

Figure 17

Dual Input Z-source Converter (Sedaghati & Babaei 2016).



State 1:

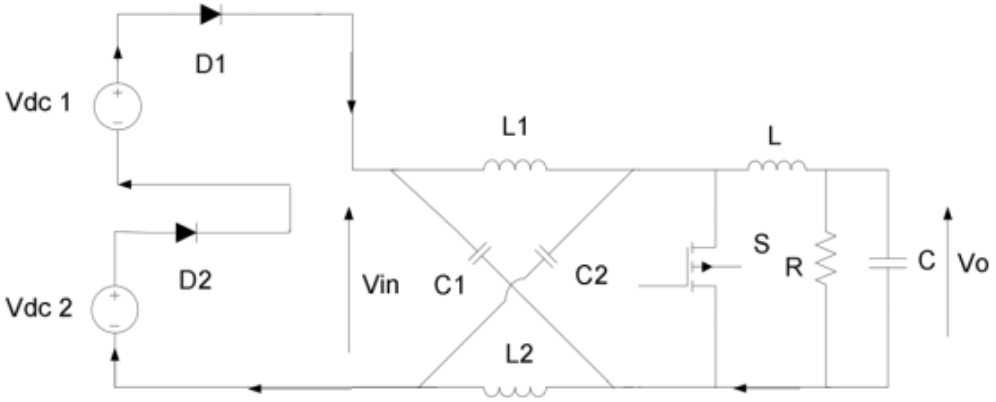
In this state the input voltage would be in series when both sources are active i.e. the voltage will be summed.

$$V_{in} = V_{dC1} + V_{dC2} \quad (2.20)$$

In addition in this mode the diodes D_1 and D_2 are forward biased while D_3 and D_4 are reverse biased, Meaning for the current to get to the z-sources network it needs to flow through D_1 and D_2.

Figure 18

State 1 Equivalent Circuit (Sedaghati & Babaei 2016).



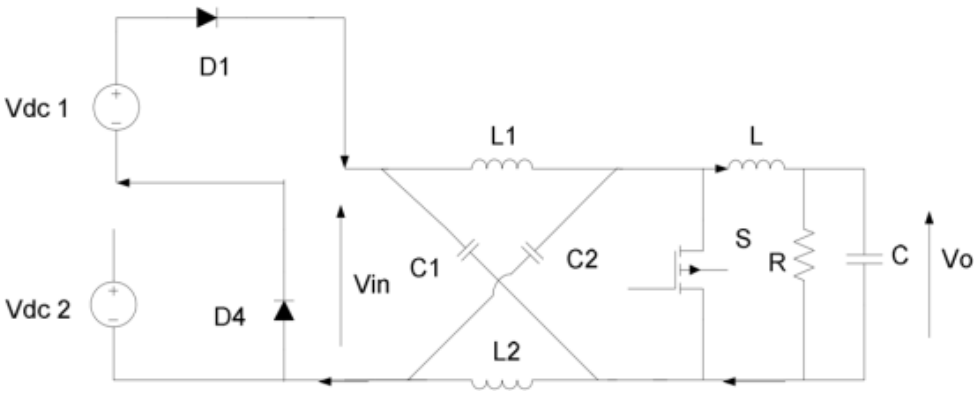
State 2:

In this state the first source is the sole source of energy supply to the converter. As shown in figure 19 when source 1 is in operation D_1 is forward biased while D_3 is reversed, which means that the current has to flow through D1 to get to the z-source network and the load.

$$V_{in} = V_{dC1} \quad (2.21)$$

Figure 19

State 2 Equivalent Circuit (Sedaghati & Babaei 2016).



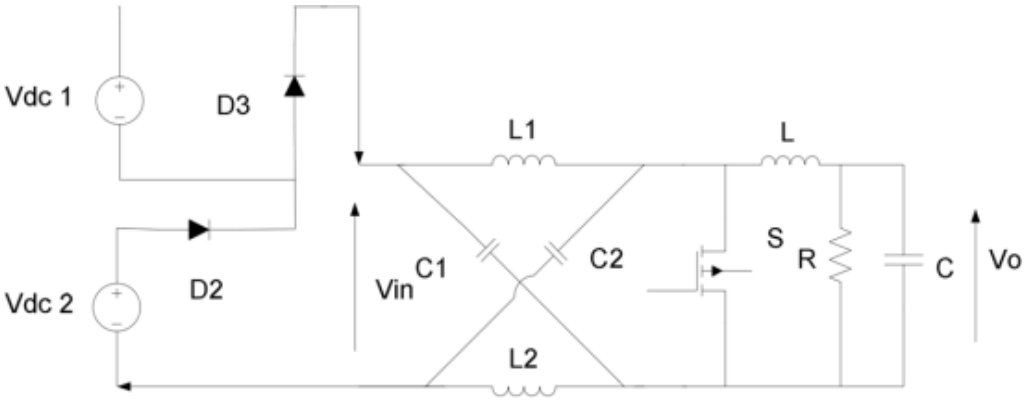
State 3:

In this state the second source supplies voltage to the converter while the first is cut off. When source 2 is active diode D2 is forward biased while D4 is reversed. The current in this state will pass through D3 when the first source is inactive as shown in figure 20.

$$V_{in} = V_{dc2} \tag{2.22}$$

Figure 20

State 3 Equivalent Circuit (Sedaghati & Babaei 2016).



State 4:

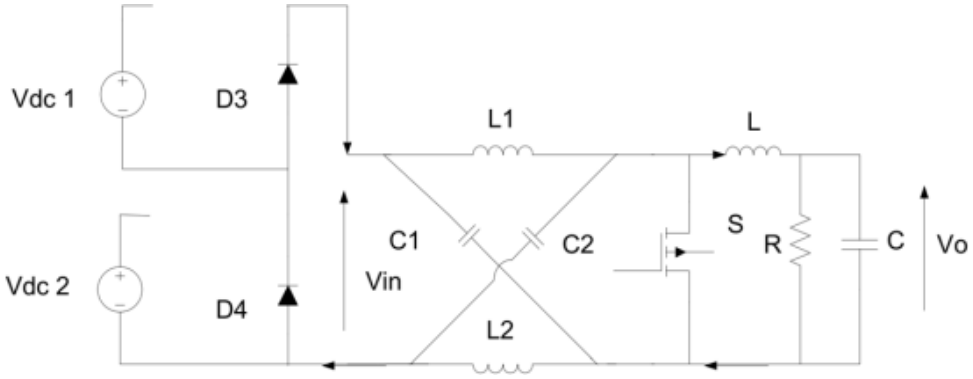
In this state the converter is inactive because both sources are disconnected, this however only lasts for a very short time. When both sources are disconnected D_1 and D_2

are turned off, leaving D_3 and D_4 as the sole which forces the current from the previous states to remain on the path provided.

In this state $V_{in} = 0$

Figure 21

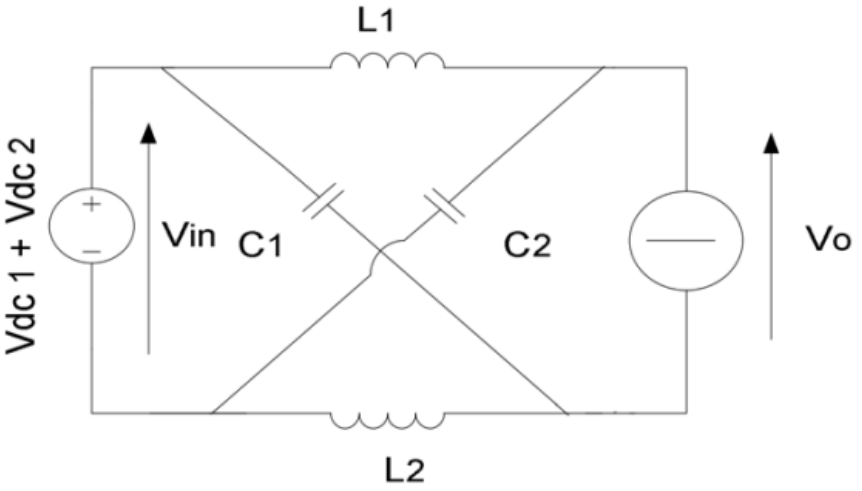
State 4 Equivalent Circuit (Sedaghati & Babaei 2016).



In the steady state analysis this converter operates in two modes. In the first mode the switch is in the off state while D_1 and D_2 are on. Furthermore, the capacitors will be charged while the inductor discharges to the load. Figure 22 shows the operation of mode 1.

Figure 22

Operation Mode 1 (Sedaghati & Babaei 2016).



When the switch is off (1-D)T: the following equations can be derived.

$V_{in} - V_{dC1} - V_{dC2} = 0$, $\mathrm{V_{in}} = \mathrm{V_{dC1}} + \mathrm{V_{dC2}}$ (2.23)

$\mathrm{V_C} - \mathrm{V_{in}} + \mathrm{V_L} = 0$ (2.24)

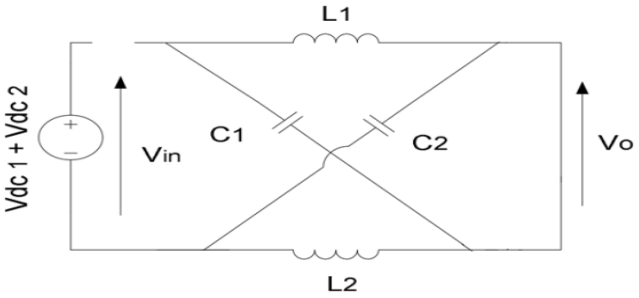
$V_o - V_{in} + 2V_L = 0$ (2.25)

Mode 2:

In this mode the switch is in the on state while D_1 and D_2 are off. In the first cycle capacitor will the energy store, in the second cycle they will recharge. In the case of the inductors store their energy in the first cycle, when it comes to the second cycle they start discharging the stored energy.

Figure 23

Operation Mode 2 (Sedaghati & Babaei 2016).



Resulting equations in this mode: when the switch is on (DT).

$$V_C = V_L \ , V_O = 0 \quad (2.26)$$

The voltage gain of this converter is:

$$\frac{V_O}{V_{dC1}+V_{dC2}} = \frac{1-D}{1-2D} \quad (2.27)$$

But

$$V_{dC1} + V_{dC2} = V_{in} \quad (2.28)$$

Therefore voltage gain is: $\frac{V_O}{V_{in}} = \frac{1-D}{1-2D}$ (2.29)

2.2 Quasi z-source dc-dc converter

Quasi-Z-Source converters originated from the step-up DC converter topology family. It can be accomplished in two ways: galvanically isolated or transformerless. The first example's architecture is comparable to that of a normal boost converter, and it may be used in solar applications as a maximum power point tracker. The converter might be utilized as a front-end voltage pre-regulator in fuel cell power systems and other applications with varying voltage at the input since it has a high efficiency even with a threefold gain input voltage. The quasi ZS DC-DC converter which is galvanically isolated and the high frequency transformer include an intermediate AC

connection that allows the needed input voltage gain to be adjusted simply by altering the turn ratio of the transformer. This transformer also functions as a galvanic isolation device in high-gain applications, which is useful in a variety of scenarios. In solar power systems, galvanic isolation is also required to minimize ground leakage currents and THD in the grid current. (Liivik et al., 2014).

Figure 24

Quasi z-source converter (Yang, et al., 2014).

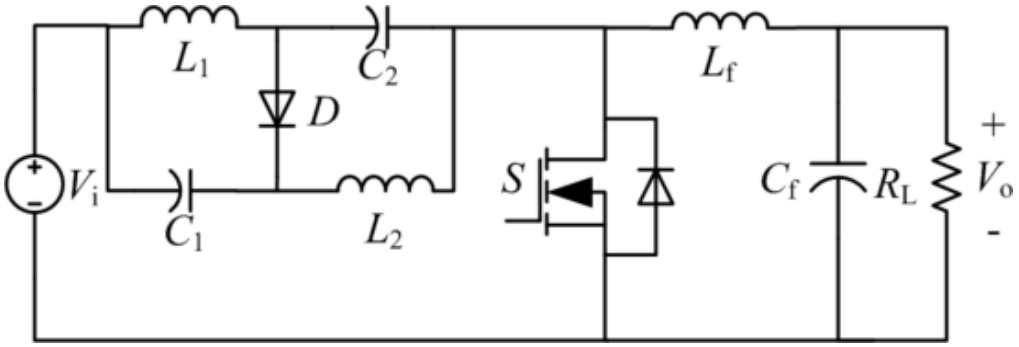
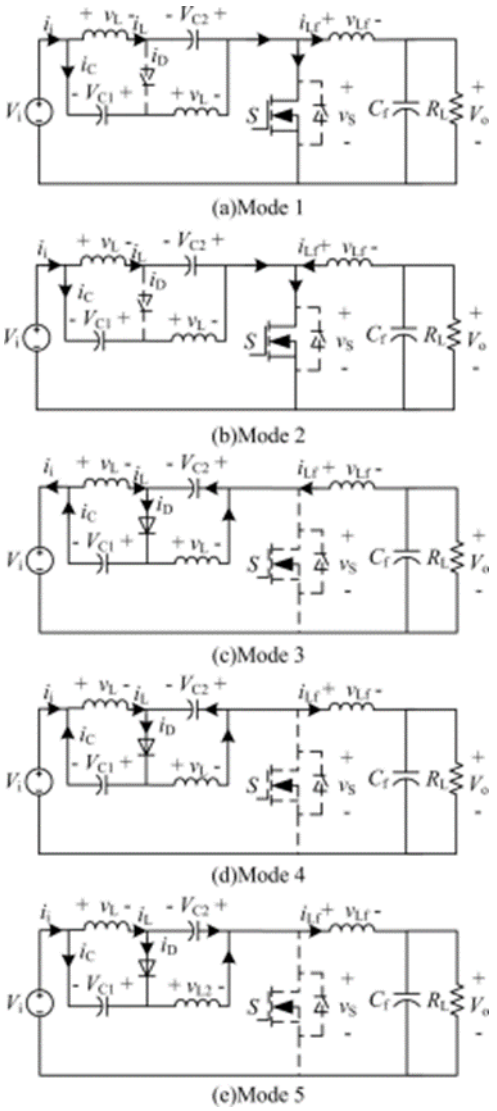


Figure 25

Modes of Operation of QZS Converter (Yang, et al., 2014).



Modes of Operation

First mode

As seen in Figure 25.a in this converter there are 3 voltage loops when diode D is off and switch S is active. Three voltage loops exist in the converter: capacitor C2 and voltage source V_i charge inductor L_1, capacitor C_1 and voltage source V_i charge inductor L_2, and the load discharge inductor L_f is. As a result, the inductor current i_L is positive and increasing linearly, whereas i_{Lf} is positive and dropping linearly. The equations

below are derived based solely on the assumption that the voltage of the switch is zero (Yang, et al., 2014).

$$V_L = V_i + V_C \tag{2.30}$$

$$V_{Lf} = -V_O \tag{2.31}$$

Second Mode

As presented in Figure. 25. b, diode D is turned off and switch S is turned on, but if switch S remains on after i_{Lf} goes to zero in mode 1, the inductor L_f is reverse-charged from capacitor C_f. i_{Lf} will be negative and rising in the opposite direction as a result. Equation (2.31) is also established in this approach (Yang, et al,. 2014).

Third mode

As displayed in Figure. 25(c), diode D is switched active while switch S is inactive, the reason being that the voltage source at the input is connected in series to the inductor L_f and impedance network, inductor L_f will discharge energy to the voltage source at the input if i_{Lf} is negative before switch S is active, and the capacitors of the impedance network. Meanwhile capacitors C_1 and C_2 are charged by the Inductors L_1 and L_2. As a result, the inductor currenti_L is linearly decreasing while i_{Lf} is increasing linearly. The following equations may be deduced based on this (Yang, et al., 2014).

$$V_L = -V_C \tag{2.32}$$

$$V_{LS} = V_S - V_O = V_i - 2V_C = -V_O \tag{2.33}$$

Fourth mode

As illustrated in Figure. 25(d), diode D is active as switch S is active, despite that the load and inductor L_f charge LDC impedance network and the voltage source V_i. L_1 and L_2 charge C_1 and C_2, respectively, simultaneously. As a consequence, i_{Lf} is positive and expanding linearly, but i_L is declining linearly. Eq (18) is found, from which the following equation is derived: (Yang, et al., 2014).

$$i_{Lf} = i_L - i_C \tag{2.34}$$

When current i_{Lf} surpasses currenti_L, according to (2.34), mode 4 terminates and current $i_C$becomes negative, leading in mode 5 (Yang, et al., 2014).

Fifth mode

From Figure. 24, like mode 4 the active or inactive states of switch S and diode D are identical. Capacitors C_1 and C_2 start to discharge to the inductor L_f and the load since the capacitor current $i_C$is negative, as previously indicated. Equations (2.33) and (2.34) have been created as well (Yang, et al,. 2014).

Diode D is inactive when switch S is active and it is turned on when switch S is turned off, according to the preceding analysis. When the active or inactive state of switch S changes, the voltage relationships change as well. As a consequence, the converter's operating mode can be reduced to two modes if either the active or inactive state of switch S or voltage relationship are taken into account. Furthermore, the source and load currents of the converter are both constant (Yang, et al., 2014).
There are two operating states while the switch is active, and three states when the switch is turned off, as seen in Figure.25 In steady state, the converter's major functioning modes are mode 1 (switch S is active) and mode 4 (switch S is inactive). Furthermore, because in mode 2 the current i_{Lf} is negative and somewhat constant, after mode 2 the converter will automatically switch to mode 3, meaning mode 3 will happen at the same time as mode 2. The status of the circuit parameters determines whether or not mode 5 will occur. As a result, the quasi-Z-source converter may operate in four different modes dependent on the circuit parameters. Figure 26 depicts the key waveforms of various operation situations, where V_g denotes the switch S driving signal (Yang, et al., 2014).

Case 1: In this situation, there are just two major operational modes (modes 1 and 4). Switch S turns off when inductor current i_{Lf} stays positive before, and the capacitor current i_C remains constant when switch S is off, as depicted in Figure. 26a (Yang, et al., 2014).

Case 2: In contrast to operating Case I, operating Case II inserts mode 5 between modes 4 and 1, resulting in a negative capacitor current i_C when switch S is in the active or inactive state as shown in Figure. 26 b (Yang, et al., 2014).

Case 3: After mode 1, mode 2 will occur and then mode 3 will follow by since current i_{Lf} may dip below zero when switch S is in the on-state. As illustrated in Figure. 26 c, operational instance 3 comprises modes 1, 2, 3, and 4 (Yang, et al., 2014).

Case 4: Modes 1 through 5 occur in operational condition 4 (Yang, et al., 2014).
As a result, when switch S is on, current i_{Lf}will be negative, and current $i_C$will be negative switch S is off, as shown in Figure. 26 d (Yang, et al., 2014).

In addition when the switch is in the on state the time duration is DT, when it is off the duration is (1-D)T. Using volt-balance second law on the inductor the equation below can be derived:

$$(\mathrm{V_i} + \mathrm{V_C})\mathrm{DT} + (-\mathrm{V_C})(1-\mathrm{D})\mathrm{T} = 0 \quad \mathrm{V_C}\frac{\mathrm{D}}{1-2\mathrm{D}}\mathrm{V_i} \tag{2.35}$$

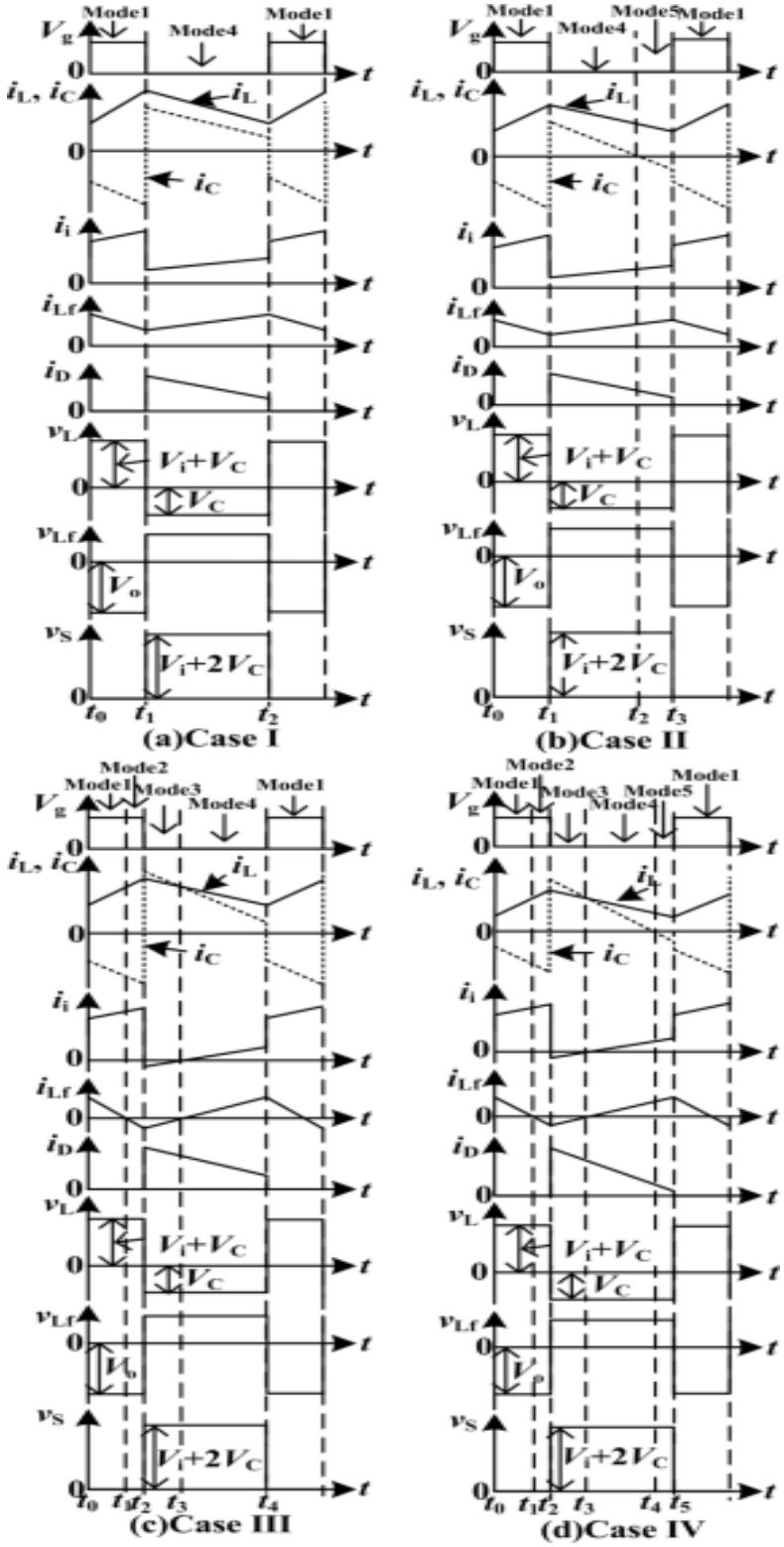
$$(-\mathrm{V_O})\mathrm{DT} + (\mathrm{V_i} + 2\mathrm{V_C} - \mathrm{V_O})(1-\mathrm{D})\mathrm{T} = 0 \tag{2.36}$$

From (2.35) and (2.36) the equation for the boost ratio of this converter can be written as:

$$\mathrm{G} = \frac{\mathrm{V_O}}{\mathrm{V_i}} \qquad \mathrm{G} = \frac{1-\mathrm{D}}{1-2\mathrm{D}} \tag{2.37}$$

Figure 26

Operation of Converter in four Cases (Yang, et al., 2014).

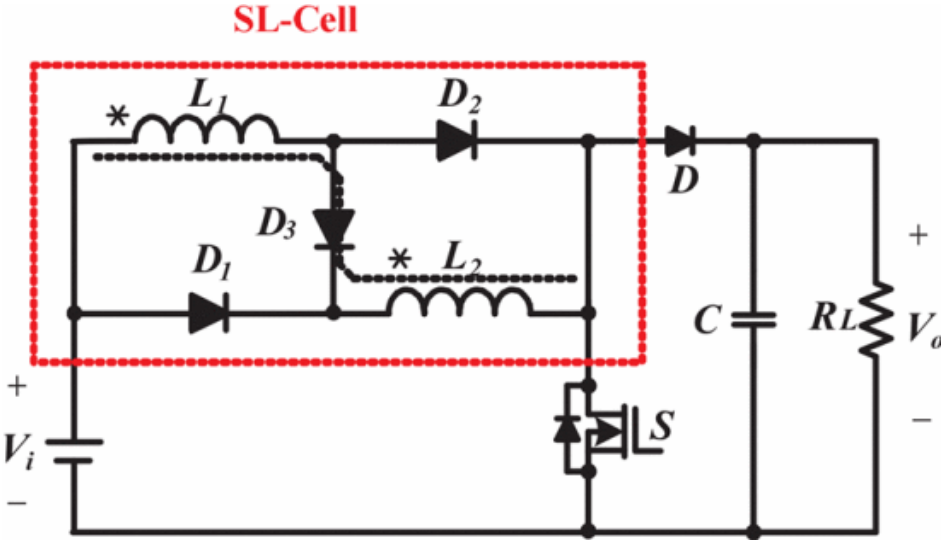


2.3 Switched inductor-based DC-DC converters

The dotted box represents the SL-cell, which may be used to substitute the inductor L in a standard Boost converter. The SL-cell consists of three diodes, as well as two identical inductors. The switch also determines the manner in which the inductors are connected i.e. they are parallel when it's active and in series when it's not. In the case of the diodes D_1 and D_2 are forward biased, D3 is reversed when it is active. When it is off the opposite of the above occurs
(He et al., 2014).

Figure 27

Switched Inductor-based DC-DC Converter (He et al., 2014).



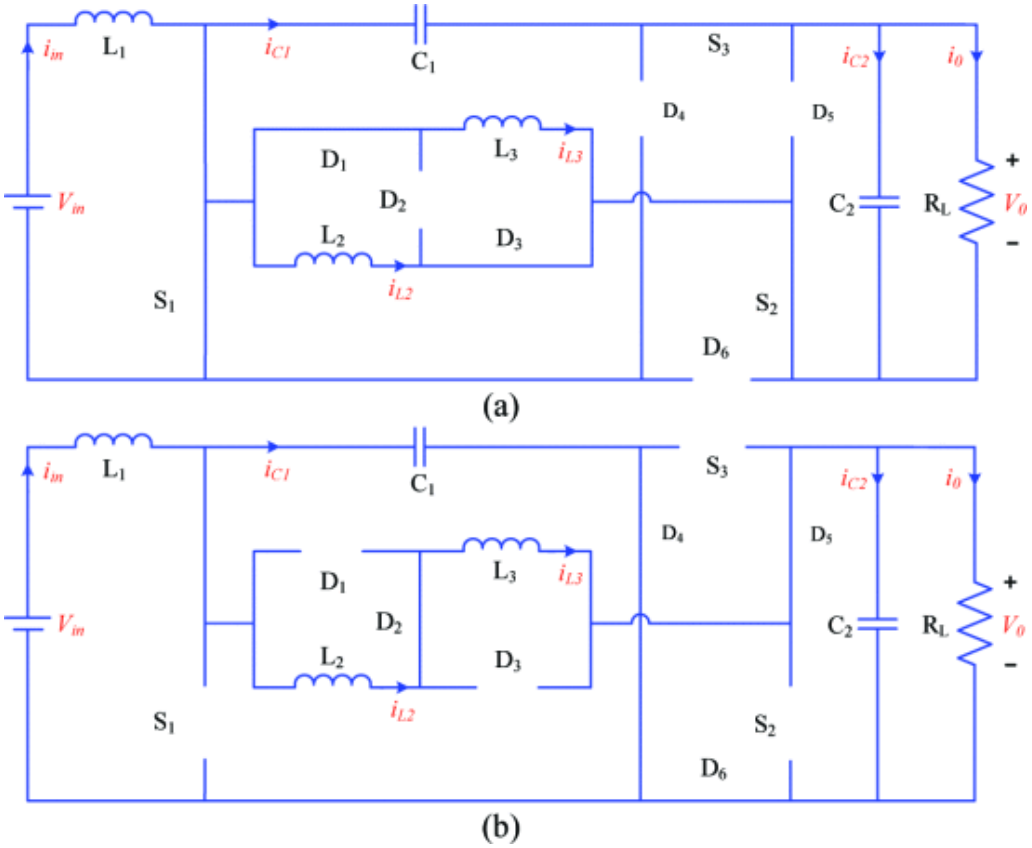
When paralleled to conventional boost converters, switched inductor converters provide benefits such as a low average current at the inductor, which aids in shrinking the size of a particular inductor. Furthermore, inductors in the converter with identical values act similarly, therefore they can be assimilated into a single magnetic core, decreasing the magnetic component size. In comparison to a boost topology, the voltage conversion ratio is greater. The SL-Boost, on the other hand, has serious flaws, such as a limited voltage gain and trouble with a 10-fold voltage gain. The switch being inactive means the voltage across it is equal to the output voltage, and a higher voltage stress is realizes across the switches with a large Rds (on) will result in a higher conduction loss.

When the output diode is switched off, the output voltage is the voltage across it. As a result, the issue of reverse recovery may become serious. (He et al., 2014).

A low input voltage may be transformed into a higher output voltage using the S-L boost DC-DC converter. The boost converter is made up of 3 inductors, two capacitors, six diodes and 3 active switches. Controlling the converter's controlled switches, which must work at a high frequency, may be done with MOSFETs and IGBTs. Because all three switches are powered by the same signal, the converter may be operated with just one control signal. In order to attain a greater boost ratio it is vital to adjust duty cycle of the switches, with this we can improve the output voltage. In addition the pwm technique can be employed to control the switching process of the switches. The switched inductor based converter has two operational modes when the current at the inductor is constant as shown in the schematics below. In this topology when the switches are operating the diodes are reverse while to D_1 and D_3 are forward biased to avoid a back flow (Shaw & Sahoo, 2018).

Figure 28

Modes of Operation (Shaw & Sahoo, 2018).



Note: (a) is mode 1. (b) Is mode 2.

The energy stored by the inductors in mode 1 i.e. when the switches are on can be derived below as:

$$V_{L1} = V_{in} \quad (2.38)$$

$$V_{L2} = V_{L3} = (V_{C1} + V_O) \quad (2.39)$$

In mode 2 the switches are turned off, Diodes D_2, D_4, D_5 and D_6 are forward biased while D_1 and D_3 are reversed. In addition the energy stored by the inductors can be written as:

$$V_{L1} = (V_{in} - V_{C1}) \quad (2.40)$$

$$V_{L2} = V_{L3} = \frac{1}{2}(V_{C1} - V_O) \quad (2.41)$$

Using volt-second law on L_1 we get:

$$(V_{in})DT + (V_{in} - V_{C1})(1 - D)T = 0 \quad (2.42)$$

By solving for V_{c1} we get:

$$V_{C1} = \frac{V_{in}}{1-D} \quad (2.43)$$

Using volt-second law on L_2 we get:

$$(V_{C1} + V_O)DT + \frac{1}{2}(V_{C1} - V_0)(1 - D)T = 0 \quad (2.44)$$

The voltage of this converter can be derived by substituting

$$G = \frac{V_O}{V_{in}} = \frac{(1+D)}{(1-D)(1-3D)} \quad (2.45)$$

2.4 Switched capacitor DC-DC converters

In this topology capacitors are used as a voltage source in the same way as the switched-inductor converter where inductors are used. High voltage gain can be accomplished by switching the capacitors from series to parallel connection. The topology of the switched capacitor converter is depicted below, with the switched capacitor cell represented in the box with dotted lines being used. The connection of the capacitors can be changed by adjusting the switch's operation state which results in a high voltage conversion ratio (He et al,. 2014).

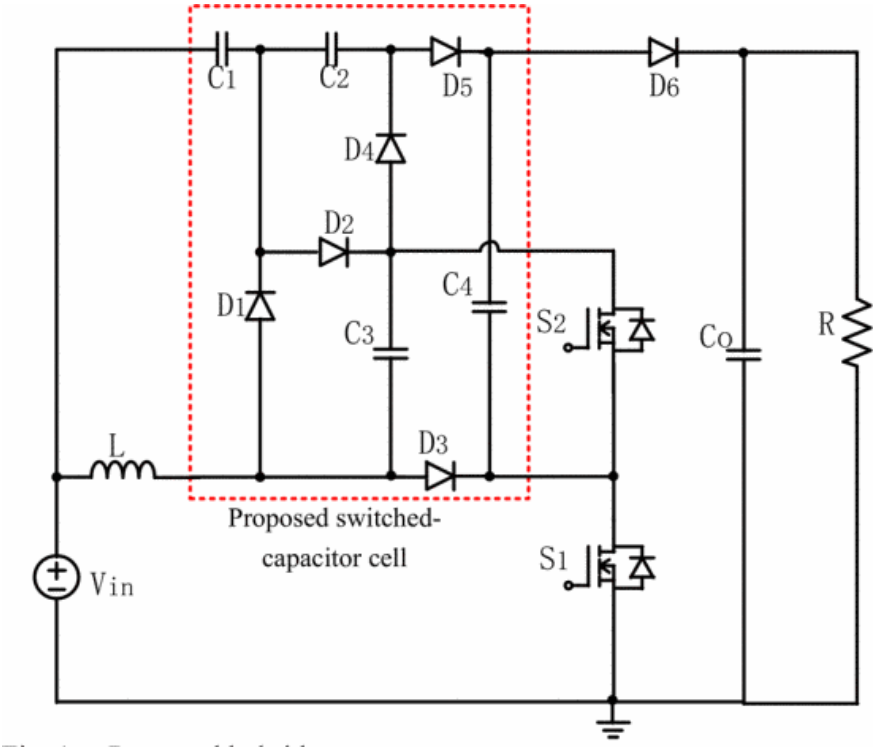
The following are some benefits of using this converter. They offer tiny size, low weight, great power density, excellent efficiency relative to all traditional power supplies

in the small values of watts, strength, and consistent input current, among other benefits. These qualities, together with the lack of magnetic devices, alleviate the EMI issues that inductors produce. The power device's voltage stress is rather low. The voltage conversion ratio is twice as big when compared to a Boost converter. All capacitors are capable of achieving self-voltage balancing. However, the SC-Boost has the following drawbacks: voltage gain is restricted, and the 10x voltage gain ratio is difficult to handle. Furthermore, the inductor size could increase because the current of the inductor and the currents at the input are the same. The stress on the switches is considerable due to the current and this might result in more conduction loss. Every switching mode power converter's primary goal is to deliver a consistent AC or DC output voltage to the load, regardless of voltage input or variations in load. A component of control must be incorporated into the energy transmission process in order for the converter to change its topology gradually and the periods of the switching of said topologies be modified for regulatory reasons.

(He et al., 2014).

Figure 29

Switched Capacitor DC-DC Converter Topology (Chen et al., 2016).



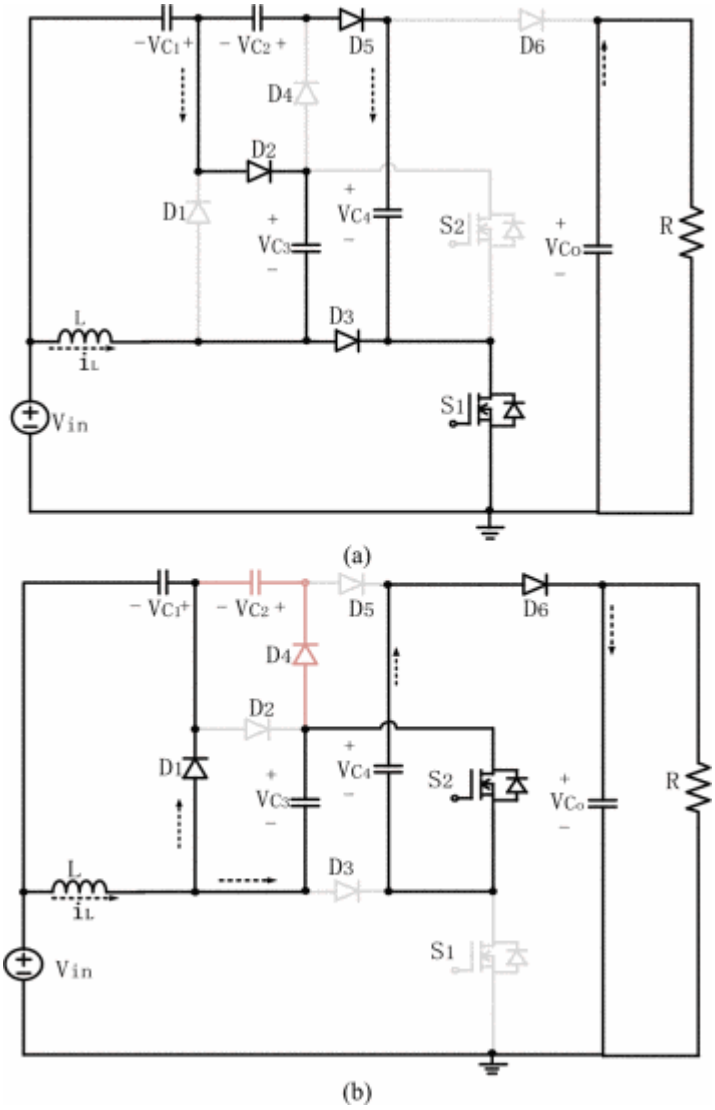
This converter operation in two modes.

Mode 1: when S_1 is on, S2 is off.

When S_1 is on and S_2 is off, the inductor is charge by the line voltage. C_3 is charged by the line in series with C_1 while C_4 is charged by the line in series with C_1 and C_2. During this time C_1 and C_2 will be discharging (Chen et al., 2016).

Figure 30

Modes of Operation (Chen et al., 2016).



Note: (a) S_1 is active while S_2 is inactive. (b) S_1 is inactive while S_2 is active

The following equation can be derived from figure 30 a.

$$V_{in} - V_L = 0 \quad (2.46)$$

$$V_{in} + V_{C1} - V_{C3} = 0 \quad (2.47)$$

$$V_{in} + V_{C1} + V_{C2} - V_{C4} = 0 \quad (2.48)$$

Mode 2: S_1 is inactive, S_2 is active.

When S_2 is turned on C_3 charges C_2. C_1 and C_2 are charged, meanwhile V_{in} in series with the inductor, C_3 and C_4 transfer energy to the load.

The following equation can be derived from figure 30 b.

$$V_L = V_{C1} \quad (2.49)$$

$$V_{C3} = V_{C2} \quad (2.50)$$

$$V_{in} = V_L - V_{C3} - V_{C4} + V_O \quad (2.51)$$

Making use of equations from (2.46) – (2.51) the voltage across the capacitors can we written as:

$$V_{C1} = \frac{V_O}{4} - V_{in}, \quad V_{C2} = V_{C3} = \frac{V_O}{4}, \quad V_{C4} = \frac{V_O}{2} \quad (2.52)$$

Volt-second balance law on the inductor gives:

$$DTV_{in} + (1 - D)(V_{in} + V_{C3} + V_{C4} - V_O)T = 0 \quad (2.53)$$

The boost ratio can be expressed as:

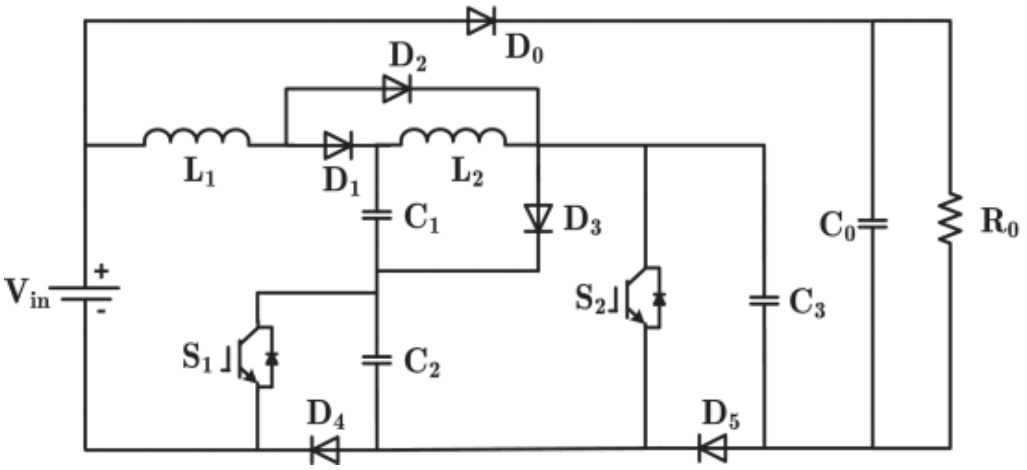
$$G = \frac{V_O}{V_{in}} = \frac{4}{1-D} \quad (2.54)$$

2.5 Switched inductor capacitor network based converters

Diodes, inductors, capacitors, and other components make up a Switched inductor and capacitor based network converter. In a switched inductor configuration, the diodes and inductors are coupled. This converter's ability to boost voltage has to do with the arrangement in the terminal at the output; this terminal is made up of the capacitors and diodes, which boosts the converter's voltage. Utilizing a single switch rather than several switches simplifies control and reduces control complexity. Capacitors 1 and 2 are equal (Kumar & Kumar, 2021).

Figure 31

Switched Inductor Capacitor Network Based Converter (Kumar & Kumar, 2021).



In certain ways, the multiple topologies of the DC-DC converter are adaptable. They do, however, operate differently and need a varied amount of circuit components and switches. When compared to some of the existing topologies, the voltage gain of the provided topology is found to be greater. The voltage gain of various converters is compared with changing duty cycles. The voltage gain of the switched inductor presented for a certain duty cycle is significantly larger than that of several previously established for DC-DC topologies with high gain. (Kumar & Kumar, 2021).

Mode 1: $T_0 < t < T_1$

This is the comparable circuit for this mode. When the switches S1 and 2 are switched on, positive voltage is applied to diodes D_0 and D_2, causing them to be forward biased. Meanwhile, the diodes D_1, D_3, D_4, and D_5 are reverse biased since they have a negative voltage across them. Following that, the source voltage V_{in} charges L_1 as well as capacitor C_2 through switches S_1, S_2 and diode D_2. L_2 is also charged through capacitor C_1, capacitor C_2, and switch S_2. Inductors store energy as the currents in the inductori_{L1} and i_{L2}increase linearly. The energy from the source V_{in} and capacitor C_3 is likewise discharged into the load through diode D_0 and switches S_1, S_2. The voltage equations are used in this mode (Chauhan, et al., 2018).

Figure 32

Operational Waveform (Kumar & Kumar, 2021).

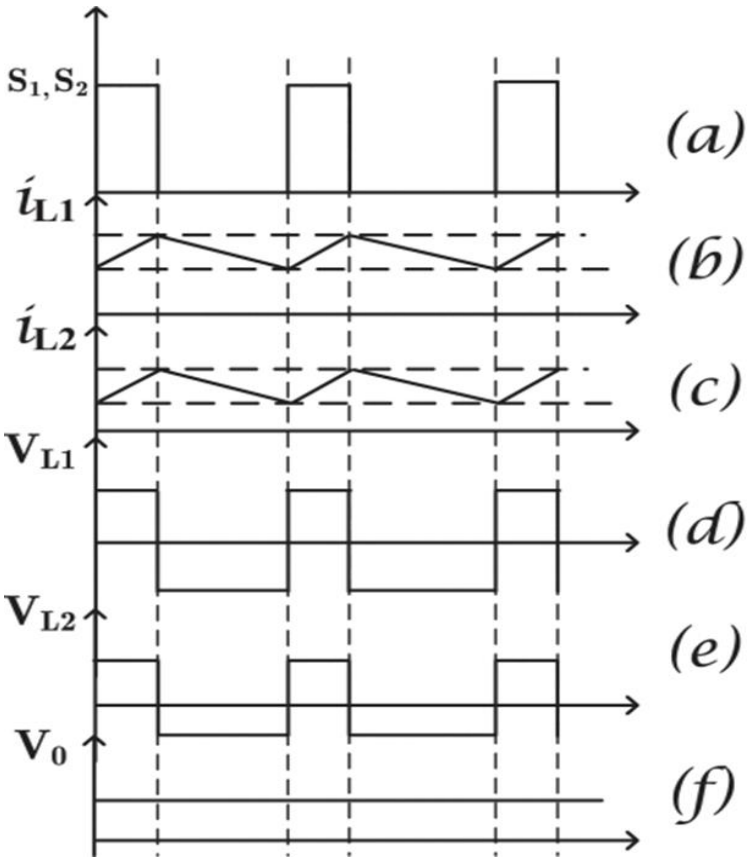
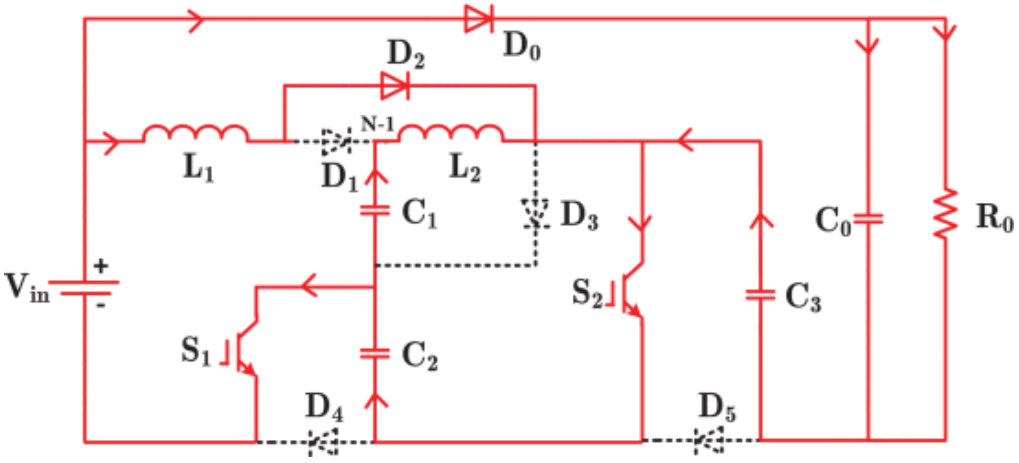


Figure 33

Equivalent Circuit for Mode 1 (Chauhan, et al., 2018).



$$V_{in} - V_0 + V_{C3} + V_{C2} = 0 \quad (2.55)$$

$$V_{C1} + V_{L2} - V_{C2} = 0 \quad (2.64)$$

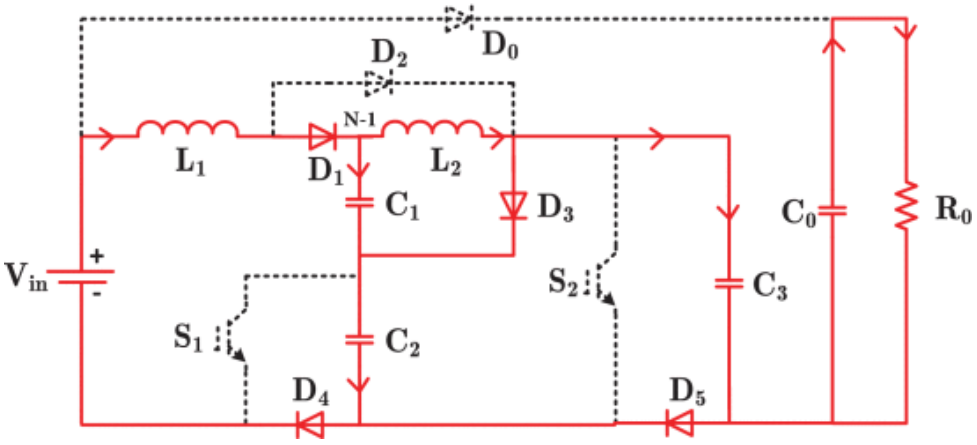
$$V_{in} - V_{L1} + V_{C2} = 0 \quad (2.57)$$

Mode 2: $T_1 < t < T_2$

The analogous circuit for this mode is shown in the diagram below. Switches S_1 and S_2 are in the off state in this mode. As a consequence, the forward biased diodes D_4 and D_5 are used. Furthermore, as the polarity of inductor L_1 and L_2 changes, negative voltage is applied to diodes D_0 and D_2, while positive voltage is applied to diode D_1. Following that, the inductor L_1 and L_2 discharge. Through diodes D_4 and D_5, the inductor L_1 charges the capacitors C_2 and C_3. Similarly, inductor L_2 charges capacitors C_1 and D_3. Furthermore, by discharging into the load, the capacitor C_0 maintains a constant voltage across the load (Chauhan, et al., 2018).

Figure 34

Equivalent Circuit for Mode 2 (Chauhan, et al., 2018).



$$V_{in} - V_{L1} + V_{C1} - V_{C2} = 0 \quad (2.58)$$

$$V_{L2} = -V_{C1} \quad (2.59)$$

$$V_{C2} = V_{C3} \quad (2.60)$$

According to the energy conservation law the following can be written for L_2:

$$\int_0^{DT} V_{L2}\,dt + \int_{DT}^{T} V_{L2}\,dt = 0 \quad (2.61)$$

Sustituting in (2.58) and (2.61) we get:

$$D(-V_{C1} + V_{C2}) + (1 - D)(-V_{C1}) = 0 \quad (2.62)$$

$$V_{C1} = DV_{C2} \quad (2.63)$$

Applying energy conservation law on L_1 we get:

$$\int_0^{DT} V_{L1}\,dt + \int_{DT}^{T} V_{L1}\,dt = 0 \quad (2.64)$$

$$D(V_{in} + V_{C2}) + (1 - D)(V_{in} + V_{C1} - V_{C2}) = 0 \quad (2.65)$$

Solving for V_{C2} we get:

$$V_{C2} = \frac{1}{1-3D-D^2} V_{in} \quad (2.66)$$

Substituting V_{C1} and V_{C2} in (2.55) the V_O can be derived as:

$$V_O = \frac{3-3D-D^2}{1-3D-D^2} V_{in} \quad (2.67)$$

The voltage of this converter can be written as:

$$G = \frac{V_O}{V_{in}} = \frac{3-3D-D^2}{1-3D-D^2} \quad (2.68)$$

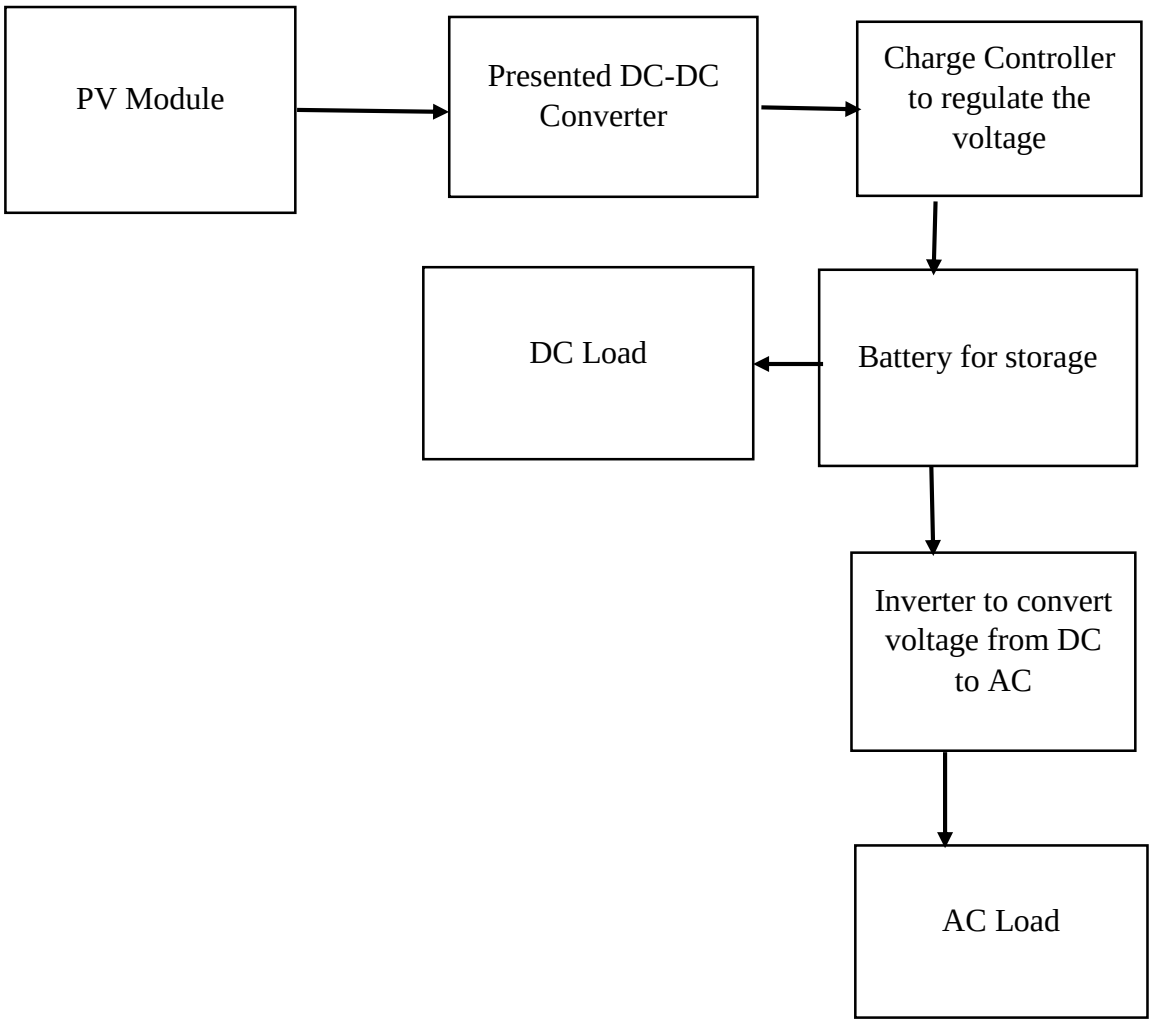
2.6 Summary

The boosting capability of the z-source is limited and it is prone to inrush current. The quasi z-source inverter at higher modulation indexes cannot produce high voltage gains. Due to inductor behavior during discharge, semiconductor switches in Switched inductor converters are subjected to high voltage stress, while Switched capacitor converters have a large number of components for better voltage gain.

CHAPTER 3

Presented Converter and Results from Simulation

The block diagram below shows how the presented converter fits in a system.



3.0 Overview

The circuit of the presented topology in figure 35 shows that the presented topology contains two networks. The modified quasi Z-Source circuit contains 9 components namely S_1, L_1 and L_2, D_1, D_2, and D_3, C_1, C_2, and C_3. The switched capacitor network consists of switch S_2, diode D_4 and capacitor C_4. D_5 is connected to the positive end of the voltage at the input and output to avoid back flow and C_f is the capacitor at

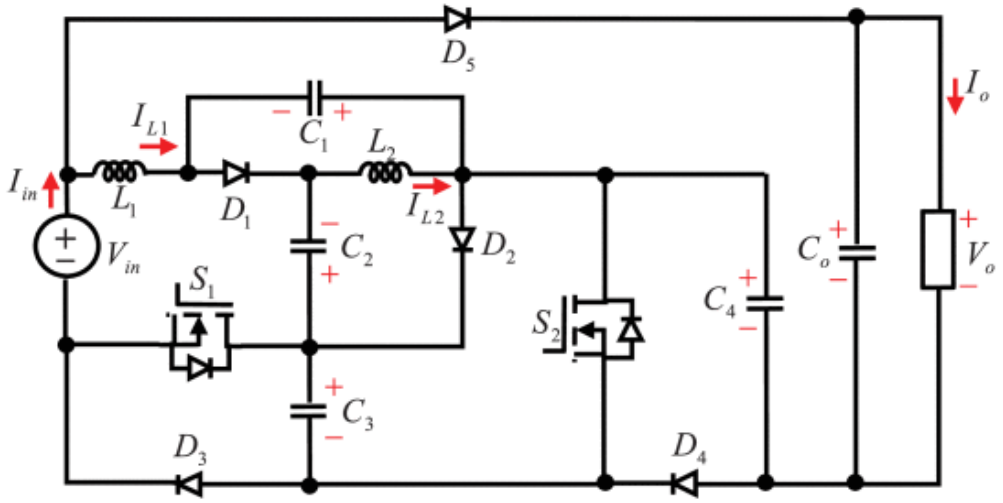
the output, thus making it a total of 14 components. Furthermore, the presented converter has a boost ratio of over 6 times the input at a duty cycle of 20%.

3.1 Presented Topology

Circuit analysis and operation modes of the presented converter as presented in figures 35 and 36 will be discussed in detail below.

Figure 35

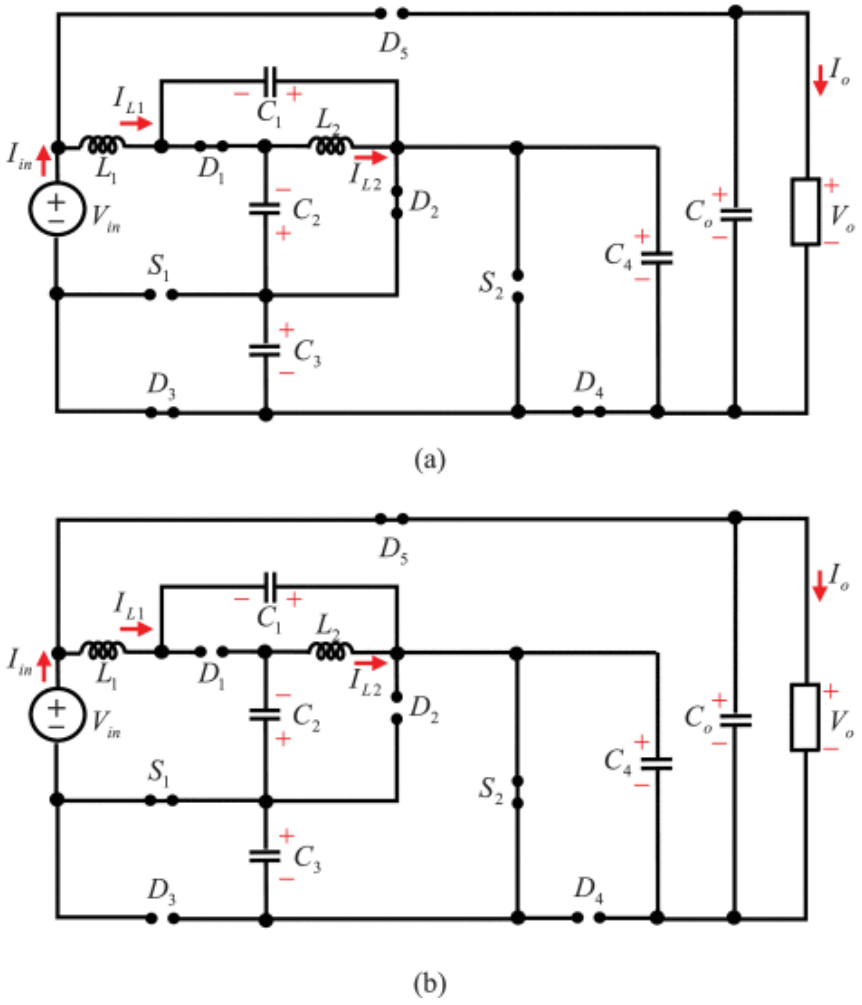
Presented Topology (Meinagh et al., 2019).



The presented converter operates in two modes as shown below in figure 36 a&b. Details of the modes of operation will be shown subsequently in the following pages.

Figure 36

Modes of Operation (Meinagh et al., 2019).



Mode 1: $t_0 - t_1$

This mode occurs when the switches are turned off and D_5 is reversed biased, which as a result will leave the rest of the diodes in the forward biased position. Also in this mode when C_1, C_3 and C_4 are charging, C_2 and the inductors will be discharging simultaneously.

The following equations can be derive from operation mode 1

Using KVL in the loop enclosing V_{in}, L_1, C_2 and C_3.

$$-V_{in} + V_{L1} - V_{C2} + V_{C3} = 0 \quad V_{L1} = V_{IN} + V_{C2} - V_{C3} \tag{3.0}$$

Using KVL in the loop enclosing C_3 and C_4:

$$V_{C3} - V_{C4} = 0 \quad \therefore \quad V_{C3} = V_{C4} \tag{3.1}$$

Using KVL in the loop enclosing L_2 and C_2:

$$V_{L2} + V_{C2} = 0 \quad \therefore V_{L2} = -V_{C2} \tag{3.2}$$

$$V_{C1} - V_{C2} = 0 \quad V_{C1} = V_{C2} \tag{3.3}$$

$$V_{S1} + V_{C3} = 0 \quad V_{S1} = -V_{C3} \tag{3.4}$$

Using KVL in the loop enclosing Vin, D_5 and Vo:

$$V_{IN} - V_{D5} - V_O = 0 \quad V_{D5} = V_{IN} - V_O \tag{3.5}$$

$$V_{S2} + V_{C4} = 0 \quad V_{S2} = -V_{C4} \tag{3.6}$$

Now for the currents we have the following:

$$i_{IN} - i_{L1} = 0 \quad i_{IN} = i_{L1} \tag{3.7}$$

$$i_{C1} + i_{C2} - i_{L2} + i_{L1} = 0 \quad i_{c1} + i_{c2} = i_{l2} - i_{l1} \tag{3.8}$$

$$i_{C3} + i_{C4} - i_{L1} = 0 \quad i_{C3} + i_{C4} = i_{L1} \tag{3.9}$$

Where V_{D5} is the voltage across Diode 5. V_{in} is the voltage at the input and V_O is the voltage at the output.

Note: V_{L1} is the voltage across the inductor L_1. V_{L2} voltages across the inductor L_2. i_{L1} is the current through L_1. i_{L2} is the current through L_2. V_{C1} is the voltages across capacitor C_1. V_{C2} is the voltages across capacitor C_2.V_{C3} is the voltages across capacitor C_3.V_{C4} is the voltages across capacitor C_4. i_{C1} is the current that flows through C_1. i_{C2} is the current that flows through C_2. i_{C3} is the current that flows through C_3 . i_{C4} is the current that flows through C_4 .V_{S1} is the voltages across S_1 .V_{S2} show the voltages across the switch S_2. I_{in} is the input current.

Mode 2: $t_1 - t_2$

In this mode, the switches are active i.e. they are on and D_5 is forward biased and allowed to operate while D_1, D_2, D_3 and D_4 are reversed biased. This as a result will make C_1, C_3 and C_4 discharge while L_1, L_2 and C_2, is also charging. In this mode the following equations can be deduced for the voltages and current.

Using KVL in the loop enclosing C_3, C_2 and L_2:

$$V_{C3} - V_{C2} - V_{L2} = 0 \quad V_{L2} = V_{C3} - V_{C2} \tag{3.10}$$

$$V_{IN} + V_{C3} + V_{C4} - V_O = 0 \quad V_O = V_{IN} + V_{C3} + V_{C4} \tag{3.11}$$

For the loop enclosing V_{IN}, C_3, C_1 and L_1 when KVL is applied the following can be deduced:

$V_{IN} + V_{C3} + V_{C1} - V_{L1} = 0 \qquad V_{L1} = V_{IN} + V_{C3} + V_{C1}$ (3.12)

$I_{IN} - I_O - I_{L1} = 0 \quad I_{L1} = I_{IN} - I_O$ (3.13)

$i_{C1} + I_{L1} = 0 \qquad i_{C1} = -I_{L1}$ (3.14)

$i_{C2} - I_{L2} = 0 \quad i_{C2} = I_{L2}$ (3.15)

$-I_{IN} - I_{L2} - i_{C3} = 0 \qquad i_{C3} = -I_{IN} - I_{L2}$ (3.16)

$I_{L1} - I_{IN} - i_{C4} = 0 \quad i_{C4} = I_{L1} - I_{IN}$ (3.17)

Voltages across the semiconductors are:

$V_{C2} - V_{C1} - V_{C3} - V_{D1} = 0 \quad \therefore V_{D1} = V_{C2} - V_{C1} - V_{C3}$

(3.18)

$V_{D2} = V_{D3} = -V_{C3}$ (3.19)

$V_{D4} + V_{C4} = 0$

(3.20)

Where V_{D1}, V_{D2}, V_{D3} and V_{D4} represent the voltages across the diodes.

3.2 Steady state analysis of the presented topology

This analysis shows the switching process of the switches using Pwm. The Switches have similar gate pulses. Using the voltage balance law on the inductors for the duration of a single switch cycle. In the following equations below we show how the equation for the voltages across the inductor and capacitor are derived. The equations for input voltage, output voltage and voltage are also derived.

Switching period T= $T_{ON} + T_{OFF}$ (3.21)

Duty cycle D = $\frac{T_{ON}}{T}$ (3.22)

When the switch is off i.e. duringT_{OFF}: from equation (3.21) $T_{OFF} = T - T_{ON}$

But $T_{ON} = DT$ therefore $T_{OFF} = T - DT$ = (1-D) T (3.23)

$V_{L1ON} + V_{L1OFF} = 0$ (3.24)

$$\begin{cases} (V_{IN} + V_{C3} + V_{C1})DT + (V_{IN} + V_{C2} - V_{C3})(1-D)T = 0 \\ V_{IN} + V_{C3} + V_{C1})D + (V_{IN} + V_{C2} - V_{C3})(1-D) = 0 \\ V_{C3} + V_{C1}D + V_{IN} + V_{C2} - V_{C3} - V_{C2}D + V_{C3}D = 0 \end{cases} \quad (3.25)$$

$V_{C1} = V_{C2}$ Therefore

$V_{IN} + V_{C2} - V_{C3} + 2V_{C3}D = 0$ (3.26)

$V_{IN} = -V_{C2} + V_{C3} - 2V_{C3}D$ (3.27)

For L_2:

$$V_{L2ON} + V_{L2OFF} = 0 \quad (3.28)$$

$$\begin{cases} (V_{C3} - V_{C2})DT + (-V_{C2})(1-D)T = 0 \\ (V_{C3} - V_{C2})D - V_{C2}(1-D) = 0 \\ V_{C3}D - V_{C2}D - V_{C2} + V_{C2}D = 0 \end{cases} \quad (3.29)$$

$$V_{C3}D - V_{C2} = 0 \quad (3.30)$$

Substituting equation (3.30) in (3.27):

$$\begin{cases} V_{IN} = -(V_{C3}D + V_{C3} - 2V_{C3}D) \\ V_{IN} = V_{C3} - 3V_{C3}D \end{cases} \quad (3.31)$$

$$\mathrm{V_{IN}} = (1 - 3\mathrm{D})\mathrm{V_{C3}} \quad (3.32)$$

From (3.30) making V_{c3} the subject of formula:

$$\mathrm{V_{IN}} = -\mathrm{V_{C2}} + \frac{\mathrm{V_{C2}}}{\mathrm{D}} - 2\left(\frac{\mathrm{V_{C2}}}{\mathrm{D}}\right)\mathrm{D} \quad (3.33)$$

$$\mathrm{V_{IN}} = -\mathrm{V_{C2}} + \frac{\mathrm{V_{C2}}}{\mathrm{D}} - 2\mathrm{V_{C2}} \quad (3.34)$$

$$\mathrm{V_{IN}D} = \mathrm{V_{C2}} - 3\mathrm{V_{C2}D} \quad (3.35)$$

$$V_{C2} = \frac{D}{1-3D} V_{IN} \quad (3.36)$$

From (3.30)

$$\mathrm{V_{C2}} = \mathrm{V_{C3}D}$$

Substituting in (3.32):

$$\mathrm{V_{IN}} = -\mathrm{V_{C3}D} + \mathrm{V_{C3}} - 2\mathrm{V_{C3}D} \quad (3.37)$$

$$\mathrm{V_{IN}} = \mathrm{V_{C3}} - 3\mathrm{V_{C3}D} \quad \mathrm{V_{IN}} = (1 - 3\mathrm{D})\mathrm{V_{C3}} \quad (3.38)$$

$$\mathrm{V_{C3}} = \frac{\mathrm{V_{IN}}}{1-3\mathrm{D}} \qquad \mathrm{V_{C3}} = \frac{1}{1-3\mathrm{D}}\mathrm{V_{IN}} \quad (3.39)$$

For the output voltage:

$$\mathrm{V_O} = \mathrm{V_{IN}} + \mathrm{V_{C3}} + \mathrm{V_{C4}} \quad (3.40)$$

From (3.1): $\mathrm{V_{C3}} = \mathrm{V_{C4}}$

From (3.32): $\mathrm{V_{IN}} = (1 - 3\mathrm{D})\mathrm{V_{C3}}$

Substituting (3.1) and (3.32) in (3.40):

$$\mathrm{V_O} = (1 - 3\mathrm{D})\mathrm{V_{C3}} + 2\mathrm{V_{C3}} \quad (3.41)$$

$$\mathrm{V_0} = 3\mathrm{V_{C3}} - 3\mathrm{V_{C3}D} \quad \mathrm{V_O} = (3 - 3\mathrm{D})\mathrm{V_{C3}} \quad (3.42)$$

$$\mathrm{V_O} = 3(1 - \mathrm{D})\mathrm{V_{C3}} \quad (3.43)$$

The voltage gain can be derived as follows:

$$G = \frac{V_O}{V_{IN}} \tag{3.44}$$

$$G = \frac{3-3DV_{C3}}{1-3DV_{C3}} \qquad G = \frac{3(1-D)}{1-3D} \tag{3.45}$$

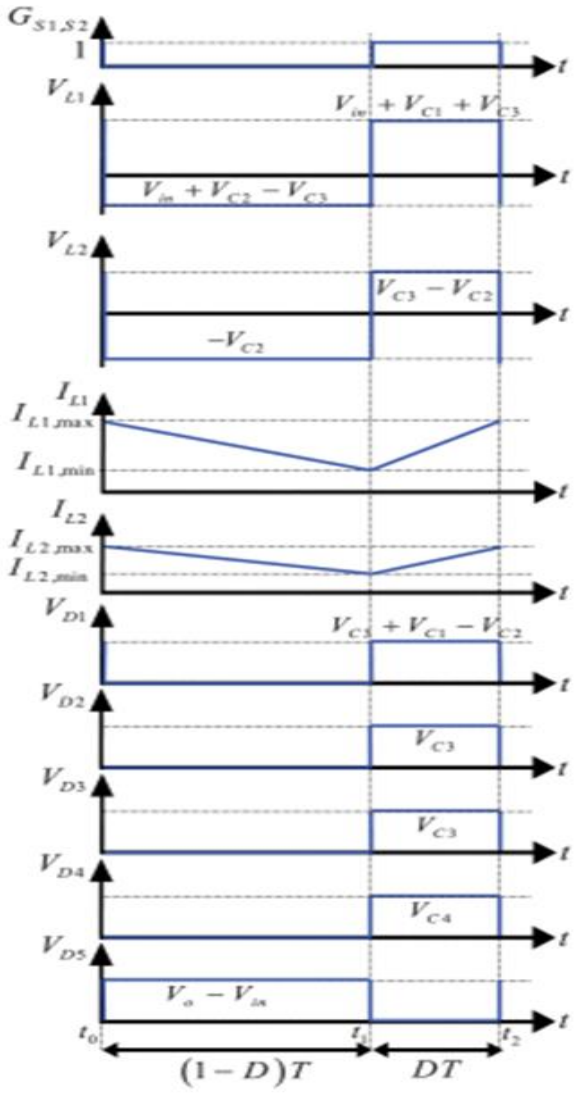
Note: D in the equation is duty cycle.

G is the boost ratio or gain.

According to equation (3.45), the boost capacity of the present topology is no doubt high with in a low duty cycle, this will also be proved in the simulations on the circuit of the presented topology. Figure 37 illustrates the waveform analysis of the components.

Figure 37

Waveform Analysis of the Converter (Meinagh et al., 2019).



3.3 Passive component design

Inductors

The ripples in current for inductor 1 can be derived by replacing (3.0), (3.36) and (3.39) in$V_L = L\,di/dt$:

$$\Delta I_{L1} = \frac{V_{L1} DT}{L1} \tag{3.46}$$

$$T = \frac{1}{F} \quad \text{D is the duty cycle which implies } D = (1 - D)$$

$$\Delta I_{L1} = \frac{V_{L1}(1-D)}{L_1 f_s} \tag{3.47}$$

From (3.0):

$$V_{L1} = V_{IN} + V_{C2} - V_{C3}$$

Substituting for V_{IN}, V_{C2}& V_{C3}:

$$V_{L1} = \frac{2D}{1-3D} V_{IN} \tag{3.48}$$

$$\therefore \Delta I_{L1} = \frac{2D(1-D)}{L_1 f_S (1-3D)} V_{IN} \tag{3.49}$$

Where f_S is the switching frequency.

For inductor 2:

$$\Delta I_{L2} = \frac{V_{L2}(1-D)}{L_2 f_S} \tag{3.50}$$

$$V_{L2} = \frac{D}{1-3D} V_{IN}$$

$$\therefore I_{L2} = \frac{D(1-D)}{L_2 f_S (1-3D)} \tag{3.51}$$

Considering Kirchhoff's current law in Figure 35 and current balance law through a single switching period for capacitors 1&2 the average current of the inductors can be written as:

$$I_{L\,ave} = I_{IN} - I_O \quad I_{Lave} = \frac{G^2 V_{IN}}{R} - \frac{G V_{IN}}{R} \tag{3.52}$$

$$G = \frac{3(1-D)}{1-3D}$$

$$I_{Lave} = \left(\frac{3(1-D)}{1-3D}\right)^2 - \frac{3(1-D)}{1-3D}$$

$$I_{Lave} = \frac{(3-3D)(3-3D) - (3-3D-9D+9D^2)}{(1-3D)^2}$$

$$I_{Lave} = \frac{6-6D}{(1-3D)^2}$$

$$I_{Lave} = \frac{6(1-D)}{(1-3D)^2} V_{IN} \quad (3.53)$$

$$I_{L1ave} = I_{L2ave} \quad (3.54)$$

I_{Lave} = average current of the inductors.

The inductor current ripple factor can be written as: using (3.49), (3.51), (3.53) and (3.54):

$$L_1 = 2L_2 = \frac{RD(1-3D)}{3x_{L1}\%f_s} \qquad \text{where } x_L\% = \Delta I_L / I_{L,ave} \quad (3.55)$$

Capacitors

The ripple voltage on the capacitors can be derived by substituting equation (3.14) and (3.15) in $I_C = C\, dv_C/dt$ while taking (3.53) and (3.54) into account.

$$\Delta V_{C1} = \Delta V_{C2} = \frac{3D(1-D)(3D^2-4D+3)}{C_{1,2} f_S R(1-3D)^2} V_{IN} \quad (3.56)$$

$$\Delta V_{C3} = \frac{3D(1-D)(3D^2-7D+6)}{C_3 f_S R(1-3D)^2} V_{IN} \quad (3.57)$$

$$\Delta V_4 = \frac{3D^2(1-D)}{C_4 f_S R(1-3D)} V_{IN} \quad (3.58)$$

Capacitor ripple factor can be derived using (3.36), (3.39), (3.45), (3.56), (3.57) and (3.58).

$$C_{1,2} = \frac{3(1-D)(3D^2-4D+3)}{x_{C1,2}\% f_S R(1-3D)} \quad (3.59)$$

$$C_3 = \frac{3D(1-D)(3D^2-7D+6)}{x_{C3}\% f_S R(1-3D)} \quad (3.60)$$

$$C_4 = \frac{3D^2(1-D)}{x_{C4}\% f_S R} \quad (3.61)$$

3.4 Comparison with other High Gain Converters

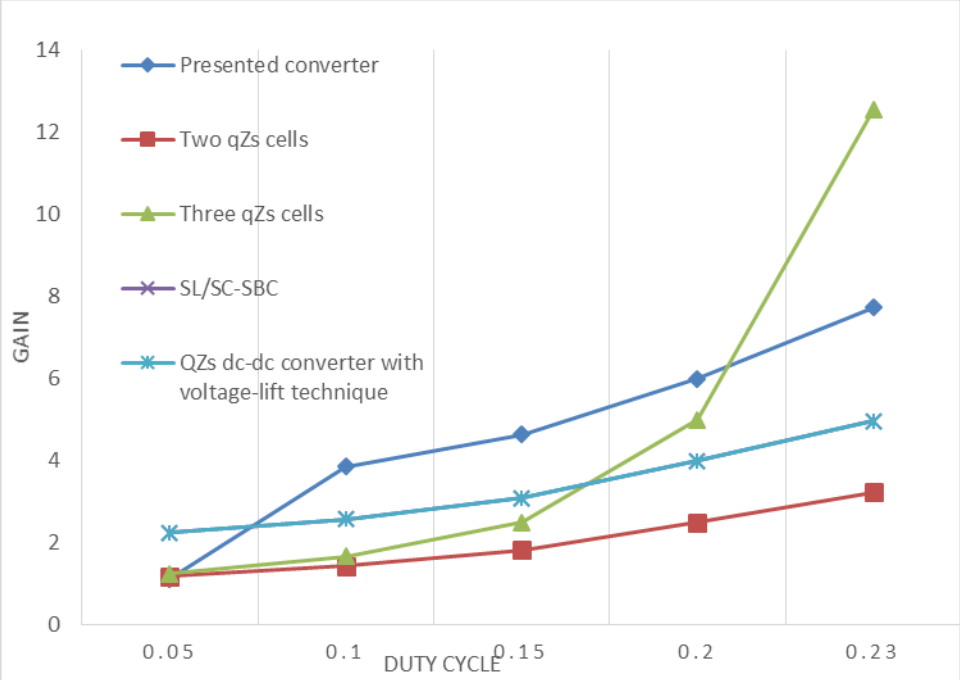
To have a better understanding and clarification of the structures and advantages of the presented topology, the topology was compared to other topology with similar structures and nearly equal deviation range in their duty cycles.

In table 3 we see that the QZS has the least number of active components while the SL/SC-SBC has the highest number of active components but in terms of passive elements the SL/SC-SBC has the smallest number. According to table 3 the component count in the circuit of the present topology comes in third compared to the others. Furthermore looking at the duty cycle range the present topology has the lowest. In addition when it comes to the stress on the capacitors, switches and diodes the presented topology has low values as shown in the simulation results.

Figure 38 shows a graph of gain against duty cycle. It is a comparison of the boosting capabilities of the presented converter and other converters. As shown in the graph we see that the presented topology has the second best boost capacity.

Figure 38

Comparison of Parameters in Table 3



Note: This graph was drawn using Microsoft excel.

Table 3

Comparison of Presented Converter with other High Gain DC-DC Converters (Meinagh et al., 2019).

parameters		Presented converter	Two cells of qZs	Three cells of qZs	SL/SC-SBC	"QZs dc-dc converter with voltage lift technique"
Number of components		2L, 5C, 2S and 5D.	5C, 3L, 3D and 1S.	7C, 4L, 4D and 1S.	2L, 3C, 2S and 7D.	3D, 1S, 4C and 4L
Voltage stress	switches	$\frac{GV_{IN}}{3(1-D)}$	GV_{IN}	GV_{IN}	$\frac{DGV_{IN}}{1-D}$ $\frac{GV_{IN}}{2}$	GV_{IN}
	diodes	$\frac{GV_{IN}}{3(1-D)}$ $(G-1)V_{IN}$	GV_{IN}	GV_{IN}	$\frac{DGV_{IN}}{1-D}$, $\frac{GV_{IN}}{2}$, $\frac{DGV_{IN}}{2(1-D)}$	$\frac{GV_{IN}}{1-D}$ $\frac{GV_{IN}}{2}$
Capacitor voltage		$\frac{DGV_{IN}}{3(1-D)^2}$ $\frac{GV_{IN}}{3(1-D)}$	DGV_{IN}, $2DGV_{IN}$, $(1-2D)GV_{IN}$	$(1-2D)GV_{IN}$ DGV_{IN},$2DGV_{IN}$ $(1-3D)GV_{IN}$	$\frac{DGV_{IN}}{1-D}$ $\frac{GV_{IN}}{2}$	$\frac{GV_{IN}}{2}$ $\frac{(1+D)GV_{IN}}{2(1-D)}$
Duty cycle range		$0 < D \leq 0.20$	$0 < D \leq 0.33$	$0 < D < 0.25$	$0 < D \leq 0.33$	$0 < D \leq 0.33$
Voltage gain		$\frac{3(1-D)}{1-3D}$	$\frac{1}{1-3D}$	$\frac{1}{1-4D}$	$\frac{2(1-D}{1-3D}$	$\frac{2(1-D)}{1-3D}$

Note: S=Switches, L=Inductors, D= Diodes

3.5 Simulation Results

Simulations of the presented topology is done by using PSCAD/EMTDC version 4.2. Behaviors of the voltages and currents of various components and the overall performance of the presented converter will be illustrated below.

Table 4

Input Parameters of the Components.

Parameters	Values
Input voltage	40v
Load resistance	400Ω
L_1	500µH
L_2	500µH
C_1	470µF
C_2	470µF
C_3	470µF
C_4	470µF
C_f	470µF
Frequency	50Hz
Types of switch	IGBT

Figures 39 shows the voltage across inductor 1 with a minimum of V_{L1min}=–167Volts and a maximum of V_{L1max} = 44 Volts. Figure 40 show the voltages across inductor 2 with the highest being V_{L2max}= 23.02oltsV and lowest being VL2min= –84 Volts.

Figure 39

Inductor (vL_1) voltage

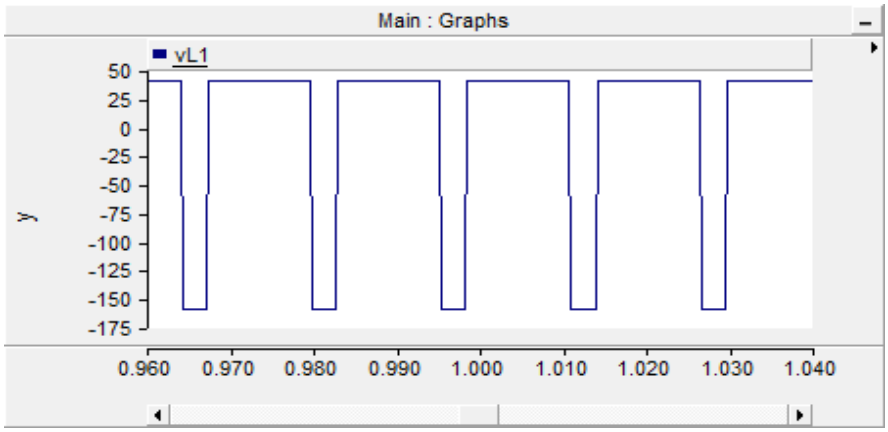


Figure 40

Inductor (vL_2) voltage

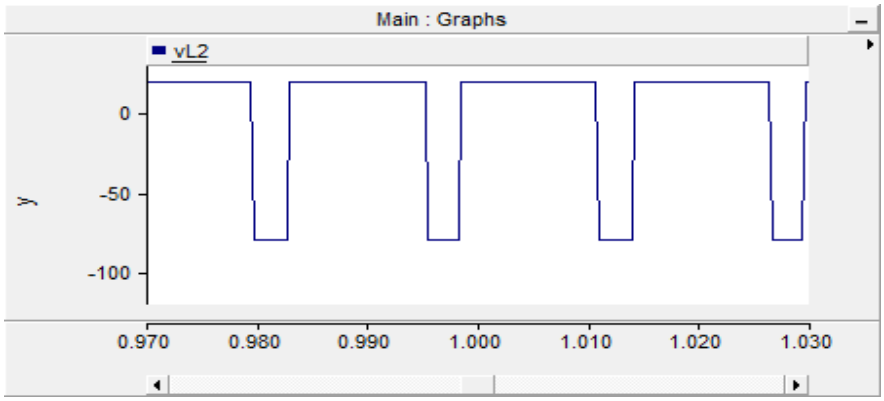
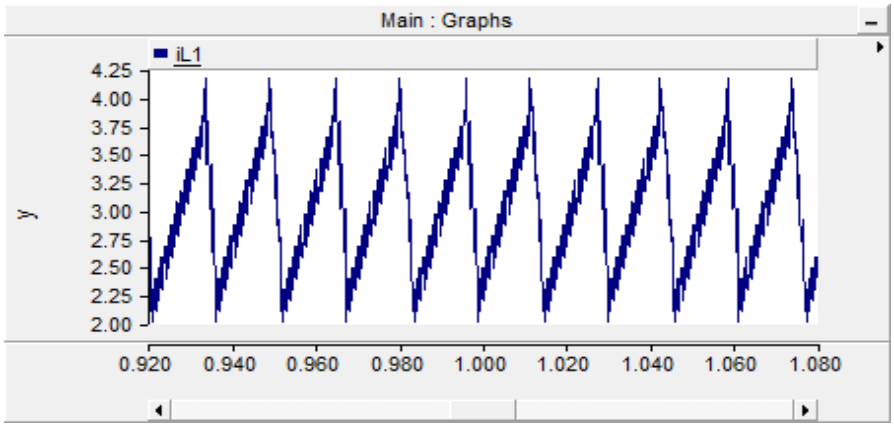


Figure 41 shows the current through inductor 1 at a voltage input of 40v.

Figure 41

Inductor (iL_1) current



The current of inductor 2 at 40v input is shown below in figure 42.

Figure 42

Inductor (iL_2) current

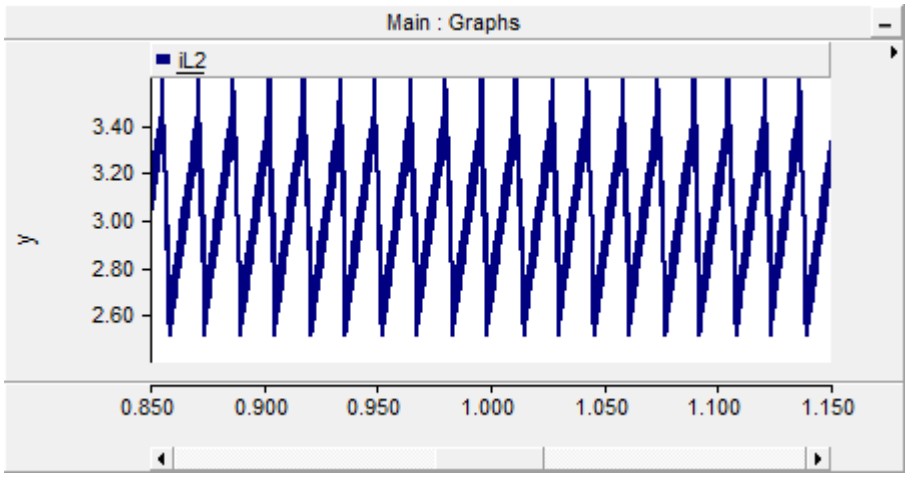


Figure 43 and 44 show that the voltage across C_1=C_2= 22V, this validates the assumption in the steady state analysis. In figures 45 and 46 the voltage across V_{C3}=V_{C4}= 106.90, this validates the steady state analysis.

Figure 43

Capacitor (vC_1) Voltage

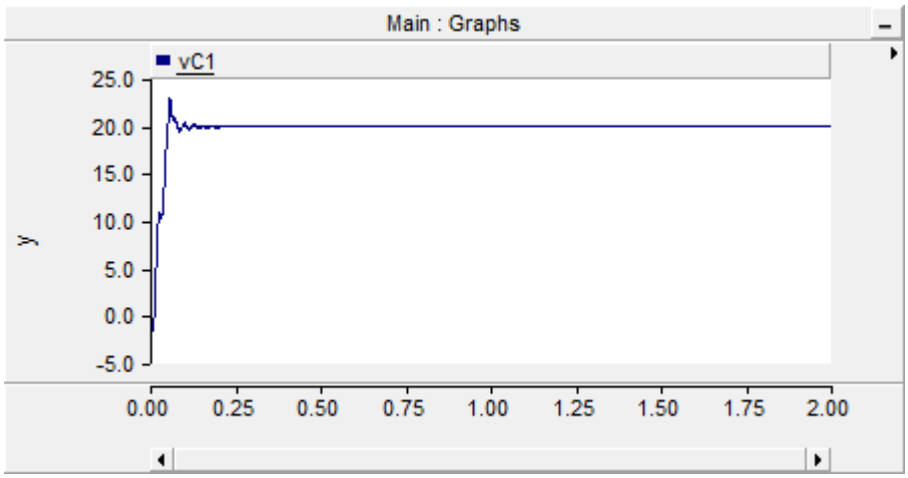


Figure 44

Capacitor (vC_2) Voltage

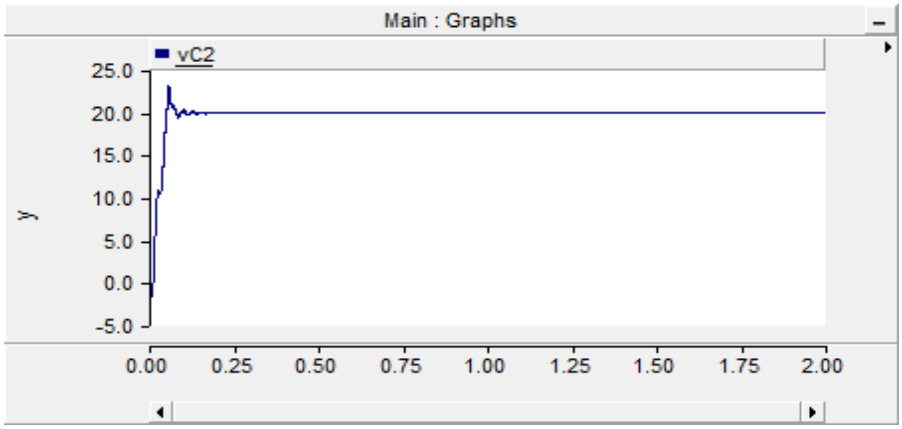


Figure 45

Capacitor (vC_3) Voltage

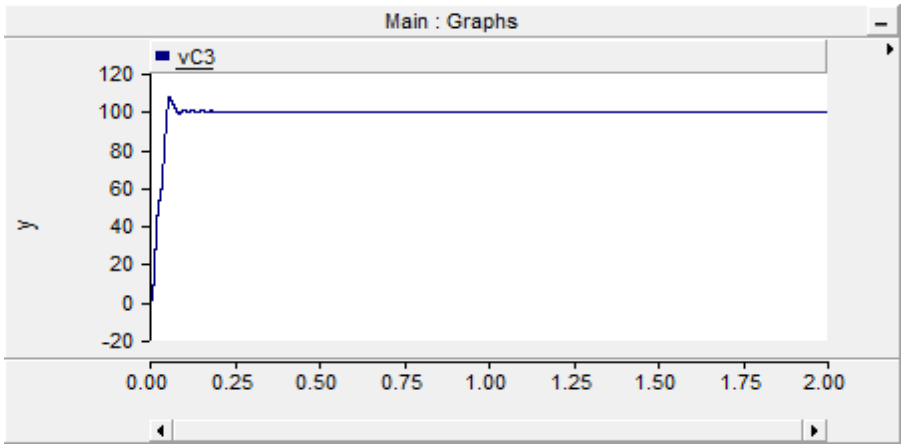


Figure 46

Capacitor (vC_4) Voltage

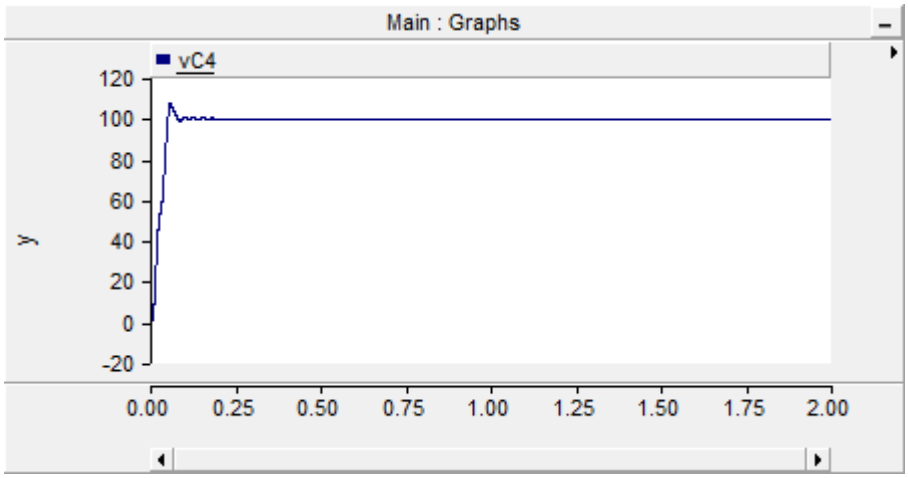
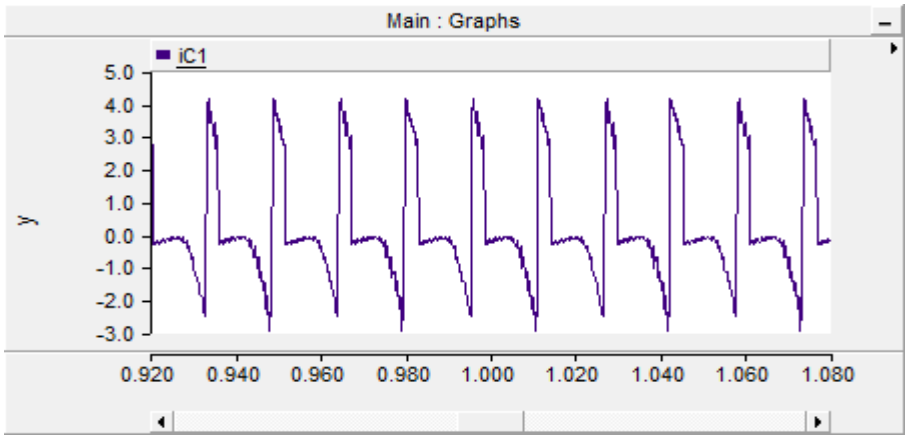


Figure 47

Capacitor (iC_1) Current



The current through the capacitor C_1, C_2, C_3, C_4, C_f is shown below from figure 48 to 51.

Figure 48

Capacitor (iC_2) Current

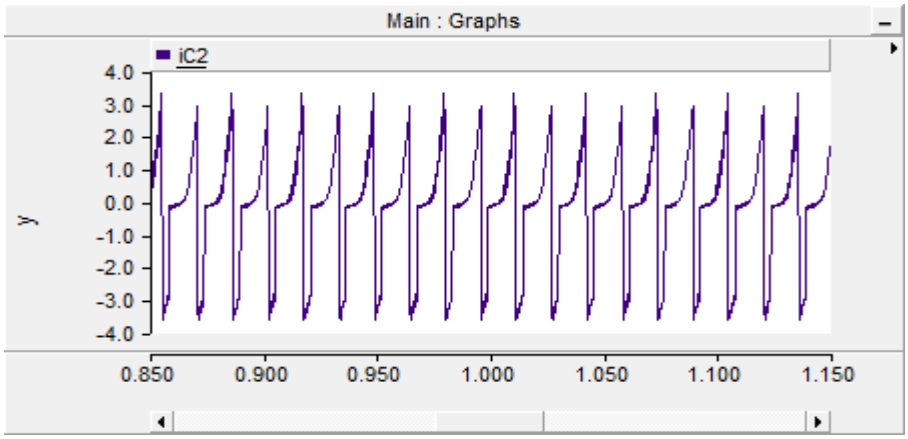


Figure 49

Capacitor (iC_3) Current

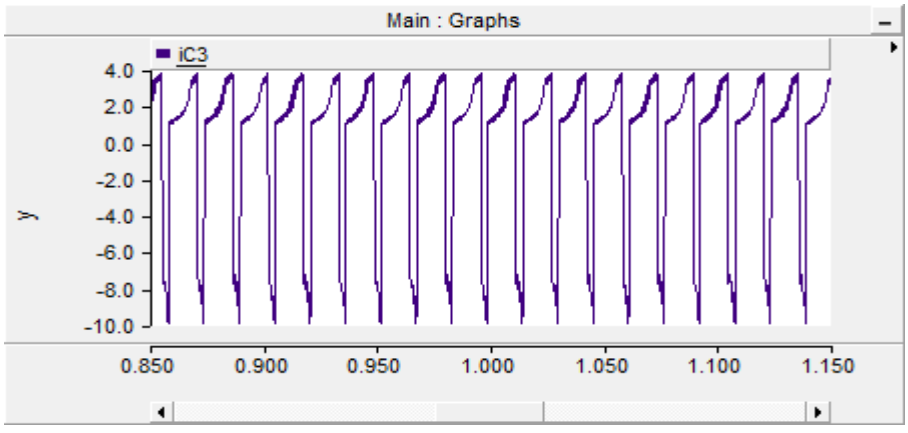


Figure 50

Capacitor (iC_4) Current

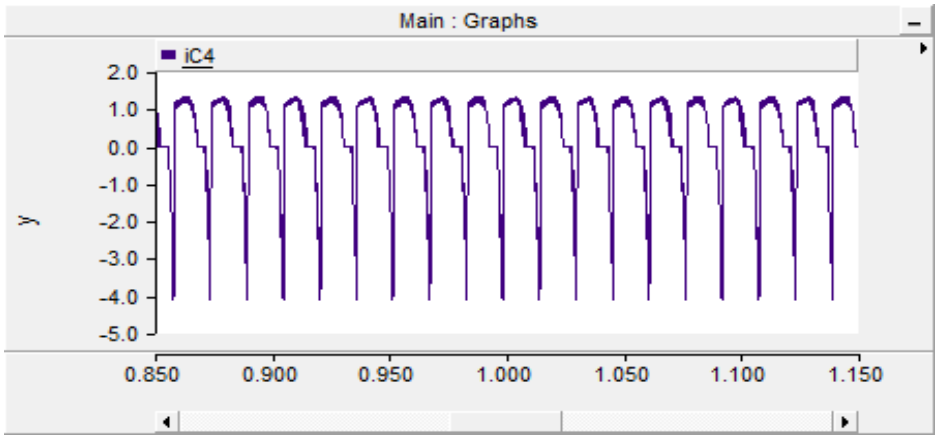


Figure 51

Capacitor (iC_f) Current

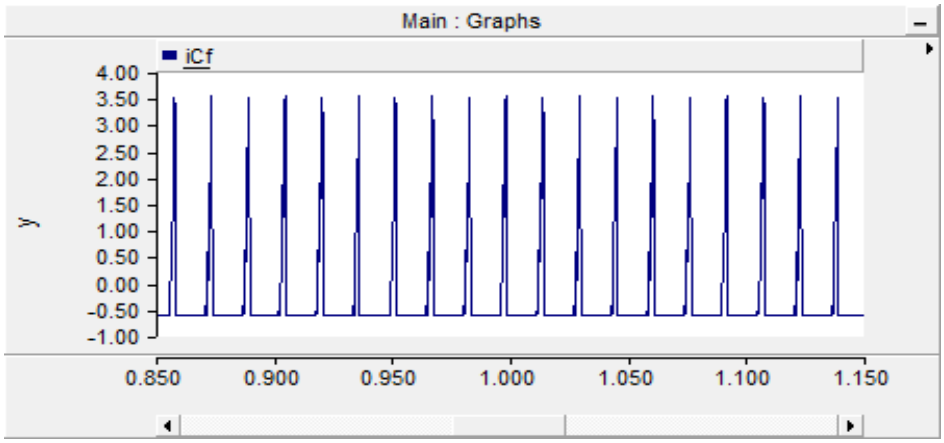
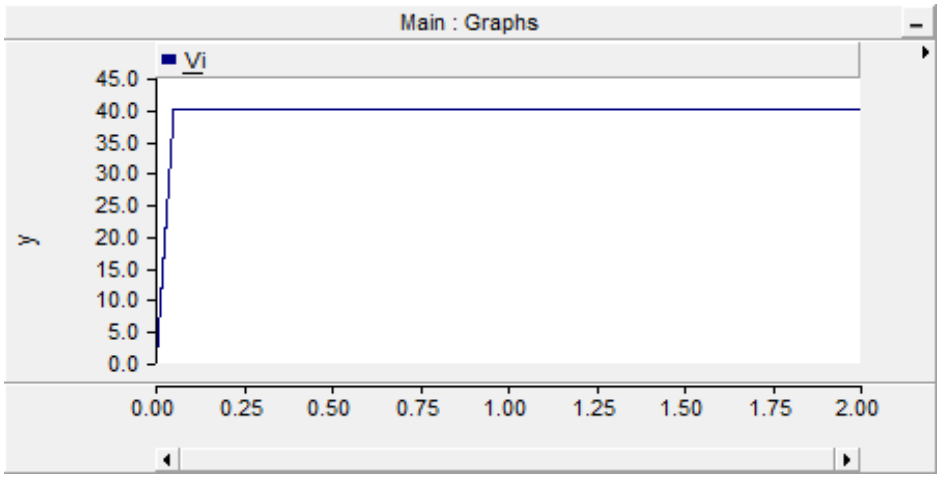


Figure 52

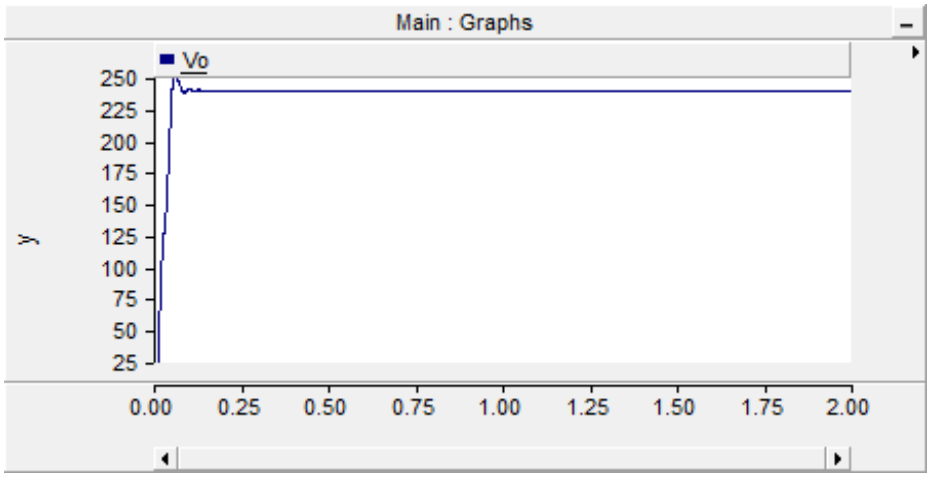
Input Voltage



As shown in figure 53 V_0= 253.65V, this means that the boost factor of the converter is over six times the input value.

Figure 53

Output Voltage



Figures 54 shows the input current.

Figure 54

Input Current

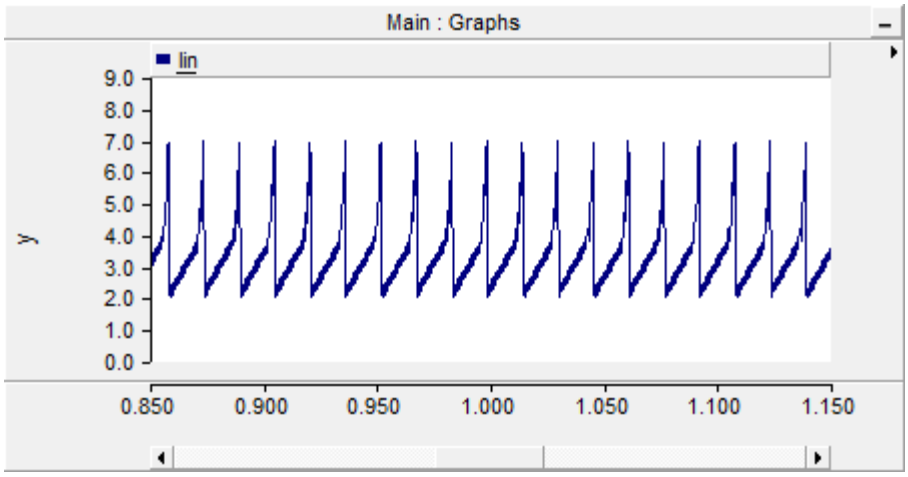
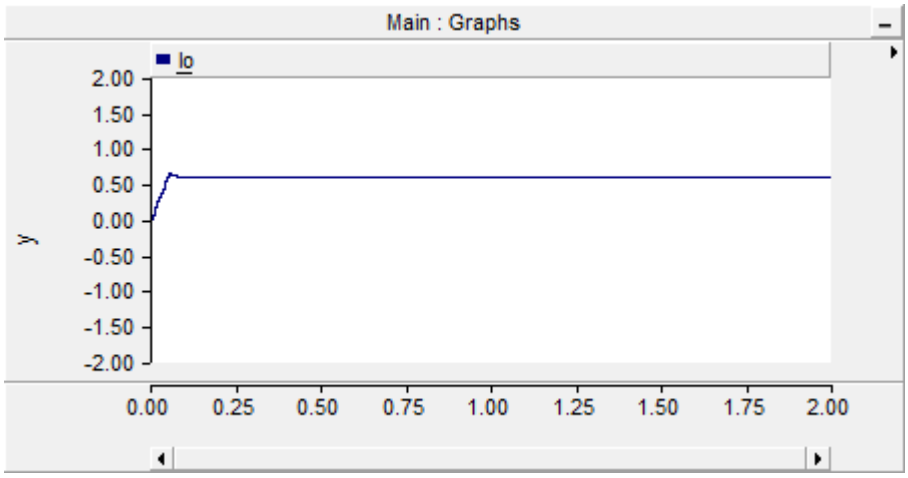


Figure 55 shows the output currents of the presented topology.

Figure 55

Output Current



As stated in chapter 1, another important quality of this presented converter is its capability to attain low voltage stresses on the semiconductor components. The simulations results show the values of converter voltage on the semiconductor as follows, S_1=106, S_2=106, D_1=105, D_2=105, D_3=105 and D_4=105V, meanwhile for diode D_5 the voltage stress is equal to 200V, this value is a bit high compared to the other diodes but this error is negligible according to equation (3.4), (3.5), (3.6), (3.18), (3.19) and (3.20). Thus, validating the theory that proposed converters attain low voltage stresses on the semiconductor components.

Figure 56

Diode (vD_1) Voltage

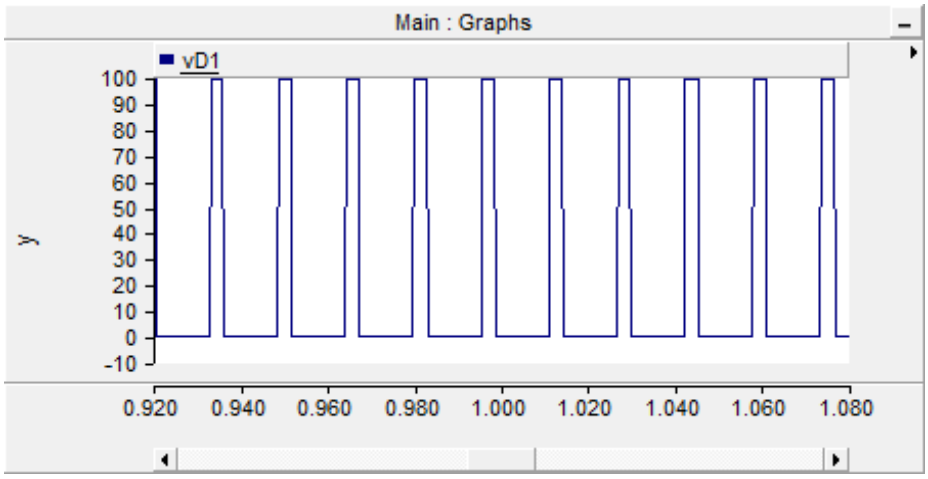


Figure 57

Diode (vD_2) Voltage

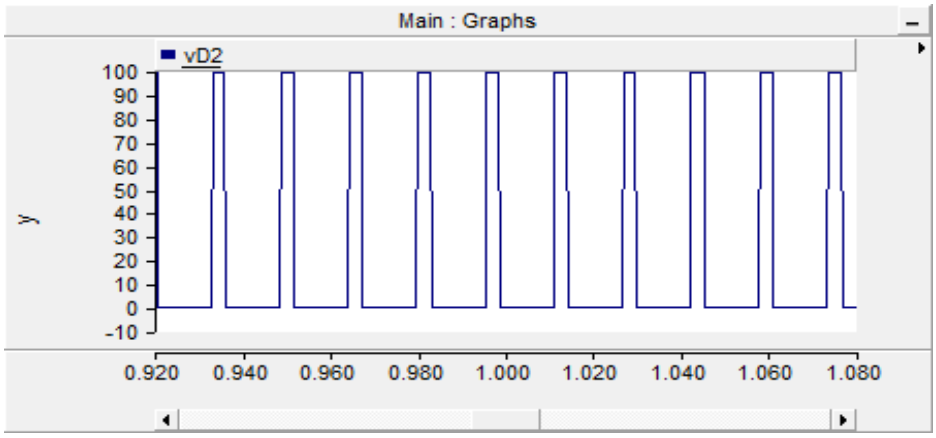


Figure 58

Diode (vD_3) Voltage

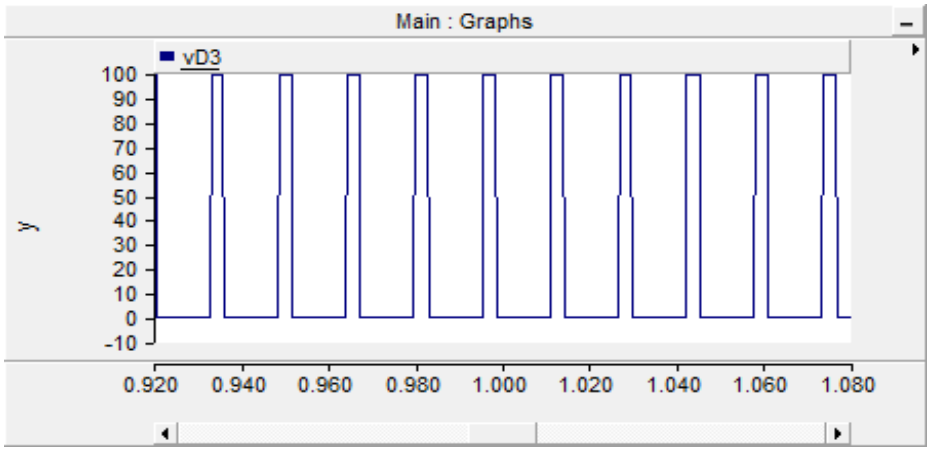


Figure 59

Diode (vD_4) Voltage

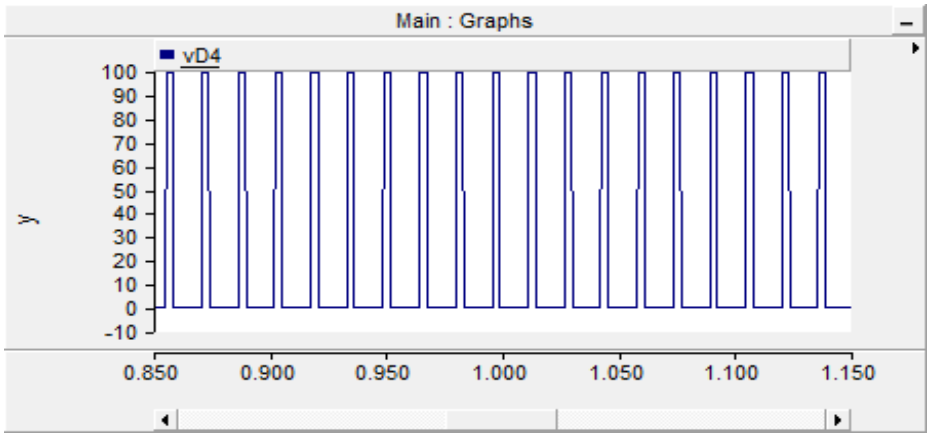


Figure 60

Diode (vD_5) Voltage

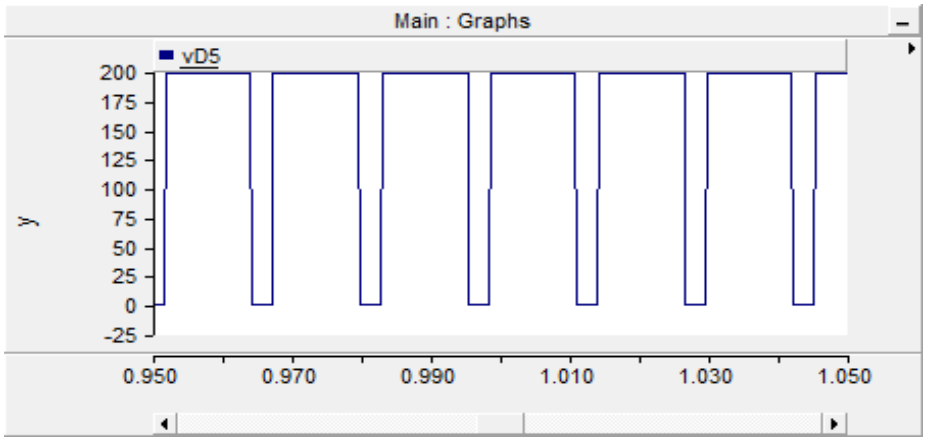


Figure 61

Diode (iD_1) Current

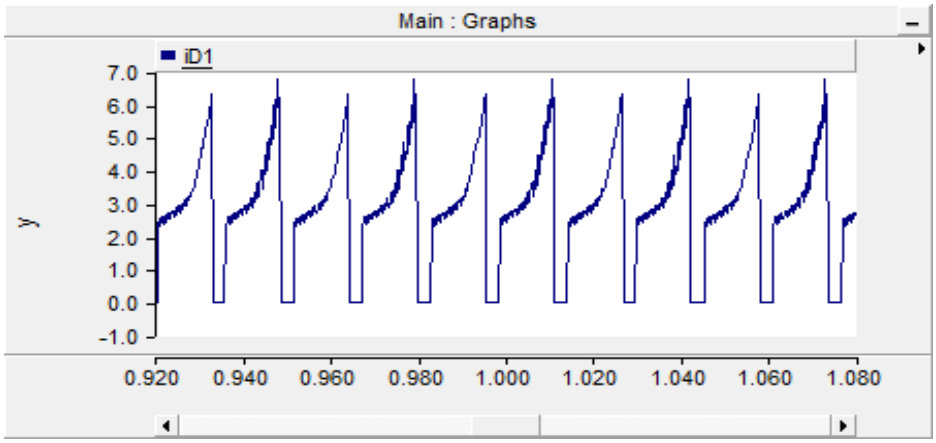


Figure 62

Diode (iD_2) Current

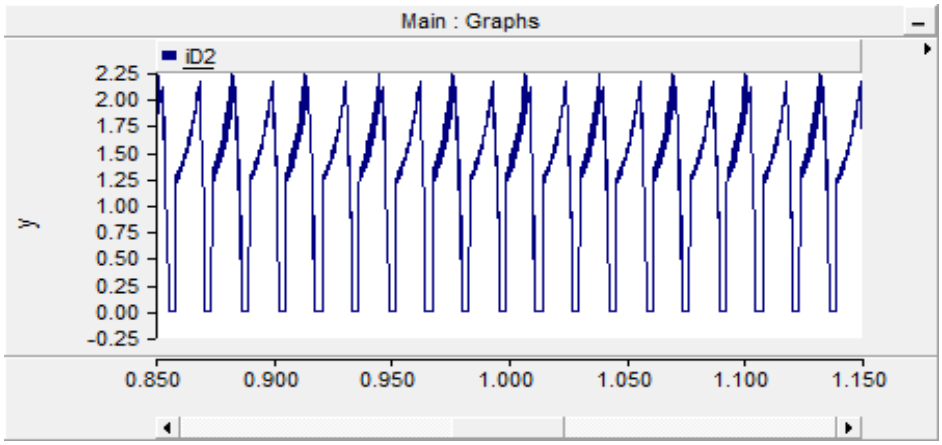


Figure 63

Diode (iD_3) Current

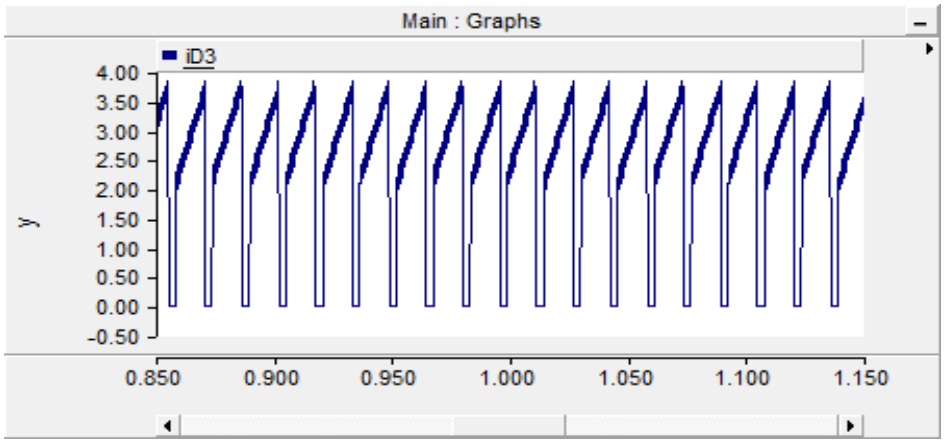


Figure 64

Diode (iD_4) Current

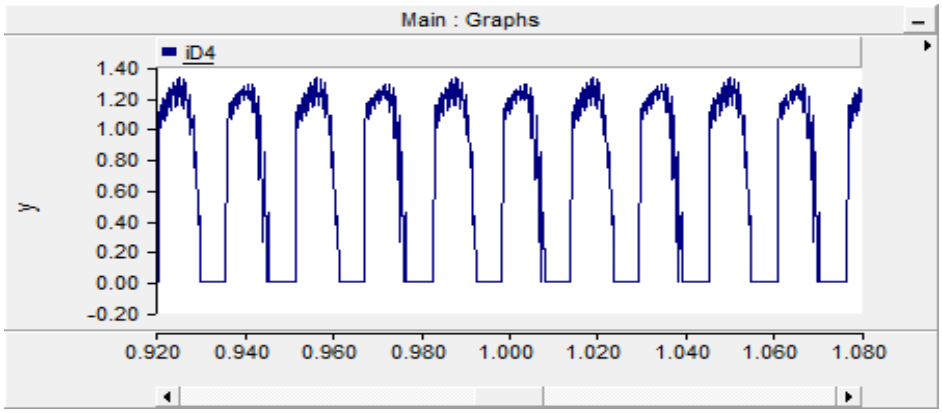


Figure 65

Diode (iD_5) Current

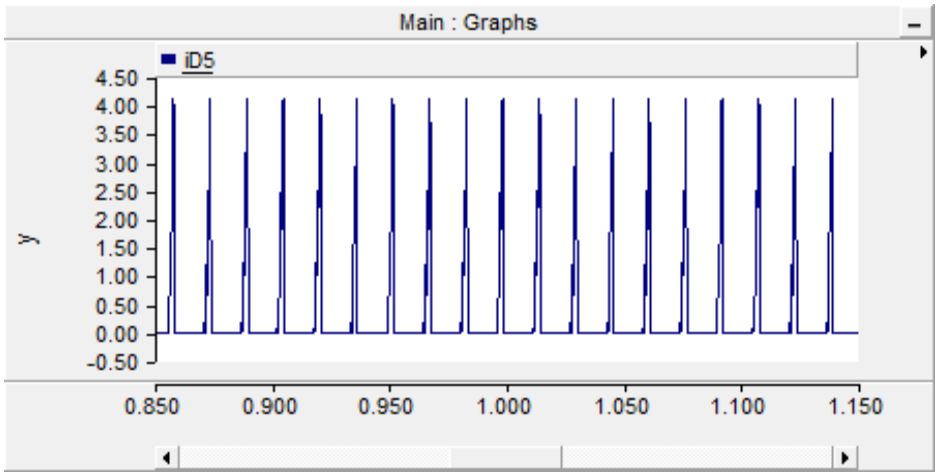


Figure 66

Switch (vS_1) Voltage

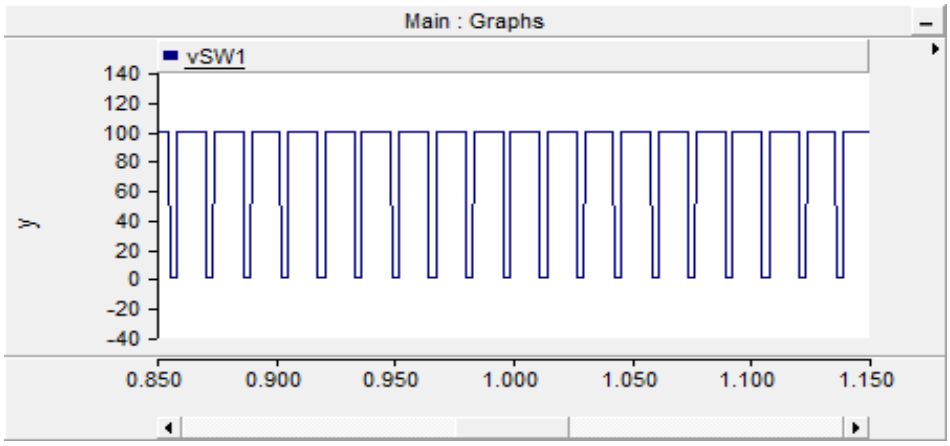


Figure 67

Switch (vS_2) Voltage

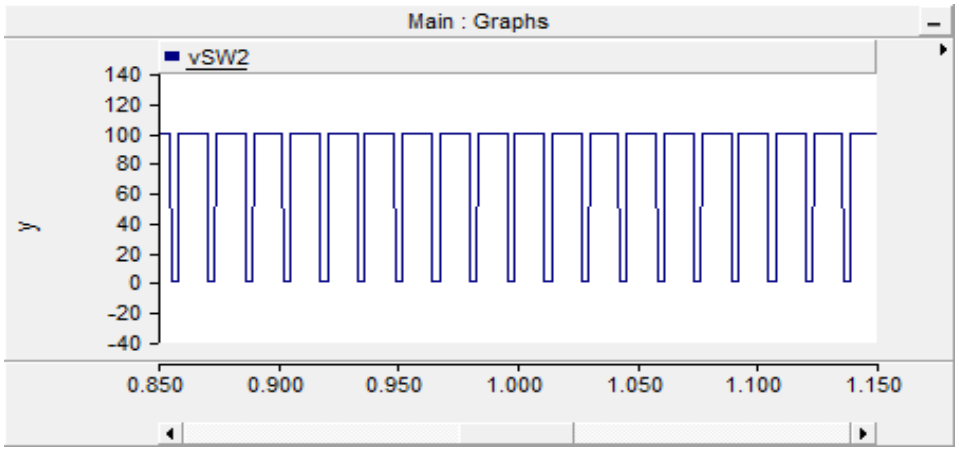


Figure 68

Switch (iS_1) Current

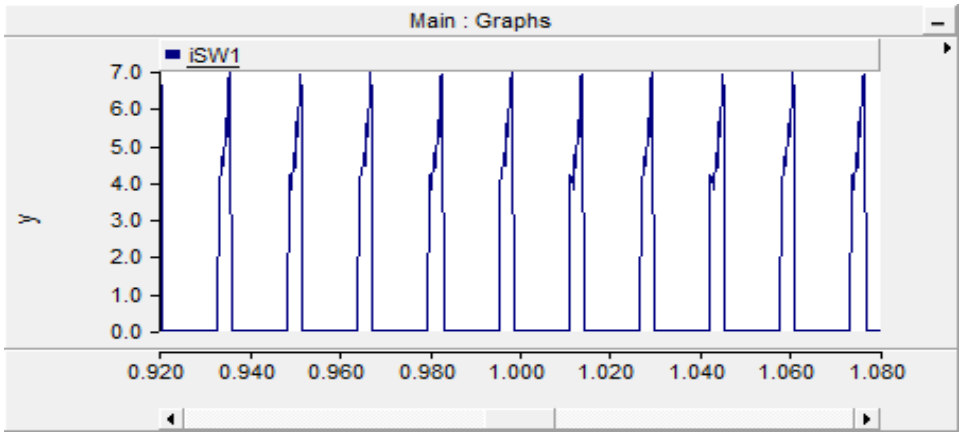
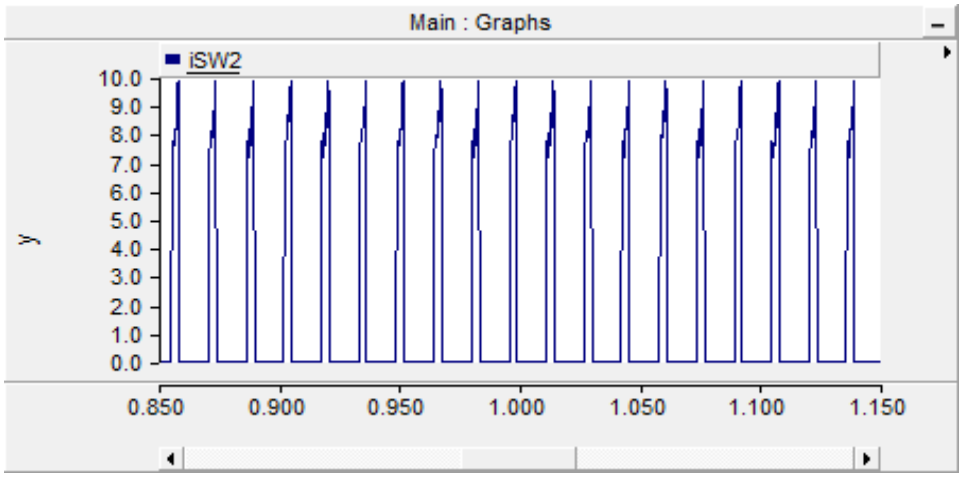


Figure 69

Switch (iS_2) Current



3.6 Comparative Analysis of Output Voltage at Various Duty Cycles

Figure 70 shows output voltages at different duty cycles with an interval of 10%. As evident in figure 70 at a duty cycle of 30% output voltage is at maximum but the stress on the semiconductor was quadrupled which is not ideal. Furthermore, since actual experiments are not performed on the converter to determine its efficiency therefore duty cycle of 20% would be the most suitable.

Figure 70

Output Voltage at Various Duty Cycles

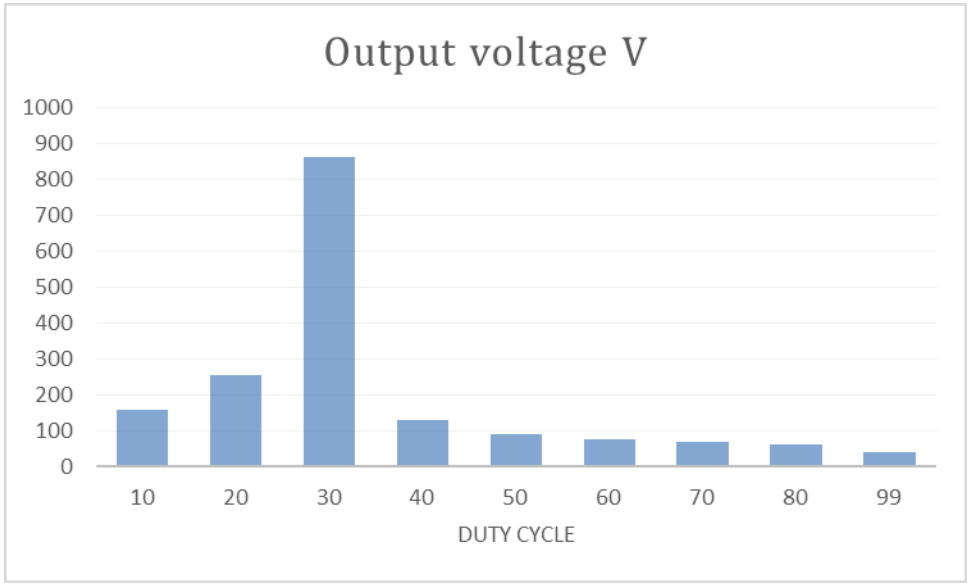


Table 5

Summary of Simulation Results

Parameter	Voltage in volts(max)	(min)	Current in amps (max)	min
Source	40	0	7.0	2.0
Inductor 1, L_1	44.52	-167.37	4.20	2.0
Inductor 2, L_2	23.02	-84.55	4.0	2.40
Capacitor 1, C_1	22	-0.95	4.0	-2.5
Capacitor 2, C_2	22	-1.54	3.0	-3.5
Capacitor 3, C_3	106.90	0	4.1	-10
Capacitor 4, C_4	106.90	0	1.3	-4.0
Capacitor 5, C_f	253.65	0	3.5	-0.53
Switch 1	106.0	0	7	0
Switch 2	106.0		10	0
Diode 1, D_1	105.0	-0.55	6	0
Diode 2, D_2	105.0	-0.26	2.25	0
Diode 3, D_3	105.0	-0.17	3.9	0
Diode 4, D_4	105.0	-0.27	1.32	0
Diode 5, D_5	200	-0.13	4.0	0
Output	253.65	0	0.63	0

3.7 Summary

This chapter detailed the operation of the presented the presented topology, as shown in the simulation results which was possible with the use of PSCAD/EMTDC we were able to verify the boosting capability of the presented topology. Furthermore, the result form the simulation shows the advantages of the presented converter, these include high boosting of the input voltage at a low duty cycle. In addition PWM was used to control the switching process of the switching in the circuit. Furthermore, looking at circuitry of the presented converter has a suitable number of components and very little voltage stresses on its components.

CHAPTER 4

4.0 Introduction

This chapter is a brief description of the overall findings in this thesis and a summary on the literature review, the analysis and results. Furthermore, recommendations for future work are also included.

4.1 Overview

This thesis presents a dc-dc converter with high boosting capabilities, from chapter 3 we see that this converter has high voltage gain, less stress on the semiconductor components, low duty cycles and less elements compared to other high gain converters.

The literature review shows how different topologies have been proposed one after the other over the years for applications in renewable energy. The literature was presented on impedance source networks like z-sources converter, quasi z-source converter switched capacitor network etc. in this section we looked at their mode operations, voltage gain and how far they have come in terms of evolution. However, there are some disadvantages that are related to these impedance source networks, these disadvantages range from high duty cycle, high number components, high voltage stress on the diodes and switches, and complex circuits.

Furthermore, from the circuit of the presented topology we can see that the presented topology contains a modified quasi z-source circuit and a switched capacitor circuit. The modified quasi Z-Source circuit contains 9 components namely S_1, L_1 and L_2, D_1, D_2, and D_3, C_1, C_2, and C_3. The circuit for the switched capacitor contains 3 components namely S_2, D_4 and C_4; diode D_5 is connected to the positive end of the voltage at the input and output to prevent backflow of current and C_f is the output capacitor. The presented converter has a total of 14 components. A steady-state analysis of the topology was done to determine the ratio between the input and output voltage. Mathematical analysis showed a voltage gain of 6 times the input voltage at a duty cycle of 20%. This stimulation was done on PSCAD 4.2 and the results confirmed the advantages stated in chapter 1. This converter has the ability to generate diverse output voltages for different values of duty cycle.

4.2 Recommendations for Future Work

For future works the number of switched capacitor networks can be increased, the converter can also be coupled with a 3-phase multilevel inverter. Furthermore, we can also explore its application in electric vehicles.

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Appendices

Appendix A

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