ZUBEIR MOHAMED NUR

SYMMETRIC AND ASYMMETRIC DC SOURCE ANALYSIS OF AN IMPROVED SINGLE-PHASE H-BRIDGE MULTILEVEL INVERTER

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Approval

We certify that we have read the thesis submitted by Zubeir Mohamed Nur titled "**Symmetric and Asymmetric DC Source Analysis of an Improved Single-Phase H-Bridge Multilevel Inverter**" and that in our combined opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master in Electrical and Electronic Engineering.

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Declaration

I hereby declare that all information, documents, analysis and results in this thesis have been collected and presented according to the academic rules and ethical guidelines of the Institute of Graduate Studies, Near East University. I also declare that as required by these rules and conduct, I have fully cited and referenced information and data that are not original to this study.

Zubeir Mohamed Nur

15/07/2024

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Zubeir Mohamed Nur

Abstract

Symmetric and Asymmetric DC Source Analysis of an Improved Single-Phase H-Bridge Multilevel Inverter

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Assoc. Prof. Dr. Samuel Nii Tackie

M.Sc., Department of Electrical and Electronics Engineering

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This study presents symmetric and asymmetric DC source analysis of an improved single-phase H-bridge structure MLI. The chosen topology features these components; 6 input dc voltage sources, and 12 power switches with 12 drivers. The analysis of the symmetric magnitude yields 9 voltage steps. For the asymmetric structure was able to generate 31 voltage steps. The topology utilizes less components to produce a sinusoidal high-quality waveform, increasing the inverter's efficiency and reducing cost. The higher stepped voltage levels are applicable for DC renewable energy sources, like solar. The selected control method for the switching circuit is the fundamental frequency control method, that has some benefits over other techniques. Analysis of the proposed topology's components usage was conducted and was compared to other existing topologies. PSCAD/EMTDC is the software used to investigate and simulate the proposed inverter. An incremented step voltage of 22V is used for the simulation parameters. The results showed a high-quality sinusoidal output voltage waveform with 330V peak voltage aligning perfectly with the reference signal, and load current waveform of 6.35A amplitude. The standing voltages of the switches validate the theory calculation.

Keywords: multilevel inverter, single-phase h-bridge inverter, symmetric and asymmetric analysis.

Özet

Geliştirilmiş Tek Fazlı H-Köprüsü Çok Seviyeli Eviricinin Simetrik ve Asimetrik DC Kaynak Analizi

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Bu çalışmada, geliştirilmiş tek fazlı H-köprüsü çok seviyeli eviricinin simetrik ve asimetrik DC kaynak analizi sunulmaktadır. Seçilen topoloji şu bileşenleri içerir; 6 giriş DC voltaj kaynağı ve 12 sürücülü 12 güç anahtarı. simetrik yapılandırması analizi 9 voltaj seviyesi verir. Asimetrik yapılandırması için 31 gerilim seviyesi üretilebildi. Topoloji; sinüzoidal olan, eviricinin verimliliğini artıran ve maliyeti daha düşük olan yüksek kaliteli dalga şekli üretirken daha az bileşen kullanmaktadır. Daha yüksek kademeli voltaj seviyeleri, güneş enerjisi gibi DC yenilenebilir enerji kaynakları için geçerlidir. Anahtarlama devresi için seçilen kontrol yöntemi, temel frekans kontrol yöntemidir, diğer tekniklere göre bazı avantajları olan. Önerilen topolojinin bileşen kullanımının analizi yapıldı ve mevcut diğer topolojilerle karşılaştırıldı. Önerilen tek fazlı çok seviyeli eviricinin araştırılması ve simülasyonu için PSCAD/EMTDC kullanılmaktadır. Simülasyon parametreleri için 22 V'luk artımlı bir adım voltajı kullanılmıştır. Sonuçlar, referans sinyaliyle mükemmel uyum sağlayan 330 V tepe voltajına sahip yüksek kaliteli sinüzoidal çıkış voltajı dalga formu ve 6,35 A genliğinde yük akımı dalga formu göstermiştir. Anahtarların durma voltajları teorik hesaplamayı doğrulamaktadır.

Anahtar Kelimeler: çok seviyeli evirici, tek fazlı h-köprü evirici, simetrik ve asimetrik analiz.

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List of Abbreviations

AC:	Alternating Current
APOD:	Alternative Phase Opposite Disposition
CHB MLI:	Cascaded H-Bridges Multilevel Inverter
CMV:	Common Mode Voltage
DC:	Direct Current
DC MLI:	Diode Clamped Multilevel Inverter
EMTDC:	Electromagnetic Transients with DC
FC MLI:	Flying Capacitor Multilevel Inverter
FFCM:	Fundamental Frequency Control Method
IGBT:	Insulated-Gate Bipolar Transistor
MLI:	Multi-Level Inverter
MOSFET:	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT:	Maximum Power Point Tracking
NLC:	Nearest Level Control
NPC:	Neutral Point Clamped
PD:	Phase Disposition
POD:	Phase Opposite Disposition
PSCAD:	Power System Computer Aided Design
PV:	Photovoltaic
PWM:	Pulse Width Modulation
SHE:	Selective Harmonic Elimination
SPWM:	Sinusoidal Pulse Width Modulation
SSI:	Split Source Inverter
STATCOM:	A STATic synchronous COMpensator
SVM:	Support Vector Machine
THD:	Total Harmonic Distortion

CHAPTER I
Introduction

Overview

In the last years, there have a notable increase in the development of power electronic converters and are used for electrical energy conversion in all power categories. Modern civilization heavily relies on electricity, the most widely used form of energy. However, using fossil fuels or radioactive materials in power plants, in particular, has a substantial an effect on the environment and causes extensive contamination. Furthermore, the price of fossil fuels keeps rising. In this case, the appeal of renewable energy sources is growing for purposes other than only lowering environmental pollution levels.

Recent advancements of technology have rendered renewable energy systems more viable choice. There are various types of renewable energy: wind, solar, hydropower energy, and others. Although it is heavily dependent on changing environmental conditions, solar energy is one of the major sources of renewable energy that is receiving more attention in power system research. Photovoltaic energy has countless advantages, such as a long lifespan, minimal maintenance and operation costs, and a favorable environmental impact. Wind energy is widely used, generating more power than solar and nearly the same as hydropower energy.

In (Miñambres Marcos et al., 2017), a PV inverter is suggested that is connected to the grid and, an inverter that combines both batteries and supercapacitors, a hybrid energy storage. The suggested hybrid energy storage design, which combines batteries and supercapacitors, effectively lowers the charge and discharge rate while also giving a nearly sinusoidal waveform. For conditioning while supplying electricity from renewable energy sources require the use of power electronics device.

Standard photovoltaic cells can only produce less than 3 watts of power at 0.5 volts; in order to achieve the required power needed for high-power applications, they should be linked in an arrangement of series and parallel connections. Modules comprise PV systems, while modules comprise arrays. Depending on the application, the realistic power generation of photovoltaic modules might range from a couple of

watts to over 300W. Another renewable energy source is wind energy, which is produced in wind power plants; the wind passes through turbines, causing constant rotation and generating electricity. These projects are predicted to remain the majority in the coming decades due to the large demand and economic competitiveness. However, solar generation systems, for example, the rooftop installation and buildings that are integrated with PV systems, and the recent increase in electric cars across the globe would have a significant effect on renewable energy generation.

The fluctuating supply of renewable energy sources considerably restricts their ability to be integrated at higher levels. This situation has inspired several researchers in this field. As a result, there has been considerable interest in studying ways to incorporate an energy storage system to deal with the extra demand for electricity. Energy storage devices with high energy retention and little energy loss can enhance the stability of power systems (Mizutani et al., 2016). According to (Romlie et al., 2014), energy storage systems (ESS) can be a desirable option.

An inverter is made of power electronic components, which operate to change a voltage's features; it changes from direct current into an alternating current; in addition, it could vary the magnitudes. The majority of inverters include power switches as their primary controllable component, which can be any of the following: IGBTs, MOSFETs, thyristors, and others. Controlling the power switches on and off states, their switching pattern results in the expected output voltage, that has a sinusoidal waveform pattern. One or multiple direct current voltage sources are connected to the inverter power circuit's input, producing a smooth, sinusoidal output waveform at various voltage waveform levels. The idea of MLI was first identified in the middle of the 70s, but it wasn't until 1980 that (Nabae et al., 1982) presented the Neutral Point Clamped, the first multilevel inverter.

MLI offer many benefits over their predecessors, the two-level inverters. Among these benefits are; it increases the output voltage levels generated, better quality output waveforms, it reduces the stress that are placed on the components, reducing the total harmonic distortions (THD), employing low rated-switches in terms of voltage, less electromagnetic interferences. Conventional inverter face difficulties

operating at high voltages, switching voltage stress, with these issues it diminishes the efficiency of power system, especially renewable energy system. Multilevel inverters are preferred in these applications as they overcome those limitations.

In photovoltaic cells, the sunlight arrays are effectively converted to electricity. It's like a diode form with a p-n junction. How it is designed is required for the maximum amount of sunlight radiation. The concept idea relies on how incident photons interact with the silicon electrons. If the energy from the photons exceeds that of the silicon, it will create an electron pair hole, in which the higher energy photons, the conduction band, will be absorbed by the cells, and the remaining energy difference is transformed into heat.

To achieve these grid connection criteria in accordance with international legislation and standards, the current control method is a crucial component. The source of renewable energy itself needs to be extremely safe and efficient in order for connected applications to be secure and dependable. As a result, additional controllability must be integrated into next-generation renewable energy systems by offering supplementary services. Inverters that provide these sorts of functions are referred to as multifunctional inverters. Given this, a thorough analysis of multifunctional inverters with different controls is necessary.

Three distinct configurations serve as the foundation for photovoltaic power plants, which are given as: central, multi-string, and string designs. Choosing any of these topologies will undergo factors to prove it is the best option depending on where the area is located, how much power level is expected to be drawn from the power plant, the cost of the process and how efficient it will be most of the time.

1. Central

   This is the most favorable and well-known configuration of the PV application. In central configuration, what it does is its design connects multiple PV panels to a single inverter. Their panel arrangement is in a hundred arrays, with every one of them having hundreds of strings, and the connection is parallel. Likewise, for the dc voltage part, for its numbers to be proper, the PV panels in those strings are series arranged.

2. String

   This string setup links one PV string to only one inverter. It has an advantage when the sun exposure is less, and there is partial shade, the efficiency of the power produced is increased due to the flexibility that enables independent maximum power point tracking. The power converters, which involve two conversion steps and galvanic isolation, could be used to prevent loss of current and voltage that exceeds the limit of the highest in the panels present. Generally, there is the chance to employ an inverter that has the characteristics of low-frequency transformers or a converter with a higher-frequency transformer.

3. Multi-string

   This setup, multi-string arrangement blends and mixes the discussed configurations above, central and strings. It has a series of connected photovoltaic panels, which are linked to independent converters, then linked to a shared central inverter.

Comparing the three configurations, it is concluded that the central setup has limited adaptability, from the dc wires, there are significant losses but moderate losses from their ac side, although, with having less maintenance over time and less setup cost, they also have a strong quality. In comparison to the other arrangement, the string and multi-string have greater adaptability and dependability, and on their dc side, the losses are less, more time with the maintenance.

The PV system's primary goal is to produce active power. Many power quality issues may be resolved, and overall system performance can be improved with smart PV system control. Using multifunctional inverters in solar PV systems allows for this. In solar powered renewable energy systems, the multilevel multifunctional inverter is an essential component of technology. When the multifunctional potential of the inversion is investigated, the PV system's utilization factor is significantly increased. For (Babaie, M. et al. 2020), solar energy using photovoltaic panels must be used for both dc and ac applications to meet the needs of portable electrical energy-based operated applications. Multilevel inverters are utilized to achieve this, and the topology type is the only factor that affects the quality of the converted AC power.

Control strategies play a crucial role in raising the multilevel inverters' output voltage quality and are also appropriate for introducing quality waveforms. Utility companies establish certain guidelines and regulations, as well as grid codes, for PV systems connecting to the grid. These requirements include maintaining excellent power factor, frequency, flicker, quantity of administered dc current, and harmonics of the current. Especially in contrast to the traditional two-level inverter, the right control approach and Pulse Width Modulation (PWM) methods, which have the least amount of passive filter needs, are needed to solve harmonic difficulties. To comply with grid codes, a suitable control method selection and grid synchronization approach are required.

Conventional multilevel inverters have been categorized into three topologies named: the cascaded H-bridge MLI, the capacitor-clamped MLI, and the diode-clamped (Neutral point clamped) MLI. A neutral point clamped MLI, simply a three-level diode clamped inverter was suggested. Additionally, a number of other experts have employed the design at additional levels for a variety of purposes. Diode Clamped MLI divides levels using ‘n-1’ capacitors for n-levels and uses a common dc bus for all three phases. Diodes are used in the construction to minimize the voltage stress it has on power devices. The critical setback of the diode clamped MLI inverter is that its peak phase output voltage amounts to half the value of the dc source.

In 1975, a somewhat novel arrangement utilizing power switches with an H-bridge structure was suggested. Three levels can be produced at the output, +Vdc, -Vdc, and 0V, by one H-bridge using a single-phase full-bridge inverter. To create the necessary waveform, a cascaded H-bridge (CHB) inverter connects many of these H-bridges to separate DC sources. Every bridge has the capacity to increase the output by two levels. Because the setup uses minimal switches and without clamping devices, this structure only needs a minimal number of components. Using a variety of DC sources, including batteries and other renewable energy sources, this converter can create a waveform that is nearly sinusoidal.

Meynard and Foch (1992) presented a different type of multilevel inverter design called the flying capacitor inverter. Power switch configurations are comparable to diode clamped multilevel inverters. Instead of using diodes as a

clamping mechanism, capacitors are employed. The arrangement creates a ladder-like design of dc link capacitors, with the output voltage levels determined by the voltage differential between two neighboring capacitors. Figure 1.2 mentions the classification of MLI.

From the conventional MLI topologies, the most selected one for their operational simplicity and design is the CHB MLI. Due to its significance, it has been used in many applications, such as industrial applications for integrating renewable energy. Unlike FC and DC MLI, it’s notable since it does not require capacitors and diodes for voltage balancing. It's not like CHB MLI is without limitations; nonetheless, the CHB units need a separate dc supply, but proposed topologies, like (Babaei, et al. 2007), aim to get around this by utilizing a one dc source and less switches and less cost. Furthermore, additional advancements of MLI topologies, such as hybrid, modular, and impedance-based topologies, have been designed.

The numerous power switches seen in standard MLIs are a disadvantage as they increase the inverters' size and cost. Because a large number of capacitors are required at higher voltage levels, the flying capacitor MLI circuit design becomes more complicated. The capacity of three-phase inverters to deliver more power than single-phase inverters is one of their main benefits. Furthermore, a three-phase connection enables more efficient energy transmission and improved load balancing. This makes them the perfect option for heavy industrial and other applications requiring high power levels. Research efforts in MLI production work towards upgrading the topological designs and simplify the control systems. The objectives are; an increased stepped output voltage level while minimizing the amounts of components utilized in the system. This makes the system more effective and reliable, which this research mostly focuses on, a topology with increased levels of output voltage and less switches.

The conventional NPC MLI is integrated with the PV system; still, as mentioned by (Panda et al., 2018), an additional regulator must be used to retain the potential difference along each capacitor. PV panels can be used with CHB MLI; however, as the number of levels rises, additional PV panels must be paired in series or parallel. Consequently, when the inverter level rises, so does the number of

switches. Therefore, the quantity of switches needed in relation to the necessary voltage level is a crucial factor in building MLI. To arrive the same result as a 7-level CHB MLI, a recent topology is created with a decreased number of switches while also not adding more H bridges (Ahmed et al., 2010).

However, due to the lack of galvanic separation between the inverter and the grid, transformer less inverters are vulnerable to high-frequency leakage current, safety issues, and dc current injection. The parasitic capacitance connecting the ground and the frame of the PV panel is what causes the high-frequency leakage current. Single-phase and three-phase options are among the many solutions that researchers have developed. The primary goal of different types of single-phase inverters; (Li et al., 2015) and (Gu et al., 2013) is to achieve continuous common mode voltage using unipolar PWM along with more switches. Unfortunately, this approach is only capable of low power.

The dc bypass options are introduced, hence proposing three-phase inverter topologies (Freddy et al., 2015) and (Morris et al., 2017). These topologies have a lower time-varying common mode voltage (CMV) value even after they reduce the CMV amplitude to a specific point. To reduce leakage currents, the authors (Guo et al., 2015) proposed a novel architecture with additional switches added to the ac side. However, the three-phase inverter structures that were previously mentioned only include two-level inverter structures.

CHB MLI is categorized into two different groups: symmetric and asymmetric CHB. Only the voltage magnitudes of these two varieties of CHB inverters differ. Asymmetric topologies have different input voltage magnitudes compared to symmetric topologies, which have the same voltage magnitude for all their voltage sources.

Compared to symmetric topologies, asymmetric structures can produce higher output voltage levels. The asymmetric CHB can be further categorized into binary and trinary to regulate the magnitudes of the voltage source. They each have a different sequence to determine the magnitude of the voltage source. We will discuss more details in the next chapter.

Compared to a symmetric cascaded multilevel inverter, building the asymmetric MLI design will occupy less space and will cost less money while delivering equal output voltage levels of the symmetric design (Babaei et al., 2014). However, in order to reach the intended voltage levels, this effective multilevel system requires a sizable amount of power electronic devices, elevating the electrical stress placed on the switches and raising the system's cost (Dixon et al., 2010).

Among the proposed topologies, a popular converter that is used for photovoltaic applications is the cascaded H-bridge. These design applications include medium voltage equipment and power motors that utilize high power. The arrangements have the H-bridge cells in series in an asymmetric setup connected to separate voltage sources. However, to prevent fluctuation voltage in the solar setup system (Yu et al., 2016), they employed a dc-to-dc step converter with high-frequency separation. For the three-phase, assume the number of modules as ‘n’; the multilevel inverter will output voltage steps of 2n+1 having symmetric configuration; because of its flexibility, this gives a chance to connect enormous amounts of modules together to even further increase the output power levels.

More significantly, (Blaabjerg et al., 2006) provide an explanation of power electronics applications in renewable energy systems. Topologies for solar and wind applications, both onshore and offshore, were offered by the authors. A detailed explanation of how voltage and frequency control are affected by reactive and active power in relation to performance behavior was provided. Power inverters appropriate for renewable energy were examined by (Sekar et al., 2017). Three phase cascaded transformer MLI arrangements have been researched; in this study, the transformer’s secondary windings are linked in series to deliver space isolation between the two sides, the dc and ac. Surendra Babu et al. (2014) presented an inverter that has two levels used for STATCOM, the multilevel inverter makes a connection to the side that the lower voltage of the transformer, and the high voltage side is connected to the grid system.

The primary integration topologies used for renewable energy integration are suggested in (Paulino et al., 2011). Several inverter topologies were shown in the paper, including three phase full-bridge, fly-back, NPC, and Z-source inverters. In

addition, the article discussed their advantages and unique impact on the integration of renewable energy sources.

Furthermore, the multilevel inverter circuit needed for the integration was created by (Amamra et al., 2017). The discussed inverter which had six levels was solely constructed on the pulse width and height modulation technique. The researcher concluded that to minimize power loss and successfully remove fundamental harmonics, a low switching frequency technique would be preferable. Furthermore, compared to other inverter topologies, it requires minimal power electronic switches as well as proper gate drivers, which reduces maintenance costs.

Problem Statement

MLI are now essential parts of the systems that produce and supply electricity. However, they have some flaws that academic experts are working on improving. Among these disadvantages, the efficiency problem is a crucial restriction. Size, volume, cost, and conversion losses are a few variables that either directly or indirectly affect efficiency. Renewable energy sources have shown a significant integration due to their development technology, which has lower costs and dependency, and its calculated usage of their power will just keep rising. With those expectations, nevertheless, pose a challenge, to mention a few: the need to improve the panels in solar PV, increase the number of power electronic inverters, and constant maintenance in order to achieve the highest efficiency with more voltage levels, furthermore, output more power.

The overall amount of components used in the inverter design, particularly the semiconductor switches and dc power sources, influences the cost, increases the volume and size, and increases the losses from conduction and switching. Power electronics are essential to power systems and cannot be substituted by alternative devices; nevertheless, they can be redesigned or built to minimize these problems, enhancing the inverter's effectiveness and performance.

Purpose and Objective of the Thesis

In this thesis, the aim is to propose symmetric and asymmetric DC source analysis of an improved single-phase H-bridge multilevel inverter, and design a

topology that reduces and overcomes the problems we stated in the previous section. The objective is a topology that has less components; input dc sources and power switches that generate elevated output voltage levels, that has quality waveforms with less distortion and better efficiency. The proposed methodology is single-phase H-bridge MLI with 12 switches and 6 dc voltage sources. This will result in having a minimum size, less cost and higher efficiency.

The novelty in this thesis is designing, simulating and analysis of symmetric and asymmetric inverter, an improved one to that of conventional inverter. The scope of the project is comparative analysis and performance evaluation, simulation is carried out to achieve a quality output waveform with less losses that validates the theory concept.

The Importance of the Study

The importance of the thesis is to illustrate the impact that different topologies of MLI will have on applications with increased efficiency without adding more complex devices, and the difference between symmetric and asymmetric topology and the arrangement of the switches, gate drivers, and voltage sources has on the overall performance. Renewable energy sources, for example, solar cell supply, are considered among the productive sources over a long period of time with less maintenance. In order to utilize the captured electricity in an interrelated grid system, it must also be linked to the utility grid. The recovered power will be beneficial if reduced harmonic inverter results and effective control strategies are used. Proposing a power electronic device to convert the energy is crucial, a topology with less dc source, installation area, switches, and higher efficiency and performance.

Limitation of the Thesis

Since the thesis is based on simulation, it has few restrictions on the research, but regardless, it could still pose some difficulties with the application tools and the software version being used. The simulation is being carried out by the software PSCAD, which has minimal inconsistency with the simulation results and the experimental setup. Therefore, the limitation of the study does not result in a big impact.

Thesis Organization

The content of the thesis is categorized into sections, chapters which follows as:

- Chapter 1: Introduction; Overview, Problem Statement, Purpose and Objective of the Thesis, The Importance of the Study, Limitation of the Thesis, Thesis Organization.
- Chapter 2: Literature Review of Multilevel Inverters.
- Chapter 3: Proposed Single-Phase H-bridge Topology and Simulation Results
- Chapter 4: Conclusion.

CHAPTER II
Literature Review

Overview

The demand for a better quality of electrical power in this modern time is increasing drastically, and the conversion of energy from one form to another is very important. With this high interest, the use of renewable energy for additional sources has been gaining more popularity due to its less impact on environmental issues. Renewable energy is usually dependent on factors, and their power generation is not usually constant every time; for example, solar PV systems depend on sunlight and changes during the night. The EU, USA, and China have been at the forefront of producing enormous amounts of power from renewable energy in recent years. China is taking the lead with the highest generated power. Figure 2.1 shows that the capacity has increased more than double in the last four years, with solar PV having an incredible increase from 20GW to 80GW.

Some of the advantages of renewable energy:

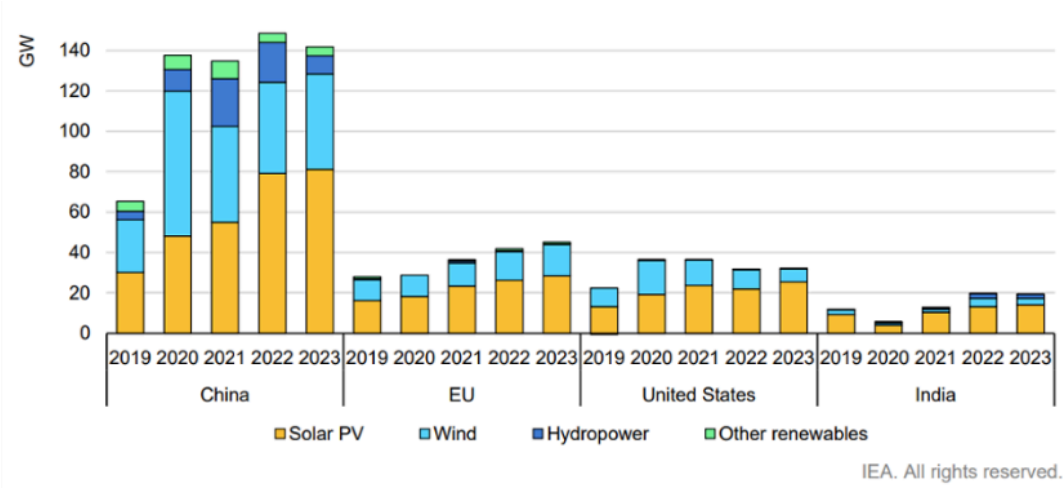
- Renewable sources of energy supplement traditional power generation, making it more reliable.
- Renewable energy sources provide long-term sustainability.
- Compared to conventional approaches, renewable applications generate little or no harmful substances that are released into the environment.
- Both the original and ongoing costs are reduced.

The disadvantages:

- Reliability concerns, some depend on weather which affects the generation of electricity.
- Energy storages are required, for example batteries due to the fluctuation changes
- Installation area, they require a large space if large-scale system is used.
- Grid integration will be difficult and requires changes to the existing infrastructure.

Figure 2.1

Renewable Capacity in China, EU, US and India, 2019-2023. (Michael O'Boyle, 2023)



PV applications need less fluctuation of energy and maximize the efficiency of solar cells; PV inverters are a big part of that. Inverters change the direct current output from the solar panels into alternating current. Multilevel inverters (MLI) are able to generate various stepped output voltage levels using one or many dc sources, MLI output voltage levels can range from three levels to more. The more the levels produced, the improved quality waveform of the load. MLI are the best devices for applications of high-power. Decades ago, the MLI principle was first implemented. The first functional multilevel inverter was the Diode Clamped MLI, which was initially developed in 1980 by (Nabae et al., 1982).

A survey of the literature on the present situation of inverters is discussed in this chapter. A summary of the PV system setups is provided. Classification of multilevel inverters, MLI topologies. The main areas of this review include power circuits, modulation strategies, topologies with a focus on reducing design components.

Solar Photovoltaic System

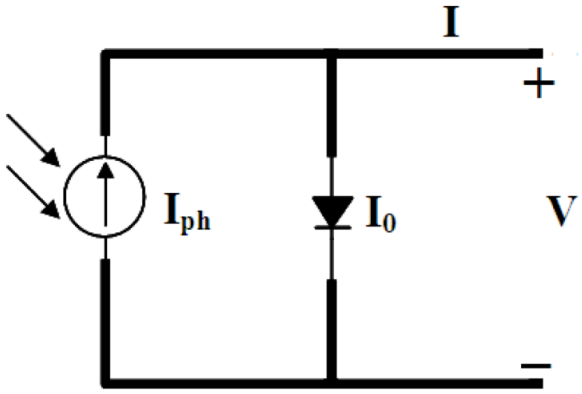
Photovoltaic cells are designed to harness the photovoltaic effect, whereby sunlight striking the surface of the PV panel is converted into electrical energy by the PV cells. Currently, polycrystalline, monocrystalline, and amorphous silicon, among others, are the prevailing semiconductors utilized in the production of solar power cells. To overcome the limitations of just one cell's power, numerous cells are linked

in series and parallel to create a more powerful photovoltaic array. In current panel modules, this is achieved by connecting 72-96 cells in series and using three to four bypass diodes to connect substrings of the panels. Whenever PV cells are joined in series and parallel, their generated voltage, as well as current flow, rise proportionally. Figure 2.3 illustrates the behavior and attributes of the current and voltage in a typical photovoltaic module under certain working circumstances, as shown through the current-voltage (I-V) curve. A source of current and a diode linked in parallel may be seen as a standard solar power cell. Figure 2.2 illustrates the perfect solar cell's equivalent circuit. As an example of a Shockley solar cell, consider the current-voltage characteristic:

$$I = I_{ph} - I_0 \left(e^{\frac{qV}{KT}} - 1 \right) \tag{2.1}$$

Figure 2.2

Ideal Solar Cell Equivalent Circuit (Zhao et al., 2011)

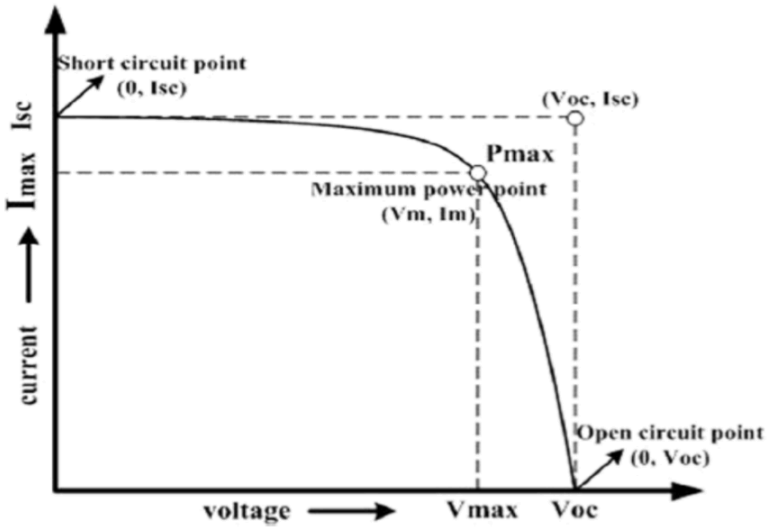


Where K stands for the Boltzmann fixed, V for the terminal voltage, and q for the electron charge. The total heat output is denoted by T. The generated current is denoted by I_{ph}, while the diode saturation current is denoted by I. Figure 2.2 displays the I-V characteristic of a perfect solar cell. In an ideal scenario, the open circuit voltage V_{oc} and the generated current I_{ph} are equal.

$$V_{oc} = \left(\frac{KT}{q}\right) \ln \left(1 + \frac{I_{ph}}{I_0}\right) \tag{2.2}$$

Figure 2.3

The Current Voltage Curve (I-V) (El-Ahmar et al., 2016)



Array Configuration

To achieve the intended terminal voltage and current, photovoltaic arrays on solar energy systems may be configured in parallel, in series, or in a hybrid configuration. While it is possible to attain higher voltages with a series string configuration. A combination of series and parallel layout is therefore frequently employed, this facilitates the amplification of current and voltage, ultimately leading to the completion of the desired power level. Five distinct categories of inverters can be distinguished: Central, string, multi-string, AC module, and cascaded inverters are among the numerous forms of inverters.

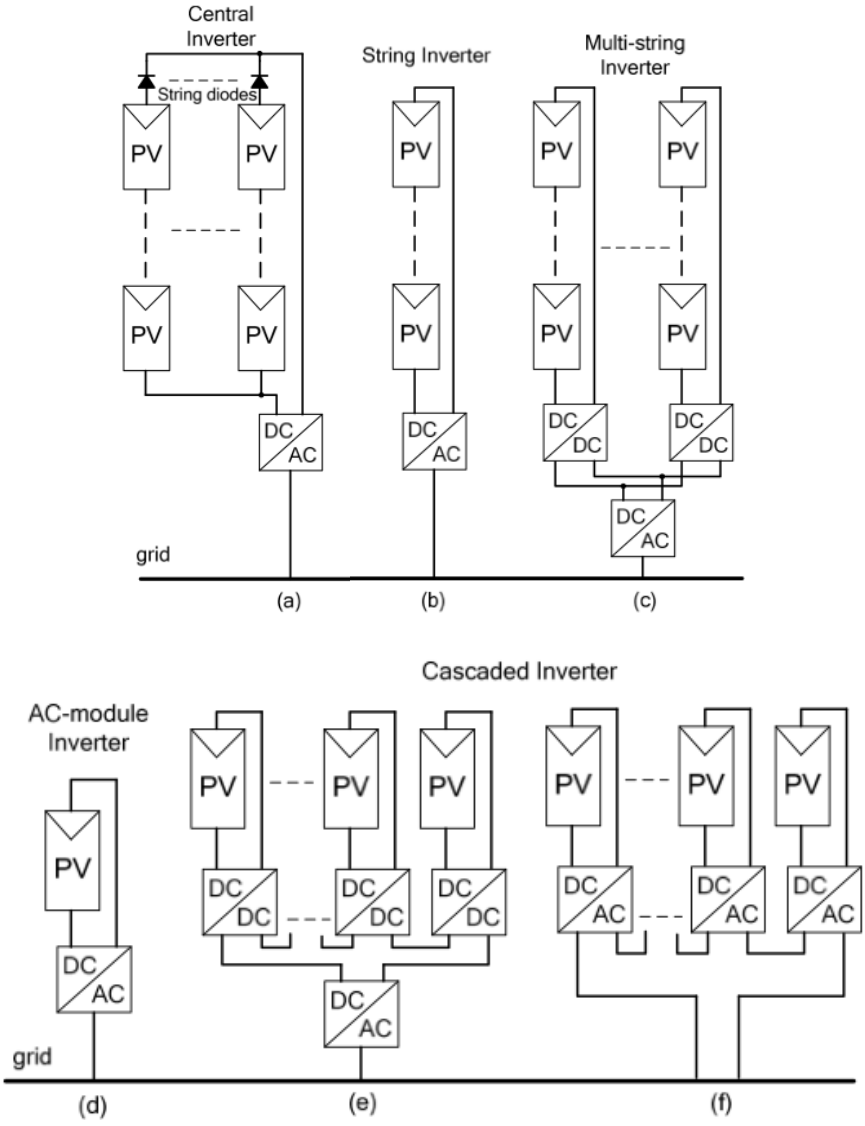
Central inverters are often regarded as outdated technology in the context of solar power systems. The centralized MPPT control leads to insufficient flexibility to customer needs, as well as increased electrical discharge hazards and losses in DC cables, string diodes, and PV module mismatches. As seen in Figure 2.4(a), Its architecture offers a higher power capacity compared to string inverters, exhibits superior inverter efficiency and cost-effective. For medium to large size photovoltaic projects, central inverters remain the most suitable choice.

String inverters are specifically intended to be used in photovoltaic systems that include just 1 PV string, as seen in Figure 2.4(b). As no string diodes are there and their related losses, it is possible to apply individual MMPT to each PV string.

Therefore, compared to the central inverter configuration, the overall efficiency is enhanced. String inverters are particularly effective for smaller-scale projects, particularly in situations where there is little space to place the modules in a consistent direction and the shadowing is unexpected.

Figure 2.4

(a) Central Inverter (b) String Inverter (c) Multi-String (d) AC-Module (e),(f) Cascaded Inverter (Mateus et al., 2022)



Multi-string inverter, seen in Figure 2.4(c), is an improvement compared to string inverters (Meinhard et al., 2000), (Schonberge et al., 2009). The advantages of string technology may be maintained in multi-string inverters, which allow them to achieve higher power levels. An electrical device that integrates the inverter and PV

module is the AC-module inverter, depicted in Figure 2.4(d). This structure minimizes the losses caused by incompatibility between PV modules by connecting the AC-module inverter directly to a single PV panel. There are two distinct types of cascaded inverters that are now available. Figure 2.4(e) illustrates a dc to dc converter cascaded arrangement of PV modules. There is a dedicated dc to dc converter on each PV module.

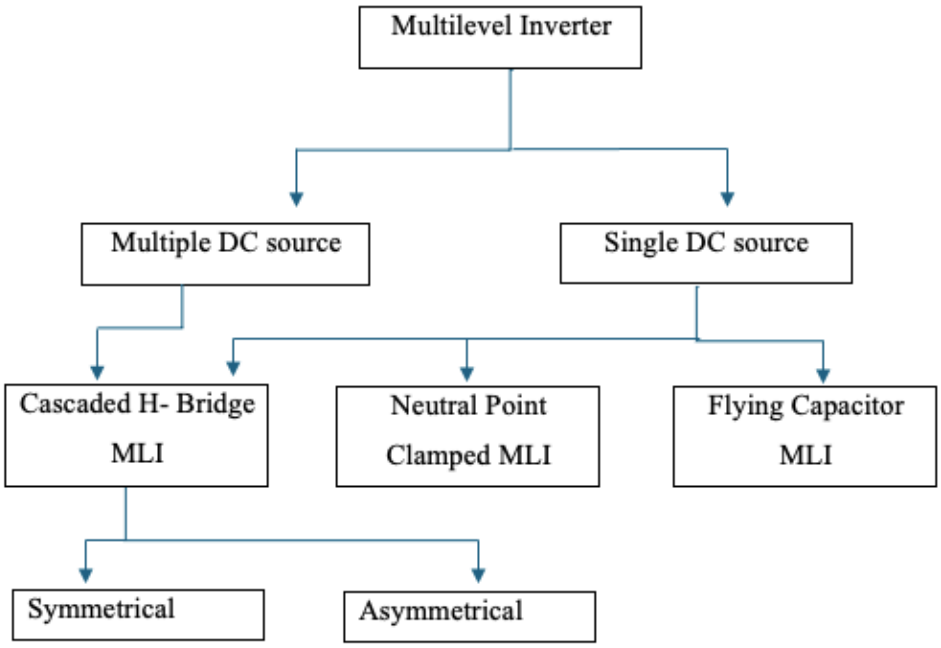
Figure 2.4(f) displays an additional cascaded inverter, where individual PV panels are coupled to their corresponding dc-ac inverters. The inverters are connected in series to attain a heightened voltage step. This cascaded inverter will preserve the advantages of the "converter per panel" approach while enhancing the utilization of each PV module, integrating multiple sources, and guaranteeing system redundancy.

Multilevel Inverter

A multilevel inverter receives input voltages from one or many dc sources and turns them into the required alternating voltage. Renewable energy sources, solar cells and fuel cells provide this direct current voltage source. The fundamental concept behind this design is to generate a staircase output voltage waveform that resembles a sinusoidal shape. Figure 2.5 illustrates the classification of MLI.

Figure 2.5

Classification of MLI



H-Bridge MLI, Diode Clamped MLI (Neutral Point Clamped), and Flying Capacitor MLI topologies are the three traditional designs for multilevel inverters. Modern technology encompasses several complex inverter configurations, such as hybrid MLI, modular MLI, and impedance-based MLI.

Diode Clamped MLI

A conventional topology, the diode clamped multilevel inverter, also known as Neutral Point Clamped (NPC) inverter, clamps the input voltage using a series of diodes. Implementing this topology guarantees an even dispersion of the source voltage throughout the capacitors that are linked to both the input and the output. Diode clamped topology, in contrast to some inverter topologies, solely necessitate a single direct current input voltage.

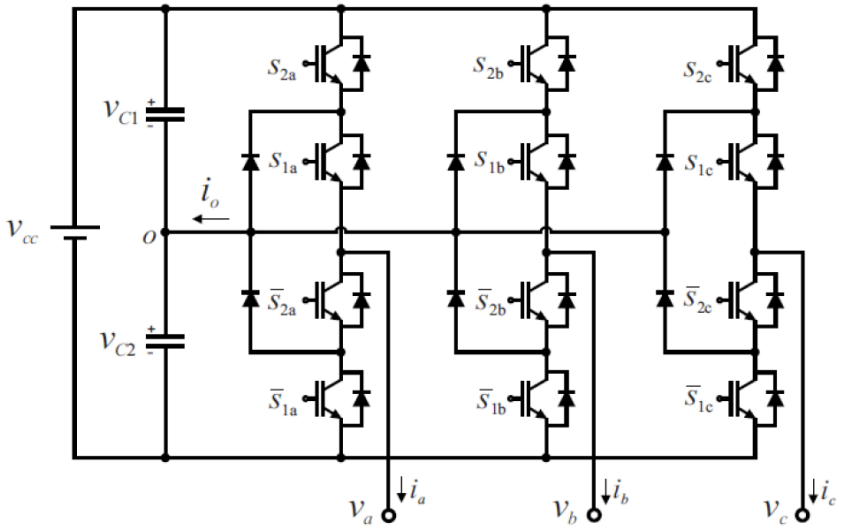
The overall quantity of diodes used for this design may vary, particularly when larger output voltage levels are desired, and lots of diodes are required for the clamping objective. The diode clamped topology utilizes only one dc voltage source. The maximum it can produce is half the input dc voltage. The quantity of capacitors connected to each output step in a clamping diode circuit dictates the number of output steps. The diode clamped topology will get complex and use many components with many levels desired, this is one of the limitations of NPC inverters**.**

Nabae et al. (1982) suggests a diode clamped topology. The dc link voltage of a 3-level DCMLI is classified into three discrete levels. As illustrated in Figure 2.6, this is accomplished by connecting two bulk capacitors in series. The NPC architecture comprises twelve semiconductor switches, 1 dc source, 6 CD (clamping diodes), and 2 capacitors for the three-phase MLI. The NPC topology has the ability to provide three distinct levels of output voltages: 0V, +1/2 E_d, and −1/2 E_d. Assuming that both capacitors receive an identical voltage from the source, the subsequent equation can be utilized to represent their respective voltages:

$$V_{C1} = \frac{1}{2}V_{cc} = V_{C2} = \frac{1}{2}V_{cc} \tag{2.3}$$

Figure 2.6

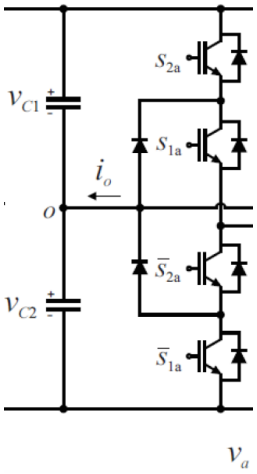
Three Levels NPC (Fuerback et al., 2013)



Following its first presentation by (Nabae et al., 1982), other researchers have proposed versions of diode clamped MIL structures. Increased levels are attained by altering the circuit architecture of the original topology circuit, improving the different PWM methods; topologies aim to reduce the quantity of clamping diodes while minimizing the usage of semiconductor switches.

Figure 2.7

NPC



The standard neutral point clamped single-phase setup is shown in Figure 2.7. The existence of this structure led to the development of the T-type NPC and active NPC topologies. Various alternate configurations for neutral point clamped inverters

have been created due to changes made to the basic NPC construction. Here are some NPC inverters:

I. Active NPC
II. T-Type NPC

The fundamental premise of the topologies mentioned is to reduce the number of clamping diodes and enhance control flexibility, taking advantage of the fixed nature of diodes. To create the active NPC inverter, the clamping diode of the standard neutral point clamped inverter is replaced by an active switch. A T-type Neutral Point Clamped configuration, sometimes referred to as a switch clamp, is created by using bidirectional switches to link the neutral point to the output point. The following figures illustrate the ANPC and T-type NPC configurations. These configurations are generated using a 3-level clamping diode inverter.

Figure 2.8

(a) ANPC (b) T-NPC

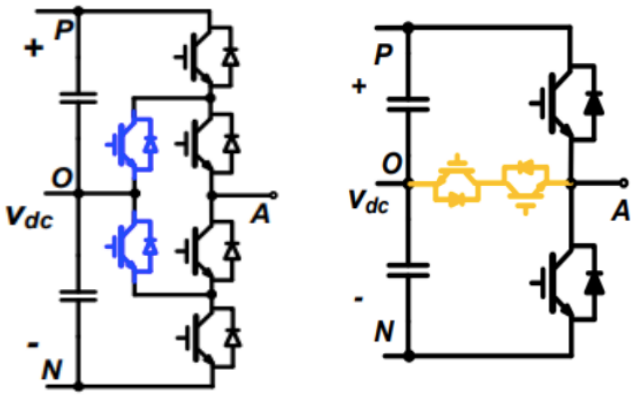


Figure 2.8(a) illustrates the power circuit of the proposed ANPC topology, which substitutes the clamping diodes of the traditional design with unidirectional power switches. Figure 2.8(b) illustrates the circuit of the T-type NPC. Bidirectional switches are used as substitutes for the typical restraining diodes seen in construction. During every switching cycle, the maximum voltage that may be blocked by every semiconductor switch must be equal to half of the direct current supply. The occurrence of reduced harmonics is a direct result of a meticulously controlled

inverter, which effectively eliminates sudden fluctuations in both positive and negative voltage levels (E and -E).

Nonlinear power converters offer several benefits, such as the ability to control reactive power and mitigate harmonics at higher levels. However, they also come with certain drawbacks, such as the need for a significant number of diodes at higher levels and the difficulty of regulating the actual power flow of individual converters (Lai & Peng, 1996).

Figure 2.9 illustrates a 3-phase 7-level diode clamped inverter. a common dc link are shared among the three phases, which is further split into seven levels by utilizing six capacitors. The voltage difference applied to every switching component is restricted to a maximum of V_{dc}, and the potential difference drop on each capacitor is likewise bounded to V_{dc}, along the presence of clamping diodes.

Figure 2.9

Three-Phase Diode Clamped Inverter for 7 Levels (Islam et al., 2014)

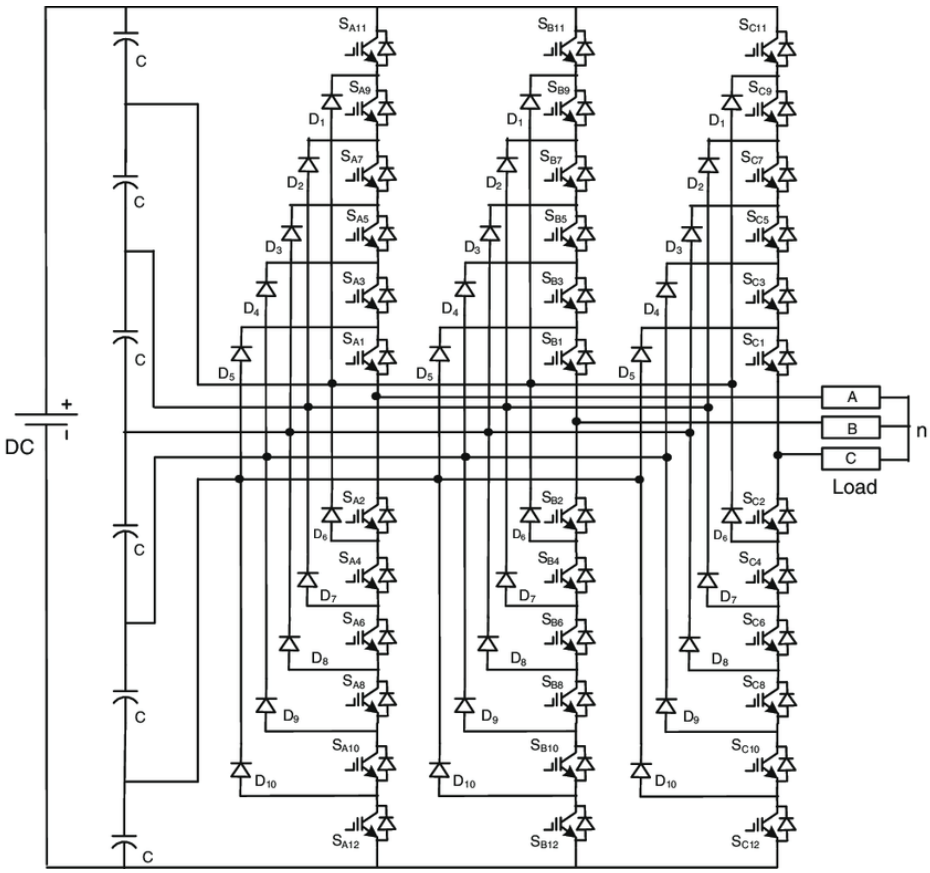


Table 2.1 displays the various output voltage levels associated with a single phase of the inverter in relation to the negative value reference voltage V_o. The status condition is represented by a numerical value between zero and one, which corresponds to the state of the switch (on or off). During a phase, deactivating one set of switches necessitates the corresponding action of activating the other set of switches. The switch patterns in phase 'a' are represented as S_{A1}, S_{A12}, S_{A3}, S_{A10}, S_{A5}, S_{A8}, S_{A7}, S_{A6}, S_{A9}, S_{A4}, and S_{A11}, S_{A2}. To address the voltage balancing problem, it is possible to handle it by incorporating advanced control mechanisms or introducing an extra balancing circuit.

Table 2.1

7-Level DC Inverter Voltage Levels with the Semiconductor Switches

Voltage	**Switch States**											
V	**S_{A1}**	**S_{A3}**	**S_{A5}**	**S_{A7}**	**S_{A9}**	**S_{A11}**	**S_{A12}**	**S_{A10}**	**S_{A8}**	**S_{A6}**	**S_{A4}**	**S_{A2}**
$V_0 = 0$	0	0	0	0	0	0	1	1	1	1	1	1
$V_1 = V_{dc}$	1	0	0	0	0	0	0	1	1	1	1	1
$V_2 = 2V_{dc}$	1	1	0	0	0	0	0	0	1	1	1	1
$V_3 = 3V_{dc}$	1	1	1	0	0	0	0	0	0	1	1	1
$V_4 = 4V_{dc}$	1	1	1	1	0	0	0	0	0	0	1	1
$V_5 = 5V_{dc}$	1	1	1	1	1	0	0	0	0	0	0	1
$V_6 = 6V_{dc}$	1	1	1	1	1	1	0	0	0	0	0	0

The line voltages Vab, Vbc, and Vca are formed by the voltages across the phase legs between the a to b, b to c, and c to a. A diode clamped inverter with n levels produces a phase voltage output at the n level and a line voltage output at the (2n-1) level. When all bottom semiconductor switches from S_{A12}, S_{A10}, S_{A8}, S_{A6}, S_{A4} to S_{A2} are turned on, the diode D_6 must obstruct five voltage levels, namely $5V_{dc}$, as specified in Table 2.1 for the first phase named 'a'. D_2 has to prevent the flow of $2V_{dc}$, similar to how D_1 needs to prevent the flow of $4V_{dc}$. Additionally, D_2 must also block the flow of $2V_{dc}$. The diodes needed for each phase of the inverter is calculated by the formula (m-1) x (m-2), where m indicates the number of diodes linked in series. This is because every blocking diode does have an exact voltage rating. Possible applications of DC inverter:

1. The production of static VARs
2. Variable speed control of high-power drives
3. AC and DC transmission lines for high voltage

Mailah et al. (2012) presented a 5-level NPC MLI to decrease the total current in the distribution line. Furthermore, the input voltage may be amplified by a substantial factor if necessary. The restraining diode in this specific topology has a significant magnitude, particularly in the three-phase configuration. An advantage of using the neutral clamped topology is that it leads to a decreased cost for the inverter design. This is accomplished by eliminating the need for an output filter, which becomes crucial at higher output voltages to reduce the presence of harmonics. The three-phase design comprises a single direct current voltage source, a total of four capacitors, eighteen clamping diodes, and eighteen unidirectional power switches. The levels produced at the output: 0, $\frac{\pm V_{dc}}{2}$, $\frac{\pm V_{dc}}{4}$, for the switching of the semiconductor has a blocking voltage step; $\frac{V_{dc}}{(n-1)}$.

The given topology has many benefits:
1. Decreases in the ratings of clamping diodes
2. The number of components is reduced
3. Reduces system costs
4. Ratings for switches decreased
5. Utilization of the traditional pulse width modulation method

The proposed architecture combines an impedance source (Z-Source) with a NPC inverter, as first suggested by (Xing et al., 2014). This architecture allows for the optimal combination of the most beneficial features from both topologies. The impedance-based topology offers the capacity to do buck-boost operations and exhibits resistance to electromagnetic radiation as a result of its shoot-through state.
The advantages are:

1. Used back-to-back systems, more than one power conversion states are connected.
2. Pre-charging the capacitor device in advance.
3. The efficiency of fundamental frequency switching is very high.

Disadvantages:

1. The presence of intermediate dc levels may cause overcharging or discharging if not closely monitored, making it challenging to accomplish real power flow with a single inverter.
2. A device with an increased number of levels will need many clamped diodes.

Flying Capacitor MLI

The Flying Capacitor (FC), also known as a capacitor clamped inverter, employs a series connection of capacitors to provide voltage clamping. They influence the magnitude of the graded voltage, despite only having one voltage source for the input voltage. The load voltage steps is defined by the quantity of capacitors in the closed loop circuit for each stage. Hence, the load voltage may be represented as the aggregate of the clamping capacitor voltages across all phases. According to (Lai & Peng, 1996), this sort of inverter has the benefit of not requiring clamping diodes. Due to the elimination of unnecessary repetition, just one dc supply is sufficient. According to (Sinha & Lipo, 1997), there are some advantages. The flying capacitor topology has many benefits, including:

- Harmonic distortion is reduced.
- Decreasing costs by removing the need for an output filter.
- They are utilized in applications that need high voltage.
- They are used to correct reactive power.
- Appropriate for integration into photovoltaic systems.
- The use of clamping diodes are not needed.

To effectively control inverters and maintain the efficiency of high-power systems, it is necessary to use a larger number of capacitors. However, this may lead to increasing switching losses, as shown by (Lai & Peng, 1996.). A further issue related to flying capacitor connections that need initialization and control is the usage of redundant levels. Figure 2.10 depicts a traditional FC multilevel inverter consisting of five levels. It is a network consisting of three cascading capacitors and one independent capacitor. The topology is constructed using a total of 10 clamping capacitors, 1 dc source, and 8 semiconductor switches.

Figure 2.10

FC Inverter 5-Level (Lai & Peng, 1996)

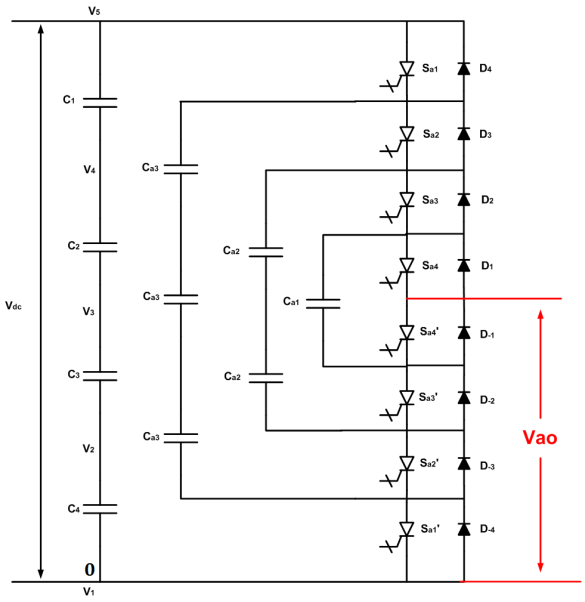


Table 2.2

5-Level FC Inverter Switching Pattern

Voltage Output	SW_{a1}	SW_{a2}	SW_{a3}	SW_{a4}	$SW_{a4'}$	$SW_{a3'}$	$SW_{a2'}$	$SW_{a1'}$
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = \frac{3}{4}V_{dc}$	1	1	1	0	1	0	0	0
$V_3 = \frac{1}{2}V_{dc}$	1	1	0	0	1	1	0	0
$V_2 = \frac{1}{4}V_{dc}$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

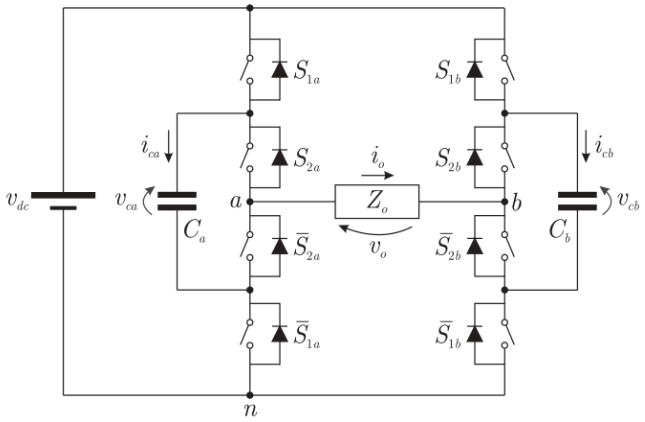
The authors (Saccol et al., 2019) conducted a thorough examination of a one phase HB FC that exhibits asymmetrical voltages, indicating that the voltage magnitudes are unequal. To enhance the stepped levels unchanging the number of semiconductors, one may include an asymmetric feature to avoid the complicated structures that come with very high output voltage levels. Figure 2.11 illustrates the configuration of the topology.

The topology has an H-bridge structure, with two legs: one for the v_{an} and the second v_{bn}. This topology can generate 4 levels of output for the load, for the output voltage is subtracting one leg voltage from the other leg. Each leg voltage drop has to

be controlled, which means to controlling the voltage across the capacitors, for the asymmetric FC inverter topologies pose difficulties to control it.

Figure 2.11

Single-Phase Asymmetric HB Flying Capacitor (Saccol et al., 2019)



Techniques were proposed to overcome it; the first technique, the capacitor voltage v_{ca} is evaluated to be twice the second capacitor voltage. For the second technique, the voltages are the same. The following parameters are defined:

$$v_0 = v_{an} - v_{bn} \tag{2.4}$$

$$v_{ca} = 2v_{cb} \tag{2.5}$$

$$v_{cb} = \frac{2}{n-1} \tag{2.6}$$

$$v_{ca} = v_{cb} \tag{2.7}$$

$$v_{cb} = \frac{2}{n-1} \tag{2.8}$$

Where ‘n’ stands for number of stepped levels

Le and Lee (2016) proposed a novel inverter design that combines two-level and flying capacitor inverter topologies. The given topology is classified as a hybrid topology due to its derivation technique, which enables it to supply six various levels of load voltage. When the charging and discharging operations of numerous capacitors are combined, the output voltage levels are the same. The voltage levels produced by FC MLI are very versatile and efficient. Reducing the size, volume, and weight of the inverter might be possible by using a less quantity of circuit components. Compared to inverters with a higher number of components, this one has better efficiency. This design does not reduce switching loss. The provided topological structure is seen in

Figure 2.12. Aside from the eight unidirectional power relays, there are also four capacitors. The flying capacitor consists of three capacitors and four switches, while the two-level inverter only has one capacitor and 4 switches.

Figure 2.12

Hybrid Flying Capacitor Inverter (Le & Lee, 2016)

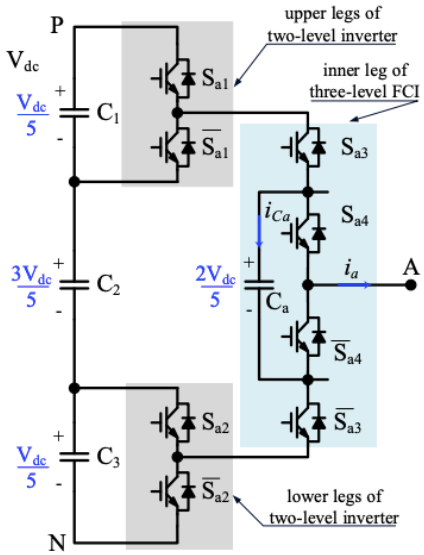


Table 2.3

Switching States 6-level Hybrid Flying Capacitor Inverter

Stages	SW_{a1}	SW_{a2}	SW_{a3}	SW_{a4}	V_{AN}	i_{Ca}
V_0	0	0	0	0	0	0
V_1	1	1	0	0	$\frac{V_{dc}}{5}$	0
V_2	0	0	0	1	$2\frac{V_{dc}}{5}$	$-i_a$
V_3	0	0	1	0	$2\frac{V_{dc}}{5}$	i_a
V_4	1	1	0	1	$3\frac{V_{dc}}{5}$	$-i_a$
V_5	1	1	1	0	$3\frac{V_{dc}}{5}$	$-i_a$
V_6	0	0	1	1	$4\frac{V_{dc}}{5}$	0
V_7	1	1	1	1	$\frac{V_{dc}}{5}$	0

Abdelhakim et al. (2017) introduced a new split source-based inverter (SSI) in their paper, which makes use of flying capacitors. Single stage SSI topologies have the ability to support a wide range of merits, including continuous dc link voltage and input current, by incorporating the FC topology into the SSI topology.

Figure 2.13 shows the SSI-FC architecture. The architecture has 12 switches, one input dc source, 4 capacitors, and 3 diodes. It is a three-phase configuration, each lower portion of the topology consists of two switches. The capacitance value may be calculated using equation (2.9), where ΔV_c represents the phase's peak current and $I_\emptyset$ signifies the peak ripple voltage. The inductors, capacitors discharging time, and voltages values is defined as:

$$C = \frac{I_\emptyset}{f_S \Delta V_c 2\sqrt{2}} \tag{2.9}$$

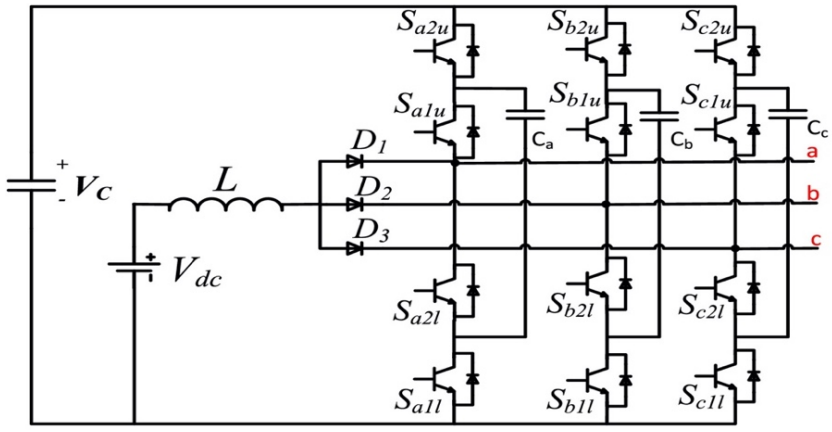
$$L = \frac{V_{dc}(2M-1)}{2 f_S \Delta I_L} \tag{2.10}$$

$$\frac{V_{in}}{V_{dc}} = \frac{1}{1-M} \tag{2.11}$$

$$\frac{V_\emptyset}{V_{dc}} = \frac{M}{1-M\sqrt{3}} \tag{2.12}$$

Figure 2.13

3-Level SSI-FC Inverter (Abdelhakim et al., 2017)



Cascaded H-Bridge MLI

The cascaded H-bridge inverter is created by connecting many H-bridge structures in a series. Each H-bridge inverter (cell) in a series system operates with its own dc source. While it is more common and organized to combine numerous single-phase H-bridge structures in series, parallel configurations are also feasible options for obtaining this topology. The stepped voltage levels that can be achieved by the

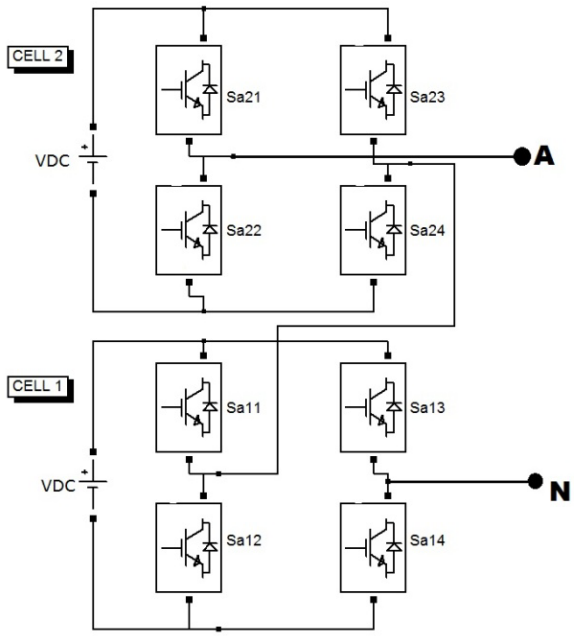
structure of CHB are based on the magnitudes of th dc links, size and the number of h-bridge units connected.

CHB MLI is a simpler form of inverter, as opposed to FCMLI and DCMLI. This inverter does not include capacitors and clamping diodes. A wide range of dc input sources, mostly consisting of renewable energy sources like wind, photovoltaics, and biomass, provide the many voltage levels for the output. The input voltage sources can be varied depending on the extent of your design and its purpose. The cascaded H-bridge inverter's voltage input sources, if they are all equal in magnitude, it is called symmetric topology. For the topologies with different input sources are called asymmetric.

The configuration of a single-phase system with CHB topology may be seen in Figure 2.14. This topology utilizes two H-bridge structure components to provide an output voltage with five levels. Increasing the units of H-bridge structure will result a higher output voltages (Tenconi et al., 1995).

Figure 2.14

CHB MLI (Teja et al., 2020)



Sa21–Sa24 are the input and output voltages for the "cell 1" H-bridge, which operates using Vdc and VA. The "Cell 2" H-bridge uses Sa11–Sa14 switches, with Vdc representing the input voltage and VN representing the output voltage.

The basic circuit configuration of the five-level CHB MLI is depicted in Figure 2.15. The aggregate load voltage is determined by combining the individual voltages of each module. H-bridge inverter has the ability to generate three separate outputs: V_{dc}, $-V_{dc}$, and 0. The ac voltage magnitude varies between $-2V_{dc}$ and $+2V_{dc}$ throughout the five levels. The output voltage has a waveform that closely resembles a sinusoidal pattern.

The cascaded H-bridge topology offers notable benefits in terms of its versatility and simplicity (Babaei, 2008). A further benefit of this system is its capacity to generate much greater voltage steps. The control information for the cascaded design is provided in Table 2.4.

Figure 2.15

Five level CHB MLI

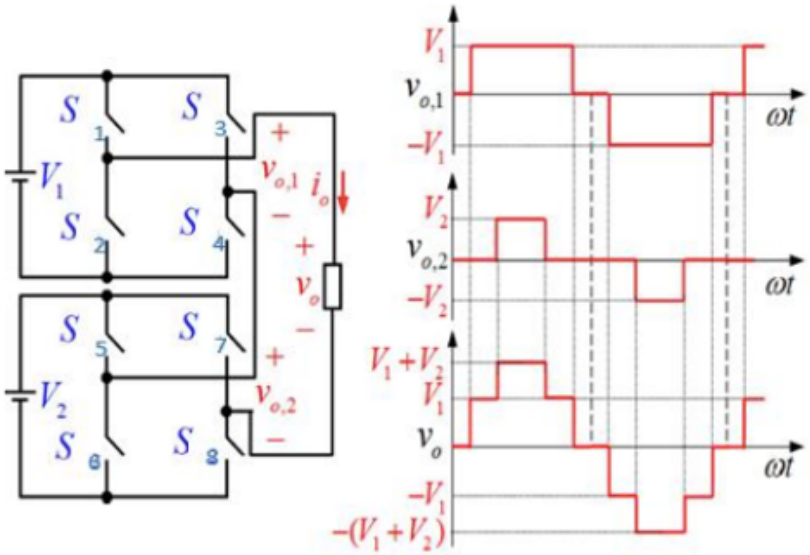


Table 2.4

5-Level CHB Inverter

V	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	SW_7	SW_8
V_1+V_2	1	0	0	1	1	0	0	1
V_1	1	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0
$-V_1$	0	1	1	0	0	0	0	0
$-(V_1+V_2)$	0	1	1	0	0	1	1	0

Soto et al. (2003) introduced a new and innovative design for 5-level cascaded H-bridge inverters. This design included interface inductors arranged in series circuits, together with a single direct current source. (Siddique et al., 2019) introduce an enhanced CH inverter. The basic unit is created by combining two bidirectional switches, unidirectional switch, and two direct current sources to the H-bridge architecture.

A fault-tolerant and hybrid cascaded H-bridge MLI topic was proposed by (Mhiesan et al., 2020). It presented that with the increased switches in the topology, there is a high chance the switches will have faulty switches, which results in less efficiency and dependability. A feature has been added to the topology throughout the H-bridges to ensure that the efficiency and dependability is not limited. The feature is one with an X-crossed shaped added to the H-bridge structure, which increased the stepped output voltage levels generated and the efficiency. Unfortunately, the price for the addition of the switches and devices will increase the cost of maintenance in regard to the gate drivers in the topology.

Symmetric and Asymmetric CHB MLI.

Both symmetric and asymmetric cascaded H-bridges are used in cascaded H-bridge multilevel inverters. The primary differentiation between the two categories of cascaded multilevel inverters is mainly based on the magnitude of the input dc voltage.

The example study shown in Figure 2.16(a) demonstrates that a symmetric topology is defined by input voltages of equal magnitudes in both cells. On the other hand, an asymmetric architecture involves different sizes of the input voltages in the two cells. Trinary and binary topologies are two further categories for asymmetric topologies. The categorization of diode clamped inverters as symmetrical or asymmetrical rely on the input dc voltage (Song-Manguelle et al., 2001). The equation below represents the output generation capacity of a symmetrical cascaded multilevel inverter. In the formula, the variable "n" stands the amount of full bridges units that are linked in series.

$$N_{step} = 2n + 1 \tag{2.13}$$

The difference between the trinary and binary asymmetric configuration is that trinary has higher output levels than the binary, and the ratio of their dc sources magnitudes differ. The input voltage ratio for a binary cascaded H-bridge MLI is one to two, as shown in Figure 2.16(b), provided that the quantity of input dc voltage and H-bridges connection are equal. Similarly, for a trinary CHB MLI, the input voltage ratio is one to three. An asymmetrical multilevel inverter is created by connecting two H-bridge modules in series. The number of output voltage stages for a binary inverter is seven, while for a trinary inverter it is nine. Asymmetric cascaded inverters use the same number of switches but provide a higher range of load voltage levels.

For symmetric cascaded topologies, the output voltage will be the total voltage of each cascaded unit $V_o=V_1+V_2+V_3$. The maximum output voltage

$$V_{o,max} = nV_{dc} \tag{2.14}$$

For the Asymmetric cascaded topologies, which the sources magnitude is two and three times the initial voltage source. The following expressions are used to determine the stepped levels;

$$\text{For 1:2 ratio :} \quad N_{step} = 2^{n+1} - 1 \tag{2.15}$$

$$\text{For 1:3 ratio :} \quad N_{step} = 3^{n} \tag{2.16}$$

The mathematical correlation between the several types of cascade H-bridge inverters is shown in Table 2.5. Babaei (2008), and (Babaei & Hosseini, 2009), presented the comparisons (Babaei & Moeinian, 2010).

The benefits:

1. Fewer components are needed compared to other multilevel inverters, regardless of the desired output voltage.
2. This inverter type is made more compact and easier to deploy by not using voltage balancing capacitors and clamping diodes.
3. Implementing soft-switching is necessary to reduce switching losses and minimize strain on the device when following this design.

Disadvantage is:

1. Each inverter requires its own individual DC power supply.

Figure 2.16

(a) Symmetric CHB MLI (b) Asymmetric CHB MLI (Prasadarao et al., 2015)

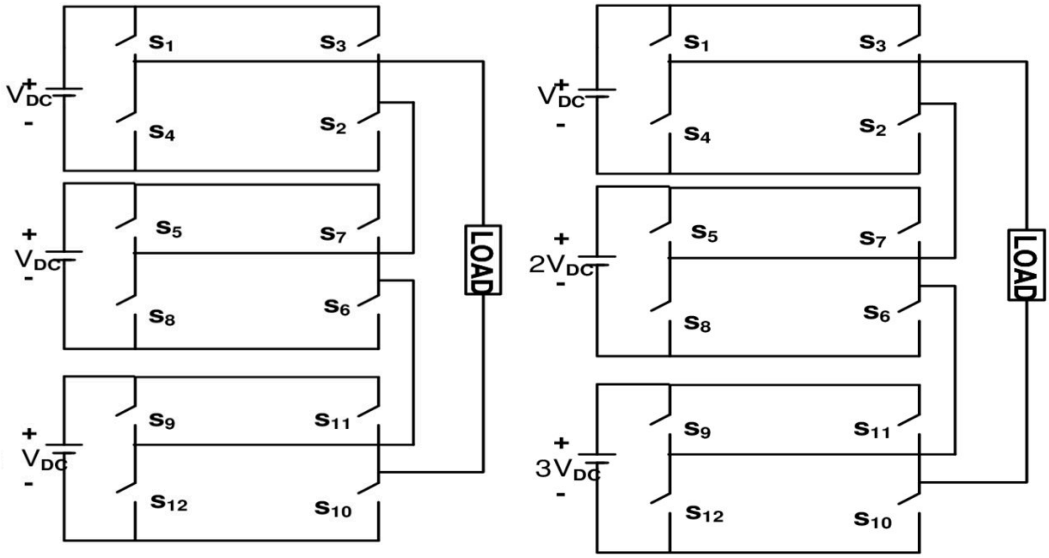


Table 2.5

Symmetric and Asymmetric Voltage Configurations

Variables	**Symmetric**	**Asymmetric**	
		Binary	**Trinary**
N_{step}	$2n+1$	$2^{n+1}-1$	3^n
V_n	V_{dc}	$2^{n-1}V_{dc}$	$3^{n-1}V_{dc}$
V_o	nV_{dc}	$(2^n-1)V_{dc}$	$\left(\frac{3^n-1}{2}\right)V_{dc}$
V_{stand}	$4nV_{dc}$	$4(2^n-1)V_{dc}$	$2(3^n-1)V_{dc}$

"n" represents the number of full bridges units

Where:

N_{step}	The steps generated
V_n	DC voltage sources used
V_o	Maximum voltage produced
V_{stand}	Total maximum voltage the switches can handle

All the conventional multilevel inverters mentioned above can be used depending on the components you will use and the number of generated voltage steps. The Table 2.6. below compares the components of MLI types needed for same output

level per phase. The comparison of MLI types in Table 2.6 illustrates that CHB MLI uses the least number of devices for the same output level. The DC sources are half the amount of the others, and they not necessarily need clamping capacitors or diodes.

Table 2.6

Conventional MLI Types Components Comparison

MLI Type	Neutral Point Clamped MLI	Flying Capacitor MLI	Cascaded H-Bridge MLI
DC link capacitors	$m-1$	$m-1$	$\frac{m-1}{2}$
Main diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Switches	$2(m-1)$	$2(m-1)$	$2(m-1)$
Transformers	0	0	0
Clamping capacitors	$m-1$	$\frac{(m-1)(m-2)}{2}$	0
Clamping diodes	$(m-1)(m-2)$	0	0

Where 'm' = voltage level, m = 3, 4, 5, 6, ...

Cascaded Multilevel Inverter Topologies

In this section, we will discuss other published multilevel inverter topologies, mainly the cascaded inverter topologies. Most of the topologies are recent developments, and some of them are improved inverters regarding the number of devices used, the efficiency, and the levels of output voltages produced. Cascaded topologies are not just limited to cascaded H bridge topology, but also the other conventional multilevel inverters can be made into cascaded topologies by connecting multiple units of the main topology together in series.

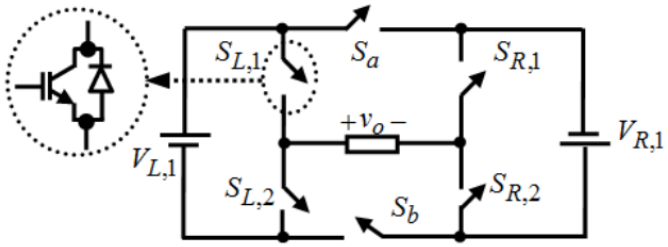
There are topology structures that can be constructed in different and modified designs; there are ones that do not produce negative output voltage levels, and some others do not have an H-bridge structure.

In their study, (Babaei et al., 2014) provided a new cascaded multilevel inverter architecture. The described topology is a result of structural improvements made to the traditional H-bridge topology. Figure 2.17 depicts the fundamental circuit configuration of this design. Regarding voltage, each of the six power switches in the

H-bridge functions in a single direction. Furthermore, this design integrates two voltage sources. This setup may provide seven different levels of voltage as its output; for the H-bridge, three levels are produced only. The potential magnitudes of the output voltage may vary between 0 and $\pm V_1$, as well as $\pm (V_1 + V_2)$. This topology is able to produce 7 levels if the magnitudes of the sources are chosen different, otherwise, if it's same, it only generates five output voltage levels.

Figure 2.17

Basic Structure MLI (Babaei et al., 2014)



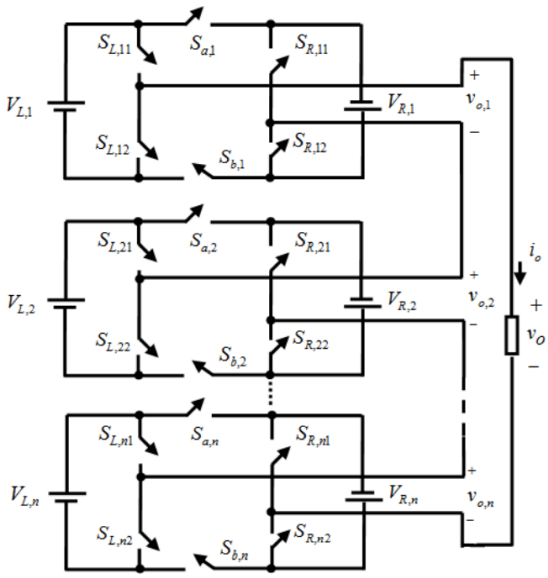
The cascaded units of the topology will produce more output voltage levels and maximum voltage, which will be the total voltages of Vo of each cascaded unit shown in Figure 2.18. For the number of switches, the equation used is:

$$N_{switch} = N_{IGBT} = N_{driver} = 6n \tag{2.17}$$

$$N_{Source,Variety} = 2n \tag{2.18}$$

Figure 2.18

Cascaded MLI (Babaei et al., 2014)



Aalami et al., (2018) proposed a novel cascaded MLI structure that integrates a limited number of components to achieve improved efficiency, decreased costs, and lower component sizes. The fundamental configuration of the proposed inverter is depicted in Figure 2.19 and Figure 2.20. The construction consists of 10 power switches and two direct current sources. The presented inverter amplifies the number of stepped output levels, representing an improvement compared to the conventional H-bridge architecture. This H-bridge layout deviates from the standard by having 7 stages at the output.

Figure 2.19

H-bridge Multilevel Inverter (Aalami et al., 2018)

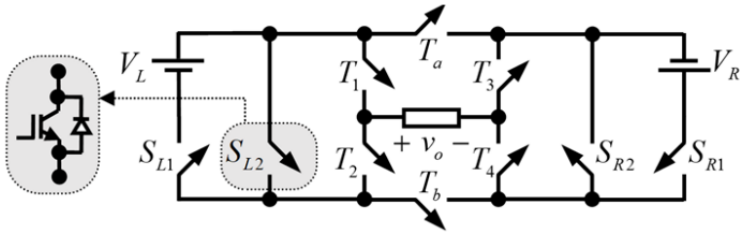
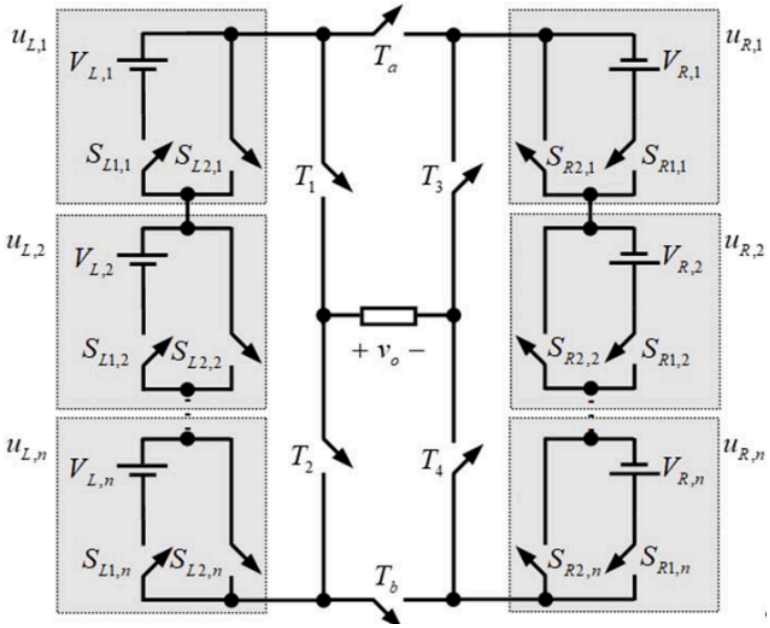


Figure 2.20

CHB MLI (Aalami et al. 2018)



The switching stages must have at least one switch turned ‘on’ from the left side (S_{L1}, S_{L2}) of the topology and one from the right side (S_{R1}, S_{R2}) and the ones from

the middle, the H-bridge design one switch from each square arm (T_1, T_3) and (T_2, T_4). The variables terms used are defined as:

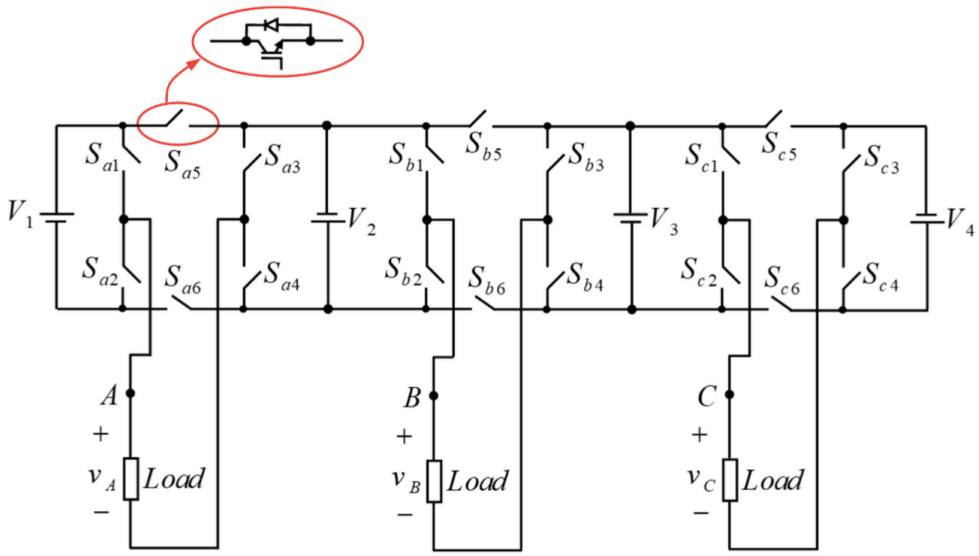
$$N_{switch} = N_{IGBT} = N_{driver} = 4n + 6 \quad (2.19)$$

$$N_{source} = 2n \quad (2.20)$$

The authors (Tackie & Babaei 2020) proposed a modified H-bridge multilevel inverter based for three-phase, it generated 7 level for the phase voltage and line voltages of 13 levels, positive and negative. There were no capacitors used, therefore no extra devices to balance voltages across them. The topology utilized less components, 18 unidirectional switches and 4 sources shown in Figure 2.21. The aim was to lower the size, cost and volume of the inverter, while enhancing the performance of the inverter and reducing the losses.

Figure 2.21

Three-phase MLI (Tackie & Babaei 2020)



Yahya et al., (2019) proposed a unique cascaded MIL approach. The given architecture is characterized by its low switching losses, efficient use of the dc source, and a small number of components, including switches. When comparing this design to the traditional H-bridge, it is clear that the former generates double the amount of voltage steps, got a modular structure, and utilizes switches with equal ratings. All these factors contribute to the simplicity of control and the circuits. The basic structure is seen in Figure 2.22. The H-bridge arrangement consists of four switches, with one

being unidirectional and the other three being bidirectional. The other components make up the rest of the structure. The H-bridge allows achieving both positive and negative levels. The parameters as follows:

$$V_{0,max} = (2n-1)\,V_{dc} \tag{2.21}$$

$$N_{step} = 4n-1 \tag{2.22}$$

$$N_{IGBT} = 2n+4 \tag{2.23}$$

$$N_{switch} = N_{driver} = n+6 \tag{2.24}$$

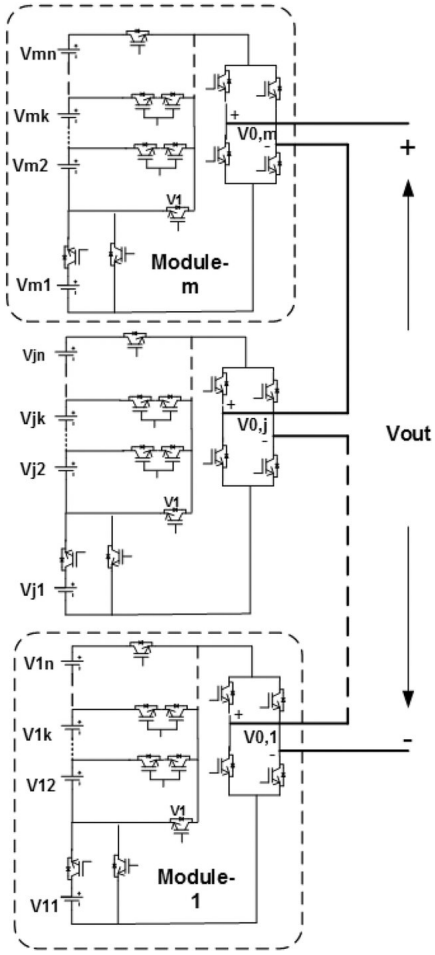
For more quality power the stepped levels have to be increased, for the voltage dc source ratio and the maximum output voltage are described as follows:

$$V_i = \begin{cases} 2^{i-1}V_{dc}, & i = 1 \\ 2^{(i-j)}V_{dc}, & i = 2,3,4,\ldots j = i-1 \end{cases} \tag{2.25}$$

$$V_{o,max} = (2n-1)V_{dc} \tag{2.26}$$

Figure 2.22

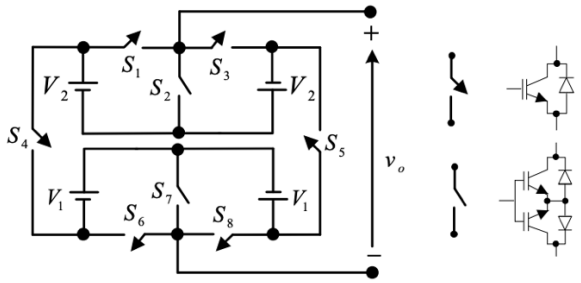
Cascaded MLI Topology (Yahya et al., 2019)



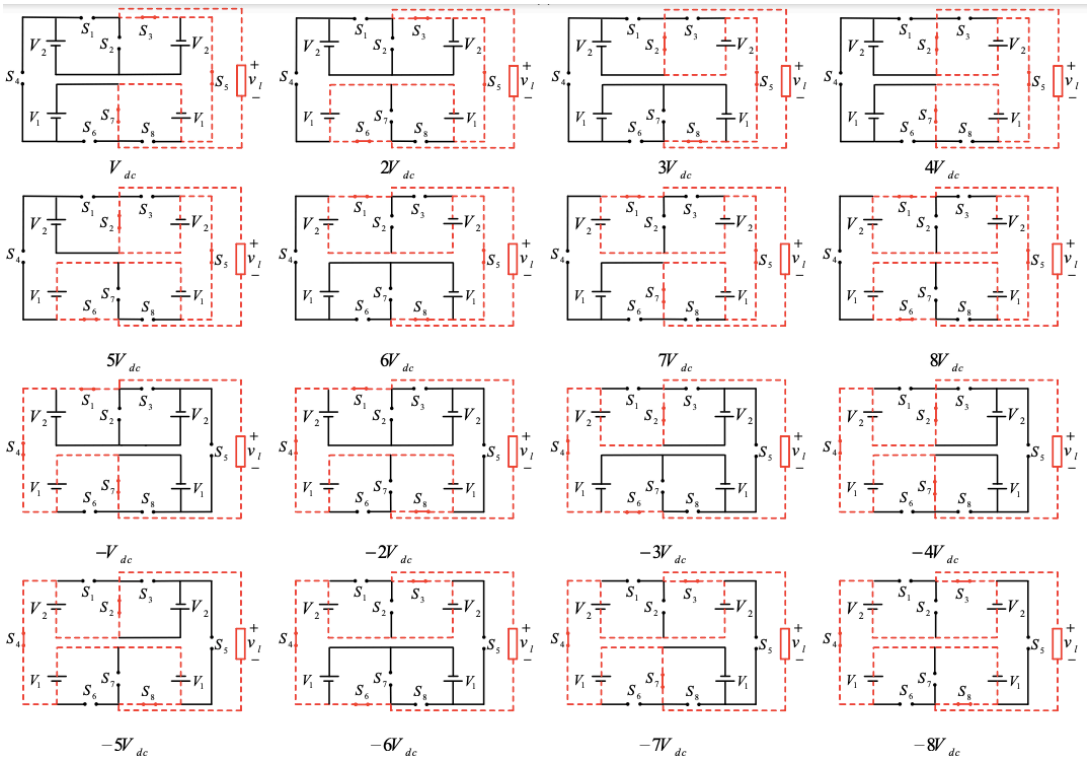
In 2016, (Sarbanzadeh et al., 2016) introduced a novel cascaded MLI design. This topology has used the unidirectional and bidirectional switches in order to achieve the power output needed and generated stepped output levels of seventeen levels, four input dc voltages, the switches are eight total. The proposed topology structure is shown figure 2.23(a), while the Figure 2.23(b) shows the stages path for the output levels. Further levels of output voltage can be achieved through cascaded circuits of the same basic structure connected in series. The characteristic of the topology different from some inverters is its capability to produce negative voltage without utilizing the basic H-bridge structure.

Figure 2.23

(a) The Presented Sub-level MLI (b) Switching Stages (Sarbanzadeh et al., 2016)



(a)



(b)

The MLI topology (Sarbanzadeh et al., 2016) from the circuit above the switches S_4 and S_5 are the switches used to determine the positive and the negative voltage steps. As illustrated in the Figure 2.23(b) when S_5 is closed (on), it produces positive values, while S_4 produces negative values. In case it is coupled in sub-modules inverter as cascaded, let's give sub-modules as 'n'; If the dc link values are all equal like $V_{1,1}=V_{2,1}$, the quantity of switches, the components and the maximum output voltage and the number of levels generated is shown below:

$$N_{switch} = 8n \tag{2.27}$$

$$N_{IGBT} = 10n \tag{2.28}$$

$$N_{driver} = 8n \tag{2.29}$$

$$N_{dc-link} = 4n \tag{2.30}$$

$$N_{level} = 8n + 1 \tag{2.31}$$

$$N_{variety} = 1 \tag{2.32}$$

$$V_{o,max} = 2\sum_{j=1}^{n}\left(V_{1,j} + V_{2,j}\right) = 4nV_{dc} \tag{2.33}$$

If the dc links are different and the topology is asymmetric, for example, if $2V_{1,1}=V_{2,1}$. Then the number of levels generated will be improved and the maximum output voltage:

$$N_{variety} = 2n \tag{2.34}$$

$$N_{level} = 13^n \tag{2.35}$$

$$V_{o,max} = 2\sum_{j=1}^{n}\left(V_{1,j} + V_{2,j}\right)V_{dc} = \frac{1}{2}(13^n - 1)V_{dc} \tag{2.36}$$

Krishnan et al. (2018) presented clear details of a cascaded MLI inverter. The design described consists of a central unit composed of 2 and 4 unidirectional and bidirectional power switches respectively. The vital unit operates on power delivered by two direct current sources. A study is conducted to evaluate the symmetrical and asymmetrical functioning of the given inverter. Figure 2.24 demonstrates the three-phase connection of the given topology. The suggested inverter topology enables the production of an output voltage with five to seven levels for symmetric operation and nine to fifteen steps for asymmetric operation, using one or two units. The binary magnitude for the voltage source arrangement The equations for the symmetric and asymmetric topology are as:

$$N_{switches} = 4N \tag{2.37}$$

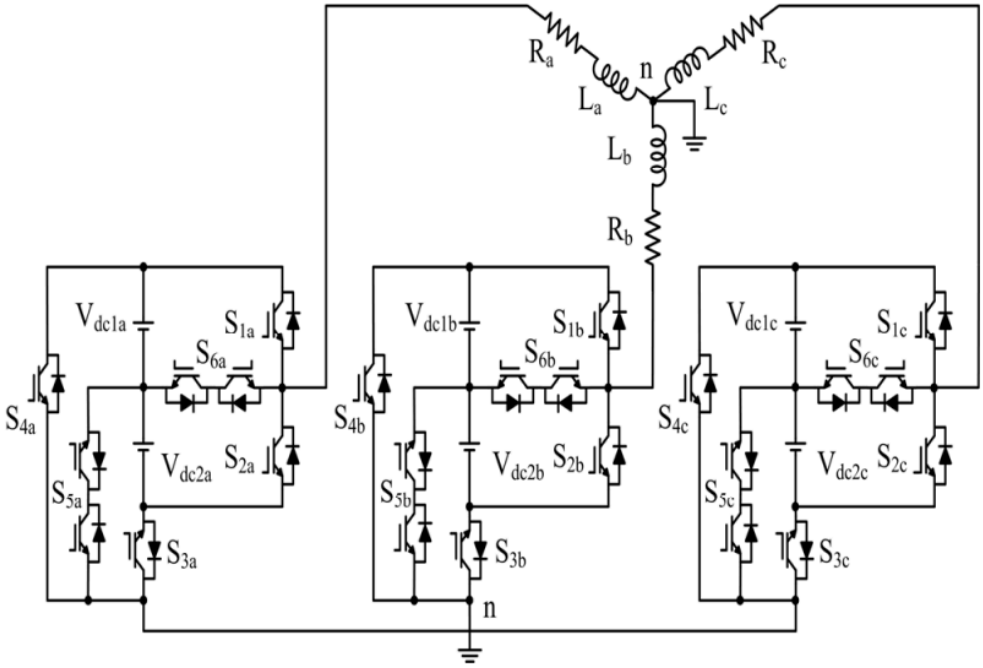
$$N_{driver} = 2N + 4 \quad (2.38)$$

Symmetric: $N_{level} = 2N + 1$ (2.39)

Asymmetric: $N_{level} = 2^{N+1} - 1$ (2.40)

Figure 2.24

Three-Phase Cascaded MLI (Krishnan et al. 2018)



The author in (Siwakoti 2018) describes an active 5-level NPC that has a minimum number of components. Three-phase designs need a decreased number of semiconductor switches. While all phases share two capacitors and a single dc voltage source, each phase is equipped with four power switches, one transistor, and one capacitor.

Figure 2.25

(a) 6 Levels Three-Phase NPC MLI (b)Phase A, Active NPC Inverter (Siwakoti 2018)

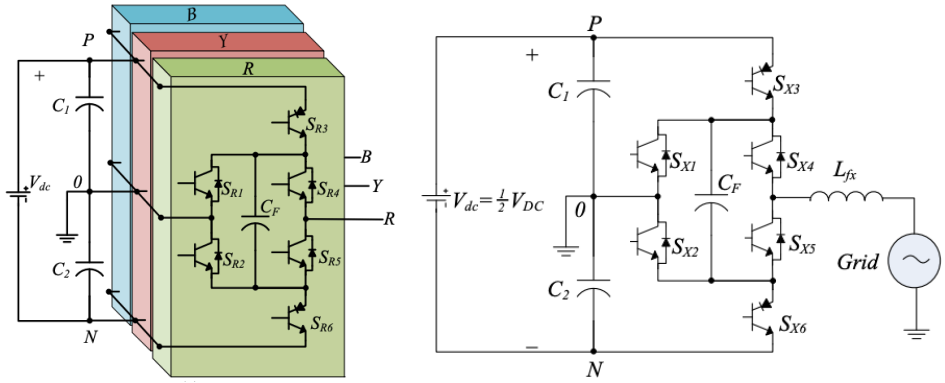


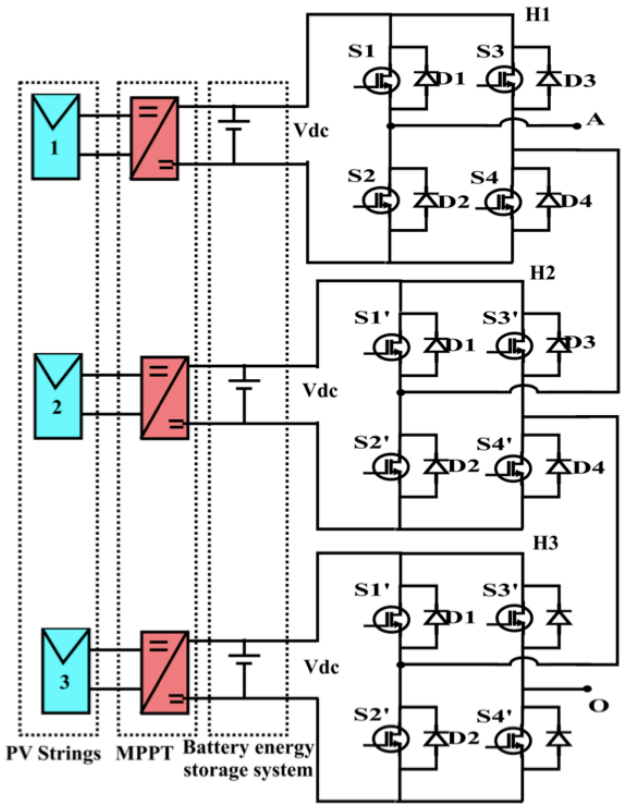
Figure 2.25(a) displays the three-phase structure. Single phase A, which has the same topology as seen in Figure 2.25(b). The exhibited enhanced NPC topology has the potential to benefit renewable energy systems.

DC Renewable Energy Sources Application Topologies

A block schematic of a multilevel inverter of solar energy is shown in Figure 2.26. It includes numerous PV strings, an MPPT charge controller, and batteries. Diode clamped and CHB MLI are the dominant categories of inverters used in solar applications (Peng et al.,1997), (Malinowski et al., 2010) and (Liu et al., 2008). There is a potential for energy imbalance between the sources when PV panels are partly veiled or when switching is used to produce multilevel voltages.

Figure 2.26

Block Diagram Circuit for PV (Rao et al., 2019)



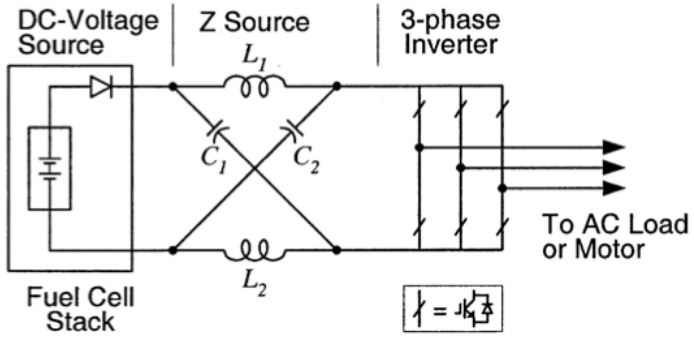
Xue et al. (2004) provided a detailed overview of the basic inverter configurations used in small-scale distributed power-generating systems. In small-scale distributed generation systems, the inverter is responsible for integrating power sources into the alternating current grid and supplying energy to ac customers. Two

main types of inverters are used for this purpose: isolated and non-isolated. These inverters should aim to decrease transient harmonic distortion in the process of dc to ac conversion.

The Z-source inverter is a unique inverter architecture, as mentioned by (Peng, 2003). A Z-source inverter, in contrast to traditional voltage- or current-source inverters, may provide both step-down (buck) and step-up (boost) outputs in relation to the input-output voltage level. Figure 2.27 portrays the Z-source inverter's circuit. Where the impedance comprised two inductors and capacitors, and its configuration mimics the shape of the letter Z.

Figure 2.27

Z Source Inverter (Peng 2003)



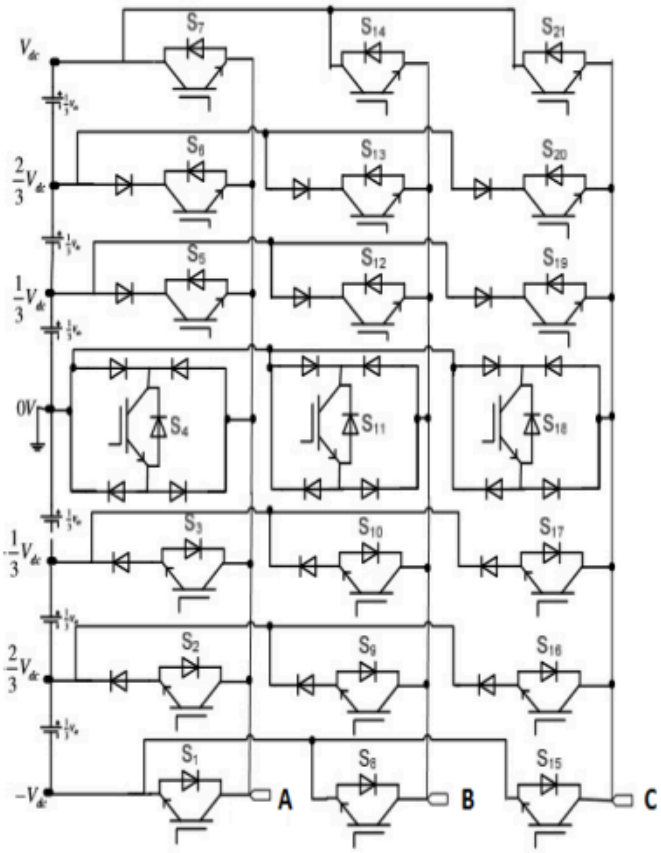
Farhangi et al. (2006) provided abundant data on the comparison between Z-source inverters and conventional inverters for PV systems. The fundamental advantage of impedance source inverters is their ability to both increase and reverse electrical power. Z-source inverters exhibited a decrease in efficiency when exposed to heavy loads, in contrast to conventional inverters, which were unaffected. Because the voltage from renewable sources like photovoltaics and fuel cells is naturally inconsistent, voltage source inverters need an extra surge stage at the beginning.

The problem of inconsistent and fluctuating power quality, and poor efficiency in renewable energy sources is generally acknowledged. In order to address this issue and guarantee the continuous delivery of energy at a high standard, it is necessary to use a multilevel inverter design. Seth et al. (2017) presented a paper, this proposed three-phase topology is crucial for MPPT for PV applications, shown in Figure 2.28.

Let's give the output number levels as N; for the whole three phases the topology requires switches of 3N, but for the diodes it is 3(N+1). The procedure for producing the upper and lower levels using a single IGBT while also integrating a bidirectional additional switch for the 0V level is explained in depth.

Figure 2.28

Three-Phase MLI Topology for Solar PV Application (Seth et al., 2017)



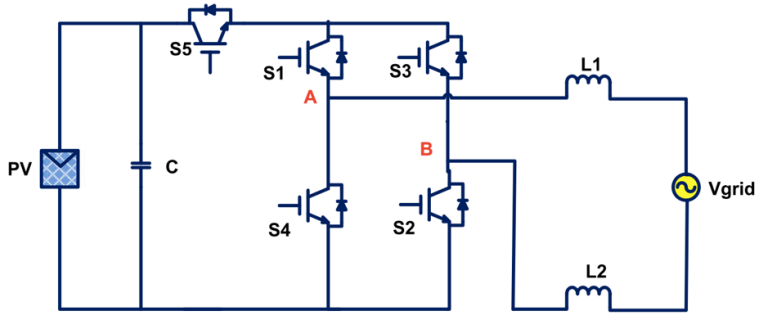
Leakage current is the dominant issue in transformer less topologies, mostly caused by the parasitic capacitance of photovoltaic systems. The parasitic capacitance must be reduced to decrease the common mode current. To prevent this flow of electric current, several circuit configurations are being used. Eliminating the leakage current may be achieved by maintaining a consistent common mode voltage. This is achieved by separating the PV and ac components of the inverter in its freewheeling phase. The leakage current in terms of the components is defined as:

$$v_{CM} = \frac{v_{AN}+v_{BN}}{2} + (v_{AN} - v_{BN})\frac{L_2-L_1}{2(L_1+L_2)} \tag{2.41}$$

An extra switch is added on the dc side to make it easier for the freewheeling path, and the leakage current is controlled by H5 inverters. According to the complete bridge inverter system, the top switch of the H5 single-phase inverter runs at the same frequency as the grid. Nevertheless, it demonstrates diminished effectiveness and significant switching losses. The H5 inverter is enhanced with the inclusion of two more switches, aiming to minimize switching losses and enhance overall efficiency. Figure 2.29 illustrates the H5 inverter used in a solar system.

Figure 2.29

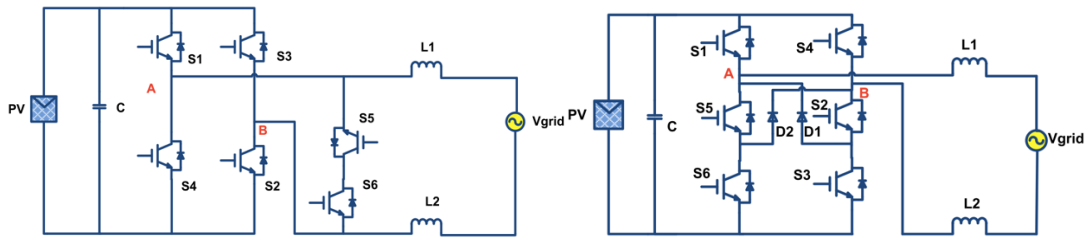
H5 Inverter for PV (Desai et al., 2024)



The High Efficient Reliable Inverter Concept (HERIC) is an enhanced design that utilizes two switches on the ac side to achieve a better isolation between the photovoltaic system and the grid. Figure 2.30(a) depicts the HERIC topology. The H6 inverter is another topological change that is used to reduce leakage current. It has been developed and studied in previous research. Figure 2.30(b), this inverter is characterized by a zero-state midpoint restricted structure. This arrangement allows for a certain level of reactive power control. Each of these arrangements signifies an increased quantity of switches, a higher density of passive components, and a more intricate driving circuit.

Figure 2.30

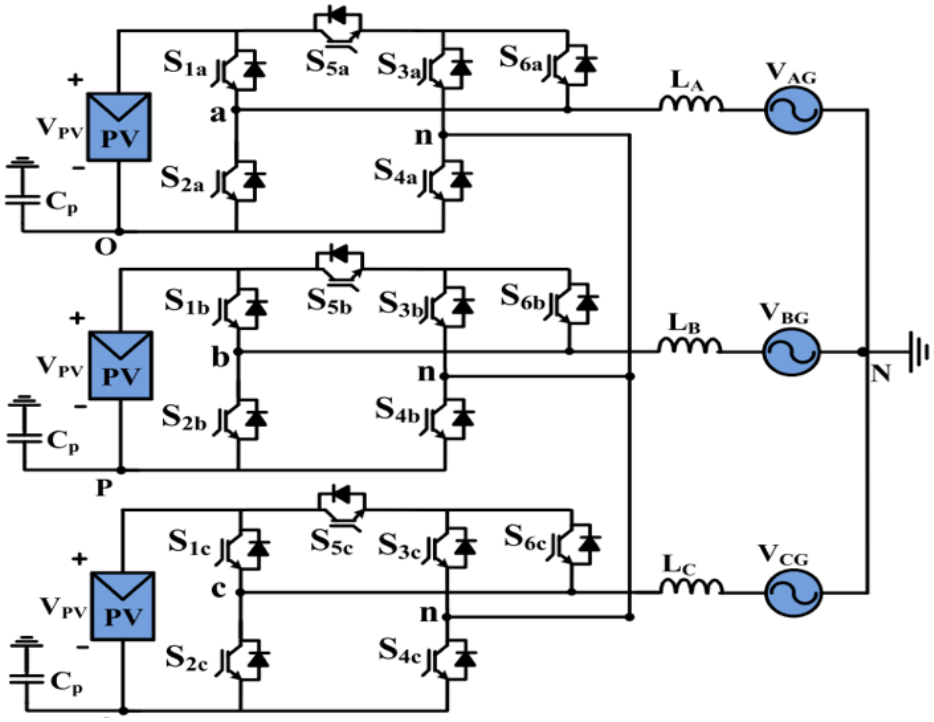
(a) HERIC Inverter for PV (b) H6 Inverter for PV (Desai et al., 2024)



Kumar et al. (2021) proposed a paper examining leakage current suppression for a three-phase CHB inverter, the outlined topology through a simulation and experimental setup was effective for the reduction of leakage current and reached the normal number of VDE 0126-01-01(<300 mA). The inverter supports PV grid-connected applications. The topology had two more switches in each phase than the conventional three phase design, illustrated in Figure 2.31.

Figure 2.31

PV Three-Phase CHB MLI (Kumar et al., 2021)



Control Techniques of MLI

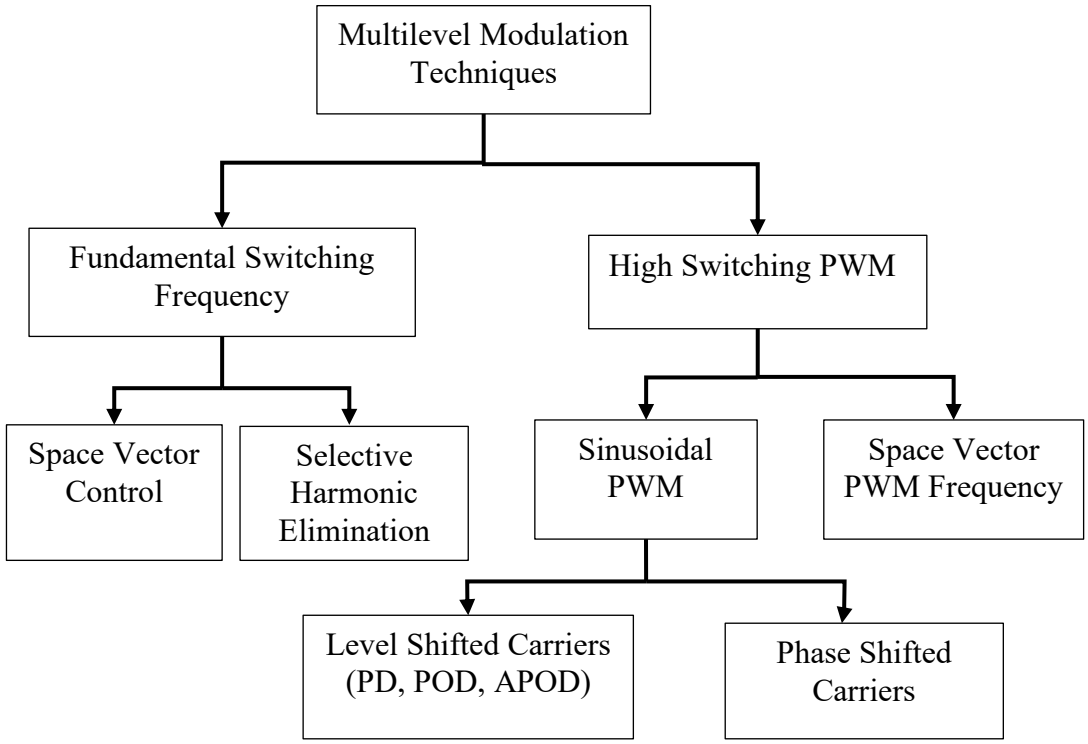
The Pulse Width Modulation approach may be easily applied to multilevel inverters with few adjustments, much as it is used in traditional inverters. The improved PWM approach is categorized into two groups: fundamental switching and high switching frequency, as seen in Figure 2.32. The staircase output voltage levels are achieved by using pulse width modulation in conjunction with the high switching frequency technique. Both switching algorithms result in a sequence of output levels arranged in a staircase pattern (Khomfoi & Tolbert, 2011).

In order to achieve the desired goal of operating an inverter with maximum efficiency, it is crucial to use a highly effective control technique. Researchers have proposed several control schemes, most of which are variations of the well-known PWM methodology. The PWM technique was first developed by Bhagwat and Stefanovic in 1983.

The choice of modulation techniques used for control in a multilevel inverter has a substantial influence on efficiency measures, including switching losses and harmonic reduction. The foundations of multilevel inverter control systems are based on basic principles and the use of high switching frequencies.

Figure 2.32

Classification of MLI Modulation Techniques



To support MLI topologies, conventional space vector PWM techniques may be readily adjusted by increasing the output voltage and the number of switching vectors. As the output levels grow, the redundancy of switches and the complexity of determining their states both increase exponentially.

Support vector machine SVM, is a very promising method in three-phase systems. However, the complexity of the system rises as the number of power

semiconductors grows. Choosing and designing suitable PWM modulation that aligns with the inverter's architecture is a crucial aspect of optimizing inverter control.

Selective Harmonic Elimination, SHE is a modulation technique used to remove certain unwanted harmonic components from the output signal (Kang et al., 2000).

Sinusoidal pulse width modulation, SPWM is the most often employed approach for controlling multilevel inverters. SPWM enables the controlled switching of power semiconductors in an inverter module by comparing a triangular carrier waveform with a sinusoidal reference waveform. Pulse width modulation using sinusoidal waves is a commonly used modulation method in two-level inverters. When used in multilevel inverters, sine PWM modulation methods may be categorized into two main branches (McGrath et al., 2002). There are two different types of multi-carrier methods:

i. level-shifted
ii. phase-shifted.

The PWM control technique has specific parameters (signal frequencies) that are related, and their equations can be derived as:

$$m_f = \frac{f_c}{f_o} \tag{2.42}$$

$$m_a = \frac{A_o}{A_{CPP}}\text{, for the phase-shifted method} \tag{2.43}$$

$$m_a = \frac{A_o}{4A_{CPP}}\text{, for level-shifted (carrier disposition method)} \tag{2.44}$$

Where: f_c = carrier signal frequency

f_o = reference signal frequency

m_a = amplitude modulation index

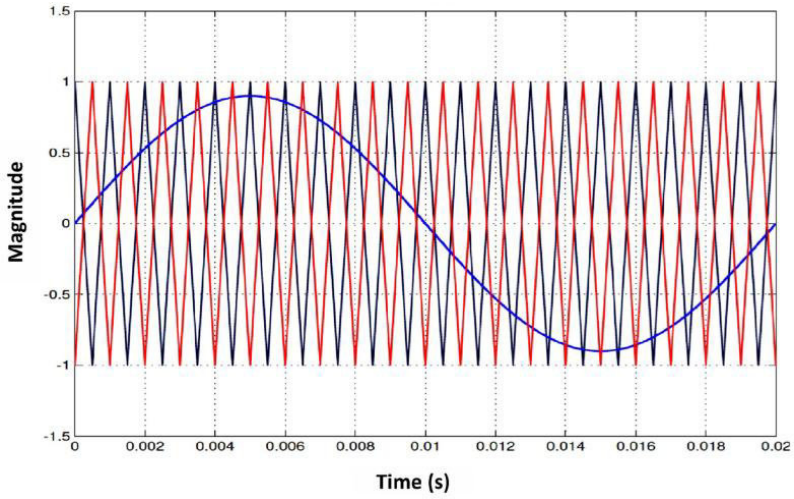
A_0 = amplitude of the reference signal

A_{CPP} = maximum value of the carrier signal

The phase-shifted carrier approach (Liang et al., 1998) will result in the spatial separation of the high-frequency carrier waves. This approach is often used in FC MLI and CHB MLI topologies. The carrier pulse generated is depicted in Figure 2.33.

Figure 2.33

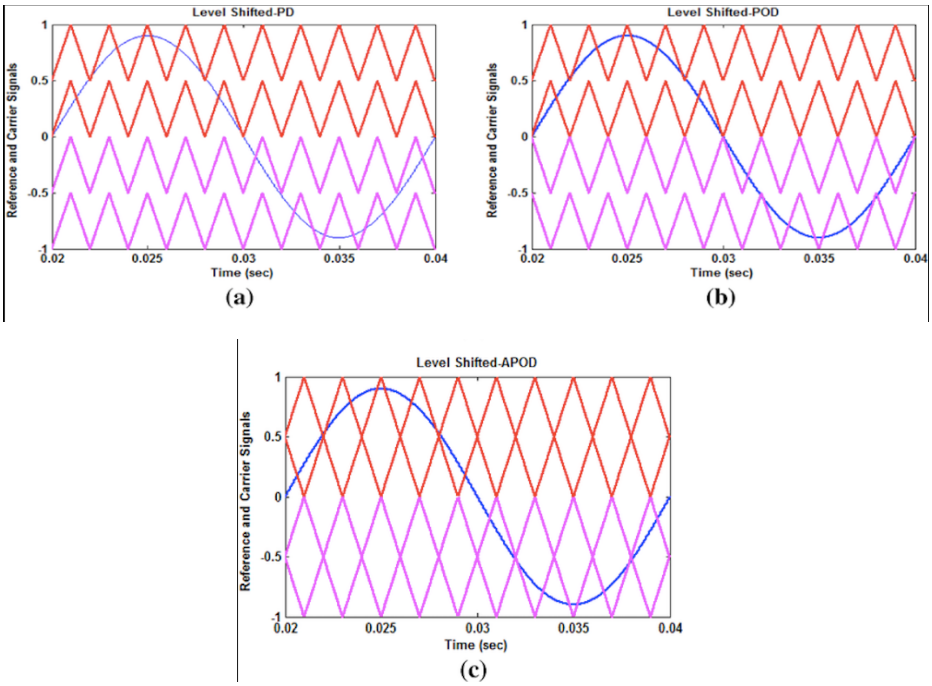
Phase Shifted Carrier (Mehta et al., 2015)



For the level shifted carriers, which are PD (Phase Disposition), APOD (Alternative Phase Opposite Disposition) and POD (Phase Opposite Disposition) are shown in Figure 2.34 their pulse waveforms differences.

Figure 2.34

(a) PD (b) POD (c) APOD (Arunachalam & Sedhuraman, 2020)



CHAPTER III

Proposed Topology and Simulation Results

Overview

This section focuses on the proposed inverter, which is symmetric and asymmetric DC source analysis of an improved single-phase H-bridge multilevel inverter. We will first discuss the classic basic H-bridge topology and how the presented topology is different from it. Comparison and investigation of the presented topology is conducted using symmetric and asymmetric magnitudes and the stepped voltage levels generated.

Contribution of the Work

The contribution the work has on the field of power electronics include:

- Less components count used: deploying fewer devices in the circuit design to reduce complexity.
- Better quality output waveforms: the elevated of the voltage steps results a good quality sinusoidal output voltage and load current waveforms.
- Cost benefit: the inverter uses fewer components which reduces the cost required for building it.
- Less power losses: the project utilizes fewer devices, switches. Therefore, the switching losses and the inverter is reduced, hence a better efficient system.

The mentioned contribution points above make the proposed inverter a good consideration option for renewable energy systems.

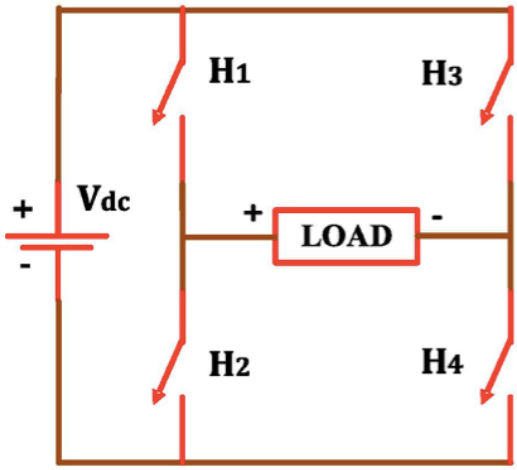
The novelty of the work is determining the asymmetric topology with fewer components give higher voltage levels, this gives simple circuit, costing less. Simulation is performed to analyze the quality of the output power. The presented inverter is designed to face the limitation challenges and could be integrated into DC renewable energy sources.

Conventional H-bridge MLI

Conventional H-bridge inverters are able to create both positive and negative levels. The conventional H-bridge inverter structure for single phase is shown in Figure 3.1. it is able to generate $+V_{dc}$, $-V_{dc}$ and 0 levels. If cascaded H-bridges are connected in series, each bridge produces 3 levels and they are added in total.

Figure 3.1

Conventional H-Bridge Inverter



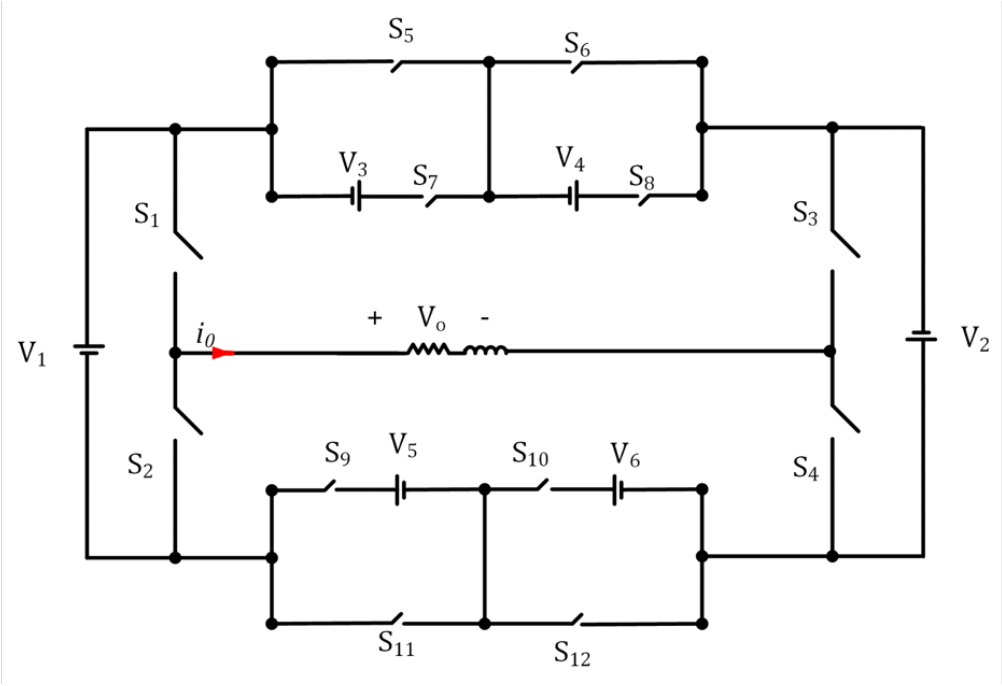
Proposed Single-Phase H-bridge MLI

The proposed inverter is an improved single-phase H-bridge MLI. Figure 3.2 illustrates the topology. It has these extra features; it has dc voltage on the right side, and there are H-bridge switches with voltage sources on each arm on the upper part and another one on the lower part of the structure. In total, the extra components compared to that of the 3-level conventional H-bridge inverter are 5 dc sources and 8 power switches. The load of the circuit is a resistance inductance (RL) load.

The presented topology produces an increased voltage step. We will calculate and compare the levels it generates using voltage sources with varying magnitudes, for example, symmetric and asymmetric structures. Bear in mind, the switching arrangement for the power switches. There's a situation to be evaded, an open circuit of the load, and a short circuit for the voltage. If it's not evaded there will be no output results, it will depend on the switches turned on.

Figure 3.2

Proposed Topology



The topology utilizes lower components to achieve stepped up voltage steps. The setup design of the circuit uses 12 power switches and 6 input dc sources. There are two dc sources on each side of the H-bridge. The two H-bridges on the top and bottom have 4 dc sources. To ensure the same positive and negative steps for the inverter, two sources will have an equal magnitude and same for the other two sources as well. of those 4 dc sources should get an equal magnitude. The link for the input sources connection is series to elevate the stepped output voltage. The topology leads to 30 positive and negative steps and 0V. In total 31 voltage steps if used asymmetric topology.

If we use the symmetric voltage sources, it will have lesser voltage levels with the same components. The symmetric topology will generate 9 voltage levels in total. The related equations for the topology for every case are as follows:

$$N_{Sources} = 6 \quad (3.1)$$

$$N_{Switches} = 12 \quad (3.2)$$

$$N_{Driver} = 12 \quad (3.3)$$

$$V_3 = V_5 \quad (3.4)$$

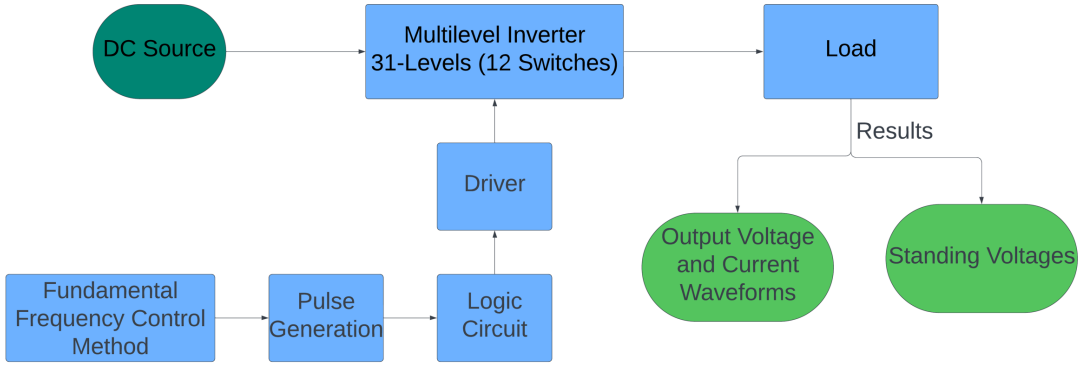
$$V_4 = V_6 \quad (3.5)$$

12 power switches are used in this topology to achieve higher output voltage levels, in asymmetric configuration it can generate 31 levels. If used less switches the desired output voltage will be hard to achieve. The 12 switches allow for easier, flexible control of the switching modes. The results of the voltage and current waveforms will have good quality and less distortions.

Generating 31 levels ensures a smoother sinusoidal output voltage waveform with less distortions. 31 levels balance the complex design and performance of the inverter with less components, power switches and higher voltage levels.

Figure 3.3

System Flow Diagram



The system flow diagram illustrated in Figure 3.3 details the sequence steps and tasks to be done, it illustrates choosing the DC sources at first, preferably solar energy, designing the inverter circuit with 12 switches, controlling the switching gating signals to generate desired output voltage levels and the load results. Symmetric and asymmetric analysis in regard to the load voltage steps.

Symmetric Topology

In symmetric setup the magnitudes of the input sources are same. In the presented topology for symmetric setup generates a 9 voltage steps. For deciding the sequence of generating the equal steps, in the topology the top H-bridge is neglected and inactive during the positive voltage steps, only the bottom will be activated. It is the opposite for the negative steps as well the bottom is inactive and top H-bridge is

activated. The equation below shows the relations of the sources' magnitudes and the highest voltage number:

$$V_1 = V_2 = V_3 = V_4 = V_5 = V_6 = V_{dc,input} \quad (3.6)$$

$$V_{output,max} = 4V_{dc,input} \quad (3.7)$$

For the sources V_3 and V_5, only one source can be used for switching states and same for V_4 and V_6. That is why the maximum output voltage is $4V_{dc,input}$. Table 3.1 details the switching modes for the symmetric setup.

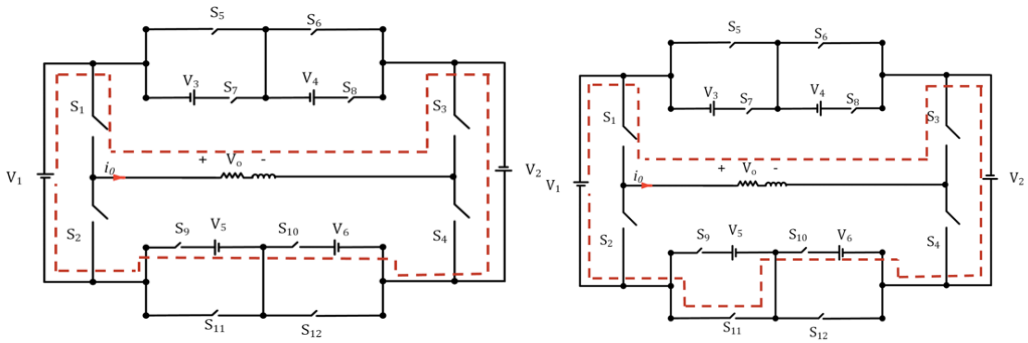
Table 3.1

Switching Modes for Symmetric Topology

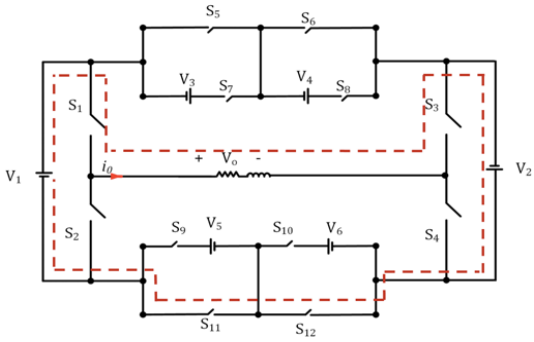
States	Turned ON Switches	V_{output}
1	SW_1, SW_3, SW_9, SW_{10}	$4V_{dc,input}$
2	SW_1, SW_3, SW_{10}, SW_{11}	$3V_{dc,input}$
3	SW_1, SW_3, SW_{11}, SW_{12}	$2V_{dc,input}$
4	SW_1, SW_4, SW_{11}, SW_{12}	$1V_{dc,input}$
5	SW_2, SW_4, SW_{11}, SW_{12}	0
	SW_1, SW_3, SW_5, SW_6	0
6	SW_2, SW_3, SW_5, SW_6	$-1V_{dc,input}$
7	SW_2, SW_4, SW_5, SW_6	$-2V_{dc,input}$
8	SW_2, SW_4, SW_5, SW_8	$-3V_{dc,input}$
9	SW_2, SW_4, SW_7, SW_8	$-4V_{dc,input}$

Figure 3.4

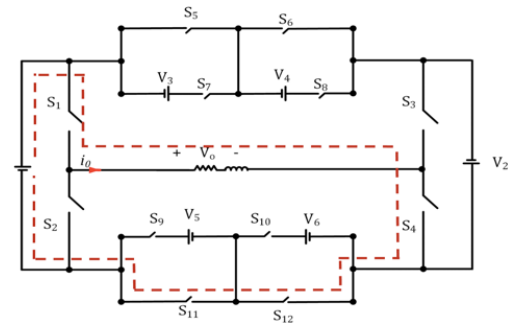
Switching States for Symmetric structure (A)4 $V_{dc,input}$ *(B)3* $V_{dc,input}$ *(C)2* $V_{dc,input}$ *(D)*$V_{dc,input}$ *(E)0 (E)0 (F)-*$V_{dc,input}$ *(G)-2* $V_{dc,input}$ *(H)-3* $V_{dc,input}$ *(I)-4* $V_{dc,input}$



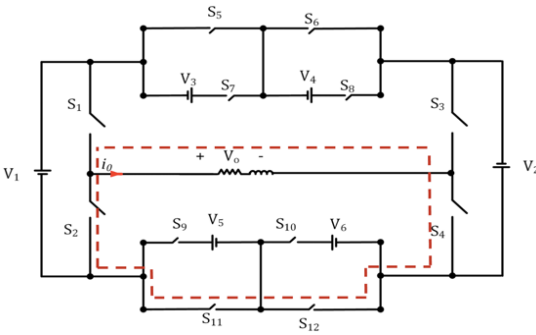
(A) $4V_{dc,input}$ (B) $3V_{dc,input}$



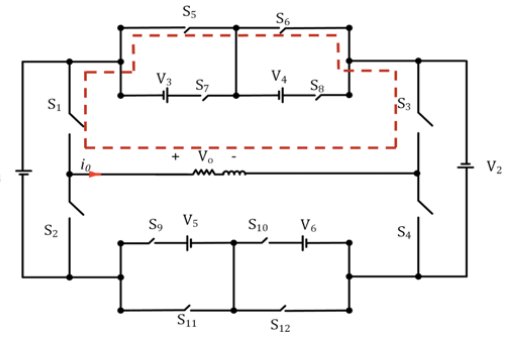
(C) $2V_{dc,input}$



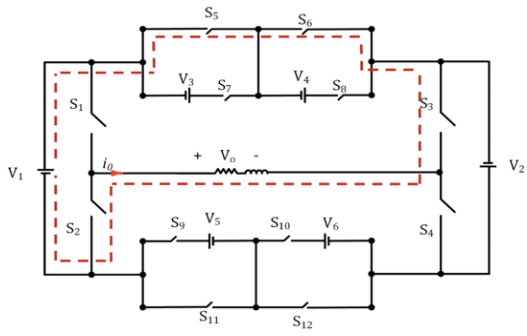
(D) $1V_{dc,input}$



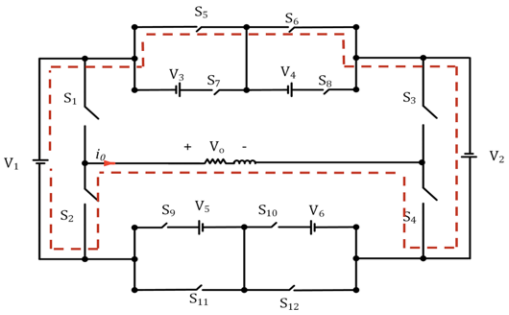
(E) 0V



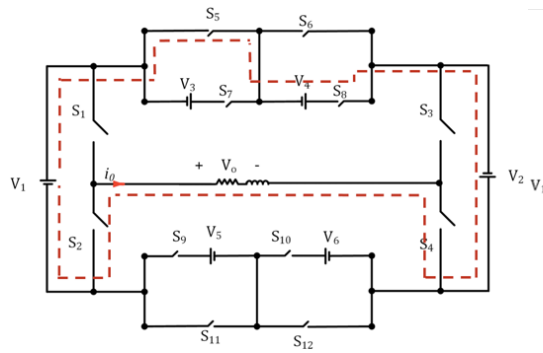
(E) 0V



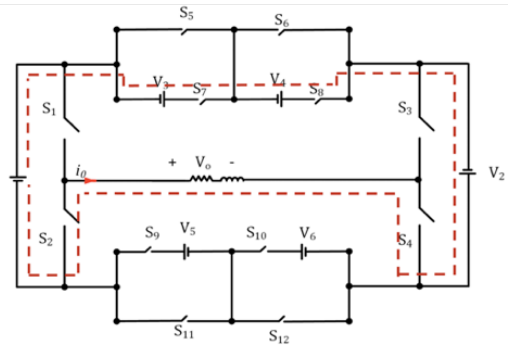
(F) $-V_{dc,input}$



(G) $-2V_{dc,input}$



(H) $-3V_{dc,input}$



(I) $-4V_{dc,input}$

Figure 3.4 illustrates the symmetric setup switching patterns. It displays the pattern for the switches to turn on for specific voltage step. The pattern about the symmetric setup is that there's a multiple patterns to make for one voltage level as the magnitudes of sources are all equal, such as $1V_{dc,input}$ as the output, switching any one

of sources is enough. However, there are certain switches that can be turned on simultaneously in order to evade the issue of open circuit and short circuit such as switch SW_1 and SW_2.

Proposed Asymmetric Topology

The proposed asymmetric topology uses varying voltage source magnitudes. It can generate a maximum of 31 voltage levels, utilizing the same range of steps for better output voltage waveform quality. The difference with the symmetric setup is that it delivered nine levels only. Table 3.2 gives the switching modes for the asymmetric setup. The parameters and relations for the levels generated, magnitudes for the sources and the peak output voltage are given as:

$$V_1 = 1V_{dc,input} \tag{3.8}$$

$$V_2 = 2V_1 \tag{3.9}$$

$$V_3 = 4V_1 \tag{3.10}$$

$$V_5 = 4V_1 \tag{3.11}$$

$$V_4 = 8V_1 \tag{3.12}$$

$$V_6 = 8V_1 \tag{3.13}$$

$$V_{ouput,max} = 15V_{dc,input} \tag{3.14}$$

$$N = 31 \text{ Levels} \tag{3.15}$$

Figure 3.5 illustrates the switching modes of the presented topology. The total levels are 31 of both positive and negative included. For the 0V step there is two switching patterns that generates it. First pattern the switches SW_1, SW_3, SW_5, SW_6 are gated on, and for the second pattern it is the switches SW_2, SW_4, SW_{11}, SW_{12}, but they are activated one at a time. Figure 3.5 details the paths of switches turned on for each level; for the positive steps the pattern follows through the lower H-bridge unit while the top H-bridge is neglected. From the table, to generate positive 14 voltage level, the switches pattern activated are SW_2, SW_3, SW_9, $SW_{10,}$ and for the negative 12 voltage level, the switches are SW_1, SW_3, SW_7, SW_8. When one pattern is occurring, the remaining switches are in blocking mode. The stepped voltage level relies on the sources gated on. Controlling the switching patterns is necessary.

The comparison of the symmetric and asymmetric switching states shown in Table 3.1 and Table 3.2 illustrates the asymmetric analysis has many states and different combinations of the switches turned on in order to increase the voltage level.

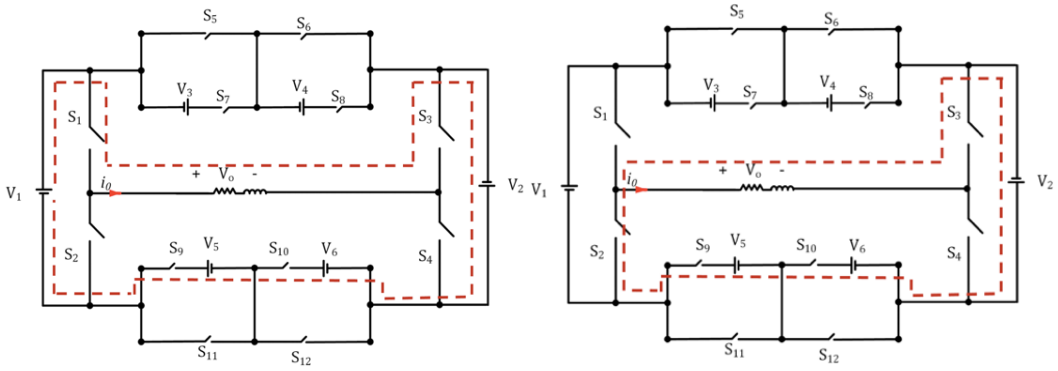
Table 3.2

Switching Pattern for Asymmetric Proposed Topology

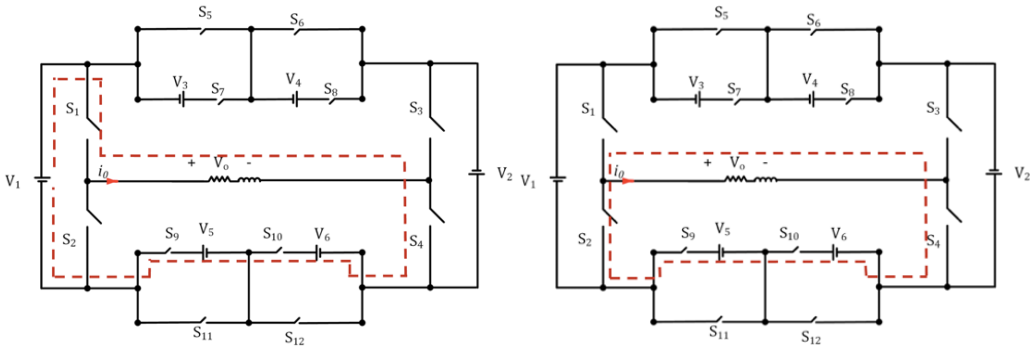
Modes	SW Activated	Input Sources	V_{output}
I	SW_1, SW_3, SW_9, SW_{10}	$V_1+V_2+V_5+V_6$	$15V_{(dc,input)}$
II	SW_2, SW_3, SW_9, SW_{10}	$V_2+V_5+V_6$	14 $V_{(dc,input)}$
III	SW_1, SW_4, SW_9, SW_{10}	$V_1+V_5+V_6$	13 $V_{(dc,input)}$
IV	SW_2, SW_4, SW_9, SW_{10}	V_5+V_6	12 $V_{(dc,input)}$
V	SW_1, SW_3, SW_{10}, SW_{11}	$V_1+V_2+V_6$	11 $V_{(dc,input)}$
VI	SW_2, SW_3, SW_{10}, SW_{11}	V_2+V_6	10 $V_{(dc,input)}$
VII	SW_1, SW_4, SW_{10}, SW_{11}	V_1+V_6	9 $V_{(dc,input)}$
VIII	SW_2, SW_4, SW_{10}, SW_{11}	V_6	8 $V_{(dc,input)}$
IX	SW_1, SW_3, SW_9, SW_{12}	$V_1+V_2+V_5$	7 $V_{(dc,input)}$
X	SW_2, SW_3, SW_9, SW_{12}	V_2+V_5	6 $V_{(dc,input)}$
XI	SW_1, SW_4, SW_9, SW_{12}	V_1+V_5	5 $V_{(dc,input)}$
XII	SW_2, SW_4, SW_9, SW_{12}	V_5	4 $V_{(dc,input)}$
XIII	SW_1, SW_3, SW_{11}, SW_{12}	V_1+V_2	3 $V_{(dc,input)}$
XIV	SW_2, SW_3, SW_{11}, SW_{12}	V_2	2 $V_{(dc,input)}$
XV	SW_1, SW_4, SW_{11}, SW_{12}	V_1	1 $V_{(dc,input)}$
XVI	SW_2, SW_4, SW_{11}, SW_{12}	-	0
	SW_1, SW_3, SW_5, SW_6	-	0
XVII	SW_2, SW_3, SW_5, SW_6	$-V_1$	-1 $V_{(dc,input)}$
XVIII	SW_1, SW_4, SW_5, SW_6	$-V_2$	-2 $V_{(dc,input)}$
XIX	SW_2, SW_4, SW_5, SW_6	$-(V_1+V_2)$	-3 $V_{(dc,input)}$
XX	SW_1, SW_3, SW_6, SW_7	$-V_3$	-4 $V_{(dc,input)}$
XXI	SW_2, SW_3, SW_6, SW_7	$-(V_1+V_3)$	-5 $V_{(dc,input)}$
XXII	SW_1, SW_4, SW_6, SW_7	$-(V_2+V_3)$	-6 $V_{(dc,input)}$
XXIII	SW_2, SW_4, SW_6, SW_7	$-(V_1+V_2+V_3)$	-7 $V_{(dc,input)}$
XXIV	SW_1, SW_3, SW_5, SW_8	$-V_4$	-8 $V_{(dc,input)}$
XXV	SW_2, SW_3, SW_5, SW_8	$-(V_1+V_4)$	-9 $V_{(dc,input)}$
XXVI	SW_1, SW_4, SW_5, SW_8	$-(V_2+V_4)$	-10 $V_{(dc,input)}$
XXVII	SW_2, SW_4, SW_5, SW_8	$-(V_1+V_2+V_4)$	-11 $V_{(dc,input)}$
XXVIII	SW_1, SW_3, SW_7, SW_8	$-(V_3+V_4)$	-12 $V_{(dc,input)}$
XXIX	SW_2, SW_3, SW_7, SW_8	$-(V_1+V_3+V_4)$	-13 $V_{(dc,input)}$
XXX	SW_1, SW_4, SW_7, SW_8	$-(V_2+V_3+V_4)$	-14 $V_{(dc,input)}$
XXXI	SW_2, SW_4, SW_7, SW_8	$-(V_1+V_2+V_3+V_4)$	-15 $V_{(dc,input)}$

Figure 3.5

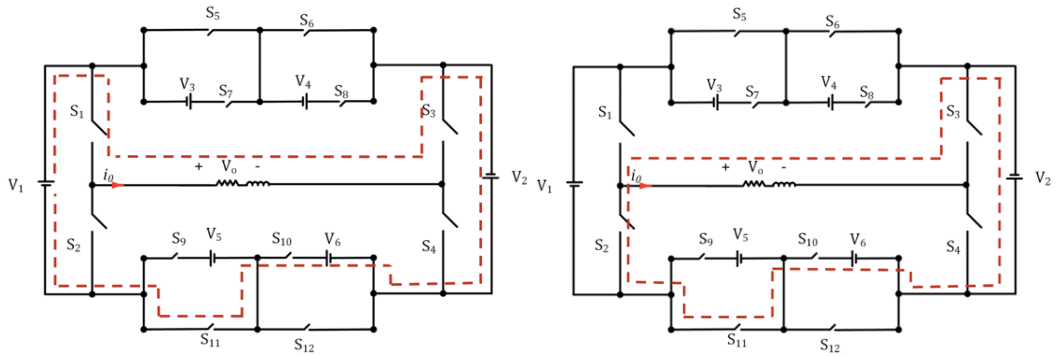
Switching States for Asymmetric Proposed Topology



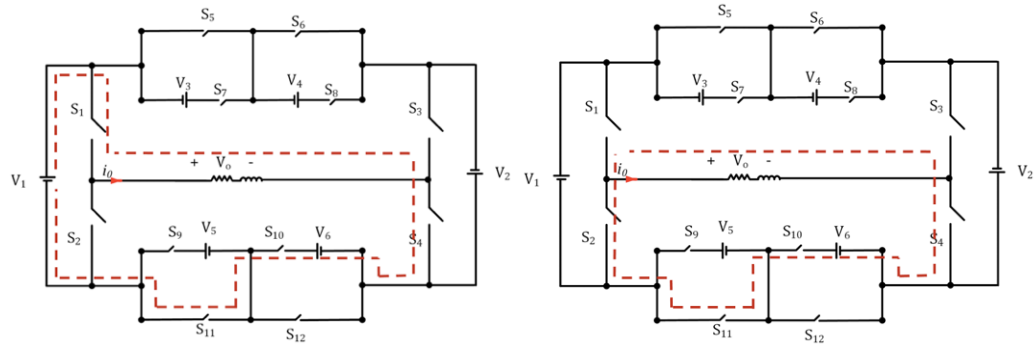
(i) $15V_{dc}$ (ii) $14V_{dc}$



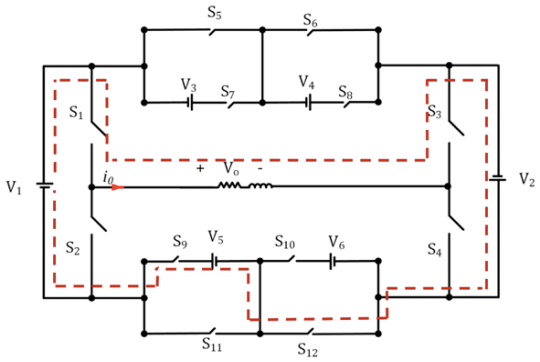
(iii) $13V_{dc}$ (iv) $12V_{dc}$



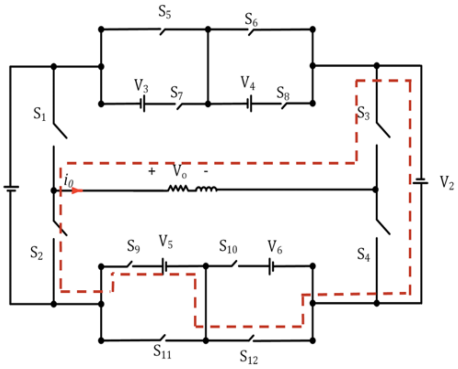
(v) $11V_{dc}$ (vi) $10V_{dc}$



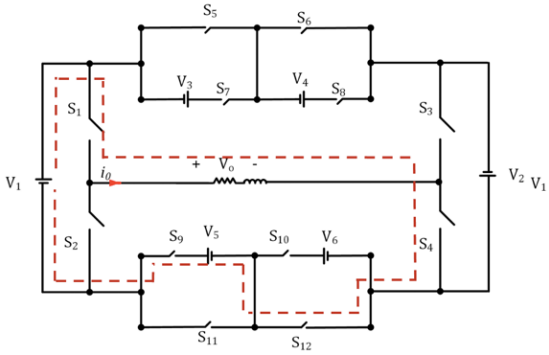
(vii) $9V_{dc}$ (viii) $8V_{dc}$



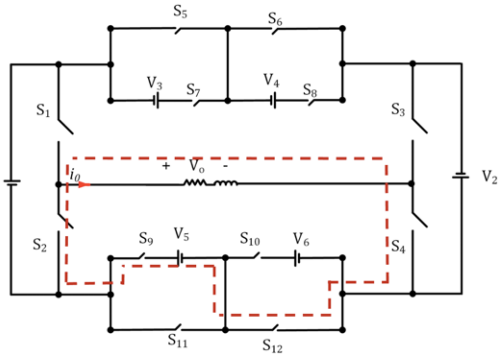
(ix) $7V_{dc}$



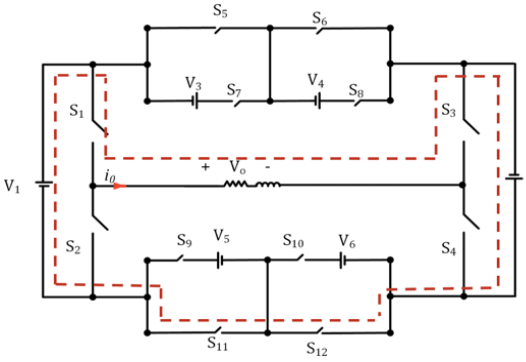
(x) $6V_{dc}$



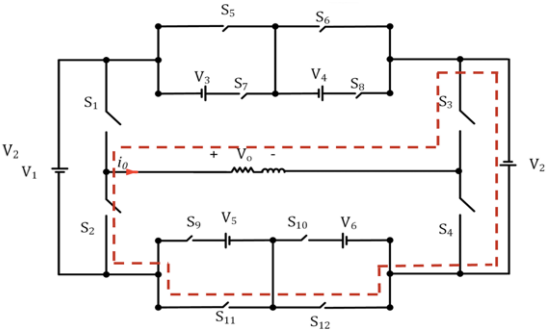
(xi) $5V_{dc}$



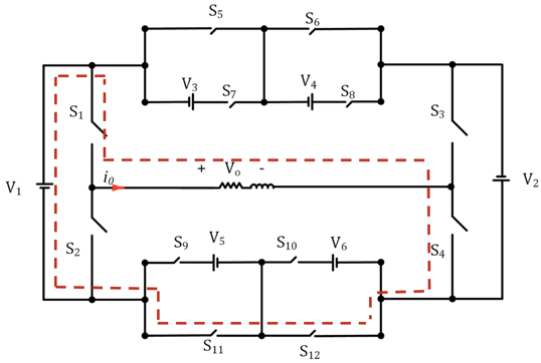
(xii) $4V_{dc}$



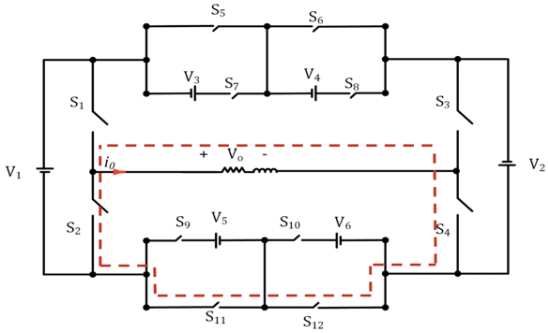
(xiii) $3V_{dc}$



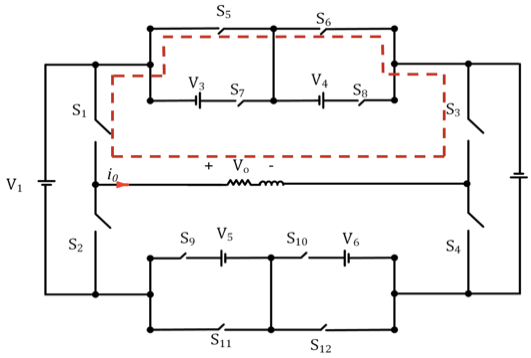
(xiv) $2V_{dc}$



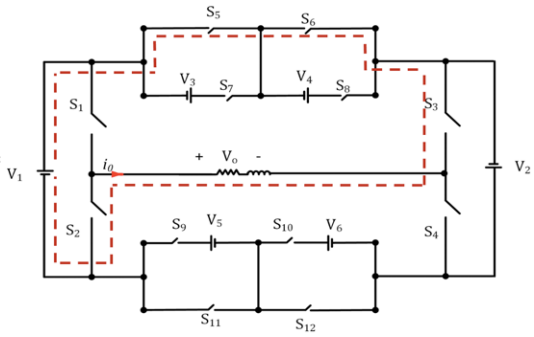
(xv) V_{dc}



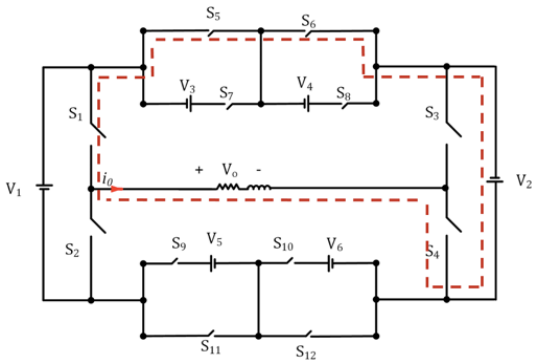
(xvi) 0



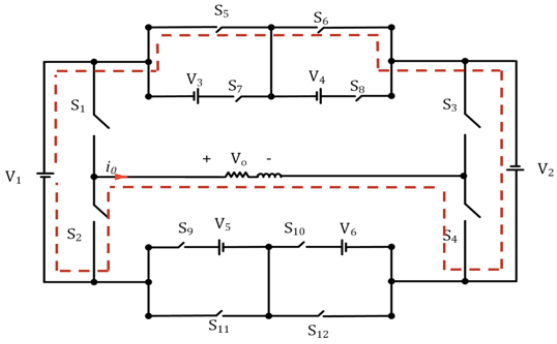
(xvi) 0



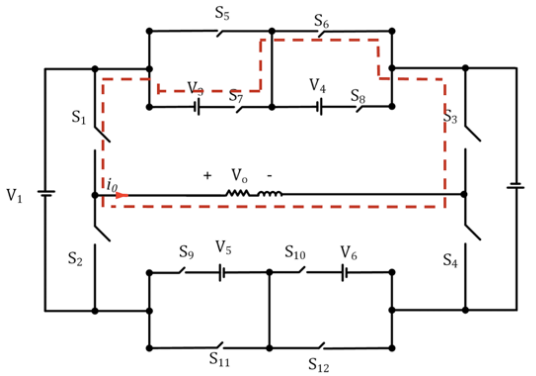
(xvii) $-V_{dc}$



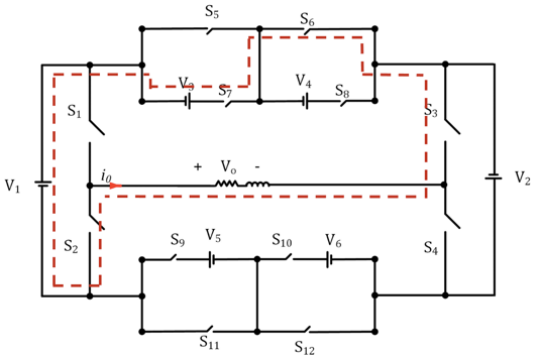
(xviii) $-2V_{dc}$



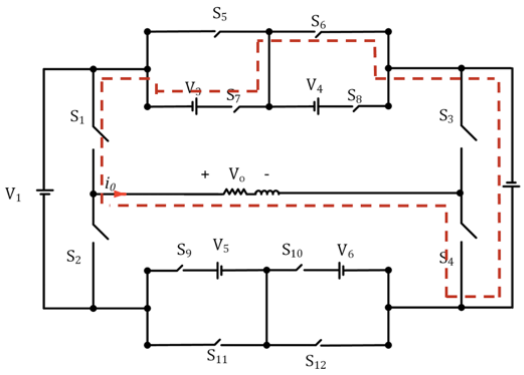
(xix) $-3V_{dc}$



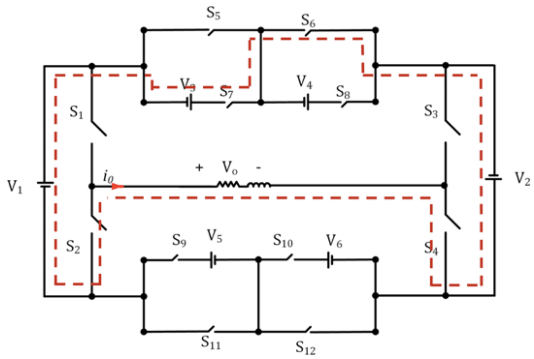
(xx) $-4V_{dc}$



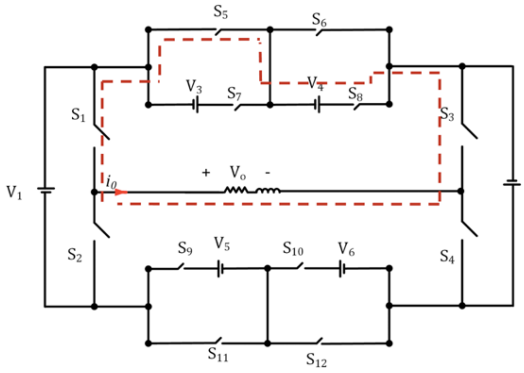
(xxi) $-5V_{dc}$



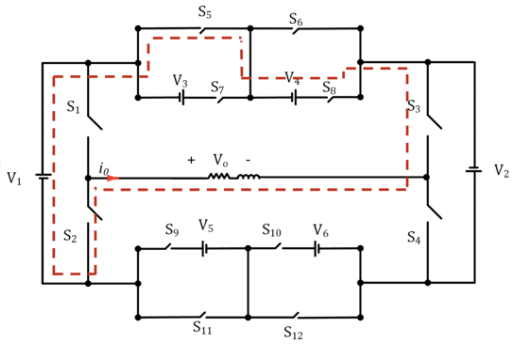
(xxii) $-6V_{dc}$



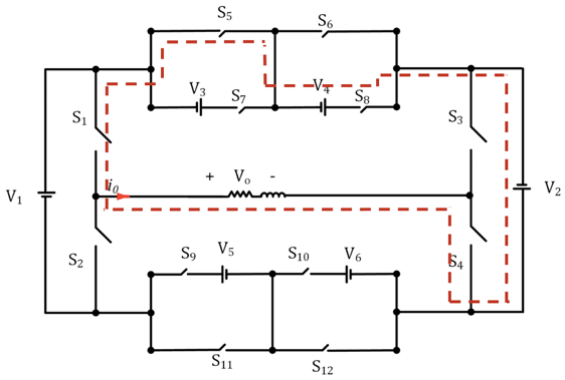
(xxiii) $-7V_{dc}$



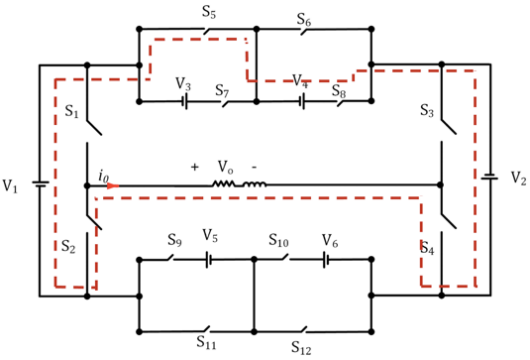
(xxiv) -8V_{dc}



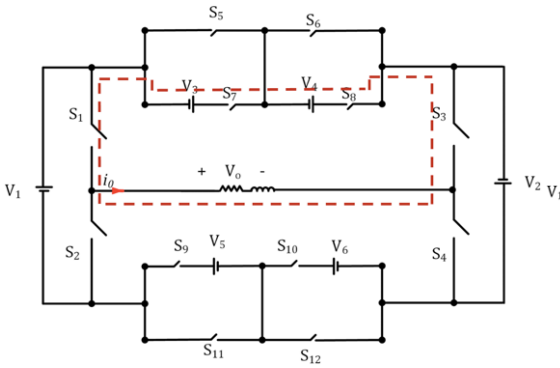
(xxv) -9V_{dc}



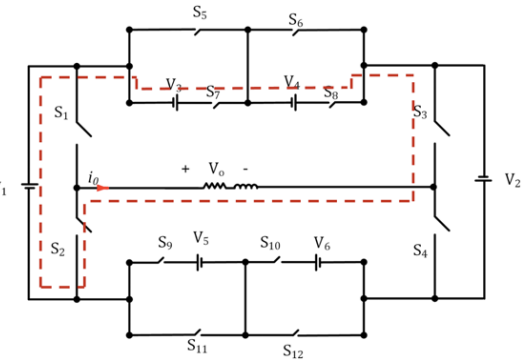
(xxvi) -10V_{dc}



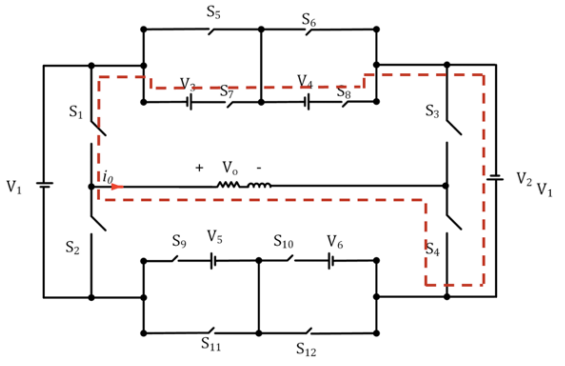
(xxvii) -11V_{dc}



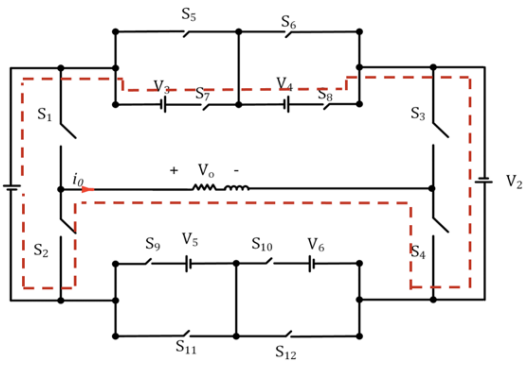
(xxviii) -12V_{dc}



(xxix) -13V_{dc}



(xxx) -14V_{dc}



(xxxi) -15V_{dc}

Figure 3.5 shows the path for the circuit to be activated to control the voltage level generated. The red line dots demonstrate the close circuit of the load for the specific voltage level. For example in Figure 3.5 (xii), to generate positive level of four steps, 4 $V_{dc,input}$, the red line close path follows through the switches SW_2, SW_4, SW_9 and SW_{11}, this allows V_5 source to be activated. for the case of generating -11V_{dc}, it must be used the sources of V_1, V_2, V_4. The switches must be turned on for the close circuit are switches SW_2, SW_4, SW_5 and SW_8.

PSCAD Software

Power systems computer-aided design (PSCAD) is a simulation software mostly used for power systems, it is user friendly for circuits modelling, designing and simulations, visualization for power electronics components and control methods. It handles complex systems like electromagnetic transient.

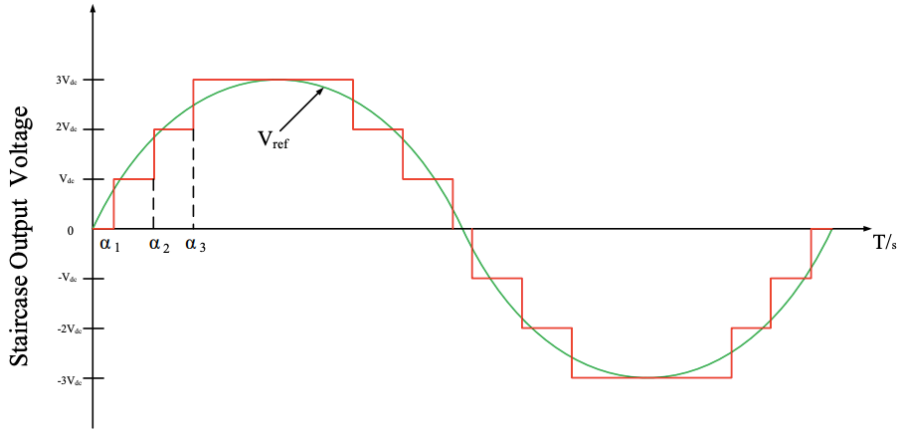
The purpose for the software in this project, PSCAD is mostly used for designing multilevel inverter with more effective and accuracy. The data type used is assigning real numbers to the dc sources, selecting components, logic control; Booleans and measurement tools, which are easier, and it allows custom changes. It allows a thorough analysis on the switching approach for the inverter. The visualization graphs and reports allow the analysis of the inverter's performance, switching losses. The graphs are clearer for the output results.

Fundamental Frequency Control Method (FFCM)

Switching control for the inverter is very crucial, the method used in this project is the FFCM, known as also nearest level control, it has some benefits including lower switching losses, more phases control is simple and shifts a 120-degree angle in contrast to other control techniques, for example, nearest vector control. The way it selects its number is by using the reference signal and the stepped output voltage and choose the closest level number. The stepped voltage levels used for normalizing the reference signal and multiplying the nearest number with the varying magnitudes of the source results to the stepped voltage the inverter delivers. The switching control method is carried out in PSCAD software and the simulation results.

Figure 3.6

Fundamental Frequency Control Method



Standing Voltage

The standing voltage of an inverter is defined as the voltage the switches can handle when they not turned on and is able to block it. This means the switch turned on does not have standing voltage in that instance. In every switching period the blocking voltage of a switch changes, but the maximum of the voltage levels is the standing voltage of that specific switch. Switches who have higher numbers of standing voltage cost more, therefore, it is vital to select a one with less ratings which means when modeling the inverter, you have to account the magnitude of the sources that are used in the system. The presented topology has 12 switches, the relations of the switches' standing voltage to the input sources is given as:

$$V_{SW1} = V_1 = V_{dc,input} \quad (3.16)$$

$$V_{SW2} = V_1 = V_{dc,input} \quad (3.17)$$

$$V_{SW3} = V_2 = 2\,V_{dc,input} \quad (3.18)$$

$$V_{SW4} = V_2 = 2\,V_{dc,input} \quad (3.19)$$

$$V_{SW5} = V_3 = 4\,V_{dc,input} \quad (3.20)$$

$$V_{SW6} = V_4 = 8\,V_{dc,input} \quad (3.21)$$

$$V_{SW7} = V_3 = 4\,V_{dc,input} \quad (3.22)$$

$$V_{SW8} = V_4 = 8\,V_{dc,input} \quad (3.23)$$

$$V_{SW9} = V_3 = 4\,V_{dc,input} \quad (3.24)$$

$$V_{SW10} = V_4 = 8\,V_{dc,input} \quad (3.25)$$

$$V_{SW11} = V_3 = 4\,V_{dc,input} \quad (3.26)$$

$$V_{SW12} = V_4 = 8\,V_{dc,input} \quad (3.27)$$

The standing voltage for the whole inverter system is given as:

$$V = 54\ V_{dc,input} \tag{3.28}$$

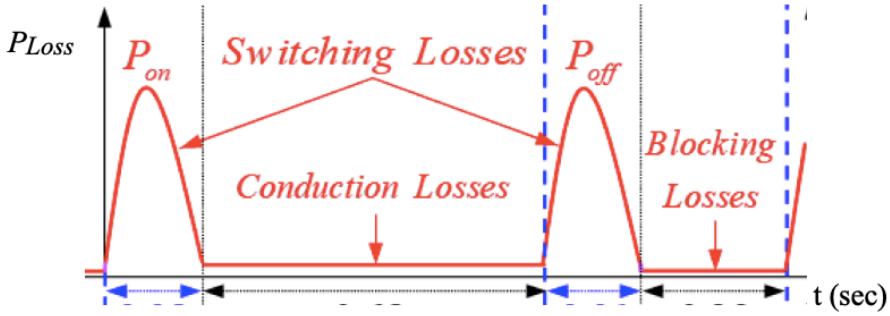
Inverter Power Losses

This section discusses the losses that occur in the switches of the system. The losses are classified into three parts known as: Switching losses, blocking losses and conduction losses. Furthermore, losses by the switches does occur both in its on and off period. The addition of three losses results to the total losses for the inverter system.

The Figure 3.7 illustrates the losses of the switches in a whole one period, both on and off state, as can be seen by the graph the switching losses is during on and off period, while conduction losses is during on state only, and the blocking losses during off state. Usually, the blocking losses is not included during the calculation as the value is too small compared to others, as its current is nearly zero therefore power loss is far less.

Figure 3.7

Inverter Power Losses



Switching Losses

Switching losses occur both states and it's a time dependent. The equation for both states and the total switching losses is given as:

$$E_{on} = \int_0^{t_{on}} v(t)\, i(t)\, dt = \int_0^{t_{on}} \left[\left(\frac{I'}{t_{on}} t\right)\left(-\frac{V_{sw}}{t_{on}}(t - t_{on})\right)\right] dt = \frac{1}{6} V_{sw}\, I'\, t_{on} \tag{3.29}$$

$$E_{off} = \int_0^{t_{off}} v(t)\, i(t)\, dt = \int_0^{t_{off}} \left[\left(\frac{V_{sw}}{t_{off}} t\right)\left(-\frac{I}{t_{off}}(t - t_{off})\right)\right] dt = \frac{1}{6} V_{sw}\, I\, t_{off} \tag{3.30}$$

$$P_{SW} = f_s \sum_{k=1}^{N_{switch}} \left[\sum_{i-1}^{N_{on}} E_{on} + \sum_{i=1}^{N_{off}} E_{off}\right] \tag{3.31}$$

Where:

E_{on} = On state

E_{off} = Off state

T_{on} = On period time

T_{off} = Off period time

P_{SW} = Total switching losses

I = Current during on state

I' = Current during off state

V_{SW} = Voltage of the switch in off-state

Conduction Losses

These losses depend on the elements of the switches used in the system, we have 12 switches, 4 that are bidirectional. The switches have IGBTs and diodes. Therefore, the losses of the diodes and transistors give the total power losses for the conduction. The formula is given as:

$$P_{C,T}(t) = \left(V_T + R_T i^{\beta}(t)\right) i(t) \quad (3.32)$$

$$P_{C,T} = \frac{1}{2\pi}\int_0^{2\pi} n_T(t) \left[\left(V_T + R_T i^{\beta}(t)\right) i(t)\right] d(\omega t) \quad (3.33)$$

$$P_{C,D}(t) = \left(V_D + R_D i(t)\right) i(t) \quad (3.34)$$

$$P_{C,D} = \frac{1}{2\pi}\int_0^{2\pi} n_D(t) \left[\left(V_T + R_D i(t)\right) i(t)\right] d(\omega t) \quad (3.35)$$

$$P_C = P_{C,T} + P_{C,D} \quad (3.36)$$

Where:

$P_{C,T}$ = Power loss for the transistor

$P_{C,D}$ = Power loss for the diode

V_T, R_T = The voltage and resistive component of the transistor

V_D, R_D = The voltage and resistive component of the diode

For the whole inverter system, the total power losses, and the efficiency are given as:

$$P_{Losses} = P_C + P_{SW} \quad (3.37)$$

$$\eta = \frac{P_{out}}{P_{input}} \quad (3.38)$$

Comparison Analysis

This part we will compare the presented inverter to published topologies. The topologies all have 31 stepped voltage levels. Table 3.3 details the comparison done in terms of the common components used in designing the inverters. The components of the proposed topology is 50. The main focus being the IGBTs in the switches and

the driver circuit used. The presented topology used 4 bidirectional switches, therefore, it has more IGBTs and diodes than the driver, as common emitter driver is used. 12 drivers are utilized, 16 IGBTs and 16 diodes as well. The conventional MLI have the highest counts with clamping diodes and capacitors used.

The input source counts, the proposed topology used second highest number among the other published topologies, only [1] has higher, but the switches and diodes of the proposed are fewer. Inverter [4] has the fewest total components, with 12 switches and 3 sources, however the proposed topology is among the inverters with least number of components in the circuit, the third least. This makes the proposed topology worth a viable consideration.

Table 3.3

Comparison Topologies Study

Topologies	Voltage Level	DC Source	Switches IGBT	No. Driver	Diode	Clamped Diode	Capacitor	Clamped Capacitor	Total Component
Proposed	31	6	16	12	16	0	0	0	50
[1]	31	15	18	18	32	0	0	0	83
[2]	31	2	16	16	18	0	4	0	56
[3]	31	2	18	18	20	0	4	0	62
[4]	31	3	12	10	12	0	4	0	38
[5]	31	4	16	16	16	0	0	0	52
[6]	31	4	12	12	12	0	0	0	40
CHB	31	15	60	60	60	0	0	0	195
FC	31	1	60	60	60	0	30	435	646
NPC	31	1	60	60	60	870	0	30	1081

NOTE: references from Table 3.3

[1] = (Kubendran et al., 2024), [2] = (Roy et al., 2019), [3] = (Ahmad et al., 2020), [4] = (Hussan et al., 2020), [5] = (Chinthamalla, 2017), [6] = (Tackie et al., 2023).

If higher voltage levels are to be generated with less devices, using asymmetric topology is the best to achieve it. However, it comes with challenges, a more sophisticated switching control technique is needed for effectiveness.

For the DC sources if used higher voltage magnitudes, will deliver efficient power to the users, and the need for step-up transformer is reduced. However, the high input voltage levels will have limitation, higher stress to the components in the system, the standing voltages of the switches will be rated higher to handle it.

Results of the Simulation

The simulation is conducted through PSCAD, the presented topology has a resistance inductance (RL) load. The components; 12 switches, four bidirectional ones, and 6 input sources.

The simulation parameters used for the circuit is illustrated in Table 3.4. it is selected a switching frequency of 50kHz, a higher frequency which equates to good output waveforms but also leads to more losses, the aim is to balance it as our objective a better power quality. The load has standard frequency of 50Hz for ac loads.

A modulation index of 1 is selected, the modulation index has effects on the results, as it determines the peak of the voltage in comparison with the reference signal, affects the harmonic distortion. Higher modulation means higher output voltage. It is selected as ‘1’, more than that will cause overmodulation and distortions in output waveforms. The resistive inductive load parameters are 50Ω for the resistance and 0.05H for the inductance.

The DC sources voltage is chosen with an incremented voltage step of 22V. It is chosen as 22V since the inverter generates 15 positive voltage level. therefore, the product voltage of 15 level with 22V steps results to 330V which is the peak voltage beneficial for renewable energy applications, that require higher voltage and longer distance transmission. It’s easier to be integrated into existing infrastructure.

Table 3.4

Simulation Configurations

Variables	Magnitude
Output Frequency	50Hz
Output Resistance	50Ω
Modulation Index	1
Output Inductance	0.05H
Switching Frequency	50kHz
Input DC Sources	V_1=22V, V_2=44V, V_3=88V, V_4=176V, V_5=88V, V_6=176V

The system's simulation gave an inverter with 31 stepped voltage levels with each level rising 22V step, as illustrated in Figure 3.8 it displays the voltage steps along with the reference waveform, they are close and aligning with each other. Amplitude voltage of 330V is achieved. The waveforms are good quality sine wave with less distortions. The load current is given in figure 3.9, it's waveform a peak 6.35A current.

The standing voltage for the switches is depicted in Figure 3.10 every switch has its own graph result to show the blocking voltage of the simulation and it validates the theory principle. It shows the switches have a maximum blocking voltage of the one we calculated. Switch SW_1 has 22V standing voltage same for SW_2. SW_3 and SW_4 has 44V standing voltage

Among the switches, there are four bidirectional switches: SW_5, SW_6, SW_{11} and SW_{12}. From Figure 3.10 it can be seen they have a graph for both positive and negative values for the voltage axis which suggests it blocks the voltage both polarities. SW_{11} and SW_5 have 88V standing voltage, and for the other two switches SW_{12} and SW_6 has 176V.

Figure 3.8

Stepped Output Voltage and Reference Signal Waveforms

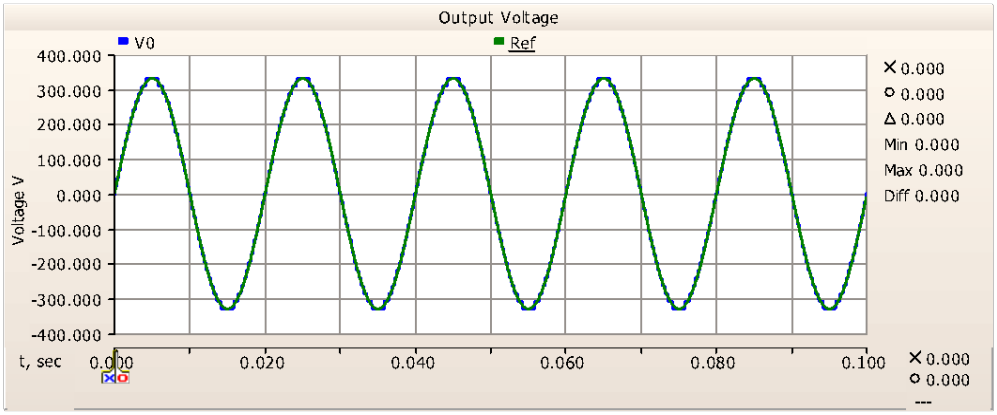


Figure 3.9

Load Current

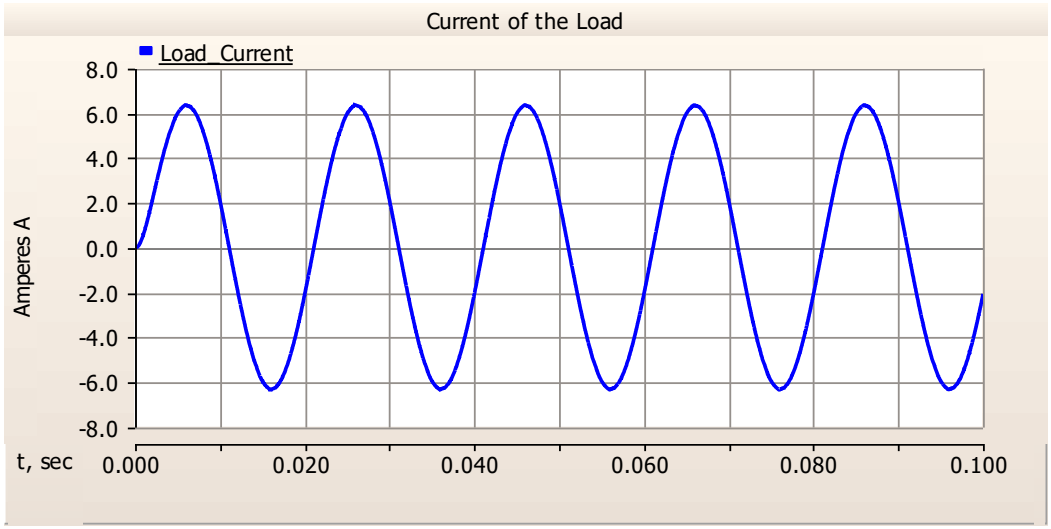
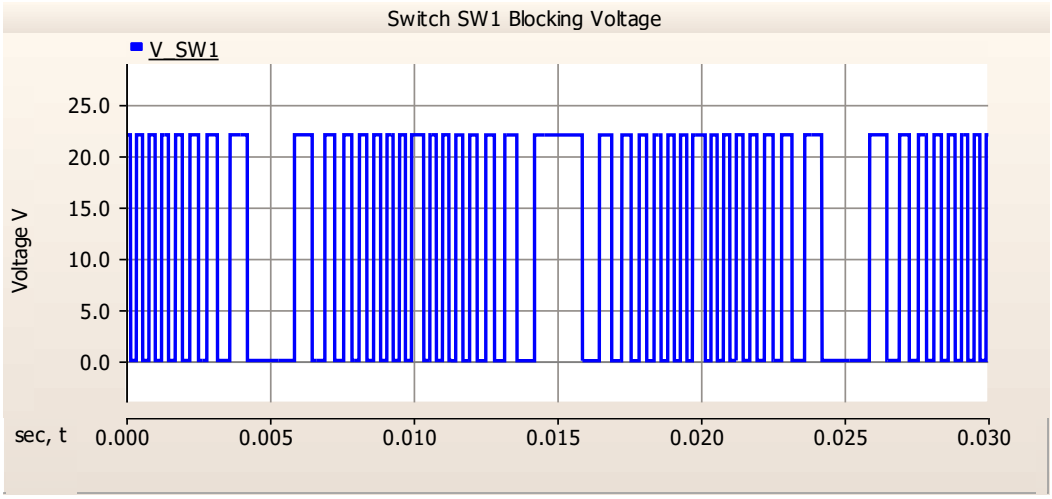


Figure 3.8 displays the output voltage, the green line represents the reference signal, which is sine wave pattern, while the blue line is the stepped output voltage of the inverter with incremented steps, which aligns perfect with the green line of the reference waveform.

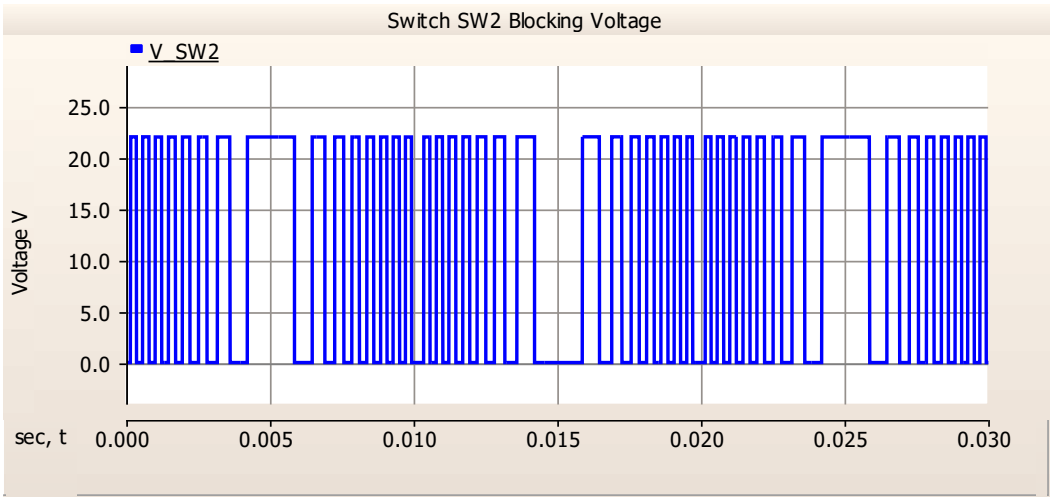
Figure 3.9 is the load output current waveform; it has good quality with less to no distortions.

Figure 3.10

SW_1 to SW_{12} Standing Voltages

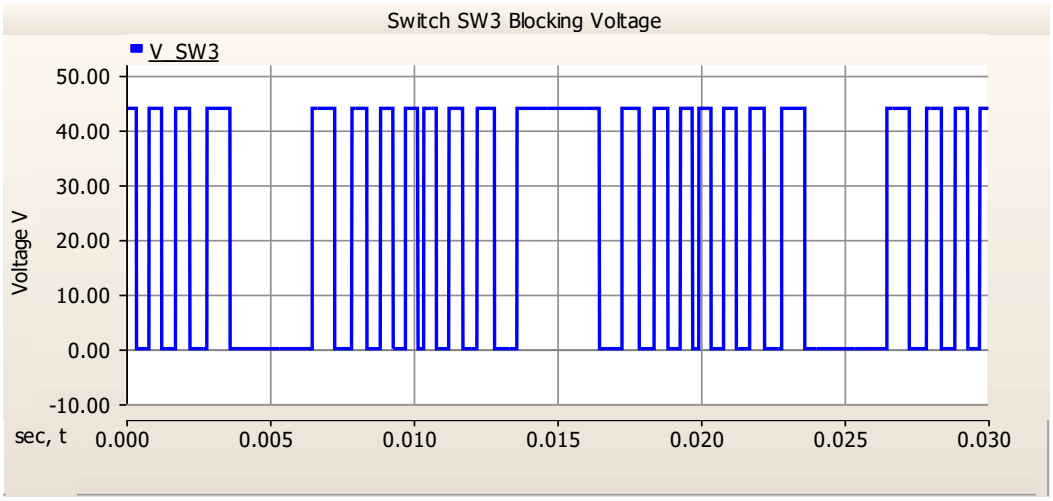


(A)

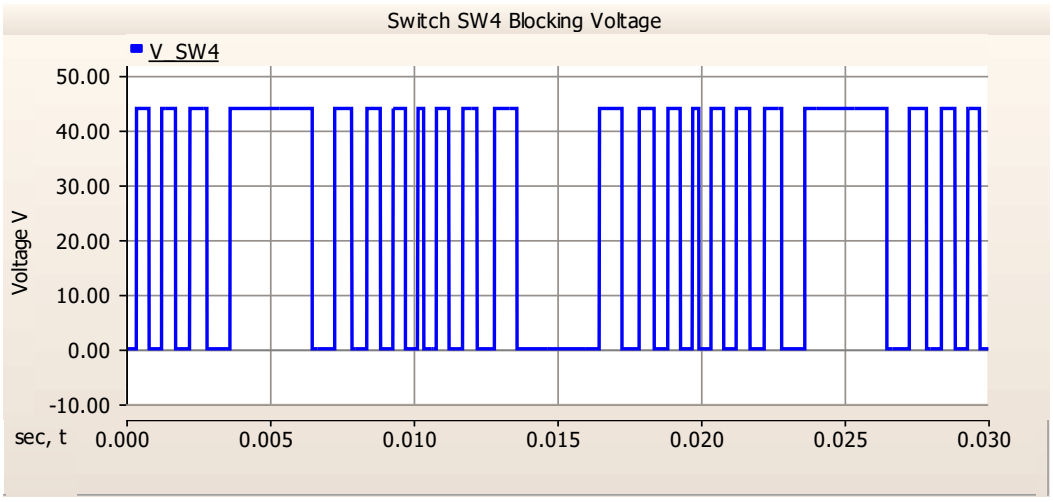


(B)

Figure 3.10(a) displays the standing voltage for switch SW_1, and Figure 3.10(b) is for switch SW_2 both have 22V standing voltage. As can be seen when switch SW_1 has gated on, for switch SW_2 it is gated off in that period, to avoid short circuit.

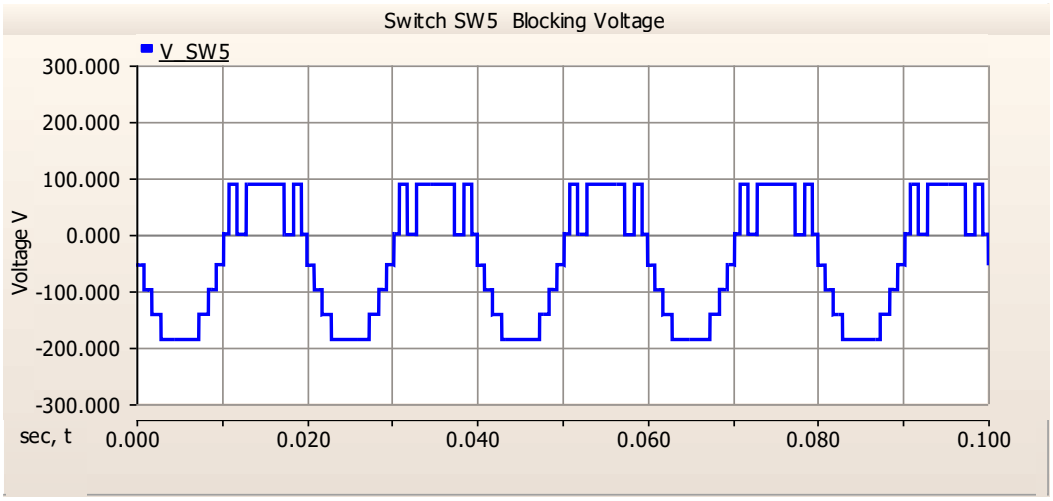


(C)

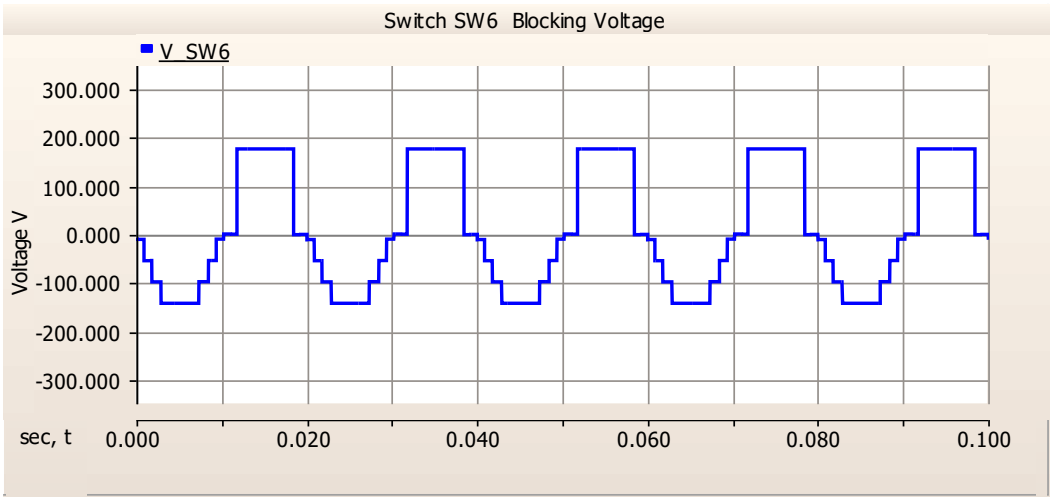


(D)

The switching gate for switch SW_3 and SW_4 is displayed in Figure 3.10(c) and Figure 3.10(d) respectively, they have 44V standing voltage. Same as switch SW_1 and switch SW_2 they not gated on simultaneously.

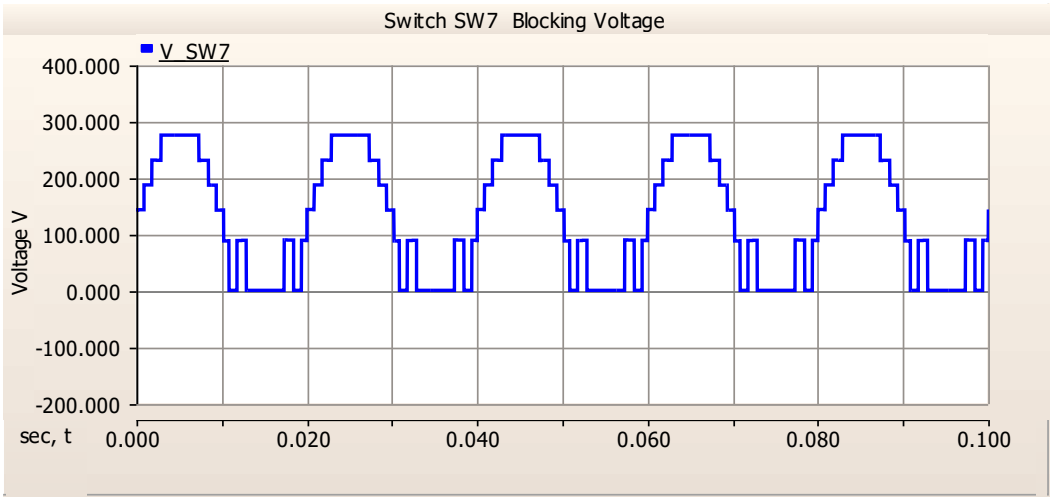


(E)

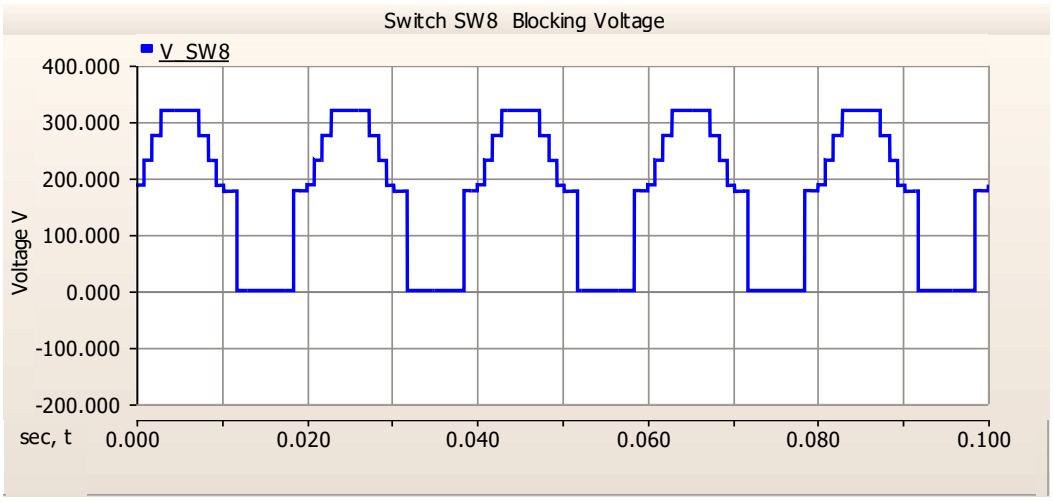


(F)

The standing voltages for switches SW_5 and SW_6 shown in Figures 3.10(e) and 3.10(f), demonstrates that they bidirectional switches, from the graph they able to block voltage both polarities. Switch SW_5 has standing voltage of 88V, switch SW_6 has standing voltage of 176V. As can be seen from the graph the second half cycle they active from 0.01to 0.02 seconds.

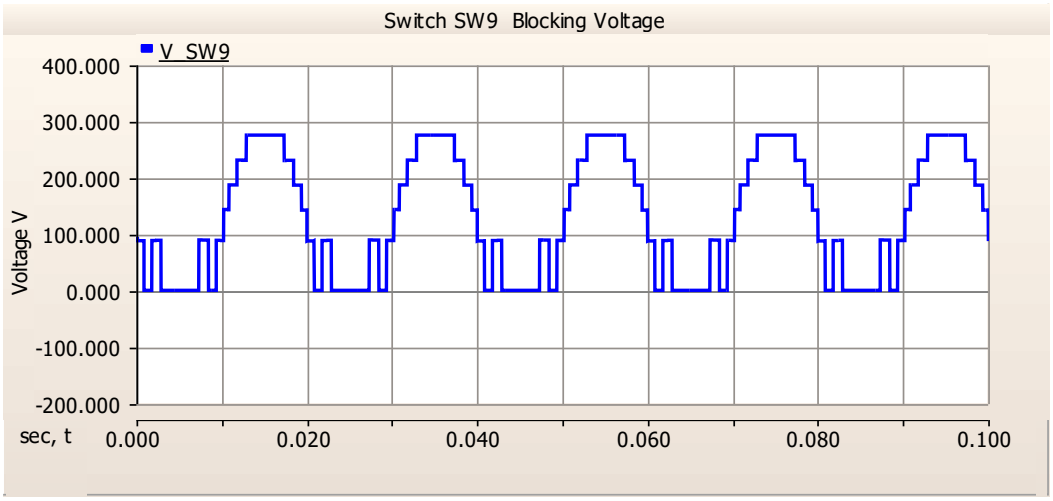


(G)

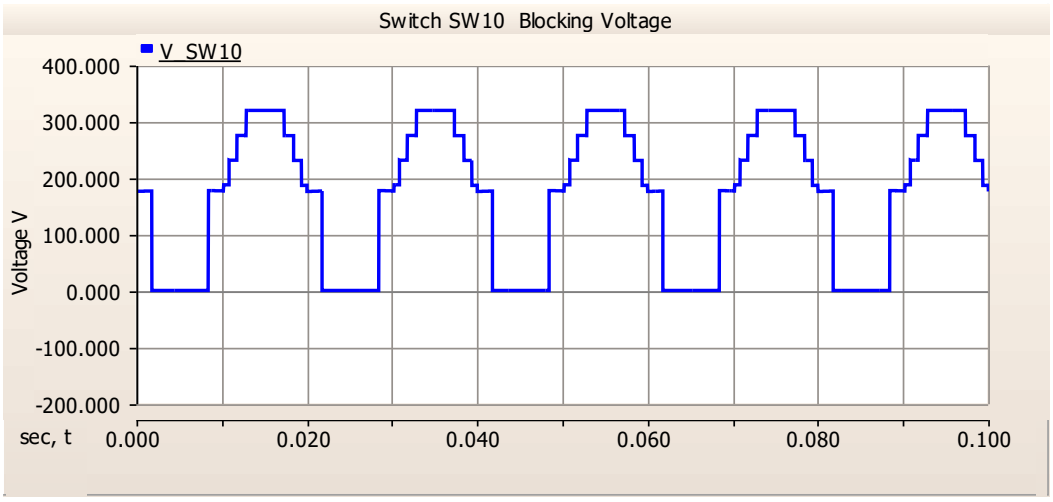


(H)

The graphs above, Figure 3.10(g) and 3.10(h) displays a period of 0.1 seconds which is five periods. For switches SW_7 and SW_8, they are inactive in the positive cycle. Switch SW_7 has 88V standing voltage and switch SW_8 has 176V standing voltage, validating the theoretical calculation.

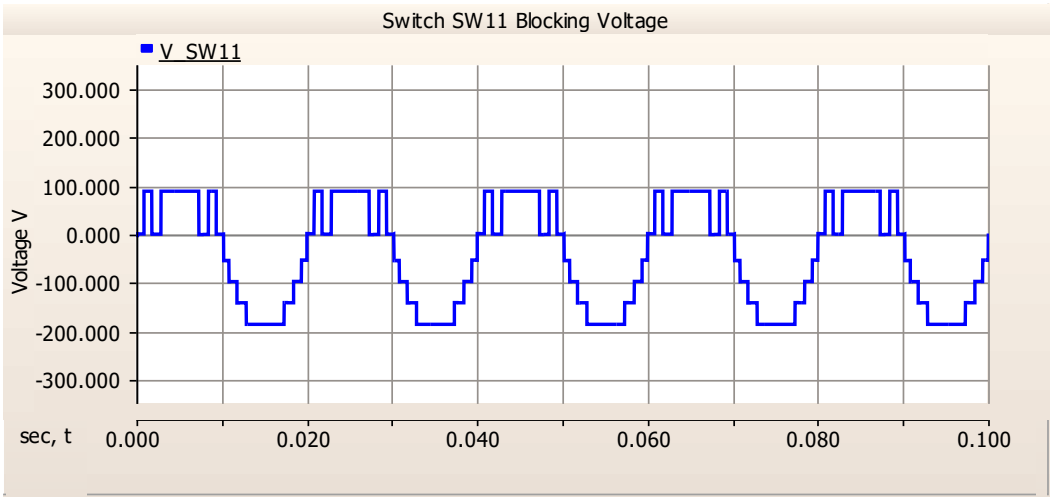


(I)

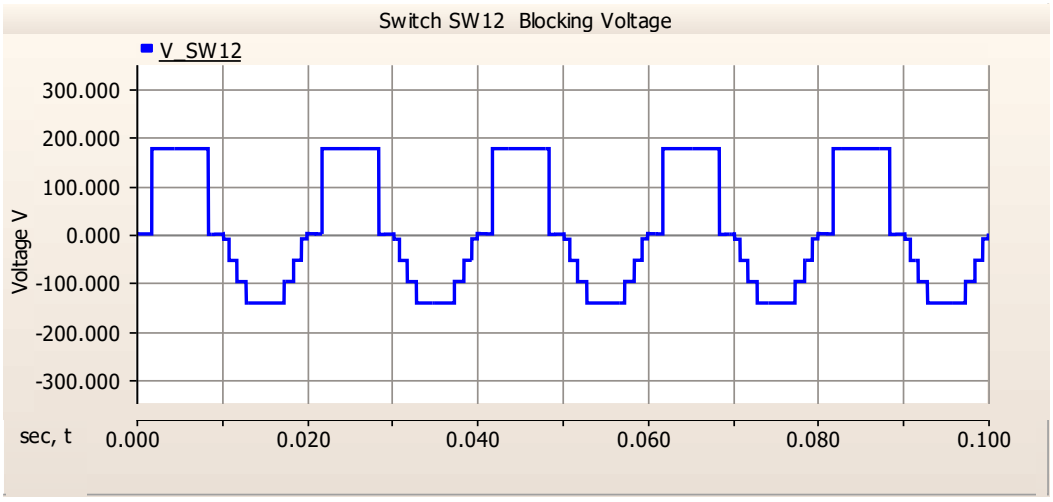


(J)

Switch SW_{10} has higher standing voltage, 176V than switch SW_9 which is 88V. The negative cycle they are inactive as illustrated in Figure 3.10(i) and Figure 3.10(j).



(K)



(L)

Figure 3.10(k) and 3.10(l) displays the standing voltages for switch SW_{11} and switch SW_{12} both are bidirectional switches. Illustrated in the graph the highest point of the voltage standing voltage of 88V for switch SW_{11}, and for switch SW_{12} it is 176V.

The comparison of the standing voltages in the above graph results shows the different switches ratings required to construct the inverter system, with some switches having higher voltage ratings than others. SW_3 rating should handle a voltage of 44V, while SW_1 is 22V.

CHAPTER IV
Conclusion and Future Works

Conclusion

Power electronics devices have surged in relevance over the last few decades as a crucial tool for regulating electrical power throughout every power category.
The advancement in technology recent years have elevated the interest in the field of renewable energy sources which made multilevel inverter important research. Renewable energy sources generate dc voltage, therefore power electronic is needed to change the dc voltage into ac for applications or connect to the grid. Conventional H-bridge inverter requires lots of devices to generate higher voltages, increasing the losses and cost. This thesis focuses on designing a symmetric and asymmetric DC source analysis of an improved single-phase H-bridge multilevel inverter, targeting higher stepped output voltage levels, less components used and better efficiency.

The contents of the thesis are split into four sections. Chapter 1 is the introduction, the aim, objective, and limitations of the proposed topology. Chapter 2 is the literature review and study on multilevel inverters and DC renewable energy source, their classification, topologies and control methods. Chapter 3 is the proposed topology of single-phase H-bridge multilevel inverter, analysis of symmetric and asymmetric configuration, and the results of the simulation. Lastly, chapter 4 covers the conclusion and future works.

The novelty of the proposed topology is that it’s able to deliver 31 stepped output voltage levels, while employing 12 power switches and 6 input sources. Four of those switches are bidirectional switches, which can block voltage both polarities. It is better improved inverter of the traditional H-bridge inverter, with 2 extra H-bridge units to the upper and lower section of the circuit, to achieve both positive and negative levels and two input sources for the extra H-bridge units.

The thesis did investigation on the symmetric and asymmetric setups of the proposed and the differences; the symmetric analysis delivered less voltage steps in comparison while utilizing the same components. Symmetric setup was able to produce 9 voltage levels while asymmetric analysis' results showed higher voltage steps employing a variety of dc sources; it was able to generate 31 levels. PSCAD

software is employed for the simulation of the project. The simulation parameter, the initial input dc source is given as 22V which equates every stepped level is ±22V. The peak voltage for the simulation should be 330V for the 31 stepped levels. Selected control technique was the FFCM which has fewer switching losses and other benefits over others. The outputs results are analyzed for the proposed asymmetric topology, it illustrated a better-quality output waveform. Stepped output voltage, load current and the standing voltages are given.

The results of the output voltage step is illustrated in the results along with the reference voltage waveform in same graph, green line waveform for the reference and blue line for the stepped output voltage. It shows it aligns with the sine wave of the reference signal The amplitude is 330V. The results for the load current, it has an amplitude of 6.35A and it's better-quality waveform with no distortions.

The standing voltages results for the switches validate the theoretical principle. The blocking voltage of the inverter is 1188V, it is the summation of all the standing voltages of the switches.

The contribution of the thesis, the proposed inverter adds further advancement on the rising field of renewable energy technology, an inverter that generates higher voltage levels, with better power quality, reduced losses and cost effective.

Future Works

Consideration for better improvement of the project, the topology can be designed into three-phase multilevel inverter for renewable energy application, which provides higher power capability and can handle unbalanced loads where power demand fluctuates, it will be suitable for industrial applications. The changes required to the design simulation will be to generate three waveforms that are shifted by 120 degrees from each other. This will require more devices, power switches and more complicated control technique.

Furthermore, generating more voltage levels higher than 31 level, while utilizing minimized components as possible and providing experimental results of it.

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Appendices

Appendix A

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